A Family of Exponential Step-Down Switched-Capacitor Converters and Their Applications in Two-Stage Converters

Song Xiong, Siu-Chung Wong, *Senior Member, IEEE*, Siew-Chong Tan, *Senior Member, IEEE*, and Chi K. Tse, *Fellow, IEEE*

***Abstract*—This paper presents a family of exponential voltage step-down switched-capacitor (ESC) converters. Considering the demand of large-voltage-gain step-down converters in the market, it is difficult to achieve the step-down requirement with good efficiency for a single-stage buck converter. The two-stage converter has been an effective solution for high-voltage-step-down applications. In this paper, making use of the large-voltage-gain conversion property of the ESC converter, a two-stage ESC-buck converter is proposed. A mathematical tool for the accurate calculation of efficiency is developed. The efficiency characteristic of the proposed ESC converter is established. Experimental efficiency measurements are carried out using the ESC converter proposed and two different types of commercially available buck converter ICs. The results show that the efficiency of the ESC-buck converter is higher than that of a single buck converter for large-voltage-gain applications.**

***Index Terms*—Exponential step-down switch-capacitor converter, large-voltage-gain-two-stage converter, switched capacitor converter.**

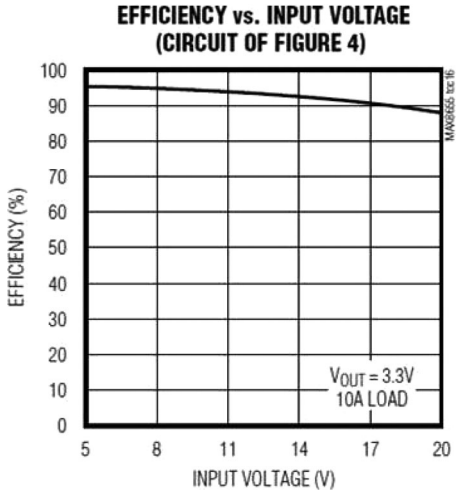

Fig. 1. Typical efficiency curve of a buck converter (From datasheet of MAX8655).

I. Introduction

THE supply voltage of modern microprocessors and application-specified integrated circuit chips is continuously reducing, targeting for less power dissipation and larger scale integration, to a level of less than 1 V [1]. The standard dc bus supply voltages are commonly 12, 24, and 48 V. Large-voltage-gain dc–dc converters for electronic product applications are therefore of high demand.

Buck-based step-down dc–dc converters are usually used in the industry as point-of-load converters, which are simple in structure and mature in control methods, for achieving the required voltage step-down conversion [2]–[5]. For applications in modern electronic devices, high power density and high efficiency are among the top considerations. Increasing the switching frequency is an effective way to reduce the size of bulky elements such as magnetic components and charge storage capacitors. However, the switching loss of the buck converter with large-voltage-gain increases dramatically due to its extreme small duty cycle $D = \frac{V_{\rm out}}{V_{\rm in}}$, which not only limits the switching frequency, but also complicates its implementation [6]–[8]. Moreover, it deteriorates the dynamic performance of the converter and further reduces its efficiency due to the very short on-time and very long freewheeling time within the switching cycle. The drawback can be readily observed from the efficiency versus input voltage curves, as shown in Fig. 1, of a buck converter available in the market, where the converter efficiency decreases rapidly with increasing input voltage. Converters with transformers would be a good choice to achieve large-voltage-gain conversion. However, this decreases the power density and increases the cost, conflicting the requirement of modern electronic applications. As a matter of fact, the single buck-type converter may not be able to satisfy the requirements of applications requiring large-voltage-gain conversion.

Considering the size and weight requirements in modern electronic products, a good candidate power converter is the switched-capacitor (SC) dc–dc converter, which has the advantages of small size, light weight, high efficiency and high power density [9]–[16]. SC converters, which consist exclusively of

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power switches and capacitors, remove magnetic components from their topologies, become very suitable for integrated circuit (IC) implementation [17]. However, SC dc–dc converters cannot achieve high efficiency with voltage regulation [10]–[16], [18]–[21], which limits their applications.

The limitations of the single-stage converters have spurred the interests in developing a new kind of high-voltage-gain two-stage dc–dc converters [6]–[8], [22]–[29]. Such a converter is made up of a first-stage SC converter, followed by a second-stage buck converter. For this two-stage SC-buck converter, the first-stage SC converter steps down the input voltage while the second-stage buck converter mainly regulates the output voltage. This two-stage converter has an overall efficiency possibly higher than the single buck converter, because the second-stage buck converter runs at a lower input voltage with higher efficiency. The energy saved by the efficiency improvement of the second stage makes room for the first-stage converter to convert the voltage down. It is obvious that if the energy saved by the second-stage buck converter is higher than the energy loss consumed by the first-stage converter, then the overall efficiency will be improved. Recalling the consideration on power density, the possibility of integrated circuit implementation for the SC stage, and high switching frequency with robust control for the buck stage, it is highly possible that the overall two-stage SC-buck converter can be small in size and light in weight.

Although SC converter products with efficiency as high as 98%, such as LTC1044, MAX1044, SI7660, GS7660, etc., are available in the market, the rated power is always very low, which limits their applications in two-stage converters. Moreover, most SC converters embedded in a two-stage converter design use a large number of switches when the voltage conversion ratio is high [22], [27]–[30]. Besides, first-stage SC converter with fixed conversion ratio in paper [6] also deteriorate its advantages when the input voltage is further increased. Therefore, it is necessary to develop a type of SC converters with fewer switches and high conversion efficiency. This paper will propose a family of exponential voltage step-down switched-capacitor (ESC) converters to satisfy the requirements. The ESC converter proposed will allow the creation of a two-stage ESC-buck converter which works at a higher input voltage with high efficiency than a single-stage buck converter.

Efficiency analysis is important for the optimal design of SC converters. SC converter circuits with different voltage conversion ratios can normally be built with energy transfer using either series or parallel connection of capacitors from the input power source to the output loading. An SC converter with a parallel-charging of capacitors from an input voltage source and subsequently series-discharging to an output load can provide an effective voltage step-up conversion [31]. Conversely, a series-charging and parallel-discharging SC converter can provide an effective voltage step-down conversion [28]. To obtain the efficiency information for a number of capacitors, linearity in the capacitor voltage has been assumed by designing the converter using a switching frequency much higher than the reciprocal of the time constant of the switch topology [32]. The traditional state-space averaging technique used in PWM converters can be readily applied. However, the technique cannot be used for the analysis when the time constants of the state variables are close to the switching period of the SC converter. To solve this problem, the flying capacitors can be designed with identical components and the SC converter circuit can thus be readily simplified in its state-space operations as a set of first-order RC networks of voltage to capacitor energy transfer or a set of second-order RC networks of capacitor to capacitor energy transfer. An average-current-based conduction loss model for the SC converter has been proposed in [33], [34]. Using some approximations, the model has successfully reduced each operation state of the SC converter into an equivalent first-order RC network which greatly simplifies the efficiency analysis of the original SC converter. Alternatively, without the calculation of the averaged current, RC networks of up to second order are used for the calculation of the efficiency of SC converters in [28], [31], [35]. However, the family of ESC converters proposed in this paper has state-space RC subcircuits of order higher than two depending on the voltage step-down requirement. Therefore, a mathematical tool for the accurate calculation of efficiency of the ESC converter will be developed in this paper.

As previously mentioned, the efficiency of the two-stage converter can be higher than a single-stage buck converter. However, no study has been conducted to identify the exact requirements for improving the overall efficiency of the two-stage converter, and to quantify the improvement achievable over a single-stage buck converter. This paper will answer these questions by the mathematical tool developed.

This paper is organized as follows. Section II proposes a family of ESC converters and describes their working principle. Section III proposes a mathematical tool for the fast calculation of efficiency of the ESC converter. Section IV introduces the two-stage ESC-buck converter. Section V shows the area of improvements of the two-stage ESC-buck converter. Section VI shows the experimental results of the ESC-buck converter. Section VII concludes this paper.

II. Family of Exponential Step-Down SC Converters

A second-order SC converter will be introduced in the next section. Subsequently, the converter will be generalized to a family of exponential SC converters.

A. Topology and Operation of a Second-Order Exponential SC Converter

An SC step-down converter as shown in Fig. 2(a) is proposed in this paper. It is a second-order flying-capacitor converter which has a voltage transfer ratio of $V_o = \left(\frac{1}{2}\right)^2 V_{\text{in}}$. Comparing with the SC converters in [28] and [30], the ESC converter introduced in the next section which is to be generalized uses fewer switches.

For this proposed converter, we use the switch timing diagram shown in Fig. 2(b), where the first stage timing (ϕ_{10}, ϕ_{11}) has a phase delay of $\frac{T}{4}$ relative to the second stage timing (ϕ_{20}, ϕ_{21}). Fig. 3 shows the four main operating states of the SC converter, neglecting the much shorter deadtime state as indicated in Fig. 2(b). With reference to Fig. 3, the flying capacitor C_{f1}

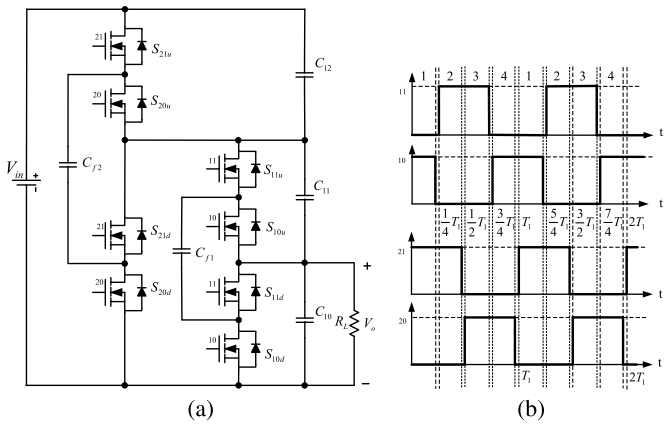


Fig. 2. Proposed SC converter and its timing diagram. (a) Topology. (b) Timing diagram.

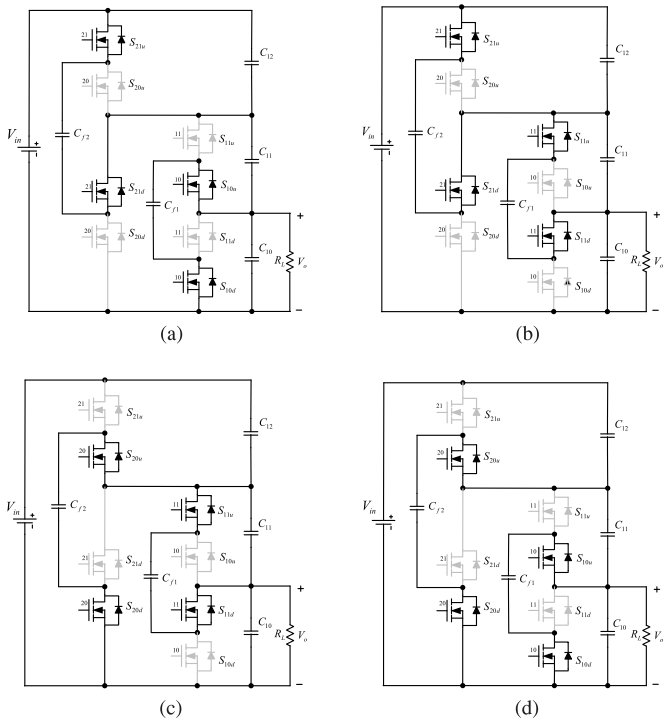


Fig. 3. Four main states of the proposed SC converter. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

TABLE I
SIMULATION PARAMETERS OF THE PROPOSED SC CONVERTER

Switching frequency f_s	200 kHz
flying caps C_{f1}, C_{f2}	94 μF
Capacitors C_1, C_2, C_3	188 μF
Input voltage	20 V
R_L	10 Ω
Switches	NTMFS4897

is in parallel with C_{11} in states 2, 3 and with C_{10} in states 1, 4. While the flying capacitor C_{f2} is in parallel with C_{12} in states 1, 2 and with the input of the next stage circuitry in states 3, 4.

A SPICE model of the second-order SC converter with simulation parameters shown in Table I is built. The simulation result shown in Fig. 4 gives the detailed waveforms of capacitor voltages of the converter.

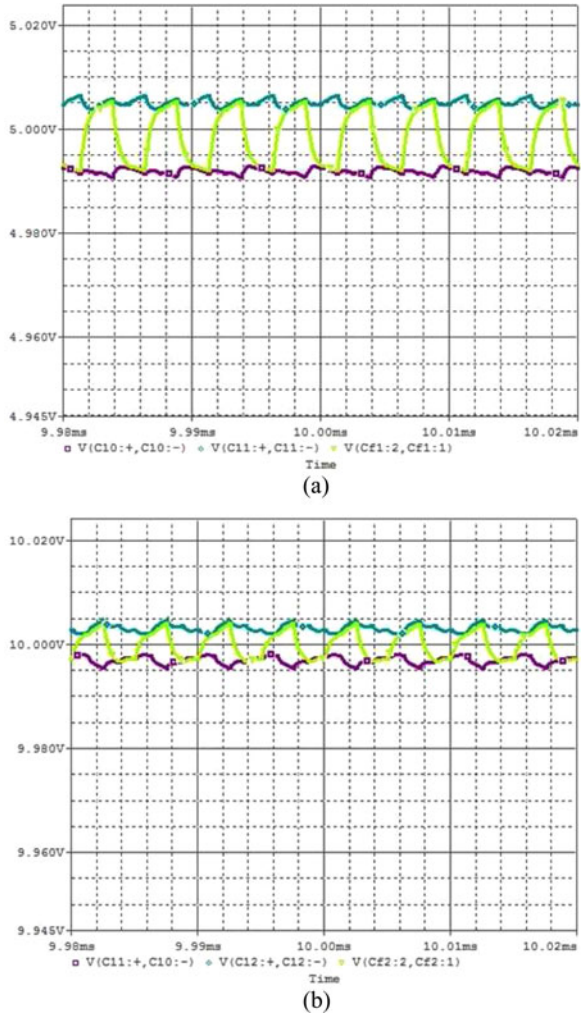


Fig. 4. Simulation waveforms of each capacitor of the proposed SC converter. (a) Waveforms from top to bottom: V_{11}, V_{f1}, and V_{10}. (b) Waveforms from top to bottom: V_{12}, V_{f2} and $V_{11} + V_{10}$.

B. Generalization to Higher Order Exponential Step-Down SC Converter

By comparing the topology of Fig. 2 with the basic structure shown in Fig. 5(a) [9], an extended structure can be identified as shown in Fig. 5(c) which allows repeated applications to form a series of exponential SC converters. Fig. 6 shows the second-order and third-order exponential SC converters. In general, by cascading $n-1$ extended structures and a basic structure, an nth-order ESC converter is formed with an output voltage given by

$$V_o = \left(\frac{1}{2}\right)^n V_{\text{in}}. \tag{1}$$

In this paper, the interleaved control method shown in Fig. 2(b) can be easily generalized to the nth-order ESC converter. Each structure of the ESC converter is switching at a

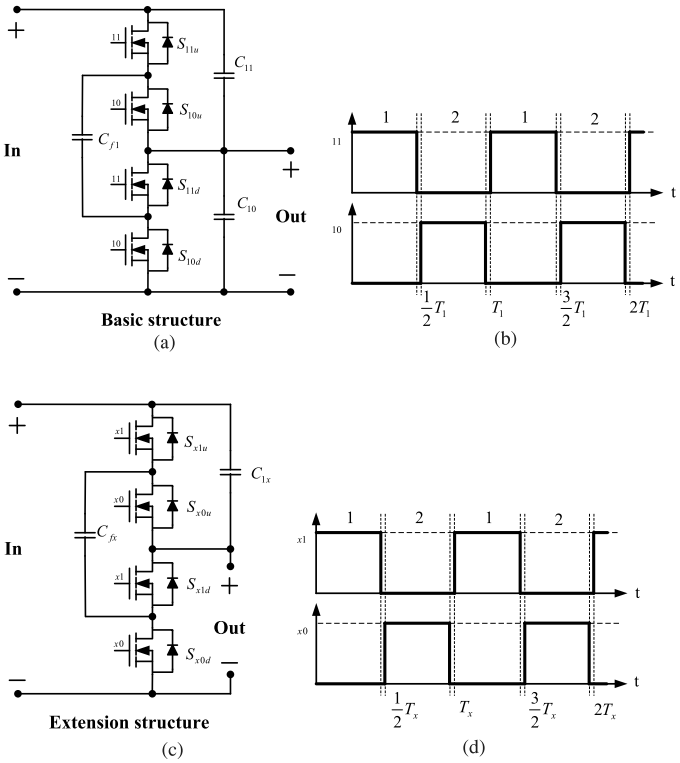


Fig. 5. Generalized exponential SC converter's structures. (a) Basic structure. (b) Basic structure timing diagram. (c) Extension structure. (d) Extension structure timing diagram.

period of T. The timing (ϕ_{k1}, ϕ_{k2}) of the kth structure has a phase delay of $\frac{T}{2n}$ relative to the timing of the $(k-1)$th structure, where $k = 2, 3, \ldots, n$.

III. Efficiency Analysis of the ESC Converter

Efficiency analysis is important for the design of an SC converter. Usually, state-space averaging is effective for the analysis of pulse-width-modulated power electronic converters, where the time constants of state variables are designed to be much longer than the reciprocal of the switching frequency and can be regarded as piece-wise linear within a switching period [32]. The piece-wise-linear property of the state variables allows local linear averaging within each substate followed by an overall duty-cycle-weighted averaging of all substates to obtain an averaged system equation for a switching period. The state-space-averaged system equation is often considered as being continuous for the frequencies interested. However, state-space averaging cannot be directly applied to the SC converter for the reason that the time constants of state variables are close to the switching period, and therefore, state variables are exponentially varying. More general techniques for the calculation of steady-state solution of power converters can be found in [36] and [37]. The steady-state solution can be used for the calculation of converter efficiency, small signal response, or subsequent circuit-parameter optimization. The methods start with the state-space formulation for each operating mode within a switching period and look for steady-state solutions using some closed-form solutions which are solved numerically. Numerical

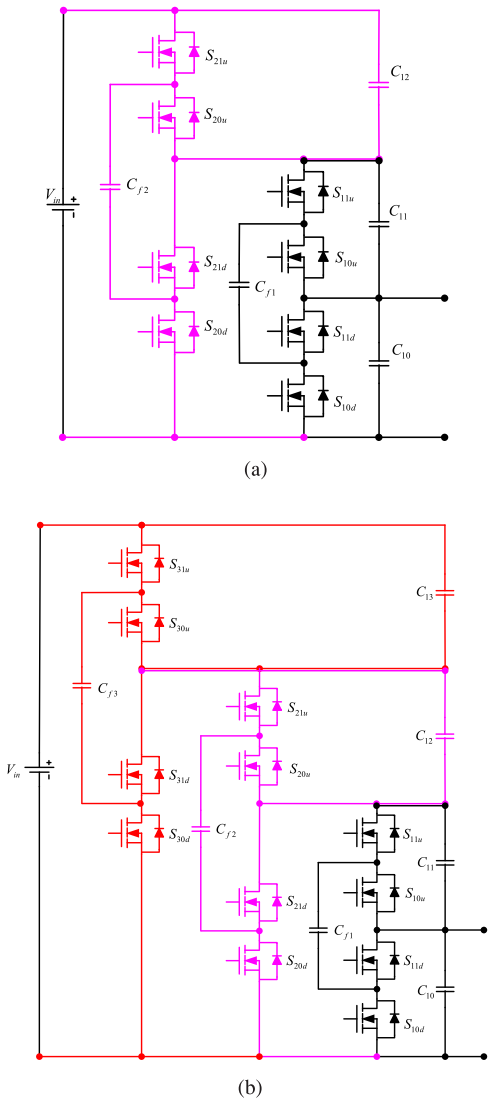


Fig. 6. Generalized exponential SC converter. (a) Second-order exponential SC converter. (b) Third-order exponential SC converter.

calculation can be time consuming while analytical calculation can be difficult to obtain [36]. Moreover, the technique proposed in [37] optimizes for efficiency and output ripples by selecting a set of best switching time instances within a switching cycle under different loading conditions. The procedure is, however, rather complicated in both analytical and numerical calculations for the SC converter proposed in this paper.

Although a full analytical equation can be difficult to obtain, a discrete-time analysis can readily be formulated for high-order capacitor circuits which can be difficult to analyze using methods in [28], [31], and [33]–[37]. The discrete time analysis can be accurate by using a sufficiently small discrete time interval. The formulation will be illustrated as follows.

Considering the time-varying capacitor voltage as shown in Fig. 7, the state equation is given as

$$I(t) = C\frac{dV(t)}{dt} \tag{2}$$

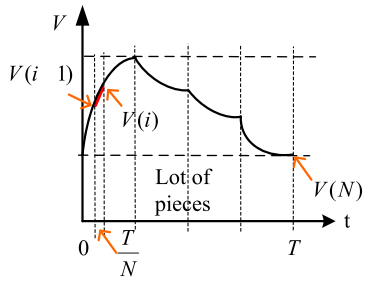


Fig. 7. Capacitor voltage waveform.

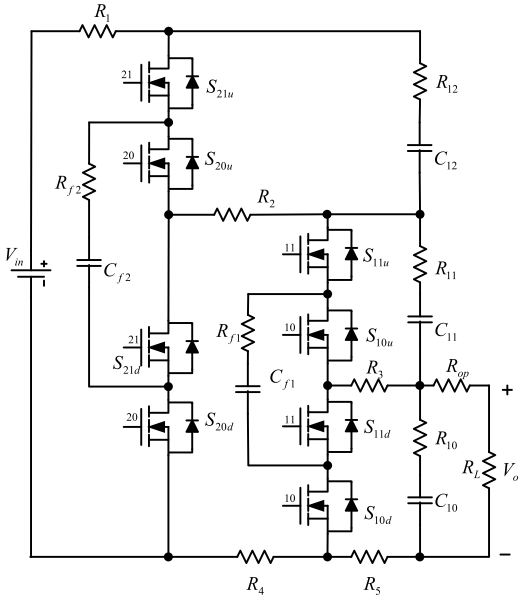


Fig. 8. Second-order ESC converter with consideration of the ESRs.

which can be approximated as

$$I(t) = C\frac{\Delta V(t)}{\Delta t} \tag{3}$$

for an interval $\Delta t = \frac{T}{N}$, where T is the switching period and N is a sufficiently large integer.

Within a period, the capacitor voltage is represented in the discrete-time domain with equal spacing Δt, as a sequence of $\{V(1), V(2), \ldots, V(i), \ldots, V(N+1)\}$. Using (3), a discrete-time state equation can be written as

$$V(i) = V(i-1) + R_{\text{eq}} I(i) \tag{4}$$

where

$$R_{\text{eq}} = \frac{T}{NC}. \tag{5}$$

To illustrate the discrete-time state-space analytical technique, the second-order ESC converter will be used as an example circuit in the next section.

A. Analysis of the Second-Order ESC Converter

The second-order ESC circuit shown in Fig. 8 will be analyzed in this section. All effective resistors including the capacitor ESRs are incorporated in the analysis for better accuracy in the

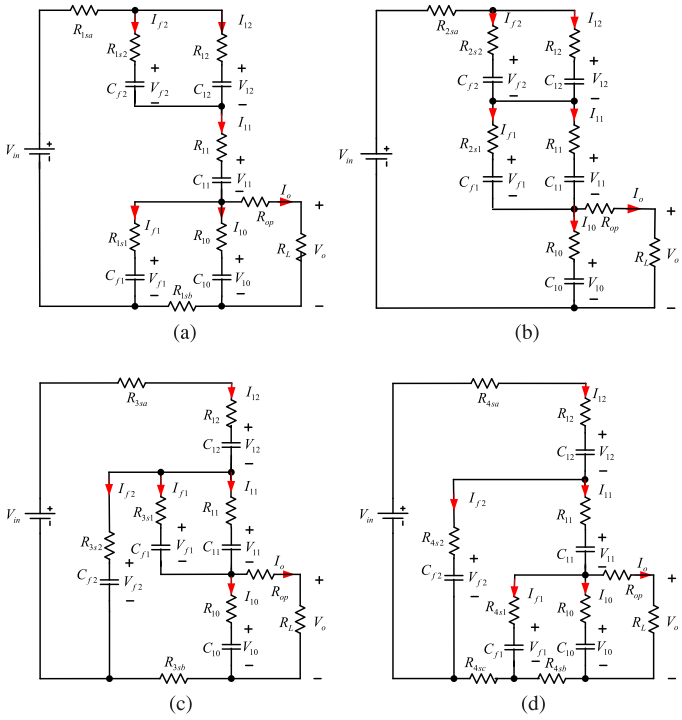


Fig. 9. Equivalent circuit of the four-stage of operation. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

efficiency calculation. For each discrete time i, the state equation is defined as

$$\mathbf{V}(i) = \mathbf{V}(i-1) + \mathbf{R}_{\text{eq}}\mathbf{I}(i) \tag{6}$$

where

$$\mathbf{V}(i) = [\,V_{10}(i), V_{11}(i), V_{12}(i), V_{f1}(i), V_{f2}(i)\,]^T \tag{7}$$

and

$$\mathbf{I}(i) = [\,I_{10}(i), I_{11}(i), I_{12}(i), I_{f1}(t), I_{f2}(i)\,]^T \tag{8}$$

are the state-column vectors at time i, and

$$\mathbf{R}_{\text{eq}} = \begin{bmatrix} R_{\text{eq}10} & 0 & 0 & 0 & 0 \\ 0 & R_{\text{eq}11} & 0 & 0 & 0 \\ 0 & 0 & R_{\text{eq}12} & 0 & 0 \\ 0 & 0 & 0 & R_{\text{eq}f1} & 0 \\ 0 & 0 & 0 & 0 & R_{\text{eq}f2} \end{bmatrix} \tag{9}$$

is the equivalent-resistance diagonal matrix with element $R_{\text{eq}xx} = \frac{T}{NC_{xx}}$ given by (5), where the subscript $xx = 10, 11, 12, f1$, and $f2$. The ESC converter goes through four states in its normal operation, as shown in Fig. 9. For each state $k = 1, 2, 3, 4$, a general state equation can be formulated as

$$\mathbf{V}(i) = \mathbf{A}_k\mathbf{V}(i-1) + \mathbf{B}_k\mathbf{U}_k, \tag{10}$$

where

$$\mathbf{A}_k = \begin{bmatrix} a_{k,11} & a_{k,12} & a_{k,13} & a_{k,14} & a_{k,15} \\ a_{k,21} & a_{k,22} & a_{k,23} & a_{k,24} & a_{k,25} \\ a_{k,31} & a_{k,32} & a_{k,33} & a_{k,34} & a_{k,35} \\ a_{k,41} & a_{k,42} & a_{k,43} & a_{k,44} & a_{k,45} \\ a_{k,51} & a_{k,52} & a_{k,53} & a_{k,54} & a_{k,55} \end{bmatrix} \tag{11}$$

$$\mathbf{B}_k = \begin{bmatrix} b_{k,11} & b_{k,12} \\ b_{k,21} & b_{k,22} \\ b_{k,31} & b_{k,32} \\ b_{k,41} & b_{k,42} \\ b_{k,51} & b_{k,52} \end{bmatrix} \tag{12}$$

and

$$\mathbf{U}_k = \begin{bmatrix} V_{\text{in}}(i) \\ I_o(i) \end{bmatrix}. \tag{13}$$

The matrix elements can be readily determined by nodal analysis for each state and therefore their expressions are omitted for brevity.

The number M of time points for each state is equally assigned, such that $N = 4M$. The end point of state variables of each state can be calculated by successive applications of (10) for each time point. Eventually, we have for each k,

$$\begin{aligned} \mathbf{V}(kM) = {} & \mathbf{A}_k^M \mathbf{V}((k-1)M) \\ & + (\mathbf{A}_k - \mathbf{I})^{-1}(\mathbf{A}_k^M - \mathbf{I})\mathbf{B}_k\mathbf{U}_k. \end{aligned} \tag{14}$$

At steady state, the condition

$$\mathbf{V}(4M) = \mathbf{V}(0) \tag{15}$$

holds. Hence, using (15), the steady-state solution is obtained as

$$\begin{aligned} \mathbf{V}(0) = {} & (\mathbf{I} - \mathbf{A}_1^M \mathbf{A}_2^M \mathbf{A}_3^M \mathbf{A}_4^M)^{-1} \\ & \times \Big[\mathbf{A}_4^M \mathbf{A}_3^M \mathbf{A}_2^M (\mathbf{A}_1 - \mathbf{I})^{-1}(\mathbf{A}_1^M - \mathbf{I})\mathbf{B}_1\mathbf{U}_1 \\ & + \mathbf{A}_4^M \mathbf{A}_3^M (\mathbf{A}_2 - \mathbf{I})^{-1}(\mathbf{A}_2^M - \mathbf{I})\mathbf{B}_2\mathbf{U}_2 \\ & + \mathbf{A}_4^M (\mathbf{A}_3 - \mathbf{I})^{-1}(\mathbf{A}_3^M - \mathbf{I})\mathbf{B}_3\mathbf{U}_3 \\ & + (\mathbf{A}_4 - \mathbf{I})^{-1}(\mathbf{A}_4^M - \mathbf{I})\mathbf{B}_4\mathbf{U}_4\Big]. \end{aligned} \tag{16}$$

The time points of state variables within a switching cycle at steady state can readily be calculated using (16) and (10). It should be noted that the aforementioned procedure is much simpler than that used in [37] for obtaining the steady-state solution, and the calculated results will be used for the calculations of the loss in each resistor and the output power.

1) *Loss in Each Resistor*

$$E_R = f_s \sum_{n=1}^{N} R_i I_R^2(n) \frac{T}{N} = \frac{1}{N} \sum_{n=1}^{N} R I_R^2(n). \tag{17}$$

2) *Output Power*

$$E_o = f_s \sum_{n=1}^{N} V_{10}(n) I_o \frac{T}{N} = \frac{1}{N} \sum_{n=1}^{N} I_o V_{10}(n). \tag{18}$$

So, the overall efficiency can be calculated as

$$\eta = \frac{E_o}{E_o + \sum E_R} \times 100\% \tag{19}$$

where $\sum E_R$ is the sum of all losses in resistors including the losses in R_{dson} of the switches.

TABLE II
EXPERIMENT AND SIMULATION PARAMETERS

type	Experiment	Calculation
Input voltage	20 V	20 V
Switches	NTMFS4897	$R_{dson} = 1.12$ mΩ
C_{10}	Murata $6 \times 47\mu$F	From measurement
C_{11}, C_{12}	Murata $4 \times 47\mu$F	and confirmed
C_{f1}, C_{f2}	Murata $3 \times 47\mu$F	with datasheet
R_1, R_{op}	NA	20 mΩ, 3 mΩ
$R_2 \ldots R_5$	NA	5 mΩ, 5 mΩ, 7 mΩ, 8 mΩ

B. Experiment Verification

In order to verify the validity of the discrete-time calculation method, SPICE simulation waveforms and experimental measurements based on the second-order ESC converter are performed using the parameters given in Table II. Fig. 10 shows comparisons of the waveforms from SPICE simulations and discrete-time calculations. The waveforms match well if we ignore the short-state transition dead times which are not considered by the discrete-time calculations. Fig. 11 shows a comparison of the results from the experiment and discrete-time calculations. The experimental results match well with the calculations.

IV. EXPONENTIAL SC-BUCK CONVERTER

A family of ESC converters have been introduced in Section II. It can be readily seen that the ESC converters have a fixed conversion ratio of $(\frac{1}{2})^n$. The lack of voltage regulation will dramatically limit their applications. While papers [6], [7], [22]–[24], [26]–[28] show that a two-stage converter can have a better efficiency than that of a single buck converter for large-voltage-gain conversion applications. The voltage regulation can be obtained from a second-stage buck converter. Here, the ESC converter can be used for this two-stage converter application, where the voltage conversion ratio is exponentially selectable and the conversion efficiency is properly maintained.

In this paper, the ESC converter is used as the first-stage converter of the two-stage converter. Fig. 12 shows an example of the second-order ESC-buck converter. The first stage is a second-order ESC converter to step-down the input voltage to its quarter to improve system efficiency, while the second-stage buck converter regulates the output voltage.

In this two-stage ESC-buck converter topology, the first-stage ESC converter can have a freedom of choosing an order which suits best the application requirements.

V. THEORETICAL POSSIBILITY OF EFFICIENCY IMPROVEMENTS OF A TWO-STAGE CONVERTER OVER A SINGLE-STAGE CONVERTER

In a two-stage converter, the overall efficiency is the product of the efficiencies of the two stages. Denoting the first-stage efficiency as η_1, and the second-stage efficiency as η_2, the overall efficiency of the two-stage converter is $\eta_1\eta_2$. If the first-stage converter is removed, then the second-stage converter will work at an undesirably high input voltage that results in an efficiency of $\eta_2 - \Delta\eta_2$, i.e., a drop of $\Delta\eta_2$. For a more efficient two-stage

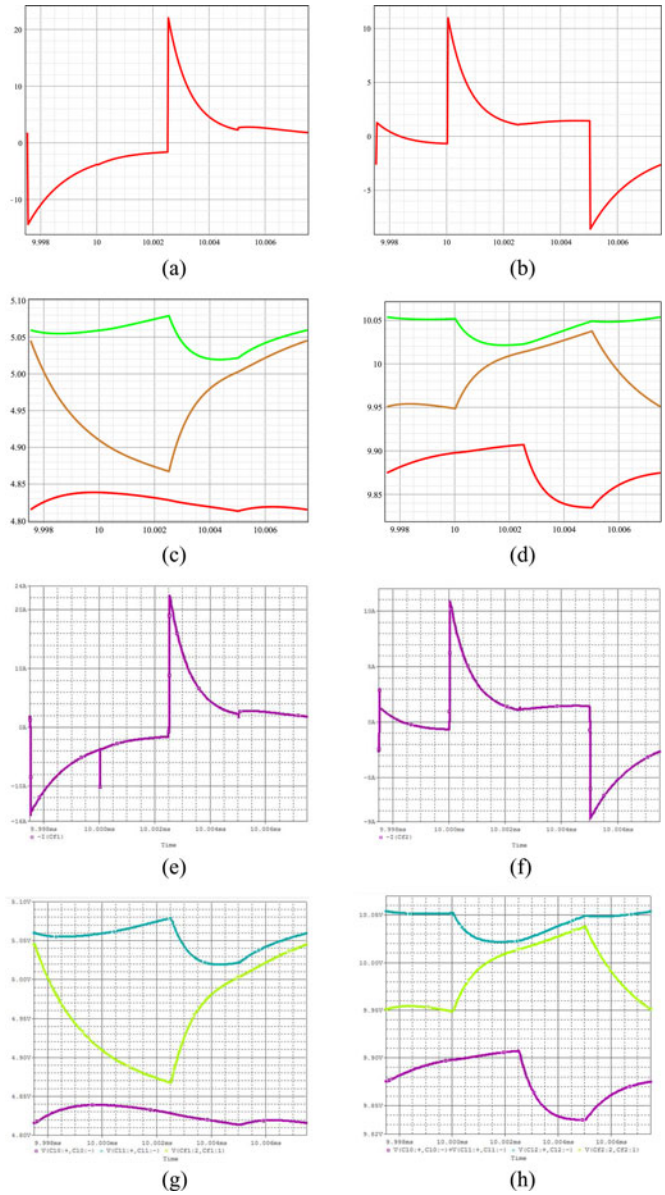


Fig. 10. Comparisons of calculated and SPICE-simulated waveforms. (a)–(d) are calculated results. (e)–(h) are SPICE simulated results. (a) I_{f1}. (b) I_{f2}. (c) V_{11},V_{f1}, and V_{10} from top to bottom, respectively. (d) V_{12},V_{f2}, and $V_{11}+V_{10}$ from top to bottom, respectively. (e) I_{f1}. (f) I_{f2}. (g) V_{11},V_{f1}, and V_{10} from top to bottom, respectively. (h) V_{12}, V_{f2}, and $V_{11}+V_{10}$ from top to bottom, respectively.

converter, we have

$$\eta_1\eta_2-(\eta_2-\Delta\eta_2)>0, \quad \text{i.e.,}$$
$$\eta_1>1-\frac{\Delta\eta_2}{\eta_2}. \tag{20}$$

Equation (20) indicates that a larger $\Delta\eta_2/\eta_2$ gives more headroom for a two-stage converter to have efficiency improvement. This property will be used for explaining the efficiency improvement of a two-stage converter over a single-stage converter in the next section.

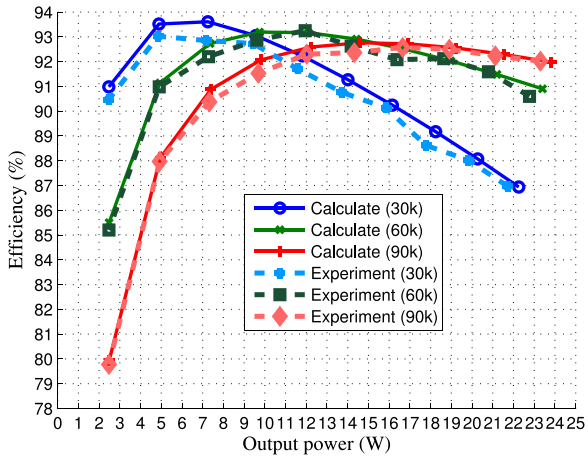


Fig. 11. Comparison of results from experiment and discrete-time calculation at three switching frequencies.

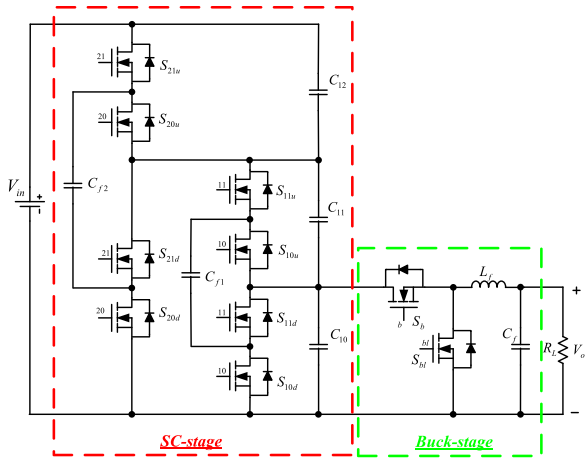


Fig. 12. Second-order ESC-buck converter.

TABLE III
MAIN PARAMETERS OF THE TWO BUCK CONVERTERS

IC type	IR3820	MAX8655
Input voltage	2.5–21 V	4.5–25 V
Output voltage	1.8 V	1.2 V
Switching frequency	300 kHz	400 kHz
Filter inductor	1.7 μH	0.82 μH
Output capacitor	2×47 μF	4×47 μF

VI. EFFICIENCY ANALYSIS OF ESC-BUCK CONVERTER USING EXPERIMENTAL RESULTS

In order to analyze the properties of the ESC-buck converter, several prototypes have been built. In this paper, two commercially available buck converter ICs, MAX8655 and IR3820, are used. The parameters of the two buck converters are shown in Table III. Meanwhile, a separate ESC converter is also built with discrete components. Table IV shows the parameters of the ESC-buck converters that are constructed with IC MAX8655 and IR3820 as the second stage.

TABLE IV
PARAMETERS OF THE ESC-BUCK CONVERTERS

ESC type	First-Order	Second-Order
Flying cap C_{f1}	$6 \times 47\ \mu$F	$6 \times 47\ \mu$F
Flying cap C_{f2}	NA	$6 \times 47\ \mu$F
Capacitor C_{10}	$1 \times 47\ \mu$F	$1 \times 47\ \mu$F
Capacitor C_{11}	$1 \times 47\ \mu$F	$1 \times 47\ \mu$F
Capacitor C_{12}	NA	$1 \times 47\ \mu$F
Switches	NTMFS4897NF	NTMFS4897NF

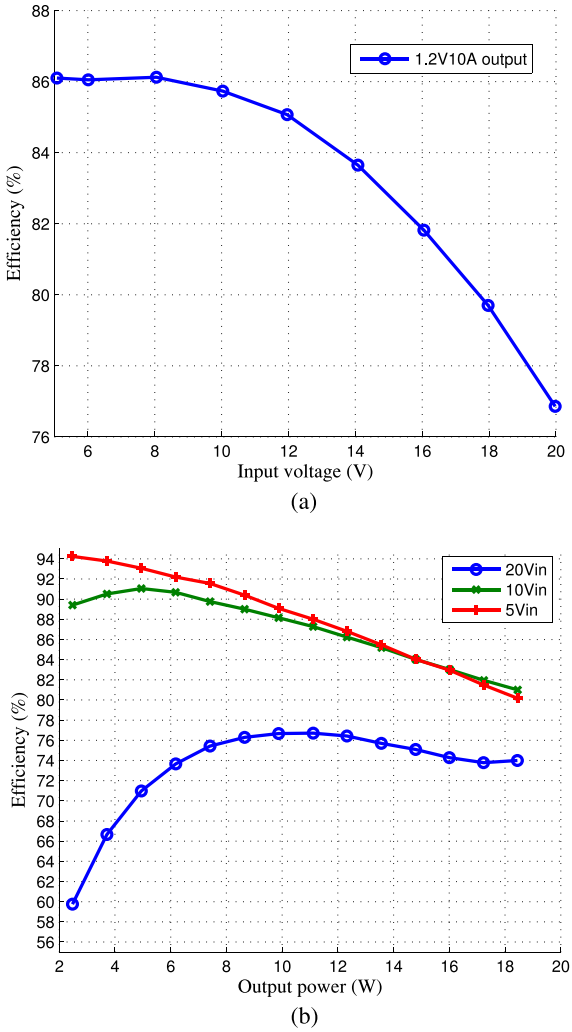


Fig. 13. Efficiency curves of MAX8655 buck converter. (a) Buck converter efficiency versus input voltage. (b) Buck converter efficiency versus output power.

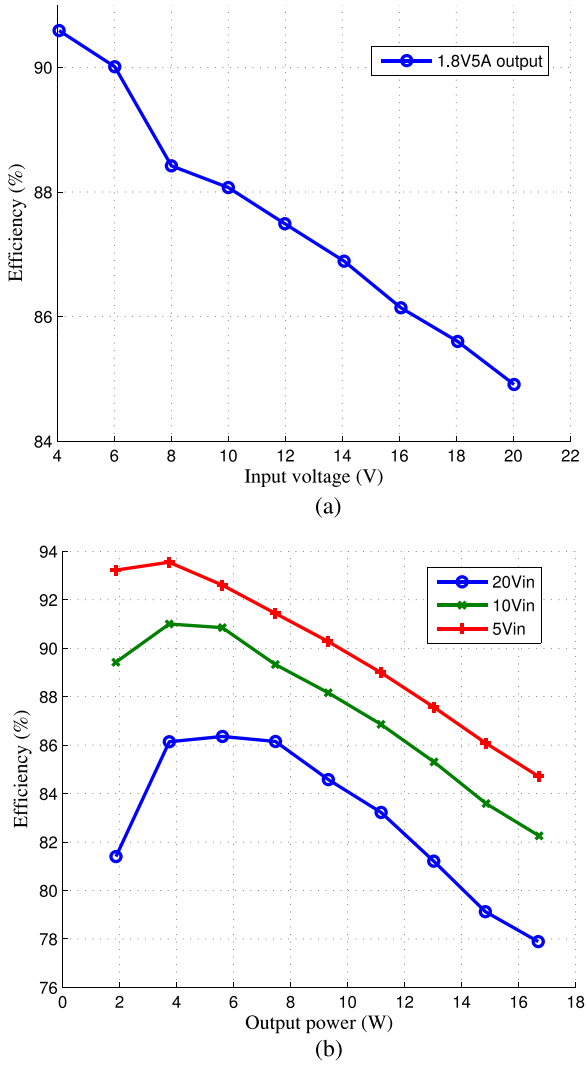


Fig. 14. Efficiency curves of IR3820 buck converter. (a) Buck efficiency at different input voltage. (b) Buck efficiency at different output power.

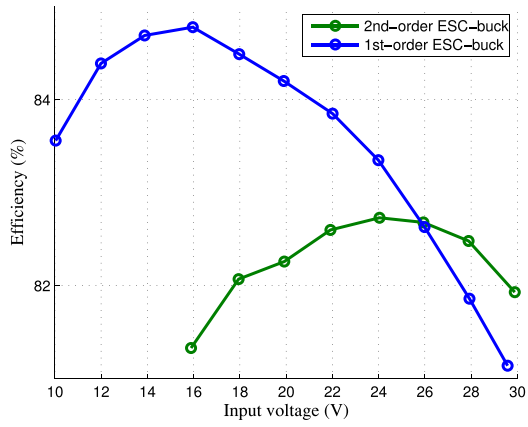
A. *Efficiencies of Single-Stage Buck Converters*

Fig. 13(a) shows the measured efficiency of the buck converter using MAX8655 versus input voltage, which is typical compared with the data sheet from the manufacturer. Fig. 13(b) shows the efficiency improvement for an input voltage reduction from 20 to 10 V and 5 V. It is therefore expected from (20) that there will be efficiency improvement by inserting a first- or second-order ESC converter in front of the buck converter IC MAX8655 to a 20 V supply voltage. Furthermore, at low output power, the efficiency of the second-order ESC-buck converter can be better than the first-order ESC-buck converter.

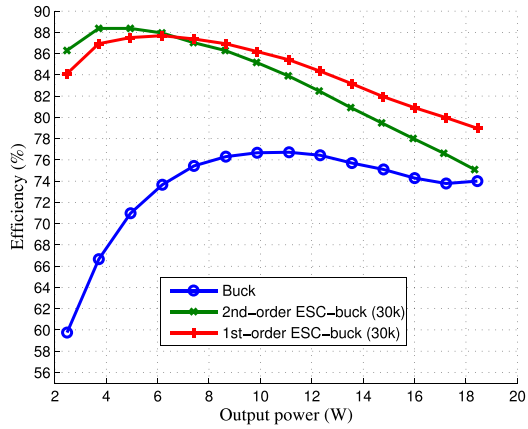
Fig. 14 shows the efficiency of the buck converter using IR3820. From Fig. 14(a) and (20), the headroom of efficiency improvement by inserting a second-order ESC converter can be better than a first-order ESC converter, in front of the buck converter using IR3820.

B. *Efficiency of ESC-Buck Converters*

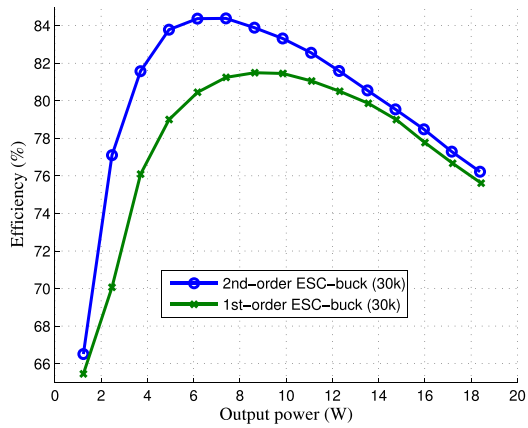
The buck converters analyzed in the last section are connected with a front-end first- or second-order ESC converter for efficiency improvement. Fig. 15(a) gives the efficiency comparison of first-order and second-order ESC-buck converter using the buck IC MAX8655. The second-order ESC-buck converter has a better efficiency than the first-order ESC converter when the input voltage is higher than 26 V. In Fig. 15(b), as expected from the analysis in the last section, the two-stage first- or second-order ESC-buck converter can generally have higher efficiency than the single-stage MAX8655 buck converter for large-voltage-gain applications. The first- or second-order ESC-buck converter excels at different loading conditions. However,



(a)

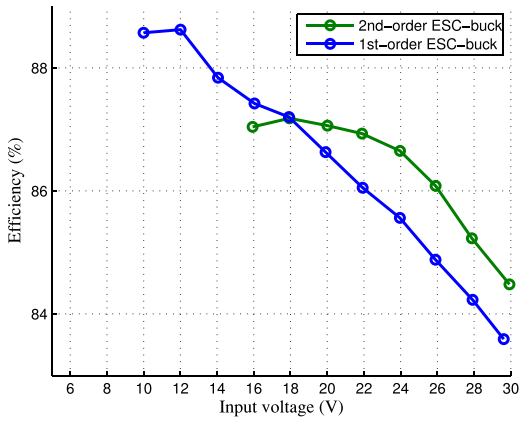


(b)

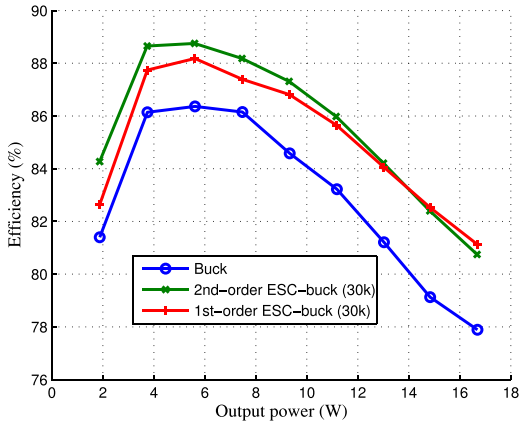


(c)

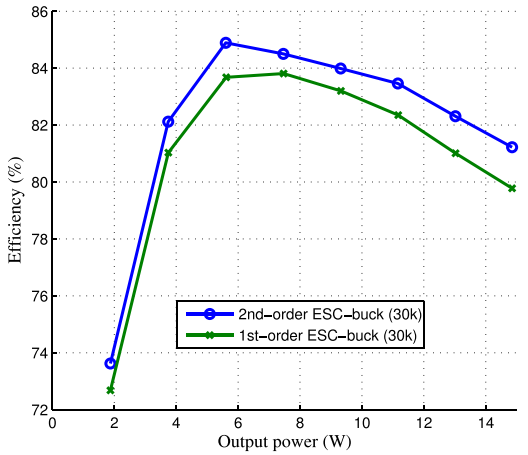
Fig. 15. Efficiency analysis of ESC-buck converter using MAX8655 at an regulated output voltage of 1.2 V. (a) ESC-buck Efficiency versus input voltage at 30 kHz with 10 A output. (b) Comparison of efficiencies using different order ESC-buck converters with front-end ESC operating at 30 kHz and an input voltage of 20 V. (c) Comparison of efficiencies using different order ESC-buck converters with front-end ESC operating at 30 kHz and an input voltage of 30 V.



(a)



(b)



(c)

Fig. 16. Efficiency analysis of ESC-buck converter using IR3820 at a regulated output voltage of 1.8 V. (a) ESC-buck Efficiency versus input voltage at 30 kHz with 5 A output. (b) Comparison of efficiencies using different order ESC-buck converters with front-end ESC operating at 30 kHz and an input voltage of 20 V. (c) Comparison of efficiencies using different order ESC-converters with front-end ESC operating at 30 kHz and an input voltage of 30 V.

when operating at an even higher input voltage of 30 V, which is over the input voltage ratings of a single-stage MAX8655 buck converter, the efficiency of the second-order ESC-buck converter is higher than that of the first-order ESC-buck converter for the load range specified.

Fig. 16 shows that converters using IR3820 have similar efficiency properties. The only difference is that the second-order ESC-buck converter can have better efficiency than the first-order ESC-buck converter at a wider input voltage range due to the larger efficiency headroom.

VII. Conclusion

This paper presents a family of SC converters which can step-down the input voltages at a ratio that increases exponentially with their orders. Experimental results verify the performance of the proposed converters. Because of the lack of voltage regulation, the application of the proposed converter is limited. However, there are numerous commercially available buck integrated circuits whose efficiencies generally deteriorate with increasing input voltage. Thus, the combined application of the ESC converter as a front-end converter and a regulated buck converter can provide a large-voltage-step-down ratio for regulated dc–dc conversion applications. Analysis based on the efficiency headroom of individual buck converter ICs, the two-stage ESC-buck converter can have an overall efficiency better than a single-stage buck converter for the large-voltage-step-down ratio applications. The efficiency analysis is supported by experimental results and explained with discrete-time efficiency analysis. Considering the possibilities of the integration of two-stage ESC-buck converters, these integrated large-voltage-step-down ratio dc–dc converters are expected to have a strong competitive niche in the market.

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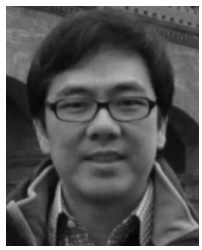

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