Title	Elimination of an Electrolytic Capacitor in AC/DC Light-Emitting Diode (LED) Driver With High Input Power Factor and Constant Output Current
Author(s)	Chen, W; Hui, SYR
Citation	IEEE Transactions on Power Electronics, 2012
Issued Date	2012
URL	http://hdl.handle.net/10722/164083
Rights	Creative Commons: Attribution 3.0 Hong Kong License

Elimination of an Electrolytic Capacitor in AC/DC Light-Emitting Diode (LED) Driver With High Input Power Factor and Constant Output Current

Wu Chen, *Member, IEEE*, and S. Y. Ron Hui*, *Fellow, IEEE*

Abstract—While LEDs enjoy relatively long lifetime up to 10 years, the lifetime of traditional LED drivers using electrolytic capacitor as storage element is limited to typically less than 5 years. In this paper, an ac/dc LED driver without electrolytic capacitor is studied. Compared with other methods to eliminate electrolytic capacitor, the proposed driver has the advantages of almost unity input power factor and constant output current for LEDs. The operation principle, detailed design procedure of the main circuit, and control strategy are presented. The feasibility of the proposed converter has been successfully verified by experiments.

Index Terms—AC/DC LED drivers, electrolytic capacitors, lifetime, light-emitting diodes (LEDs).

I. INTRODUCTION

LED technology has now emerged promising technology to replace conventional lighting devices [1]. Reports in [2]–[6] have demonstrated the LED color and multistring brightness control, particularly in display applications. The long lifetime of LED in the range of 80 000–100 000 h [7] stands out the relatively short lifetime problem of many existing LED drivers using electrolytic capacitors as the energy storage. It is well known that the lifetime of a high-quality electrolytic capacitor is typically 10 000 h at 105 °C. It is temperature dependent due to the use of liquid electrolyte and is reduced by half for every 10 °C rise in operating temperature [8]. The big difference in the lifetimes of the LED devices and the drivers justifies the need for eliminating the electrolytic capacitor in the LED drivers.

Recently, several methods have been proposed to eliminate electrolytic capacitors in ac/dc drivers for LED applications [9]–[15]. Fig. 1 shows the circuit diagram of the ac/dc driver for an LED application. It is known that the electrolytic capacitors in the ac/dc LED driver are used to balance the energy difference between the input pulsating power and the output constant power. Hence, if the electrolytic capacitors are reduced or elim-
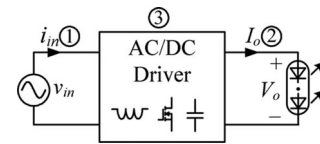
Fig. 1.   Block diagram of the ac/dc driver for LED application.

inated in the driver, the key issue is how to tackle the I/O power imbalance.

The first approach is to modulate the line input current shape. If the peak-to-average ratio of the input pulsating power is reduced, the less storage capacitance will be needed to balance the energy difference between the instantaneous input power and the output constant power. In [9] and [10], the third- and fifth-harmonic signals are injected into the input current to reduce the peak-to-average ratio of the input power. In [11], a control strategy based on a distorted sinusoidal reference in a power factor correction (PFC) converter is proposed to modulate the line input current, which reduces the input pulsating power and allows the reduction of the output capacitance. The advantage of these methods is that traditional main circuits (such as Boost and Flyback converters) can be needed and only modifications on the control circuits are needed. However, the shortcoming of this approach is that the input power factor is reduced.

The second approach is to use pulsating current or current with relatively large ripple to drive LEDs. If the output power is pulsating and equal or close to the instantaneous input power, then no or a little storage capacitor will be needed to balance the energy difference between the input power and the output power. In [12]–[14], two kinds of topologies are proposed for the LED driver, in which LEDs are driven with pulsating current at twice the line frequency. In [15], a reliable passive LED driver is proposed with the help of the general photoelectrothermal theory for LED systems, in which LEDs are driven with relative large current ripple. This approach is suitable for applications, in which tight LED power control is not needed and reliability is critical, such as public/road lighting systems, but is not suitable for some applications in which system compactness and tight current control are of priority.

The third approach is to adopt some energy storage elements to handle the power difference [16]–[27]. From the energy storage element viewpoint, it can be classified into magnetic and capacitive elements [16]. Inductors (magnetic element) are employed as the energy storage element in [17] and [18]; when the input power is lower than the output power, the magnetic

energy stored in the inductor is delivered to the output terminal to compensate the deficit; when the input power is larger than the output power, the excessive energy will be stored in the inductor. Therefore, a bulky electrolytic capacitor can be reduced or eliminated. In [19], a passive *LC* resonant circuit is employed as the energy storage element. The main disadvantage of the use of inductor as the energy storage element is relatively larger magnetic core loss and winding loss. Compared with inductor, the use of a capacitor (capacitive element) as the energy storage element is almost lossless. The basic concept behind the reduction or elimination of a bulky electrolytic capacitor is to utilize small capacitance with large voltage ripple for energy storage instead of large capacitance with small voltage ripple [20]. Generally speaking, the topologies using capacitor with large voltage ripple for energy storage can be categorized into series-capacitor structure [20]–[24] and parallel-capacitor structure [25]–[27]. The former one means that the capacitor handles all the I/O energy and the latter one means that the capacitor handles parts of the I/O energy. A single-stage Boost–Flyback PFC converter with large dc bus voltage ripple is proposed in [20] and [21], in which the input energy is delivered to the bus capacitor through Boost, and then the energy stored in the bus capacitor is transferred to the output through Flyback. In [22] and [23], the input energy is delivered to the storage capacitor through the Flyback or single-ended primary-inductor converter , and then the energy is transferred to the output from the capacitor through Flyback. The bulky electrolytic capacitor in these topologies is reduced or eliminated, but the efficiency of the whole system is aggravated because the entire energy is processed twice to reach the output. Recently, several topologies belonging to capacitor parallel structure have been proposed [25]–[27]. In [25] and [26], a current pulsation smoothing parallel active filter for single-stage photovoltaic (PV) power to ac gird module is presented, in which a bidirectional Buck–Boost circuit is connected in parallel to the dc bus. A three-port structure converter with dedicated power ripple port is proposed in [27], in which minimum capacitance requirement can be achieved.

A novel Flyback ac/dc driver without electrolytic capacitor for an LED application is proposed in this paper. It not only achieves near-unity input power factor, but also provides constant output current for LEDs, which is essential for applications requiring tight current control. The paper is organized as follows. Section II gives the operation principle of the driver. The detailed designs of the main circuit and control strategy are presented in Section III. The experimental results of a 13.5-W experimental prototype are shown in Section IV and a conclusion is given in Section V.

II. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

Fig. 2 shows the circuit configuration of the proposed ac/dc LED driver. D_{r1}–D_{r4} are the input rectifier diodes. T_r is the Flyback transformer, in which N_{p1} and N_s are the primary and secondary windings of the traditional Flyback transformer, and N_{p2} is an additional auxiliary winding. C_a is the energy storage capacitor with large voltage ripple. Q_1–Q_3 are the main switches. D_R is the output rectifier diode. D_{a1} is the freewheel-
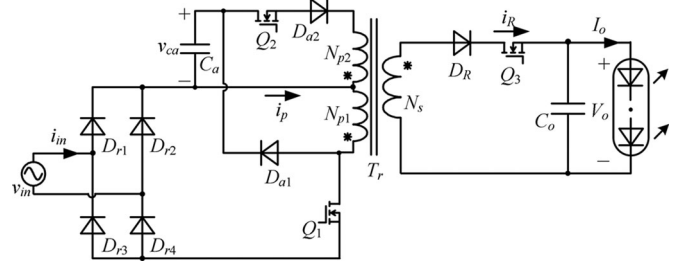

Fig. 2. Main circuit of the proposed ac/dc LED driver (an input LC filter is ignored).
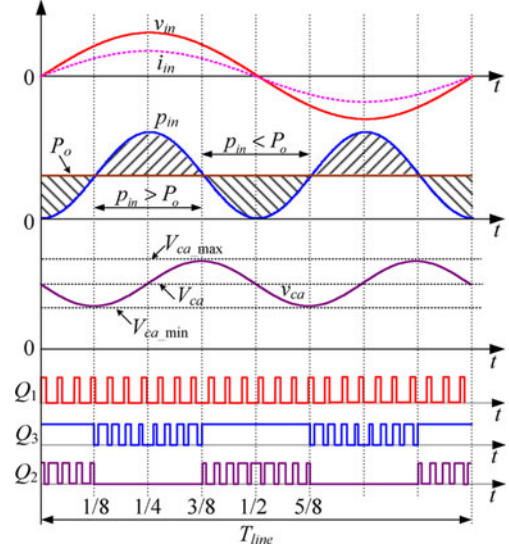

Fig. 3. Key operation waveforms of the proposed ac/dc LED driver.

ing diode. D_{a2} is the blocking diode to block the reverse current flowing through Q_2. C_o is the output filter capacitor.

The key waveforms of the proposed ac/dc LED driver are shown in Fig. 3. Q_1 is controlled to keep the duty cycle almost unchanged in a line period and the Flyback converter is designed to operate in discontinuous current mode (DCM) so that a high input power factor can be automatically achieved. During the line period when the input power $p_{\rm in}$ is lower than the output power P_o, Q_3 is turned on all the time and Q_2 is controlled to achieve the constant output current for the LED load. C_a is discharged, the stored energy is delivered to the output to compensate the deficit and hence $v_{\rm ca}$ decreases. When $p_{\rm in} > P_o$, Q_2 is turned off and Q_3 is controlled to achieve the constant output current for the LED load. The excessive input energy will be transferred into C_a and hence $v_{\rm ca}$ increases. Therefore, the operating mode for the period of $p_{\rm in} < P_o$ is different from that for the period of $p_{\rm in} > P_o$. The switching sequences under different input power conditions are shown in Fig. 4. It should be noted that i_m is the magnetizing current reflected to the primary winding N_{p1}.

A. Operating Modes When $p_{\rm in} < P_o$

Fig. 4(a) shows the key switching sequence when $p_{\rm in} < P_o$. There are four switching stages in a switching period, and the corresponding equivalent circuits are shown in Fig. 5.
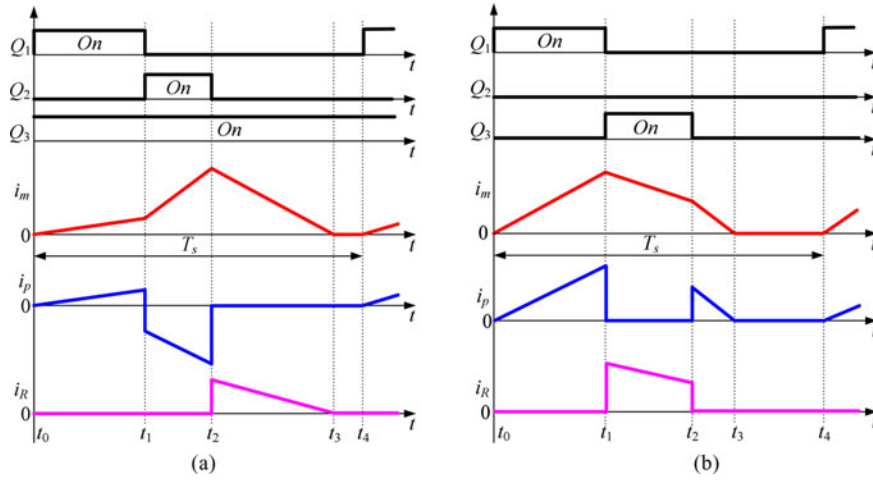
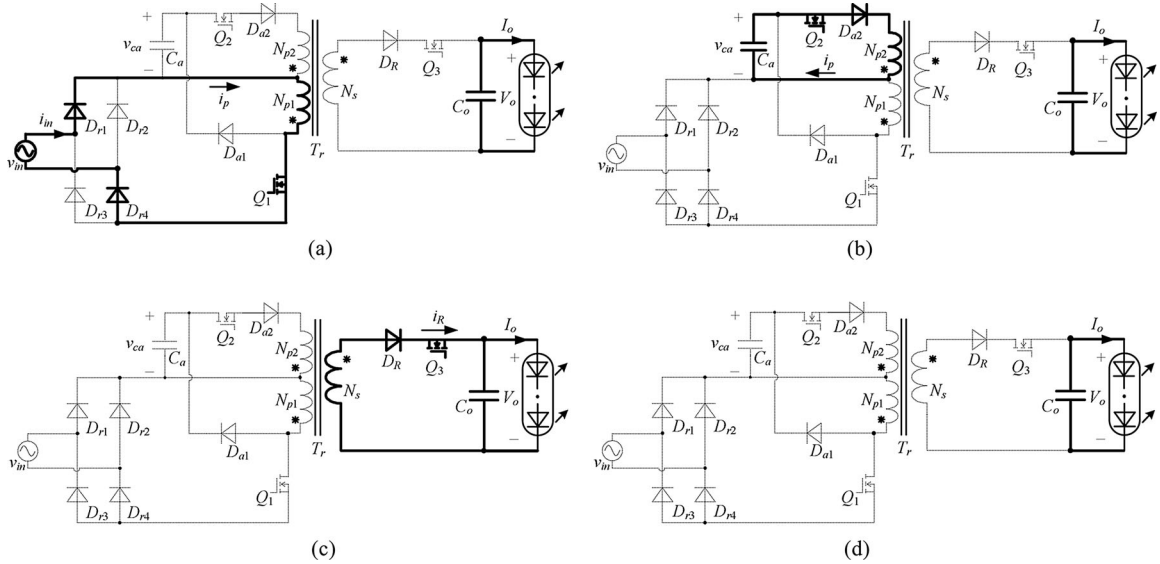Fig. 4.   Switching sequence under different input powers. (a) $p_{\text{in}} < P_o$. (b) $p_{\text{in}} > P_o$.

Fig. 5.   Equivalent circuits during one switching period when $p_{\text{in}} < P_o$. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$. (c) $[t_2, t_3]$. (d) $[t_3, t_4]$.

1) *Stage A1 [t_0, t_1] [see Fig. 5(a)]:* Before t_0, i_p, and i_m are zero, and the LED load is powered by C_o. At t_0, Q_1 is turned on. It should be noted that Q_3 is always ON within the period of $p_{\text{in}} < P_o$. D_{r1} and D_{r4} (or diagonal diodes D_{r2} and D_{r3}) conduct. Assuming input voltage v_{in} remains unchanged during a switching period, i_m increases linearly as

$$i_m(t) = \frac{|v_{\text{in}}(t)|}{L_1}(t - t_0) \tag{1}$$

where L_1 is the self-inductance of the primary winding N_{p1}.

2) *Stage A2 [t_1, t_2] [see Fig. 5(b)]:* At t_1, Q_1 is turned off and Q_2 is turned on. Although Q_3 is ON, no current flows through it because the dot side of the secondary winding is negative. After Q_2 is turned on, C_a is discharged and i_m continues increasing linearly, assuming the voltage v_{ca}

keeps unchanged during a switching period

$$
\begin{aligned}
i_m(t) &= \frac{v_{\text{ca}}(t)N_{p1}}{L_1 N_{p2}}(t - t_1) + \frac{|v_{\text{in}}(t)|}{L_1}(t_1 - t_0) \\
&= \frac{v_{\text{ca}}(t)N_{p1}}{L_1 N_{p2}}(t - t_1) + \frac{|v_{\text{in}}(t)|}{L_1}D_1 T_s
\end{aligned} \tag{2}
$$

where D_1 and T_s are the duty cycle of Q_1 and switching period, respectively.

3) *Stage A3 [t_2, t_3] [see Fig. 5(c)]:* At t_2, Q_2 is turned off; the energy stored in the transformer is released through the secondary winding to the output. Referring to (2), the magnetizing current at t_2 is

$$
\begin{aligned}
I_m(t_2) &= \frac{v_{\text{ca}}(t)N_{p1}}{L_1 N_{p2}}(t_2 - t_1) + \frac{|v_{\text{in}}(t)|}{L_1}D_1 T_s \\
&= \frac{v_{\text{ca}}(t)N_{p1}}{L_1 N_{p2}}D_2 T_s + \frac{|v_{\text{in}}(t)|}{L_1}D_1 T_s
\end{aligned} \tag{3}
$$

where D_2 is the duty cycle of Q_2.

Because i_m is the magnetizing current reflected to the primary winding N_{p1}, the magnetizing current reflected to the secondary winding N_s is $i_m N_{p1}/N_s$. The self-inductance of the secondary winding is $L_1 N_s^2/N_{p1}^2$. Hence, the secondary current i_R is

$$i_R(t) = \frac{I_m(t_2)N_{p1}}{N_s} - \frac{V_o N_{p1}^2}{L_1 N_s^2}(t - t_2). \qquad (4)$$

At t_3, i_R reduces to zero. The time interval of $t_3 - t_2$ is expressed as

$$\Delta T_1 = t_3 - t_2 = \frac{I_m(t_2)L_1 N_s}{V_o N_{p1}}. \qquad (5)$$

4) *Stage A4 [t_3, t_4] [see Fig. 5(d)]:* During this mode, no current flows through the transformer winding and the transformer is initialized. C_o supplies the current to the LED load. When $p_{in} < P_o$, in order to keep the output current and thus output power constant, energy is also provided by C_a. Because the duty cycle of Q_1 is kept unchanged during a line period, the duty cycle of Q_2, which corresponds to energy release, should be used to regulate the output current.

B. Operating Modes When $p_{in} > P_o$

Fig. 4(b) shows the key switching sequence when $p_{in} > P_o$. There are four switching stages in a switching period, and the corresponding equivalent circuits are shown in Fig. 6.

1) *Stage B1 [t_0, t_1] [see Fig. 6(a)]:* Similar to Fig. 5(a), Q_1 is turned on and the input voltage causes the current in the magnetizing inductor to increase during this stage. It should be noted that Q_2 is always OFF during the line period when $p_{in} > P_o$.

2) *Stage B2 [t_1, t_2] [see Fig. 6(b)]:* At t_1, Q_1 is turned off and Q_3 is turned on. Then, the energy stored in the transformer is released through the secondary winding to the output. Referring to (1) and similar to (4), i_R can be expressed as follows:

$$\begin{aligned} i_R(t) &= \frac{I_m(t_1)N_{p1}}{N_s} - \frac{V_o N_{p1}^2}{L_1 N_s^2}(t - t_1) \\ &= \frac{|v_{in}(t)| N_{p1}}{L_1 N_s}(t_1 - t_0) - \frac{V_o N_{p1}^2}{L_1 N_s^2}(t - t_1) \\ &= \frac{|v_{in}(t)| N_{p1}}{L_1 N_s}D_1 T_s - \frac{V_o N_{p1}^2}{L_1 N_s^2}(t - t_1). \end{aligned} \qquad (6)$$

In order to keep the output current constant, the released energy to the output must be constant in a switching period. At t_2, Q_3 is turned off. Referring to (6), i_R at t_2 can be written as

$$\begin{aligned} I_R(t_2) &= \frac{|v_{in}(t)| N_{p1}}{L_1 N_s}D_1 T_s - \frac{V_o N_{p1}^2}{L_1 N_s^2}(t_2 - t_1) \\ &= \frac{|v_{in}(t)| N_{p1}}{L_1 N_s}D_1 T_s - \frac{V_o N_{p1}^2}{L_1 N_s^2}D_3 T_s \end{aligned} \qquad (7)$$

where D_3 is the duty cycle of Q_3.

For the proper operation of this stage, the minimum values of v_{ca}, V_{ca_min} must satisfy

$$V_{ca\_min} > \frac{V_o N_{p1}}{N_s}. \qquad (8)$$

3) *Stage B3 [t_2, t_3] [see Fig. 6(c)]:* After Q_3 is turned off, the excessive energy, which is stored in the transformer, is released to C_a through the primary winding N_{p1} and D_{a1}. C_a is charged and i_m decreases linearly, assuming that v_{ca} remains unchanged during a switching period

$$i_m(t) = \frac{I_R(t_2)N_s}{N_{p1}} - \frac{v_{ca}(t)}{L_1}(t - t_2). \qquad (9)$$

At t_3, i_m reduces to zero. The time interval of $t_3 - t_2$ is expressed as

$$\Delta T_2 = t_3 - t_2 = \frac{I_R(t_2)N_s L_1}{N_{p1} v_{ca}(t)}. \qquad (10)$$

4) *Stage B4 [t_3, t_4] [see Fig. 6(d)]:* During this mode, no current flows through the transformer winding and the transformer is initialized. C_o supplies the current to the LED load. When $p_{in} > P_o$, in order to keep the output current and power constant, the excessive energy is absorbed by C_a. Because the duty cycle of Q_1 is kept unchanged during a line period, the duty cycle of Q_3, which corresponds to energy release to the output, should be used to regulate the output current.

From the previous analysis, it can be seen that only two out of three main switches have switching actions during a switching period, leading to the possibility of reduced switching losses and higher conversion efficiency.

Compared with existing methods presented in [10] and [20] that reduce the input power factor when the electrolytic capacitors are replaced, the proposed LED driver can improve and achieve near-unity input power factor. The method in [10] aims at reducing the peak-to-average ratio of the input pulsating power but cannot ensure the instantaneous input power to be equal to the output power. The sizes of the output filter capacitance in [10] and [20] are 141 μF and 660 μF, respectively, for an output power of 60 W, while that in this proposal is 10 μF for an output power of 13.5 W. In addition, the energy storage capacitor in this proposal can effectively balance the I/O power while keeping the output current constant without large electrolytic filter capacitor. Also, the proposed LED driver involves a parallel-capacitor structure. It has a higher conversion efficiency compared with series-capacitor structure, in which the energy storage capacitor handles all the I/O energy [20], [24].

III. CIRCUIT DESIGN AND CONTROL STRATEGY

A. Main Circuit Design

For a single-phase ac/dc driver, the input voltage can be expressed as

$$v_{in}(t) = V_m \sin \omega t \qquad (11)$$

where V_m is the peak value of the input voltage and ω is the line angular frequency.
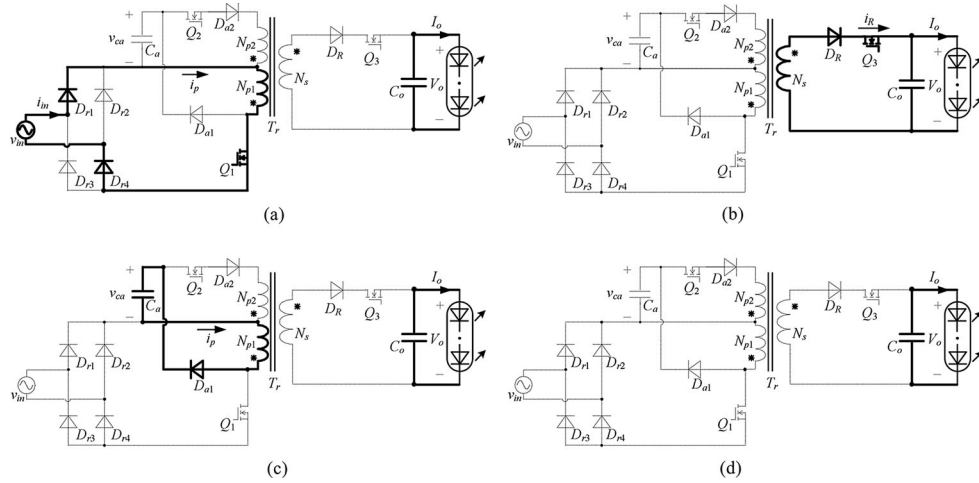
Fig. 6. Equivalent circuits during one switching period when $p_{\mathrm{in}} > P_o$. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$. (c) $[t_2, t_3]$. (d) $[t_3, t_4]$.

Referring to Fig. 3, for an ac/dc LED driver with unity power factor and constant output current, the needed storage capacitor and its waveform can be expressed as [10]

$$C_a = \frac{2P_o}{\omega(V_{\mathrm{ca\_max}}^2 - V_{\mathrm{ca\_min}}^2)} = \frac{P_o}{\omega \Delta V_{\mathrm{ca}} V_{\mathrm{ca}}} \qquad (12)$$

$$v_{\mathrm{ca}}(t) = \sqrt{V_{\mathrm{ca\_min}}^2 + \frac{P_o}{\omega C_a}(1 - \sin 2\omega t)} \qquad (13)$$

where $V_{\mathrm{ca\_max}}$ is the maximum value of v_{ca}, $\Delta V_{\mathrm{ca}} = V_{\mathrm{ca\_max}} - V_{\mathrm{ca\_min}}$ is the amplitude of the voltage ripple, and V_{ca} is the average amplitude of v_{ca}.

To keep the output current constant, the average current through Q_3 in a switching period must be equal to the output current I_o. From (3) to (5), we can determine that when $p_{\mathrm{in}} < P_o$, the average current through Q_3 is

$$\frac{I_m(t_2)\Delta T_1 N_{p1}}{2N_s T_s} = I_o. \qquad (14)$$

From (6) and (7), it can be shown that when $p_{\mathrm{in}} > P_o$, the average current through Q_3 is

$$\frac{1}{2}\left(\frac{|v_{\mathrm{in}}(t)| N_{p1}}{L_1 N_s} D_1 T_s + I_R(t_2)\right) D_3 = I_o. \qquad (15)$$

For the Flyback PFC converter operating under DCM, we have [10]

$$I_o = \frac{V_m^2 D_1^2}{4L_1 V_o f_s} \qquad (16)$$

where f_s is the switching frequency.

Because the proposed LED driver must be operated under DCM to achieve a high input power factor, the sum of the time interval on stages 1–3 under different input power conditions must satisfy the following equations:

$$T_{\mathrm{sum1}} = D_1 T_s + D_2 T_s + \Delta T_1 \leq T_s \qquad (p_{\mathrm{in}} < P_o) \quad (17)$$

$$T_{\mathrm{sum2}} = D_1 T_s + D_3 T_s + \Delta T_2 \leq T_s \qquad (p_{\mathrm{in}} > P_o). \quad (18)$$

From (16), we have

$$D_1 T_s = \frac{2\sqrt{P_o L_1 T_s}}{V_m}. \qquad (19)$$

From (3), (4), (5), and (14), we can obtain

$$I_m(t_2) = \sqrt{\frac{2P_o T_s}{L_1}} \qquad (20)$$

$$\Delta T_1 = \frac{N_s \sqrt{2P_o L_1 T_s}}{V_o N_{p1}} \qquad (21)$$

$$D_2 T_s = (1 - \sqrt{2}|\sin\omega t|)\frac{N_{p2}\sqrt{2P_o L_1 T_s}}{v_{\mathrm{ca}}(t)N_{p1}}. \qquad (22)$$

It can be seen that ΔT_1 is constant for a given ac/dc LED driver and D_1 can reach its maximum value at the minimum input voltage, i.e.,

$$D_{1\_\mathrm{max}}T_s = \frac{2\sqrt{P_o L_1 T_s}}{V_{m\_\mathrm{min}}} \qquad (23)$$

where V_{m_min} is the minimum peak value of the input voltage.

Referring to Fig. 3, when $p_{\mathrm{in}} < P_o$, $\sin\omega t$ and $v_{\mathrm{ca}}(t)$ are both monotone decreasing functions during $(3/8)T_{\mathrm{line}}$ to $(1/2)T_{\mathrm{line}}$; hence, (22) is a monotone increasing function and its maximum amplitude during $3/8\ T_{\mathrm{line}}$ to $1/2\ T_{\mathrm{line}}$ is

$$D_{2\_\mathrm{max}}T_s = (1 - \sqrt{2}|\sin\omega t|)\frac{N_{p2}\sqrt{2P_o L_1 T_s}}{v_{\mathrm{ca}}(t)N_{p1}}\bigg|_{\omega t = \pi}$$

$$= \frac{N_{p2}\sqrt{2P_o L_1 T_s}}{N_{p1}\sqrt{V_{\mathrm{ca\_min}}^2 + (P_o/\omega C_a)}}. \qquad (24)$$

By differentiating (22) with respect to t during $(1/2)T_{\mathrm{line}}$ to $(5/8)T_{\mathrm{line}}$

$$\frac{d(D_2 T_s)}{dt} = \frac{N_{p2}\sqrt{2P_o L_1 T_s}}{N_{p1}}$$

$$\cdot \frac{\sqrt{2}\omega V_{\mathrm{ca\_min}}^2 \cos\omega t + P_o F_1(t)/C_a}{[v_{\mathrm{ca}}(t)]^{1.5}} \qquad (25)$$

where $F_1(t) = \cos 2\omega t + \sqrt{2}(\cos\omega t - \sin\omega t)$.

It can be found that both $\cos \omega t$ and $F_1(t)$ are negative values during $(1/2)T_{\text{line}}$ to $(5/8)T_{\text{line}}$. Therefore, (22) is a monotone decreasing function and its maximum amplitude is the same as (24) during $(1/2)T_{\text{line}}$ to $(5/8)T_{\text{line}}$.

Substitution of (21), (23), and (24) into (17) yields

$$F_2 = \frac{2\sqrt{P_o L_1 T_s}}{V_{m\_\min}} + \frac{N_{p2}\sqrt{2P_o L_1 T_s}}{N_{p1}\sqrt{V_{\text{ca}\_\min}^2 + (P_o/\omega \cdot C_a)}}$$
$$+ \frac{N_s \sqrt{2P_o L_1 T_s}}{V_o N_{p1}} - T_s \leq 0 \quad (p_{\text{in}} < P_o). \quad (26)$$

From (7), (15), and (19), we have

$$D_3 T_s = \frac{N_s \sqrt{P_o L_1 T_s}(2|\sin \omega t| - \sqrt{-2\cos 2\omega t})}{V_o N_{p1}}. \quad (27)$$

Combining (7), (10), (19), and (27) yields

$$I_R(t_2) = \frac{N_{p1}}{L_1 N_s}\sqrt{-2\cos 2\omega t\, P_o L_1 T_s} \quad (28)$$

$$\Delta T_2 = \frac{\sqrt{-2\cos 2\omega t\, P_o L_1 T_s}}{v_{\text{ca}}(t)}. \quad (29)$$

Substitution of (23), (27), and (29) into (18) yields

$$T_{\text{sum2}} = \sqrt{P_o L_1 T_s}\left(\frac{2}{V_{m\_\min}} + \frac{N_s(2|\sin \omega t| - \sqrt{-2\cos 2\omega t})}{V_o N_{p1}}\right.$$
$$\left. + \frac{\sqrt{-2\cos 2\omega t}}{v_{\text{ca}}(t)}\right) \leq T_s \quad (p_{\text{in}} > P_o). \quad (30)$$

For the proper operation of the proposed LED driver, (26) and (30) must be satisfied under different input powers. For a given set of specifications of a driver, parameters such as L_1, N_{p1} : N_{p2} : N_s, C_a, $V_{\text{ca}\_\min}$ need to be determined. A simple design example is given as follows.

The specifications of the LED driver are $V_o = 45$ V, $P_o = 13.5$ W, $T_s = 10\ \mu$S, and $V_{m\_\min} = 127$ V.

From Section II, we know that the maximum voltage across Q_3 is $(v_{\text{ca}}(t)N_s/N_{p1}) - V_o$, the maximum voltage across D_R is $\max((v_{\text{ca}}(t)N_s/N_{p2}) + V_o, (|v_{\text{in}}(t)|N_s/N_{p1}) + V_o)$, the maximum voltage across Q_1 is $\max((V_o N_{p1}/N_s) + |v_{\text{in}}(t)|, |v_{\text{in}}(t)| + v_{\text{ca}}(t))$, and the maximum voltage across Q_2 is $(V_o N_{p2}/N_s) + v_{\text{ca}}(t)$. The maximum peak current through Q_3 is $\max[\sqrt{2P_o T_s/L_1}(N_{p1}/N_s), (2|v_{\text{in}}(t)|N_{p1}\sqrt{L_1 P_o T_s}/(L_1 N_s V_m)]$. It can be seen that the turns ratio of the Flyback transformer merely determines the voltage stress and current stress of devices. Hence, the choices of the turns ratio and devices can be combined. Arbitrarily, we choose N_{p1} : N_{p2} : $N_s = 2$:2:1.

Fig. 7 shows the left-hand terms of (26) as the function of C_a and L_1 under different $V_{\text{ca}\_\min}$. To keep the DCM operation of the proposed driver, the choices of C_a and L_1 must guarantee that the corresponding value of F_2 is lower than zero. It can also be found that the smaller the $V_{\text{ca}\_\min}$, the proper value of L_1 becomes lower for a special C_a, which means relatively larger peak current in the primary and secondary devices.

The appropriate choice of parameters based on (26) only means that the driver operates properly during the line period of $p_{\text{in}} < P_o$. Inequality (30) must be verified with the chosen
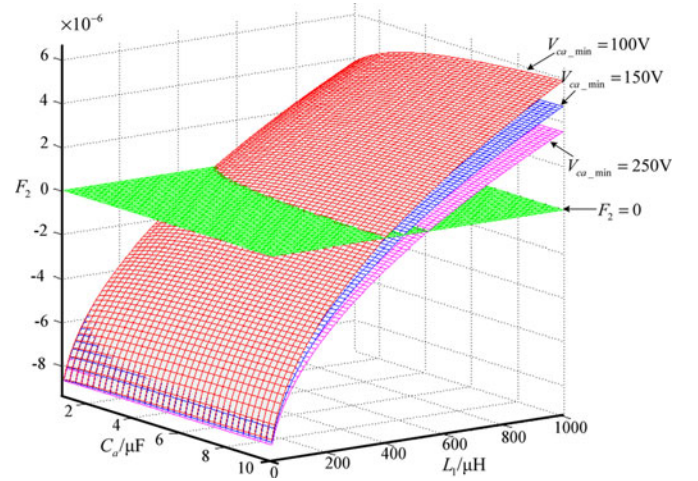

Fig. 7. Surface of the formula F_2 as the function of C_a and L_1 under different $V_{\text{ca}\_\min}$.
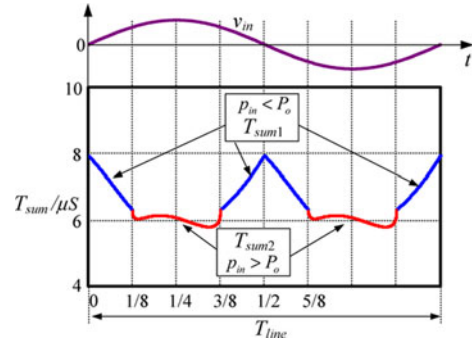

Fig. 8. Values of T_{sum1} and T_{sum2} in a line period.

parameters to check whether it is suitable for the period of $p_{\text{in}} > P_o$.

For example, $C_a = 5\ \mu$F, $L_1 = 300\ \mu$H, and $V_{\text{ca}\_\min} = 150$ V based on (26) are chosen initially. Then, we can substitute these parameters into (17) and (30), and T_{sum} is shown in Fig. 8 under different input powers during a line period. It can be found that $T_{\text{sum}} < T_s$ in the whole line period, which means that the chosen parameters can ensure the driver to operate under DCM.

Based on the chosen C_a and $V_{\text{ca}\_\min}$, the values of $V_{\text{ca}\_\max}$ and V_{ca} can be calculated by (12). Then, the voltage stress of devices can be determined.

B. Control Strategy Design

In [25] and [26], a current hysteresis control is used to force a double-frequency current to flow through the inductor to eliminate the low-frequency PV current ripple. In [27], the voltage shape of the storage capacitor, which leads the line voltage by 45°, is controlled. In this paper, a simple control over the average voltage amplitude of the storage capacitor is employed. The control diagram block of the proposed ac/dc LED driver is shown in Fig. 9.

Compared with the traditional Flyback converter, the main switch Q_1 in the proposed driver is not directly controlled by
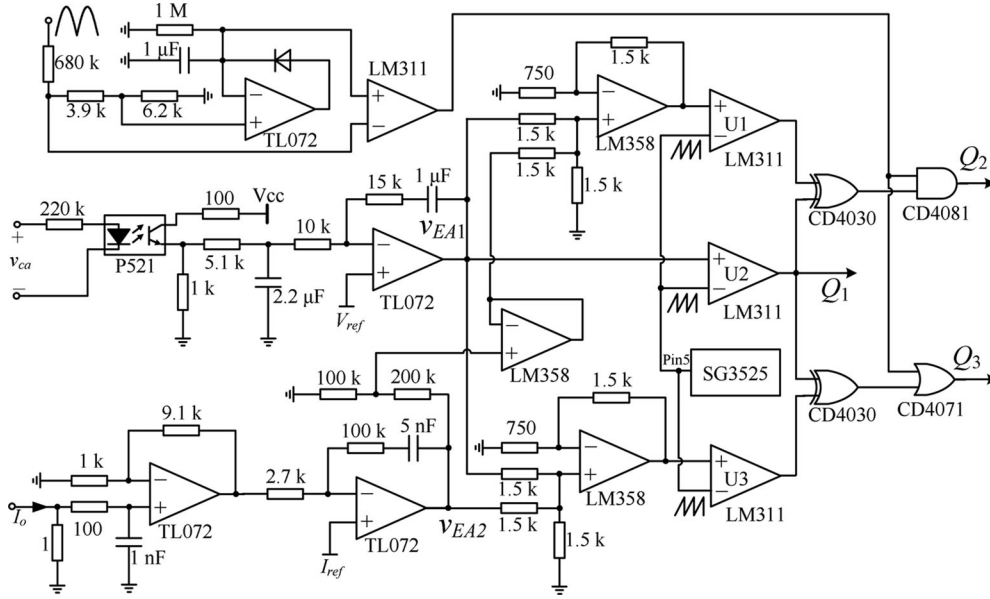
Fig. 9.   Electrical diagram of the control circuit for the proposed ac/dc LED driver.

the output current feedback. Q_1 is controlled by the feedback of the average voltage amplitude of v_{ca}. v_{ca} is sensed through photocoupler P521 and sent to a passive RC low-pass filter ($R = 5.1$ kΩ and $C = 2.2$ μF) for comparison with the reference voltage V_{ref}. The difference is amplified through proportional-integral regulator PI1 ($1.5 + 100/s$). The output voltage of PI1, v_{EA1}, is compared with a sawtooth signal (Pin5 of SG3525) to generate a switching signal for Q_1. Q_2 and Q_3 are directly controlled by the output current feedback. I_o is sensed through a 1-Ω resistor and amplified 10.1 times, and then compared with the reference. The difference is amplified through regulator PI2 ($37 + 7.4 \times 10^4/s$). To guarantee effective turn-*on* signals of Q_2 and Q_3 following the turn-*off* signal of Q_1, v_{EA1} is added to v_{EA2} for comparison with the sawtooth signal. The outputs of U1 and U3 are XORed (CD4030) with the output of U2, respectively. A coefficient 0.33 (formed by 100 and 200 kΩ) is introduced to smooth the transition period from $p_{in} < P_o$ to $p_{in} > P_o$ or vice versa. The rectified input voltage is sensed to determine the line period of $p_{in} < P_o$ or $p_{in} > P_o$.

IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed LED driver, a prototype has been built and tested in the laboratory. The load consists of an LED string using 15 CREE cool white LEDs (model number: XREWHT-L1-WG-Q5-0-04) in series. The key components of the circuit are listed in Table I. It can be found that only a 10-μF output filter capacitor is employed. In contrast, if a conventional Flyback converter is adopted for the same LED load and assuming that the output voltage ripple is 1 V, a 950-μF output filter capacitor is required according to (12).

Fig. 10 shows the experimental waveforms of v_{in}, i_{in}, v_{ca}, and I_o at 110- and 220-VAC input, respectively. It can be seen that the input current is close to sinusoidal shape and the output current is almost constant under different input voltages. The storage capacitor voltage has a large voltage ripple with twice the line frequency and provides the function of energy buffer.

TABLE I
KEY COMPONENTS LIST

Q_1, Q_2	STW12NK80Z (800V/10.5A)
Q_3	IRF640 (200V/18A)
$D_{r1} \sim D_{r4}$	MURS160T3 (600V/1A)
D_{a1}, D_{a2}	STTH208 (800V/2A)
C_a	3 μF/630V
C_o	10 μF/100V
L_1	230 μH
$N_{p1} : N_{p2} : N_s$	30:30:15
f_s	100 kHz

Fig. 11 shows the experimental waveforms of v_{in}, gate-source voltage of Q_2 $v_{gs(Q2)}$, gate-source voltage of Q_3 $v_{gs(Q3)}$, and I_o at 110- and 220-VAC input, respectively. It can be seen that Q_3 is turned on all the time and Q_2 is controlled to achieve the constant output current when $p_{in} < P_o$, and Q_2 is turned off all the time and Q_3 is controlled to achieve the constant output current when $p_{in} > P_o$, which confirms the previous analysis.

Fig. 12 shows the experimental waveforms of $v_{gs(Q1)}$, $v_{gs(Q2)}$, $v_{gs(Q3)}$, i_p, and i_R under the period of $p_{in} < P_o$ and $p_{in} > P_o$, respectively. It can be seen that Q_2 is turned on after the turn-off of Q_1 to compensate the insufficient energy when $p_{in} < P_o$ and Q_3 is turned off and the excessive energy is delivered to C_a when $p_{in} > P_o$, which agrees well with the expected switching sequence in Fig. 4.
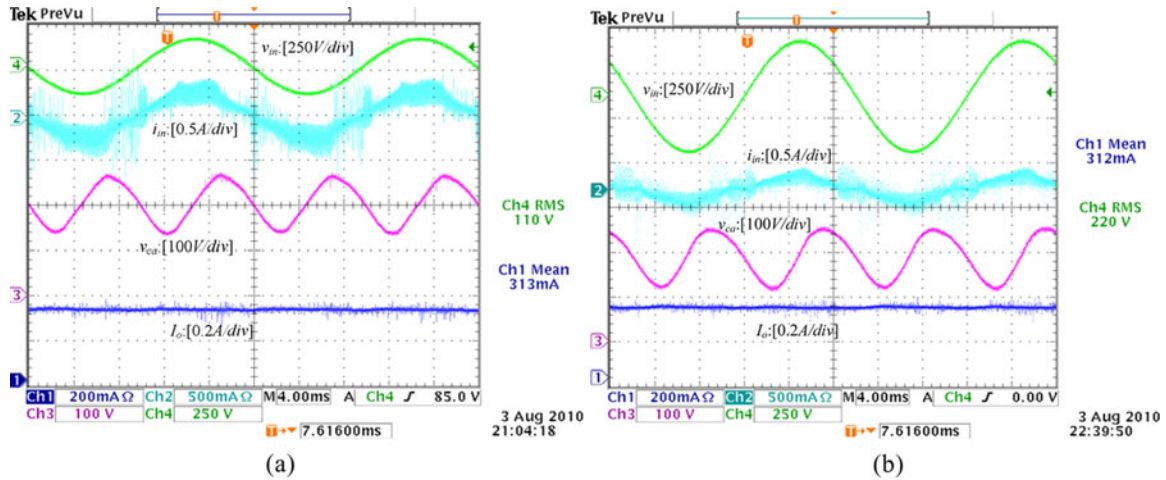
Fig. 10. Waveforms of $v_{\rm in}$, $i_{\rm in}$, $v_{\rm ca}$, and I_o under (a) 110-VAC input; (b) 220-VAC input.
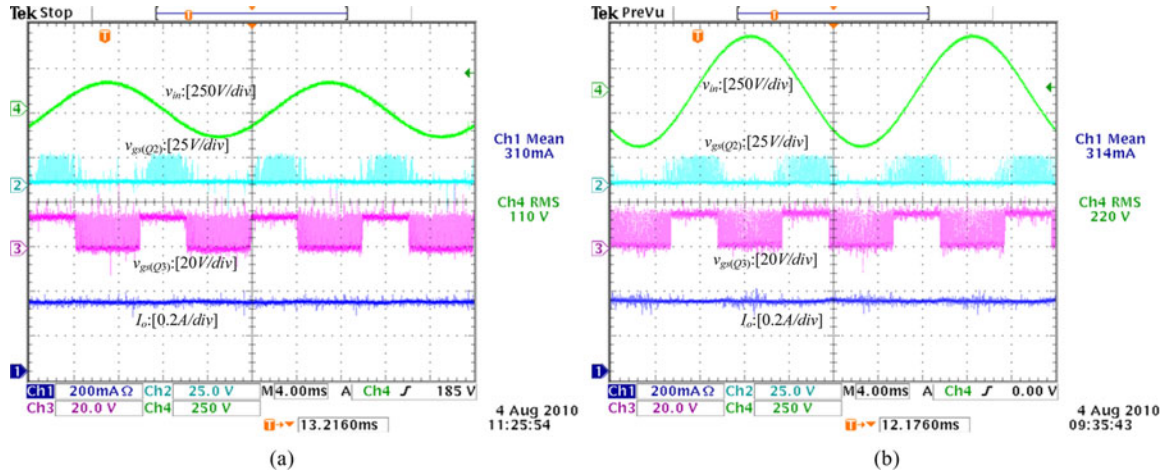

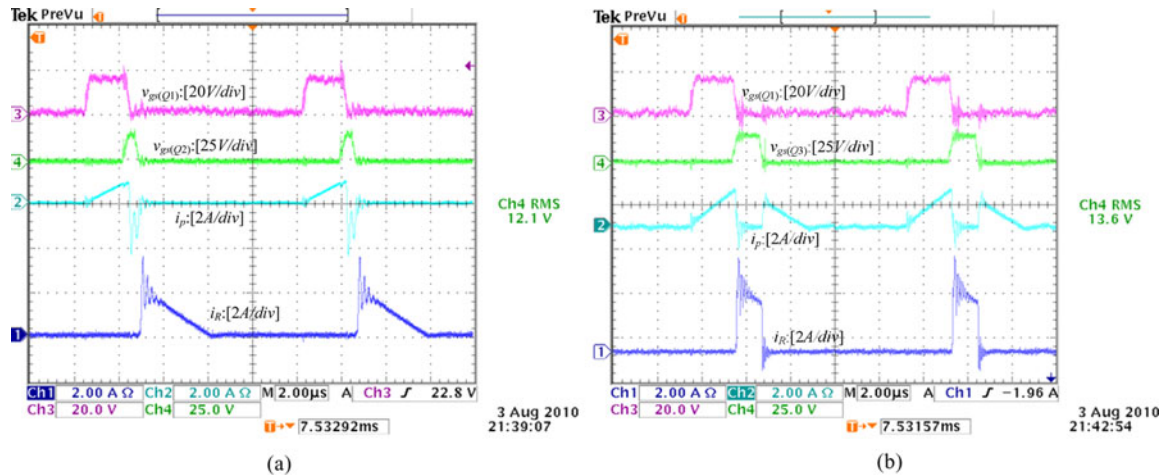Fig. 11. Waveforms of $v_{\rm in}$, $v_{\rm gs(Q2)}$, $v_{\rm gs(Q3)}$ and I_o under (a) 110-VAC input; (b) 220-VAC input.

Fig. 12. Waveforms of $v_{\rm gs(Q1)}$, $v_{\rm gs(Q2)}$, $v_{\rm gs(Q3)}$, i_p, and i_R when (a) $p_{\rm in} < P_o$; (b) $p_{\rm in} > P_o$.

Fig. 13 shows the measured input power factor versus the input voltage. It can be seen that the input power factor of the proposed LED driver is above 0.97. It should be noted that the input power factor decreases when the line voltage increases, that is mainly because there is a small LC ($C = 47$ nF) filter between the ac mains and the input rectifier bridge. When the line voltage increases, the 47-nF capacitor will produce more reactive current and the input current (into the rectifier bridge)
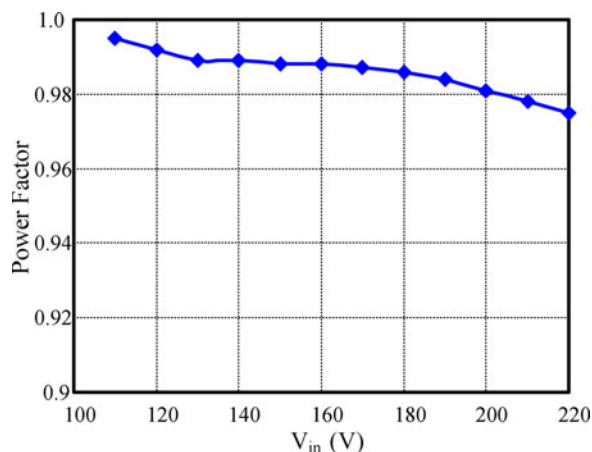
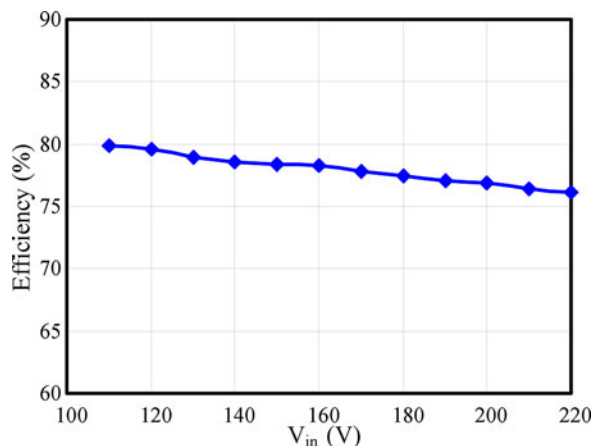Fig. 13. Measured input power factor versus input voltage.

Fig. 14. Measured conversion efficiency versus input voltage for a 13.5-W prototype

will decrease due to the constant output power. Under these two factors, the input power factor decreases.

Fig. 14 shows the measured conversion efficiency versus the input voltage for a 13.5-W prototype. The conversion efficiency decreases with the increasing line voltage. The main reason is that the switching losses of the three switches, which are sensitive to voltage variation, are the dominant power loss component and the conduction losses are comparatively small due to the originally small input current.
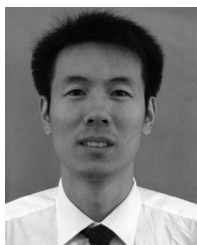
V. CONCLUSION

Despite the long lifetime of modern LED devices, the relatively short lifetimes of electrolytic capacitors in many existing LED drivers limit the lifetime of the overall LED systems. To overcome this problem, we propose a Flyback ac/dc driver without using electrolytic capacitor. The proposed circuit allows the use of small capacitance with large voltage ripple for energy storage. Consequently, nonelectrolytic capacitors can be used in this circuit. The operation principles, features, and designs have been illustrated in a practical prototype. The experimental results show that the driver can generate a sinusoidal input cur-

rent with near-unity power factor and simultaneously provide a constant output current for the LED load.

REFERENCES

[1] I. L. Azevedo, M. G. Morgan, and F. Morgan, "The transition to solid-state lighting," *Proc.. IEEE*, vol. 97, no. 3, pp. 481–510, Mar. 2009.

[2] X. Qu, S.-C. Wong, and C. K. Tse, "Noncascading structure for electronic ballast design for multiple LED lamps with independent brightness control," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 311–340, Feb. 2010.

[3] Y.-K. Lo, K.-H. Wu, K.-J. Pai, and H.-J. Chiu, "Design and implementation of RGB LED drivers for LCD Backlight modules," *IEEE Trans. Ind. Electron.*, vol. 56, no. 12, pp. 4862–4871, Dec. 2009.

[4] C.-Y. Wu, T.-F. Wu, J.-R. Tsai, Y.-M. Chen, and C.-C. Chen, "Multistring LED backlight driving system for LCD panels with color sequential display and area control," *IEEE Trans. Ind. Electron.*, vol. 55, no. 10, pp. 3791–3800, Oct. 2008.

[5] H.-J. Chiu, Y.-K. Lo, J.-T. Chen, S.-J. Cheng, C.-Y. Lin, and S.-C. Mou, "A high-efficiency dimmable LED driver for low-power lighting applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 735–743, Feb. 2010.

[6] H.-J. Chiu and S.-J. Cheng, "LED backlight driving system for large-scale LCD panels," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2751–2760, Oct. 2007.

[7] (2010). [Online]. Available: http://www.colorkinetics.com/support/whitepapers/LEDLifetime.pdf.

[8] (2010). [Online]. Available: http://www.cde.com/catalogs/AEappGUIDE.pdf.

[9] B. Wang, X. Ruan, K. Yao, and M. Xu, "A method of reducing the peak-to-average ratio of LED current for electrolytic capacitor-less AC–DC drivers," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 592–601, Mar. 2010.

[10] L. Gu, X. Ruan, M. Xu, and K. Yao, "Means of eliminating electrolytic capacitor in AC/DC power supplies for LED lightings," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1399–1408, May 2009.

[11] D. G. Lamar, J. Sebastián, M. Arias, and A. Fernández, "Reduction of the output capacitor in power factor correctors by distorting the line input current," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2010, pp. 196–202.

[12] G. Spiazzi, S. Buso, and G. Meneghesso, "Analysis of a high-power-factor electronic ballast for high brightness light emitting diodes," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, 2005, pp. 1494–1499.

[13] E. Mineiro Sá Jr., C. S. Postiglione, F. L. M. Antunes, and A. J. Perin, "Low cost ZVS PFC driver for power LEDs," in *Proc. IEEE Ind. Electron. (IECON)*, 2009, pp. 3551–3556.

[14] R. A. Pinto, M. R. Cosetin, M. F. da Silva, G. W. Denardin, J. Fraytag, A. Campos, and R. N. do Prado, "Compact emergency lamp using power LEDs," in *Proc. IEEE Ind. Electron. (IECON)*, 2009, pp. 3494–3499.

[15] S. Y. R. Hui, S. Li, X. Tao, W. Chen, and W. M. Ng, "A novel passive off-line light-emitting diode (LED) driver with long lifetime," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2010, pp. 594–600.

[16] R. Wang, F. Wang, R. Lai, P. Ning, R. Burgos, and D. Boroyevich, "Study of energy storage capacitor reduction for single phase PWM rectifier," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2009, pp. 1177–1183.

[17] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1419–1429, Sep./Oct. 2000.

[18] S. Li, B. Ozpineci, and L. M. Tolbert, "Evaluation of a current source active power filter to reduce the DC bus capacitor in a hybrid electric vehicle traction drive," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2009, pp. 1185–1190.

[19] Y. X. Qin, H. S. H. Chung, D. Y. Lin, and S. Y. R. Hui, "Current source ballast for high power lighting emitting diodes without electrolytic capacitor," in *Proc. IEEE Ind. Electron. (IECON)*, 2008, pp. 1968–1973.

[20] B. Zhang, X. Yang, M. Xu, Q. Chen, and Z. Wang, "Design of Boost-Flyback single-stage PFC converter for LED power supply without electrolytic capacitor for energy-storage," in *Proc. IEEE Int. Power Electron. Motion Control Conf. (IPEMC)*, 2009, pp. 1668–1671.

[21] K. Yao, M. Xu, X. Ruan, and L. Gu, "Boost-Flyback single-stage PFC converter with large DC bus voltage ripple," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2009, pp. 1867–1871.

[22] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the DC input for an

AC photovoltaic module system," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, Sep. 2006.

[23] G. H. Tan, J. Z. Wang, and Y. C. Ji, "Soft-switching flyback inverter with enhanced power decoupling for photovoltaic applications," *IET Electr. Power Appl.*, vol. 2, no. 5, pp. 316–324, Mar. 2007.

[24] J. Garcia, A. J. Calleja, E. L. Corominas, D. Gacio, and J. Ribas, "Electronic driver without electrolytic capacitor for dimming high brightness LEDs," in *Proc. IEEE Ind. Electron (IECON)*, 2009, pp. 3518–3523.

[25] A. C. Kyritsis, N. P. Papanicolaou, and E. C. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected AC-PV modules," in *Proc. Eur. Conf. Power Electron. Appl.(EPE)*, 2007, pp. 1–10.

[26] A. C. Kyritsis, N. P. Papanicolaou, and E. C. Tatakis, "Enhanced current pulsation smoothing parallel active filter for single stage grid-connected AC-PV modules," in *Proc. Power Electron. Motion Control Conf. (EPE-PEMC)*, 2008, pp. 1287–1292.

[27] P. T. Krein and R. S. Balog, "Cost-effective hundred-year life for single-phase inverters and rectifiers in solar and LED lighting applications based on minimum capacitance requirements and a ripple power port," in *Proc. IEEE Appl. Power Electron. Conf. (APEC)*, 2009, pp. 620–625.

Professor Ron Hui (F'03) received the B.Sc. (Eng. Hons) degree from the University of Birmingham, Birmingham, U.K., in 1984, and the D.I.C. and Ph.D. degrees from the Imperial College of Science and Technology, London, U.K., in 1987.

He was a Lecturer at the University of Nottingham, U.K., in 1987–1990. In 1990, he joined the University of Technology, Sydney, and was appointed as a Senior Lecturer at the University of Sydney, in 1992, where he became a Reader in 1995. He joined the City University of Hong Kong, Kowloon, Hong Kong (CityU), as a Professor in 1996 and was promoted to the Chair Professor in 1998. In 2001–2004, he was an Associate Dean of the Faculty of Science and Engineering, CityU. From 2011, he holds the Chair Professorship at both the University of Hong Kong and Imperial College London. He is the author of more than 200 technical papers, including more than 150 refereed journal publications and book chapters. More than 55 of his patents have been adopted by industry.

Dr. Hui is a Fellow the IET. He has been an Associate Editor (Power Conversion) of the IEEE TRANSACTIONS ON POWER ELECTRONICS since 1997 and an Associate Editor (Lighting Technology) of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS since 2007. He has been appointed twice as an IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2004 and 2006. He served as one of the 18 administrative committee members of the IEEE Power Electronics Society and was the Chairman of its Constitution and Bylaws Committee from 2002 to 2010. He received the Excellent Teaching Award at CityU in 1998 and the Earth Champion Award in 2008. He won the IEEE Best Paper Award from the IEEE IAS Committee on Production and Applications of Light in 2002, and two IEEE Power Electronics Transactions Prize Paper Awards for his publication in Wireless Battery Charging Platform Technology in 2009 and for his paper on LED system theory in 2010. His inventions on wireless charging platform technology underpin key dimensions of Qi, the world's first wireless power standard, with freedom of positioning and localized charging features for wireless charging of consumer electronics. In November 2010, he received the IEEE Rudolf Chope R&D Award from the IEEE Industrial Electronics Society, the IET Achievement Medal (The Crompton Medal), and was elected to the Fellowship of the Australian Academy of Technological Sciences and Engineering.

Wu Chen (S'05–M'12) was born in Jiangsu, China, in 1981. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2003, 2006, and 2009, respectively.

From 2009 to 2010, he was a Senior Research Assistant in the Department of Electronic Engineering, City University of Hong Kong, Kowloon, Hong Kong. In 2010–2011, he was a Postdoctoral Researcher in FREEDM Systems Center, North Carolina State University, Raleigh. Since Sept. 2011, he has been an Associate Research Fellow with the School of Electrical Engineering, Southeast University, Nanjing, China. His main research interests include soft-switching dc/dc converters, inverters, and power electronic system integration.