



Title	Common-Mode Noise Cancellation in Switching-Mode Power Supplies Using an Equipotential Transformer Modeling Technique
Author(s)	Chan, YP; Pong, BMH; Poon, NK; Liu, JCP
Citation	IEEE Transactions On Electromagnetic Compatibility, 2012, v. 54 n. 3, p. 594-602
Issued Date	2012
URL	http://hdl.handle.net/10722/155656
Rights	Creative Commons: Attribution 3.0 Hong Kong License

Common-Mode Noise Cancellation in Switching-Mode Power Supplies Using an Equipotential Transformer Modeling Technique

Yick Po Chan, *Student Member, IEEE*, Bryan Man Hay Pong, *Senior Member, IEEE*,
Ngai Kit Poon, *Member, IEEE*, and Joe Chui Pong Liu

Abstract—Electromagnetic interference (EMI) is a significant challenge in the design of high-efficiency switching-mode power supplies due to the presence of common-mode (CM) noise. In many power-supply designs, a variety of noise suppression schemes must be implemented in order to meet EMI requirements. Most of these schemes create power loss that lead to efficiency and thermal issues. In this paper, a transformer construction technique is proposed that effectively reduces the CM noise current injecting across the isolated primary and secondary windings. This technique is based on the zero equipotential line theory. A transformer design with the proposed CM noise cancellation technique can achieve high conversion efficiency as well as substantial CM noise rejection.

Index Terms—Antiphase winding, common-mode (CM) noise cancellation, equipotential line, transformer winding.

I. INTRODUCTION

ELECTROMAGNETIC interference (EMI) is a significant challenge in the design of high-efficiency switching-mode power supplies (SMPS) due to the presence of common-mode (CM) noise. In many power-supply designs, a variety of noise suppression schemes must be implemented in order to meet EMI requirements. Most of these schemes create unwanted power loss that lead to size, efficiency, and thermal issues. Currently, there are several commonly known methods to minimize CM noise. A brief summary of methods for minimizing CM noise flowing through a line impedance stabilization network and problems associated with these schemes are given as follows.

- 1) *Use of CM noise filters*: This involves time-consuming designs as suggested by Shih and Chen [1], which are commonly used in many SMPS. To obtain satisfactory EMI suppression, a bulky CM noise suppression filter is usually required. Large filters are undesirable due to the increasing demand for smaller SMPS, as well as their placement on the power path. Damnjanovic *et al.* [2], [3] acknowledged the importance of CM choke filter size and proposed

surface mount device (SMD) CM choke designs [4]. Although SMD CM chokes are small, they are typically only effective above 1 MHz or above, leaving noise below 1 MHz unsuppressed. This frequency limitation is not limited to SMD chokes as it is common to large CM chokes as well. Roc'h *et al.* [5], [6] also emphasized the importance of CM choke filter design because it is often difficult to design a low power loss, minimal size filter. An active CM filter is proposed by Mortensen and Venkataramanan [7] to further reduce CM noise. With an active design, the designer has greater flexibility to fine tune the CM filter beyond a passive design alone; however, active filters are not easily modeled and the gain bandwidth product is severely limited by the active components.

- 2) *Minimize the parasitic coupling capacitors from the primary winding to the secondary winding*: This leads to a high leakage inductance and produces efficiency problems.
- 3) *Bypass capacitor connected across the primary and the secondary side*: Chen *et al.* [8] have discussed the effects of this Y-Capacitor on CM noise performance, but the applicable capacitance is always limited by safety standards and this method alone usually cannot provide a low enough impedance to shunt all of the CM noise current flowing along this path.
- 4) *Faraday shielding*: This method requires careful integration of a conducting sheet into the transformer to shunt away noise current. This is not always effective because there are many paths which the CM noise current can go. The shield must be properly installed in order to meet safety requirements.

The CM noise source in SMPS is created by the high-frequency, high-voltage switching on the primary MOSFET. In the example of an isolated flyback converter, the CM noise current can be imagined to mainly follow two paths as shown in Fig. 1, via the parasitic capacitor from the drain node of the MOSFET to the ground, or via the isolation transformer coupling path to the secondary, then through the parasitic capacitor to the ground.

There are other techniques [9]–[15] that have been proposed to reduce the conducted CM noise that causes EMI. In the first noise path described, Cochrane *et al.* [9] employed a compensation capacitor with an antiphase winding to passively cancel the noise current flowing through the MOSFET parasitic capacitor. However, this simple addition of the capacitor cannot stop the

Manuscript received November 13, 2009; revised November 11, 2010 and May 13, 2011; accepted July 26, 2011. Date of publication September 19, 2011; date of current version June 15, 2012.

Y. P. Chan and B. M. H. Pong are with The University of Hong Kong, Hong Kong (e-mail: achan@eee.hku.hk; mhp@eee.hku.hk).

N. K. Poon and J. C. P. Liu are with the PowerELab Limited, Hong Kong (e-mail: nkpoon@powerelab.com; cpliu@powerelab.com).

Digital Object Identifier 10.1109/TEMC.2011.2166270

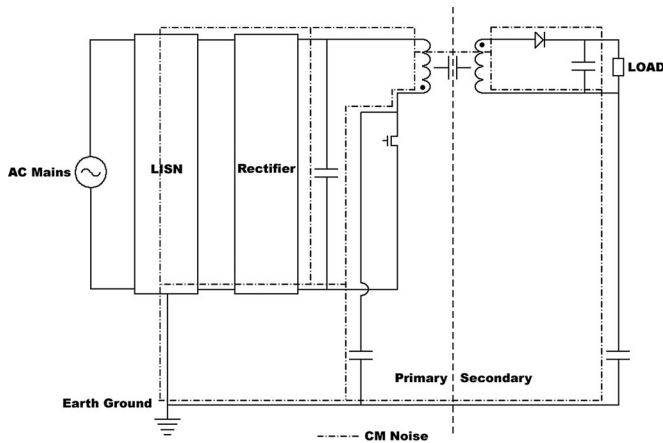


Fig. 1. Flyback converter showing CM noise paths.

significant part of the noise current flowing through the secondary side and returned via the ground path. Herbert [10] proposed the use of two or more transformers in series to reduce the overall parasitic capacitance between the primary and secondary windings, thereby minimizing coupling between windings. This option requires additional magnetic components and tedious designs. The reduction of the cross-coupling between the primary and secondary side is undesirable because this would increase the leakage inductance and lead to poor conversion efficiency in many cases. Wang and Lee [11] proposed an alternative method for canceling the CM noise by creating negative capacitances that balance the parasitic capacitances at different points in the power converter. Obtaining repeatable results for multiple prototype designs remains a challenge for this technique.

CM current coupled from the MOSFET heat sink is often the focus of many researchers. However, this is not the only path that CM current can flow. When the secondary ground is connected to earth ground, which is the case for Class I products, this presents a path with comparable or lower impedance. CM current can flow through the capacitance between the primary and the secondary windings to earth ground and violates the EMI regulations. This paper focuses on this issue which has not been widely discussed.

The proposed method for reducing CM noise is based on the production of a balanced antiphase noise voltage source [12], [13] with a special transformer construction arrangement. An analytical model with a P-Spice equivalent circuit is also presented to explain the method theory. This method produces no loss and requires no extra components, which is favorable in terms of converter energy efficiency and small physical size. This method is applied to several popular converter topologies and the transformer winding construction is explained.

II. EQUIPOTENTIAL LINE CONCEPT—ANTIPHASE WINDING

The equipotential line concept for CM noise reduction is introduced to cancel the noise current flowing via the primary winding to the secondary winding coupling capacitance C_{PS} . The idea is to produce an electric field opposite to that produced by the primary winding, where ideally, it is possible to reduce

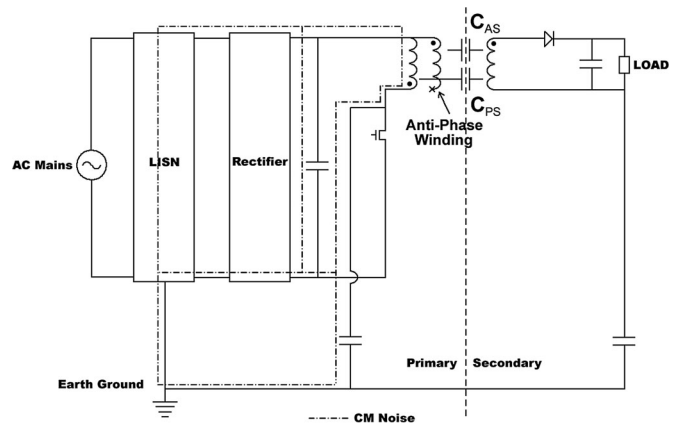


Fig. 2. Flyback converter with an antiphase winding.

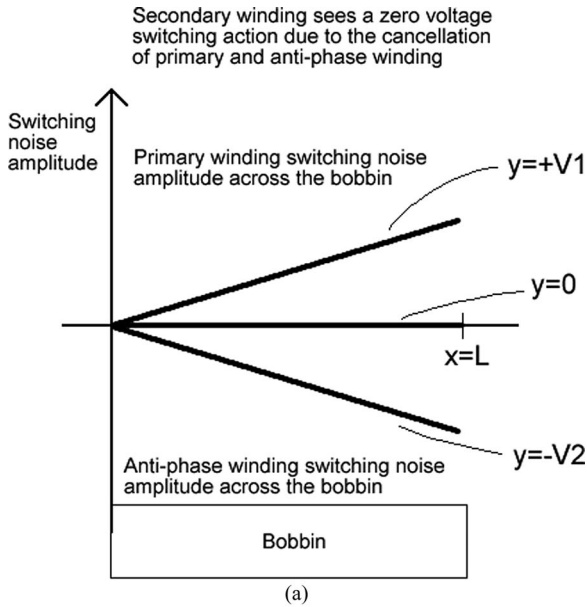
the switching potential of the secondary winding to zero. In this case, no CM current will flow through the capacitance C_{PS} . The opposite electric field is produced by an additional antiphase winding.

The flyback converter example in Fig. 1 is considered and an antiphase winding with the same number of turns to the primary winding is added, as shown in Fig. 2. To achieve the best possible noise cancellation, the wire gauge of the antiphase and the spread along the bobbin should be the same as the primary winding.

First, connect one end of the antiphase winding to the circuit. The primary positive dc terminal because it sets a quiet node to one side of this antiphase winding, therefore the noise voltage generated on the antiphase winding is defined. Next, the other side of the antiphase winding should be left unconnected since only the antiswitching potential along the transformer is needed. No power current flow is necessary and this connection scheme contributes negligible loss, where the proximity loss created by this extra winding should be minimal. The cost is increased due to the addition of the antiphase wiring and there is a size increase due to the extra layer of winding. This is normally beneficial as the experiment in Section V confirms the substantial reduction of the input CM choke filter inductance value to achieve similar CM noise reduction. If the coupling capacitance between the antiphase and the secondary winding C_{AS} is equal to C_{PS} , then the secondary winding will experience the same magnitude of noise from the primary and the antiphase winding and see an overall noise amplitude of zero along the bobbin. The secondary winding is said to be on the zero equipotential line shown in Fig. 3(a).

Fig. 3(b) demonstrates a simple P-Spice equivalent circuit model of the effect of an antiphase winding. To verify the cancellation of the CM noise flowing across the transformer, a bypass capacitor can be placed across the primary and secondary winding to provide a current return path. It is clear that if the measured voltage potential between the primary and secondary ground is zero, the CM noise flowing via C_{PS} is effectively canceled by the antiphase winding.

If the turns ratio N_{PS} between the primary and secondary windings is comparable, then the secondary winding will, in



Equivalent Circuit Model
 V1 = Switching noise source from the primary winding
 V2 = Switching noise source from the anti-phase winding
 C1 = C_{PS}
 C2 = C_{AS}
 Y = A bypass capacitor used for measurement purpose

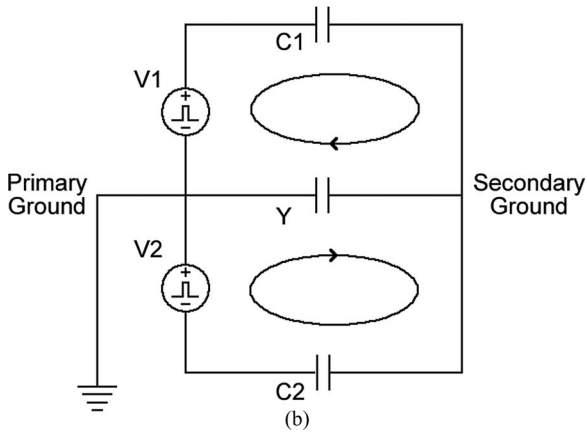
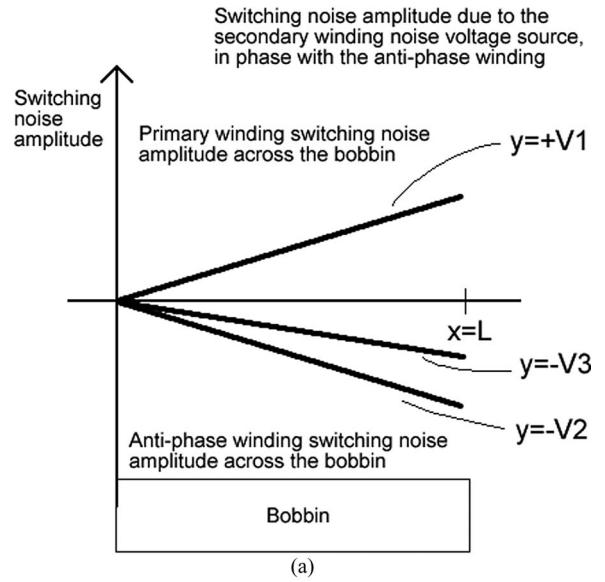


Fig. 3. (a) Graph showing the noise amplitudes along the bobbin. (b) Equivalent circuit model.

fact, be one of the noise voltage source across the bobbin that cannot be neglected, similar to the antiphase winding in the same phase because the switching action will also induce a switching voltage across the secondary winding, as shown in Fig. 4(a).

Since the secondary winding noise is coupled to both the primary and antiphase windings, the relative coupling capacitance is, therefore, C_{PS} + C_{AS}. Fig. 4(b) shows the equivalent circuit. The principle is the same where the primary–secondary ground node can be measured to verify the effectiveness of such a cancellation scheme.

Fig. 5(a) shows the winding construction in a physical transformer of a common flyback or forward converter. Let the primary winding **P** have N_P turns and the secondary winding **S** have N_S turns. In order to balance the current flowing across the coupling capacitor C_{PS}, the windings must be in antiphase and also the turns ratio must equals 1.



Equivalent Circuit Model
 V1 = Switching noise source from the primary winding P
 V2 = Switching noise source from the secondary winding S
 V3 = Switching noise source from the anti-phase winding A
 C1 = C_{PS}
 C2 = C_{PS}+C_{AS}
 C3 = C_{AS}
 Y = A bypass capacitor used for measurement purpose

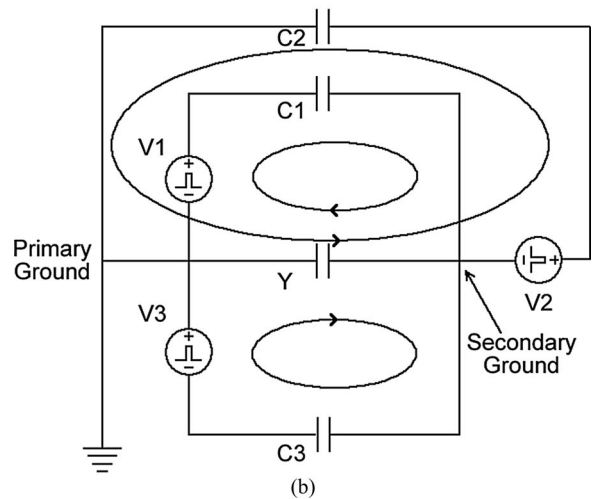


Fig. 4. (a) Graph showing the noise amplitudes along the bobbin with the secondary noise source. (b) Equivalent circuit model.

Therefore, to meet the balancing condition, an extra winding is necessary to provide the flexibility in designing this type of transformer, shown in Fig. 5(b), so the zero equipotential condition can be achieved without having to sacrifice the conversion efficiency and limit the turns ratio N_{PS} between the primary winding **P** and secondary winding **S**. This winding **A** does not need to carry any power current and it has no power consumption.

If N_P > N_S, then the noise voltage across winding **P** will have a greater magnitude than the noise voltage across winding **S**. Intuitively, winding **A** should have a phase the same as winding **S** in order to provide the canceling noise voltage source. In Fig. 5(b), to meet the zero equipotential state, the balanced

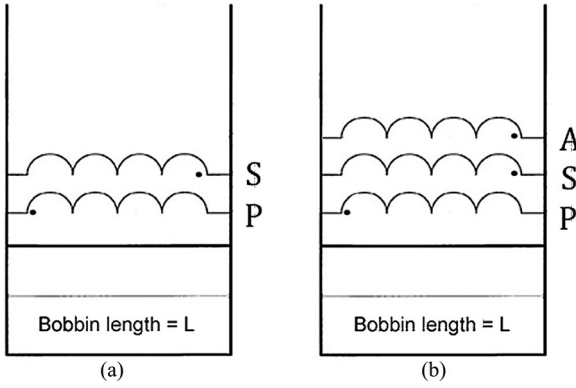


Fig. 5. (a), (b) Winding phase arrangement of a typical flyback or forward converter and the additional antiphase winding.

condition is

$$V_P(C_1) - V_S(C_2) - V_A(C_3) = 0 \quad (1)$$

where $V_P = N_{PS}(V_S) = N_{PA}(V_A)$ and $N_{PS} = (N_P/N_S)$, $N_{PA} = (N_P/N_A)$

$$\therefore V_P(C_1) - \frac{1}{N_{PS}}V_P(C_2) - \frac{1}{N_{PA}}V_P(C_3) = 0$$

$$\therefore C_1 = \frac{1}{N_{PS}}C_2 + \frac{1}{N_{PA}}C_3.$$

Now, $C_2 = C_1 + C_3$

$$\therefore C_1 = \frac{1}{N_{PS}}(C_1 + C_3) + \frac{1}{N_{PA}}C_3$$

$$\therefore C_{AS} = \frac{(N_{PS} - 1)}{((N_{PS}/N_{PA}) + 1)}C_{PS}. \quad (2)$$

It can be seen from (2) that if $N_{PS} = 1$, then $C_{AS} = 0$, i.e., the extra winding **A** is not required. This implies when N_P is equal to N_S , as shown in Fig. 6, with both windings wound across the whole length of bobbin in antiphase, switching voltage generated by the primary winding will be effectively canceled by the secondary winding switching voltage as their switching amplitude is equal, but this construction is uncommon in SMPS design due to its lack of step-up or step-down features.

It is also proved that if $N_{PS} < 1$, i.e., $N_P < N_S$, then C_{AS} is negative and the original phase assumption of winding **A** is actually in wrong phase to balance the noise across the transformer. Notice the significance of this result; the turns ratio N_{PA} , as well as C_{AS} , can be easily controlled by the transformer construction without affecting the original design parameters N_{PS} and C_{PS} .

In Fig. 7(a), windings **P** and **S** are wound physically from the same end. This transformer construction can never achieve zero CM noise current flowing across C_{PS} because it is constructed in a way that whenever a switching action occurs, both windings experience the same direction of noise magnitude along the bobbin, and the zero equipotential condition cannot be satisfied for any N_{PS} value. When winding **A** is introduced in Fig. 7(b) with turns N_A , it must be in antiphase of both windings **P** and **S**; to meet the zero equipotential state, the balanced

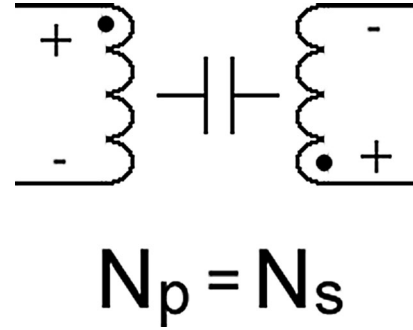
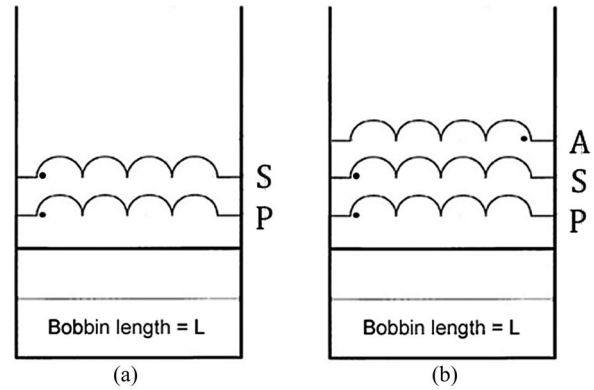


Fig. 6. Windings **P** and **S** wound in antiphase.



Equivalent Circuit Model

V1 = Switching noise source from the primary winding **P**

V2 = Switching noise source from the secondary winding **S**

V3 = Switching noise source from the anti-phase winding **A**

C1 = C_{PS}

C2 = $C_{PS} + C_{AS}$

C3 = C_{AS}

Y = A bypass capacitor used for measurement purpose

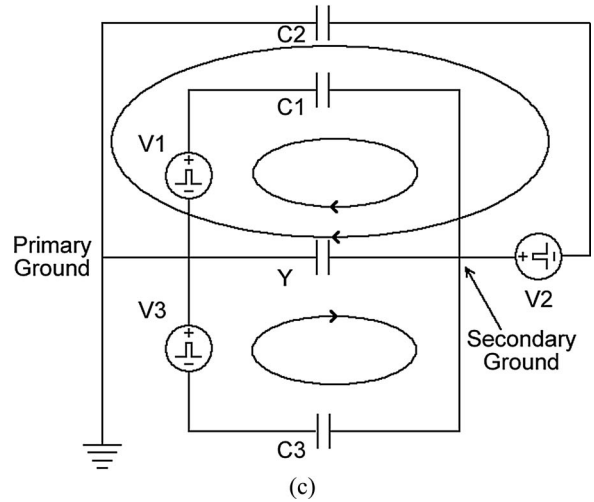


Fig. 7. (a), (b) Alternative winding phase arrangement of a typical flyback or forward converter and the additional antiphase winding with its (c) equivalent noise model.

condition is

$$V_P(C_1) + V_S(C_2) - V_A(C_3) = 0 \quad (3)$$

$$\therefore V_P(C_1) + \frac{1}{N_{PS}}V_P(C_2) - \frac{1}{N_{PA}}V_P(C_3) = 0.$$

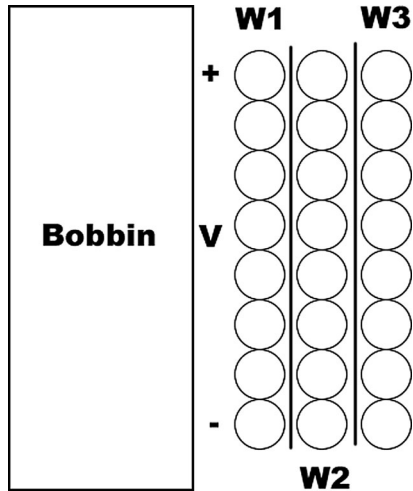


Fig. 8. Cross section of a three-layered transformer.

$$\begin{aligned} \therefore C_1 + \frac{1}{N_{PS}} C_2 &= \frac{1}{N_{PA}} C_3 \\ \therefore C_1 + \frac{1}{N_{PS}} (C_1 + C_3) &= \frac{1}{N_{PA}} C_3 \\ \therefore C_{AS} &= \frac{(N_{PS} + 1)}{((N_{PS}/N_{PA}) - 1)} C_{PS}. \end{aligned} \quad (4)$$

Equation (4) shows that if $N_{PS}/N_{PA} = N_A/N_S = 1$, i.e., $N_A = N_S$, then $C_{AS} = \infty$, i.e., the extra winding A alone cannot cut off the noise. Also, for a valid positive value of C_{AS} , $N_{PS}/N_{PA} = N_A/N_S > 1$, i.e., $N_A > N_S$.

III. WINDING LAYER ELECTRICAL SHIELDING EFFECT

When a transformer is constructed with multiple winding layers, inherently, there is an electric shielding effect applied between layers that are not adjacent to each other. Fig. 8 shows the cross section of a three-layered transformer, when there is a switching voltage V generated across $W1$, if winding $W2$ is tied to the same quiet node as $W1$, effectively, it acts as an electric shield between winding $W1$ and $W3$. CM current from $W1$ will be injected into $W2$. $W2$ is not the same as an electrical shield with a fixed potential since $W2$ will have a defined switching voltage as well as $W1$, and the CM current injected to $W3$ can be assumed to be influenced by $W2$ only.

Now, if winding P is wound in between windings A and S instead of the P, S, A configurations shown in Figs. 5(b) and 7(b), then influence from winding A to S will be effectively shielded by winding P , and winding S cannot see the switching potential from winding A . Therefore, the winding A, P, S configuration cannot achieve zero equipotential line along winding S .

IV. WINDING CONSTRUCTION TECHNIQUES IN DIFFERENT CONVERTER TOPOLOGIES

Two scenarios shown in Figs. 5 and 7 have been presented in common SMPS flyback and forward topologies and their corresponding winding techniques and balancing conditions that effectively cut off most CM noise across the isolated trans-

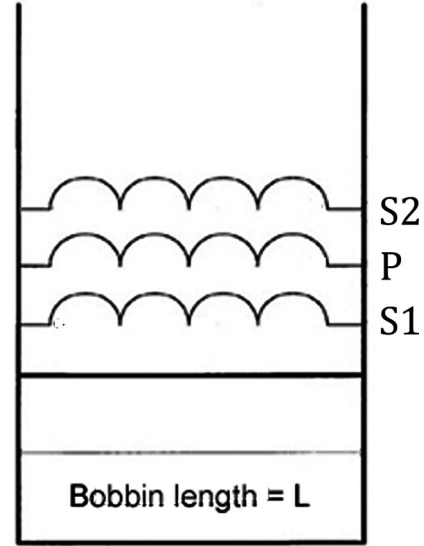


Fig. 9. Winding arrangement of a typical half-bridge or full-bridge converter.

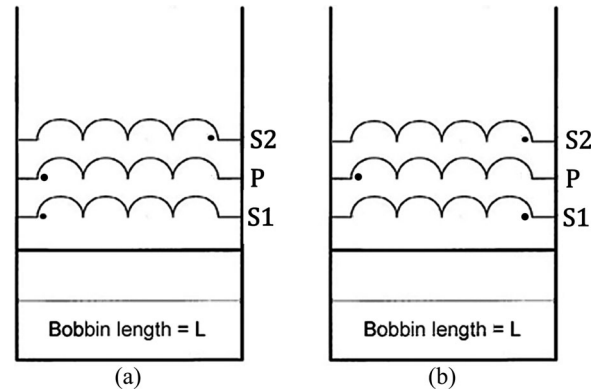


Fig. 10. (a), (b) Winding arrangements of a typical bridge transformer.

former. In the following section, different topologies are explored: bridge converters with a primary winding and two secondary windings, and push-pull converters with two primary windings and two secondary windings.

A. Bridge Converters

A common half-bridge or full-bridge converter has a primary winding P incorporated with two secondary windings $S1$ and $S2$, as shown in Fig. 9. For simplicity, each winding is assumed to have occupied the full width of the bobbin and $N_P > N_S$ is also assumed.

There are a few possible winding constructions for bridge converters. In normal designs, two secondary windings are constructed in a way that sandwich the primary winding to maximize the coupling capacitances. Windings $S1$ and $S2$ are assumed to have the same number of turns N_S and $S1$ and $S2$ can be wound in the same phase or in antiphase as shown in Fig. 10(a) and (b).

In Section II, zero equipotential along the secondary winding was discussed, and if this is applied in the earlier construction, then $S1$ and $S2$ should both see a zero switching potential so

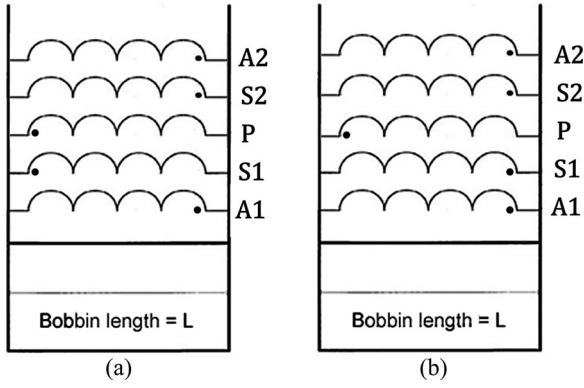


Fig. 11. (a), (b) Winding arrangements of a typical bridge transformer with antiphase windings.

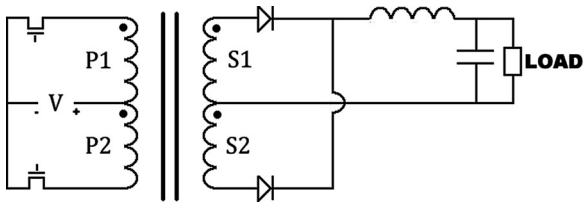


Fig. 12. Typical push-pull converter.

that the CM noise can effectively be eliminated. Therefore, two antiphase windings **A1** and **A2** are required in this particular case, as shown in Fig. 11(a) and (b).

In Fig. 11(a), due to the winding shielding effect, influence from winding **A2** to **S1** or winding **A1** to **S2** is blocked by winding **P**, and the equivalent circuit model can be assumed to be split into two groups of windings, namely windings **P**, **S1**, and **A1** and windings **P**, **S2**, and **A2**.

The windings group **P**, **S1**, and **A1** has a similar equivalent circuit to that shown in Fig. 7(b), whereas the windings group **P**, **S2**, and **A2** has a similar equivalent circuit to that shown in Fig. 5(b). Therefore, the zero equipotential condition on winding **S1** in Fig. 11(a) is

$$C_{A1S1} = \frac{(N_{PS1} + 1)}{((N_{PS1}/N_{PA1}) - 1)} C_{PS1}. \quad (5)$$

On winding **S2**, the zero equipotential condition is

$$C_{A2S2} = \frac{(N_{PS2} - 1)}{((N_{PS2}/N_{PA2}) + 1)} C_{PS2}. \quad (6)$$

In Fig. 11(b), which is similar to Fig. 11(a), except that the group windings **P**, **S1**, and **A1** is now

$$C_{A1S1} = \frac{(N_{PS1} - 1)}{((N_{PS1}/N_{PA1}) + 1)} C_{PS1}. \quad (7)$$

B. Push-Pull Converters

The transformer structure of a general push-pull converter shown in Fig. 12 consists of two primary windings **P1** and **P2** with same number of turns N_P and two secondary windings **S1** and **S2** with same number of turns N_S .

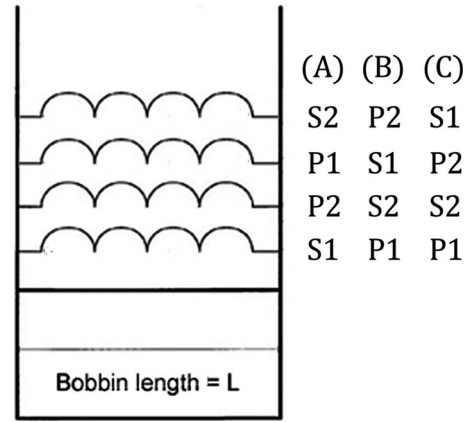


Fig. 13. Winding combinations of a push-pull converter.

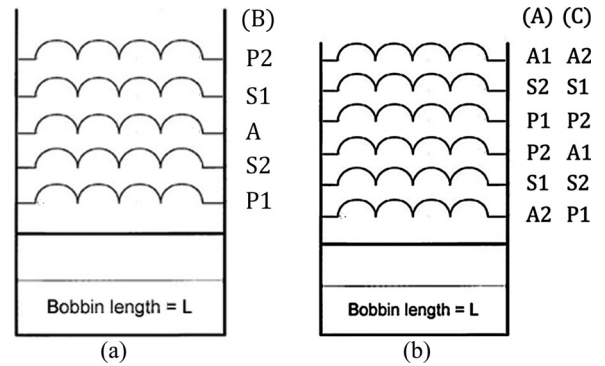


Fig. 14. (a), (b) Winding combinations in a push-pull converter with antiphase windings.

There are quite a few possible winding configurations, but the three common configurations are shown in Fig. 13. With ordinary construction methods, all of the configurations in Fig. 13 require the same amount of winding space. If zero equipotential lines along the secondary windings are needed in the push-pull converter design, configurations A and C require two antiphase windings placed adjacent to **S1** and **S2** to form two **P**, **S**, **A** winding groups, whereas configuration B requires only one antiphase winding sandwiched between **S1** and **S2**.

Fig. 14(a) shows configuration B with an extra winding **A** that should be constructed so that it has the same winding turns as **P1** and **P2** and wound in antiphase to both **P1** and **P2**. By tuning the capacitances C_{AS1} and C_{AS2} depending on the winding direction, a similar analysis as described in (2) and/or (4) can be employed to achieve zero equipotential along **S1** and **S2**.

In the modified configurations A and C shown in Fig. 13(b), the windings can be separated into two winding groups: **P2**, **S1**, and **A2** and **P1**, **S2**, and **A1**. For these configurations, C_{AS1} and C_{AS2} must be determined. Windings **A1** and **A2** should be constructed in antiphase to **P1** and **P2**, respectively.

V. EXPERIMENTS

A flyback converter was built as described in Figs. 1 and 2 to test the proposed method. The experiments concentrate on meeting the zero equipotential line along the bobbin on the

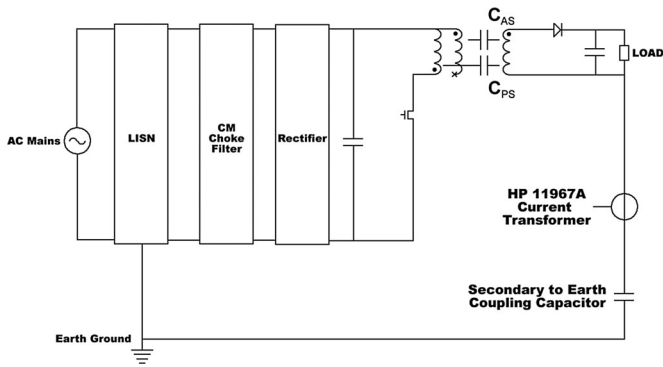


Fig. 15. Conducted EMI setup for CM noise measurement with HP 11967A current transformer.

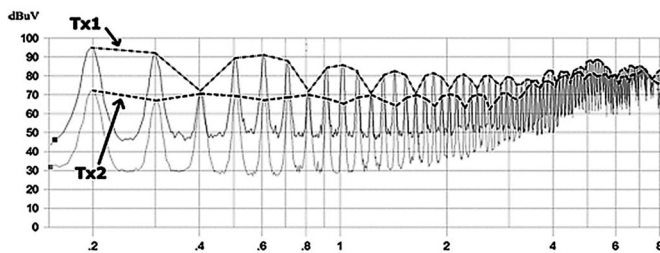


Fig. 16. Conducted EMI tests showing different CM noise reduction performance.

secondary winding. The switching frequency was 100 kHz and the converter had an input of 230-V ac, output 25-V dc, and an output of 1.5 A. Fig. 5 showed the transformer constructions of Figs. 1 and 2. The turns ratio was $N_{PS} = 3.90$.

A conducted EMI test from 100 kHz to 8 MHz was performed and a radio frequency current probe (HP 11967A) was employed to measure the noise current passed through the transformer primary–secondary coupling path. The setup is shown in Fig. 15. An initial test scan suggested that a small 2-mH CM filter is necessary to maximize the performance of the proposed method.

In Fig. 16, trace 1 shows the original transformer Tx1 performance as constructed in Fig. 5(a) with a 2-mH CM choke filter, but without the antiphase winding A. When the antiphase winding A was employed in Tx2 as constructed in Fig. 5(b), the EMI performance dramatically improved by about 20 dB at the frequencies below 1 MHz and the noise rejection was effective up to 8 MHz. The experimental result shows the theory proposed works effectively to reduce CM noise. To compare the performance of the antiphase winding method with the popular CM choke filter method, the CM EMI profile of the flyback converter with the antiphase winding and a small (2 mH) CM choke filter was recorded. Then, the antiphase winding was removed and the CM choke inductance is increased to produce a similar CM EMI profile. It was found out that a much bigger inductance (82 mH) was needed to suppress the CM current profile to the same level. Hence, the antiphase winding method can reduce the CM choke inductance by over 40 times. Such re-

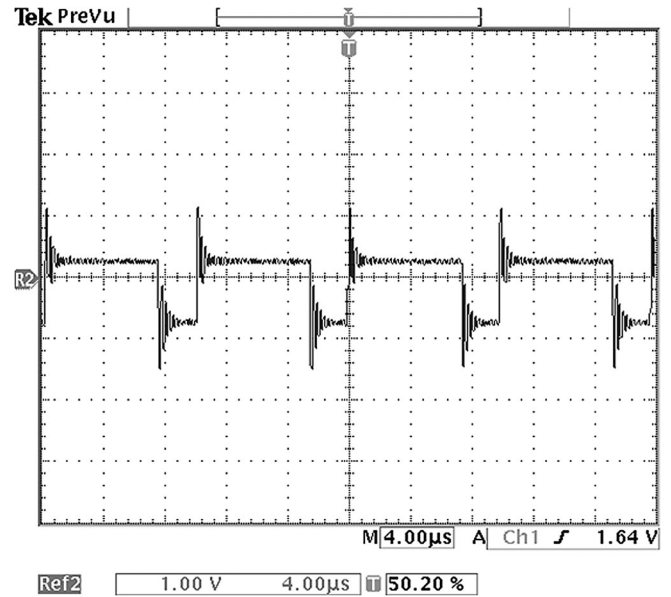


Fig. 17. Measurement from an isolated oscilloscope showing the noise measured in at 230-V ac.

duction can, therefore, reduce conduction loss in the CM choke filter effectively.

VI. PRACTICAL METHOD TO SHOW THE NOISE STABILIZATION ACROSS THE PRIMARY AND SECONDARY SIDE

In practical designs, EMI performance tends to be measured in the latter stage; hence, the antiwinding performance cannot be verified during the transformer design stage. The following measurement method can provide an insight to the CM noise cancellation in the switching frequency range. An isolated oscilloscope with earth ground disconnected should be used for this measurement to ensure the noise measured is purely due to the generation of the power-supply switching action. The isolated oscilloscope may have poor frequency characteristics at the high oscillating frequency, but the cancellation at the lower switching frequency can be clearly shown if the antiphase solution is effective. In this converter, the capacitance to earth ground was much smaller than the capacitance between the primary and secondary. A Y-type capacitor (Y-cap) was employed that was typically larger than the stray capacitance to the earth ground to allow most of the CM current to flow through it. The Y-cap was chosen to be 100 pF in this experiment to allow a low impedance path for CM mode noise while obtaining measurable results. Figs. 17 and 18 show the measurements across the Y-cap for a transformer with $C_{PS} = 80$ pF at 100 kHz. Equation (2) suggested $C_{AS} = 47.5$ pF at 100 kHz. Fig. 18 confirms that the switching frequency waveform was almost canceled along the path, and the spikes seen were caused by the slight mismatch of the high-frequency parasitic impedances. This result also matched with the EMI result in Fig. 16 showing significant noise suppression at low frequencies. Fig. 19 shows the CM noise path via the isolated transformer and the Y-Cap. The

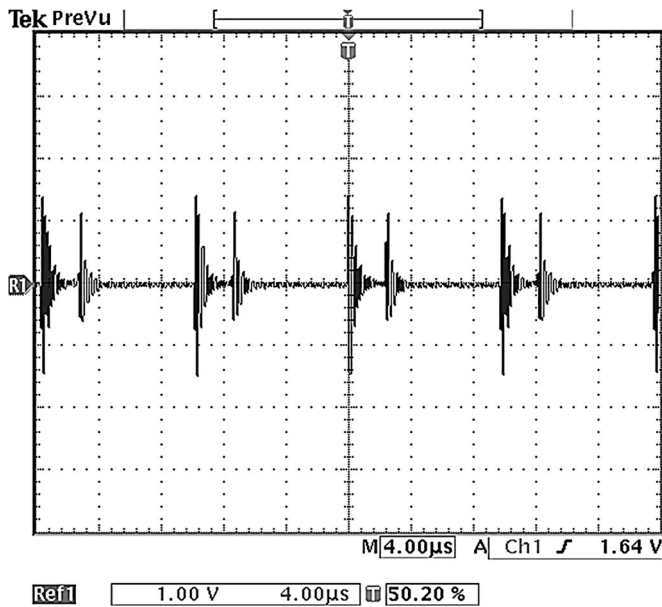


Fig. 18. Measurement from an isolated oscilloscope showing the noise measured in at 230-V ac.

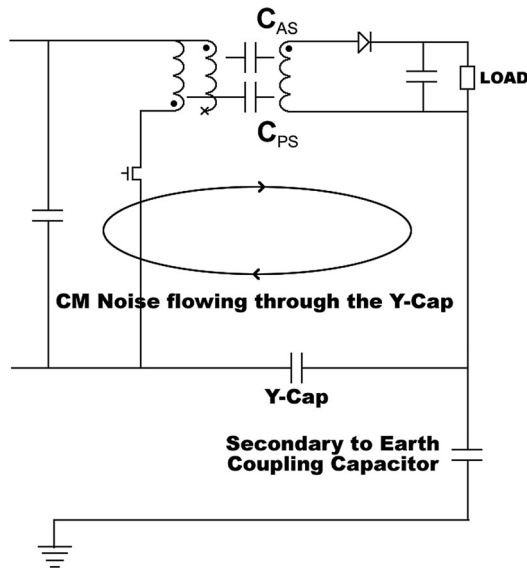


Fig. 19. CM noise path via the isolated transformer and the Y-Cap.

previous EMI result showed this noise rejection method is effective up to 8 MHz.

VII. CONCLUSION

In this paper, a special transformer construction technique is proposed. This technique employs the zero equipotential line theory to construct an antiphase winding. It effectively reduces CM noise by eliminating the noise voltage across the isolated primary and secondary windings. The concept of maintaining

an equipotential line along the bobbin and quiet node connections are justified with analyses. The antiphase winding is easy to design, and it does not carry high current which is advantageous over conventional CM noise filters. Detailed models for popular power converter topologies are analyzed and explained. Experimental results prove the effectiveness of this method and CM noise is reduced considerably. This method facilitates and provides a useful way to cancel noise passing through an isolated transformer, confirmed by the test results and conducted EMI tests. A CM noise current measurement is also proposed to aid in practical designs and provide useful insights on the CM noise passing through the transformer. A transformer design with the proposed CM noise cancellation technique can achieve high conversion efficiency as well as good noise immunization.

REFERENCES

- [1] F.-Y. Shih and D. Y. Chen, "A procedure for designing EMI filters for AC line applications," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 170–181, Jan. 1996.
- [2] M. Damnjanovic, G. Stojanovic, V. Desnica, L. Zivanov, R. Raghavendra, P. Bellew, and N. Mcloughlin, "Analysis, design, and characterization of ferrite EMI suppressors—Part II," *IEEE Trans. Magn.*, vol. 42, no. 2, pp. 270–277, Feb. 2006.
- [3] M. Damnjanovic, L. Zivanov, and G. Stojanovic, "Common mode chokes for EMI Suppression in Telecommunication Systems," in *Proc. Int. Conf. Comput. Tool*, Sep.9–12, 2007, pp. 905–909.
- [4] M. Damnjanovic, L. Zivanov, and G. Stojanovic, "Analysis of effects of material and geometrical characteristics on the performance of SMD common mode choke," in *Proc. 26th Int. Conf. Microelectron.*, May11–14, 2008, pp. 267–270.
- [5] A. Roc'h, H. Bergsma, D. Zhao, B. Ferreira, and F. Lefeink, "A new behavioural model for performance evaluation of common mode chokes," in *Proc. 18th Int. Zurich Symp. Electromagn. Compat.*, Sep. 24–28, 2007, pp. 501–504.
- [6] A. Roc'h, H. Bergsma, D. Zhao, B. Ferreira, and F. Lefeink, "Comparison of evaluated and measured performances of common mode chokes," in *Proc. Int. Symp. Electromagn. Compat.*, Sep.8–12, 2008, pp. 1–5.
- [7] N. Mortensen and G. Venkataraman, "An active common mode EMI Filter for switching converters," in *Proc. IEEE Ind. Appl. Soc. Annu. Meet.*, Oct.5–9, 2008, pp. 1–7.
- [8] P. Chen, H. Zhong, Z. Qian, and Z. Lu, "The passive EMI cancellation effects of Y capacitor and CM model of transformers used in switching mode power supplies (SMPS)," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, Jun. 20–25, 2004, vol. 2, pp. 1076–1079.
- [9] D. Cochrane, D. Y. Chen, and D. Boroyevic, "Passive cancellation of common-mode noise in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 1, no. 3, pp. 756–763, May 2003.
- [10] E. Herbert, "Transformer for switched mode power supplies and similar applications," U.S. Patent 6 137 392, Oct. 24, 2000.
- [11] S. Wang and F. C. Lee, "Common-mode noise reduction for power factor correction circuit with parasitic capacitance cancellation," *IEEE Trans. Electromagn. Compat.*, vol. 49, no. 3, pp. 537–542, Aug. 2007.
- [12] W. Xin, N. K. Poon, C. M. Lee, M. H. Pong, and Z. Qian, "A study of common mode noise in switching power supply from a current balancing viewpoint," in *Proc. IEEE Power Electron. Drive Syst. Conf.*, Jul. 1999, vol. 2, pp. 621–625.
- [13] C. P. Liu, M. H. Pong, and N. K. Poon, "Apparatus for reducing common mode noise current in power converters," U.S. Patent 6 490 181, Dec. 3, 2002.
- [14] W. Xin, M. H. Pong, Z. Y. Lu, and Z. M. Qian, "Novel boost PFC with low common-mode EMI: Modeling and design," in *Proc. IEEE Appl. Power Electron. Conf.*, New Orleans, LA, 2000, pp. 178–181.
- [15] S. Wang, P. Kong, and F. C. Lee, "Common mode noise reduction for boost converters using general balance technique," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun.18–22, 2006, pp. 3142–3147.



Yick Po Chan (S'05) received the M.Eng. degree in electrical and electronic engineering from Imperial College London, London, U.K., in 2003. He is currently working toward the Ph.D. degree at the Power Electronics Laboratory, The University of Hong Kong, Hong Kong.

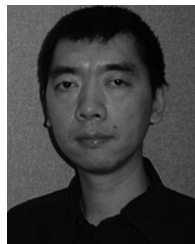
He was with the PowerELab Ltd., Hong Kong, as a Design Engineer. His research interests include transformer modeling, electromagnetic interference (EMI) reduction techniques, EMI filter modeling, and design optimization.



Bryan Man Hay Pong (M'84–SM'96) was born in Hong Kong. He received the B.Sc. degree in electronic and electrical engineering from the University of Birmingham, Birmingham, U.K., in 1983, and the Ph.D. degree in power electronics from Cambridge University, Cambridge, U.K., in 1987.

He was with National Semiconductor Hong Kong as a Senior Design Engineer and then a Chief Design Engineer. He was also with ASTEC International as a Principal Engineer and a Division Engineering Manager. He is currently an Associate Professor at The

University of Hong Kong, Hong Kong. He is in charge of the Power Electronics Laboratory. He has co-invented a number of patents. His research interests include high-efficiency and high-reliability power conversion, electromagnetic interference reduction techniques, magnetic components, and other aspects of switch-mode power conversion.



Ngai Kit Poon (M'95) received the B.Eng.(Hons.) degree in electronic engineering from the City University of Hong Kong, Hong Kong, in 1995, and the Ph.D. degree from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 2003.

After graduation, he was with Artesyn Technologies (Asia Pacific) Limited for three and a half years before joining the Power Electronics Laboratory, The University of Hong Kong, Hong Kong, then becomes the Co-Founder of PowerELab Ltd., Hong Kong, a spinoff company from The University of Hong Kong.

He is the key inventor of more than 20 patents, and 50 journal and conference paper have been published. He is the founder of the Web-based software PowerEsim. His current interest includes soft-switching techniques, electromagnetic interference modeling, power factor correction topologies, synchronous rectification, converter modeling, pulsewidth modulated inverters, simulation technique, and fast transient regulators.



Joe Chui Pong Liu received the B.Eng. degree in electrical and electronic engineering from The University of Hong Kong, Hong Kong, in 1993, and the Ph.D. degree from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 2007.

He is currently the Chief Technical Officer in the PowerELab Ltd., Hong Kong, a spinoff company from The University of Hong Kong. His current research interests include soft-switching techniques, rectifierless ac to dc conversion, synchronous rectification, converter modeling, inverters, and digital

control.