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<td><strong>Citation</strong></td>
<td>IEEE Electron Device Letters, 2008, v. 29 n. 10, p. 1155-1158</td>
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<tr>
<td><strong>Issued Date</strong></td>
<td>2008</td>
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<td><strong>URL</strong></td>
<td><a href="http://hdl.handle.net/10722/58727">http://hdl.handle.net/10722/58727</a></td>
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Improved Electrical Properties of Ge p-MOSFET With HfO$_2$ Gate Dielectric by Using TaO$_x$N$_y$ Interlayer

J. P. Xu, X. F. Zhang, C. X. Li, P. T. Lai, and C. L. Chan

Abstract—The electrical characteristics of germanium p-metal-oxide–semiconductor (p-MOS) capacitor and p-MOS field-effect transistor (FET) with a stack gate dielectric of HfO$_2$/TaO$_x$N$_y$ are investigated. Experimental results show that MOS devices exhibit much lower gate leakage current than MOS devices with only HfO$_2$ as gate dielectric, good interface properties, good transistor-characteristics, and about 1.7-fold hole-mobility enhancement as compared with conventional Si p-MOSFETs. These demonstrate that forming an ultrathin passivation layer of TaO$_x$N$_y$ on germanium surface prior to deposition of high-$k$ dielectrics can effectively suppress the growth of unstable GeO$_x$, thus reducing interface states and increasing carrier mobility in the inversion channel of Ge-based transistors.

Index Terms—Germanium, high-$k$, pMOSFET, TaON interlayer.

I. INTRODUCTION

With the continual scaling down of the dimensions of metal–oxide–semiconductor field-effect transistor (MOSFET), high-$k$ metal–oxide dielectrics, e.g., HfO$_2$ and ZrO$_2$, are used to replace SiO$_2$ as gate dielectric to reduce gate leakage, and also, high-mobility semiconductor such as germanium is used as channel material to increase the operating speed of the devices. High-quality insulator/channel interface is desirable for high-$k$/Ge MOS devices [1]–[4]. Kim et al. [5] reported that an ultrathin nitride interlayer (AlN: $k \sim 9$ and Hf$_3$N$_4$: $k \sim 20$) inserted between HfO$_2$ and germanium substrate could effectively passivate the Ge surface and increase the $k$ value of the stacked gate dielectric as compared to the case with GeO$_x$N$_y$ as interlayer. Sugawara et al. [6] demonstrated that Ge MOS capacitor with ALD HfO$_2$ and plasma-synthesized TaON interlayer showed superior electrical properties. Since TaO$_x$N$_y$ has a high $k$ value of $\sim 26$ [7], [8] and high thermal stability, it should be a promising candidate as an interlayer between high-$k$ dielectric and Ge substrate. In this letter, Ge-based MOS capacitors and MOSFETs with Al/HfO$_2$/TaO$_x$N$_y$ stack gate are fabricated. Measurements show that, owing to the passivation role of the TaO$_x$N$_y$ interlayer, excellent electrical properties with low gate leakage current, low interface-state density, good output characteristics, and high hole mobility can be obtained for the HfO$_2$/TaO$_x$N$_y$ gate-dielectric p-MOSFET when compared with its counterpart without the passivation layer.

II. EXPERIMENTS

Ring-structure p-MOSFETs were fabricated on n-type (100) Ge wafers (0.1–0.2 Ω·cm) from Umicore, using a self-aligned technology. Before depositing the gate dielectric, Ge wafers were cleaned using semiconductor-grade trichloroethylene, acetone, and ethanol for 5 min, respectively, and rinsed with DI water several times, followed by 15-s diluted HF (1:50) dipping and 15-s DI water rinsing for five cycles to remove Ge native oxide. The rms surface roughness of the Ge wafers after cleaning was 0.14–0.15 nm for a 5-μm$^2$ area, which was measured by AFM. After drying in N$_2$, the wafers were immediately transferred into the Denton Vacuum Discovery Deposition System. TaN$_x$ of 1.0 nm was deposited by reactive sputtering of Ta in an Ar/N$_2$ (12:18) ambient, followed by the deposition of a nominal 9.0-nm HfO$_2$ by reactive sputtering of Hf in an Ar/O$_2$ (24:6) ambient. For comparison, a nominal 9.0-nm HfO$_2$ was directly deposited on the cleaned Ge substrate without the TaN$_x$ layer to make the control sample. A postdeposition annealing (PDA) was carried out in wet N$_2$ at 500 °C for 5 min to improve the dielectric quality, transform TaN$_x$ into Ta$_2$O$_x$N$_y$ [9], and also suppress the formation of unstable GeO$_x$ [10]. The wet N$_2$ atmosphere was realized by bubbling pure N$_2$ through DI water at 95 °C with a flow rate of 500 mL/min. Subsequently, Al was e-beam evaporated, and ring gate electrode with inner and outer radii of 45 and 145 μm (so, the gate length = 100 μm) was patterned using optical lithography and etched in diluted H$_2$PO$_4$. Then, the samples were divided into the following two groups: one for fabrication of capacitors, and another for preparation of p-MOSFETs. For the p-MOSFETs, source/drain regions were formed by accurately timing the etching of the high-$k$ dielectric in a CF$_4$-based plasma, followed by a self-aligned BF$_2$ implantation at 20 keV with a dose of $4 \times 10^{15}$ cm$^{-2}$. Source/drain electrodes were formed by e-beam evaporation of Al through a lift-off process. Finally, dopant activation and forming-gas annealing were simultaneously completed in H$_2$/N$_2$ (5% H$_2$) for 20 min.

Manuscript received June 26, 2008. Current version published September 24, 2008. This work was supported in part by the National Natural Science Foundation of China under Grant 60776016 and in part by the Small Project Funding of the University of Hong Kong under Grant 200707176147, and the University Development Fund (Nanotechnology Research Institute) of the University of Hong Kong under Grant 00660009. The review of this letter was arranged by Editor M. Ostling.

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Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2008.2004282
Fig. 1. Normalized HF $C-V$ curves of the HfO$_2$/Ge and HfO$_2$/TaO$_x$N$_y$/Ge MOS capacitors, with nominal HfO$_2$ thickness of 9.0 nm and nominal TaO$_x$N$_y$ thickness of 1.0 nm. The inset is their gate leakage current density.

Fig. 2. TEM photograph of the HfO$_2$/Ge MOS sample after PDA, showing the formation of an unstable GeO$_x$ interlayer. 

at a low temperature of 400 °C to suppress Al diffusion into the gate dielectrics.

III. RESULTS AND DISCUSSION

Fig. 1 shows the typical HF (1-MHz) $C-V$ curves of the HfO$_2$/Ge (denoted as nonpassivated sample) and HfO$_2$/TaO$_x$N$_y$/Ge (denoted as passivated sample) MOS capacitors. The total physical thicknesses of their dielectrics are 10.0 and 10.4 nm, respectively, measured by multiwavelength ellipsometer, in which the Cauchy model and light wavelengths ranging from 400 to 1000 nm with incidence angles of 65°, 70°, and 75° were used to obtain the film thickness. A 2.0–2.2-nm GeO$_x$ interlayer, formed between the high-$k$ dielectric and substrate, is estimated from the TEM photograph of the nonpassivated sample shown in Fig. 2. For the passivated sample, a 0.4-nm increase in dielectric thickness after PDA should be ascribed to the conversion of the TaN$_x$ layer to a TaO$_x$N$_y$ passivation layer. Although the nonpassivated sample physically has a thinner gate dielectric than the passivated one, it has a larger capacitance equivalent thickness extracted from the accumulation capacitance ($C_{ox}$) in Fig. 1 than the latter (3.9 versus 2.6 nm) due to the lower $k$ value of its GeO$_x$ interlayer. A small distortion occurs in the weak inversion region of the $C-V$ curve for the nonpassivated sample, indicating that there exists a large amount of interface states. This is supported by the $D_{it}$ distribution in bandgap, as shown in Fig. 3. The inset in Fig. 1 shows the leakage current density of the two MOS capacitors. The leakage current density of the nonpassivated sample at $V_g = V_{fb} + 1$ V is about one order of magnitude larger than that of the passivated sample, which should be related to the growth of a GeO$_x$ interlayer leading to a large $D_{it}$ and, thus, larger interface-trap-assisted tunneling current [11] (the HfO$_2$/TaO$_x$N$_y$/Ge sample in [6] has smaller leakage current mainly because HfO$_2$ prepared by ALD has better dielectric quality, hence having smaller $D_{it}$ and $Q_{ox}$). Thus, an ultrathin TaO$_x$N$_y$ interlayer inserted between the high-$k$ dielectric and Ge substrate can effectively suppress the formation of unstable GeO$_x$, leading to improved interface properties for MOS devices. Fig. 3 shows the frequency dependence of $C-V$ curves measured at frequencies ranging from 1 to 800 kHz, and the interface-state distribution in the bandgap of germanium. The normal conductance method [12] was used to extract $D_{it}$'s just for the purpose of a relative comparison between the samples, although it has been shown to produce numerically inaccurate results for germanium [13]–[16]. The $D_{it}$ near the midgap for the passivated sample is $5 \times 10^{11} - 1 \times 10^{12}$ eV$^{-1} \cdot$ cm$^{-2}$, which is much smaller than that for the nonpassivated sample ($3.2 \times 10^{12} - 4.6 \times 10^{12}$ eV$^{-1} \cdot$ cm$^{-2}$).

The output characteristics of the p-MOSFETs are shown in Fig. 4. The HfO$_2$/TaO$_x$N$_y$ gate-dielectric p-MOSFET shows a larger $I_d$ than that of the HfO$_2$ gate-dielectric p-MOSFET. This should be attributed to the larger oxide capacitance (see Fig. 1)
higher carrier mobility (see hereafter) of the former device.

The effective hole mobility ($\mu_{\text{eff}}$) of the two Ge p-MOSFETs was extracted from the linear region of the $I_d-V_{gs}$ curves of the MOSFET with a gate length of 100 $\mu$m, which is shown as an inset of Fig. 5. From the $I_d-V_{gs}$ formula, $\mu_{\text{eff}}$ can be written as [17]

$$\mu_{\text{eff}} = \frac{I_d}{(W_{\text{eff}}/L)C_{\text{ox}}(V_{gs} - V_{th})V_{ds}}$$

and effective field ($E_{\text{eff}}$) is expressed as [18]

$$E_{\text{eff}} = \frac{Q_{\text{dep}} + \eta Q_{\text{inv}}}{\varepsilon_s}$$

$$\approx \frac{C_{\text{ox}}(V_{gs} - (1 - \eta)(V_{gs} - V_{th}))}{\varepsilon_s}$$

where $Q_{\text{inv}} \approx C_{\text{ox}}(V_{gs} - V_{th})$, $Q_{\text{dep}} = E_{\text{ox}}\varepsilon_{\text{ox}} - Q_{\text{inv}}$, $E_{\text{ox}} \approx V_{gs}/t_{\text{ox}} = V_{gs}C_{\text{ox}}/\varepsilon_{\text{ox}}$, $\varepsilon_s$ is the permittivity of Ge substrate, and $\eta = 0.3$ is the fitting parameter [17], [18]. The effective channel width $W_{\text{eff}}$ is calculated to be 537 $\mu$m [18]. For comparison, the universal hole-mobility curve for conventional Si p-MOSFETs is also shown in Fig. 5. At low effective field, the $\mu_{\text{eff}}$ of the HfO$_2$/TaO$_x$N$_y$/Ge MOSFET exhibits $\sim$1.7-fold enhancement when compared with the hole mobility of conventional Si p-MOSFETs. A peak mobility of 225 $\text{cm}^2/\text{V} \cdot \text{s}$ at 0.2 $\text{MV/cm}$ is observed in Fig. 5. On the other hand, the effective hole mobility of the HfO$_2$/Ge MOSFET is seriously degraded when compared with that of the HfO$_2$/TaO$_x$N$_y$/Ge sample. This should be mainly attributed to enhanced hole scattering arising from more interface states (see larger $D_{\text{it}}$ in Fig. 3), larger oxide leakage in Fig. 1, and larger subthreshold swing in Fig. 5) and possibly larger interface roughness associated with growth of the unstable GeO$_x$ interlayer (see Fig. 2). Thus, it can be suggested that the ultrathin TaO$_x$N$_y$ interlayer between the high-$k$ dielectric and Ge substrate can effectively improve the interface quality (lower interface-state density) and thus significantly enhance the carrier mobility (roughly 1.7 times). In addition, from the $I_d-V_{gs}$ curve, the threshold voltage ($V_{th}$) and subthreshold swing are extracted to be $-0.120 \text{ V}$ and $114 \text{ mV/decade}$ for the HfO$_2$/TaO$_x$ gate-dielectric p-MOSFET, and $-0.098 \text{ V}$ and $157 \text{ mV/decade}$ for the HfO$_2$ gate-dielectric p-MOSFET, respectively. The small negative $V_{th}$ value, particularly for the nonpassivated sample, is due to the high negative-oxide-charge densities ($Q_{\text{ox}}$)’s extracted from the HF $C-V$ in Fig. 1, which are $-9.7 \times 10^{-11}$ and $-2.1 \times 10^{12} \text{ cm}^{-2}$ for the HfO$_2$/TaO$_x$N$_y$/Ge and HfO$_2$/Ge capacitors, respectively. The smaller subthreshold swing of the HfO$_2$/TaO$_x$ p-MOSFET shows better interface quality, which is consistent with the results in Fig. 3(b). A possible origin of the negative oxide charges is the wet ambient of the PDA, which can introduce hydroxyl ions in the gate dielectric [10]. It is expected that further improvements in the electrical properties of the devices can be obtained if the device structure and processing conditions are optimized, e.g., higher activation temperature or longer activation time for the source/drain implant to activate more dopants, and rectangular gate (smaller than the ring gate) resulting in smaller transistor, thus having smaller gate leakage current and smaller S/D leakage current.

IV. SUMMARY

Germanium-based p-MOS capacitors and p-MOSFETs with high-$k$ materials as gate dielectric were fabricated. The MOS devices with HfO$_2$/TaO$_x$N$_y$ stack gate dielectric demonstrate excellent electrical properties, such as low interface-state density, small gate leakage current, and good output and transfer characteristics when compared with the control samples with HfO$_2$ gate dielectric, and also an $\sim$1.7-fold hole-mobility enhancement relative to the universal hole mobility of Si p-MOSFET. All these are due to the ultrathin TaO$_x$N$_y$ interlayer, which can effectively passivate the dielectric/germanium interface. Therefore, HfO$_2$/TaO$_x$N$_y$ stack gate dielectric should be a promising high-$k$ gate dielectric structure for fabricating high-speed Ge-based MOSFETs in the future.
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