2012-12

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SOLID-STATE ELECTRONICS, OXFORD, v. 78, n. 1, Special Issue, pp. 141-146, DEC, 2012
http://www.producao.usp.br/handle/BDPI/35150

Solid-State Electronics 78 (2012) 141–146

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Temperature impact on the tunnel fet off-state current components

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ARTICLE INFO

Article history:
Available online 29 June 2012

Keywords:
Triple gate SOI tunnel FETs
Off-state current components
Temperature
Ambipolar behavior
SRH
TAT

ABSTRACT

In this work, the temperature impact on the off-state current components is analyzed through numerical simulation and experimentally. First of all, the band-to-band tunneling is studied by varying the underlap in the channel/drain junction, leading to an analysis of the different off-state current components. For pTFET devices, the best behavior for off-state current was obtained for higher values of underlap (reduced BTBT) and at low temperatures (reduced SRH and TAT). At high temperature, an unexpected off-state current occurred due to the thermal leakage current through the drain/channel junction. Besides, these devices presented a good performance when considering the drain current as a function of the drain voltage, making them suitable for analog applications.

1. Introduction

During the last decades, MOSFET devices have been continuously scaled down, so that they reached the nanoscale domain. Meanwhile, in the most recent technological nodes of tens of nanometers, CMOS devices are facing fundamental physical limits and innovations are needed to further improve their performance. The implementation of advanced processing modules and new materials has to be complemented with alternative device concepts.

Short-channel effects and leakage currents, for instance, are very important issues, leading to an impending power crisis [1]. This power dissipation issue can be explained by analyzing the dynamic ($C_{total} \times V_{DD}^2 \times f$) and static ($I_{OFF} \times V_{DD}$) power components, where C_{total} is the equivalent capacitance, V_{DD} the supply voltage, f the switching frequency and I_{OFF} is the sum of the leakage currents when the device is in the off-state.

Therefore, it is key that the V_{DD} should be minimized in order to preserve the expected technological scaling [2]. The threshold voltage should also decrease in order to guarantee that the device will be turned on and provides sufficient drive current for the specified supply voltage.

On the other hand, even with the introduction of new materials like high-k dielectrics in combination with metal gates and a consequent reduction in gate leakage current, further scaling of the supply voltage is still limited by the subthreshold swing value of $k \cdot T/q \cdot \ln(10)$. In other words, the change of the materials does not avoid the influence of the transport mechanism in the subthreshold regime, governed by carrier diffusion over a thermal barrier and, therefore, limiting the subthreshold swing to 60 mV/dec at room temperature [3].

Taking all the mentioned points into consideration, alternative approaches are being pursued and devices with different operation principles show promising options. In this context, tunnel field effect transistors (TFETs) have been proposed as a solution for low power applications [4].

These devices, designed as a Si-based gated *p-i-n* diode, present lower subthreshold swing and reduced short-channel effects, since their conduction mechanism is based on band-to-band tunneling (BTBT) controlled by the gate [5] at the channel/source junction. Besides, the TFET structural similarity with a multiple gate SOI FET allows their implementation using standard FinFET processing techniques [6]. Previewing future applications, it is worth remembering that based on vertical nanowires [7] these devices enable the fabrication of 3D structures as well.

Regardless this optimistic prospective, tunnel field effect transistors have to face two major issues, namely the intrinsic ambipolarity and the low I_{ON} current. Ambipolarity is an undesirable characteristic since it is responsible for the exponential increase of the off-state current due to the BTBT current that occurs at the channel/drain junction under specific bias conditions. This behavior is a relevant issue for digital applications, when on- and off-state must be clearly defined. Meanwhile, low I_{ON} current could reduce the switching frequency, since this would minimize the I_{ON}/I_{OFF} ratio. Some strategies related to physical dimensions or sophisticated techniques have been recently proposed in order to overcome these concerns [8].

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http://dx.doi.org/10.1016/j.sse.2012.05.053

Since TFETs have attracted considerable attention from the scientific community due to its great potential for digital applications (perfect switch), an extensive study of the behavior of TFETs has been developed. The study of the temperature influence on the TFETs performance is mainly based on the band to band tunneling [5,9], which is the main transport mechanism of these devices. However, the temperature influence on off-state current and on its components must be also investigated in order to obtain a better understanding of the TFETs behavior as a function of temperature. Considering all these technological evolutions, the goal of this work is to study some relevant pTFET physical features and to analyze the temperature influence on the device current mainly in the off-state region, including ambipolarity effect, SRH (Shockley–Read–Hall) and TAT (Trap Assisted Tunneling) components.

2. Device characteristics

The studied triple-gate pTFET devices were fabricated on a (100) SOI substrate with 65 nm thick Si on top of a 145 nm Buried Oxide. Fin widths down to 25 nm were patterned using 193 nm optical lithography and aggressive resist and hardmask trimming. The channel of the device was left undoped which results in a natural wafer doping ($N_a = 1 \times 10^{15}$ cm^{-3}) [10]. The gate stack consists of a 100 nm poly silicon layer on top of a 5 nm TiN layer and a 2 nm HfO_2 on a 1 nm interfacial oxide. Atomic layer deposition was used for the high-k deposition while metal chemical vapor deposition was used for the deposition of the metal gate. After gate patterning, complementary source/drain doping was obtained by an extension implantation of arsenic and boron with 45° parallel to the gate using a modified mask design (Fig. 1).

Extension implantations were done through an oxide of 5 nm with an energy of 5 keV for As with dose of 1×10^{15} at/cm^2 and with an energy of 1 keV for B with dose 1.5×10^{15} at/cm^2. Next 35 nm wide nitride spacers were formed. Next, the source/drain regions outside the spacers were highly doped using the same mask design with a 0° tilt. For the n-type doping an As dose of 3×10^{15} at/cm^2 was implanted with an energy of 25 keV and a P dose of 2×10^{15} at/cm^2 with an energy of 8 keV. For p-type doping, a B dose of 3×10^{15} at/cm^2 was implanted with an energy of 3 keV. After a 1050 °C spike anneal and the formation of a 14 nm thick nickel monosilicide in the source/drain regions standard Cu back-end processing was used. A TEM image of a gate sidewall on top of the fin is shown in Fig. 2.

Measurements were performed as a function of temperature from 300 K up to 420 K, using an Agilent 4156C semiconductor parameter analyzer.

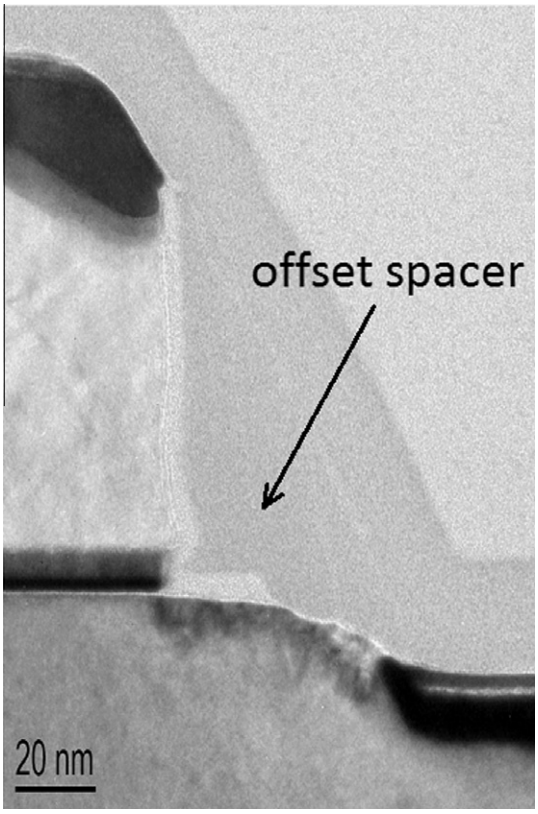

Fig. 2. TEM image of a gate sidewall on top of the fin.

Numerical simulations with Atlas [11] were performed to better understand the influence of physical characteristics on its behavior. The modified parameters for the selected models used in the numerical simulations in this work will be shown just below the expression used. A schematic view of the device is shown in Fig. 3.

3. Analysis and discussions

A conventional pTFET is a gated p-i-n diode whereby the gate is self-aligned with the drain which results in a small gate-drain/drain overlap region. This device configuration leads to a high undesirable ambipolar current. In order to analyze the ambipolar current, simulations were performed varying the gate length near

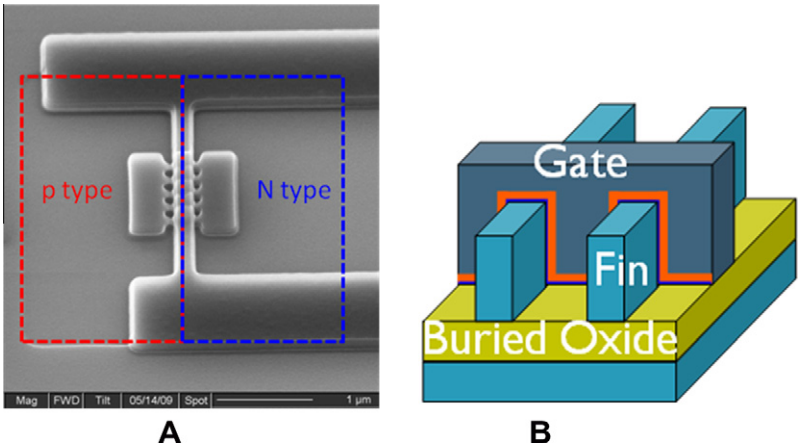

Fig. 1. (A) SEM image of the measured TFETs with a schematic doping implementation. (B) Schematic representation of MuGFET device with the same characteristics of TFET one.

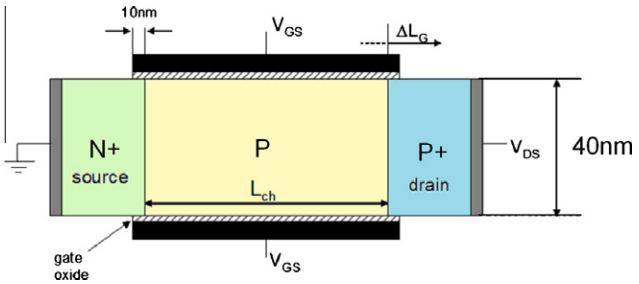

Fig. 3. Schematic representation of a pTFET device.

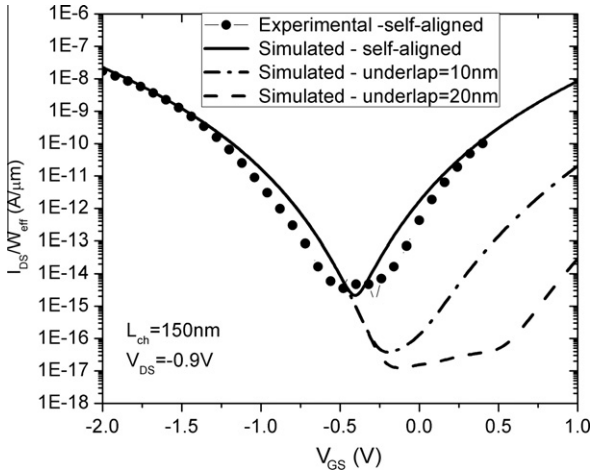

Fig. 4. Drain current as a function of gate voltage for different values of the gate/drain underlap (ΔL_G) for pTFETs.

to the drain region (ΔL_G). All the simulations considered the Kane tunneling model (local model). The variation in gate length results in $\Delta L_G > 0$ when the gate overlaps the drain–channel junction, $\Delta L_G < 0$ represents the underlap between gate and drain and the $\Delta L_G = 0$ situation refers to the self-aligned condition.

Fig. 4 presents the simulated results for the drain current as a function of the gate voltage for different values of ΔL_G and the experimental drain current behavior for a self-aligned pTFET structure at room temperature. The simulation curve for 300 K was fitted with the experimental data using the models and parameters indicated below. Analyzing the drain current for self-aligned TFET, it is possible to see that for gate bias of −0.4 V, there is an inflexion point in the I_{DS} curve. The pTFET off-state drain current ($V_{GS} > -0.25$ V) shape for self-aligned ($\Delta L_G = 0$) device presents the same behavior observed for on-state current condition ($V_{GS} < -0.55$ V) because in both cases the band-to-band tunneling (BTBT) and TAT are active and they are responsible for the drain current behavior. If the $|V_{GS}|$ is increased even more the transport mechanism becomes each time more dependent of BTBT. Fig. 5A represents a pTFET in the on-state, with the tunneling occurring at the source/channel junction, where the electrons tunnel from the valence band (channel) to the conduction band (source region). On the other hand, when the band diagram for off-sate condition ($V_{GS} \geqslant -0.4$ V) is analyzed, it is possible to see in Fig. 5B that for $V_{GS} = -0.4$ V (inflexion point) the distance between the valence and conduction bands does not enable the BTBT mechanism. In a voltage range near to −0.4 V, the predominant phenomenon is SRH. Increasing the gate voltage, the trap-assisted tunneling is activated and when $V_{GS} = 0$ V, both TAT and BTBT are working together. For high values of the gate voltage ($V_{GS} = 1$ V), there is a barrier narrowing at the drain/channel junction. In this situation, electrons tunnel from drain to channel, causing the undesirable ambipolar current.

Fig. 4 shows that by increasing the gate underlap at the drain/channel junction, the ambipolar current strongly decreases [12] and therefore, the off-state current becomes dependent basically on TAT (Trap-Assisted-Tunneling) and SRH (Shockley–Read–Hall) recombination components.

Fig. 6 shows the drain current as a function of gate voltage for ΔL_G of −20 nm (A), −10 nm (B) and 0 nm (C), for four different temperatures (240 K, 300 K, 360 K and 420 K). It can be noticed that with increasing underlap the off-state current tends to decrease due to the reduction of the BTBT influence on off-state region and as a consequence the off-state current, that is more dependent of TAT and SRH, becomes more temperature dependent.

When the most relevant current component is BTBT, there is a small temperature dependence caused by band gap narrowing [13], compared to others components. Eq. (1) expresses this behavior, with a slight current increase as the temperature raises.

$$G_{BTBT} = \frac{(\mathrm{BTBT}\cdot \mathrm{A\_KANE})}{\sqrt{E_g}} F^{\mathrm{BTBT.GAMMA}} \exp\left[-(\mathrm{BTBT}\cdot \mathrm{B\_KANE})\frac{E_g^{\frac{3}{2}}}{F}\right] \quad (1)$$

where $\mathrm{BTBT}\cdot \mathrm{B\_KANE} = 2.3 \times 10^7$ V/(cm eV$^{3/2}$) was used in these simulations, maintaining for the other parameters the default values used in the Atlas simulator [9]. E_g is the bandgap and F is the electric field.

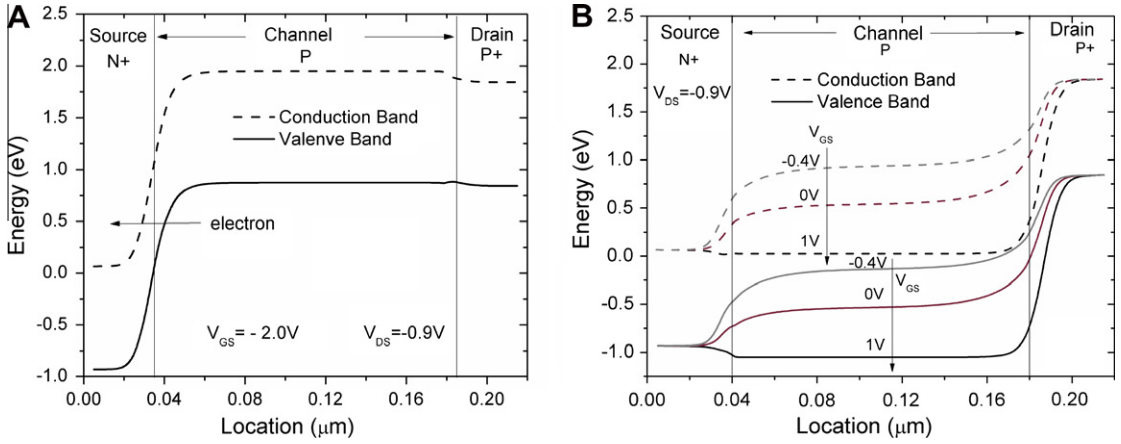

Fig. 5. Bandgap energy from source to drain at on-state (A) and at off-state (B) for a pTFET.

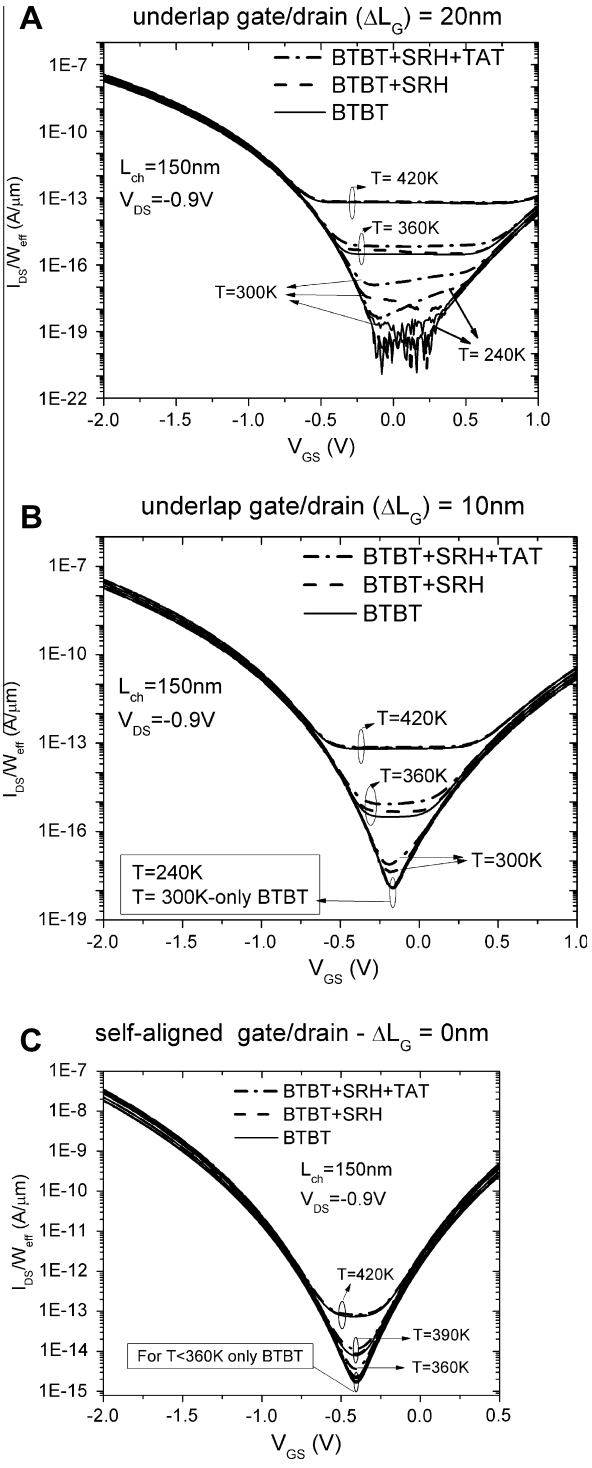

Fig. 6. Simulated drain currents as a function of gate voltage for pTFETs at different temperatures and $\Delta L_G = -20$ nm (A), $\Delta L_G = -10$ nm (B) and $\Delta L_G = 0$ nm (C).

Conversely, when TAT and SRH play the major role, the temperature impact is much more significant. As shown in Eq. (2), the Shockley–Read–Hall model shows an exponential dependence on the temperature [14,11].

$$R_{SRH} = \frac{pn - n_i^2}{\mathrm{TAUP0}\left[n + n_i \exp\left(\frac{\mathrm{ETRAP}}{kT_L}\right)\right] + \mathrm{TAUN0}\left[p + n_i \exp\left(\frac{-\mathrm{ETRAP}}{kT_L}\right)\right]} \quad (2)$$

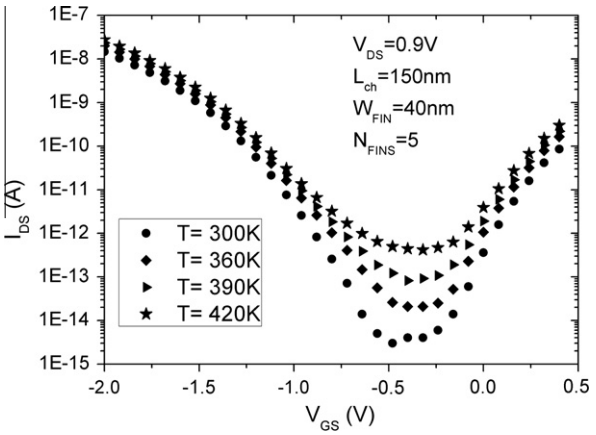

Fig. 7. Experimental drain current as a function of gate voltage for different temperatures and $\Delta L_G = 0$ nm.

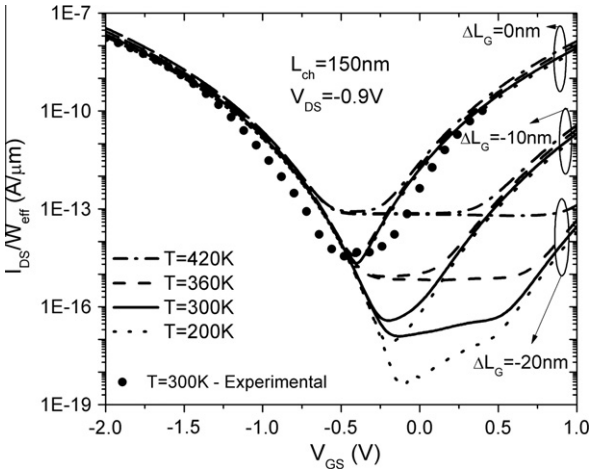

Fig. 8. Drain current as a function of gate voltage for temperatures from 240 K to 420 K and for ΔL_G from 0 to −20 nm.

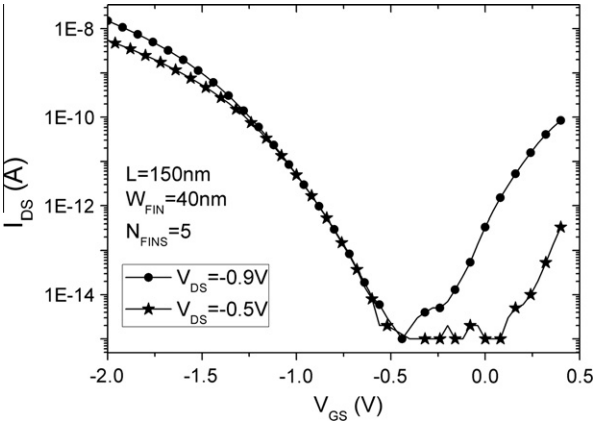

Fig. 9. Experimental drain current as a function of gate voltage for different drain voltages at room temperature.

where TAUP0 = TAUN0 = 10^{-6} s was used in these simulations. T_L is the lattice temperature.

Meanwhile, the TAT current predominates if the electric field at a *pn*-junction increases as a consequence of higher doping levels. This way, carriers can tunnel into the forbidden gap and recombine

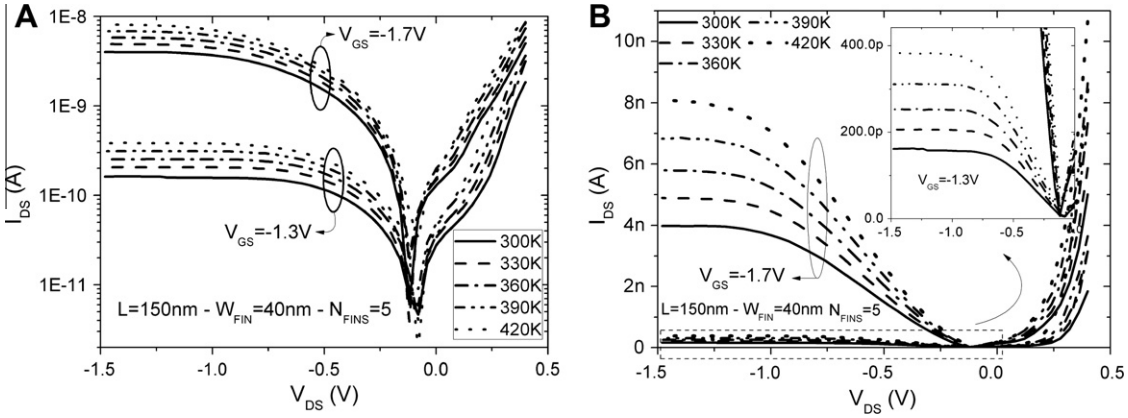

Fig. 10. Experimental drain current as a function of drain voltage for different gate voltages varying the temperature from 300 K up to 420 K.

at traps at high electric fields [15]. The SRH modified equation in order to take TAT into consideration is represented by Eq. (3).

$$R_{SRH} = \frac{pn - n_i^2}{\frac{TAUP0}{1+\Gamma_p^{DIRAC}}\left[n + n_i \exp\left(\frac{ETRAP}{kT_L}\right)\right] + \frac{TAUN0}{1+\Gamma_n^{DIRAC}}\left[p + n_i \exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \quad (3)$$

where Γ_n^{DIRAC} is the electron field enhancement term for Dirac wells and Γ_n^{DIRAC} is the hole field enhancement term for Dirac wells. These enhancement terms depend on both the effective electron tunneling mass and the electric field [15]. In the simulations these terms were modified considering an effective electron tunneling mass equal to $0.3m_0$ (m_0 is the electron mass).

For all the analyzed gate/drain underlap values, the current is basically due to the band-to-band tunneling if $V_{GS} < -0.75$ V, leading to a negligible temperature dependence.

With a 20 nm underlap (Fig. 6A), BTBT decreases for $V_{GS} > -0.75$ V (pTFET off-state condition) and SRH and TAT become dominant and consequently show a higher temperature dependence. By using modified SRH parameters in the model, I_{DS} increases due to the generation/recombination factor. By including also modified TAT parameters, I_{DS} becomes even higher due to the influence of traps. For $T = 420$ K a high leakage current is observed for $V_{GS} > -0.5$ V. This current is not related to the three components studied till now. It is the diffusion component of the thermal reverse leakage current through the drain/channel junction which is very dependent on temperature (proportional to ni^2). While its contribution is negligible for lower temperatures, it becomes very pronounced at high temperatures.

By reducing the underlap to 10 nm (Fig. 6B), the band-to-band tunneling influence on the off-state current becomes more pronounced.

While the BTBT current plays the major role for $V_{GS} < -0.5$ V, for gate voltages ranging from −0.4 V to 0.4 V the behavior becomes similar to the one obtained for a 20 nm underlap. Reducing the temperature, the SRH and TAT influence is decreased and the BTBT behavior becomes the dominant transport mechanism again.

Self-aligned devices (Fig. 6C) are less temperature dependent, since there is a high ambipolar effect (BTBT transport mechanism prevails in all regions).

Fig. 7 presents experimental curves of the drain current as a function of the gate voltage for a pTFET with temperatures ranging from room temperature up to 420 K. It is clear that the experimental results present the same trend as previously explained in the simulation part considering BTBT, SRH and TAT together. When band-to-band tunneling dominates ($V_{GS} < -1$ V or $V_{GS} > 0$ V), there is a slight temperature dependence. For the interval between these conditions, there is an off-current increase due to the SRH and TAT effects.

Fig. 8 puts together the effects of the gate length and the temperature on the drain current. It is possible to conclude that the best behavior was obtained for the highest underlap value, when the ambipolar band-to-band tunneling is minimized. It is clear that lower temperatures also contributed in the same direction. High values of underlap make TAT and SRH the most important current components and, as a consequence, increase the off-current temperature dependence because initial they are operating in a lower off-current regime.

Fig. 9 presents the drain current behavior as a function of the gate voltage for two different drain voltages (−0.5 V and −0.9 V). It is possible to notice that the ambipolar current decreases as the drain voltage is reduced in absolute value, since it decreases the tunneling close to the drain/channel junction. As a consequence, the others off-current components (SRH, TAT) become more significant and therefore the current is more sensible to the temperature influence. On the other hand, the drain voltage influence is negligible for -1.2 V $< V_{GS} < -0.5$ V, when the current is due to tunneling close to the source/channel junction and the carriers diffusion in the channel. For $V_{GS} < -1.2$ V and $V_{DS} = -0.9$ V there is a high longitudinal electric field (V_{DS}) influencing the drain current and the drift current becomes quite significant.

Fig. 10 presents experimental curves of the drain current as a function of the drain voltage for a pTFET with temperatures ranging from 300 K to 420 K. While this device works as a conventional diode for positive V_{DS}, it works as a pTFET for negative drain voltages. In this last condition, there is a drain current plateau in both log (Fig. 10A) and linear (Fig. 10B) graphs, showing a suitable performance for analog applications due to a low output conductance. It is possible to notice a slight drain current increase as the temperature rises. This behavior can be explained by the bandgap narrowing with the temperature increase that results in an exponential increase of the band-to-band tunneling current as shown in Eq. (1). In Fig. 10, it is also possible to observe that there is a slight shift of the minimum drain current (it is not centered in $V_{DS} = 0$ V). This effect occurs because although the measured devices use a high-k material as the gate dielectric and consequently the obtained gate current (I_G) is low ($I_G = 18$ pA for $V_{GS} = -1.3$ V), the tunneling for low drain bias is also very small and both currents I_{DS} and I_G reach the same order of magnitude, which shift the minimum I_{DS} value point for lower V_{DS}.

4. Conclusion

This work focused on the impact of gate/drain underlap and temperature on the off-state current components by numerical

simulation and experimentally. The drain current behavior as a function of drain voltage was also analyzed.

Regarding the underlap influence, it is possible to conclude that higher values of underlap drastically reduce the ambipolar effect, since it decreases tunneling close to the drain/channel junction. As the underlap increases, the BTBT component is reduced and, as a consequence, trap assisted tunneling (TAT) and Shockley–Read–Hall (SRH) recombination become more relevant.

Since BTBT is indirectly affected by the temperature through the bandgap narrowing, while SRH and TAT are exponentially influenced, higher values of underlap make the off-state region more temperature dependent.

Based on experimental curves, it was possible to show that the drain voltage does not affect I_{DS} when the current is due to BTBT and diffusion. However, a higher V_{DS} increases I_{DS} due to a relevant drift influence.

Finally, curves obtained by varying the drain voltage suggested that pTFET devices should present interesting performance for analog applications once that the output conductance is very low.

Acknowledgments

Paula Ghedini Der Agopian and Joao Antonio Martino thank CNPq and FAPESP for the financial support during the execution of this work. Part of the work has been performed within the frame of the CNPq-FWO Brazil-Flanders cooperation agreement.

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