A MULTILEVEL INVERTER FOR DC RETICULATION

By

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for the degree of Master of
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DECLARATION

I, the undersigned, hereby declare that the work contained in this thesis is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

S. A. Molepo
December, 2002

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SUMMARY

This report presents the design and development of a multilevel inverter for DC reticulation. Two main multilevel inverter topologies are introduced and discussed. The research focusses on the flying capacitor multilevel topology, since it became evident that it is more suitable for DC reticulation than the diode clamped multilevel topology.

A bootstrap power supply for the gate drive circuits of a multilevel inverter is developed and its feasibility verified experimentally. A self-starting auxiliary power supply, that aims at addressing the power supply problem of DC to AC and DC to DC converters, is designed and its functionality demonstrated on a flying capacitor multilevel inverter. An FPGA based digital controller for implementing the inverter's control algorithms is also discussed. This controller incorporates a feed-forward output voltage regulation technique.

Experimental results obtained with the four-level flying capacitor multilevel inverter, using the FPGA based digital controller and the self-starting auxiliary power supply, are presented in this report.

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OPSOMMING

In hierdie verslag word die ontwerp en ontwikkelling van 'n multivlak omsetter vir GS retikulasie bespreek. Twee hoof multivlak omsetter topologië word voorgestel en bespreek. Die navorsing fokus op die "vlieënde-kapasitor" multivlak topologië omdat dit duidelik geword het dat dit 'n beter opsie is vir die GS retikulasie as die diode-klamp multivlak topologië.

'n Kragbron vir die hekaandryf bane van die multivlak omsetter is ontwikkel en die werking daarvan is met experimentele toetse bevestig. 'n Self-begin kragbron, wat die probleem van die kragtoevoer aan die GS na WS en die GS na GS omsetters aanspreek, is ontwerp en die funksionaliteit is gedemonstreer met die "vlieënde-kapasitor" multivlak omsetter. 'n Digitale beheerder, gebaseer op 'n FPGA, wat gebruik word om die omsetter se beheer algoritmes te implementeer, word ook bespreek. Hierdie beheerder inkorporeer 'n vorentoe-voer uittree spannings regulasie tegniek.

Eksperimentele resultate wat gekry is met 'n vier-vlak "vlieënde-kapasitor" multivlak omsetter, wat van die FPGA gebaseerde digitale beheerder en die self-begin kragbron gebruik maak, word ook in die verslag bespreek.

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ACKNOWLEDGMENTS

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"Acknowledge Him in all your ways, and He will direct your path." Proverbs 3: 6.

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CONTENTS

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Stellenbosch University http://scholar.sun.ac.za

Stellenbosch University http://scholar.sun.ac.za

Stellenbosch University http://scholar.sun.ac.za

LIST OF FIGURES

Stellenbosch University http://scholar.sun.ac.za

Stellenbosch University http://scholar.sun.ac.za

Stellenbosch University http://scholar.sun.ac.za

Stellenbosch University http://scholar.sun.ac.za

List of Tables

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GLOSSARY

ABBREVIATIONS

A	:	Modulation index.
AC	:	Alternating current.
AD	:	Analog to digital converter.
B	:	magnetic flux density.
D	:	Duty cycle.
DC	:	Direct current.
DCMLI	:	Diode clamped multilevel inverter.
DPWM	:	Digital pulse-width modulation.
EMI	:	Electro-magnetic interference.
FCMLI	:	Flying capacitor multilevel inverter.
FPGA	:	Field programmable gate array.
IC	:	Integrated circuit.
IGBT	:	Insulated gate bipolar transistor.
ISOP	:	Input-series-output-parallel.
MOSFET	:	Metal oxide semiconductor field effect transistor.
MMF	:	Magneto-motive force.
N	:	Number of turns.
p	:	number of commutation cells in a multilevel inverter.
PCB	:	Printed circuit board.
PWM	:	Pulse-width modulation.
PFC	:	Power factor correction.
RMS	:	Root mean square.
r	:	Radius of wire.
SMPS	:	Switch mode power supply.
USD	:	United States Dollar.

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USE	:	Universal semiconductor electrification.
ZAR	:	South African Rands.

SYMBOLS

A_{core}	:	Effective area of core.
A_{Cu}	:	Area of copper wire.
A_w	:	Window area.
A_{sec}	:	Cross-sectional area of the secondary conductor.
A_{prim}	:	Cross-sectional area of the primary conductor.
C_d	:	DC bus capacitor.
C_k	:	Flying capacitor of cell k.
C_f	:	Output filter capacitor.
E	:	Energy.
f_0	:	Fundamental frequency.
f_s	:	Switching frequency.
i_l	:	Inductor current.
ic_k	:	Current flowing in capacitor of cell k.
I_0	:	Output current.
$\hat{I}$	:	Maximum current flowing in the inductor.
I_p	:	Primary current.
I_s	:	Secondary current.
I_g	:	Gate current.
Δi_{max}	:	Maximum output ripple current.
K_{Cu}	:	Copper fill factor.
L_f	:	Output filter inductor.

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N_1	:	Primary turns.
N_2	:	Secondary turns.
P_{gate}	:	Power dissipated at the gate.
P_{cond}	:	Conduction power loss.
$P_{switching}$	:	Switching power loss.
P_{rr}	:	Reverse recovery losses in a diode.
Q	:	Charge.
$R_{ds(on)}$	:	On-state resistance of a MOSFET or a CoolMOS.
R_{thjcI}	:	Junction to case thermal resistance of a switch.
R_{thjcD}	:	Junction to case thermal resistance od a diode.
R_{thcs}	:	Case to sink thermal resistance of a heat sink mounting pad.
R_{thsa}	:	Sink to ambient thermal resistance.
R_g	:	Gate resistance.
S	:	Apparent power.
T_j	:	Junction temperature.
T_{jc}	:	Junction to case temperature.
T_{case}	:	Case temperature.
T_s	:	Heat sink temperature.
T_a	:	Ambient temperature.
T_s	:	Switching period.
T_0	:	Fundamental period.
t_{on}	:	Switching device's turn on time.
t_{off}	:	Switching device's turn off time.
V_d	:	DC-bus voltage.
V_{tri}	:	Carrier waveform signal.
$V_{control}$	:	Reference waveform signal.
V_0	:	Output voltage.

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V_{cell}	:	Cell voltage.
V_{gate}	:	Gate voltage.
V_p	:	Primary voltage.
V_s	:	Secondary voltage.
v_L	:	Voltage across an inductor.
ΔV_{ck}	:	Ripple voltage in the flying capacitors.
ϕ	:	Phase shift between adjacent commutation cells.
$\Re_g$	:	Reluctance of an air gap.
$\Re_c$	:	Reluctance of core.
μ_0	:	Permeability of free space.
ω	:	Angular frequency.
φ	:	Magnetic flux.
λ	:	Eigenvalue.
τ	:	Time constant.

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CHAPTER 1

INTRODUCTION

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1.1 INTRODUCTION

Figure 1.1: *An example of illegal connections to the electricity grid.*

This chapter introduces the non technical power loss problem that is to be addressed by this research work. A solution as to how to address this problem is also proposed in this chapter. The research work's focus and structure are also outlined.

1.2 NON-TECHNICAL POWER LOSS

A cost-impact problem currently experienced by developing countries is that of non-technical power loss. This is theft of electricity done by means of illegal connections to the electricity grid. Cases of illegal power connection include by-passing of metering units, tapping into neighbouring premises and tapping directly on to the overhead distribution lines. Figure 1.1 shows an example of illegal connections to the electricity grid. These illegal connections not only lead to a loss of revenue for the utility, but also pose a very serious safety hazard to the perpetrators, as well as innocent people living in the

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affected buildings. This problem is mainly prevalent in remote areas such as rural settings and townships and it is done by tapping the domestically rated 230 V $\pm 10\%$, 50 Hz overhead ac reticulation networks and by bypassing of metering units [1]. The question of theft is not unique to South Africa, it is of concern in various parts of the world [2]. In Argentina the level of electricity fraud is estimated at between 16 and 20% [3], whereas in South Africa unofficial figures of as high as 70% have been reported in some of the affected areas [2].

1.3 PROPOSED SOLUTION

A proposed solution is to distribute electricity at a voltage and frequency that cannot be easily used. This means applying direct current (DC) reticulation at high voltage, i.e. 750 V to 1000 V level, and installing an inverting unit in each house to invert the high DC voltage to 230 V, 50 Hz that can be used by the consumer. Figure 1.2 shows the proposed DC reticulation system. The system will use the existing standard ABC conductor material currently used for AC reticulation [2].

Using DC instead of AC eliminates reactive voltage drops that can be encountered in some rural settings. The idea of a DC reticulation system was perhaps triggered by the research and development phase of the USE (Universal Semiconductor Electrification) devices at the University of Stellenbosch. During the development phase of these USE devices, Mostert et al [4] realized that the DC-link could be stretched out to form a DC distribution system.

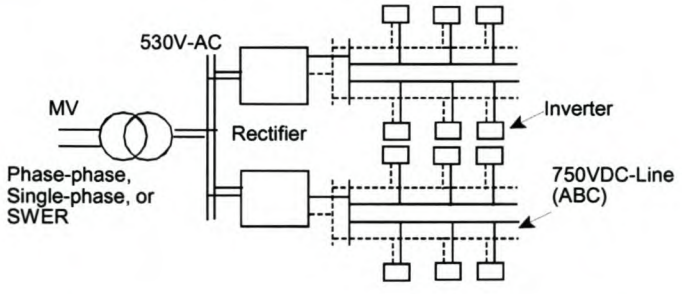

Figure 1.2: *The proposed DC reticulation system.*

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1.4 RESEARCH FOCUS

This research focuses primarily on the design and development of the power electronic device (InDispenser) for the proposed DC reticulation. This power electronic device will be fitted in each and every household and will be used to invert the high DC voltage to 230 V, 50 Hz AC voltage. The power electronic device should therefore be:

- Low cost.
- Acoustical noise-free.
- Efficient as possible to reduce cooling requirements under high ambient temperature.
- Small size.
- Power rating: 3.5 kVA
- Input: 750 - 1000 V DC
- Output: 230 V AC $\pm 10\%$, 50 Hz (Single phase)

This research investigates the possible use of a multilevel inverter for a low cost, noise-free and efficient design of the power electronic device. The decision to investigate the use of multilevel inverters was taken after constructing a standard half-bridge IGBT inverter and is based on the following observations and considerations:

- The output filter contributed significantly to the cost of the inverter. The ratio of the high DC bus voltage to the relatively low output current results in a large filter inductor.
- The use of multilevel inverters reduces the size of the filter inductor by a factor of p^2, with p the number of cells.
- The use of multilevel inverters opens possibilities of using new state-of-the-art 600 V devices, for instance, CoolMOS technology or fast IGBT technology semiconductors.
- These new devices make it possible to reduce system cost by designing an inverter with fewer number of levels.

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Figure 1.3: *A single phase prepaid metering unit.*

- Due to the added components (i.e. flying capacitors and switching devices) in flying capacitor multilevel inverters, the feasibility of these inverters for a low cost design depends solely on the success of developing a low cost gate drive circuit for multilevel inverters. Switching at high switching frequency results in small values of the flying capacitors.

The ultimate aim is to integrate the final unit with a prepaid metering system. An example of a card operated prepaid metering system is shown in Figure 1.3. A prepaid metering system enables the electricity users to pay for their electricity in advance and also provides energy consumption information to allow the customers to manage their electricity usage. With a prepaid metering system the customer purchases electrical power on a smart card. Once the card is inserted into the prepaid metering unit, the power is turned "on" and the amount of power on the card is displayed on the meter. Eventually, after all the power in the card is all used up and the meter reaches zero credit level, the prepaid metering unit automatically disconnects the load from the supply.

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1.5 RESEARCH ISSUES

Though the advantages of flying capacitor multilevel inverters make them to enjoy a great deal of interest in recent years, they (advantages) come at the expense of added components, for instance, flying capacitors and semiconductors, and complex capacitor pre-charging mechanisms.

Given the large number of switching components, it is important to make the gate drive circuits of these inverters as inexpensive as possible. The need for an isolated power supply for the gate drive circuits, is one other factor that will escalate the system cost. The success of designing a low cost inverter depends greatly on the success of addressing this isolated power supply issue.

Another issue that needs to be addressed is that of generating regulated dc power supplies from a high DC bus voltage. This is because the flying capacitor multilevel inverter will only be exposed to a high DC voltage of between 750 V to 1000 V. Therefore the success of this research work depends also on the success of developing a self-starting switch mode power supply to provide regulated dc power supplies for the electronic circuits of the inverter.

1.6 STRUCTURE OF REPORT

The current Chapter introduced the problem statement and key issues to be addressed to make this research a success. The introductory work done by Mostert et al [4] provides the base and/or foundation for this research. Challenges posed by the proposed method are briefly outlined.

Chapter 2 presents background work on the chosen topology for the power electronic device (InDispenser) to be used in the proposed DC reticulation system and cites a few but relevant literature into the design of the system's components. Also this chapter discusses at length and compare the two main multilevel topologies.

Chapter 3 presents the system overview of the power dispenser. Each main part's functionality, e.g. controller, auxiliary power supply, etc., is briefly discussed.

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The design of the inverter's gate drive circuits, reactive components and heat sink are presented in Chapter 4. The gate drive circuit incorporates the new power supply for multilevel inverters, therefore accomplishing a cost-effective design to address one of the challenges in Section 1.4.

Chapter 5 presents a field programmable gate array based (FPGA-based) pulse-width modulation (PWM) controller and also briefly discusses system protection and voltage regulation issues.

Chapter 6 discusses the design and development of a self-starting auxiliary power supply to address one of the challenges outlined in Section 1.4. The self-starting auxiliary power supply is based on the input-series-output-parallel (ISOP) inverter topology.

Cost and device analysis are discussed in Chapter 7. This will lead to a proper device and inverter selection.

Simulation study and results are presented in Chapter 8. Experimental set-ups and results for the various sections, i.e developed bootstrap power supply, power stage, auxiliary power supply, etc., are presented in Chapter 9.

Chapter 10 concludes this report with a brief summary and highlight the significant contributions made by this research work.

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CHAPTER 2

LITERATURE REVIEW

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2.1 INTRODUCTION

The aim of this research, as mentioned in Chapter 1, is the design and development of a multilevel inverter and its auxiliary power supply for DC reticulation. In recent literature, numerous multilevel inverter topologies have been introduced and studied in detail. These topologies are:

- Flying capacitor multilevel inverter (FCMLI).
- Diode clamped multilevel inverter (DCMLI).
- Cascaded multilevel inverter

Of these three multilevel topologies, only the FCMLI and the DCMLI are suitable for application in the proposed DC reticulation.
This chapter focuses on:

- The comparison of the FCMLI and the DCMLI topologies to determine which is more suitable for the proposed application.
- The investigation of switch mode power supplies (SMPS) for the design of an auxiliary power supply.
- Background work on the new state-of-the-art energy saving switching devices mentioned in Chapter 1. Pulse width modulation (PWM) strategies are also discussed.

2.2 MULTILEVEL INVERTER TOPOLOGIES

Multilevel inverters have in recent years received a great deal of interest for high power applications [5]. These inverters are suitable for high voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating. The harmonic content of the output voltage waveform for multilevel inverters decreases significantly as the number of inverter levels increases [7]. But all these advantages of multilevel inverters come at the expense of added components, for instance the flying capacitors or clamping diodes [6], complicated control algorithms and possible capacitor voltage balancing problems.The early interest in multilevel power conversion technology was perhaps triggered by Nabae et al [8] who introduced a neutral point clamped topology. The resultant

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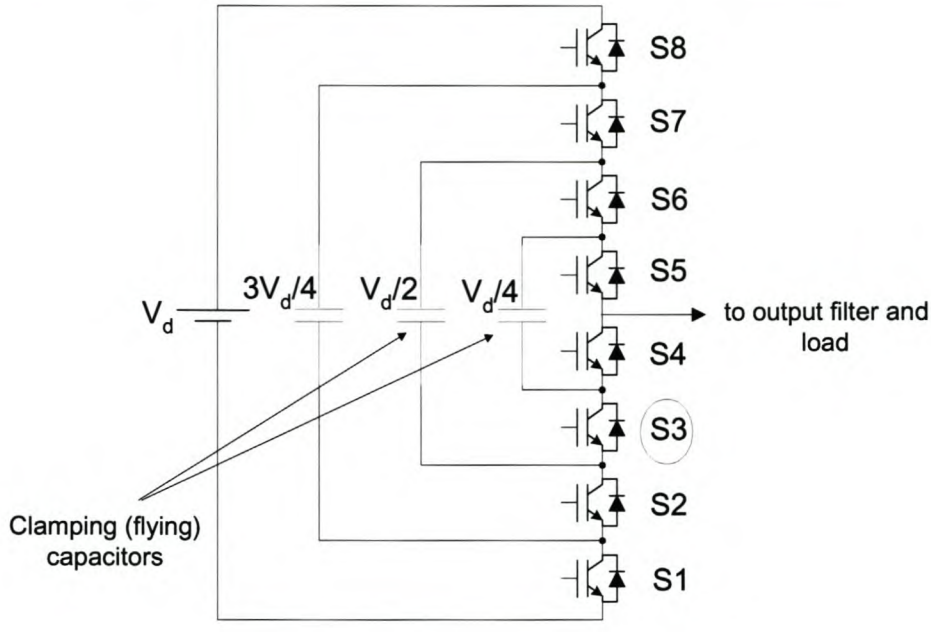

Figure 2.1: *A five-level single phase FCMLI.*

three-level waveform had considerably better spectral performance compared to that of the conventional voltage source inverter. The improvement in the spectral structure of output waveforms in using multiple levels was reiterated by Bhagwat et al [9]. Subsequently, the original neutral point clamped topology was extended to higher number of levels using the similar principle of clamping the intermittent levels with diodes [10]. In addition to improving the waveform quality, these multilevel inverters substantially reduced voltage stress on the devices. Such multilevel inverters are generally known as diode clamped inverters. However in this type of inverter, the required voltage blocking capability of the clamping diodes varies with the levels. This may result in the requirement of multiple clamping diodes at higher levels. So an alternative multilevel structure, where the voltage across an open switch is constrained by clamping capacitors instead of clamping diodes, was proposed by Meynard and Foch [7]. These inverters are commonly known as flying capacitor multilevel inverters.

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2.2.1 Flying capacitor multilevel inverter

The flying capacitor multilevel inverter (FCMLI) uses a ladder structure of DC side capacitors where the voltage on each capacitor differs from that of the next capacitor. A five-level flying capacitor multilevel inverter is shown in Figure 2.1. The size of the voltage increment between two adjacent capacitors defines the size of the voltage steps in the output voltage waveforms. Separate capacitors are used for each phase arm of a three phase inverter [6]. The voltage sharing, voltage clamping, voltage synthesis and capacitor pre-charging capabilities of this FCMLI topology are discussed below:

- **Voltage sharing**

  This topology solves the problem of static and dynamic voltage sharing of the voltage across the blocking switches. Clamping circuits (diodes and capacitors) ensure voltage sharing between the switches. For a FCMLI, the voltage stresses on the blocking switches are the same for all the switching cells and this voltage stress is given by the voltage difference of adjacent capacitors.

- **Voltage clamping**

  The maximum forward voltage of the main devices in the FCMLI is equal to the voltage difference between the capacitor connected to its cathode and the capacitor connected to its anode. Consider the highlighted switch in Figure 2.1. The forward voltage of this device can be increased until the antiparallel diode of the highlighted switch becomes forward biased. At this point, the capacitors provide a clamping voltage equal to $V_d/2 - V_d/4 = V_d/4$. All the switches in the circuit are clamped in a similar fashion. The circuit uses no additional clamping diodes [6].

- **Voltage synthesis**

  The output voltage synthesis of a FCMLI is performed by turning on the switches so that adding or subtracting of the capacitor voltages can take place. For the five-level inverter in Figure 2.1, four capacitors are used in the synthesis of each phase voltage. The capacitors have voltages of V_d, $(3/4)V_d$, $(1/2)V_d$ and $(1/4)V_d$. The switch operations are constrained so that the capacitors are never shorted and such that current continuity to the main DC bus capacitor is maintained. As an example of the voltage synthesis, a phase voltage level of $(1/2)V_d$ can be synthesized in six different ways. The capacitor combinations which produce this phase voltage level

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are listed below:

$$V_d - \frac{1}{2}V_d \tag{2.1}$$

$$V_d - \frac{3}{4}V_d + \frac{1}{4}V_d \tag{2.2}$$

$$V_d - \frac{3}{4}V_d + \frac{1}{2}V_d - \frac{1}{4}V_d \tag{2.3}$$

$$\frac{3}{4}V_d - \frac{1}{2}V_d + \frac{1}{4}V_d \tag{2.4}$$

$$\frac{3}{4}V_d - \frac{1}{4}V_d \tag{2.5}$$

$$\frac{1}{2}V_d \tag{2.6}$$

The availability of voltage redundancies in the FCMLI provides special opportunities for controlling the voltage on the individual inverter capacitors. This flexibility makes it easier to manipulate the capacitor voltages and keep them at their proper values.

2.2.2 Diode clamped multilevel inverter

The DCMLI uses a string of capacitors to divide up the DC bus voltage into a set of equal voltage levels. Each phase arm consists of a number of switching devices in series which are connected via diodes to the tap points along the DC bus capacitor. The forward voltage across each main device is clamped by the connection of diodes between the main devices and tap points along the string of DC bus capacitors. The tap points provide clamping voltage levels [6]. The voltage sharing, voltage clamping, voltage synthesis and capacitor pre-charging capabilities of this DCMLI topology are discussed below:

- **Voltage sharing**

  Only the outer switches of a DCMLI are effectively protected by the clamping diodes. Among the devices in the DCMLI, the clamping diodes have the highest stress. The fact that the voltage stresses on some of the switches are not clamped directly by the capacitors or diodes is of great concern [6].

- **Voltage clamping**

  Figure 2.2 of the DCMLI shows voltage clamping components effecting the maximum forward voltage on switch S3. The maximum forward voltage of the main

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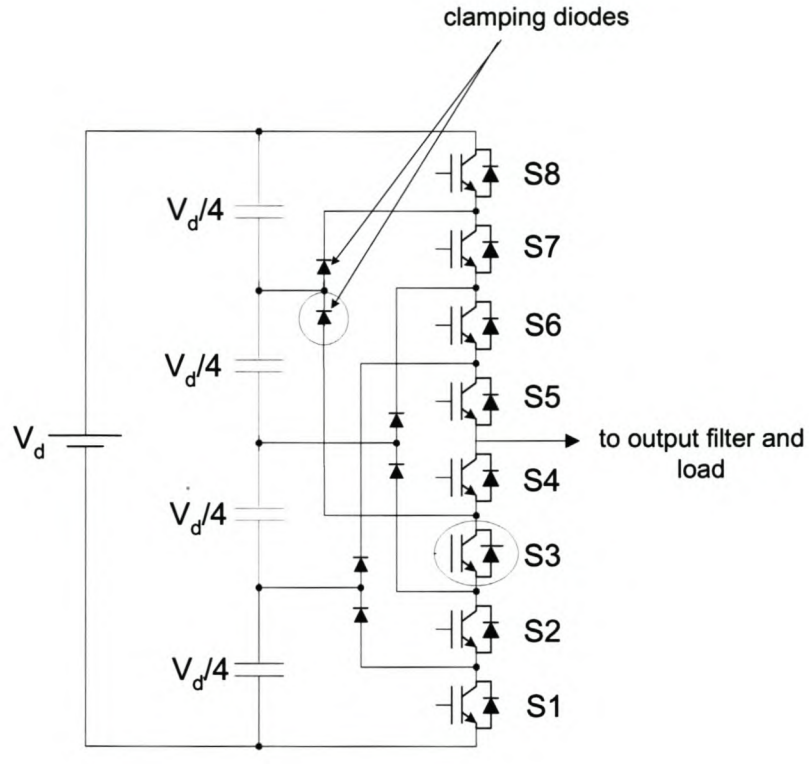

Figure 2.2: *A five-level DCMLI.*

devices is limited by a clamping diode on one end of the device and on the other end by the off-state voltages of the adjacent switches. Switch S3's anode voltage is limited to $(3/4)V_d$ by the highlighted clamping diode. The clamping diode is connected to a voltage level of $(3/4)V_d$ at a tap point along the DC capacitor string. The cathode voltage of switch S3 is given by the off-state voltage of switches S2 and S1. If the off-state voltages of S1 and S2 can be controlled, limitation of the off-state voltage stress on S3 can be assured [6].

If the off-state voltage across S1 and S2 is zero, S3 would see a forward voltage of $(3/4)V_d$. However, in normal operation, the off-state voltages are controllable and can be limited to $(1/4)V_d$.

- **Voltage synthesis**

  The DCMLI's output voltage synthesis is relatively straight forward. For the five-

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level inverter in Figure 2.2, a set of four adjacent main devices in each phase arm is on at any given time. For the outer voltage levels, the four "on" devices clamp the phase output to the top and bottom of the DC bus. For the inner voltage levels, the group of 'on' devices acts as a short-circuit connecting two of the clamping diodes back-to-back. The outer end of these back-to-back clamping diodes is connected to one of the voltage taps along the DC bus. The circuit then can be thought of as a type of multiplexer, attaching the output to one of the five available voltage levels. The DCMLI does not have phase voltage redundancies due to the different constraints on switch operation imposed by the structure [6].

The lack of redundancy of inner voltage levels in this topology results in complex control of capacitor voltages. In this type of inverter, the required voltage blocking capabilities of the clamping diodes vary with the number of levels. This may result in the requirement of multiple diodes at higher levels.

2.3 PULSE WIDTH MODULATION

In dc to dc inverters, the average dc output voltage must be controlled to equal a desired level, though the input voltage and the output load current may fluctuate. Switch-mode dc to dc inverters utilize one or more switches to transform dc from one level to another. In a dc to dc inverter with a given input voltage, the average output voltage is controlled by controlling the switch's "on" and off duration times (t_{on} and t_{off}). One of the methods for controlling the output voltage employs switching at a constant frequency (hence,

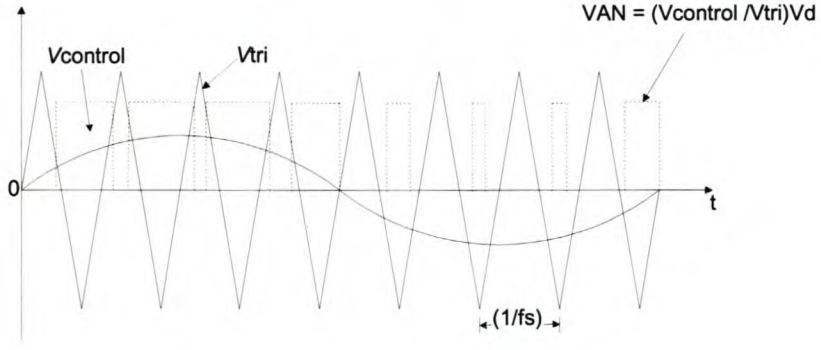

Figure 2.3: *Pulse-width modulation.*

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a constant switching time period $T_s = t_{on} + t_{off}$) and adjusting the "on" duration of the switch to control the average output voltage. In this method, called pulse-width modulation (PWM), the switch duty ratio D, which is defined as the ratio of the "on" duration to the switching time period, is varied [32]. In order to produce a sinusoidal output voltage waveform at a desired frequency, a sinusoidal control signal at the desired frequency is compared with a triangular waveform, as shown in Figure 2.3. The frequency of the triangular waveform establishes the inverter's switching frequency and is generally kept constant along with its amplitude [32].

The PWM method can remove unwanted frequency components to a higher frequency region, i.e. the sidebands of a carrier frequency. Thus the output waveform of a PWM inverter is generally improved by using a high ratio between the carrier frequency and the output fundamental frequency. Taniguchi et al [14] proposed a new sinusoidal PWM inverter for the use of power metal-oxide semiconductor field effect transistors (MOSFET) which has a high carrier-to-fundamental output frequency ratio.

2.3.1 E-prom based DPWM

Generating PWM control signals with the help of electronic hardware is rather complex. The cost of hardware implementation in the microcomputer approach is also considerable. The E-prom based PWM circuit proposed by Simard et al [16], solves the large memory requirement problem outlined in [17] and combines the advantages of fast response of the analogue technique and simplicity of the microcomputer digital technique. The circuit also has better dynamic response than a DSP-1 based modulator proposed in the literature [18].

The circuit is comprised mainly of two E-proms, a counter and an analog-to-digital (AD) converter. The output voltage is digitized by the AD converter and results in an 8-bit word having 256 possible states. The first E-prom is divided into 256 look-up tables, which contain the values of the sine wave for each value of the AD converter. The second E-prom is used to store different PWM schemes which can be selected as the output voltage varies.

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2.3.2 FPGA based DPWM

A circuit of an FPGA based PWM is comprised of an FPGA, a counter and an AD converter. Identical but phase-shifted carrier waveforms are generated inside the FPGA with the aid of an 8-bit counter. For the FCMLI the number of these carrier waveforms depends on the number of commutation cells (p) to be controlled and are phase-shifted by $2\pi/p$.

Several reference sine waveforms of different amplitudes are also internally generated and stored in the FPGA to be compared with the phase-shifted carrier waveforms to generate interleaved PWM signals. A feed-forward voltage regulation technique is employed to regulate the output voltage by using an AD to digitize the input voltage and automatically select between the several reference waveforms whenever the input voltage is varied.

2.4 DESIGNING OF REACTIVE COMPONENTS

In high voltage applications, where DC to AC or AC to DC conversion is required, an FCMLI is particularly suitable since it guarantees equal voltage sharing of series connected switches (through the flying capacitors) and improved output waveform quality. Figure 2.4 shows the general structure of an FCMLI. The switches are arranged in pairs called commutation cells. The switches of a commutation cell should be in a complementary state. FCMLI's are composed of p-commutation cells connected with a set of $(p-1)$ flying capacitors. A modulation strategy of an inverter affects the voltages of the DC capacitors as well as the current flowing through them. Therefore a modulation strategy determines the current ratings of the DC capacitors and the required capacitance to suppress the ripple voltage [6]. An interleaved pulse width modulation (PWM) switching scheme is suitable for flying capacitor multilevel inverters. This modulation strategy is described in detail in Section (2.4.1).

2.4.1 Interleaved PWM switching

This method is suitable for flying capacitor multilevel inverters because the control signals of the different cells can be interleaved to optimize the output voltage waveform [11]. Figure 2.5 shows an interleaved switching technique for a five-level FCMLI. The

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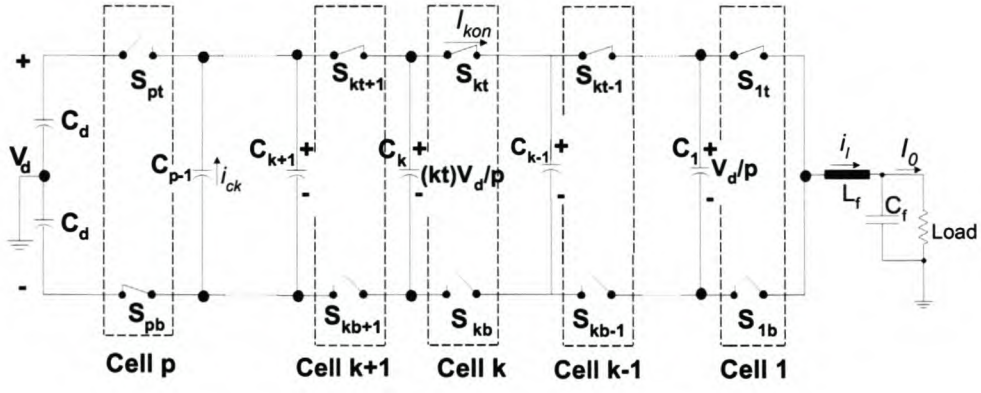

Figure 2.4: *Generalized FCMLI.*

carrier signals V_{tri1}, V_{tri2}, V_{tri3} and V_{tri4} for the four commutation cells are phase-shifted by $2\pi/p$ where p is the number of commutation cells. Each cell is controlled by its own carrier signal, e.g. V_{tri1}, which is compared with a reference signal ($V_{control}$) at a fundamental frequency. Interleaved PWM switching results in an apparent switching frequency equal to p times the switching frequency of a single cell and an output ripple voltage of amplitude V_d/p. This high apparent switching frequency reduces the size of the output filter inductor by a factor of p^2 [11] as compared to a conventional half-bridge inverter and results in small values of the flying capacitors [15].

Digital controllers for pulse width modulation inverters enjoy growing popularity due to their low power, fast response, ease of integration with other digital systems and ability to implement sophisticated control schemes. These digital pulse width (DPWM) controllers are particularly suitable for interleaved switching applications because digital logic makes the generation of identical but delayed control signals simple.

2.4.2 Design of the flying capacitors

The design method of the reactive components of the FCMLI was proposed by Hamma et al [12]. To design the capacitor C_k, it is necessary to determine the characteristics of both the ripple voltage and the root mean square (RMS) current flowing in this capacitor. In this design the ripple current in the smoothing inductor is neglected. The current flowing in the smoothing inductor is assumed to be constant ($i_l = I_0$ and $\Delta i_l = 0$), but

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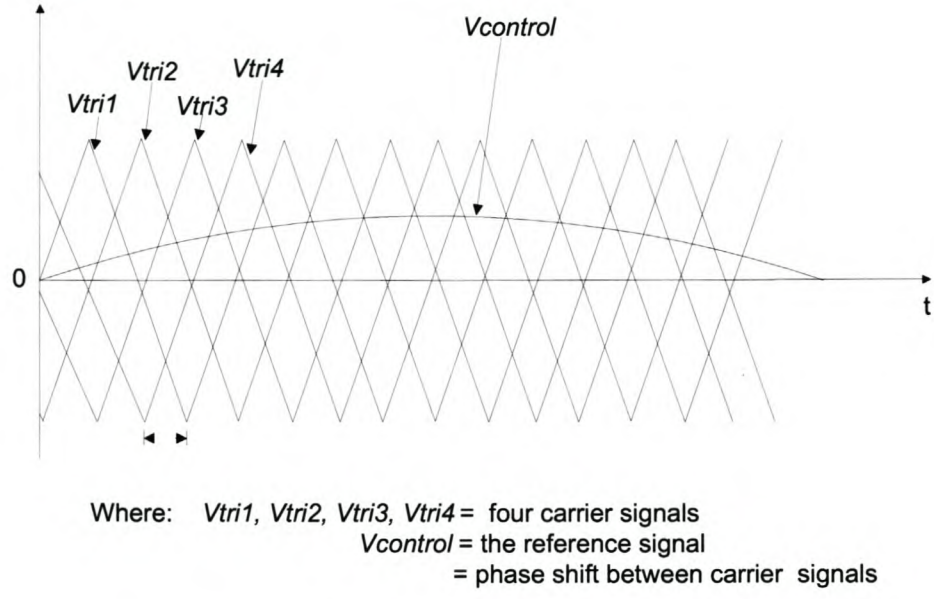

Figure 2.5: *Interleaved PWM switching.*

in practical situations this varies with time. I_0 represents the average value of the current in the inductor, i_l [12].

It is worth noting that the states of the other elementary cells have no influence on the current and voltage applied to the switches of a given cell Figure 2.4. The shape of the current i_{ck} depends only on the states of the two switches, S_{kt+1} and S_{kt}. The instantaneous current (i_{ck}) in the capacitor C_k, can only take three values [12]:

- $ic_k = I_0$, when S_{kt+1} is on and S_{kt} is off.
- $ic_k = 0$, when S_{kt+1} and S_{kt} are in the same state.
- $ic_k = -I_0$, when S_{kt+1} is off and S_{kt} is on.

According to the value of the duty cycle D and the phase difference between the triangular carrier signals (ϕ), three different operating modes can be distinguished. The following analysis is for a DC to DC inverter shown in Figure 2.6 and is valid whatever the number of cells ($p \neq 1$):

1. When $0 \leq D \leq T_s\phi/2\pi$, the charge and discharge time of the current (I_{ck}) in the

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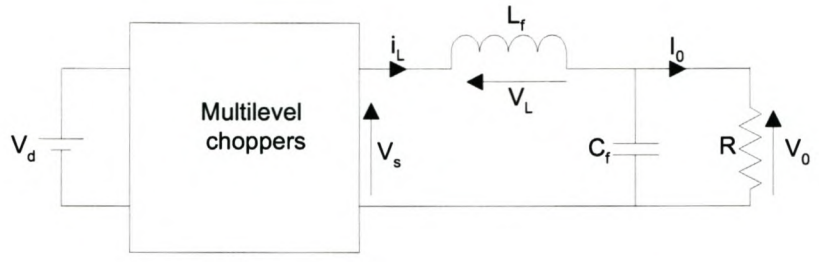

Figure 2.6: *Multilevel chopper topology (taken from [12]).*

capacitor, C_k are equal to DT_s . The expression of the RMS current is given by [12]:

$$Ick_{rms} = I_0.\sqrt{2.D} \tag{2.7}$$

Normalizing this expression with respect to I_0 gives

$$\frac{Ick_{rms}}{I_0} = \sqrt{2.D} \tag{2.8}$$

Where Ick_{rms}, I_0 and D are the RMS current flowing in the capacitor, the load current and the duty cycle respectively.

The normalized voltage ripple is given by:

$$\frac{C_k \Delta V_{ck}}{T_s I_0} = D \tag{2.9}$$

Where C_k is the flying capacitor of cell k, T_s is the switching period and ΔV_{ck} is the ripple voltage in the flying capacitor.

2. For $T_s\phi/2\pi \leq D \leq 1 - T_s\phi/2\pi$, the charge or discharge time is given by [12]:

$$\Delta t = \frac{T_s}{2\pi}\phi \tag{2.10}$$

thus,

$$\frac{Ick_{rms}}{I_0} = \sqrt{\frac{\phi}{\pi}} \tag{2.11}$$

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where ϕ is expressed in radians.
The normalized voltage ripple is specified by:

$$\frac{C_k \Delta V_{ck}}{T_s I_0} = \frac{\phi}{2\pi} \tag{2.12}$$

3. When $1 - T_s\phi/2\pi \leq D \leq 1$, in this case, the normalized RMS current and ripple voltage are obtained by the following relationships [12]:

$$\frac{Ick_{rms}}{I_0} = \sqrt{2(1-D)} \tag{2.13}$$

and

$$\frac{C_k \Delta V_{ck}}{T_s I_0} = (1-D) \tag{2.14}$$

since $\Delta t = (1-D)T_s$

A plot of the characteristics of Eq. 2.8 and Eq. 2.14, i.e. $I_{ck(rms)}/I_0$ and $C_k \Delta V_{ck}/T_s I_0$ versus duty cycle with phase-shift (ϕ) as a parameter, showed that these characteristics are symmetrical with respect to the $D = 1/2$ axis [12].

From Eq. 2.12, the value of the capacitor C_k can be determined. It should be noted that the capacitor C_k should be able to withstand the cell voltage equal to kV_d/p. The flying capacitors have the same value (capacitance), but different voltage ratings. Knowing the values of the switching frequency f, maximum ripple voltage $\Delta V_{ck(max)}$ (worst case), the load current I_0 and for a given value of the phase-shift, the size of the capacitor has to satisfy the following constraint derived from Eq. 2.12:

$$C_k \geq \frac{\phi . I_0}{2\pi f_s \Delta V_{ck(max)}} \tag{2.15}$$

2.4.3 Design of the smoothing inductor, L_f

The topology of the multilevel chopper is shown in Figure 2.6. The capacitor has to divert the ac component of the current so that only the dc current would flow in the load. For this design the voltage across the capacitor C_f is assumed constant $(Vc_f) = DV_d$, i.e. the ripple voltage $\Delta Vc_f = 0$. The smoothing inductor is designed for a given value of the ripple current and this can be determined by a computer program. When the number

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of cells increases the ripple current decreases [12].

Knowing that for an elementary chopper ($p = 1$), the maximum ripple current is given by:

$$(\Delta i_\ell)_{max} = \frac{V_d}{4 f_s L_f} \tag{2.16}$$

On the other hand it is well known that if the control signals are phase-shifted by $\phi = 2\pi/p$, the frequency and the voltage ripple of the output voltage are equal to (pf) and V_d/p, respectively. Therefore the expression of the maximum ripple current in the case of a multilevel chopper is deduced to be:

$$(\Delta i_\ell)_{max} = \frac{V_d}{4 f_s p^2 L_f} \tag{2.17}$$

This relation means that the maximum current ripple is inversely proportional to the square of the number of cells.

2.4.4 Design of the capacitor, C_f

For this design Hamma et al [12] assumed that the total ac component of ripple current flowing in L_f will flow in C_f, Figure 2.6. The voltage in the capacitor is given by the following relationship:

$$Vc_f(t) = \frac{1}{C_f} \int ic_f(t) dt \tag{2.18}$$

with $ic_f(t) = i_\ell(t) - I_0$

This relation allows the determination of the value of Vc_f for the switching instants. It can be shown that the peak-to-peak value of the voltage across the capacitor C_f when the phase-shift $\phi = 2\pi/p$ can be obtained by:

$$\Delta Vc_{f(max)} = \frac{\Delta i_{\ell(max)}}{8 p f_s C_f} \tag{2.19}$$

Substituting for the expression of the $(i_{\ell(max)})$ into Eq. 2.19 yields:

$$\Delta Vc_{f(max)} = \frac{V_d}{32 p^3 f_s^2 L_f C_f} \tag{2.20}$$

This relation means that the maximum peak-to-peak ripple voltage is inversely proportional to the cube of the number of cells.

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2.5 SWITCH MODE POWER SUPPLIES

This section investigates the use of SMPS for the design of an auxiliary power supply. This auxiliary power supply will be designed for a DC bus voltage of between 750 and 1000 V.

2.5.1 Overview of switching power supplies

Regulated dc power supplies are required for most analog and digital electronic systems. Most power supplies are designed to meet some or all of the following requirements [32]:

- Regulated output: The output voltage must be held constant within a specified tolerance for changes within a specified range of the input voltage and the output loading.
- Isolation: The output may be required to be electrically isolated from the input.
- Multiple outputs: There may be multiple outputs that may differ in their voltage and current ratings. Such outputs may be isolated from each other.

In addition to these requirements, common goals are to reduce power supply size and weight and improve their efficiency. Advancement in the semiconductor technology led to switching power supplies gaining superiority over traditional linear power supplies because of their smaller size and higher efficiency as compared to the linear power supplies [32].

In switching power supplies, the transformation of dc voltage from one level to another is accomplished by using dc to dc inverter circuits. These circuits employ solid-state devices (IGBT, MOSFETs, etc.), which operate as controllable switches. Since the power devices are not required to operate in their active region, this mode of operation results in a lower power dissipation. Increased switching speeds, higher voltage and current ratings, and the relatively lower cost of these devices are the factors that contributed to the emergence of switching power supplies.

Two major advantages of switching power supplies over linear power supplies are now apparent, these being [32]:

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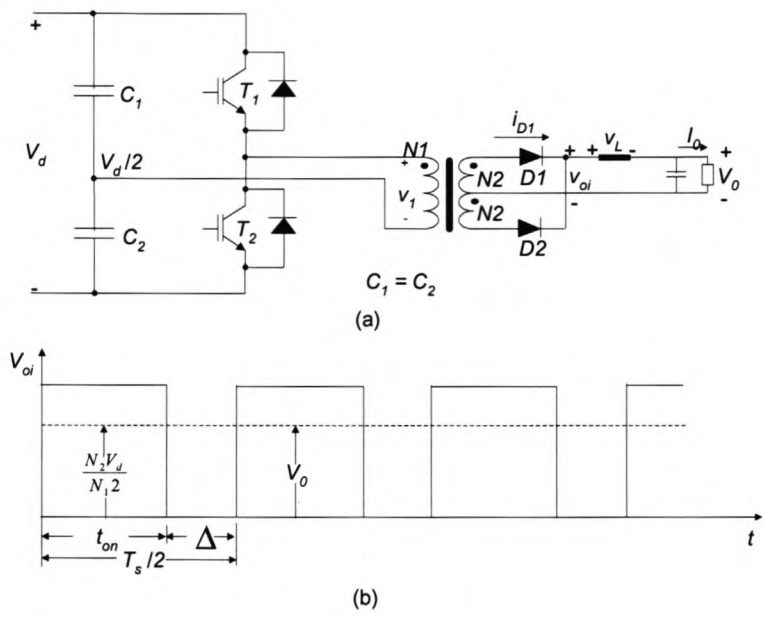

Figure 2.7: *Half-bridge dc - dc converter (taken from [32]).*

- The switching elements operate as a switch: either completely off or completely "on". By avoiding their operation in their active region, a significant reduction in power loss can be achieved. A transistor operating in on/off mode has a larger power-handling capability compared to when operating in its linear mode.
- Since a high-frequency isolation transformer is used (as compared to a 50 Hz transformer in a linear power supply), the size and weight of switching supplies can be significantly reduced.

2.5.2 Half-bridge dc to dc converter

Figure 2.7a shows a half-bridge dc to dc converter [32]. The capacitors C_1 and C_2 establish a voltage midpoint between zero and the input dc voltage. The switches T_1 and T_2 are turned on alternatively, each for an interval t_{on}. With T_1 on, $v_{oi} = (N_2/N_1)(V_d/2)$ as shown in Figure 2.7b and, therefore,

$$v_L = \frac{N_2 V_d}{N_1 2} - V_0 \qquad 0 \leq t \leq t_{on} \tag{2.21}$$

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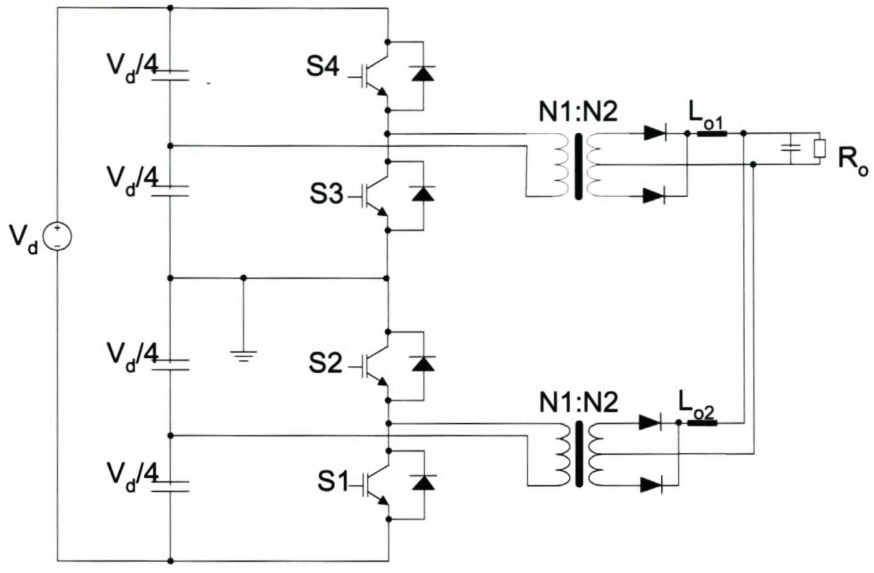

Figure 2.8: *ISOP half-bridge converter.*

During the interval Δ, when both switches are off, the inductor current splits equally between the two secondary halves. Assuming ideal diodes, $v_{oi} = 0$, and therefore,

$$v_L = -V_0 \qquad t_{on} \leq t \leq t_{on} + \Delta \tag{2.22}$$

In steady state, the waveforms repeat with a period $(1/2)T_s$ and

$$t_{on} + \Delta = \frac{1}{2}T_s \tag{2.23}$$

Equating the time integral of the inductor voltage during one repetition period to zero using Eq. 2.21 through to Eq. 2.23 yields

$$\frac{V_0}{V_d} = \frac{N_2}{N_1}D \tag{2.24}$$

where $D = t_{on}/T_s$ and $0 \leq D \leq 0.5$.
The average value of v_{oi} in Figure 2.7b equals V_0.

2.5.3 Series stacked half-bridge dc to dc converter

The fact that the auxiliary power supply is designed for a DC bus voltage of between 750 V and 1000 V makes a switching device like a MOSFET unsuitable for usage in this

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application. Therefore, an insulated gate bipolar transistor (IGBT) should be used due to the high input voltage. For an IGBT the switching frequency must be limited around 30 kHz for good efficiency due to the tail current. To increase the switching frequency for reduction of the system size while maintaining the efficiency requirement, a MOSFET should be considered for a switching device. However, due to the high input voltage, a MOSFET cannot be used in a conventional bridge topology unless the device is series connected to sustain the high voltage [19]. Several papers in the literature [20], [21], [22] and [23] address the issue of the voltage balancing at the device turn-off. To achieve the voltage balancing a passive and active balancing method is used. The passive method requires a snubber circuit and this causes additional loss and restricts the switching frequency. The active methods require complicated control circuits to achieve the voltage balancing, and the control delay of the voltage-balancing controller can increase the device stress, so that the switching speed is restricted. Moreover, perfect balancing is hard to accomplish during the switching transients [19].

The problems of the device series connection can be solved by the input-series-output parallel (ISOP)-connected converter configuration proposed by Kim et al [24]. Figure 2.8 shows the ISOP half-bridge converter. In this configuration the input voltage is divided by the series-connected input capacitors, and the outputs are paralleled. The series-connected converter experiences only the divided input voltage so that a lower voltage rating device, i.e. MOSFET, can be used for higher switching frequency operation.

2.5.4 Transformer design: dc-dc inverters

It is desirable to have power transformers that are small in weight and size and also have low power losses. The motivation for switching at high switching frequencies, is to reduce the size of the power transformer and the filter components [32]. If this benefit is to be realized, the power loss in the transformer core should remain low even at higher frequencies.

For bidirectional core excitation topologies such as the half-bridge topology, it is important to ensure that there is no volt-second imbalance during the two half-cycles of operation as this will cause the transformer to saturate. In a practical implementation,

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there are several causes of such a volt-second imbalance, such as unequal conduction voltage drops and unequal switching times of the switches. Use of an appropriate control integrated circuit (IC) eliminates saturation under start-up and transient conditions. The other way to prevent core saturation due to voltage imbalance is to use a blocking capacitor in series with the primary winding of the full-bridge inverters [32]. For the half-bridge inverter no extra DC blocking capacitors are required since the two series connected DC bus capacitors form a DC blocking capacitor.

2.6 SWITCHING DEVICES

2.6.1 Introduction

The future development of power electronic system engineering, particularly in terms of energy saving, control dynamics, noise reduction, volume and weight minimization, is being driven by new power semiconductor components. The impending technology shift is being driven by the following requirements [27]:

- Energy saving through the use of new circuit topologies based on modified semiconductor concepts.
- Intelligent energy management.
- Miniaturization of electrical systems through the use of ultra fast switching components.
- Cost reduction through system integration.
- Increase in reliability through higher integration densities.
- Increase in operating temperature.
- Integration of power electronics and mechanics.

The prime movers driving the technology shift in power electronics are the pressure to rationalize the use of energy, cost optimization of power electronic system management.

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2.6.2 A new high-voltage power MOSFET

MOSFET devices are quite interesting in terms of switching speed and easy driving capability. However, in high voltage devices the technology process leads to high values of the on-state resistance, thus reducing the current-carrying capability. In on-state conditions, power MOSFET devices experience high power losses, which increase at increasing temperatures. Standard technology for high-voltage power MOSFET manufacturing is reaching its own physical limit: a reduction of the device on-state resistance is strongly limited by the drain resistivity value, which is designed according to the requirements of high-voltage blocking capability [25]. Hence a reduction of the on-state resistance $R_{ds(on)}$ is a key factor analyzed in recent years by the power MOSFET designers [25]. Recently a new concept of power MOSFET design has been proposed that is able to overcome this limitation [26]: the drain charge balance allows increasing the doping concentrations of the conduction region while maintaining the requested blocking capability. The reduction in the silicon conduction losses allow a valuable resizing of the physical die size, together with a convenient package reduction. The range of the device applications is allocated in switching converters such as Switch Mode Power Supplies (SMPS), Power Factor Correctors (PFC) and portable welding equipment [25].

2.6.3 CoolMOS Technology

The CoolMOS technology - developed for the production of charge compensated devices is presented and discussed in the literature [26], [27], [28]. Due to its novel internal structure the device offers a dramatic reduction of the on-state resistance with a completely altered voltage dependence of the device capacitances.

As a result of the immense reduction in the chip area, CoolMOS transistors exhibit a very low input capacitance in comparison with identical transistors in conventional technology. CoolMOS transistors can be operated with the lowest control power, the cheapest driver circuit and the highest switching frequencies [27]. The typical value of the threshold voltage $V_{gs(th)}$ is 4.5 V (range 3.5 V to 5.5 V at $25°C$), yet in spite of this, the CoolMOS transistors reach their nominal $R_{ds(on)}$ already at 10 V gate voltage [27]. The controllability of the di/dt and dv/dt values of these devices is a strong advantage for the application engineer [27].

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2.6.4 IGBT in NPT Technology

In virtually all fields of application for high-speed, high voltage switches, MOSFET and IGBT devices have now completely ousted bipolar junction transistors [35]. Whereas for a long time the area of low switching frequencies ($\leq$ 50 kHz) has appeared to be the domain of the IGBT, modern high-speed IGBTs are now beginning to compete with MOSFETs even in their traditional fields of application, i.e. switch mode power supplies.

High-speed IGBTs are making inroads wherever their specific advantages can be fully utilized, these being [35]:

- Excellent ruggedness (short circuit protection, latch-up free, avalanche rated).
- Superior on-state characteristics at high currents.

Because of their superior current-carrying capability and ruggedness, IGBTs have gained greatest acceptance in their traditional application field of drive systems. However, the development of the ultra-fast IGBT has now drastically extended this field.

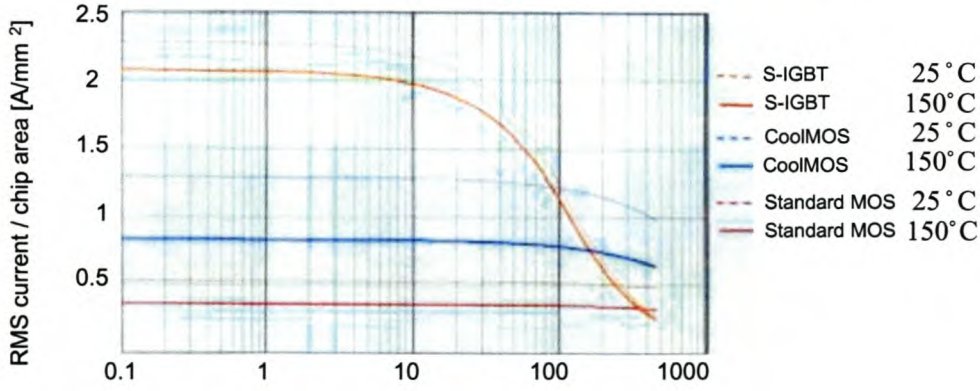

Figure 2.9: *Current-carrying capability per chip area as a function of the switching frequency; a standard MOSFET, CoolMOS and IGBT compared (taken from [35]).*

As Figure 2.9 shows, the IGBT is superior in terms of current-carrying capability to the standard MOSFET up to 300 kHz and beyond, depending on the power dissipation density, and to the CoolMOS under typical operating conditions up to around 100 kHz [35].

These high possible operating frequencies make the IGBTs ideally suitable for switch mode power supplies and power factor corrector (PFC) applications.

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2.7 SUMMARY

The two topologies suitable for DC reticulation were discussed and compared. The FCMLI emerged as the most suitable choice for the DC reticulation application, as compared to the DCMLI.

Switch mode power supplies were investigated for possible use in the design and development of an auxiliary power supply. The input-series-output-parallel topology showed great potential in this regard as this topology presents a possibility of using small, fast switching and low cost switching devices, e.g. MOSFETs.

The possibility of using the new-state-of-the-art switching devices, i.e. CoolMOS and fast IGBT technology, was explored. A careful selection between these devices could lead to a low cost and efficient design.

PWM strategies from recent literature were discussed, and the FPGA based digital pulse width modulation (DPWM) was chosen for the controller, since this method is suitable for interleaved PWM switching.

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CHAPTER 3

SYSTEM OVERVIEW

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Parameter	Value	Unit
Power rating	3.5	kVA
Input voltage	750 - 1000	V DC
Output voltage	230 $\pm$10%	V_{RMS}
Output frequency	50	Hz
Switching frequency	50	kHz
Maximum operating temperature	40	$°C$

Table 3.1: *System specifications.*

3.1 INTRODUCTION

This chapter contains a brief system overview. The system specifications are presented in Table 3.1 and the purpose of the main system components are discussed below.
The system is comprised of a flying capacitor multilevel inverter, a controller, two soft-starting switches, an output filter, an auxiliary power supply and the load.
The sections that follows provide a brief overview of the individual components of the system.

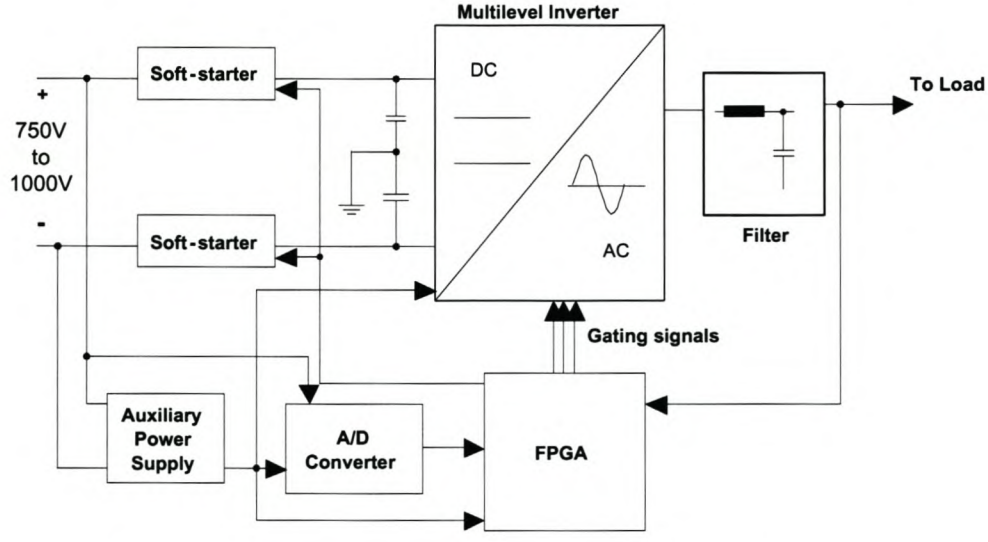

Figure 3.1: *Block diagram of the system.*

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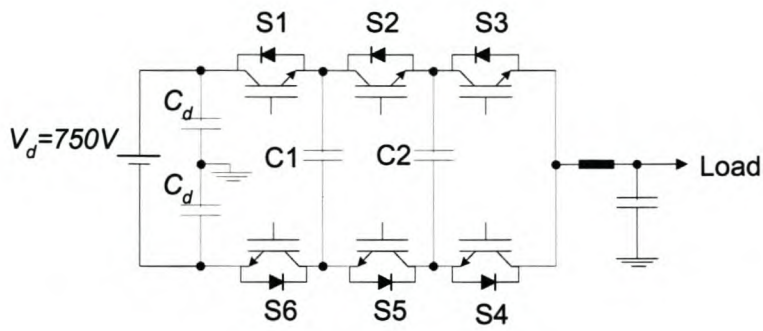

Figure 3.2: *A four level multilevel inverter.*

3.2 THE FLYING CAPACITOR MULTILEVEL INVERTER

The proposed solution to address the non-technical power loss problem, is to apply DC reticulation at high DC voltage levels. This method requires a single-phase inverter to invert the high DC voltage to a 50 Hz, $230 \pm 10\%$ V_{RMS} supply for the household appliances. A flying capacitor multilevel inverter (FCMLI) was chosen over the diode clamped multilevel inverter (DCMLI) because of the following:

- The clamping diodes of a DCMLI have a relatively high voltage rating. Because of this, multiple clamping diodes may be required at high voltage levels.
- For a single-phase DCMLI, a large voltage ripple appears across the DC bus capacitors.
- Possible capacitor voltage balancing problems may be experienced for a DCMLI with more than three levels.

The inverter designed for this system is a four-level FCMLI, Figure 3.2, using 600 V fast IGBTs. The decision to build a four-level FCMLI with these devices is based on the cost analysis which follows later in Chapter 7. Special attention will be given to the design of a low cost gate drive circuit and the pre-charging mechanism of the flying capacitors.

3.3 THE CONTROLLER

The controller consists mainly of an FPGA (Field programmable Gate array) and an analog-to-digital converter. The gating signals for the switching cells are generated by

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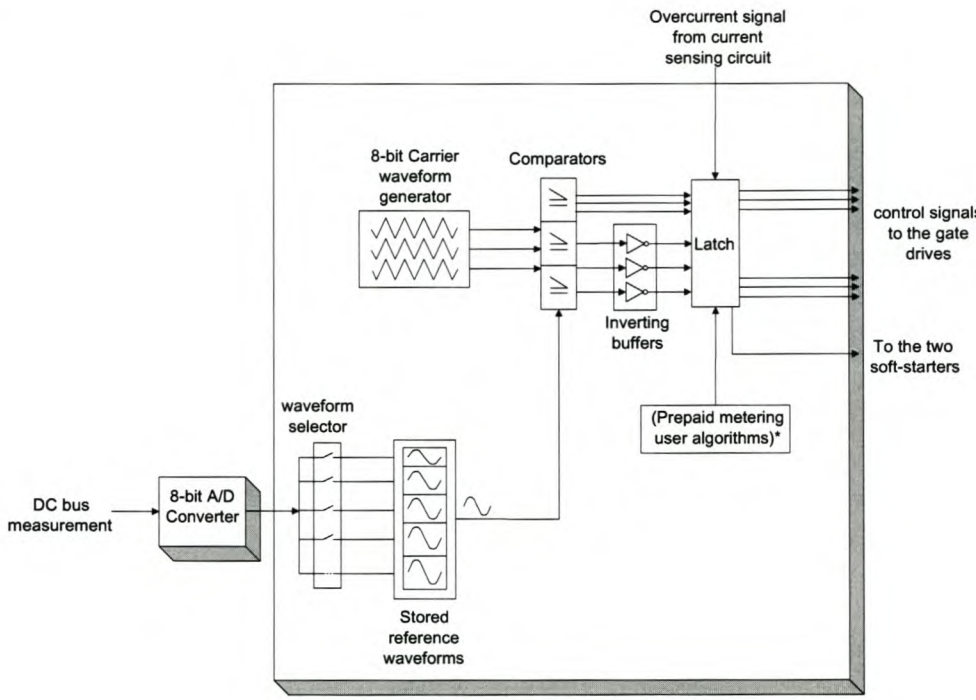

Figure 3.3: *Functional block diagram of the control.*

comparing a reference sine waveform stored inside the FPGA with p triangular carrier waveforms phase-shifted by $2\pi/p$, with p the number of switching cells. This interleaved switching method results in an apparent switching frequency equal to p times the switching frequency of a single cell, (pf). An output voltage regulator is required to ensure that the inverter's output voltage remains within the specified range of 230 V_{RMS} $\pm 10\%$ for any given DC input voltage between 750 V and 1000 V.

A simple feed-forward control technique is used to regulate the output voltage by monitoring the DC input voltage. This control technique uses an analog-to-digital converter to measure the input DC voltage. The controller is also used for overcurrent and shortcircuit protection for the system by monitoring the output current with the use of a current sensing circuit. The controller also operates the two soft starting switches.

In the final unit the controller may contain the prepaid metering algorithms as well as the algorithms for the user interface. This will make the system more immune to by-passing

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Parameter	Value	Unit
Power rating	15	W
Input voltage	750 - 1000 V DC	V
Switching frequency	50	kHz
Regulated dc output voltages:		
Output 1	30	V
Output 2	30	V
Output 3	22	V
Output 4	22	V
Output 5	22	V
Output 6	7	V

Table 3.2: *Specifications for the auxiliary power supply.*

and tampering.

3.4 THE AUXILIARY POWER SUPPLY

The flying capacitor multilevel inverter's controller and gate drive circuits need regulated dc power supplies for them to operate and start-up the inverter. The problem is that the inverter is exposed only to a dc input voltage between 750 V and 1000 V. This high dc voltage should be used to generate regulated dc power supplies for the FCMLI electronic circuitry. A switch mode power supply which will incorporate a self-starting circuit is therefore required. This switch mode power supply has to have electrically isolated multiple dc regulated supplies for the system's electronic circuitry. The specifications of this auxiliary power supply are summarized in Table 3.2.
To adhere to the electrical isolation requirement for the FCMLI gate drive circuits, a dc-dc inverter with electrical isolation should be used for this application. If a conventional half-bridge topology is used for the auxiliary power supply, then an IGBT should be used instead of a MOSFET. This is because of the high input voltage of between 750 V - 1000 V. But due to the high cost of a 1200 V rated IGBT and its inability to switch at a high frequency, a MOSFET was considered for a switching device.

To allow the use of a smaller, faster switching device like a MOSFET, the auxiliary power

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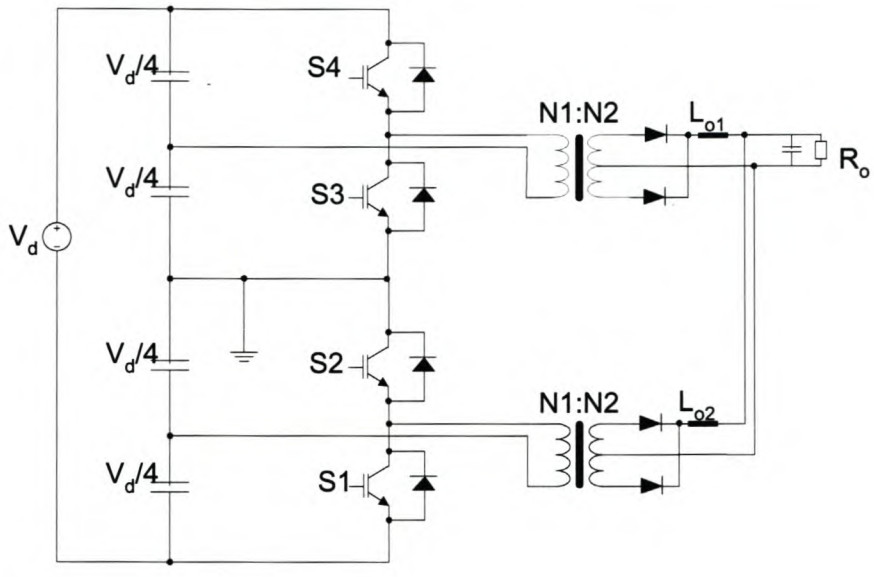

Figure 3.4: *An ISOP-based auxiliary power supply.*

supply is designed as an inverter based on the input-series-output-parallel (ISOP) inverter topology. This inverter is mainly built out of two conventional half-bridge inverters connected in series. The fact that a self-starting circuit of a conventional half-bridge inverter is complex, makes that of an input-series-output-parallel inverter even more complex to design.

3.5 THE SOFT-STARTERS

At start-up the DC-bus capacitors initially appear as a short circuit across the dc source, which may result in an unacceptably large inrush current. To limit this inrush current, a series element between the dc side of the rectifier and the DC-bus capacitors can be used. Two series elements are required per system, since the midpoint of the two DC capacitors of a system will be connected to the ground. This configuration means that the bottom capacitor of the DC bus of a system is connected in parallel to the bottom capacitor of another system in close proximity. The second series element limits the inrush current into this bottom DC capacitor. These series elements could either be a:

- Thermister
  A thermister has a large resistance when it is cold, thus limiting the inrush current

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at start-up. As this element heats up, its resistance goes down to a reasonably low value to yield a reasonable efficiency. However, it has a long thermal time constant, and therefore if a short term power outage occurs that is long enough to discharge the DC-bus capacitors but not long enough to allow the thermister time to cool down, a large inrush current can result when power is restored.

- Current-limiting resistor
  A current-limiting resistor is used in conjunction with a parallel connected semiconductor switch to make up the series element. Initially the switch is off and the current-limiting resistor limits the inrush current at start-up. When the DC-bus capacitors are charged up, the switch is turned "on", thus bypassing the current-limiting resistor.

From the brief description of the series elements, the current-limiting resistor seemed to be much more effective as compared to the thermister. This soft-starting series element in conjunction with the auxiliary power supply and pre-charging resistors help with the pre-charging of the DC capacitors (DC bus and flying capacitors) prior to the switching of the inverter.

3.6 LOAD

The loads for this system are household appliances, i.e a television set, a refrigerator and a small stove. A load profile analysis of typical household appliances was conducted and the inrush currents for these appliances when being switched "on" are shown in Figure 3.5 and Table 3.3.
A worst case scenario is when the appliances are switched "on" simultaneously, e.g. when power is restored after power outage. During this time the start-up current will

Appliance	start-up Current (A_{peak})	start-up Current (A_{rms})
Refrigerator	9	6.4
Television	25	17.7
Small stove	14	9.9
Video recorder	20	14

Table 3.3: *Load profiles of typical household appliances.*

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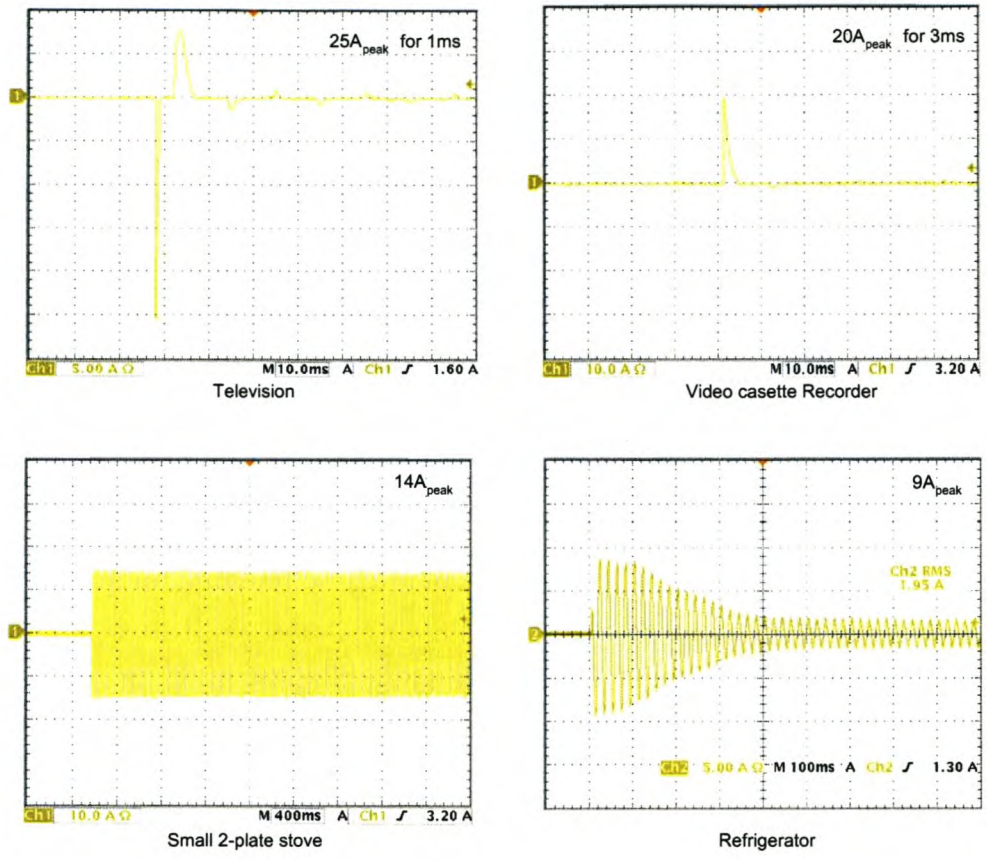

Figure 3.5: *Load profiles of typical household appliances at turn on.*

be equal to $48A_{rms}$, which is the sum of the start-up currents of all the appliances. The system has to be designed in such a way as to be able to handle a current of this magnitude for a few cycles without going into overcurrent protection mode.

3.7 SUMMARY

The entire system was overviewed in this chapter. Also the main system components were discussed and the following conclusions reached:

- For the inverting unit the flying capacitor multilevel inverter was chosen over the diode clamped multilevel inverter mainly due to the simplicity of using interleaved switching for these inverters.

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- A digital FPGA-based PWM controller was chosen, because this controllers are particularly suitable for interleaved switching.
- Due to the high input voltage to the inverting unit, the choice of a switch mode power supply (SMPS) to be used as an auxiliary power supply was confined to the input-series-output-parallel inverter topology. This topology allows the use of smaller, faster and cost-effective switching devices despite the high input voltage to the inverter.
- Two soft-starters are required per system. A combination of a current limiting resistor and a parallel switch seems to be more effective as a soft-starter than a thermister.
- Typical household loads were analysed. It was found that the start-up power required for the household appliances when they are all switched "on" simultaneously is equal to 11 kVA. Therefore the system should be able to provide 11 kVA start-up power for a short duration of time (a few cycles).

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CHAPTER 4

INVERTER DESIGN

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4.1 INTRODUCTION

This chapter investigates the design of a low cost gate drive circuit for a flying capacitor multilevel inverter (FCMLI). The inverter's output filter, heat sink and DC capacitors are also designed in this chapter. The flying capacitor pre-charging problem is outlined and a start-up mechanism that addresses this problem is presented. The specifications of the inverter are summarized in Table 4.1. A full circuit diagram of the inverter with all the components and their designed values is shown in Figure 4.1.

Parameter	Symbol	Value	Unit
Power rating	S	3.5	kVA
Input voltage	V_d	750 - 1000 V DC	V
Output voltage	V_0	230 $\pm$10%	V_{RMS}
Maximum output current	I_0	22.5	A
Output frequency	f_0	50	Hz
Switching frequency	f_s	50	kHz
Operating temperature	T_a	40	$°C$

Table 4.1: *Inverter specifications.*

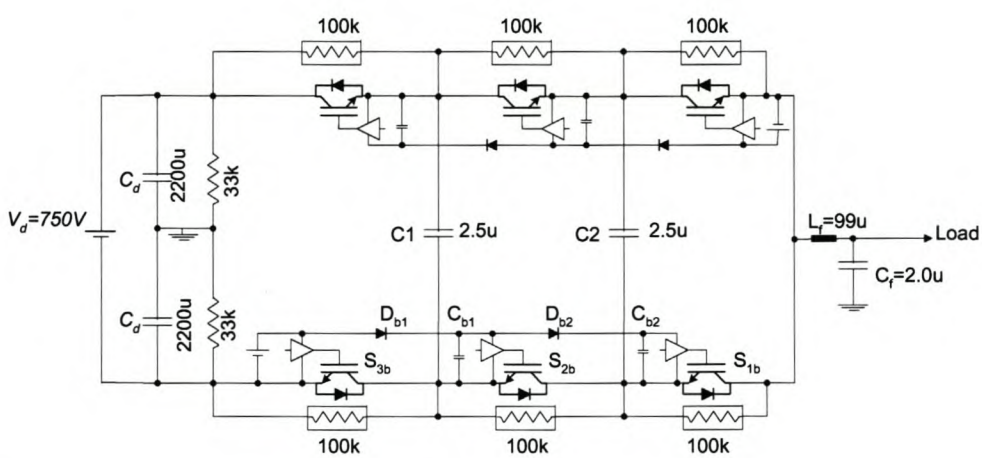

Figure 4.1: *A full circuit diagram of the inverter showing the designed component values.*

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4.2 GATE DRIVES

4.2.1 Introduction

The primary function of a gate drive circuit is to switch a power semiconductor device from the off state to the on state and vice versa. The drive circuit is the interface between the control circuit and the power switch. It amplifies the control signals to levels required to drive the power switch and provides electrical isolation between the power switch and the control circuit. Electrically isolated drive circuits require isolated dc power supplies [32].

Advantages of multilevel inverters come at the expense of added switching components. One factor that escalates the overall cost of inverters is the need for isolated dc power supplies for the gate drives. Given the large number of switching components for multilevel inverters and the need for isolated dc power supplies, it is important to make the gate drive circuits as inexpensive as possible without compromising efficiency and reliability. To accomplish a cost-effective design of the gate drives, a new bootstrap power supply for multilevel inverters was developed (Section 4.2.3).

4.2.2 Dc power supply

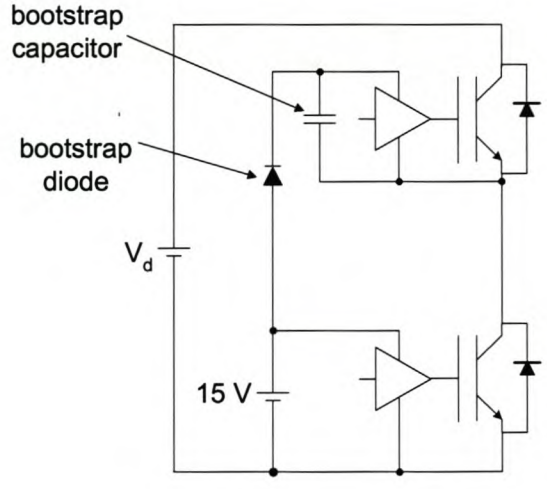

Figure 4.2: *A half-bridge inverter with bootstrap power supply.*

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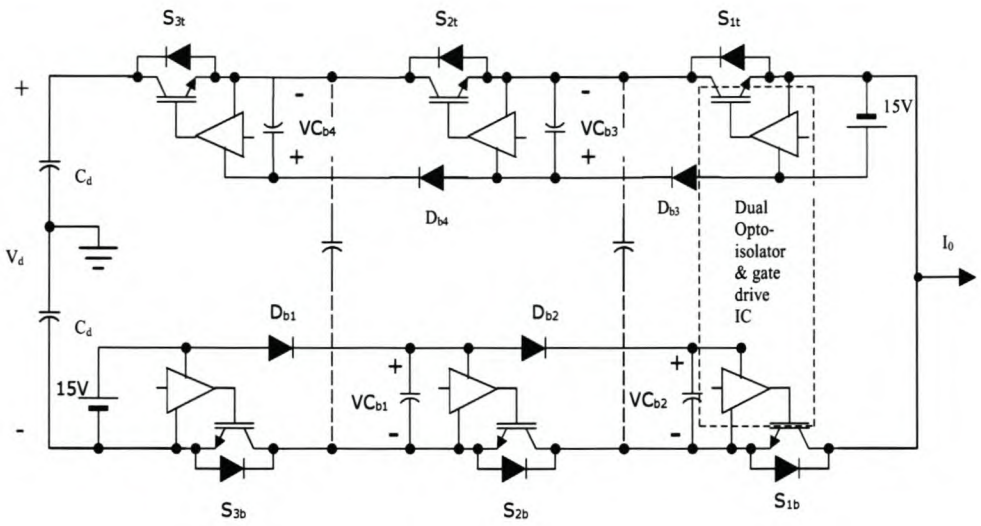

Figure 4.3: *A four-level multilevel inverter with bootstrap power supply.*

This bootstrap power supply for multilevel inverters, Figure 4.3, is an extension of the standard bootstrap power supply for a half-bridge inverter shown in Figure 4.2.

A p-level multilevel inverter is comprised of a series connection of $(2p - 2)$ switching devices, which is the same as connecting $(p - 1)$ half-bridge inverters in series. This is illustrated by Figure 4.3, which is a four-level multilevel inverter with bootstrap powered gate drive circuits.

The operation of this bootstrap power supply for multilevel inverters is as follows: There has to be two 15 V isolated power supplies from the auxiliary power supply discussed in Chapter 6. The operation is discussed using only the bootstrap power supply of the bottom switches, Figure 4.3.
The 15 V power supply from the auxiliary power supply is directly connected to the supply voltage terminal (V_{cc}) of the first gate drive, i.e. gate drive of switch S_{3b}. Turning this switch "on" pulls the emitter of switch S_{2b} to the same voltage potential as the ground terminal of the 15 V power supply voltage. This charges the bootstrap capacitor voltage (V_{Cb1}) through the bootstrap diode (D_{b1}). This bootstrap capacitor voltage (V_{Cb1}) provides a supply voltage to the V_{cc} terminal of the gate drive circuit of switch S_{2b}. By the same mechanism, the bootstrap capacitor C_{b2} will charge whenever switch S_{2b} is turned

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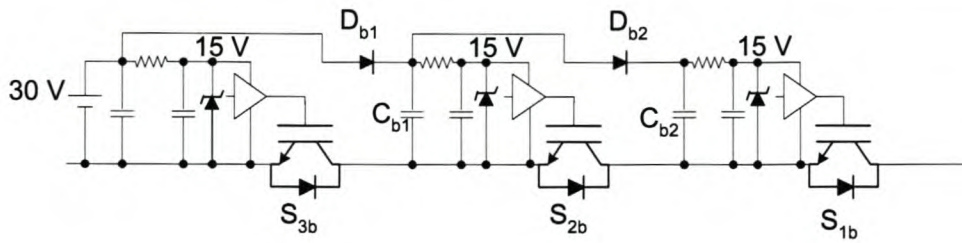

Figure 4.4: *Modified bootstrap power supply.*

"on". The bootstrap power supply of the top switches is operated in the same way.

The problem experienced with the circuit of Figure 4.3 was a voltage drop of approximately 1 V across each bootstrap diode. With a 15 V auxiliary power supply, the bootstrap capacitor voltage V_{Cb1} will be equal to $15 - V_{Db1} \approx 14V$ and the bootstrap capacitor voltage V_{Cb2} will be equal to $15 - (V_{Db1} + V_{Db2}) \approx 13V$.

For a four-level multilevel inverter this might not pose a problem, since the last switch's gate drive will be fed with 13 V, which is enough to turn "on" the gate of a MOSFET or IGBT. A problem arises with the increase in the number of levels. For example, the last switch of an eight-level multilevel inverter using this bootstrap power supply will see a gate voltage of approximately 9 V. This gate voltage is too small to be able to turn "on" the gate of a MOSFET or IGBT.
The problem was solved by increasing the power supply voltage of the auxiliary power supply from 15 V to 30 V and regulating it with a simple zener-based regulator to yield 15 V for the gate drive circuits, Figure 4.4. The voltage drops across the bootstrap diodes are inevitable, but this method allows the gate drive circuit of each switch to be supplied with 15 V.

Two major requirements that the bootstrap diode for multilevel inverters need to satisfy are that it should be able to block the cell voltage and it should be a fast recovery diode to achieve a high switching frequency.

A shortcircuit on the DC-bus or the flying capacitors is avoided by electrically isolating the control signals. This is accomplished by using a low cost dual integrated opto-coupler

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and gate drive integrated circuit (HCPL-314J) [38] as an interface between the control circuit and the gate drive circuit. The HCPL314J is suitable for this application, since it has the following features:

- It has two channels integrated in one surface-mount package, therefore it requires less board space.
- Integrated optocoupler and gate drive, a gate driver that also provides electrical isolation between the control circuit and the gate drive circuit.
- It has low power consumption (3 mA operating current), making it suitable for bootstrap technique applications.

4.2.3 Design of the gate resistor and the bootstrap capacitor

The design and selection of the gate resistor and the bootstrap components for the gate drive circuit of Figure 6.2 is as follows:

- Gate resistor.
  IGBTs and MOSFETs are both voltage-controlled devices. To turn on the device, a voltage must be applied between the gate and the source terminals. The gate resistance is designed using the gate to emitter voltage applied to the gate of the switching device.

  Figure 4.5 relates the gate voltage to the gate charge when a constant current is supplied to the gate. During the first voltage rise, the gate-to-source capacitance is charging and during the flat part, the gate-to-drain capacitance is charging. During the second voltage rise, both capacitances are charged and the switching device can be switched on successfully. Therefore Figure 4.5 clearly differentiates between the charge required for the gate-source and gate-to-drain capacitances and the charge required to switch the switching device. This implies that the difference of the applied gate voltage and the voltage corresponding to the flat part of Figure 4.5 is responsible for switching on the gate of a voltage controlled device. For a gate voltage of 15 V, the gate resistance is therefore given by:

$$R_{g(min)} = \frac{V_{gate} - 7}{I_{g(max)}}$$

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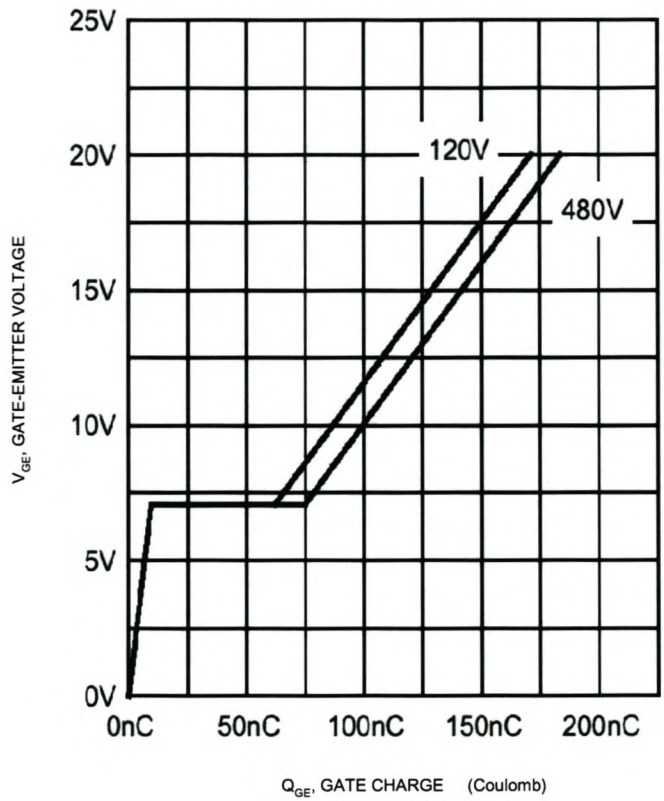

Figure 4.5: *Graph of a typical gate charge of the SKW30N60 CoolMOS [39].*

$$= \frac{15-7}{0.4}$$
$$= 20\ \Omega \tag{4.1}$$

Where $I_{g(max)}$ is the maximum output current of the gate drive IC, V_{gate} is the applied gate to emitter voltage and 7 V is the voltage at which the gate capacitances become fully charged.

The maximum power dissipated in the gate resistor during turn "on" is given by:

$$P_{max(gate)} = I^2_{g(max)} R_{g(min)}$$
$$= (0.4)^2(20)$$
$$= 3.2\ \text{W} \tag{4.2}$$

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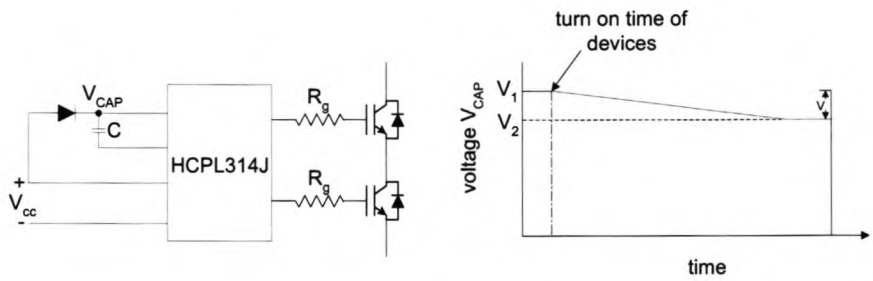

Figure 4.6: *Bootstrap capacitor voltage.*

Since energy is defined as the power dissipated over a period of time, the energy consumed by the gate resistor at turn "on" is given by:

$$\begin{aligned} E_{max(gate)} &= P_{max(gate)} t_{on} \\ &= (3.2)(93 \times 10^{-9}) \\ &= 297 \text{ nJ} \end{aligned} \tag{4.3}$$

Where t_{on} is obtained from the datasheet and is the turn "on" time of the gate.

- Bootstrap capacitor.

  The bootstrap capacitor's selection is based on the fact that, it should be able to provide enough turn "on" energy to the gate of the switching device and the gate drive circuit without its voltage dropping too low. This is illustrated in Figure 4.6.

  The law of conservation of energy states that energy may neither be created or destroyed. Since the sum of all the energies in a system is constant, the energy consumed from the bootstrap capacitor of Figure 4.6 is given by:

$$\text{Energy consumed from the capacitor (C)} = (1/2)CV_1^2 - (1/2)CV_2^2 \tag{4.4}$$

  The total energy consumed from the bootstrap capacitor during turn "on" by the gate drive circuit is summarized in Table 4.2. The energy consumed by the gate drive IC is obtained from its datasheet and the energy consumed by the gate resistor is calculated in Eq. 4.3.

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Energy consumed from the bootstrap capacitor	Symbol	Value	Units
Energy consumed by gate driver IC	E_{IC}	210×10^{-9}	J
Energy consumed by the gate resistor	E_{R_g}	297×10^{-9}	J
Total Energy	$E_{drivecircuit}$	507×10^{-9}	J

Table 4.2: *Energy consumed from the bootstrap capacitor.*

Assuming V_1 and V_2 in Figure 4.6 to be equal to 15 V and 14.5 V respectively, the value of the bootstrap capacitor (C) is calculated using Eq. 4.4 to be:

$$\begin{aligned} C &= \frac{2(210 \times 10^{-9} + 297 \times 10^{-9})}{(15^2 - 14.5^2)} \\ &= 68 \text{ nF} \end{aligned} \tag{4.5}$$

4.3 OUTPUT FILTER

4.3.1 Filter inductor

The purpose of the output filter is to limit the maximum output ripple current, $\triangle i_{max}$, to an acceptable level. To derive the filter inductor equation for multilevel inverters we first start by deriving the equation for an elementary chopper of Figure 4.7, with only one cell ($p = 1$).

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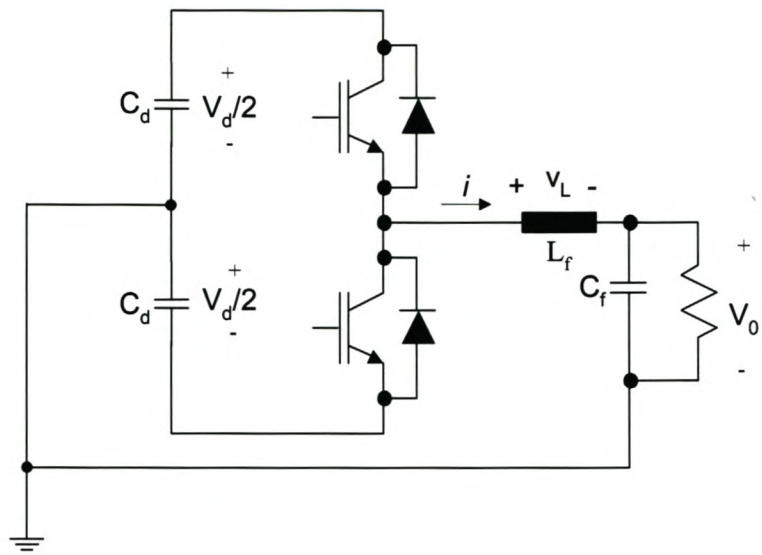

Figure 4.7: *An elementary chopper.*

Knowing that the voltage across an inductor is given by

$$v_l = L_f \frac{di}{dt} \tag{4.6}$$

And knowing that when the top switch is "on", the voltage across the inductor is given by $(V_d/2 - V_0)$. The expression for the ripple current is therefore given by:

$$\triangle i = \left\{ \frac{\left(\frac{V_d}{2} - V_0\right)}{(L_f)} \right\} t_{on} \tag{4.7}$$

Where t_{on} is the "on" time of the top switch in Figure 4.7.

From Figure 4.8 the "on" time of the top switch is given by

$$D_T = \frac{T_s}{2}(f_r(t) + 1) \tag{4.8}$$

Where D_T is the duty cycle of the top switch and $f_r(t)$ is the reference signal applied to the pulse-width modulator.

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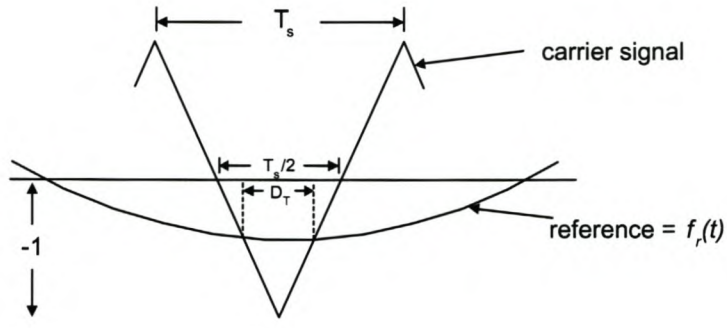

Figure 4.8: *The duty cycle of the top switch.*

Assuming a constant duty cycle, the output voltage (V_0) is equal to $(V_d/2)f_r(t)$. The ripple current in the inductor is therefore given by:

$$\begin{aligned} \triangle i &= \frac{1}{2}\left\{\frac{(\frac{V_d}{2} - \frac{V_d}{2}f_r(t))}{L_f}\right\} T_s(1 + f_r(t)) \\ &= \frac{V_d}{4L_f}(1 - f_r(t))(1 + f_r(t))T_s \end{aligned} \tag{4.9}$$

The ripple current is maximum when its derivative is equal to zero. The derivative of the ripple current is given by:

$$\frac{d\triangle i}{df_r(t)} = \frac{V_d T_s}{4L_f}(2f_r(t)) \tag{4.10}$$

Since the ripple current is maximum when $d\triangle i/df_r(t) = 0$, therefore $\triangle i$ is at its maximum when $f_r(t) = 0$. Hence, the maximum ripple current Δi_{max} is given by:

$$\triangle i_{max} = \frac{V_d}{4L_f}T_s \tag{4.11}$$

Solving for L_f, from Eq. (4.11) yields:

$$L_f = \frac{V_d}{4f_s \triangle i_{max}} \tag{4.12}$$

Eq. 4.12 is for an elementary chopper with only one cell.

For multilevel inverters the effective switching frequency is (pf_s) and the size of the voltage steps is given by V_d/p where p is the number of switching cells. Therefore for multilevel inverters the filter inductor equation is given by:

$$L_f = \frac{V_d}{4p^2 f_s \triangle i_{max}} \tag{4.13}$$

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For a four-level multilevel inverter with V_d equal to 1000 V, switching frequency of 50 kHz and a worst case maximum ripple current assumed to be 5.6 A (25% of the peak output current), the value of the filter inductor was calculated to be 99 μH.
An inductor with an inductance value of 99 μH was designed. The design input parameters are given in Table 4.3.
The design procedure consists of several parts and it is as follows:

- Core selection
  The selection of a core is influenced by the operating frequency. For a 50 kHz switching frequency a ferrite core will be the first choice. E-cores are suitable for high power applications such as switch mode power supplies and DC to DC or DC to AC inverters. A general purpose ETD 59 ferrite E-core made of an F6 material was chosen mainly because it offers medium permeability and high saturation. The properties of this chosen e-core as given on its datasheet are summarized in Table 4.4.

- Number of turns.
  Knowing that $v = N(d\varphi/dt)$ (Faraday's law) and that $v = L_f(di/dt)$ (voltage across an inductor), and assuming a linear relationship between the magnetic flux and current we get:

$$\begin{aligned} N &= \frac{L_f \hat{I}}{\hat{B}_{max} A_{core}} \\ &= \frac{(99 \times 10^{-6})(28.1)}{(270 \times 10^{-3})(368 \times 10^{-6})} \\ &= 28 \text{ turns} \end{aligned} \tag{4.14}$$

  Where L_f is the inductance of the output filter, $\hat{B}_{max}$ is the maximum saturation flux density, $\hat{I}$ is the maximum current flowing in the inductor and A_{core} is the effective area of the core.

Parameter	Symbol	Value	Units
Inductance	L_f	99	μH
Inductor maximum current	$\hat{I}$	28.1	A
Switching frequency	f_s	50	kHz

Table 4.3: *Output filter inductor's design input parameters.*

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Part number	Frequency range (kHz)	Effective area (A_{core})	Bobbin window area (A_w)	Saturation flux density ($\hat{B}_{max}$)
ETD 59	10 - 400	368 mm^2	730 mm^2	270 mT

Table 4.4: *The properties of the ETD 59 E-core.*

- Air gap.
  The reluctance $\Re_g$ of an air gap (g) of length l_g is given by [33]:

$$\Re_g = \frac{l_g}{\mu_0 A_{core}} \tag{4.15}$$

The magneto-motive force MMF produced by a conductor (with N turns) carrying current I is defined by:

$$MMF = NI \tag{4.16}$$

Since the produced MMF is a function of the magnetic flux generated and the total reluctance ($\Re$) in the core, the MMF can be defined as:

$$\begin{aligned} NI &= (\Re_c + \Re_g)\varphi \\ &\approx \Re_g \phi \qquad \text{for } \Re_g >> \Re_c \\ N\hat{I} &= \Re_g \hat{B}_{max} A_{core} \qquad \text{for maximum flux } (\varphi_{max}) = \hat{B}_{max} A_{core} \end{aligned} \tag{4.17}$$

Substituting Eq. (4.15) into Eq. (4.17) yields

$$l_g = \frac{\mu_0 N \hat{I}}{\hat{B}_{max}} \tag{4.18}$$

Where μ_0 is the permeability of free space.

With the number of turns equal to 28 (from Eq. 4.14), the length (l_g) of air gap g is given by:

$$l_g = \frac{\mu_0 N \hat{I}}{\hat{B}_{max}}$$

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$$\begin{aligned} &= \frac{(4\pi \times 10^{-7})(28)(28.1)}{270 \times 10^{-3}} \\ &= 0.0037 \text{ m} \\ &= 3.7 \text{ mm} \end{aligned} \tag{4.19}$$

- Winding parameters

  The area of the copper wire (A_{Cu}) is determined by the current flowing in it. With a maximum $\hat{I}$ of 28.1 A given in Table 4.3 and a maximum current density of 6 A/mm^2, the maximum inductor current will require a copper wire with a cross-sectional area equal to 4.68 mm^2. The skin depth in the copper wire at 50 kHz switching frequency is given by [32]:

$$\begin{aligned} \delta &= \sqrt{\frac{2}{\mu_i \sigma \omega}} \\ &= \sqrt{\frac{2}{(1800)(0.01)2\pi(50000)}} \\ &= 0.0006 \text{ m} \\ &= 0.6 \text{ mm} \end{aligned} \tag{4.20}$$

  Where μ is the magnetic material's permeability, σ is the conductivity of the material and ω is the angular switching frequency.

  If the diameter of the copper wire is $\leq 2\delta$, then the problems associated with skin effect can be neglected. Since $2\delta = 1.2$ mm, a copper wire with a diameter of 1.0 mm was selected. The cross-sectional area of this 1.0 mm diameter wire is given by:

$$\begin{aligned} A_{Cu} &= \pi r^2 \\ &= 0.78 \text{ mm}^2 \end{aligned} \tag{4.21}$$

  But the desired conductor area is equal to 4.68 mm^2. Therefore six conductors with a diameter of 1 mm and a cross-sectional area of 0.78 mm^2 are placed in parallel to make the desired conductor area.

  The copper fill factor (K_{Cu}) of a litz wire is 0.3 [32]. Therefore from the equation

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of K_{Cu} given by [32], the maximum number of turns is given by:

$$\begin{aligned} N &= \frac{K_{Cu}A_w}{A_{Cu}} \\ &= \frac{(0.5)(730)}{0.78} \\ &= 468 \text{ turns} \end{aligned} \tag{4.22}$$

The bobbin is capable of fitting 468 conductors of 1 mm in diameter. The number of turns required to make an inductance of 99 μH are equal to 28. Using six conductors in parallel gives a total number of $28 \times 6 = 168$ which is less than the maximum number of turns.

4.3.2 Filter capacitor

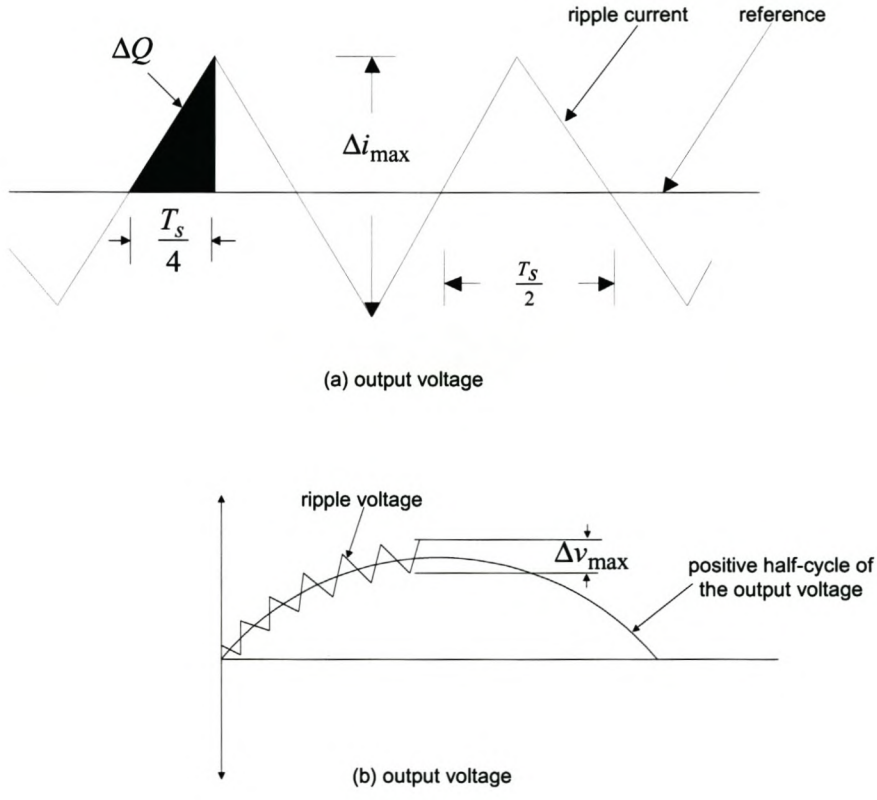

Figure 4.9: *Current and voltage in the filter inductor.*

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The capacitor in the filter has to divert the ripple component of current so that only the fundamental current is delivered to the load. The filter capacitor of a multilevel inverter is designed for the same current amplitude and ripple voltage as in a conventional inverter but the effective switching frequency is (pf_s) instead of f_s [30]. The voltage ripple in the capacitor is given by:

$$\triangle v = \frac{\triangle Q}{C_f} \tag{4.23}$$

Knowing that the ripple current waveform in an inductor is a triangular periodic waveform, from Figure 4.9 we have:

$$\triangle Q = \frac{T_s}{4}(\frac{\triangle i_{max}}{2}) \tag{4.24}$$

Therefore the ripple voltage in the filter capacitor of an elementary chopper, with $p = 1$, is given by:

$$\triangle v_{max} = \frac{\triangle i_{max}}{8 f_s C_f} \tag{4.25}$$

The ripple voltage of a multilevel inverter with p cells is given by:

$$\triangle v_{max} = \frac{\triangle i_{max}}{8 p f_s C_f} \tag{4.26}$$

Assuming a peak to peak current ripple of 25 % the output current, the RMS current $(I_{c(rms)})$ in the filter capacitor is estimated by [34]:

$$\begin{aligned} I_{c(rms)} &= \left(\frac{\Delta i_{max}}{2}\right)\frac{1}{\sqrt{3}} \\ &= \left(\frac{5.6}{2}\right)\frac{1}{\sqrt{3}} \\ &= 1.62 \text{ A} \end{aligned} \tag{4.27}$$

Substituting Eq. 4.13 into Eq. 4.26 gives the expression for the output filter capacitor of a multilevel inverter.

$$C_f = \frac{V_d}{32 p^3 f_s^2 L_f \triangle v_{max}} \tag{4.28}$$

For a four-level multilevel inverter with V_d equal to 1000 V, switching frequency of 50 kHz, an assumed maximum ripple voltage of 2% the peak output voltage (6.5 V) and a filter inductor value of 99 μH, the value of the filter capacitor was calculated to be equal

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to $0.7\ \mu F$. Since the peak output voltage can reach a maximum of 340 V ($240 \times \sqrt{2}$), the voltage rating of the filter capacitor has to be more than 340 V. Any capacitor with a capacitance of more than $0.7\ \mu F$ and a voltage rating of more than 340 V can be used as the filter capacitor. Due to unavailability of a 400 V, $1\mu F$ capacitor, a 1000 V, $2\mu F$ capacitor was used instead.

4.4 DC CAPACITORS

4.4.1 Flying capacitors

The safety of operation of a multilevel inverter may depend on the voltage distribution in the flying capacitors. For this reason, it is very important to check the stability of this voltage distribution, i.e., determine whether the system is capable of compensating for small (or even large) perturbations around the balanced point of operation [31]. If the duty cycles are identical and the phase shift between adjoining cells is $(2\pi)/p$, the natural stability of the voltage distribution will be ensured.

However, Hochgraf et al [6] mentioned that pre-charging of these capacitors at start-up is more complex. During start-up, devices could be unevenly stressed while the system evolves towards balanced distribution. Depending on the time the system will take to balance, so many things might happen which may lead to destruction of the entire system. Therefore provisions should be made for this (see Section (4.3.1)).

Due to the natural stability of the voltage distribution [12], a maximum voltage of 333 V (this value is for a three cell inverter with a maximum DC bus voltage of 1000 V) is applied across each blocking switch. This voltage is clamped with the use of flying capacitors. During a switching cycle the output current flowing through the floating capacitors causes a voltage ripple. This voltage ripple (bound at 5 % of the DC-bus voltage, i.e. 50 V), the switching frequency (50 kHz), phase shift between cells $(2\pi)/p$ and the output current (15.9 A_{RMS} for a 3.5 kVA system) allow us to use Eq. 4.29 to calculate the value of the flying capacitors.

$$C_k = \frac{\phi I_0}{2\pi \triangle V_c f_s} \tag{4.29}$$

From Eq. 4.29, the flying capacitor value is $2.1\ \mu$F. The two flying capacitors should have voltage ratings of 333 V and 666 V. Due to unavailability of a $2.1\ \mu$F capacitor,

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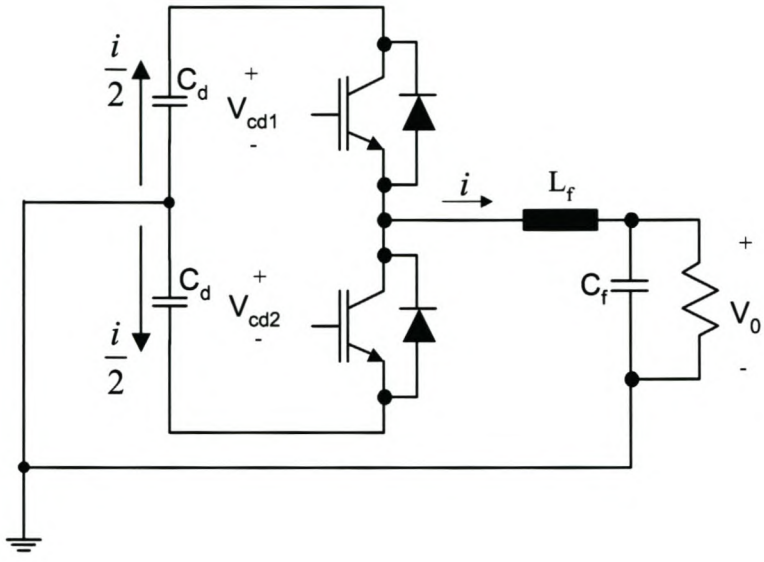

Figure 4.10: *Ripple current in the DC-bus capacitors of a half-bridge inverter.*

a 1000 V rated 2.5 μF high frequency polypropylene flying capacitors from FACON industries were used.

4.4.2 DC bus capacitors and Bleeding resistors

- DC bus capacitors.
  The selection of the two DC bus capacitors shown in Figure 4.10 is determined mainly by the ripple current, cost and temperature withstanding capabilities. For this application, each of the DC bus capacitors has to have a voltage handling capability of 500 V and a ripple current capability of half the RMS current, i.e. 7.95 A. The high-frequency component of the ripple current is ignored in the calculation of the DC bus capacitance.

  The current flowing in the filter inductor is given by:

$$i = 22 \sin \omega t \tag{4.30}$$

  With 22 A the peak output current.

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The current flowing through the bottom capacitor is given by:

$$\frac{i}{2} = C_d \frac{dV_{dc2}}{dt} \tag{4.31}$$

Substituting Eq. 4.30 into Eq. 4.31 gives

$$\begin{aligned} dV_{dc2} &= \frac{11}{C_d} \sin \omega t \, dt \\ V_{dc2} &= \frac{-11}{C_d \omega} \cos \omega t + \frac{V_d}{2} \end{aligned} \tag{4.32}$$

Where ω is the fundamental angular frequency equal to $2\pi 50$ rad/s.

Assuming a maximum voltage ripple of 2% on the DC-bus with a voltage of 1000 V. The expression of the maximum allowable voltage ripple on the DC-bus is given by:

$$\begin{aligned} v_{max} &= \frac{11}{C_d \omega} \\ &= 20V \end{aligned} \tag{4.33}$$

From Eq. 4.33 the DC-bus capacitance is determined to be

$$\begin{aligned} C_d &= \frac{11}{(314)(20)} \\ &= 1752 \ \mu\text{F} \end{aligned} \tag{4.34}$$

The capacitance value of each of the two DC bus capacitors has to be $1752 \ \mu$F. Due to unavailability of a $1752 \ \mu$F capacitor, the DC bus was made of a series connection two 500 V, $2200 \ \mu$F electrolytic capacitors in parallel with two $0.47 \mu F$ high frequency polypropylene capacitors. This polypropylene capacitors are used to enhance the high frequency handling capability of the DC bus. The selected capacitors's part numbers and characteristics are summarized in Table 4.5.

- Bleeding resistors.
  A bleeding resistor is a resistor that discharges a high voltage DC bus when an inverter is switched off, i.e with no load. Bleeding resistors fitted across the DC bus capacitors will ensure a quick automatic discharge of these capacitors immediately

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Capacitor	Type	Capacitance (μF)	Voltage rating (V)	Ripple current (A)
AYX-HR	Electrolytic	2200	500	7.6
MKP1.44/2	Polypropylene	0.47	1200	

Table 4.5: *DC bus capacitors specifications.*

after the supply is disconnected. By doing this the risk of electric shock to people who are unfamiliar with the properties of storage capacitors will be avoided. The design of these bleeding resistors is based on the desired time it will take the capacitors to be discharged. From the step response of an RC circuit the voltage across a discharging capacitor is given by

$$v(t) = V_0 e^{-t/RC} \tag{4.35}$$

To discharge a $2200\mu F$ DC bus capacitor with an initial voltage (V_0) of 500 V to a final voltage (v(t)) of 10 V using a 33 kΩ bleeding resistor will take

$$\begin{aligned} t &= -RC\ln(\frac{v(t)}{V_0}) \\ &= 284 \text{ s} \end{aligned} \tag{4.36}$$

With a bleeding resistor of 33 kΩ, the DC bus will take 284 seconds to discharge to 10 V.

The power rating of this resistor is equal to

$$\begin{aligned} P &= \frac{V^2}{R} \\ &= \frac{500^2}{(33000)} \\ &= 7.6 \text{ W} \end{aligned} \tag{4.37}$$

Therefore a 10 W, 33k bleeding resistor is connected across each DC capacitor.

4.4.3 Pre-charging of capacitors at start-up

A flying capacitor multilevel structure is built in such a way that the flying capacitors do not charge to their desired value until the inverter starts switching. In a case where

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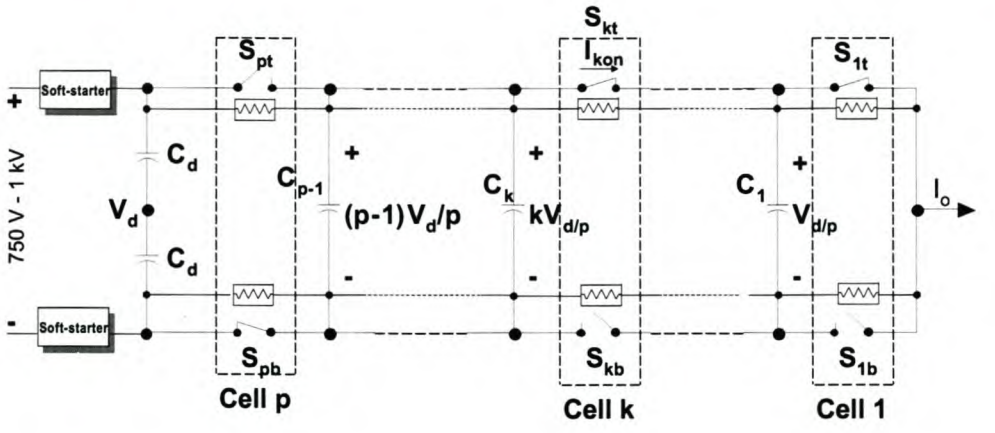

Figure 4.11: *General structure of FCMLI with pre-charging resistors.*

an auxiliary power supply is used, the inverter starts switching when the DC bus voltage has reached a certain desired level. This poses a serious threat to the switching devices of the commutation cell closest to the DC bus. To illustrate this, consider the following scenario: A three level FCMLI using 600 V switching devices and with an auxiliary power supply getting its start-up power from a 1000 V DC bus. For a four-level FCMLI with a DC bus of 1000 V, each commutation cell should be designed to sustain a voltage equal to $1000/3 = 333$ V. Since the rating of the selected switching devices is equal to 600 V, then the 333 V commutation cell voltage can be blocked successfully. Without pre-charging the flying capacitors at start-up, the voltage of the commutation cell nearest to the DC bus will be 1000 V. This voltage is higher than the voltage rating of the switching devices, hence a threat to the commutation cell. Figure 4.12 illustrates this.

This problem of pre-charging the DC capacitors at start-up is solved by connecting resistors across switching devices, as in Figure 4.13. The current limiting resistors in the soft-starters allow the DC capacitors to charge through the pre-charging resistors to their desired voltages. During this time the inverter is still switched off since the self-starting auxiliary power supply is still getting started.

By the time the self-starting auxiliary power supply switches the entire system "on" and also switches "on" the soft-starting switches, the DC capacitors will have reached their desired voltage and therefore the chance of device failure due to uneven voltage sharing

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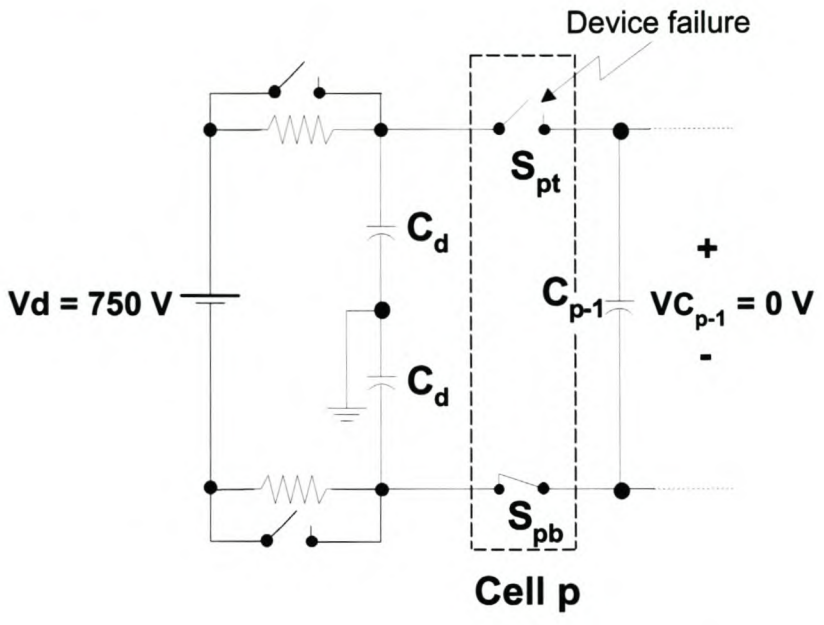

Figure 4.12: *The commutation cell closest to the DC bus at start-up.*

is minimized. The design of the pre-charging resistors of the FCMLI in Figure 4.13 was based on the time it will take the capacitors to fully charge before the auxiliary power supply turns the inverter "on". The charging time constants of the capacitors were calculated to determine the time it will take these capacitors to fully charge. Since the auxiliary power supply takes at most five seconds to start, the values of the pre-charging resistors should be designed in such a way that the two flying capacitors charge fully in less than five seconds. The pre-charging resistors have to be of the same value to avoid uneven voltage stresses on the devices. The design of the pre-charging resistors is as follows:

- Power rating and resistance value.
  Assuming that the voltage across the flying capacitor is initially at zero and choosing a 2 W pre-charging resistor, the resistance value is calculated to be

$$\begin{aligned} R &= \frac{V^2}{P} \\ &= \frac{(750-0)^2}{2} \\ &= 281 \text{ k}\Omega \end{aligned}$$

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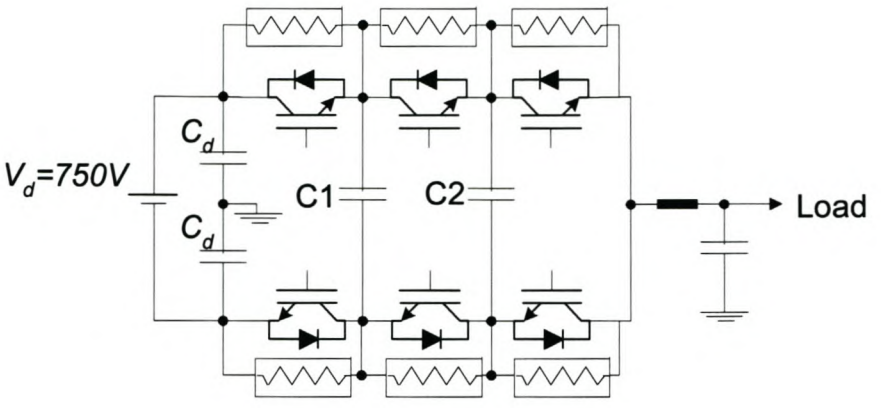

Figure 4.13: *A four-level FCMLI with pre-charging resistors.*

$$\approx 300\ \text{k}\Omega \tag{4.38}$$

Where V = the voltage across the pre-charging resistor.
750 V = the voltage of the DC bus when the inverter starts switching.
P = peak power rating of the resistor.
Due to unavailability of 281 k resistors, 300 k resistors were used instead.

- The charging time constant of the flying capacitors.
  The pre-charging circuit is designed in such a way that the flying capacitors are fully charged before the self-starting auxiliary power supply is switched on. The pre-charging circuit is shown in Figure 4.14.

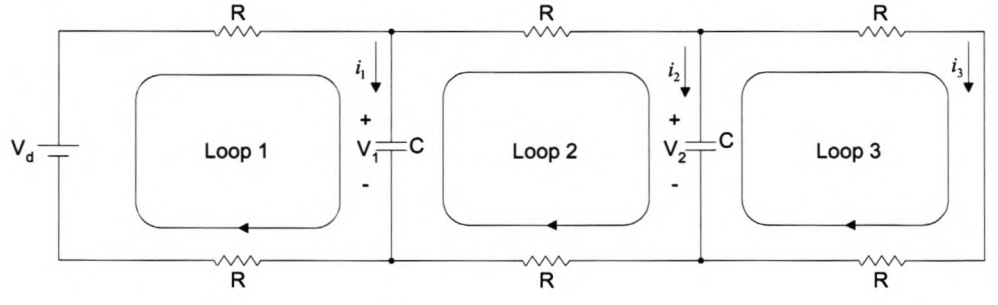

Figure 4.14: *The flying capacitors pre-charging circuit.*

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Using Kirchhoff's laws, the following equations can be derived from Figure 4.14:

$$V_d = 2R(i_1 + i_2 + i_3) + V_1 \tag{4.39}$$

$$V_1 = 2R(i_2 + i_3) + V_2 \tag{4.40}$$

$$V_2 = 2Ri_3 \tag{4.41}$$

With $i_1 = C\dot{V}_1$, $i_2 = C\dot{V}_2$ and $i_3 = \frac{V_2}{2R}$, the equations Eq. 4.39 and Eq. 4.40 can be rearranged and given by:

$$V_d = 2R(C\dot{V}_1 + C\dot{V}_2 + \frac{V_2}{2R}) + V_1 \tag{4.42}$$

$$V_1 = 2R(C\dot{V}_2 + \frac{V_2}{2R}) + V_2 \tag{4.43}$$

Where $\dot{V}_1$ and $\dot{V}_2$ are equal to $\frac{dV_1}{dt}$ and $\frac{dV_2}{dt}$ respectively.
Eq. 4.42 and Eq. 4.43 can be rewritten as differential equations:

$$\dot{V}_1 = \frac{1}{2RC}(V_d - V_1) - \frac{1}{2RC}(V_1 - V_2) - \frac{V_2}{2RC} \tag{4.44}$$

$$\dot{V}_2 = \frac{1}{2RC}(V_1 - 2V_2) \tag{4.45}$$

Using vector-matrix notation, the differential equations of Eq. 4.44 and Eq. 4.45 are given by:

$$\begin{bmatrix} \dot{V}_1 \\ \dot{V}_2 \end{bmatrix} = \begin{bmatrix} \frac{-1}{RC} & \frac{1}{2RC} \\ \frac{1}{2RC} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{2RC} \\ 0 \end{bmatrix} V_d \tag{4.46}$$

The standard form of Eq. 4.46 is:

$$\dot{V} = XV + YV_d \tag{4.47}$$

The eigenvalues of matrix X are given by the roots of the characteristic equation

$$[\lambda I - X] = 0 \tag{4.48}$$

Substituting matrix X in Eq. 4.48 gives:

$$\begin{bmatrix} (\lambda + \frac{1}{RC}) & (\frac{-1}{2RC}) \\ (\frac{-1}{2RC}) & (\lambda + \frac{1}{RC}) \end{bmatrix} = 0 \tag{4.49}$$

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Solving Eq. 4.49, the eigenvalue of matrix X is given by:

$$\begin{aligned}(\lambda + \frac{1}{RC})(\lambda + \frac{1}{RC}) - \left(\frac{1}{2RC}\right)^2 &= 0 \\ (\lambda + \frac{1}{RC})(\lambda + \frac{1}{RC}) &= \left(\frac{1}{2RC}\right)^2 \\ (\lambda + \frac{1}{RC}) &= \pm\frac{1}{2RC}\end{aligned} \tag{4.50}$$

From Eq. 4.50 λ has two solutions. The solutions are given by:

$$\lambda = \frac{-3}{2RC} \quad \text{or} \quad \lambda = \frac{-1}{2RC} \tag{4.51}$$

The time constants for charging the two flying capacitors are given by the reciprocal of λ. Using the pre-charging resistor value calculated in Eq. 4.38 and the 2.5 μF flying capacitor value, the time constant (τ) is given by:

$$\begin{aligned}\tau &= -\frac{1}{\lambda} \\ &= \frac{2RC}{3} \quad \text{or} \quad 2RC\end{aligned} \tag{4.52}$$

From Eq. 4.52, the time constants are calculated to be 1.5 s and/or 0.5 s. Since these time constants are less than the time it will take the auxiliary power supply to switch the inverter, the flying capacitors will be fully charged prior to the switching of the inverter.

4.4.4 Simulations of the flying capacitor voltages

This section presents simulations of the flying capacitor voltages with and without the precharging circuit. The simulations were performed with Simplorer simulation software. The simulation models are shown in Appendix A and the simulation parameters are given in Table 4.6. The first model was not fitted with the pre-charging circuit whereas the second model was.

Results obtained with these simulation models are shown in Figure 4.15 and Figure 4.16 respectively. From Figure 4.15 it can be seen that immediately after the inverter started switching, the voltage across the commutation cell closest to the DC bus is greater than

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the desired and expected commutation cell voltage of 333 V (under balanced conditions). This uneven voltage sharing across a switching device might cause failure of the inverter. Figure 4.15 shows that the precharging circuit employed solves the uneven voltage sharing. It can be seen that the inverter remains in the off mode until the flying capacitors are charged to their desired voltage levels. At no instant in time does the voltage of the commutation cell closest to the DC bus go beyond the expected 333 V (cell voltage).

Parameter	Symbol	Value	Unit
DC bus capacitance	C_d	2200	μF
DC bus voltage	V_d	1000	V DC
Output filter capacitor	C_f	1	μF
Output filter inductor	L_f	99	μH
Load resistance	R	15	Ω
Switching frequency	f_s	50	kHz
Pre-charging resistor	R_p	300	kΩ

Table 4.6: *Simulation parameters of the four-level multilevel inverter.*

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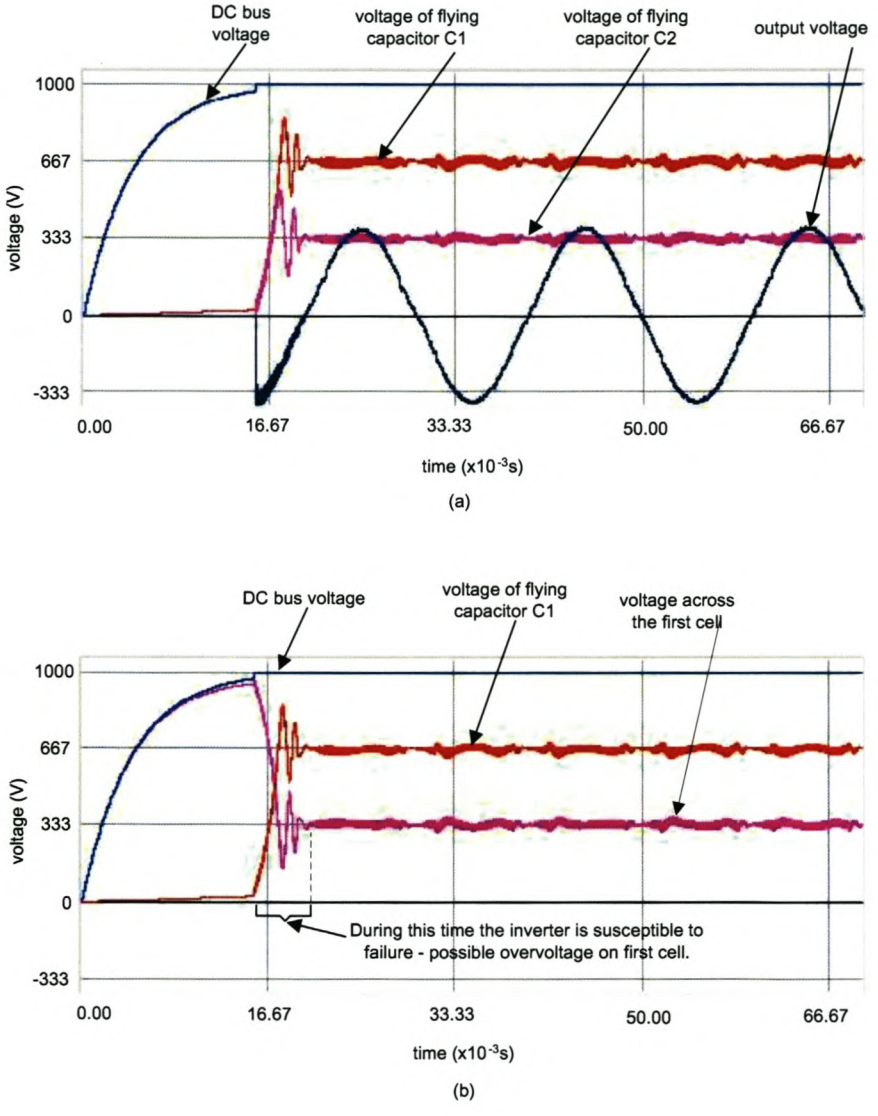

Figure 4.15: *Simulation results for a four-level FCMLI without a pre-charging circuit.*

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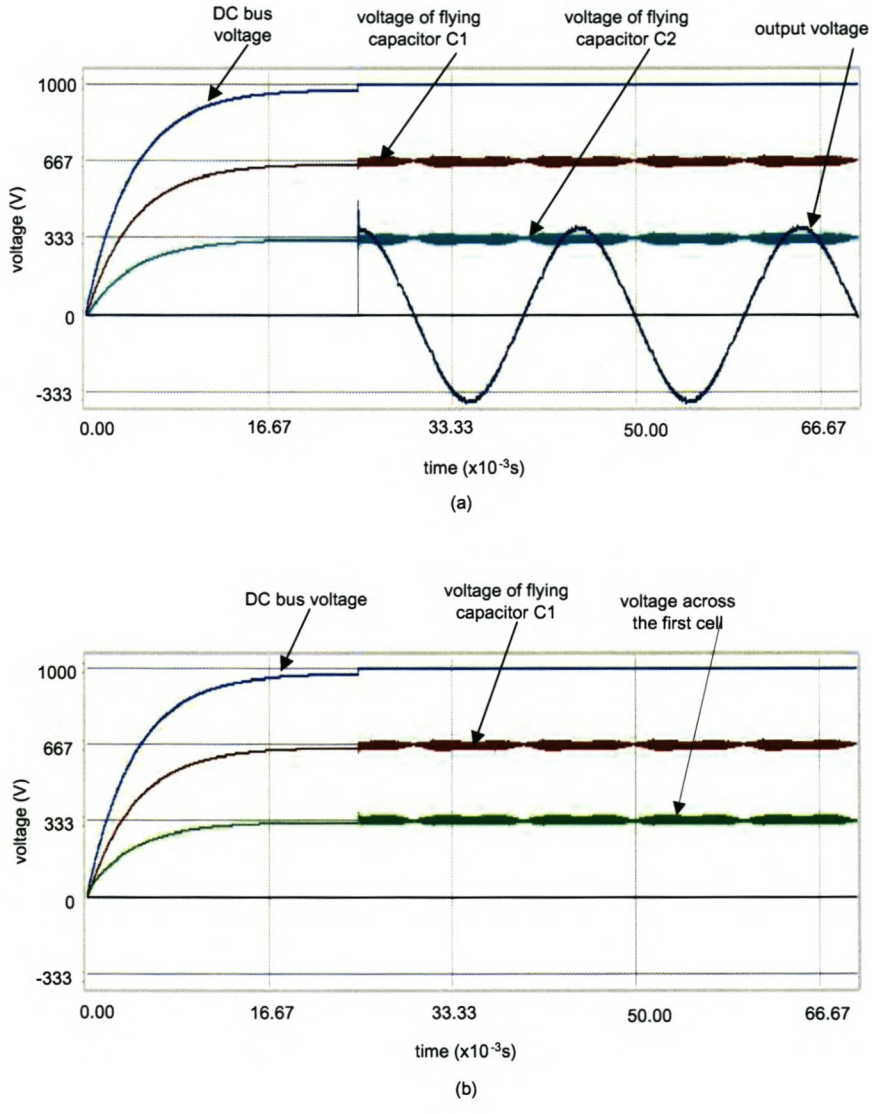

Figure 4.16: *Simulation results for a four-level FCMLI with a pre-charging circuit.*

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4.5 HEAT SINK DESIGN

For comparison, the heat sink design is done for each of the four different inverters. These inverters are:

- A four-level flying capacitor multilevel inverter (FCMLI) with 41 A, 600 V IGBT switching devices.
- A four-level FCMLI with 20 A, 650 V CoolMOS switching devices.
- An eight-level FCMLI with ordinary 200 V MOSFET switching devices.
- A standard 1200 V IGBT half-bridge inverter.

A thermal safety margin was not considered for the heat sink design, but this will be taken into account when choosing a heat sink for a specific inverter.

4.5.1 Introduction

Heat sinks are devices that enhance heat dissipation from a hot surface, usually the case of a heat generating device to a cooler ambient by increasing the surface area that is in direct contact with the coolant. To avoid switching device damage and to achieve long life and reliable performance the device's junction temperature should be effectively controlled within the limits set by the device design engineers.

The choice of a proper heat sink depends on the allowable junction temperature the device can tolerate. For a worst-case design (no thermal safety margin), the maximum junction temperature, the maximum ambient temperature and the maximum power dissipation of device are used. The maximum power dissipation is the sum of the switching power loss and conduction loss of device.

The design is for a case where all the switching devices of an inverter are mounted on the same heat sink. The heat sink is designed for an inverter with a sinusoidal output current of 16 A_{rms}, a switching frequency of 50 kHz and a worst case ambient temperature of $40°C$.

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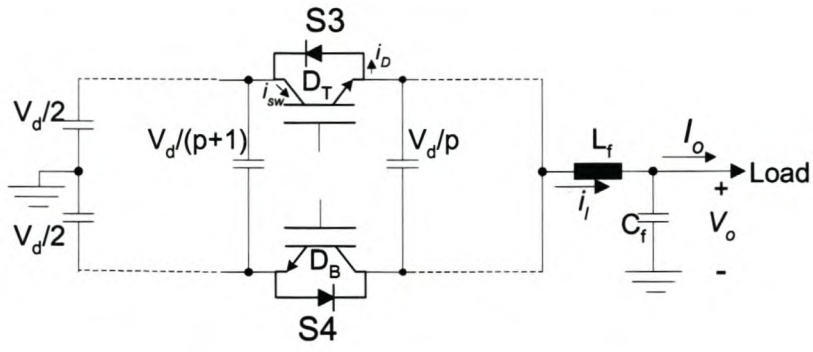

Figure 4.17: *A typical cell of a flying capacitor multilevel inverter.*

4.5.2 Conduction and switching power losses

Figure 4.17 is a circuit diagram of a typical cell of a multilevel inverter. The two switches are controlled in a complementary manner, so that only one switch can conduct at a time. The power losses are calculated based on what is happening in the top switch of the typical cell of Figure 4.17.

Conduction losses occur only when the switches are turned "on". The "on" time is determined by the duty cycle (D) of the switches, which is dependent on the modulation index (A) of the reference signal. The modulation index (A) of the reference signal is given by:

$$\begin{aligned} A &= \frac{2\hat{V}_0}{V_{d(min)}} \\ &= \frac{(2)(325)}{750} \\ &= 0.867 \end{aligned} \tag{4.53}$$

Where $\hat{V}_0$ is the peak output voltage and $V_{d(min)}$ is the minimum input voltage. The maximum duty cycle (D_T) of the top switch is given by:

Since the bottom switch is turned on when the carrier waveform is greater than the reference waveform, then from Figure 4.18, the duty cycle (D_B) of the bottom switch is given by:

$$\begin{aligned} D_B T_s &= \frac{T_s}{2}[1 - A\sin(wt)] \\ D_B &= \frac{1}{2}[1 - A\sin(wt)] \end{aligned} \tag{4.54}$$

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$ref_{(max)} = A\sin(\omega t) = 0.867$

$ref_{(min)} = A\sin(\omega t) = 0$

$(D_B T_s)_{(max)} = \frac{T_s}{2}$; when ref is minimum

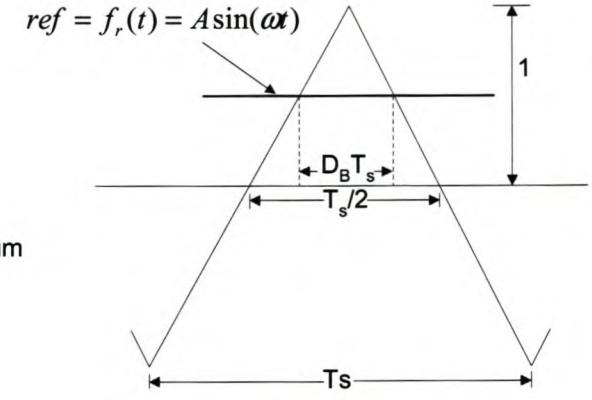

Figure 4.18: *The duty cycle of the bottom switch.*

The duty cycle (D_T) of the top switch is given by:

$$\begin{aligned} D_T &= 1 - D_B \\ D_T &= \frac{1}{2}(1 + A\sin(wt)) \end{aligned} \tag{4.55}$$

The power loss in a device is a function of the current flowing through it and the "on" voltage or the on-state resistance of the device, depending on whether the device is an IGBT or a MOSFET. Since the "on" voltage of the switch is given in the datasheet, only the current passing through the switch at an instant in time needs to be calculated. When the top switch is "on", the current flowing in it is the same as the current flowing in the inductor. This is illustrated in Figure 4.19.

Assuming unity power factor and ignoring the ripple current, the current in the filter inductor is given by:

$$i_l = Bsin(wt) \tag{4.56}$$

Where $w = 2\pi \times 50$

$B = I_0\sqrt{2} = 22.5\text{A}$

The conduction and switching losses of a device are solely dependent on the "on" voltage (for an IGBT), the on-state resistance (for a MOSFET) and the switching times of the device. These parameters are obtained from a device datasheet. For the switching devices of the four different inverters, these parameters are summarized in Table 4.7.

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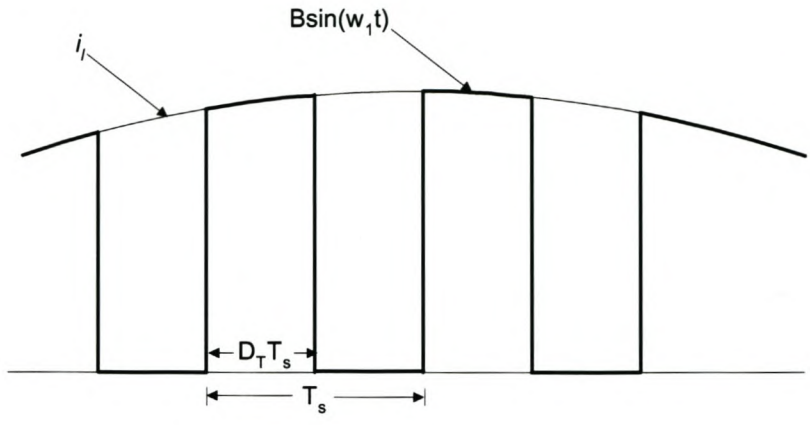

Figure 4.19: *The current through the top switch.*

Parameter	200 V MOSFET	650 V CoolMOS	600 V IGBT	1200 V IGBT
V_{on} (V)	-	-	2.5	2.4
R_t (Ω)	0.15	0.19	-	-
t_{on} (s)	52×10^{-9}	145×10^{-9}	78×10^{-9}	150×10^{-9}
t_{off} (s)	59×10^{-9}	160×10^{-9}	349×10^{-9}	600×10^{-9}
V_F (V)	1.5	1.2	1.65	3.2
$I_F = I_{RMS}$ (A)	15.9	15.9	15.9	15.9
I_{rr} (A)	5.55	19.7	5.5	14
t_{rr} (s)	251×10^{-9}	610×10^{-9}	400×10^{-9}	150×10^{-9}

Table 4.7: *Switching parameters of the four different switches.*

- The conduction losses in the switching devices.
  - Conduction losses in the 600 V S-IGBT.
    The conduction energy dissipated in the top IGBT device during one switching cycle, is given by:

$$\begin{aligned} E_{i(cond)} &= V_{on} \times D_T T_s \times (B \sin(wt_i)) \\ &= V_{on} \frac{1}{2}(1 + A \sin(wt_i))(B \sin(wt_i))T_s \end{aligned} \tag{4.57}$$

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The average conduction losses dissipated in a switch are given by:

$$\begin{aligned}
P_{cond} &= \frac{1}{T}\sum_{i=1}^{M} E_{i(cond)} \\
&= \frac{1}{T}\sum_{i=1}^{M} \frac{1}{2} V_{on}(1 + A\sin(wt_i))(B\sin(wt_i))T_s \\
&\approx \frac{1}{T}\int_0^{T/2} \frac{1}{2} V_{on}(1 + A\sin(wt))(B\sin(wt))\,dt \\
&= \frac{V_{on}}{2T}\int_0^{T/2} (B\sin(wt) + AB\sin^2(wt))\,dt \\
&= \frac{V_{on}}{2T}\left[\frac{-B}{w}\cos(wt) + AB(\frac{t}{2} - \frac{\sin 2(wt)}{4w})\right]_0^{T/2} \\
&= \frac{V_{on}}{2T}\left[\frac{2B}{w} + AB(\frac{T}{4})\right] \\
&= \frac{V_{on}}{2T}\left[\frac{2BT}{2\pi} + AB(\frac{T}{4})\right] \\
&= V_{on}\left[\frac{B}{2\pi} + \frac{AB}{8}\right] \qquad (4.58)
\end{aligned}$$

Where V_{on} is the switch's "on" voltage, $\left[\frac{B}{2\pi} + (\frac{AB}{8})\right]$ is the average current passing through the switch $(i_{ave(switch)})$ and M is the number of switching cycles in a fundamental cycle (T).

Using Eq. 4.58, the conduction losses in the S-IGBT are given by:

$$\begin{aligned}
P_{cond(S-IGBT)} &= V_{on}\left[\frac{B}{2\pi} + \frac{AB}{8}\right] \\
&= 2.5\left[\frac{22.5}{2\pi} + \frac{(0.867)(22.5)}{8}\right] \\
&= 15\ \text{W} \qquad (4.59)
\end{aligned}$$

– Conduction losses in the 650 V CoolMOS.

The average conduction losses dissipated in a CoolMOS or a MOSFET device over one fundamental cycle, are given by:

$$\begin{aligned}
P_{cond(CoolMOS)} &= R_t I_{RMS}^2 D \qquad (4.60) \\
&= (0.19)(15.9^2)0.5 \\
&= 24\ \text{W} \qquad (4.61)
\end{aligned}$$

Where R_t is the on-state resistance, D is the duty cycle and I_{RMS} is the RMS current flowing in the CoolMOS switch.

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- Conduction losses in the 200 V ordinary MOSFET.
  Using Eq. 4.61 we get

$$\begin{aligned} P_{cond(MOSFET)} &= R_t I_{RMS}^2 D \\ &= (0.15)(15.9^2)0.5 \\ &= 19 \text{ W} \end{aligned} \tag{4.62}$$

- Conduction losses in the 1200 V IGBT module.
  Using Eq. 4.58, the conduction losses in the IGBT module are given by:

$$\begin{aligned} P_{cond(module)} &= V_{on}\left[\frac{B}{2\pi} + \frac{AB}{8}\right] \\ &= 2.4\left[\frac{22.5}{2\pi} + \frac{(0.867)(22.5)}{8}\right] \\ &= 14.4 \text{ W} \end{aligned} \tag{4.63}$$

- Conduction losses in the antiparallel diodes of the IGBT.

- Conduction losses in the anti-parallel diode of the 600 V S-IGBT.
  For an IGBT, the average current flowing in the bottom diode ($i_{ave(diode)}$) is equal to the average current in the inductor $i_{ave(l)}$ minus the current flowing in the top switch ($i_{ave(switch)}$). The average current flowing through the diode over one fundamental cycle is therefore given by:

$$\begin{aligned} i_{ave(diode)} &= i_{ave(l)} - i_{ave(switch)} \\ &= \frac{1}{T}\int_0^{T/2} B\sin(wt)dt - i_{ave(switch)} \\ &= \frac{1}{T}\left[\frac{-B}{w}\cos(wt)\right]_0^{T/2} - i_{ave(switch)} \\ &= \frac{1}{T}\left[\frac{2B}{w}\right] - i_{ave(switch)} \\ &= \frac{B}{\pi} - \left[\frac{B}{2\pi} + \frac{AB}{8}\right] \\ &= \frac{B}{2\pi} - \frac{AB}{8} \end{aligned} \tag{4.64}$$

  The conduction losses dissipated in an antiparallel diode of an IGBT device over one fundamental cycle are given by:

$$P_{cond(IGBT-diode)} = V_{on} i_{ave(diode)}$$

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$$= V_{on}\left[\frac{B}{2\pi} - \frac{AB}{8}\right] \tag{4.65}$$

Using Eq. 4.65, the conduction losses of the antiparallel diode in the S-IGBT device are given by:

$$\begin{aligned} P_{cond(S-IGBT-diode)} &= V_{on}\left[\frac{B}{2\pi} - \frac{AB}{8}\right] \\ &= 1.65\left[\frac{22.5}{2\pi} - \frac{(0.867)(22.5)}{8}\right] \\ &= 1.88 \text{ W} \end{aligned} \tag{4.66}$$

– Conduction losses in the anti-parallel diode of the 1200 V IGBT module.
Using Eq. 4.65, the conduction losses of the antiparallel diode in the IGBT module are given by:

$$\begin{aligned} P_{cond(module-diode)} &= V_{on}\left[\frac{B}{2\pi} - \frac{AB}{8}\right] \\ &= 3.2\left[\frac{22.5}{2\pi} - \frac{(0.867)(22.5)}{8}\right] \\ &= 3.66 \text{ W} \end{aligned} \tag{4.67}$$

- The switching losses in the devices.
The average total **switching losses for the IGBT** ($P_{S(IGBT)}$) is a function of the current waveform, the switching frequency (f_s) and the turn "on" and turn off energies. The energy lost in a switch during a switching cycle is given by:

$$E_{i(switch)} = \frac{1}{2}V_{cell}(Bsin(w_1 t_i))(t_{on} + t_{off}) \tag{4.68}$$

The switching power loss in the switch over one fundamental period is approximated by:

$$\begin{aligned} P_{switching} &\approx \frac{1}{T}\sum_{i=1}^{M}\frac{1}{2}V_{cell}B\sin(wt_i)(t_{on} + t_{off}) \\ &= \frac{1}{2TT_s}V_{cell}B(t_{on} + t_{off})\sum_{i=1}^{M} sin(wt_i)T_s \\ &\approx \frac{1}{2TT_s}V_{cell}B(t_{on} + t_{off})\int_0^{T/2} sin(wt)dt \\ &= \frac{1}{2TT_s}V_{cell}B(t_{on} + t_{off})\left[\frac{-1}{w}cos(wt)\right]_0^{T/2} \end{aligned}$$

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$$
\begin{aligned}
&= \frac{1}{2TT_s} V_{cell} B(t_{on} + t_{off})[\frac{2}{w}] \\
&= \frac{1}{2\pi T_s} V_{cell} B(t_{on} + t_{off}) \\
&= \frac{f_s}{2\pi} V_{cell} B(t_{on} + t_{off}) \qquad (4.69)
\end{aligned}
$$

- Switching losses in the 600 V S-IGBT.
  Using Eq. 4.69 we get

$$
\begin{aligned}
P_{switching(S-IGBT)} &= \frac{f_s}{2\pi} V_{cell} B(t_{on} + t_{off}) \\
&= \frac{50000}{2\pi}(333)(22.5)(427 \times 10^{-9}) \\
&= 25.45 \text{ W} \qquad (4.70)
\end{aligned}
$$

- Switching losses in the 650 V CoolMOS.
  Using Eq. 4.69 we get

$$
\begin{aligned}
P_{switching(CoolMOS)} &= \frac{f_s}{2\pi} V_{cell} B(t_{on} + t_{off}) \\
&= \frac{50000}{2\pi}(333)(22.5)(305 \times 10^{-9}) \\
&= 18.2 \text{ W} \qquad (4.71)
\end{aligned}
$$

- Switching losses in the 200 V ordinary MOSFET.
  Using Eq. 4.69 we get

$$
\begin{aligned}
P_{switching(MOSFET)} &= \frac{f_s}{2\pi} V_{cell} B(t_{on} + t_{off}) \\
&= \frac{50000}{2\pi}(143)(22.5)(111 \times 10^{-9}) \\
&= 2.84 \text{ W} \qquad (4.72)
\end{aligned}
$$

- Switching losses in the 1200 V IGBT module.
  Using Eq. 4.69 we get

$$
\begin{aligned}
P_{switching(module)} &= \frac{f_s}{2\pi} V_{cell} B(t_{on} + t_{off}) \\
&= \frac{50000}{2\pi}(1000)(22.5)(750 \times 10^{-9}) \\
&= 134.3 \text{ W} \qquad (4.73)
\end{aligned}
$$

- Reverse recovery losses in the antiparallel diodes.
  A diode conducting a forward current (I_F) needs a small but significant amount of

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time to change from the on-state to the blocking state. This time is called the reverse recovery time of the diode. The turn-off energy of the diode during a switching cycle is given by [36]:

$$E_{rr} = I_{rr} V_{cell} D \frac{t_{rr}}{2} \tag{4.74}$$

Where I_{rr} is the reverse recovery current, t_{rr} is the reverse recovery time, V_{cell} is the voltage across the diode at recovery and D is the duty cycle.

The power loss over one fundamental cycle is given by [37]:

$$P_{rr} = 0.125 I_{rr} t_{rr} V_{cell} f_s \tag{4.75}$$

- Reverse recovery losses of the S-IGBT's antiparallel diode.
  Using Eq. 4.75, the reverse recovery losses in the antiparallel diode of the S-IGBT device are given by:

$$\begin{aligned} P_{rr(S-IGBT)} &= 0.125 I_{rr} t_{rr} V_{cell} f_s \\ &= 0.125(5.5)(400 \times 10^{-9})(333)(50000) \\ &= 4.6 \text{ W} \end{aligned} \tag{4.76}$$

- Reverse recovery losses of the CoolMOS's antiparallel diode.
  Using Eq. 4.75, the reverse recovery losses in the antiparallel diode of the CoolMOS device are given by:

$$\begin{aligned} P_{rr(CoolMOS)} &= 0.125 I_{rr} t_{rr} V_{cell} f_s \\ &= 0.125(5)(610 \times 10^{-9})(333)(50000) \\ &= 6.3 \text{ W} \end{aligned} \tag{4.77}$$

- Reverse recovery losses of the MOSFET's antiparallel diode.
  Using Eq. 4.75, the reverse recovery losses in the antiparallel diode of the MOSFET device are given by:

$$\begin{aligned} P_{rr(MOSFET)} &= 0.125 I_{rr} t_{rr} V_{cell} f_s \\ &= 0.125(5.55)(251 \times 10^{-9})(143)(50000) \\ &= 1.24 \text{ W} \end{aligned} \tag{4.78}$$

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Parameter	200 V MOSFET	650 V CoolMOS	600 V S-IGBT	1200 V IGBT
Switching losses (W)	2.84	18.2	25.45	134.3
Conduction losses (W)	19	24	15	14.4
Diode's reverse recovery losses (W)	1.24	6.3	4.6	6.56
Diode's conduction losses (W)	-	-	1.88	3.66
Total power loss per switch (W)	23.08	48.5	46.93	158.92
Total power loss per inverter (W)	161.56	145.5	140.79	158.92

Table 4.8: *Thermal parameters of the different switches.*

– Reverse recovery losses of IGBT module's antiparallel diode.
Using Eq. 4.75, the reverse recovery losses in the antiparallel diode of the IGBT module device are given by:

$$\begin{aligned} P_{rr(IGBT-module)} &= 0.125 I_{rr} t_{rr} V_d f_s \\ &= 0.125(7)(150 \times 10^{-9})(1000)(50000) \\ &= 6.56 \text{ W} \end{aligned} \tag{4.79}$$

The total power loss per device and per inverter are summarized in Table 4.8.

4.5.3 Heat sink value calculation

Transmission of heat from a heat generating source (e.g. a junction of a switching device) via the heatsink to the ambient takes place in three successive steps, these being:

- transfer from the heat source to the casing surface of the switching device.
- transfer from the casing surface to the heatsink surface.

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- transfer from the heatsink to the surrounding medium by either free or forced convection.

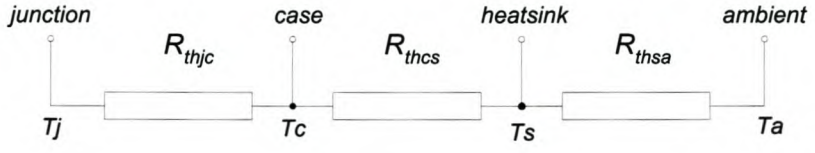

Figure 4.20: *Thermal equivalent circuit of a circuit.*

Thermal resistances of the switching devices considered for the heat sink design are shown in Table 4.9 as per device datasheets. Thermal resistance is defined as the degree of a temperature increase resulting from a power input and is used as a measure of determining and comparing the heat transfer capacity of heat sinks.

Parameter	Symbol &units	200 V MOSFET	650 V CoolMOS	600 V S-IGBT	1200 V IGBT
Junction to case thermal resistance for the switch	R_{thjcI} $(°C/W)$	1	0.6	0.5	0.39
Junction to case thermal resistance for the diode	R_{thjcD} $(°C/W)$	-	-	1	0.7
Case to sink thermal resistance (mounting pad)	R_{thcs} $(°C/W)$	0.4	0.4	0.4	0.035
Junction temperature	T_j $(°C)$	175	150	150	150

Table 4.9: *Thermal parameters of the different switches.*

- **IGBT inverter**
  The junction-to-case temperatures (T_{jc}) for the 600 V IGBT and its internal Emcon diode are calculated using the thermal-to-case thermal resistances (R_{thjcI}) or

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(R_{thjcD}) and the power loss of each component.

$$\begin{aligned} T_{jcI} &= R_{thjcI} \times [P_{cond(IGBT)} + P_{switching(IGBT)}] \\ &= 0.5 \times (15 + 25.45) \\ &= 20.22\ ^{\circ}C \\ T_{jcD} &= R_{thjcD} \times [P_{rr(IGBT)} + P_{cond(IGBT-diode)}] \\ &= 1 \times 6.48 \\ &= 6.48\ ^{\circ}C \end{aligned} \tag{4.80}$$

The maximum junction-to-case temperature is used in the design since it represents the worst-case condition. The maximum allowable case temperature (T_c) at the maximum allowable junction temperature (T_j) is therefore given by

$$\begin{aligned} T_c &= T_j - T_{jcmax} \\ &= 150 - 20.22 \\ &= 129.78\ ^{\circ}C \end{aligned} \tag{4.81}$$

The maximum allowable heat sink temperature (T_s) is given by

$$\begin{aligned} T_s &= T_c - [R_{thcs}(\text{Total power loss per switch})] \\ &= 129.78 - [0.4(46.93)] \\ &= 111.0\ ^{\circ}C \end{aligned} \tag{4.82}$$

Heat sink selection is done based on the value of the sink-to-ambient thermal resistance (R_{thsa})of a particular heat sink. This value is calculated for a worst-case power loss of all the switching devices conducting during a switching period in an inverter. R_{thsa} is given by

$$\begin{aligned} R_{thsa} &= \frac{T_s - T_a}{(\text{Total power loss per inverter})} \\ &= \frac{111.0 - 40}{140.79} \\ &= 0.5\ \frac{^{\circ}C}{W} \end{aligned} \tag{4.83}$$

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A heat sink with R_{thsa} less or equal to $0.5\frac{^{\circ}C}{W}$ will be able to dissipate the power generated by the switching devices to the surrounding air effectively and with ease.

To allow for at least a 30 % thermal safety margin, a heat sink with R_{thsa} 30 % less than the designed $0.5\frac{^{\circ}C}{W}$ should be used. A Semikron P150/170 naturally cooled heat sink with a sink-to-ambient thermal resistance of $0.2\frac{^{\circ}C}{W}$ was chosen. This choice of heat sink gives a thermal safety margin of approximately 60 %. The heat sink calculation of the four-level FCMLI CoolMOS inverter, ordinary eight-level FCMLI MOSFET inverter and half-bridge IGBT inverter are outlined below. These are done for comparison purposes only.

- **CoolMOS inverter**

  The junction-to-case temperature (T_{jc}) for the 650 V CoolMOS is calculated using the thermal-to-case thermal resistances (R_{thjc}) and the average power loss for the switching device.

$$\begin{aligned} T_{jc} &= R_{thjc} \times [P_{cond(CoolMOS)} + P_{switching(CoolMOS)}] \\ &= 0.6 \times 42.2 \\ &= 25.32\ ^{\circ}C \end{aligned} \tag{4.84}$$

  The junction-to-case temperature is used to calculate the maximum allowable case temperature (T_{case}). T_c is given by the equation:

$$\begin{aligned} T_c &= T_j - T_{jcmax} \\ &= 150 - 25.32 \\ &= 124.7\ ^{\circ}C \end{aligned} \tag{4.85}$$

  The maximum allowable heat sink temperature (T_s) is given by

$$\begin{aligned} T_s &= T_c - [R_{thcs}(\text{Total power loss per switch})] \\ &= 124.7 - [0.4(48.5)] \\ &= 105.3\ ^{\circ}C \end{aligned} \tag{4.86}$$

  The sink-to-ambient thermal resistance (R_{thsa}) determines the size and type of a heat sink to be used to prevent overheating of the switching devices of an inverter.

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R_{thsa} for this inverter is given by:

$$\begin{aligned} R_{thsa} &= \frac{T_s - T_a}{[\text{Total power loss per inverter}]} \\ &= \frac{105.3 - 40}{145.5} \\ &= 0.42 \ \frac{^\circ C}{W} \end{aligned} \tag{4.87}$$

- **MOSFET inverter**

  The junction-to-case temperature (T_{jc}) for the 200 V MOSFET is calculated using the thermal-to-case thermal resistance R_{thjc} and the switch's power loss.

$$\begin{aligned} T_{jc} &= R_{thjc} \times [P_{cond(MOSFET)} + P_{switching(MOSFET)}] \\ &= 0.5 \times 21.84 \\ &= 10.92 \ ^\circ C \end{aligned} \tag{4.88}$$

  The maximum allowable case temperature (T_{case}) at the maximum allowable junction temperature (T_j) is therefore given by the equation:

$$\begin{aligned} T_c &= T_j - T_{jcmax} \\ &= 175 - 10.92 \\ &= 164.08 \ ^\circ C \end{aligned} \tag{4.89}$$

  The maximum allowable heat sink temperature (T_s) is given by

$$\begin{aligned} T_s &= T_c - [R_{thcs}(\text{Total power loss per switch})] \\ &= 164.08 - [0.4(23.08)] \\ &= 154.85 \ ^\circ C \end{aligned} \tag{4.90}$$

  The sink-to-ambient thermal resistance (R_{thsa}) for a heat sink that would enhance the dissipation of the total power generated by the seven switches of the eight-level FCMLI is given by the equation:

$$\begin{aligned} R_{thsa} &= \frac{T_s - T_a}{[\text{Total power loss per inverter}]} \\ &= \frac{154.85 - 40}{161.56} \\ &= 0.71 \ \frac{^\circ C}{W} \end{aligned} \tag{4.91}$$

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- **IGBT half-bridge inverter**

The junction-to-case temperatures (T_{jc}) for the 600 V IGBT and its internal freewheeling diode are calculated using their respective thermal-to-case thermal resistances and the power loss in each one of them.

$$\begin{aligned} T_{jcI} &= R_{thjcI} \times [P_{cond(module)} + P_{switching(module)}] \\ &= 0.39 \times 148.7 \\ &= 57.99\ ^{\circ}C \\ T_{jcD} &= R_{thjcD} \times [P_{rr(module)} + P_{cond(module-diode)}] \\ &= 0.7 \times 10.22 \\ &= 7.15\ ^{\circ}C \end{aligned} \tag{4.92}$$

Only the maximum junction-to-case temperature is used, because it represents the worst-case scenario. The maximum allowable case temperature (T_{case}) at the maximum allowable junction temperature (T_j) is therefore given by:

$$\begin{aligned} T_c &= T_j - T_{jcmax} \\ &= 150 - 57.99 \\ &= 92.01\ ^{\circ}C \end{aligned} \tag{4.93}$$

The maximum allowable heat sink temperature (T_s) is given by

$$\begin{aligned} T_s &= T_c - [R_{thcs}(\text{Total power loss per switch})] \\ &= 92.01 - [0.035(158.92)] \\ &= 86.45\ ^{\circ}C \end{aligned} \tag{4.94}$$

The sink to ambient thermal resistance for a suitable heat sink to prevent the IGBT module from overheating is calculated as follows:

$$\begin{aligned} R_{thsa} &= \frac{T_s - T_a}{[\text{Total power loss per inverter}]} \\ &= \frac{86.45 - 40}{158.92} \\ &= 0.29\ \frac{^{\circ}C}{W} \end{aligned} \tag{4.95}$$

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	200 V MOSFET inverter	650 V CoolMOS inverter	600 V IGBT inverter	1200 V IGBT Half bridge
R_{thsa} $(°C/W)$	0.71	0.42	0.5	0.29

Table 4.10: *Sink to ambient thermal resistances of the designed heat sinks.*

The sink to ambient thermal resistance of the heat sinks for the four different inverters are summarized in Table 4.10. These R_{thsa} values are for a 0 % thermal safety margin. The R_{thsa} of each inverter should be reduced by at least 30 % to allow for a 30 % thermal safety margin.

4.6 SUMMARY

The development and design of a low cost gate drive circuit for multilevel inverters was investigated. Because of the requirement of isolated power supplies for all the gate drive circuits, it was found that the success towards the design of a low cost gate drive circuit rested solely on the success of designing a low cost isolated power supply. A cost-effective design of the gate drive circuit was accomplished by the development of a new bootstrap power supply for multilevel inverters.
The inverter's output filter, heat sink and DC capacitors were successfully designed. The pre-charging mechanism of the flying capacitors was presented and explained.

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CHAPTER 5

CONTROLLER DESIGN

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5.1 INTRODUCTION

This chapter focuses on the design and development of an FPGA-based digital controller, to operate the soft-starting switches and to control the switching devices of the flying capacitor multilevel inverter. An overcurrent protection method and an output voltage regulation method are also discussed in this chapter.

5.2 CONTROL STRATEGY

An FPGA-based PWM controller was designed and developed for implementing the control algorithms for the four-level flying capacitor multilevel inverter. MaxplusII programming software and an IEEE standard VHDL programming language was used to generate the control algorithms. The algorithms are given in detail in Appendix B. A digital control method was chosen because of its simplicity in implementing interleaved switching. Due to the large memory requirement of the control algorithms, an FPGA-based controller was chosen over a DSP-based. Figure 5.1 shows the picture of the developed controller board.

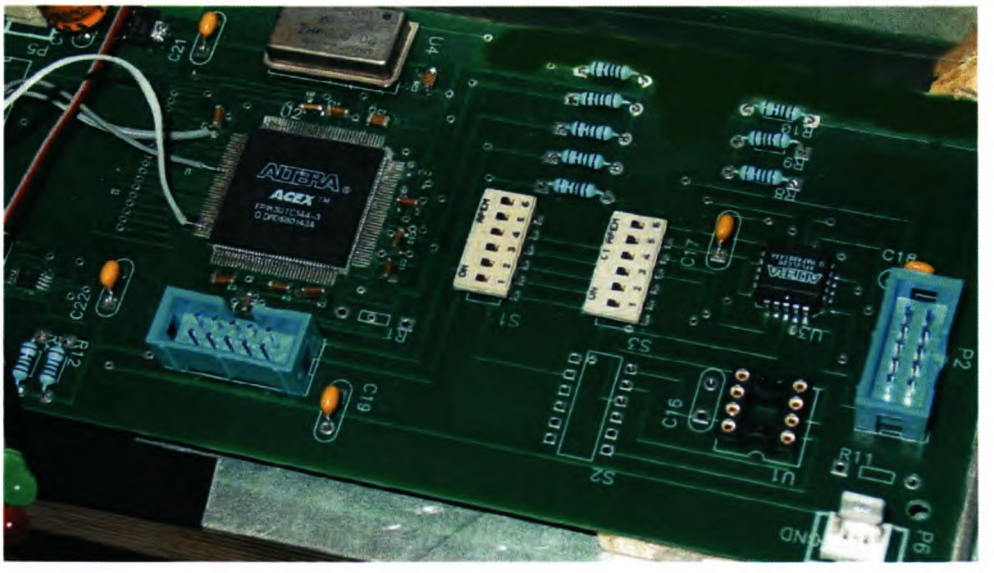

Figure 5.1: *A picture of the FPGA-based controller board.*

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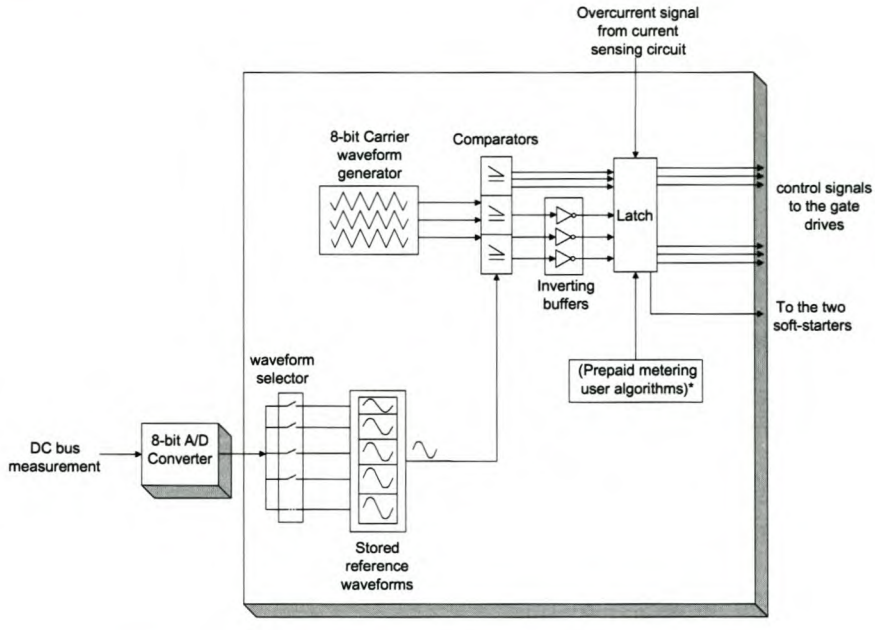

Figure 5.2: *Functional block diagram of the controller.*

The controller is comprised mainly of an FPGA (EP1K50TC144-3) and an 8-bit analog-to-digital converter (TLP548IP). A functional block diagram of this controller is shown in Figure 5.2.

The FPGA generates interleaved gating signals for the inverter by comparing three phase-shifted triangular carrier waveforms, generated internally, with a reference sine waveform stored inside the FPGA. At most four reference sine waveforms with different modulation indexes are stored in the FPGA. The FPGA also operates the two soft-starting switches and helps with over-current protection by using an external current sensing circuit.

A simple feed-forward control algorithm for regulating the output voltage is also implemented inside the FPGA. This voltage regulation method uses the FPGA in conjunction with the analog-to-digital converter to ensure that the output voltage remains within the specified range of 230 V $\pm 10\%$ for any given input voltage between 750 V and 1000 V.

In the final system, the controller may contain prepaid metering algorithms as well as the user interface algorithms. This will make the system more immune to by-passing and tampering, because of the ease to disconnect a load by latching off the gating signals whenever the prepaid power is all used up.

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Reference waveform	Modulation index	DC bus voltage range (V)	Output voltage range (V)
1	0.867	760 - 800	223 - 235
2	0.829	801 - 850	225 - 239
3	0.782	851 - 900	225 - 239
4	0.738	901 - 950	225 - 238

Table 5.1: *Output voltage regulation.*

5.3 VOLTAGE REGULATION

The analog-to-digital converter measures the input DC voltage and gives an 8-bit digital output signal. A voltage variation on the DC bus will induce a change on the digital output signal of the analog-to-digital converter. To keep the inverter's output voltage within the specified range, the FPGA will automatically select a reference waveform with a desired modulation index whenever this change is detected. The modulation indexes of the four reference waveforms are given in Table 5.1.
From Table 5.1, it is clear that for a DC bus input voltage of between 760 V to 950 V the output voltage will be bound between the specified range of 220 V and 240 V. The output voltages of Table 5.1 have been computed taking into account a ± 10 V drop across any three switching devices of the inverter.

5.3.1 Simulations of the feed-forward voltage regulation technique

A computer simulation of the feed-forward voltage regulation technique was conducted on the power stage of the four-level FCMLI. For this simulation, the DC bus voltage was varied between 750 V and 900 V. The simulation model was constructed as shown in Appendix A. The simulation model has two different reference waveforms, one with a modulation index of 0.867 and the other with a modulation index of 0.738. Simulation results obtained with this model without using the feed-forward voltage regulation technique, i.e. using only the reference waveform with a modulation index of 0.867, are shown in Figure 5.3. A significant change in the output voltage can be clearly observed on Figure 5.3 when the DC bus voltage is changed from 750 V to 900 V.

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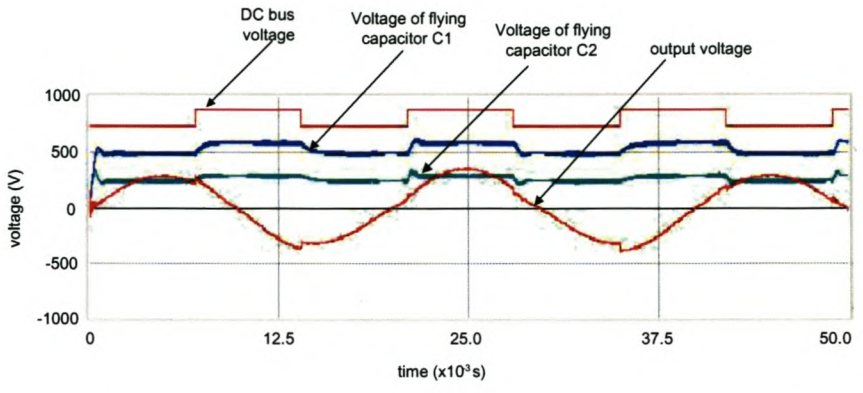

Figure 5.3: *Simulation results of the four-level FCMLI without the feed-forward output voltage regulation.*

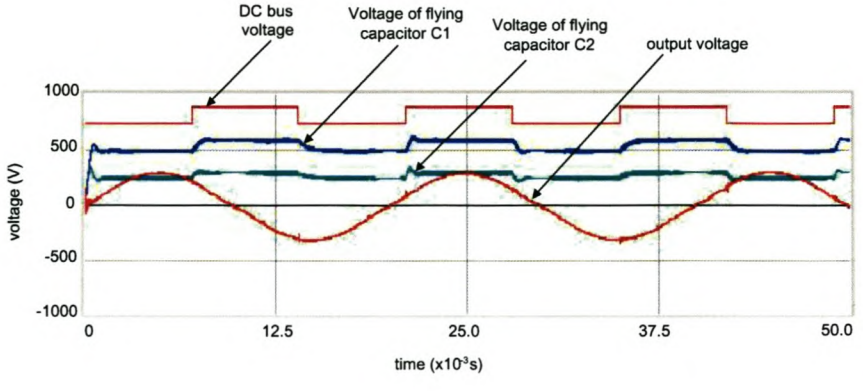

Figure 5.4: *Simulation results of a four-level FCMLI with the feed-forward output voltage regulation.*

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Simulation results obtained with the use of the feed-forward voltage regulation technique are shown in Figure 5.4. At first the reference waveform with a modulation index of 0.867 was used and the DC bus voltage was set at 750 V. After a while the DC bus voltage was increased from 750 V to 900 V. During the increment of the DC bus voltage, the reference waveform with a modulation index of 0.738 was automatically selected to counteract the effect caused by this increment on the output voltage.

5.4 OVER-CURRENT PROTECTION

The need to measure the flow of current in electronic systems is common. The fact that switching devices employed in electronic systems have specific current ratings, warrants the putting into place of measures to prevent failure of the devices due to over-current. Measuring a current means converting it into a voltage, which may then be compared with a reference signal in a comparator of a current sense circuit. There are several solutions for doing this, these being:

- **Using a current transformer**
  Using a sensing circuit that employs a current transformer as in Figure 5.5 is one alternative of measuring the output current. This method is often used in high power applications where electrical isolation is needed between the current to be measured and the control circuit. This method of using a current transformer was fully investigated for a low cost over-current protection circuit design. Due to the high price of the current transformer, this method cannot be successfully used for a low cost design.

- **Using a shunt current sense resistor**
  The availability of extremely low value current sense resistors combined with opto-isolated amplifiers presents a real alternative to using expensive sensors. This is important in high power applications where electrical isolation is essential. This method of current measurement with the use of a current sense resistor is illustrated in Figure 5.6. The employment of Ohm's law in this method makes it the simplest and the lowest cost method. The power loss in the resistor can be minimized by amplifying the voltage with an operational amplifier. The important factors in this case are the availability of sense resistors with values below 15 $m\Omega$, up to 5 W power rating with good surge withstand ability and low inductance.

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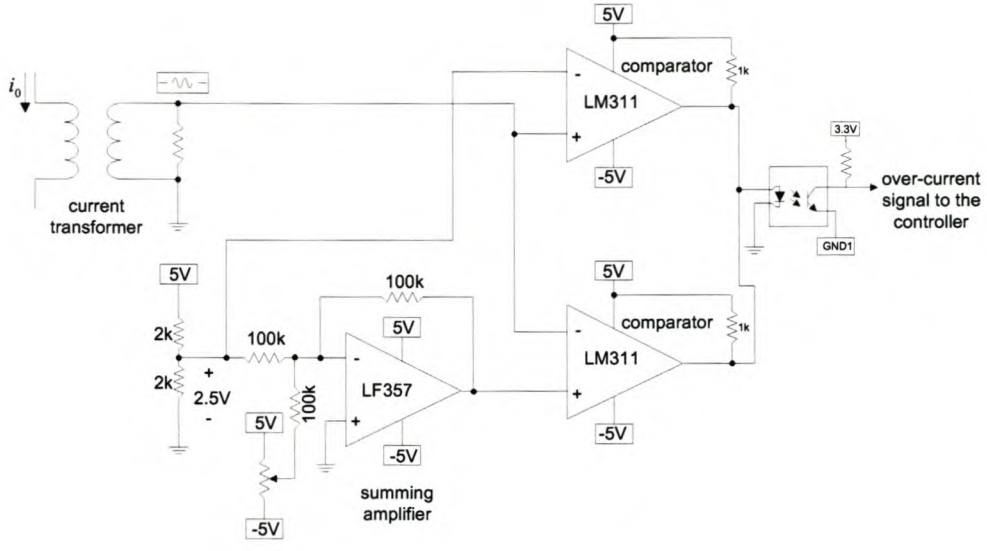

Figure 5.5: *Current measurement with a current transformer.*

In this application, the over-current protection circuit is designed to protect a switching device (in this case a 41 A rated IGBT) of a flying capacitor multilevel inverter, against an over-current. The circuit is designed in such a way that the inverter will go into over-current protection mode when the current flowing in the IGBT is equal to 40 A_{peak}.

During a fault condition, the current is allowed to increase to 40 A_{peak} before the inverter turns off. Using ohm's law (V=IR), the voltage seen across the current sense resistor when a 40 A_{peak} current flows through it is equal to 0.6 V. Since the voltage on the inverting terminal of the comparator should be more than 2.5 V during a fault current, the gain factor of the non-inverting amplifier is therefore set at 4.38. This will amplify the 0.6 V to 2.63 V. The comparator will compare the amplified 2.63 V signal with a 2.5 V reference signal and send out a fault signal that will latch off the gating signals in the controller. The gating signals will be latched off only if the amplified signal on the inverting terminal of the comparator is greater than the 2.5 V reference signal.

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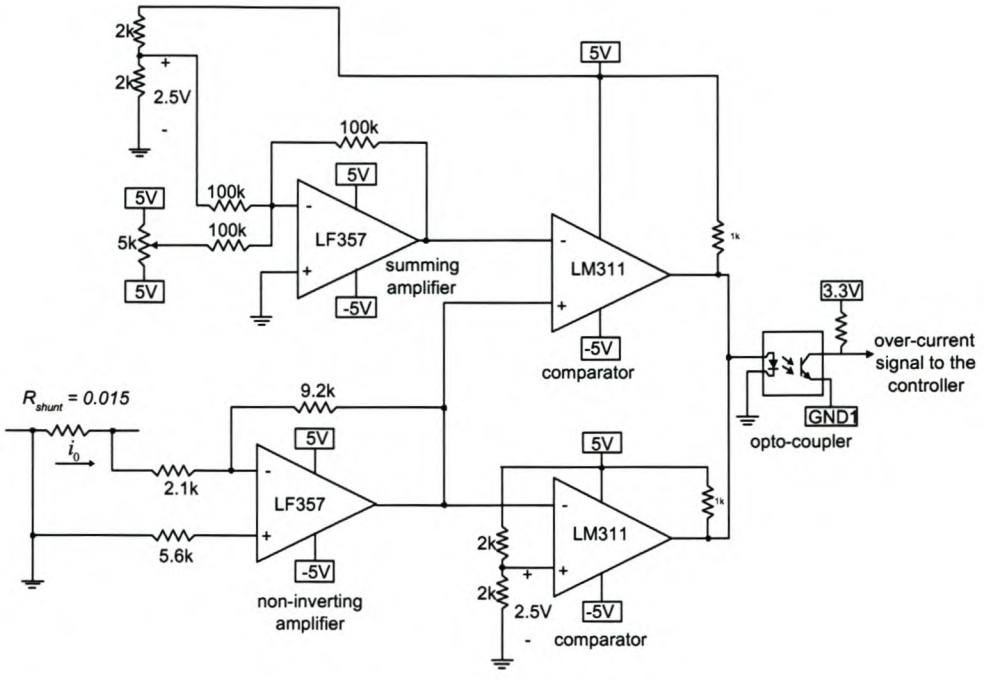

Figure 5.6: *Current measurement with a resistive shunt.*

5.5 SOFT STARTER

The two soft-starting switches used to limit inrush current into the DC bus capacitors are operated by this controller. This allows a degree of flexibility as to when to switch the soft-starting switches "on" and when to switch them off, depending on the value of the DC bus voltage. At start-up, the controller and the soft-starting switches are off, making it possible for the DC bus capacitors to charge through the current limiting resistors in parallel with the soft-starting switches. Once the DC bus capacitors are charged, the auxiliary power supply self-starts and provides power to the controller. The controller immediately turns "on" the soft-starting switches, thereby short-circuiting the current limiting resistor. The soft-starting switches remain "on" until there is a power outage or until the DC bus voltage drops to an unacceptable level.

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5.6 SUMMARY

A digital FPGA-based PWM controller was designed and developed successfully. The control algorithms of the four-level flying capacitor multilevel inverter were implemented in this controller. The operation of the two soft-starting switches was also discussed. A feed-forward voltage regulation method for regulating the output voltage of the flying capacitor multilevel inverter was presented and discussed in this chapter. With the aid of an external current sensing circuit, this controller is also used for protecting the switching devices against over-current. A series-shunt current sensing circuit for over-current protection was also designed and discussed.

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CHAPTER 6

AUXILIARY POWER SUPPLY

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Parameter	Value	Unit
Power rating	15	W
Input voltage	750 - 1000 V DC	V
Switching frequency	50	kHz
Regulated dc output voltages:		
Output 1	30	V
Output 2	30	V
Output 3	22	V
Output 4	22	V
Output 5	22	V
Output 6	7	V

Table 6.1: *Auxiliary power supply specifications.*

6.1 INTRODUCTION

A major problem facing DC to AC inverters is the power supply problem. Since these DC to AC inverters are exposed only to a high dc voltage, somehow this high dc voltage should be used to generate regulated dc power supplies for the electronic circuitry of these inverters. What is going to provide power to these electronic circuitry to turn "on" the inverter? The answer is an auxiliary self-powering power supply. This auxiliary power supply uses a bootstrap circuit, which is a method of direct powering from the input voltage, in this case dc voltage, for a short period of time. Bootstrap circuits can be passive and cheap, using only resistors and capacitors, or active with turn-off circuits to save power when the power supply is up and running.
The auxiliary power supply specifications are given in Table 6.1.

6.2 INPUT-SERIES-OUTPUT-PARALLEL TOPOLOGY

Figure 6.1 shows a block diagram of a self-starting auxiliary power supply that is based on the input-series-output-parallel (ISOP) inverter topology [19]. The main components shown in the block diagram are:

- An SG3525 pulse width modulator - used to generate pulse width modulated control signals for the switches of the two series stacked half-bridge inverters.

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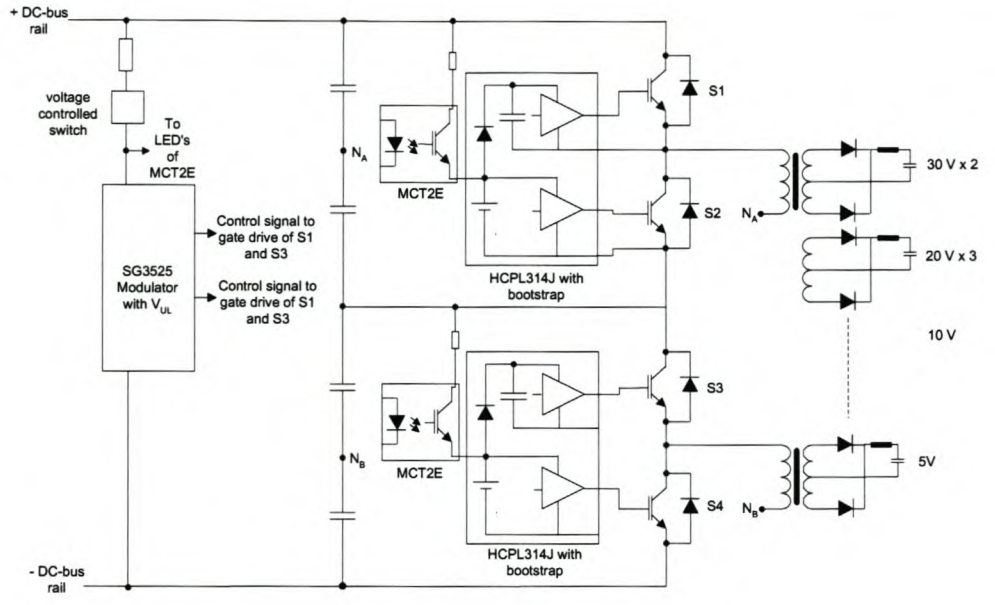

Figure 6.1: *Block diagram of a self-starting auxiliary power supply.*

- A voltage controlled switch - used to isolate the pulse width modulator from the bootstrap components, so that the modulator does not draw current before the bootstrap capacitor is fully charged.
- Two MCT2E opto-couplers - used to prevent the gate drive circuits from drawing current from the bootstrap components before they are fully charged.
- Two dual gate drive and opto-coupler IC's (HCPL314J) - these are gate drive circuits for the switching devices of the two stacked inverters and they also provide electrical isolation between the gate drive circuit and the pulse width modulator.
- Two small E-core transformers - provide electrical isolation between the multiple outputs of the ISOP inverter.

For this application the minimum input voltage of the auxiliary power supply is about 750 V. Due to the high input voltage, an insulated gate bipolar transistor should be used instead of a MOSFET in a conventional half-bridge topology. Most IGBT's have a switching frequency limited to around 30 kHz and they are not cost-effective. To increase the switching frequency for reduction of system size and cost, a MOSFET should

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be considered as a switching device. However, due to the high input voltage, a MOSFET cannot be used in a conventional bridge topology unless the device is series connected to sustain the high voltage.

The problems of the device series connection can be solved by the input-series-output parallel (ISOP)-connected inverter configuration discussed in the literature review under the switch mode power supply section. In this configuration the input voltage is divided by the series connected input capacitors and the outputs are paralleled. Each of the series stacked inverter experiences only half the input voltage so that a lower voltage-rating device, i.e. a MOSFET, can be used for higher switching frequency operation [19].

6.3 CONTROL METHOD

Since this topology consists of two series stacked identical half-bridge inverters that switches at the same time, a simple pulse-width modulation controller for a half-bridge inverter is required for this application. The controller and gate drive circuit is shown in Figure 6.2. The controller circuit consists of a saw-tooth generator, a reference voltage, an error amplifier and a comparator. The frequency of the saw-tooth is set by adjusting an external resistance of an RC circuit connected to a specific terminal of the SG3525 pulse width modulator. The control signals are generated by comparing the saw-tooth waveform and the reference waveform in the comparator.

The fact that the inverter should be able to self-start with a passive bootstrap power supply makes the selection of the control components, i.e. the pulse width modulator and the bootstrap components, an important aspect of this design. A passive bootstrap circuit requires a controller with a wide hysteresis band on its under-voltage lockout setting. This helps in minimizing the size of the bootstrap components and gives the inverter time to start properly before the bootstrapped supply voltage, Vcc, runs out of steam. For this application a pulse width modulator (SG3525) with an internal input under-voltage lockout, was used. For the gate drive circuit, two HCPL314J dual gate driver IC's from Agilent Technologies with built-in optocouplers were used. These gate drivers are suitable for bootstrap power supply applications since they have low power consumption.

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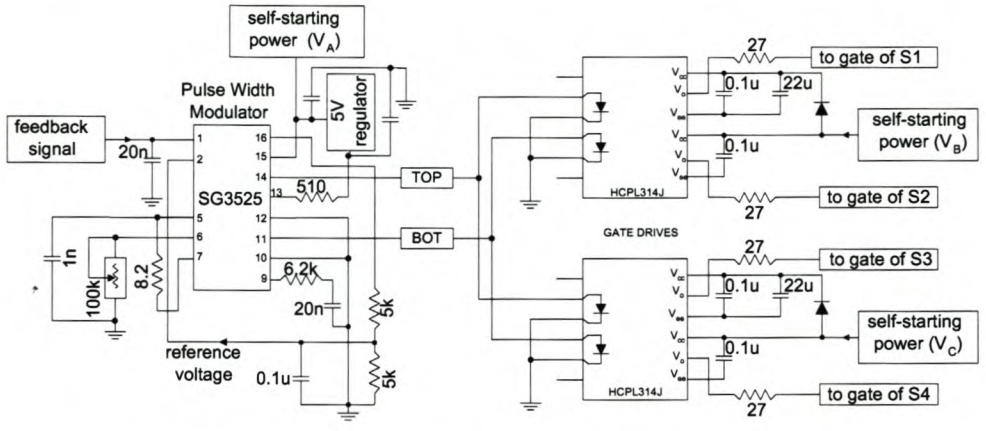

Figure 6.2: *Pulse width modulator and gate drives.*

6.3.1 Design of the gate drive circuit components

The design and selection of the gate resistor and the bootstrap components for the gate drive circuit of Figure 6.2 are as follows:

- Gate resistor.
  IGBTs and MOSFETs are both voltage-controlled devices. To turn on the device, a voltage must be applied between the gate and the source terminals.

  Using Figure 6.3 and the same method as the one illustrated in Section 4.2.3, the gate resistance is given by:

$$\begin{aligned} R_{g(min)} &= \frac{V_{gate} - 8}{I_{g(max)}} \\ &= \frac{15 - 8}{0.4} \\ &= 17.5\ \Omega \end{aligned} \tag{6.1}$$

  Where $I_{g(max)}$ is the maximum output current of the gate drive IC, V_{gate} is the applied gate to emitter voltage and 8 V is the voltage at which the gate capacitances become fully charged.

  The power dissipated in the gate resistor during turn on is given by:

$$P_{max(gate)} = I^2_{g(max)} R_{g(min)}$$

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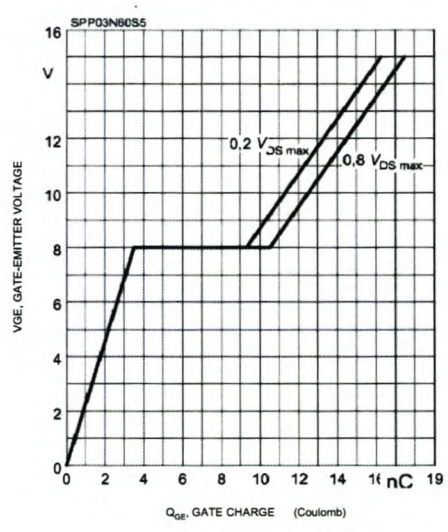

Figure 6.3: *Graph of a typical gate charge of the SPP03N60S5 CoolMOS [39].*

$$\begin{aligned} &= (0.4)^2(17.5) \\ &= 2.8 \text{ W} \end{aligned} \tag{6.2}$$

Since energy is defined as the power dissipated over a period of time, the energy consumed by the gate resistor at turn on is estimated by:

$$\begin{aligned} E_{max(gate)} &= P_{max(gate)} t_{on} \\ &= (2.8)(60 \times 10^{-9}) \\ &= 168 \text{ nJ} \end{aligned} \tag{6.3}$$

Where t_{on} is obtained from the datasheet and is the turn on time of the gate.

- Bootstrap capacitor.

  The bootstrap capacitor's selection is based on the fact that it should be able to provide enough turn-on energy to the gate of the switching device and the gate drive circuit without its voltage dropping too low. This is illustrated in Figure 6.4.

  The law of conservation of energy states that energy may neither be created or destroyed. Since the sum of all the energies in a system is constant, the energy consumed from the bootstrap capacitor of Figure 6.4 is given by:

$$\text{Energy consumed from the capacitor (C)} = (1/2)CV_1^2 - (1/2)CV_2^2 \tag{6.4}$$

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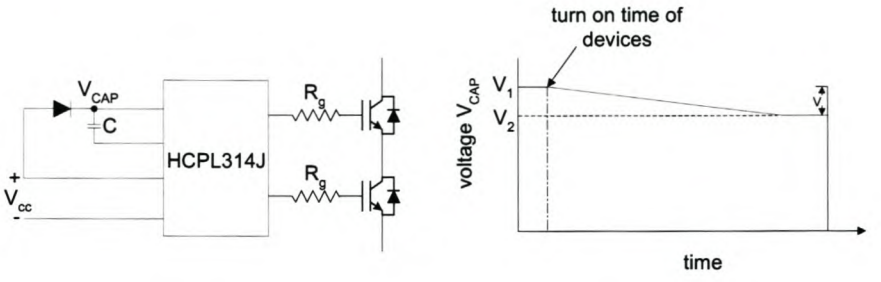

Figure 6.4: *Bootstrap capacitor voltage.*

The total energy consumed from the bootstrap capacitor during turn on, by the gate drive circuit is summarized in Table 6.2. The energy consumed by the gate drive IC is obtained from its datasheet and the energy consumed by the gate resistor is calculated in Eq. 6.3.

Energy consumed from the bootstrap capacitor	Symbol	Value	Units
Energy consumed by gate driver IC	E_{IC}	210×10^{-9}	J
Energy consumed by the gate resistor	E_{R_g}	168×10^{-9}	J
Total Energy	$E_{\text{drivecircuit}}$	378×10^{-9}	J

Table 6.2: *SPP03N60S5 parameters, obtained from its datasheet.*

Assuming V_1 and V_2 in Figure 6.4 to be equal to 15 V and 14.5 V respectively, the value of the bootstrap capacitor (C) is calculated using Eq. (6.4) to be:

$$\begin{aligned} C &= \frac{2(210 \times 10^{-9} + 168 \times 10^{-9})}{(15^2 - 14.5^2)} \\ &= 51 \text{ nF} \end{aligned} \tag{6.5}$$

- Bootstrap diode.
  The bootstrap components of the power supply of the gate drive circuit were carefully chosen. The bootstrap diodes have to be fast recovery diodes and should

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be able to withstand a maximum voltage of 500 V. The diodes used are BYV26E 1000 V ultrafast recovery diodes with a reverse recovery time of 75 ns.

6.4 TRANSFORMER DESIGN

Winding	Voltage (V)	Current (mA)	Purpose
1	30	100	power the gate drives of top switches of the FCMLI
2	30	100	power the gate drives of bottom switches of the FCMLI
3	22	100	assist the bootstrap power supply of the SG3525 modulator at start-up
4	22	100	assist the bootstrap power supply of the MCT2E at start-up
5	22	100	assist the bootstrap power supply of the MCT2E at start-up
6	7	100	power the controller of the FCMLI

Table 6.3: *Transformer's multiple outputs.*

The auxiliary power supply has to supply start-up power to the main inverter's gate drive and controller circuitry. It also has to provide power to boost the self-start bootstrap power supply mechanism so that eventually it will take over and run of its own generated power. Hence, the transformer has to have multiple outputs. The voltages of these multiple outputs are given in Table 6.3.

The design of the transformer is as follows:
Since the two half-bridge inverters are series stacked, at 1000 V (which is the maximum voltage the main inverter should be able to operate at) the primary voltage of the transformer is bound at -250 V and 250 V.
An E-core of type E/42/21/15 made of an N27 material was chosen for the design of the transformer. This choice was made because E-cores are suitable for inverter and switching power transformer applications and because N27 material E-cores are recommended

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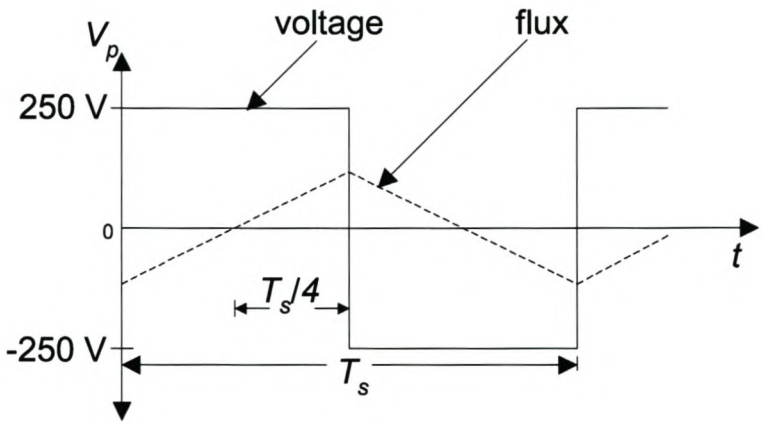

Figure 6.5: *Transformer primary voltage and flux waveforms.*

Parameter	Symbol	Value	Unit
Effective area of core	A_e	178	mm^2
Maximum magnetic flux density of core	$\hat{B}_m$	200	mT
Maximum magnetic flux	$\varphi = \hat{B}_m A_e$	35.6	μWb
Switching frequency	f_s	50	kHz
Maximum primary side voltage	V_p	250	V
Minimum input voltage	$V_d/2$	375	V

Table 6.4: *Transformer design parameters.*

for power applications in the frequency range of up to 100 kHz.

The design input parameters are given in Table 6.4.

Faraday's law is used in the design of the primary windings. Rearranging Faraday's law

$$V_p = N_1 \frac{d\varphi}{dt} \tag{6.6}$$

we get

$$N_1 = V_p \frac{\Delta t}{\Delta \varphi} \tag{6.7}$$

Since $\varphi = \hat{B}_m A_e$ then,

$$N_1 = V_p \frac{T_s}{4 A_e \Delta \hat{B}_m}$$

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$$= 35 \text{ turns} \tag{6.8}$$

The value 35 is the minimum number of primary turns that will make the transformer not to saturate. The primary number of turns on the transformers used is 52.

From Eq. 2.24 and Eq. 6.8 the secondary windings for the secondary voltages are:

- 30 V windings

$$\begin{aligned} N_2 &= \frac{(30 \text{ V})(52 \text{ turns})}{(375)(0.5)} \\ &= 8 \text{ turns} \end{aligned} \tag{6.9}$$

- 22 V windings

$$\begin{aligned} N_2 &= \frac{(22 \text{ V})(52 \text{ turns})}{(375)(0.5)} \\ &= 6 \text{ turns} \end{aligned} \tag{6.10}$$

- 7 V windings

$$\begin{aligned} N_2 &= \frac{(7 \text{ V})(52 \text{ turns})}{(375)(0.5)} \\ &= 2 \text{ turns} \end{aligned} \tag{6.11}$$

The thickness of the primary and secondary wires is a function of the current flowing through them, and is determined using the maximum current density of 6 A/mm^2. The cross-sectional area of the secondary wire (A_{sec}) is therefore given by:

$$A_{sec} = \frac{I_p}{6} \tag{6.12}$$

The diameter of the secondary wire is given by:

$$\begin{aligned} \text{Diameter} &= \sqrt{\frac{4A_{sec}}{\pi}} \\ &= \sqrt{\frac{4(\frac{I_p}{6})}{\pi}} \end{aligned} \tag{6.13}$$

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Using Eq. 6.13, the diameters of the 250 mA and 100 mA secondary wires are equal to 0.23 mm and 0.145 mm respectively. A wire of diameter 0.4 mm was used for all the secondary windings.

The primary current is given by the relation:

$$\frac{I_p}{I_s} = \frac{V_s}{V_p} = \frac{N_2}{N_1} D \tag{6.14}$$

The secondary currents induce a total current of about 39.4 mA into the primary winding. Therefore the cross-sectional area of the primary wire is given by:

$$\begin{aligned} A_{prim} &= \frac{39.4 \times 10^{-3}}{6} \\ &= 0.006 \text{ mm}^2 \end{aligned} \tag{6.15}$$

The thickness of each of the secondary wires is given by:

$$\begin{aligned} Diameter &= \sqrt{\frac{4A_{prim}}{\pi}} \\ &= 0.1 \text{ mm} \end{aligned} \tag{6.16}$$

The diameter of the primary wire is therefore equal to 0.1 mm, but a wire of diameter 0.4 mm was used in the design.

6.5 THERMAL DESIGN OF THE SWITCHING DEVICES

The voltage rating and current rating of the switching devices have to be more than half the DC bus voltage and more than the primary current of the transformer, respectively. The average current flowing in the primary side of the transformer is equal to 39.4 mA and half of the maximum DC bus voltage is equal to 500 V. A suitable and easily accessible switch for this application was found to be a SPP03N60S5 CoolMOS semiconductor. The voltage rating and current rating of this switch are 650 V and 3.2 A respectively. To ensure that the switching devices do not overheat, the power loss in these devices are calculated in order to select an appropriate heat sink. A proper thermal design will enhance the transfer rate of the dissipated power to the cooler surroundings of a heat generating device by conduction and convection. The parameters required to calculate the power losses are obtained from the device datasheet, and are summarized in Table 6.5. The maximum dissipated power in a switch is given by the sum of the switching power loss, the conduction loss and the reverse recovery losses in that switch. These are calculated as follows:

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- Conduction losses in the CoolMOS switch.
  Using Eq. 4.61, the conduction losses dissipated in a CoolMOS are given by:

$$\begin{aligned} P_{cond(CoolMOS)} &= \frac{R_t I_{RMS}^2}{2} \\ &= \frac{(1.4)(39.4 \times 10^{-3})^2}{2} \\ &= 1.1 \text{ mW} \end{aligned} \tag{6.17}$$

  Where R_t is the on-state resistance and I_{RMS} is the RMS current flowing in the CoolMOS switch.

- Switching losses in the CoolMOS switch.
  Using Eq. 4.69 we get

$$\begin{aligned} P_{switching(CoolMOS)} &= \frac{f_s}{2\pi} V_d B(t_{on} + t_{off}) \\ &= \frac{50000}{2\pi}(500)(39.4 \times 10^{-3})(115 \times 10^{-9}) \\ &= 18 \text{ mW} \end{aligned} \tag{6.18}$$

  Where B is the peak current flowing through the switch.

- Reverse recovery losses in the anti-parallel diode.
  Using Eq. 4.75, the reverse recovery losses in the anti-parallel diode are given by:

$$\begin{aligned} P_{rr(CoolMOS)} &= 0.125(I_{rr})(t_{rr})(V_{cell})(f_s) \\ &= 0.125(39.4 \times 10^{-3})(1700 \times 10^{-9})(500)(50000) \\ &= 210 \text{ mW} \end{aligned} \tag{6.19}$$

Parameter	Value	Units
On state resistance	1.4	Ω
turn on time	60	ns
turn off time	55	ns
Diode forward	1.2	V

Table 6.5: *Thermal parameters of the SPP03N60S5.*

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The sum of the total power loss dissipated in one of the four CoolMOS switching devices is equal to 0.25 W. The total power dissipated by the four devices of the auxiliary power supply is therefore equal to $0.25 \times 4 = 1$ W. The total power loss is negligibly small to warrant the use of a heat sink.

6.6 THE SELF-STARTING MECHANISM

This section discusses the mechanism behind the operation of the auxiliary self-starting power supply mentioned in Section 6.2. A bootstrap method is used to start-up this inverter from the DC bus voltage. The pulse-width modulator used has an undervoltage lockout setting on its supply voltage terminal. This feature prevents the modulator from turning on before the supply voltage is above or equal to V_{UL} (Under Voltage Lockout). The self-starting circuit of Figure 6.6 is comprised of two main parts. These are:

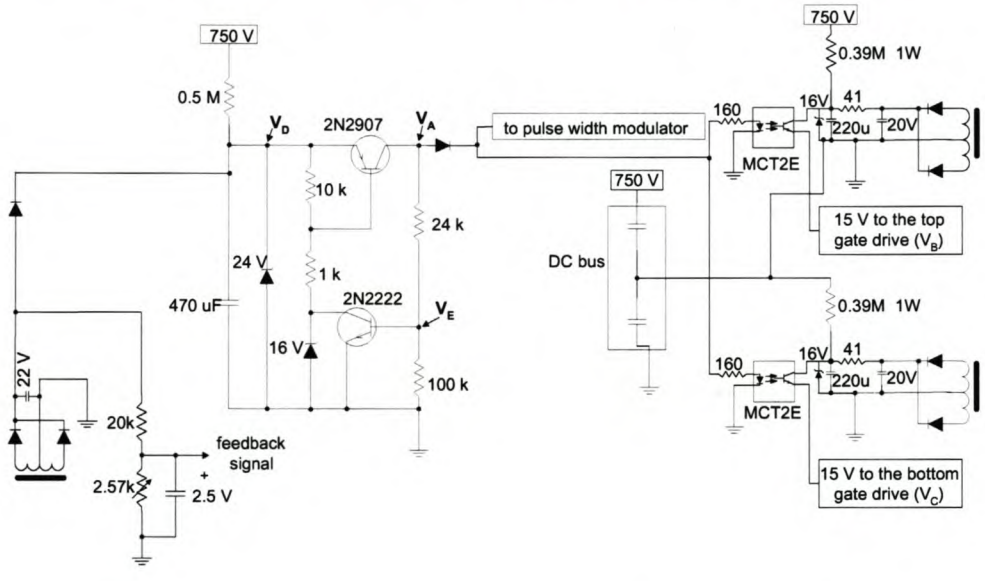

Figure 6.6: *A self-starting circuit for the auxiliary power supply.*

- A circuit to provide power to the pulse width modulator.
  This circuit is composed of a bootstrap power supply circuit and a voltage controlled switch. The voltage controlled switch consists mainly of a pnp transistor (2N2907), an npn transistor (2N2222) and a 16 V zener diode. Initially the two

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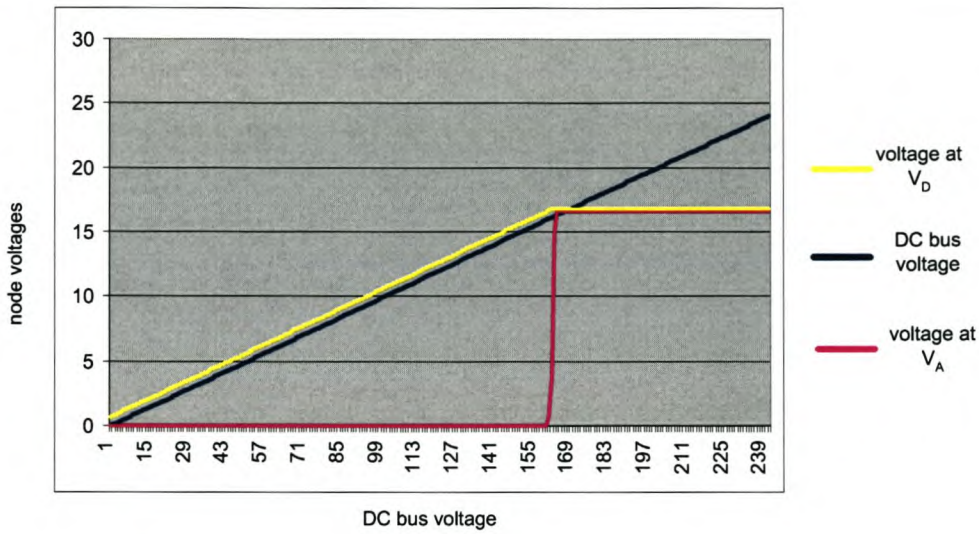

Figure 6.7: *Simulation results of the voltage controlled switch.*

transistors are off and the zener diode is blocking voltage V_D, therefore allowing V_D to rise to 16 V. With V_D equal to 16 V, the zener diode starts to conduct. During this time the collector to base voltage of the pnp transistor is greater than the threshold voltage of 0.7 V.

This turns the pnp transistor "on" and allows power to flow to the pulse width modulator. During this time, voltage V_E is pulled above the 0.7 V threshold voltage of the npn transistor. With V_E above 0.7 V the npn transistor turns "on" and pulls the base voltage of the pnp transistor to ground so that the pnp transistor (2N2907) remains "on". A PSPICE simulation result of this circuit is shown in Figure 6.7.

- A circuit to provide power to the gate drives.

  This circuit is composed of two opto-couplers and two bootstrap power supply circuits, for supplying power to the gate drive circuits of the top and bottom half-bridge inverters.

The basic operating principle of this circuit is as follows:
The two 220 μF capacitors charges slowly through the two 0.39 MΩ resistors. Due to the clamping 16 V zener diodes the voltage of these capacitors can only reach a maximum

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of 16 V. Since the two MCT2E opto-couplers are off the voltage of the 220 μF capacitors will remain at 16 V until the opto-couplers are switched "on".

The 470 μF capacitor slowly charges through the 0.5 MΩ resistor. This capacitor can only charge to a maximum of 16 V, because of the 16 V clamping zener diode. During this charging time the voltage controlled switch is off. Once the voltage across the 470 μF reaches 16 V, the voltage controlled switch is automatically turned "on" to provide start-up power to the pulse width modulator and also to provide a high impedance signal to the photodiodes of the MCT2E opto-couplers. This high impedance signal switches "on" the transistors of the MCT2E and therefore allowing power to flow to the gate drives.

After the circuit has started switching, special windings on the transformer provides power to the critical components of the self-starting circuit to make the power supply self-sufficient.

It is vital for the two 220 μF capacitors to charge to 16 V faster than the 470 μF capacitor, since the voltages of the two 220 μF capacitors have to be at 16 V potential when the voltage controlled switch turns "on". This is illustrated in Figure 6.8. The Figure 6.8 is obtained with a Matlab program of Appendix B and it shows only the linear part of the exponential capacitor voltage waveforms.

The 220 μF and 470 μF capacitor values were randomly selected and their charging times chosen to be approximately 3 and 5 seconds respectively for a minimum DC bus voltage of 750 V. The resistor values are designed to fulfil the timing requirement. Knowing the capacitor values and their desired charging times, the resistor values can be calculated using the equation of an RC step response circuit. The equation of an RC step response circuit is given by [34]:

$$v(t) = V_s(1 - e^{-t/RC}) \tag{6.20}$$

The resistor values are calculated to be:

- A charging resistor for the $220\mu F$ with $V_s = 375V$.
  From Equation (6.20) we have:

$$R = \frac{-t}{C\left(\ln\left(\frac{V_s - v(t)}{V_s}\right)\right)}$$

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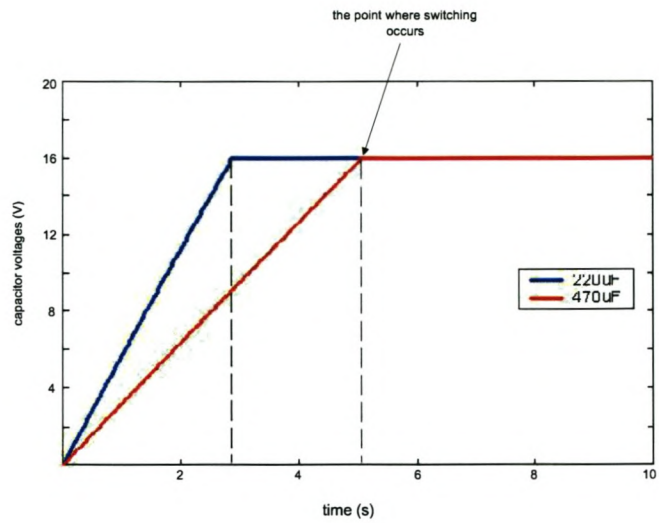

Figure 6.8: *The graph of the capacitor voltages.*

$$\approx 0.3 \text{ M}\Omega \tag{6.21}$$

Where: $t = 3$ s.
$C = 220\ \mu F$.
$V_s = 375$ V.
$v(t) = 16$ V.

- A charging resistor for the $470\mu F$ with $V_s = 750V$.

$$\begin{aligned} R &= \frac{-t}{C\left(\ln\left(\frac{V_s - v(t)}{V_s}\right)\right)} \\ &\approx 0.5 \text{ M}\Omega \end{aligned} \tag{6.22}$$

Where: $t = 5$ s.
$C = 470\ \mu F$.
$V_s = 750$ V.
$v(t) = 16$ V.

6.7 SUMMARY

To address the power supply problem facing DC to AC inverters, a self-powering auxiliary power supply based on the input-series-output-parallel topology was introduced.

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The bootstrap components of this self-starting circuit were designed and the principle of operation of the self-starting circuit discussed. The pulse width modulation control method of this auxiliary power supply was discussed. A multiple output transformer for supplying electrically isolated dc power supplies to the four-level FCMLI was designed successfully. A thermal design for the switching devices of the auxiliary power supply was done but the power loss in the devices was negligibly small to warrant the use of a heat sink.

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CHAPTER 7

CONVERTER ANALYSIS & SELECTION

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7.1 INTRODUCTION

This chapter focuses on the cost analysis of the different inverters under investigation for a low cost inverter design. These inverters are:

- A Four-level flying capacitor multilevel inverter (FCMLI) with 41 A, 600 V IGBT switching devices.
- A Four-level FCMLI with 20 A, 650 V CoolMOS switching devices.
- An Eight-level FCMLI with ordinary 200 V MOSFET switching devices.
- A standard 1200 V IGBT half-bridge inverter.

A brief analysis of the switching devices is also presented. This analysis will help to establish as to which device and inverter has robust and cost-effective properties desired for this design.

7.2 COST ANALYSIS

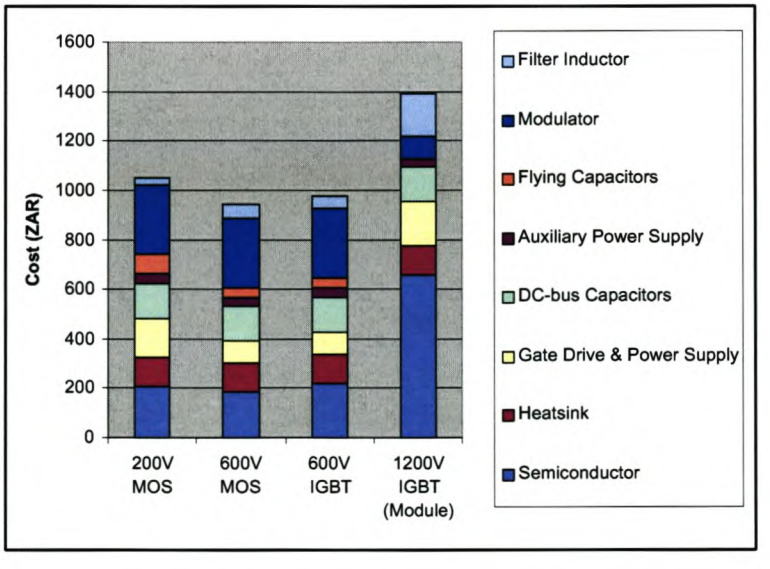

Figure 7.1: *Graph of components cost.*

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	200 V MOSFET inverter	650 V CoolMOS inverter	600 V IGBT inverter	1200 V IGBT Half bridge
Filter inductor value (μH)	18	99	99	893
Total power losses per inverter (W)	161.56	145.5	140.79	158.92
Efficiency (%)	95.4	95.8	96.0	95.4
R_{thsa} ($°C/W$)	0.71	0.42	0.5	0.29
Switch Price (R)	17	35	42	750
Price of switches per inverter (R)	17×14 $= 238$	35×6 $= 210$	42×6 $= 252$	750×1 $=750$

Table 7.1: *Efficiency, cost and size comparison for the different inverters.*

The analysis was made by comparing the price and robustness of components required for each of the investigated inverters. The price of components in this analysis is in South African Rands (ZAR) and is based on a currency exchange rate of 10 South African Rands to 1 United States Dollar (USD). The efficiency, the price, the size as well as the ruggedness of the switching devices used in each inverter played a significant role in the analysis.

The equations used to calculate the parameters considered in the cost analysis are outlined in Section 4.5 and their values are summarized in Table 7.1. The components cost shown in Figure 7.1 are that of experimental prototypes and a significant reduction of the components cost is envisaged if the inverters are to be produced in large quantities. The graph was plotted using a spreadsheet and the price of each component is as telephonically advised by the supplier of that particular component.

From the analysis of Table 7.1 and Figure 7.1, the two four-level flying capacitor multilevel inverters emerged as superior to the eight-level flying capacitor multilevel inverter in terms of cost, size and performance. Although the 1200 V IGBT half-bridge inverter matched the four-level FCMLI with regard to efficiency, its large filter inductor and an

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expensive switching device make it unsuitable for a cost-effective design. The eight-level 200 V MOSFET flying capacitor multilevel inverter has the smallest filter inductor, but its large size mainly due to extra components makes the four-level multilevel inverter the most attractive option.

7.3 SWITCHING DEVICE SELECTION

The voltage rating of the switching device depends on the type of inverter used. For example, the switching devices for a half-bridge inverter should be capable of sustaining the DC bus voltage of about a 1000 V, whereas those of a multilevel inverter should be able to sustain only the cell voltage, which is a fraction of the DC bus voltage.

The current rating of the switching devices is independent of the type of inverter used and it should be greater or equal to the maximum inductor current ($\hat{i}_l$). Assuming a maximum ripple current of 25%, the maximum inductor current is given by:

$$\begin{aligned} \hat{i}_l &= i_l + 0.25 i_l \\ &= 22.5 + (0.25)(22.5) \\ &= 28.1 \text{ A} \end{aligned} \tag{7.1}$$

Where:$i_l = (S/V_{0(min)})\sqrt{2}$. The current rating of the switching device should be $\geq$ 28.1A.

Device	Description	Voltage rating (V)	Current rating (A)
IRF640	Power MOSFET	200	19
SPW20N60S5	CoolMOS	650	20
SKW30N60	IGBT	600	41
CD50UDE	IGBT module	1200	50

Table 7.2: *The switching devices for the different inverters.*

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Four different switching devices were considered in the device selection. The part numbers of the switching devices as well as their current and voltage ratings are given in Table 7.2. The pros and cons of each device in the quest for realizing the objectives of this research are briefly discussed. The devices are:

- A 1200 V, 50 A IGBT half-bridge module.
  It was mentioned in Chapter 1 that the decision to investigate the use of multilevel inverters was made after constructing a standard half-bridge inverter and observing that the price of the switching device was high and the size of the heat sink was large. This device is therefore introduced in this section for the purpose of comparing its price, size and efficiency with those of the investigated multilevel inverters.

- A 200 V, 19 A ordinary MOSFET semiconductor.
  For this application, these devices can only be used in a multilevel inverter with a minimum of eight levels. This is due to the small voltage rating of these devices. The individual pricing and power loss of the switching devices are reasonable at a switching frequency as high as 50 kHz. Since the eight-level FCMLI requires extra components, this option is costly as compared to that of the four-level FCMLI.

- A 650 V, 20 A CoolMOS semiconductor.
  In literature much was said about these new state-of-the-art devices. These 650 V semiconductors have a much higher voltage blocking capability than ordinary MOSFETs, therefore allowing the design of multilevel inverters with fewer levels and thereby reducing system size and cost. A CoolMOS device's on-state resistance ($R_{ds(on)}$) is reduced by a factor of five for the same chip area as an ordinary MOSFET, hence a significant reduction of the conduction losses.

- A 600 V, 41 A IGBT semiconductor.
  Fast IGBT in NPT-technology with soft, fast recovery anti-parallel EmCon diode offers 75% lower E_{off} compared to the previous generation. This is combined with low conduction losses, short circuit withstand time of 10 μs, excellent ruggedness and temperature stable behaviour. The IGBT is also superior in terms of current-carrying capability to the standard MOSFET and CoolMOS under typical operating conditions of up to 100 kHz.

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7.4 SUMMARY

The research's objective is to design a small sized, low cost and efficient inverter. From the analysis in Section 7.2 and Section 7.3 the following conclusions can be deduced:

- Although the standard half-bridge inverter has an efficiency that matches that of the CoolMOS and IGBT inverters, its large filter inductor and high switching device price make it unsuitable for a low cost and small size design. The price of its heat sink is almost twice the price of that of the IGBT inverter, since its heat sink's thermal resistance value is almost twice that of the IGBT.

- For the eight-level flying capacitor multilevel inverter, the heat sink is reduced by almost 60% as compared to that of the standard half-bridge inverter and it also has the smallest filter inductor. But the size of this inverter is large due to the extra components that come with the higher number of levels.

- In terms of size, efficiency and cost, the two four-level flying capacitor multilevel inverters emerged superior as compared to the standard half-bridge inverter and the eight-level flying capacitor multilevel inverter. But due to the high current carrying capability and the excellent ruggedness offered by the IGBT, the four-level flying capacitor multilevel inverter using IGBT switching devices was chosen for development.

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CHAPTER 8

EXPERIMENTAL RESULTS

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8.1 INTRODUCTION

This chapter presents experimental results obtained from the practical work done on the auxiliary power supply and its self-starting circuit described in Chapter 6, the controller in Chapter 5 and the four-level inverter selected in Chapter 7. Experimental results verifying the feasibility of the developed bootstrap power supply on multilevel inverters are also presented in this chapter. The results in this Chapter were obtained using the following equipment: a Tektronix TDS3014 four-channel digital phosphor oscilloscope and a Tektronix P3010 voltage probe. The data was transferred on a stiffy and either plotted with Microsoft Excel or shown as a bitmap diagram.

8.2 AUXILIARY POWER SUPPLY

The purpose of the experimental work in this section is to verify that the self-starting auxiliary power supply complies with its specifications. The specifications are again given in Table 8.1.

Parameter	Value	Unit
Power rating	15	W
Input voltage	750 - 1000 V DC	V
Switching frequency	50	kHz
Regulated dc output voltages:		
Output 1	30	V
Output 2	30	V
Output 3	22	V
Output 4	22	V
Output 5	22	V
Output 6	7	V

Table 8.1: *The auxiliary power supply specifications.*

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Parameter	Symbol	Value	Unit
Electrolytic DC bus capacitor	C_d	470	μF
High frequency DC bus capacitor	C_d	0.47	μF
DC bus voltage	V_d	750	V DC
Switching frequency	f_s	50	kHz
Duty cycle	D	0.5	

Table 8.2: *The experimental parameters of the four-level multilevel inverter.*

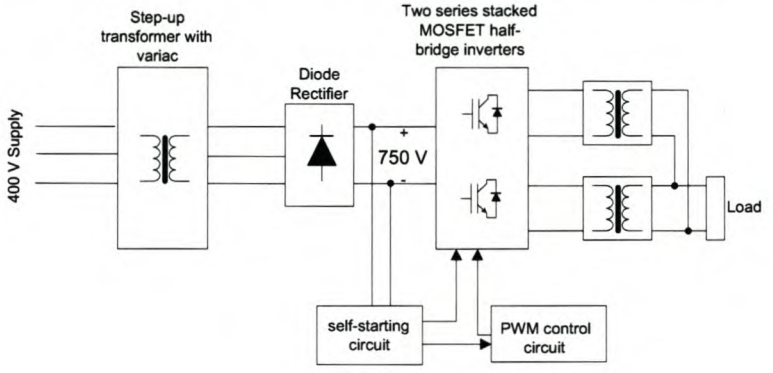

Figure 8.1: *A block diagram of the auxiliary power supply's experimental setup.*

8.2.1 Experimental setup - Auxiliary Power Supply

Figure 8.1 shows a block diagram of an experimental set-up of the auxiliary power supply. The set-up is comprised mainly of two series-stacked MOSFET phase arms, a control circuit, a self-starting circuit and two input-series-output-parallel connected step-down transformers. Each MOSFET phase arm, developed at the University of Stellenbosch for undergraduate study purposes, consists of two 600 V, 10 A MOSFET switches (IRFPC50) and two series connected 450 V, 470 μF DC bus capacitors. 1 W resistors were used as loads on the secondary side of the transformers. The resistance values of these resistors was determined using the amount of current flowing in each secondary winding as per system's specifications. The SG3425-based PWM control circuit and the self-starting circuit used in this setup were discussed in Chapter 6. The control circuit

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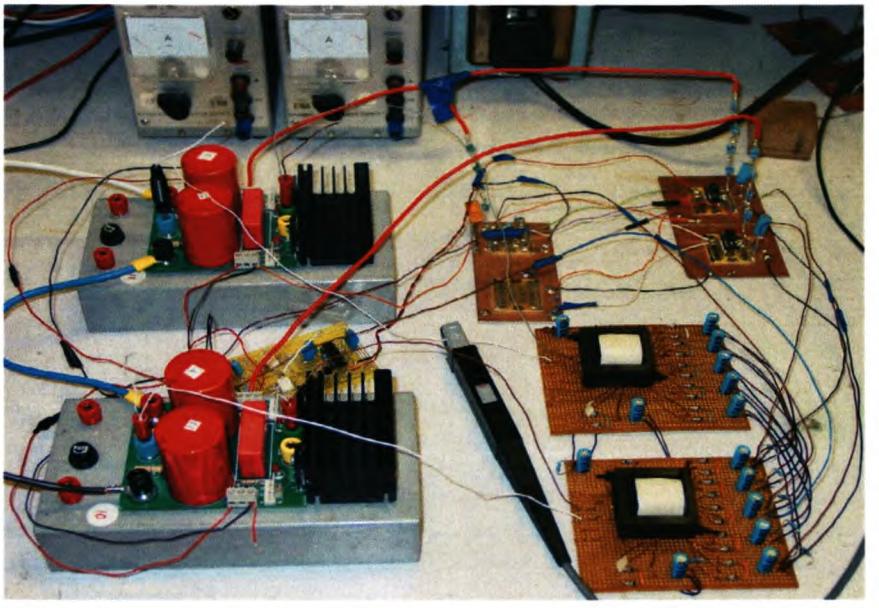

Figure 8.2: *A picture of the experimental prototype of the auxiliary power supply.*

is used to generate the PWM gating signals for the two series-stacked MOSFET phase arms while the self-starting circuit is used to provide self-starting power for the control and gate drive circuits. A full schematic of the auxiliary power supply is given in Appendix C. The picture of the experimental prototype is shown in Figure 8.2.

8.2.2 Experimental results - Auxiliary Power Supply

Figure 8.3 shows the results obtained from the self-starting circuit. The voltages of the 470 μF and the 220 μF capacitors charges exponentially. Due to the long time it takes the two capacitors to charge to the desired 16 V, the exponential rise of the voltages was not captured. The results in Figure 8.3 show key voltages of the self-starting circuit during turn "on" of the voltage controlled switch. Immediately after the voltage of the 470 μF capacitor reaches 16 V, power starts flowing to the pulse width modulator and the gate drive circuits.

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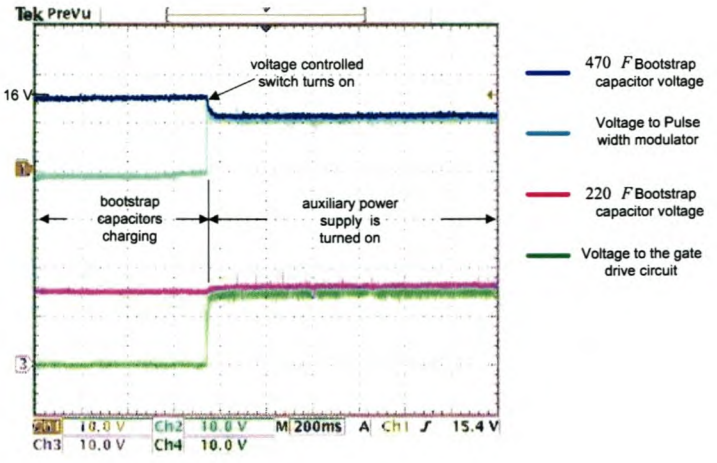

Figure 8.3: *The experimental results of the self-starting circuit.*

Figure 8.4 shows the output results of the self-starting auxiliary power supply. These results show that the auxiliary power supply self-started successfully and that it complies with its specifications. Since a 5 V regulated voltage is required at the input of the controller, a 5 V linear voltage regulator is connected on the output providing power to the controller. The 5 V regulated voltage is also shown in Figure 8.4. The remaining outputs provide power to circuits incorporating zener based voltage regulation techniques, hence voltage regulation on these outputs is unnecessary.

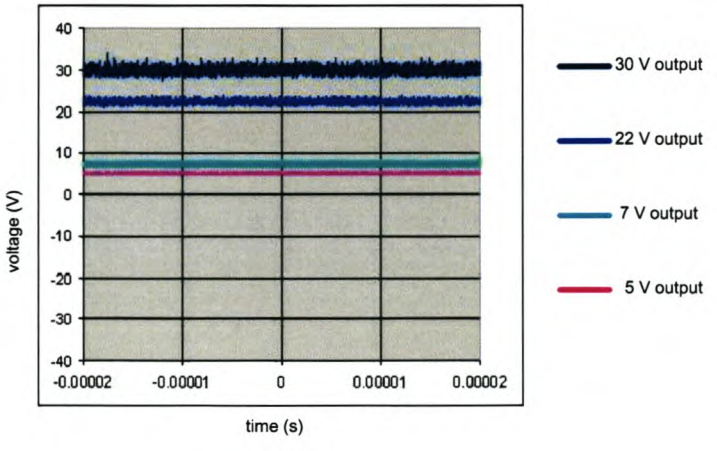

Figure 8.4: *The experimental results of the auxiliary power supply.*

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8.3 BOOTSTRAP POWER SUPPLY

The main aim of the experimental work in this section is to verify the feasibility of the developed bootstrap power supply for multilevel inverters. The power supply was introduced and discussed in Chapter 4. This bootstrap power supply is tested on an eight-level flying capacitor multilevel inverter.

8.3.1 Experimental setup - Bootstrap Power Supply

The eight-level flying capacitor multilevel inverter was constructed using seven MOSFET phase arms, developed at the University of Stellenbosch, and an FPGA based control circuit. The control circuit is used to generate fourteen PWM gating signals for the switching devices. To generate the PWM signals, seven carrier waveforms of frequency 50 kHz are generated inside the FPGA and compared with a reference waveform stored in the FPGA. Dead times of 1 μs are implemented inside the FPGA. A picture of the experimental prototype is shown in Figure 8.5

Figure 8.5: *A picture of an eight-level FCMLI experimental prototype.*

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8.3.2 Experimental results - Bootstrap Power Supply

	Switch no.	Bootstrap capacitor voltage	Voltage fed to the gate drives
TOP	1	24.9	15
	2	25.6	15
	3	26.1	15
	4	26.8	15
	5	27.5	15
	6	28.2	15
	7	29.0	15
BOTTOM	8	24.8	15
	9	25.3	15
	10	25.9	15
	11	26.8	15
	12	27.4	15
	13	28.2	15
	14	29.0	15

Table 8.3: *The bootstrap power supply voltages.*

The results obtained with the experimental prototype of the eight-level flying capacitor multilevel inverter using the developed bootstrap power supply, at a DC bus voltage of 420 V, are shown in Figure 8.6. The power supply voltages measured on the gate drive circuit of each of the fourteen switches are summarized in Table 8.3.

From the results of Table 8.3, the voltage drop across the bootstrap diodes mentioned in Chapter 4 is evident. But due to the employed zener-based voltage regulator the supply voltage of each of the fourteen gate drive circuits is 15 V. The results of Figure 8.6 and Table 8.3 verify the feasibility of the developed bootstrap power supply on multilevel inverters.

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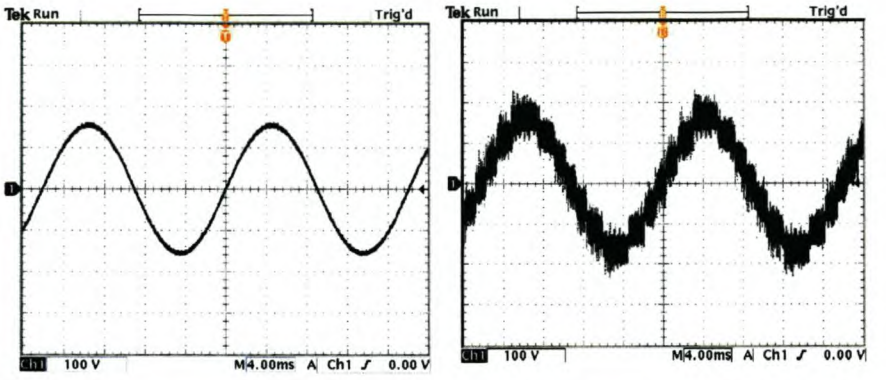

(a) Filtered output voltage of an eight-level FCMLI

(a) Unfiltered output voltage of an eight-level FCMLI

Figure 8.6: *The output voltage waveforms of the eight-level FCMLI.*

8.4 CONTROLLER

The output voltage feed-forward regulation and the overcurrent protection techniques implemented in the controller are experimentally evaluated in this section.

8.4.1 Feed-forward voltage regulation

- **Experimental setup - Feed-forward voltage regulation**
  The experimental setup of the feed-forward voltage regulation circuit is as shown in Figure 8.7.
  The setup consists of a four-level flying capacitor multilevel inverter, an FPGA based controller and an analog-to-digital converter circuit. The analog-to-digital converter circuit and the controller circuit were not mounted on the same PCB. To avoid electro-magnetic interference related problems, the feasibility of the feed-forward voltage regulation technique was demonstrated at low voltage levels. Since the reference voltage of the analog-to-digital converter is bound between 0 V and 5 V, the input analog voltage will also be within the 0 - 5 V range. Having stored four reference waveforms inside the FPGA led to the 0 V to 5 V range being divided by four. This means that the first reference waveform will be selected when the analog input voltage is bound between 0 V and 1.25 V. Since the analog to digital converter is an 8-bit device, the digital output will be bound between 0 and

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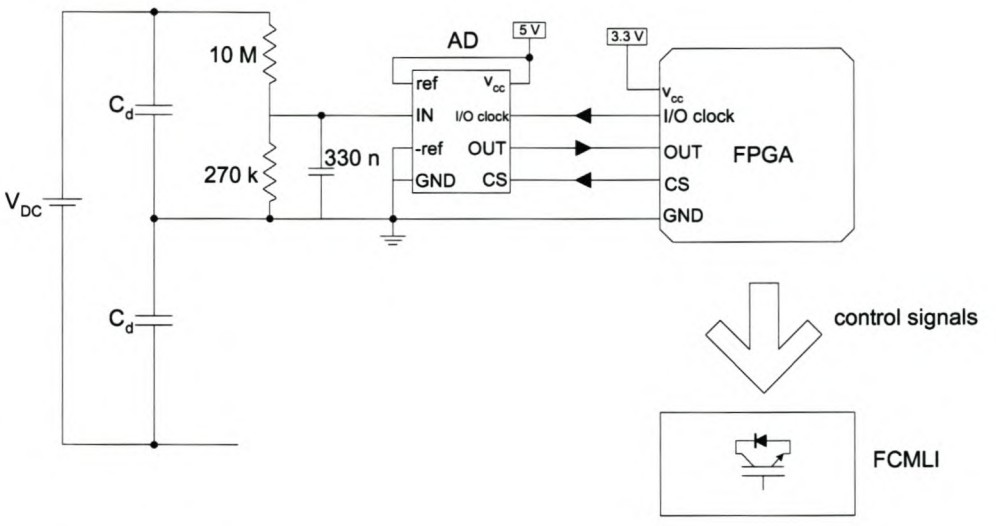

Figure 8.7: *The circuit diagram of the feed-forward voltage regulation technique.*

64 when the analog input is within the 0 V to 1.25 V range.

The voltage divider circuit, in Figure 8.7, that feeds the analog-to-digital converter with an analog input was designed such that the analog input voltage is equal to 1.25 V when the DC bus voltage is 101 V. A 10 MΩ high voltage resistor was used as part of the voltage divider circuit. To achieve a 1.25 V at the analog input of the AD, a resistor that is 40 times smaller as compared to the 10 M ohm resistor should be used to complete the voltage divider circuit. Dividing 10×10^6 by 40 gives 250×10^3, hence a 250 kΩ was used.

Due to the ripple in the DC bus voltage, a low pass filter should be employed to filter the high frequency component of the ripple voltage. The value of the filter capacitor to be used for a cut-off frequency of 10 Hz was determined.

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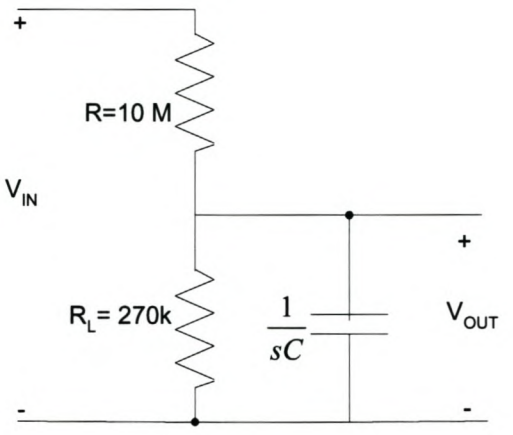

Figure 8.8: *A low pass filter voltage divider circuit*

Using the transfer function theory [34] and choosing a cut-off frequency of 10 Hz, the value of the capacitor in Figure 8.8 is given by:

$$\begin{aligned} \omega_c &= \frac{R_L + R}{R_L RC} \\ C &= \frac{R_L + R}{R_L R \omega_c} \\ &= 380 \text{ nF} \end{aligned} \tag{8.1}$$

Where ω_c is the cut-off frequency. Due to unavailability of a 380 nF capacitor, a 390 nF capacitor was used instead.

To demonstrate the functionality of this regulation technique, the circuit was re-designed for dc input voltages of up to 400 V. The output voltage was regulated between 20 V and 40 V, instead of regulating it between 220 V and 240 V. The modulation indexes of the four reference sine waveforms are given in Table 8.4.

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Reference waveform	Modulation index	DC bus voltage range (V)	Output voltage (V)
1	0.867	100	30
2	0.566	101 - 200	20 - 40
3	0.377	201 - 300	27 - 40
4	0.283	301 - 400	30 - 40

Table 8.4: *The output voltage regulation parameters.*

- **Experimental results - Feed-forward voltage regulation**

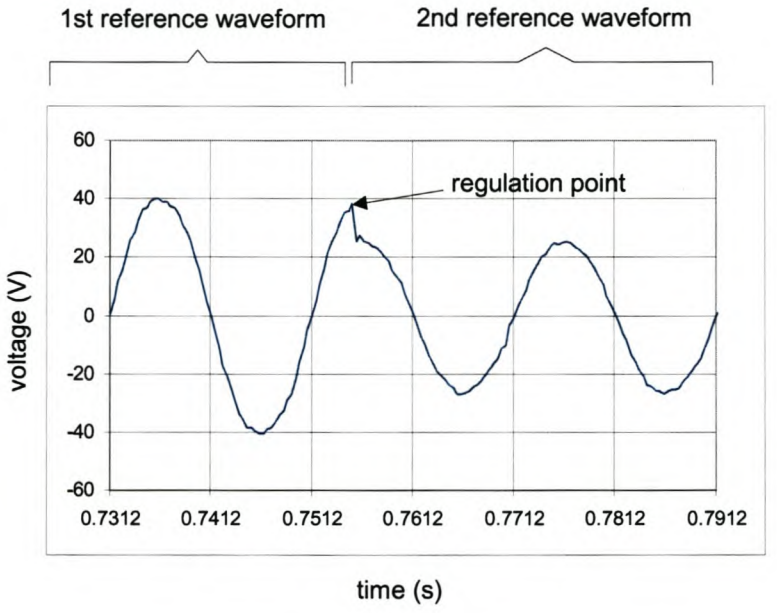

Figure 8.9: *The regulated output voltage of the FCMLI for a 100 V input voltage.*

The results of Figure 8.9 were obtained with a DC bus voltage of between ± 100 V and ± 200 V. The results are explained as follows: Firstly, the dc input voltage was increased to just below the 100 V level. During this time the reference waveform employed inside the FPGA is the one with a modulation index of 0.867.
Secondly, after a while the dc input voltage was increased to just above the 100 V level. The results of Figure 8.9 shows the point of regulation when the voltage goes

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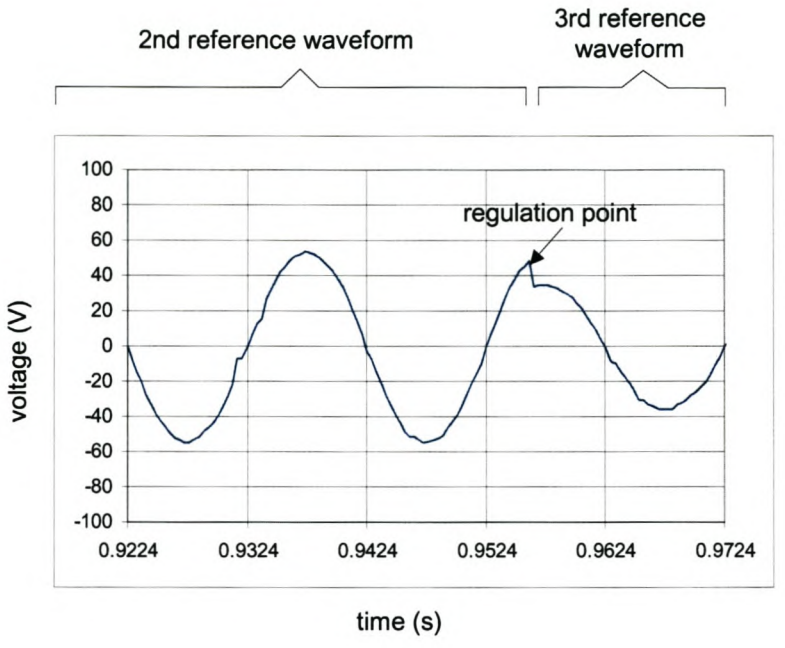

Figure 8.10: *The regulated output voltage of the FCMLI for a 200 V input voltage.*

above 100 V. This occurs when the 0.867 modulation index reference waveform is automatically disabled and the 0.566 modulation index reference waveform is selected.

Thirdly, the voltage was increased to just below 200 V and lastly the voltage was increased to above 200 V level. Figure 8.10 shows the output voltage during the voltage regulation. Problems associated with electro-magnetic interference (EMI) came into play when the dc voltage is above 200 V. These EMI problems could be avoided by mounting the FPGA and the analog-to-digital converter on the same PCB.

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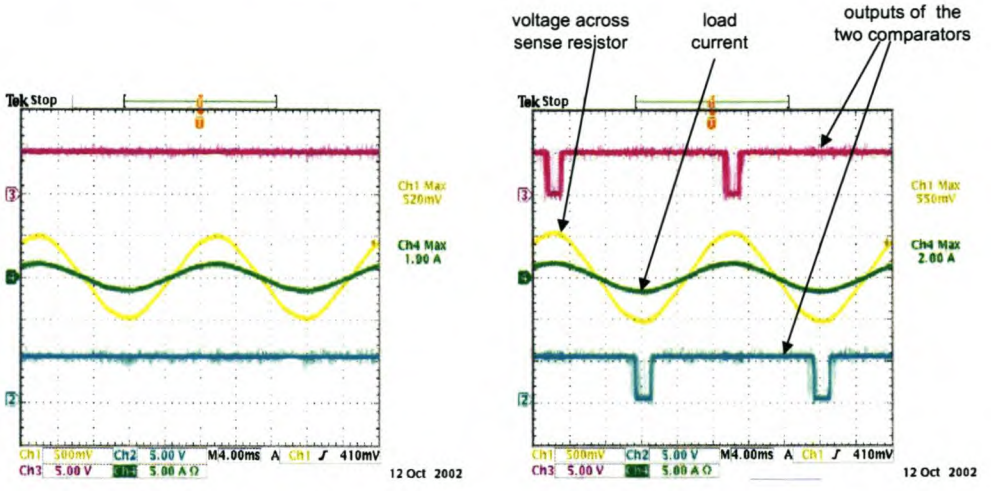
8.4.2 Overcurrent protection



(a) Results for a load current of 38 A

(a) Results for a load current of 40 A

Figure 8.11: *The results of the current sense circuit.*

- **Experimental setup - Overcurrent protection**
  The experimental setup of the overcurrent protection circuit is mainly comprised of a 15 mΩ current sense resistor, an operational amplifier, an inverting amplifier, two comparators and a non-inverting optocoupler. The amplifier is used to amplify the voltage across the current sense resistor. The two comparators compares the positive and negative cycles of the amplified voltage, whilst the optocoupler provides electrical isolation between the controller and the current sensing circuit. The circuit is designed such that the controller will see a fault signal from the optocoupler when the current flowing through the current sense resistor is equal to 40 A.

- **Experimental Results - Overcurrent protection**
  The experimental results obtained with the setup described above are shown in Figure 8.11. The results show that when the current flowing through the current sense resistor is below 40 A, the output of the comparator is high. The instant the current flowing through the current sense resistor reaches 40 A, the output of comparator goes low. During this time the controller goes into an overcurrent protection mode.

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8.5 POWER STAGE OF THE FOUR-LEVEL FCMLI

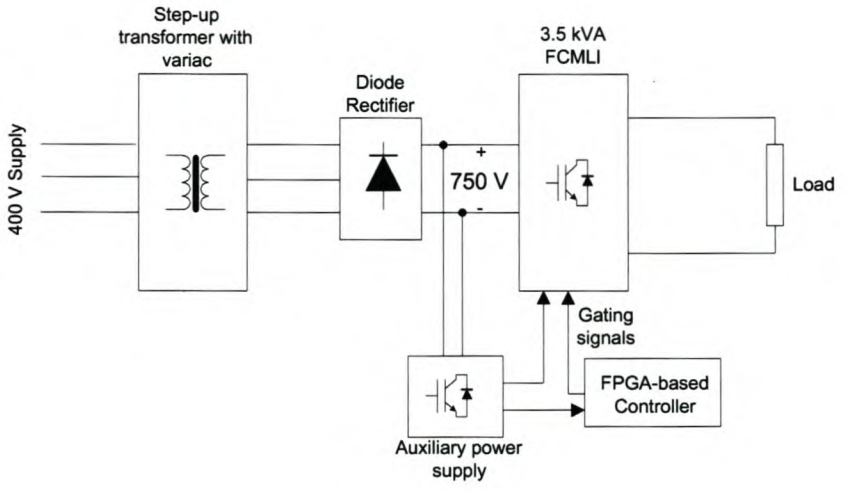

Figure 8.12: *A block diagram of the experimental setup of the inverter.*

This section presents experimental results obtained from the four-level flying capacitor multilevel inverter with bootstrap powered gate drive circuits. The inverter was only exposed to 750 V DC bus voltage and the auxiliary power supply in Chapter 6 was employed to provide the control and gate drive circuitry with the required regulated dc power supplies.

8.5.1 Experimental setup - Power Stage

Figure 8.12 is a block diagram of the experimental set-up. The set-up consists of a 400 V power supply, a step-up transformer, a diode rectifier, a power stage of a four-level flying capacitor multilevel inverter, a controller, an auxiliary power supply and a load. The power stage is comprised of the DC bus capacitors, a series connection of six SKW30N60 IGBT switches (600 V and 41 A rated voltage and current), two flying capacitors, an output filter and a load.

The experimental circuit of the power stage is as shown in Figure 8.13 and the experimental parameters of the components used are given in Table 8.5. The controller of Chapter 5 provides the control signals for the switching devices of the inverter, whereas

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Parameter	Symbol	Value	Unit
Electrolytic DC bus capacitor	C_d	2200	μF
High frequency DC bus capacitor	C_d	0.47	μF
DC bus voltage	V_d	750	V DC
Output filter capacitor	C_f	2	μF
Flying capacitor	C_k	2.5	μF
Output filter inductor	L_f	99	μH
Load resistance	R	15	Ω
Switching frequency	f_s	50	kHz

Table 8.5: *The experimental parameters of the four-level multilevel inverter.*

the auxiliary power supply of Chapter 6 provides regulated dc power supplies to the controller and the inverter's gate drive circuitry. The picture of the experimental prototype is shown in Figure 8.14.

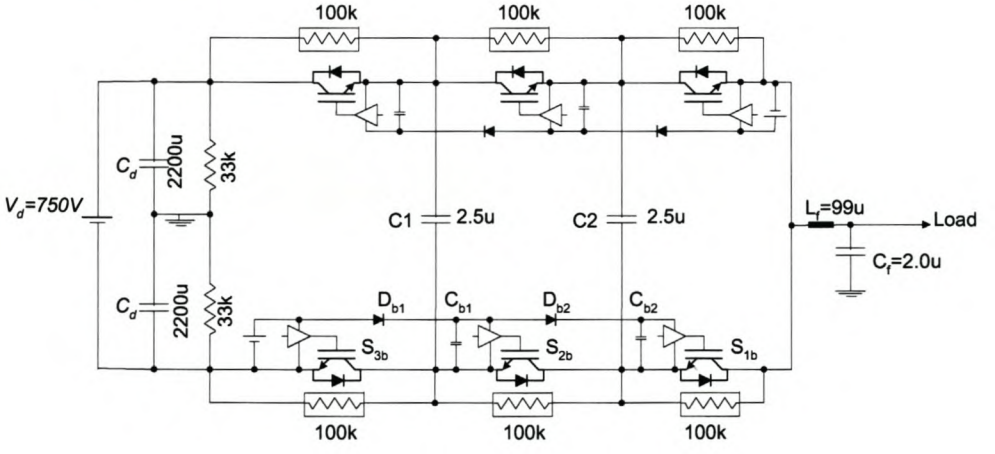

Figure 8.13: *A four-level multilevel inverter with a bootstrap power supply.*

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Figure 8.14: *A picture of the experimental prototype of a four-level FCMLI.*

8.5.2 Experimental results - Power Stage

The results obtained with the experimental prototype of Section 8.5.1 are shown in Figure 8.15. These results verifies the feasibility of the developed self-starting auxiliary power supply on a flying capacitor multilevel inverter. The results are for a DC bus of 720 V. Because the auxiliary power supply was connected to the inverter with the aid of connection wires, the system was susceptible to electro-magnetic interference. The setup showed very good results. The slight distortion in the output current can be attributed to the 1 μs dead time implemented in the controller. The output RMS voltage was measured to be 210 V. Taking into account the ± 10 V drop across the three switching devices, the expected RMS output voltage was 220 V.

To be able to show that the inverter's output voltage complies with its specifications, it was decided to replace the auxiliary power supply with Topward power supplies. This was done to avoid the EMI problems experienced when the auxiliary power supply is used to power the inverter. To solve these EMI problems the auxiliary power supply has to be integrated on the same PCB board with the main inverter and controller.

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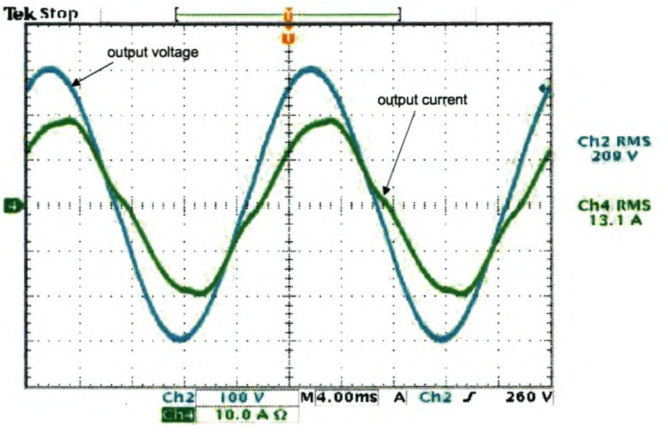

Figure 8.15: *A four-level FCMLI filtered output waveforms with the auxiliary power supply.*

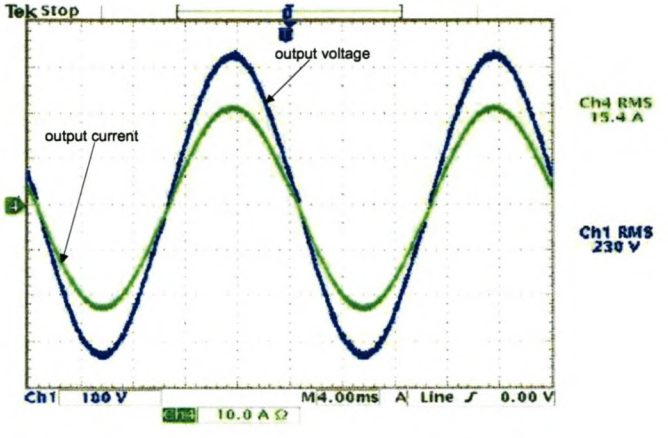

Figure 8.16: *A four-level FCMLI filtered output waveforms with isolated power supplies.*

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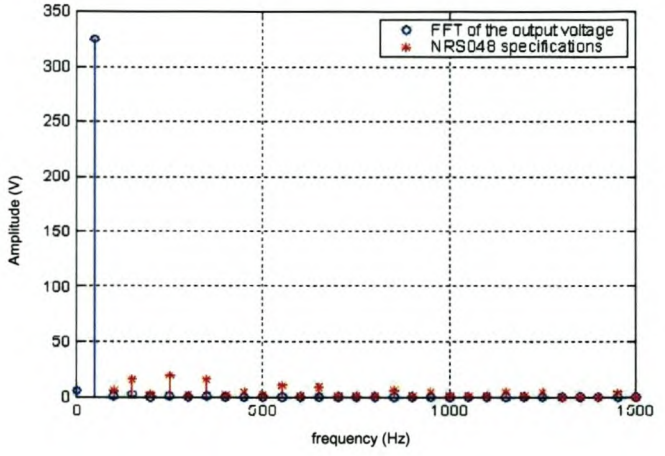

Figure 8.17: *A graphical comparison between the harmonic spectrum of the output voltage of a linear load and that of the NRS 048 specifications.*

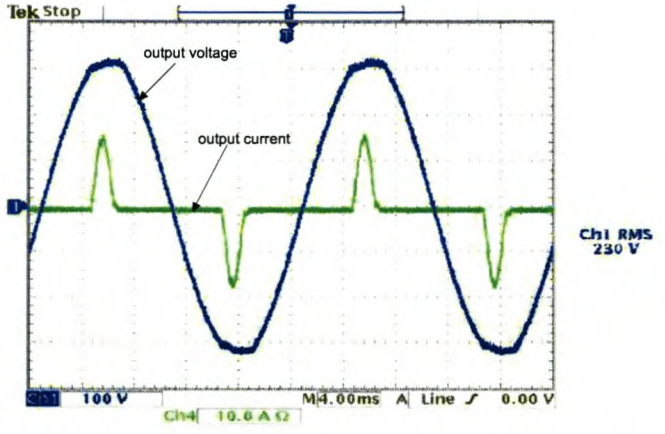

Figure 8.18: *The output voltage waveforms for a non-linear load.*

The output results obtained using Topward power supplies are shown in Figure 8.16. These results are for a purely resistive load and are for a DC bus voltage of 810 V. The input voltage was not increased beyond 810 V, since the feed-forward voltage regulation technique was not fully operational at the time these tests were conducted. The RMS voltage and RMS current were measured to be 230 V and 15 A respectively. The results show that the inverter complies with its specifications.

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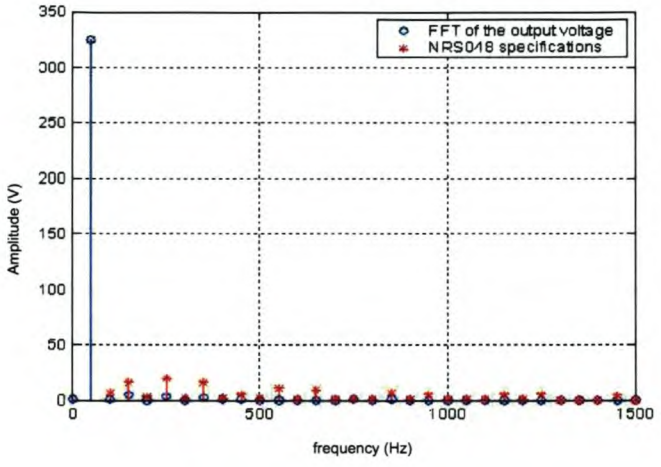

Figure 8.19: *A graphical comparison between the harmonic spectrum of the output voltage of a non-linear load and that of the NRS 048 specifications.*

The output voltage of Figure 8.16 was used to plot the harmonic spectrum using Matlab. The plotted harmonic spectrum is compared with the NRS 048 harmonics specifications in Figure 8.17. Figure 8.17 clearly shows that the harmonics of the output voltage are well within the NRS 048 harmonics specifications. The total harmonic distortion was also calculated using a Matlab program, and was found to be 0.8723 %.

The behaviour of the inverter's output waveforms was investigated under a non-linear load. The same experimental setup as that of a purely resistive load was used in this regard, except for the load which comprised of a diode rectifier in parallel with a 1100 μF capacitor and a 174 Ω resistor. Figure 8.18 shows the output voltage and the output current of the inverter for a non-linear load. The harmonic spectrum of the output voltage was plotted with Matlab. Figure 8.19 shows a comparison between the harmonic spectrum for a non-linear load with that of the NRS 048 specifications. The total harmonic distortion was calculated to be 2.1302 %.

The efficiency of the converter was measured as a function of the load current. Efficiency of a system is defined as the ratio of the average output power to the average input power. The average input power was computed with Matlab, using the measured values of the input current and input voltage for various dc input voltages. The same method was

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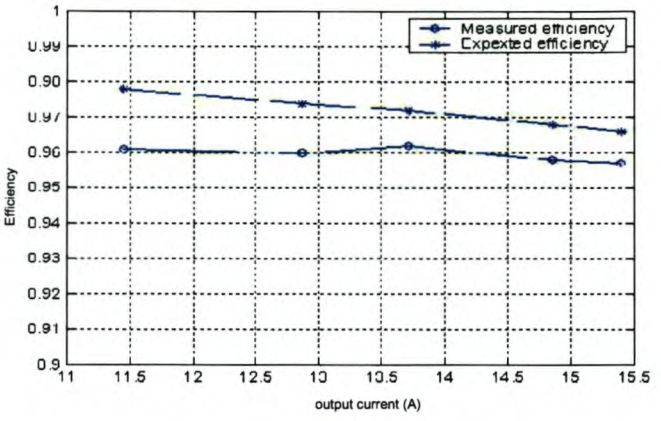

Figure 8.20: *A graph of the inverter's efficiency versus load current.*

used to compute the average output power. Figure 8.20 shows a comparison between the measured efficiency and the theoretically expected efficiency as a function of the load current. The theoretically expected efficiency was calculated using the power loss equations in Chapter 4. The efficiency of the inverter at full load was measured and it is equal to 95.7 %.

8.6 SUMMARY

Experimental tests conducted on the auxiliary power supply were successful. The experimental results obtained showed that the auxiliary power supply complied with its specifications. The feasibility of the developed bootstrap power supply on multilevel inverters was experimentally verified on an eight-level flying capacitor multilevel inverter. The functionality of the feed-forward output voltage regulation technique was demonstrated at voltages below the rated output voltage since EMI became a problem at higher voltages. The overcurrent protection circuit was tested separately from the inverter and showed potential of protecting the inverter against an overcurrent. The experimental results obtained from the experimental prototype of the four-level flying capacitor multilevel inverter showed that this inverter complies with its specifications. The efficiency and the total harmonic distortion of this inverter at full load was found to be 95.7 % and 0.8723 % respectively.

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CHAPTER 9

CONCLUSIONS

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9.1 AUXILIARY POWER SUPPLY

In DC to AC power conversion, the inverter uses inverter circuits to convert the DC voltage to AC voltage. These inverter circuits require dc power supplies. Since the proposed method of solving the non-technical power loss problem envisages the removal of the domestically rated 230 V, 50 Hz reticulation networks from the affected areas, a switch mode power supply (SMPS) that will provide regulated dc power supplies to the inverter circuits is needed. The SMPS had to be self-starting, because it also needs regulated dc power supplies to function. The design and development of a self-starting SMPS was introduced and discussed. The auxiliary power supply was successfully tested on a flying capacitor multilevel inverter.

9.2 THE CONTROLLER

An FPGA based digital PWM control method was developed for the control of the multilevel inverter. The digital method was chosen because of the simplicity of implementing interleaved switching, which is desirable for a flying capacitor multilevel inverter. This controller incorporates a feed-forward output voltage regulation technique for keeping the output voltage within a specified range. The capability of implementing complicated control algorithms in a digital controller will make the ultimate aim of integrating the flying capacitor multilevel inverter with a prepaid metering system possible. Experimental tests of this controller were conducted on a flying capacitor multilevel inverter and yielded good results. Experimental and simulation results of the incorporated feed-forward voltage regulation technique were presented.

9.3 MULTILEVEL INVERTER

DC reticulation was proposed as a solution to the non-technical power loss problem experienced by the utility. The main objective of this work was to design and develop a cost-effective, acoustical noise-free and small sized inverter for DC reticulation. The need for a cost-effective, noise-free and small sized inverter was introduced in Chapter 1. Due to the great deal of interest given to multilevel inverters in recent years, the possible

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use of these inverters for a low cost, acoustical noise-free design was investigated.

Chapter 2 presented a comprehensive study on the two main multilevel topologies, for instance the flying capacitor multilevel inverter (FCMLI) and the diode clamp multilevel inverter (DCMLI), suitable for DC reticulation. The FCMLI emerged more suitable for DC reticulation than the DCMLI. It was found from the study that due to the extra switching components in multilevel inverter topologies, the feasibility of using these inverters for DC reticulation rested on the success of developing a low cost gate drive circuit for the switching components. A low cost gate drive circuit based on the bootstrap power supply principle was developed for multilevel inverters.

The structure of the multilevel topologies allows the designer to use low voltage rated and fast switching devices, making it possible to switch at frequencies well above audible noise with minimal switching power losses. The high switching frequency results in a small filter inductor and small flying capacitors. The design and development of a flying capacitor multilevel inverter was presented and the following conclusions were drawn:

- A low cost gate drive circuit, small values of the flying capacitors and small filter inductor contributed significantly in lowering the overall cost of the inverter. The overall system cost was kept under one thousand South African Rands (ZAR).
- A switching frequency of 50 kHz resulted in an acoustical noise-free inverter, since the maximum frequency human beings can hear is approximately 23 kHz.
- A small output filter and small heat sink reduced the size of the inverter significantly as compared to the constructed standard IGBT half-bridge inverter.

Laboratory tests on the developed four-level flying capacitor multilevel inverter were conducted and the experimental results showed that the inverter satisfied its specifications. The harmonic spectrum of the output voltage was measured and compared with that of the NRS 048 specifications. The total harmonic distortion was calculated to be 0.8723 %. This validates the fact that multilevel inverters have the ability to synthesize voltage waveforms with a better harmonic spectrum.
The developed four-level flying capacitor multilevel inverter provides a low cost, acoustical noise-free and effective solution for the non-technical power loss (theft of electricity) problem.

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9.4 THESIS CONTRIBUTIONS

The main contributions of this thesis are:

- A low cost bootstrap power supply for multilevel inverters was developed. This bootstrap power supply is derived from the conventional bootstrap technique for standard half-bridge inverters.
- A self-starting switch mode power supply that uses a bootstrap technique to get start-up power from the DC bus was designed and developed. To cater for fast-switching applications the self-starting power supply was based on the input-series-output-parallel inverter topology.
- A comparison of different inverters for the proposed DC reticulation application was presented.

9.5 FUTURE WORK

Future work should focus on the following:

- System integration and size optimization. These include placing the auxiliary power supply, the FPGA part of the controller, the analog-to-digital part of the controller, the current sensing circuit and the power stage of the inverter on one printed circuit board (PCB).
- Overcurrent protection tests.
- Output voltage regulation tests at rated output voltage.
- Redesigning the controller to incorporate a prepaid metering system.
- Field tests.

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APPENDIX A

SIMULATION MODELS

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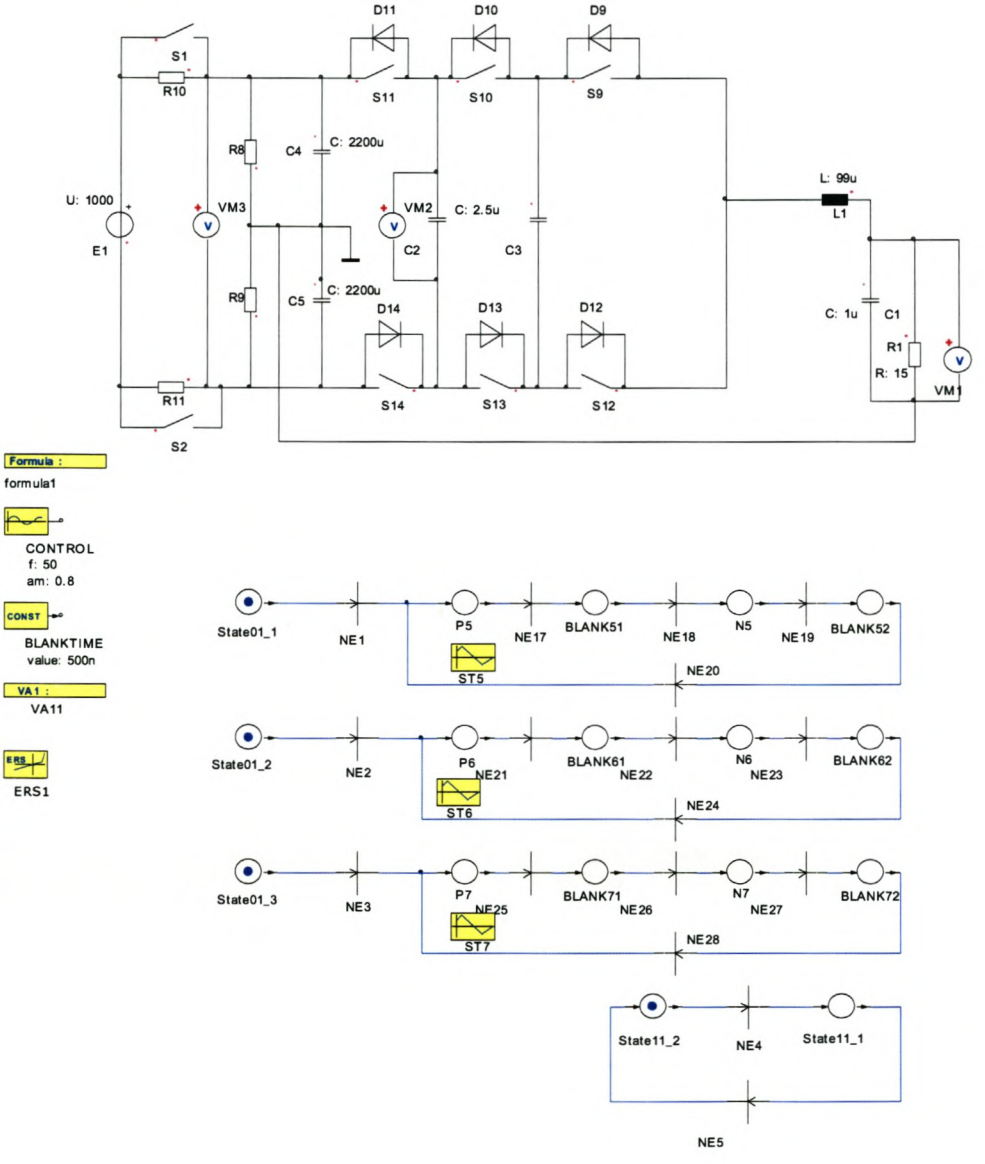

Figure A.1: *A Simplorer simulation model of the four-level FCMLI without a precharging circuit.*

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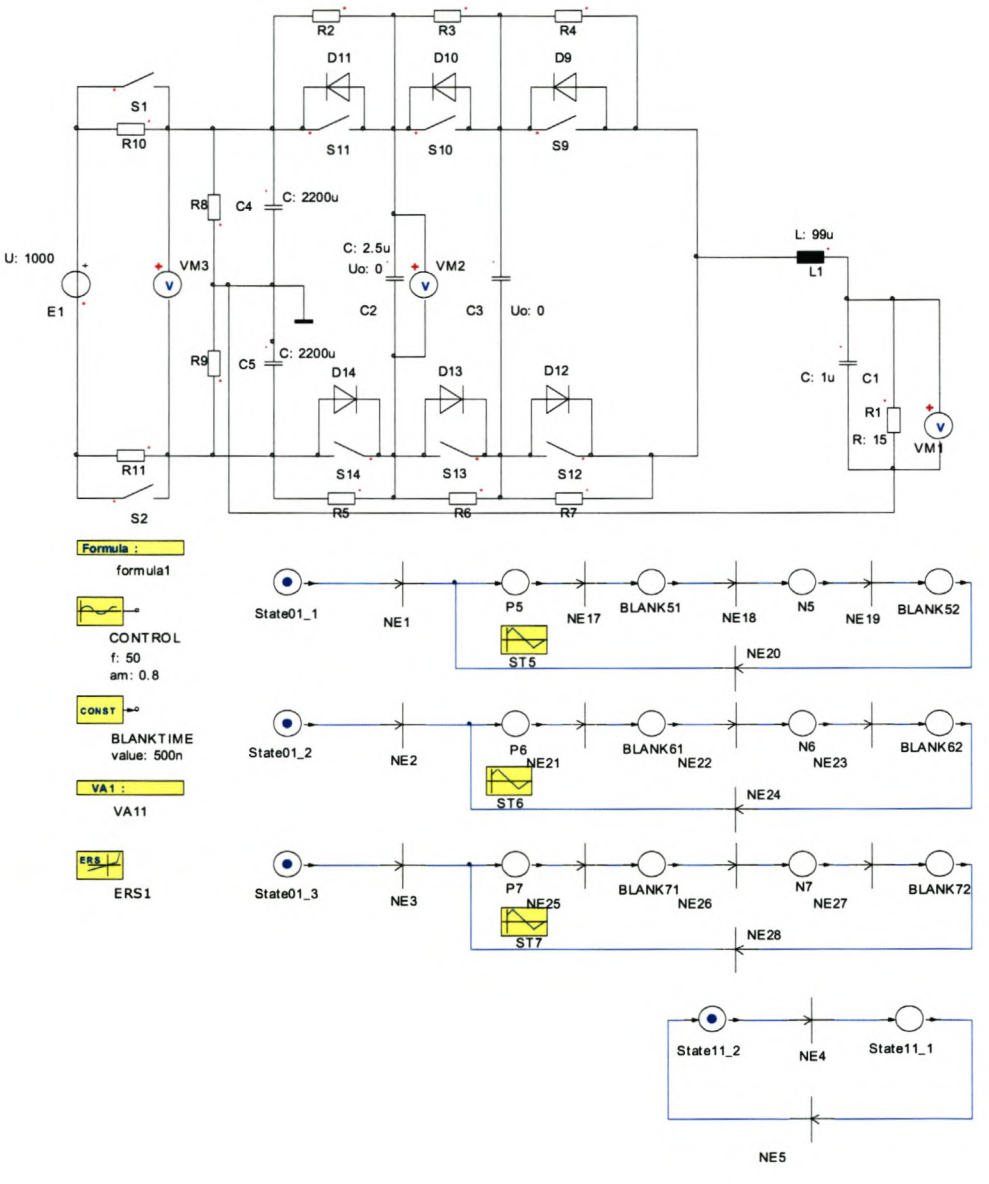

Figure A.2: *A Simplorer simulation model of the four-level FCMLI with a precharging circuit.*

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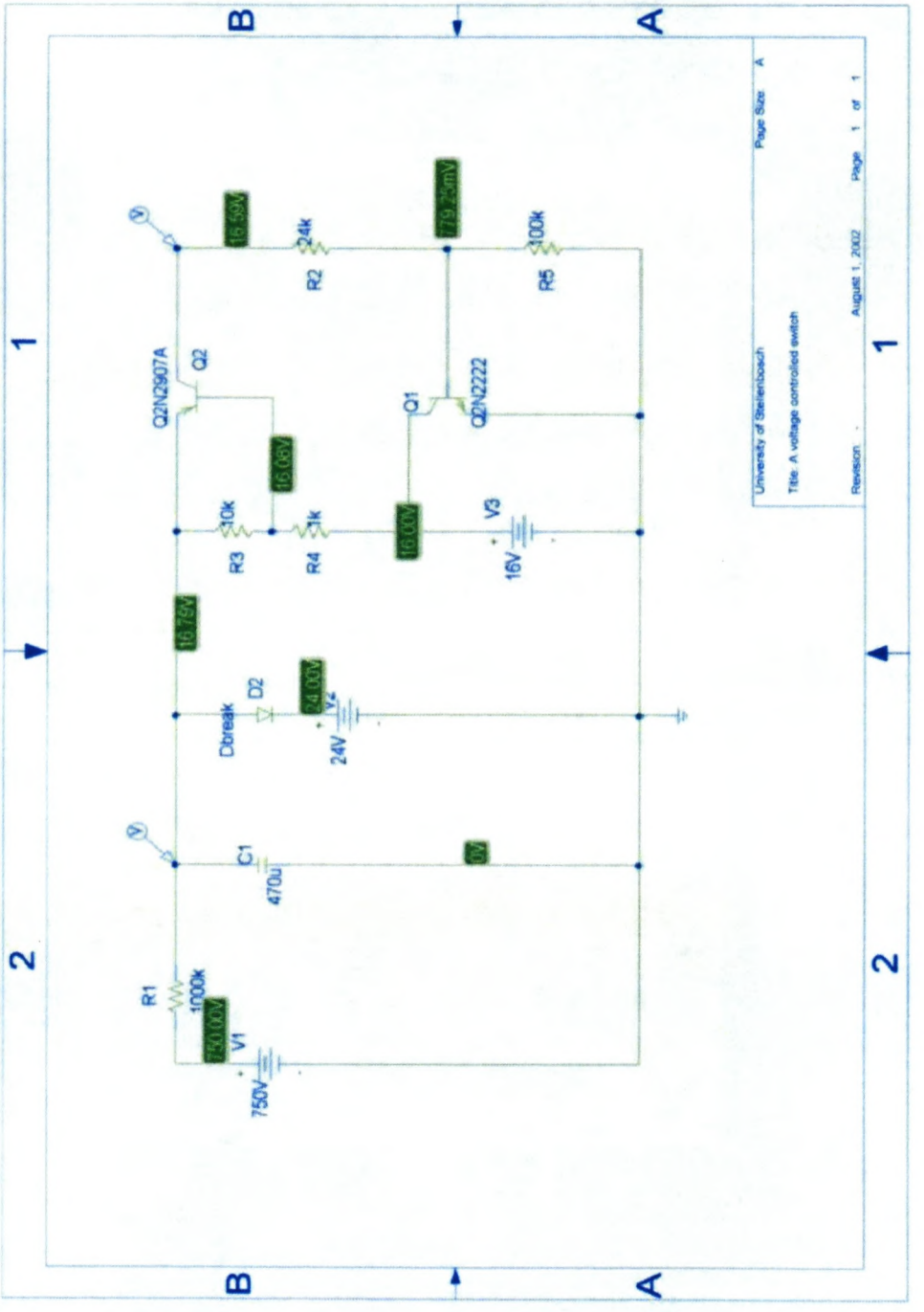

Figure A.3: *A pspice simulation model of the voltage controlled switch.*

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APPENDIX B

PROGRAMS

B.1 MATLAB

- A Matlab program for calculating the average current of the inverter. i_{peak}=22.5A;

```
fcont=50;
Tcont=1/fcont;
Ttri1=21e-6;
wcont=(2*pi)/Tcont;
ts=0;
int(1)=0;
t=[0:0.0000001:Tcont];
for k=2:1:length(t)
Vcont(k)=sin(wcont*t(k));
i(k)=(22.5)*sin(wcont*t(k));
if ts¡=Ttri1/4
Vtri1(k)=(4/Ttri1)*ts;
elseif (ts¿Ttri1/4) and (ts¡=3*Ttri1/4)
Vtri1(k)=1-(4/Ttri1)*(ts-Ttri1/4);
```

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```
else
Vtri1(k)=-1+(4/Ttri1)*(ts-3*Ttri1/4);
end
if ts¿=Ttri1
ts=0;
else
ts=ts+0.0000001;
end
s1(k) is the PWM voltage
d1(k) is the current flowing in a mosfet
when the PWM voltage is high the mosfet is on and vice versa
if (Vcont(k)¿=Vtri1(k))
s1(k)=1;
d1(k)=1;
elseif (Vcont(k)¡=Vtri1(k))
s1(k)=0;
d1(k)=0;
end
int(k)=int(k-1)+(i(k))(i(k))*0.0000001*d1(k);
I2(k)=(1/Tcont)*int(k);
end
ave(I2)=sum(I2)/200001
ave(I1)=sqrt(ave(I2))
plot(t,Vcont,t,Vtri1,t,s1);
figure;
```

- A Matlab program for calculating the charging times of the bootstrap capacitors of the self-starting circuit.

```
Vs1=750;
Vs2=500;
R=300000;
C=0.0000025;
```

$G = (1/(2 * R * C))^2 - (1/(R * C));$

$t = [0 : 0.001 : 10];$

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for k=1:1:length(t)
$V1(k) = Vs1 * (1 - exp(t(k) * G));$
if $V1(k) > 500$
$V1(k) = 500;$
end
$V2(k) = Vs1 * (1 - exp(t(k) * G));$
if $V2(k) > 250$
$V2(k) = 250;$
end

end
plot(t,V1,t,V2);
figure;

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B.2 VHDL

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```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

library lpm;
use lpm.lpm_components.all;

entity feed is
   generic(n : natural :=8);
   port
    (
      clk              : in std_logic; --20 MHz (FPGA clock)
      nReset           : in std_logic;
      adon             : in std_logic;  -- input from A/D
      direction_out    : out std_logic;
      LED              : out std_logic;
      flag_out         : out std_logic;
      p_PWM            : out std_logic;
      p_new3           : out std_logic;
      p_nPWM           : out std_logic;
      p_nnew3          : out std_logic;
      q_PWM            : out std_logic;
      q_new3           : out std_logic;
      q_nPWM           : out std_logic;
      q_nnew3          : out std_logic;
      r_PWM            : out std_logic;
      r_new3           : out std_logic;
      r_nPWM           : out std_logic;
      r_nnew3          : out std_logic;
      falling_edge     : out std_logic;
      dt_end_value     : out std_logic;
      mon              : out std_logic;
      koo              : out std_logic;
      down_clock_ad    : out std_logic;  -- A/D clock (1MHz)
      cs               : out std_logic

       );
end entity feed;

architecture rtl of feed is

   signal vcc, gnd         : std_logic;

   type   TYPE_RAMP is (RAMP_UP, RAMP_DOWN);
   type   TYPE_RAMP1 is (RAMP_DOWN, RAMP_UP);
   signal state_ramp       : TYPE_RAMP;
   signal next_ramp        : TYPE_RAMP;
   signal state_ramp1      : TYPE_RAMP1;
   signal next_ramp1       : TYPE_RAMP1;
   signal state_ramp2      : TYPE_RAMP1;
   signal next_ramp2       : TYPE_RAMP1;
   signal state_ramp3      : TYPE_RAMP;
   signal next_ramp3       : TYPE_RAMP;

   signal state_count      : unsigned(7 downto 0);
   signal next_count       : unsigned(7 downto 0);
   signal state_count1     : unsigned(7 downto 0);
   signal next_count1      : unsigned(7 downto 0);
   signal state_count2     : unsigned(7 downto 0);
   signal next_count2      : unsigned(7 downto 0);
   signal state_count3     : unsigned(7 downto 0);
   signal next_count3      : unsigned(7 downto 0);

signal PWM              : std_logic;
   signal PWM1             : std_logic;
   signal PWM2             : std_logic;
   signal ref              : unsigned(7 downto 0);
   signal v_ref            : std_logic_vector(7 downto 0);
   signal ref_idx          : unsigned(11 downto 0);
   signal v_ref_idx        : std_logic_vector(11 downto 0);
   signal P0,P1            : std_logic;
   signal p_new31          : std_logic;
   signal p_new_3          : std_logic;
   signal current_cnt      : integer range 0 to 20;
   signal next_cnt         : integer range 0 to 20;
   signal falling          : std_logic;
   signal falling_n        : std_logic;
   signal falling_n1       : std_logic;
   signal P                : std_logic;
   signal dt_end           : std_logic;
   signal nP0,nP1          : std_logic;
   signal p_nnew_3         : std_logic;
   signal current_cnt1     : integer range 0 to 20;
   signal next_cnt1        : integer range 0 to 20;
   signal falling1         : std_logic;
   signal nP               : std_logic;
   signal dt_end1          : std_logic;
   ----------------
   signal q0,q1            : std_logic;
   signal q_new_3          : std_logic;
   signal current_cnt2     : integer range 0 to 20;
   signal next_cnt2        : integer range 0 to 20;
   signal falling2         : std_logic;
   signal q_a              : std_logic;
   signal dt_end2          : std_logic;
   signal nq0,nq1          : std_logic;
   signal q_nnew_3         : std_logic;
   signal current_cnt3     : integer range 0 to 20;
   signal next_cnt3        : integer range 0 to 20;
   signal falling3         : std_logic;
   signal nq               : std_logic;
   signal dt_end3          : std_logic;
   ------------------
   signal r0,r1            : std_logic;
   signal r_new_3          : std_logic;
   signal current_cnt4     : integer range 0 to 20;
   signal next_cnt4        : integer range 0 to 20;
   signal falling4         : std_logic;
   signal r                : std_logic;
   signal dt_end4          : std_logic;

   signal nr0,nr1          : std_logic;
   signal r_nnew_3         : std_logic;
   signal current_cnt5     : integer range 0 to 20;
   signal next_cnt5        : integer range 0 to 20;
```

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```
signal falling5          : std_logic;
   signal nr               : std_logic;
   signal dt_end5          : std_logic;
   ---------------------

   signal me               : std_logic;
   signal mon_d            : std_logic;
   signal dee              : std_logic;
   ---------------------
   signal table            : unsigned(11 downto 0);
   ---------------------
   signal output_clk                    : integer range 0 to 20;
   signal scaled_down                    : std_logic;
   signal clock_scaled_down             : std_logic;
   signal cs_count                      : integer range 0 to 540;
   signal cs_new                        : std_logic;
   signal adon_out            : unsigned(7 downto 0);
   signal prev_adon_out                 : unsigned(7 downto 0);
   signal prev_adon_out1                : unsigned(7 downto 0);
   signal prev_adon_out2                : unsigned(7 downto 0);
   signal prev_adon_out3                : unsigned(7 downto 0);
   signal signal_down_clock_ad          : std_logic;
   signal adon_out_old                  : unsigned(7 downto 0);
   signal adon_out_new                  : unsigned(7 downto 0);
   signal flag                           : std_logic;
   signal direction                     : std_logic;
   signal adon_out_old_1                : unsigned(7 downto 0);
   signal table_cnt                     : integer range 0 to 20000;

begin

   gnd      <= '0';
   vcc      <= '1';

   process(clk,nReset)
    begin
      if nReset='0' then
        state_count <="01101001"; --105+
        state_count3<="00000001";
        output_clk<=0;
      elsif clk'event and clk='1' then
          state_count <= next_count;
          state_count3 <= next_count3;
          if output_clk < 19 then
           output_clk<=output_clk+1;
          elsif output_clk =19 then
           output_clk<=0;
          end if;
      end if;
    end process;
```

```
--generating 3 triangular waveform with phase shift of 360/3 (210+210/3=140)

--first triangular waveform (105 y-offset and no phase shift)
process(clk)
begin
   if clk'event and clk='1' then
     state_ramp <= next_ramp;
   end if;
end process;

process(state_ramp,state_count)
begin
   if state_count=209 then
     next_ramp  <= RAMP_DOWN;
   elsif state_count=1 then
     next_ramp  <= RAMP_UP;
   else
     next_ramp  <= state_ramp;
   end if;
end process;

process(state_ramp,state_count)
begin
   case state_ramp is
      when RAMP_UP =>
          next_count <= state_count + 1;
        if state_count = 105 then
           dee<='1';
        else
           dee<='0';
        end if;
      when RAMP_DOWN=>
          next_count <= state_count - 1;
   end case;
end process;

--comparator (comparing the first triangular waveform with the reference)
process(clk)
begin
   if clk'event and clk='1' then
     if state_count < ref(ref'left downto ref'left-state_count'left) then
       PWM     <= '1';
     else
       PWM     <= '0';
     end if;
   end if;
end process;
P       <= PWM;
nP      <= not PWM;
-----------
```

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```
-- second triangular waveform (105 offset and a phase-shift of 120 deg)
  process(clk)
  begin
    if clk'event and clk='1' then
      state_ramp1 <= next_ramp1;
    end if;
  end process;

  process(state_ramp1,state_count1)
  begin
    if state_count1=209 then
      next_ramp1  <= RAMP_DOWN;
    elsif state_count1=1 then
      next_ramp1  <= RAMP_UP;
    else
      next_ramp1  <= state_ramp1;
    end if;
  end process;

  process(state_ramp1,state_count1)
  begin
     case state_ramp1 is
        when RAMP_UP =>
            next_count1 <= state_count1 + 1;
        when RAMP_DOWN =>
            next_count1 <= state_count1 - 1;
     end case;
  end process;

  process(clk,dee)
  begin
    if clk'event and clk='1' then
       if dee ='1' then
        state_count1 <="00100010";--34
       else
        state_count1 <= next_count1;
       end if;
    end if;
  end process;


  --comparator(comparing the second triangular waveform with a the reference)

  process(clk)
  begin
     if clk'event and clk='1' then
        if state_count1 < ref(ref'left downto ref'left-state_count1'left) then
          PWM1    <= '1';
        else
          PWM1    <= '0';
        end if;
     end if;
  end process;
  q_a     <= PWM1;
  nq      <= not PWM1;
 ----------------------
```

```
-- third triangular waveform (105 offset and a phase-shift of 240 deg)
  process(clk)
  begin
     if clk'event and clk='1' then
       state_ramp2 <= next_ramp2;
     end if;
  end process;

  process(state_ramp2,state_count2)
  begin
     if state_count2=209 then
       next_ramp2  <= RAMP_DOWN;
     elsif state_count2=1 then
       next_ramp2  <= RAMP_UP;
     else
       next_ramp2  <= state_ramp2;
     end if;
  end process;

  process(state_ramp2,state_count2)
  begin
     case state_ramp2 is
        when RAMP_UP =>
            next_count2 <= state_count2 + 1;
        when RAMP_DOWN =>
            next_count2 <= state_count2 - 1;
     end case;
  end process;

  process(clk)
  begin
     if clk'event and clk='1' then
        if dee ='1' then
          state_count2 <="10101110";--174-
        else
          state_count2 <= next_count2;
        end if;
     end if;
  end process;

  --comparator (comparing the third triangular waveform with the reference)
  process(clk)
  begin
     if clk'event and clk='1' then
        if state_count2 < ref(ref'left downto ref'left-state_count2'left) then
          PWM2    <= '1';
        else
          PWM2    <= '0';
        end if;
     end if;
  end process;
  r       <= PWM2;
  nr      <= not PWM2;
```

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```
--delay time of the top switch of the first cell
  process(clk,P)
  begin
    if clk'event and clk='1' then
      P0  <= P;
      P1  <= P0;
    end if;
  end process;

  process(P0,P1)
  begin
    if P0 ='1' and P1='0' then
      falling<='1';
    else
      falling<='0';
    end if;
  end process;
  falling_edge <= falling;

  process(falling,current_cnt)
  begin
    if falling ='1' then
      next_cnt <=20;
    else
      next_cnt <=current_cnt -1;
    end if;
  end process;

  process(clk,next_cnt)
  begin
    if clk'event and clk='1' then
      current_cnt <= next_cnt;
    end if;
  end process;

  process(clk,falling,next_cnt)
  begin
    if clk'event and clk='1' then
      if falling = '1' then
        dt_end <='1';
      elsif next_cnt=2 then
        dt_end <='0';
      end if;
    end if;
  end process;
  dt_end_value  <= dt_end;
  p_new_3       <= P1 xor dt_end;
  p_PWM         <= P1;
```

```
  process(clk,p_new_3)
    begin
     if clk'event and clk='1' then
       p_new3       <= p_new_3;
     end if;
    end process;
    -------------------------
    --delay time of the bottom switch of the first cell
    process(clk,nP)
    begin
      if clk'event and clk='1' then
        nP0  <= nP;
        nP1  <= nP0;
      end if;
    end process;

    process(nP0,nP1)
    begin
      if nP0 ='1' and nP1='0' then
        falling1<='1';
      else
        falling1<='0';
      end if;
    end process;

    process(falling1,current_cnt1)
    begin
      if falling1 ='1' then
        next_cnt1 <=20;
      else
        next_cnt1 <=current_cnt1 - 1;
      end if;
    end process;

    process(clk,next_cnt1)
    begin
      if clk'event and clk='1' then
        current_cnt1 <= next_cnt1;
      end if;
    end process;

    process(clk,falling1,current_cnt1)
    begin
      if clk'event and clk='1' then
        if falling1 = '1' then
          dt_end1 <='1';
        elsif current_cnt1=2 then
          dt_end1 <='0';
        end if;
      end if;
    end process;
    p_nnew_3       <= nP1 xor dt_end1;
    p_nPWM         <= nP1;
```

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```
process(clk,p_nnew_3)
  begin
   if clk'event and clk='1' then
     p_nnew3       <= p_nnew_3;
   end if;
  end process;
  ---------------------------------
  --delay time of the top switch of the second cell
  process(clk,q_a)
  begin
     if clk'event and clk='1' then
       q0  <= q_a;
       q1  <= q0;
     end if;
  end process;

  process(q0,q1)
  begin
    if q0 ='1' and q1='0' then
      falling2<='1';
    else
      falling2<='0';
    end if;
  end process;

  process(falling2,current_cnt2)
  begin
     if falling2 ='1' then
       next_cnt2 <=20;
     else
       next_cnt2 <=current_cnt2 - 1;
     end if;
  end process;

  process(clk,next_cnt2)
  begin
     if clk'event and clk='1' then
       current_cnt2 <= next_cnt2;
     end if;
  end process;

  process(clk,falling2,current_cnt2)
  begin
     if clk'event and clk='1' then
       if falling2 = '1' then
         dt_end2 <='1';
       elsif current_cnt2=2 then
         dt_end2 <='0';
       end if;
     end if;
  end process;
  q_new_3       <= q1 xor dt_end2;
  q_PWM         <= q1;
```

```
process(clk,q_new_3)
  begin
   if clk'event and clk='1' then
     q_new3       <= q_new_3;
   end if;
  end process;
  ---------------------------
  --delay time of the bottom switch of the second cell
  process(clk,nq)
  begin
     if clk'event and clk='1' then
       nq0  <= nq;
       nq1  <= nq0;
     end if;
  end process;

  process(nq0,nq1)
  begin
    if nq0 ='1' and nq1='0' then
      falling3<='1';
    else
      falling3<='0';
    end if;
  end process;

  process(falling3,current_cnt3)
  begin
     if falling3 ='1' then
       next_cnt3 <=20;
     else
       next_cnt3 <=current_cnt3 - 1;
     end if;
  end process;

  process(clk,next_cnt3)
  begin
     if clk'event and clk='1' then
       current_cnt3 <= next_cnt3;
     end if;
  end process;

  process(clk,falling3,current_cnt3)
  begin
     if clk'event and clk='1' then
       if falling3 = '1' then
         dt_end3 <='1';
       elsif current_cnt3=2 then
         dt_end3 <='0';
       end if;
     end if;
  end process;
  q_nnew_3       <= nq1 xor dt_end3;
  q_nPWM         <= nq1;
```

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```
process(clk,q_nnew_3)
begin
 if clk'event and clk='1' then
   q_nnew3       <= q_nnew_3;
 end if;
end process;
-----------------------------------------
--delay time of the top switch of the third cell
process(clk,r)
begin
   if clk'event and clk='1' then
     r0  <= r;
     r1  <= r0;

   end if;
end process;

process(r0,r1)
begin
  if r0 ='1' and r1='0' then
    falling4<='1';
  else
    falling4<='0';
  end if;
end process;

process(falling4,current_cnt4)
begin
   if falling4 ='1' then
     next_cnt4 <=20;
   else
     next_cnt4 <=current_cnt4 - 1;
   end if;
end process;

process(clk,next_cnt4)
begin
   if clk'event and clk='1' then
     current_cnt4 <= next_cnt4;
   end if;
end process;

process(clk,falling4,current_cnt4)
begin
   if clk'event and clk='1' then
     if falling4 = '1' then
       dt_end4 <='1';
     elsif current_cnt4=2 then
       dt_end4 <='0';
     end if;
   end if;
end process;
r_new_3       <= r1 xor dt_end4;
r_PWM         <= r1;
```

```
process(clk,r_new_3)
  begin
   if clk'event and clk='1' then
     r_new3       <= r_new_3;
   end if;
  end process;
  --------------------------
  --delay time of the bottom switch of the third cell
  process(clk,nr)
  begin
     if clk'event and clk='1' then
       nr0  <= nr;
       nr1  <= nr0;
     end if;
  end process;

  process(nr0,nr1)
  begin
    if nr0 ='1' and nr1='0' then
      falling5<='1';
    else
      falling5<='0';
    end if;
  end process;

  process(falling5,current_cnt5)
  begin
     if falling5 ='1' then
       next_cnt5 <=20;
     else
       next_cnt5 <=current_cnt5 - 1;
     end if;
  end process;

  process(clk,next_cnt5)
  begin
     if clk'event and clk='1' then
       current_cnt5 <= next_cnt5;
     end if;
  end process;

  process(clk,falling5,current_cnt5)
  begin
     if clk'event and clk='1' then
       if falling5 = '1' then
         dt_end5 <='1';
       elsif current_cnt5=2 then
         dt_end5 <='0';
       end if;
     end if;
  end process;
  r_nnew_3       <= nr1 xor dt_end5;
  r_nPWM         <= nr1;
```

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```
process(clk,r_nnew_3)
begin
 if clk'event and clk='1' then
    r_nnew3       <= r_nnew_3;
 end if;
end process;

---------------------------------------
process(clk,nReset)
begin
   if clk'event and clk='1' then
     state_ramp3 <= next_ramp3;
   end if;
end process;

process(state_ramp3,state_count3)
begin
   if state_count3=209 then
     next_ramp3  <= RAMP_DOWN;

   elsif state_count3=1 then
     next_ramp3  <= RAMP_UP;

   else
     next_ramp3  <= state_ramp3;

   end if;

 end process;

 process(state_ramp3,state_count3)
 begin
    case state_ramp3 is
      when RAMP_UP =>
         next_count3 <= state_count3 + 1;
      when RAMP_DOWN =>
         next_count3 <= state_count3 - 1;
    end case;
 end process;
 koo <= dee;
----------------------------
 --address counter (using the triangular waveform state_count3 to divide the 20ms)
process(clk,state_count3,nReset)
begin
  if state_count3=0 then
    me <='1';
  else
    me <='0';
  end if;
end process;
mon_d <=me
```

```
process(clk,nReset)
begin
  if clk'event and clk='1' then
    mon <= mon_d;
  end if;
end process;

process(clk)
begin
   if clk'event and clk='1' then
     if me ='1' then
       if ref_idx < 951 then
         ref_idx   <= ref_idx + 1;
       else
         ref_idx   <= (others => '0');
       end if;
     end if;
   end if;
end process;
----------
-- A/D clock (1MHz)
--dividing the 20MHz clock to a 1MHz clock
process(clk,output_clk)
begin
       if clk'event and clk='1' then
                if output_clk = 19 then
                 scaled_down <='0';
                elsif output_clk =9 then
          scaled_down <='1';
                end if;
       end if;
end process;
clock_scaled_down <= scaled_down;

process(clk)
begin
       if clk'event and clk='1' then
       signal_down_clock_ad <= clock_scaled_down;
       end if;
end process;
down_clock_ad <= signal_down_clock_ad;

-- counter for cs of the A/D
process(clk)
 begin
       if nReset='0' then
                cs_count<=0;
       elsif clk'event and clk='1' then
                if cs_count<539 then
                cs_count<=cs_count+1;
                elsif cs_count=539 then
                cs_count<=0;
                end if;
       end if;
 end process;
```

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```
process(clk)
begin
        if clk'event and clk='1' then
                if cs_count=160 then
                  cs_new<='1';
                elsif cs_count=510 then
                  cs_new<='0';
                end if;
        end if;
end process;
cs <=cs_new;

-- a shift register for the input data from the A/D
process(signal_down_clock_ad)
        variable reg : unsigned(n-1 downto 0);
begin
        if signal_down_clock_ad'event and signal_down_clock_ad='0' then
                if (cs_count = 0) then
                        reg :="0000000" & adon;
                elsif (cs_count < 160 ) then
                        reg := reg(n-2 downto 0) & adon;
                end if;
                adon_out <= reg ;
        end if;
end process;
adon_out_new <= adon_out;

--updating the output of shift register to a new value when cs goes high
process(signal_down_clock_ad,cs_count)
begin
        if cs_count=161 then
                flag <= '1';
        else
                flag <= '0';
        end if;
end process;
flag_out <= flag;

process(signal_down_clock_ad)
begin
                if rising_edge(flag) then
                        adon_out_old <= adon_out_new;
                end if;
        end process;
```

```
--monitoring the input from the A/D and selecting a new reference waveform.
--This is done by using an offset signal Table
process(signal_down_clock_ad,adon_out_old)
begin
        if signal_down_clock_ad'event and signal_down_clock_ad='1' then
                if table_cnt =19992 then
                        if adon_out_old >= 0 and adon_out_old < 63 then
                                table <= "000000000000";
                                LED <='0';
                        elsif adon_out_old >= 63 and adon_out_old < 127 then
                                table <= "001110111000";
                                LED <='1';
                        elsif adon_out_old >= 127 and adon_out_old < 191 then
                                table <= "011101110000";
                                LED <='0';
                        elsif adon_out_old >= 191 and adon_out_old <= 255 then
                                table <= "101100101000";
                                LED <='0';
                        end if;
                end if;
        end if;
end process;

process(signal_down_clock_ad)
begin
        if rising_edge(flag) then
          prev_adon_out <= adon_out_old;
        end if;
end process;

process(signal_down_clock_ad)
begin
        if rising_edge(flag) then
          prev_adon_out1 <= prev_adon_out;
        end if;
end process;

process(signal_down_clock_ad)
begin
        if rising_edge(flag) then
          prev_adon_out2 <= prev_adon_out1;
        end if;
end process;

process(signal_down_clock_ad)
begin
        if signal_down_clock_ad'event and signal_down_clock_ad='1' then
          prev_adon_out3 <= prev_adon_out2;
        end if;
end process;
```

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```
process(signal_down_clock_ad)
begin
        if signal_down_clock_ad'event and signal_down_clock_ad='1' then
                if adon_out_old > prev_adon_out then
                        direction <= '1';
                elsif adon_out_old < prev_adon_out  then
                        direction <= '0';
                end if;
        end if;
end process;
direction_out <= direction;

--adon_out_old  increasing => direction = '1'
--adon_out_old  decreasing => direction = '0'

--changing to a new reference waveform after a 50Hz signal (20ms)
process(signal_down_clock_ad)
begin
        if nReset='0' then
                table_cnt <=0;
        elsif signal_down_clock_ad'event and signal_down_clock_ad='1' then
                if table_cnt < 19992 then
                table_cnt<=table_cnt + 1;
                elsif table_cnt=19992 then
                table_cnt<=0;
                end if;
        end if;
end process;
```

```
--generating a control sine wave
  rom_00:
  lpm_rom
    generic map
    (
     LPM_WIDTH      => 8,
     LPM_WIDTHAD    => 12,
     LPM_NUMWORDS   => 3808,
     LPM_ADDRESS_CONTROL => "REGISTERED",
     LPM_OUTDATA        => "REGISTERED",
     LPM_FILE           => "four_sinelow.mif",
     LPM_TYPE           => "LPM_ROM",
     LPM_HINT           => "UNUSED"
    )
    port map
    (
     address   => v_ref_idx,
     inclock       => clk,
     outclock  => clk,
     memenab   => vcc,
     q         => v_ref
    );

  v_ref_idx  <= ref_idx+table;
  ref       <= unsigned(v_ref);

end architecture;
```

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APPENDIX C

SCHEMATICS

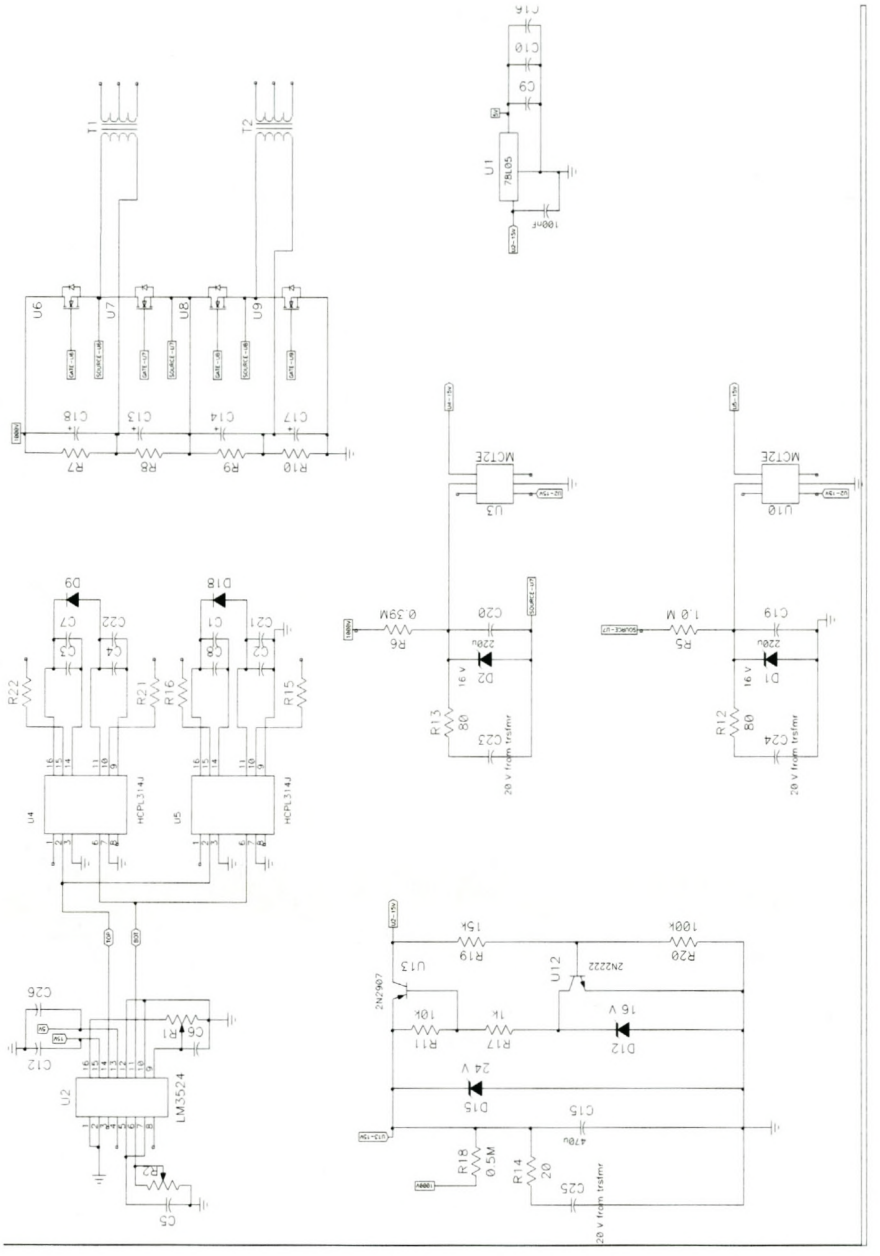

Figure C.1: *A PCAD schematic of the auxiliary power supply.*

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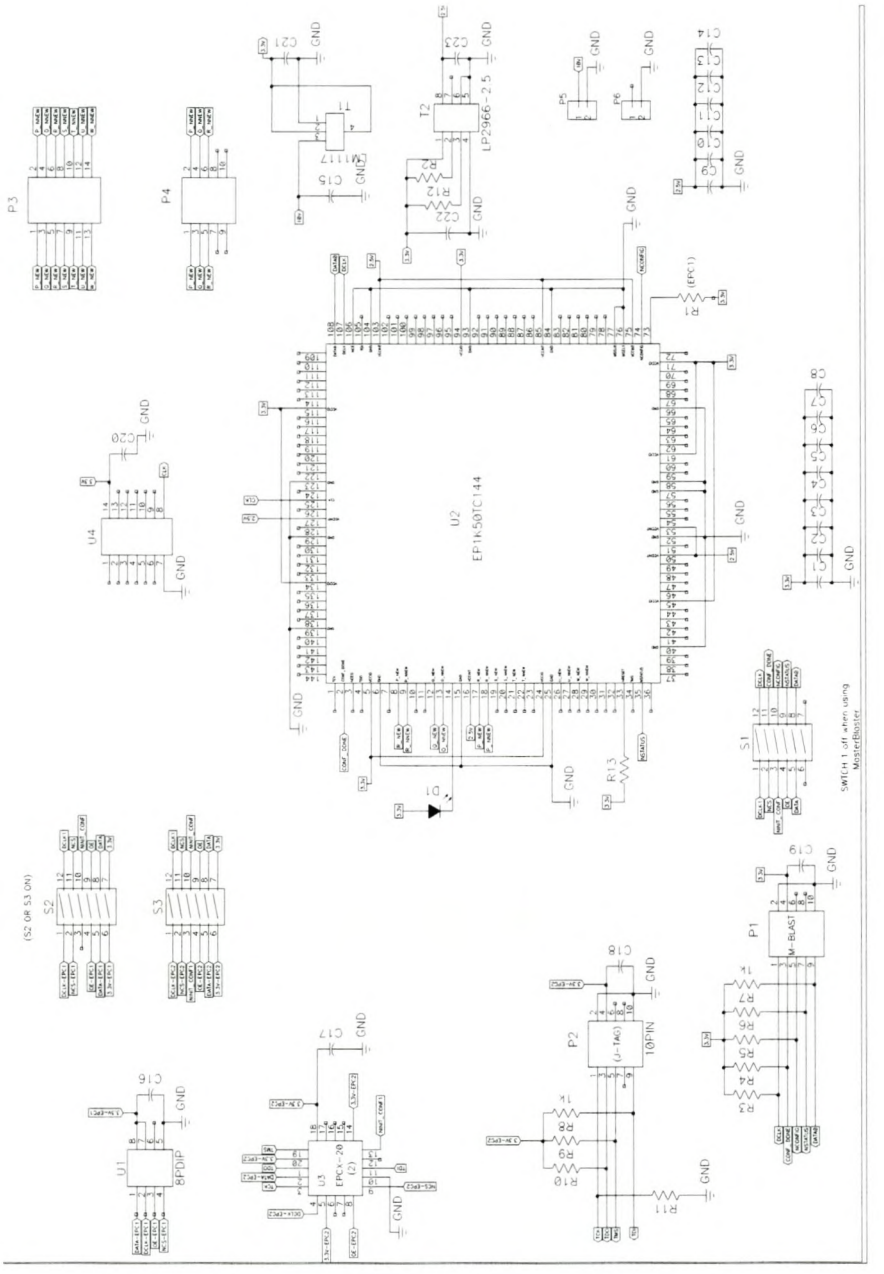

Figure C.2: *A PCAD schematic of the controller.*

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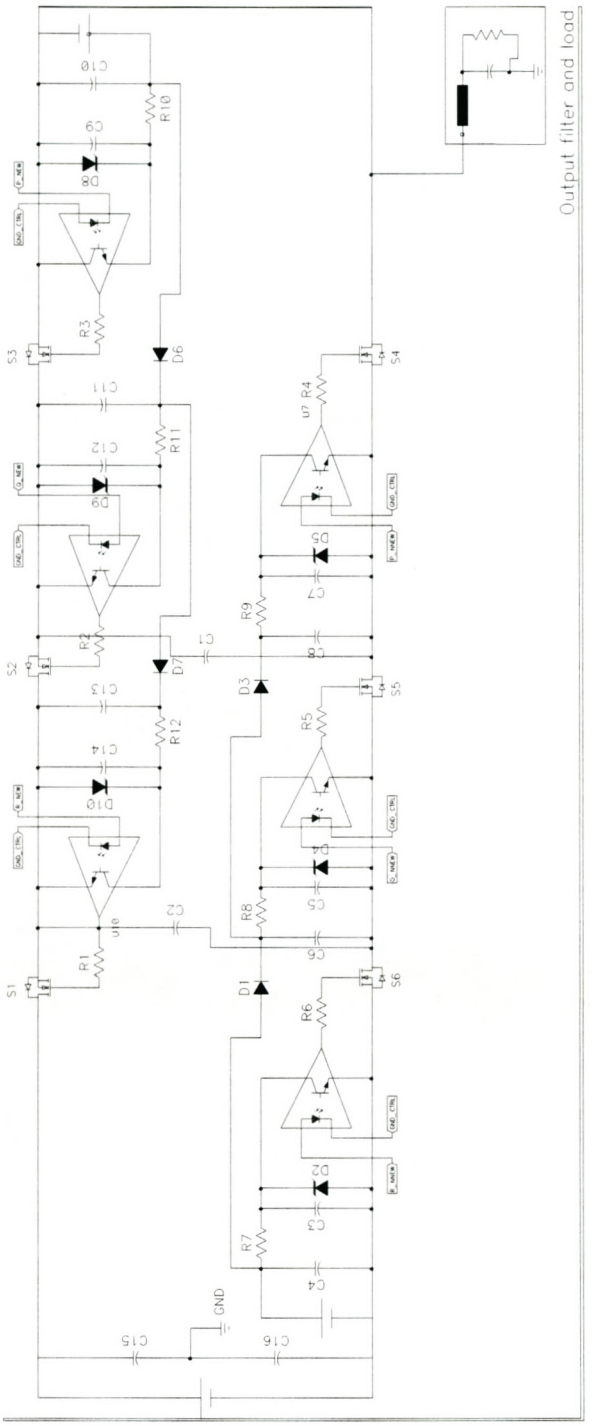

Figure C.3: *A PCAD schematic of the power stage with bootstrap power supplies.*