

## Calhoun: The NPS Institutional Archive

---

[Theses and Dissertations](#)

[Thesis Collection](#)

---

1968

# Radiation effects on metal-oxide-silicone field-effect transistors.

Olson, Phillip Roger

Monterey, California. Naval Postgraduate School

---

<http://hdl.handle.net/10945/12937>



Calhoun is a project of the Dudley Knox Library at NPS, furthering the precepts and goals of open government and government transparency. All information contained herein has been approved for release by the NPS Public Affairs Officer.

Dudley Knox Library / Naval Postgraduate School  
411 Dyer Road / 1 University Circle  
Monterey, California USA 93943

<http://www.nps.edu/library>

NPS ARCHIVE  
1968  
OLSON, P.

RADIATION EFFECTS ON METAL-OXIDE-SILICON  
FIELD-EFFECT TRANSISTORS

PHILLIP ROGER OLSON

DUDLEY KNOX LIBRARY  
NAVAL POSTGRADUATE SCHOOL  
MONTEREY CA 93943-5101









RADIATION EFFECTS ON METAL-OXIDE-SILICON  
FIELD-EFFECT TRANSISTORS

by

Phillip Roger Olson  
Lieutenant, United States Navy  
B.S., Naval Academy, 1962

[Redacted]  
Submitted in partial fulfillment of the  
requirements for the degree of

MASTER OF SCIENCE IN PHYSICS

from the

NAVAL POSTGRADUATE SCHOOL  
June 1968

NPS ARCHIVE

1968

OLSON, P.

## ABSTRACT

Radiation effects on Metal-Oxide-Silicon Field-Effect Transistors are studied. A brief history of development, theory of operation and survey of previous radiation effect work is given. Previous work points to a charge buildup in the oxide layer and a possible increase in fast surface state density as being the causes of semi-permanent degradation. Experimental work was done using a Fairchild FI 100 p-channel MOSFET to determine the feasibility of studying radiation effects using available equipment as the Naval Postgraduate School. It was found that the study of charge buildup is feasible. Data obtained agreed qualitatively with previous results. Thermal annealing of a device after irradiation reduced the semi-permanent degradation significantly as is seen in previous work. Transient photocurrents produced in the oxide layer were examined and problems were revealed which must be solved before such work will become meaningful. Package and charge scattering effects may be masking the real effects. Suggestions for future work are included.

TABLE OF CONTENTS

	Page
1. Introduction	9
2. General Introduction to MOSFET'S	9
3. History	10
4. Theory of Operation	12
5. Previous Radiation Work	17
6. Experimental	24
7. Conclusions and Suggestions for Future Work	29
8. Bibliography	31



## LIST OF ILLUSTRATIONS

Figure	Page
1. Insulated-Gate Field-Effect Transistor	32
2. Basic Unipolar Transistor Structure	33
3. Inversion Layer Due to Ionization of Ambient Gases	34
4. Typical Conductance Characteristics of a P-Channel MOSFET	35
5. Typical Electrical Characteristics	36
6. Electrical Circuits and Equipment Data	37
7. Threshold Voltage vs. Irradiation Dose	38
8. Switching Characteristic Slope vs. Irradiation Dose	39
9. Photocurrent Pulse Shapes	40



TABLE OF SYMBOLS

$E(x)$	- electric field in the oxide layer at a distance $x$ from the source region
$d$	- oxide thickness
$V(x)$	- potential in the channel at a distance $x$ from the source
$V_G$	- gate potential
$\epsilon_{ox}$	- oxide dielectric constant
$V_T$	- gate threshold potential.
$\Delta V_T$	- transient change in gate threshold voltage
$\sigma_m(x)$	- mobile charge density in the channel a distance $x$ from the source region
$\Delta G$	- device conductance
$\Delta x$	- channel length
$w$	- channel width
$\mu$	- carrier mobility
$V_D$	- drain potential
$V_S$	- source potential
$I_{DS}$	- saturation value of drain current
$J/q$	- particle current of hole-electron pairs
$\Delta n$	- excess carrier density at the surface
$S$	- surface recombination velocity
$^{\circ}C$	- degrees Celsius
(D)	- drain
(S)	- source
(G)	- gate
(B)	- base substrate

#### ACKNOWLEDGEMENTS

I am grateful to Professors John N. Dyer and Fred R. Buskirk for the time they spent running the linear accelerator for my data taking. My thanks also go to LCDR Richard Slye and LT William Stark for assistance rendered and for the use of their "wheel" which aided my experimental work immensely. I wish also to express my appreciation to Professor William Reese for showing great perserverance and patience in sponsoring this work and to Lynwood F. May for a good deal of technical assistance.

## 1. INTRODUCTION

The increasing use of transistors and integrated circuits in environments where they are subjected to relatively high doses of radiation has made the study of radiation effects on these devices necessary. This paper will deal with the effects of radiation on Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFET'S). First a general introduction to the structure, nomenclature and manufacture of MOSFET's is given. This is followed by a presentation of the history of development, theory of operation, and previous radiation effect work on this device. The experimental section of the paper presents the results of radiation effect work done using the linear accelerator at the Naval Postgraduate School.

## 2. GENERAL INTRODUCTION TO MOSFET'S

The Metal-Oxide-Semiconductor Field-Effect-Transistor has characteristic curves analogous to those of a pentode vacuum tube. Its operation in a electric circuit, however is analogous to that of a triode vacuum tube in that the current between "source" (cathode) and "drain" (anode) is modulated by a bias potential applied in the "gate" (grid) circuit (see Fig. 1). Source and drain areas form p-n junctions with the substrate. These junctions are normally reverse biased. The bias applied to the gate induces a "channel" between source and drain. MOSFET'S are either n or p type depending on whether an n-type channel is formed in a p-type substrate or a p-type channel is formed in an n-type substrate. The channel is formed immediately below the silicon dioxide-silicon substrate interface and is much shallower than the silicon dioxide

layer thickness. Changing gate bias changes the conductivity of the channel and thus the current between source and drain can be modulated. This device has the desirable characteristics of a high impedance, excellent DC to high frequency response, high gain capabilities, and a simplified structure. These characteristics give this device great promise for useful applications in integrated circuits, both digital and linear.

P-channel MOSFET'S are made by diffusing p-type silicon areas (source and drain) in an n-type silicon substrate material leaving a channel between the p-type areas of 8 to 10 microns in length. The active surface of the silicon is then passivated by thermally growing a silicon dioxide layer on it. The layer is grown to a thickness of about  $1200\text{\AA}$ . The oxide is then masked, except over the source and drain areas with a photoresistive chemical and the oxide over the source and drain areas is etched away. After the photoresistive chemical is removed, the metal electrode material is evaporated on the gate, source and drain areas. Nichrome is the metal most used, however, gold, chrome, nickel and aluminum are also used.

### 3. HISTORY

In 1928 J.E. Lilienfeld observed that a large number of charge carriers of high mobility could be produced in semiconductor material surfaces by applying an electric field perpendicular to the surface. By replacing one metal plate of a capacitor with a semiconducting material Lilienfeld found he could modulate the charge on the semiconductor plate much more rapidly with a much lower electric field in the dielectric insulator than in a

conventional capacitor with two metal plates. In 1953 Lilienfeld in the United States and O. Heil in Great Britain received patents on a type MOS-capacitor.(1) However the lack of sufficient knowledge of the physics of surfaces and thin films and the great advances being made in the field of vacuum tubes left this work in the background.

In 1948 W. Shockley and G.L. Pearson investigated the effect of electric fields normal to a thin semiconductor film and found that surface electronic states served as traps for many charge carriers and hence decreased the conductivity of charges in a direction parallel to the semiconductor surface.(2) The invention of the bipolar transistor and its immediate success, however, again left this work in the background. Shockley kept working in the area, though, and in 1952 he proposed the unipolar transistor shown in Fig. 2.(3) A depletion region is produced by reverse biasing the p-n junctions. The undepleted region in the n-type material serves as a conducting channel for majority carriers between the source and drain ohmic contacts. Increasing or decreasing the reverse bias of the p-n junctions changes the depth to which the depletion layer extends into the n-type material and hence serves to modulate the current between source and drain by changing the effective resistance to charge carrier flow between source and drain. Since the depletion region extends far below the n-type material surface, the previous problem of reduced mobility due to surface state traps was overcome. A major drawback to this device, however, is that only depletion of charge carriers can be utilized because reversing the gate voltage polarity forward biases the p-n

junctions causing large currents to flow in the gate circuit. Since the enhancement mode of operation can not be used on this device, it is limited to small signal applications. This device also has a relatively low input impedance and depends on the bulk conduction properties of silicon.

In 1960 Kahng and Atalla were the first to propose a device in which a gate electrode, insulated from the semi-conductor material, would influence the conduction between two reversed biased p-n junctions.(1) The proposed device would depend for its operation on the surface conduction properties of the silicon rather than the bulk conduction properties.

In 1962 Hofstein and Heiman improved on all previous devices with their silicon insulated-gate field-effect transistor the basic design of which is used in the MOSFET today.(4) (See Fig. 1 and Section 4 for the detailed description.)

#### 4. THEORY OF OPERATION

The MOSFET depends for its action on the capability of modulating the surface conductivity of silicon by the application of an electric field normal to the conducting surface. Figure 1 shows a cross-section of a typical MOSFET illustrating the geometry used to effect the modulation. With no voltage applied to the gate, the surface conductivity of the n-type silicon between the source and drain regions will be the same as the bulk conductivity of the n type silicon. (This is true if we neglect the effect of the surface electron states in the forbidden energy gap. This effect will be discussed later.) Making the gate negative with respect to the substrate repels electrons from the silicon-silicon dioxide

surface leaving a net positive space-charge in the silicon surface due to the ionized donor atoms whose electrons have been repelled from the surface. As the gate potential is made more negative a point is reached where the silicon surface becomes intrinsic. At this point the positive charge in the surface is still essentially supplied by the ionized donors. Increasing the negative potential of the gate still more causes the positive space charge to be enhanced by mobile positive holes being attracted to the surface. The surface is now p-type as there are more holes than electrons present. The p-type layer induced by the electric field is called an inversion layer. The inversion layer has now created an ohmic connection between the heavily doped p-type source and drain regions. This connection is called the channel. Connecting the source directly to the substrate and biasing the drain negatively with respect to the source, will now cause holes to flow from source to drain through the conducting channel. Further increasing the negative potential of the gate increases the density of holes in the channel increasing the conductivity of the channel and hence increases the current between source and drain. With no voltage applied to the gate the silicon surface again becomes n-type establishing a reverse bias p-n junction between drain and substrate because of the negative potential being supplied to the drain. In this condition only a small leakage current flows in the drain circuitry. Thus the enhancement mode of operation gives a very definite on-off switching type of response to changes in gate potential which is very useful in logic circuits.

For a given gate voltage the potential in the channel becomes more negative as the drain is approached because of the ohmic nature of the channel. Thus the potential between the gate electrode and the silicon surface decreases along the channel and is a minimum at the drain region. It follows then that the conductance of the channel varies being a maximum near the drain. Making the drain continuously more negative will eventually cause a point to be reached where the channel region near the drain becomes intrinsic again. This occurs when the drain potential is made sufficiently negative to counteract the gate potential in the channel region near the drain. In this region of the channel the surface inversion layer has been replaced by a region of space charge. The occurrence of this condition is called "pinch off". Any further increase in the negative drain potential does not essentially cause any increase in drain current, it just causes the point in the channel at which pinch off occurs to move towards the source region. The drain current is now space-charge limited and is independent of drain potential. It can readily be seen that the values of drain current and potential at which pinch off takes place depend on gate potential.

At actual silicon surfaces surface states exist, due to the termination of the silicon crystal lattice, irregularities in the structure of the surface and contaminating impurities in the crystal. These surface states tend to immobilize captured electrons and hence the channel conductivity change for a given change in gate

potential will be less than if no surface states were present.(5)

Improved fabrication techniques and the passivation of the silicon surface by the silicon dioxide layer has made the effect of surface states small under normal operations and hence these effects will be neglected in the simplified theory given below.(6)

The development of the theoretical expression for drain current ( $I_D$ ) given here is essentially that presented by Heiman and Hofstein.(4) A more detailed analysis of the surface channel may be found in articles by G.T. Wright(7) and H.K.J. Ihantola and J.L. Moll.(8) The simplification of the following theoretical development results from the assumption that the silicon dioxide thickness between the gate electrode and the silicon surface is much larger than the depth of the inversion layer in the silicon surface. This assumption allows us to skip an analysis of the space charge conditions in the inversion layer and underlying silicon regions and assume that the entire voltage drop from gate to substrate occurs across the silicon dioxide layer. Using Fig. 1 to define the geometric factors, we have:

$$E(x) = \frac{V_G - V(x)}{d}$$

Where  $E(x)$  is the electric field in the oxide at a distance  $x$  from the source,  $d$  is the oxide thickness,  $V(x)$  is the potential in the channel at a distance  $x$  from the source, and  $V_G$  is the potential of the gate.

Since  $V_G$  is negative, a positive charge will be induced on the surface of the silicon. The total induced positive charge is equal to  $\epsilon_{ox} E(x)$ , where  $\epsilon_{ox}$  is the oxide dielectric constant.

$$\epsilon_{ox} E(x) = \epsilon_{ox} \frac{V_G - V(x)}{d}$$

Since it requires a gate potential  $V_T$  (threshold voltage) to just start inversion, the expression for mobile charge density ( $\sigma_m(x)$ ) in the channel is given by:

$$\sigma_m(x) = \frac{\epsilon_{ox}}{d} \left[ (V_G - V(x)) - V_T \right]$$

where  $(V_G - V(x)) \geq V_T$ .

The conductance ( $\Delta G$ ) of a section of the channel length  $\Delta x$  and width  $w$  is given by:

$$\Delta G = \frac{\sigma_m(x) \mu w}{\Delta x}$$

where  $\mu$  is the carrier mobility and is assumed to be constant.

Now:

$$I_D = (\Delta G) (\Delta V(x))$$

Therefore:

$$(I_D)(\Delta x) = \frac{\epsilon_{ox}}{d} \mu w V(x) \left[ (V_G - V_T) - V(x) \right]$$

Integrating along the length of the channel we get:

$$I_D = \frac{\epsilon_{ox} \mu w}{d} \left[ (V_G - V_T)(V_D - V_S) - 1/2(V_D^2 - V_S^2) \right] \quad (1)$$

Where  $V_D$  is the drain potential and  $V_S$  is the source potential.

As discussed above the condition for pinch off is  $(V_G - V_D) = V_T$  or  $V_D = (V_G - V_T)$ . Putting this expression into Equation (1) gives the saturation value of drain current ( $I_{DS}$ ) as a function of  $V_G$  and  $V_T$  when  $V_S = 0$ .

$$I_{DS} = \frac{\epsilon_{ox} \mu w}{l d} (V_G - V_T)^2 \quad (2)$$

The transconductance ( $g_m$ ) of this device in the space-charge-limited region of operation is defined as:

$$g_m = \frac{\partial I_{DS}}{\partial V_G}$$

Thus:

$$g_m = \frac{\epsilon_{ox} \mu w}{l d} (V_G - V_T)$$

## 5. PREVIOUS RADIATION WORK

In 1962 the work of D.S. Peck, R.R. Blair, W.L. Brown and F.M. Smits showed that the ionization of ambient gases caused changes in nonpassivated semiconductor characteristics.(9) These changes were attributed to the collection of the ions on the non-passivated semiconductor surfaces which induced surface inversion layers that changed the junction characteristics. (See Fig. 3) It was hoped that the passivation of the semiconductor surface by thermally growing a thin layer of silicon dioxide on it would solve the problems of the effects of ionizing radiation. This would mean that MOSFET'S should be relatively insensitive to ionizing radiation

because the silicon dioxide layer serves to passify the semiconductor surface by insulating the p-n junctions from the ambient as well as insulating the gate electrode from the semiconductor surface.

However in 1964 a study of the effects of gamma-rays from a  $\text{Co}^{60}$  source on silicon planar transistors by H.L. Hughes disclosed an appreciable amount of degradation in MOSFET characteristics.(10) He proposed that the major cause of this degradation was due to a buildup of mobile positive charge in the silicon dioxide layer. In a p-channel device operating in the enhancement mode this mobile positive space charge would tend to accumulate at the silicon dioxide-silicon interface causing the silicon surface layer to become more n-type and defeating, to a certain degree, the effect of the negative potential applied to the gate electrode. Shortly after Hughes' work A.G. Stanley investigated the effect of 1.5 MeV electrons on a p-channel MOSFET.(11) His results were similar to those of Hughes and could also be explained by the postulation of the formation of a mobile positive space charge by the incident electron beam. A.J. Speth and F.F. Fang observed in n-channel MOSFET irradiation in a 16 keV electron beam that the steady state threshold voltage shifts linearly with gate bias during irradiation.(12) This effect also was attributed to the buildup of a positive space charge in the silicon dioxide at the silicon surface whose magnitude is proportional to the gate bias applied during irradiation. J.R. Szedon and J.E. Sandor in studying the effects of low energy (10-20 keV) electron irradiation of metal-oxide-semiconductors explained the shift in capacitance of the devices under irradiation

in terms of a positive charge buildup in the oxide film as well as the production of fast surface states\* in the oxide at the silicon dioxide-silicon interface which serve as traps for the mobile charge carriers.(13) In all of the foregoing work the conclusions drawn by the researchers were qualitative and just extensive enough to explain the phenomena observed in each particular case.

In late 1966, however, E.H. Snow, A.S. Grove and D.J. Fitzgerald looked directly at the problems of positive charge buildup and production of fast surface states at the silicon dioxide-silicon interface in MOSFET'S caused by electron, X-ray and ultra-violet radiation.(14) In their investigation of a voltage shift of the capacitance versus voltage characteristics of a MOS capacitor, they found that there is in fact a charge buildup in the oxide layer and that "the radiation induced charge increases linearly with the voltage applied during irradiation and not with applied field". They also showed that the threshold voltage increase exhibited by MOSFETS during irradiation is caused by the charge buildup in the oxide layer. (See Fig. 4.) In advancing a model to explain the space charge formation, Snow and his collaborators incorporated the following experimental results:

1. Positive space charge forms in the oxide layer upon exposure to ionizing radiation.
2. Space charge buildup saturates with increasing dose.

The point of saturation is dose rate independent.

\*Fast surface states are electronic states with relaxation times of about  $10^{-7}$  seconds.

3. The magnitude at which the space charge saturates depends on the gate voltage applied during irradiation. It is independent of oxide thickness.
4. The magnitude of the space charge at saturation is independent of type and orientation of silicon.
5. Etching experiments indicate that the space charge in the oxide layer forms near the silicon dioxide-silicon interface.(15)
6. The space charge formed during irradiation is neutralized if electrons are introduced into the oxide layer either by photoemission from the metal electrode of the silicon substrate, or introduced by thermal annealing.

The model presented to explain these results requires the space charge buildup to occur when the ionizing radiation produces electron-hole pairs with the electrons, for the most part, being swept from the oxide layer by the gate bias leaving the less mobile holes to be trapped in the oxide layer. In the absence of any gate bias the electrons remain in the oxide to recombine with the holes leaving fewer uncompensated holes to be trapped and hence a smaller space charge buildup results.

To establish the spatial distribution of positive charges induced in silicon dioxide by ionizing radiation, Zaininger irradiated unbiased Me-SiO<sub>2</sub>-Si capacitors with 10<sup>15</sup> electrons per cm<sup>2</sup>.(15) He then etched away successive layers of silicon dioxide of known thicknesses. As each layer was removed, the oxide charge was measured using the mercury probe technique. Zaininger found that almost

all of the positive charge was located within  $100\text{\AA}$  of the silicon dioxide-silicon interface. In this region the radiation induced electrons can escape directly to the silicon even without an applied field. To explain the fact that positive charge appears at the silicon dioxide-silicon interface also when a negative bias is applied as well as to explain the rest of the experimental results, it is assumed that a high density of hole traps exists near the silicon dioxide-silicon interface with this density decreasing rapidly away from the interface. Thus in the case of an electron-hole pair produced near the silicon dioxide-silicon interface, the electric field produced by the negative gate bias will sweep the electron from the oxide but the hole will not travel far before it is captured in the high density of hole traps. Whereas in the case of the electron-hole pair produced near the metal electrode-oxide interface, the electron will still be swept from the oxide by the electric field but the hole will have a good chance of getting to the metal electrode to recombine with a free electron because the few hole traps in this region fill very rapidly.

On the subject offast surface states Snow et al., showed by the measurement of reverse currents across one p-n junction of a MOSFET that surface recombination velocity\* increased during irradiation. Since the surface recombination velocity is directly

\*The particle current,  $J/q$ , of hole-electron pairs combining at the surface per  $\text{cm}^2$  per second is proportional to the excess carrier density at the surface,  $\Delta n$ . That is  $J/q = S\Delta n$  where the constant of proportionality,  $S$ , has the dimensions of velocity and is called the surface recombination velocity.

proportional to the density of fast surface states, the density of fast surface states would seem to increase during irradiation. No model is presented, however, to explain this phenomena as a decrease in carrier mobility at the surface would give the same results and at this time the effect of irradiation on carrier mobility at the surface is not well known.

The majority of the work cited thus far has acknowledged that the effect of radiation on MOSFETS is a sensitive function of the efect structures of the oxide but say little more. Kooi(16) Hofstein(17) and Dennehy et al.,(18) have studied this problem in detail and agree on the fact that the method of preparation is the major factor in determining the differences between different MOSFETS but what step or steps in the processes are responsible are not yet known. More work needs to be done in this area before any good correlation of data between MOS devices whose silicon dioxide layers were prepared differently can be made.

In late 1967 D.M. Long and R.D. Baer reported on transient effects in MOSFET'S due to X-ray and electron irradiation.(19) The X-rays were delivered at dose rates of  $4 \times 10^7$  rads per second and  $1.5 \times 10^{11}$  rads per second. The electrons, produced in a linear accelerator, were delivered at a dose rate of  $1 \times 10^9$  rads per second. Long and Baer found two types of transient response: (1) production of a primary photocurrent at each p-n junction in a device and (2) a transient change in the threshold voltage ( $\Delta V_T$ ) of the device. The peak photocurrent was found to vary approximately linearly with dose rate and in the range of -0.10 ma to 300 ma for p-channel enhancement mode devices. The range was limited by

the dose rates used. Long and Baer attributed  $\Delta V_T$  to the generation of carriers in the channel of the device. They found that  $\Delta V_T$  varied less than linearly with dose rate in the range of 40 to 50 mv for p-channel enhancement mode devices. Again the range was limited by the dose rates used.

It was also found that device package response is significant when studying transient effects. To look at this effect Long and Baer fabricated a dummy device by depositing the same metallization pattern used for MOSFET'S on a thick oxide layer covering a silicon chip. Leads into the device were connected as they are in real devices and transient current flow in these leads was measured during irradiation. The authors suggest that the current flow is due to electrons liberated from the encapsulated gas during irradiation providing a current path from the leads to the can of the device. They found that a positively biased lead showed a significantly larger response than a negatively biased lead. This is due to the fact that a positive lead readily attracts the liberated electrons whereas a negative lead repels the electrons and forms a space charge region around the lead which limits the current. The peak current is bias and dose rate dependent varying between  $10^{-5}$  and  $10^{-2}$  amps for a negatively biased lead. A second package phenomena found was an interaction current between two leads. The applied voltage to one lead can change the radiation induced current in the adjacent lead. This effect is not seen with a negatively biased lead because of its space charge buildup but positively biased leads attempt to draw electrons from a common volume of ionized gas resulting in a reduction of current to each

lead compared to the case where each or one of the leads is grounded. The maximum effect occurs for two equally biased positive leads and results in a transient current reduction of approximately 15%. A third package effect is charge scattering from device leads. However transient currents from charge scattering are of the order of  $10^{-14}$  to  $10^{-13}$  amps per rad per second and are negligible compared to other effects.

## 6. EXPERIMENTAL

The purpose of the experimental work done was to determine the feasibility of studying radiation effects on MOSFET'S using available equipment at the Naval Postgraduate School.

The particular MOSFET used in this work was the Fairchild FI 100, a silicon Planar II device designed for enhancement mode operation. Planar II refers to the fabrication process which is said to prevent ion migration in planar oxides under the influence of high electric field intensities (e.g.  $2 \times 10^6$  volts/cm). Typical electrical characteristics for this device are shown in Fig. 5.

The devices were irradiated in the beam of the Naval Postgraduate School linear accelerator which produces 80 Mev electrons with a peak beam current of 2.8 micro-amps delivered in pulses of one micro-second duration at a rate of 60 pulses per second. When the beam intensity is 2.8 micro-amps a dose of  $5.8 \times 10^3$  rads per pulse is being delivered to a silicon target.

The photocurrent produced between the gate and substrate in the oxide layer of a particular device and the change in switching characteristics of the device were monitored during irradiation

with the equipment and circuits shown in Fig. 6. The measurements made concentrated attention on effects in the oxide layer of MOSFET'S.

The change in  $V_T$  with increasing dose is a direct indication of charge buildup with increasing dose. Figure 7 shows  $V_T$  as a function of dose for two different cases. In Case 1 the device was being switched at a rate of one kilo-Hertz while the drain junction was continuously biased at -3 volts. In Case 2 the device had no bias potentials applied to either drain or gate during irradiation. The actual voltage applied to the gate of the device in Case 1 was zero for one half of the ramp generator cycle and then increased linearly to -20 volts during the remaining half of the cycle. Since the beam was only on for a micro-second every 1/60th of a second, chances are there were relatively few coincidences of a voltage being applied to the gate when a beam pulse arrived. During the run for Case 2 difficulties were experienced in maintaining a steady linear accelerator beam current. Thus the data presented for this run can only be used to show a general trend. In both cases the change in threshold voltage, which is a measure of charge buildup in the oxide layer, increases rapidly at low doses and increases slowly with increasing dose at high total doses. Data taken at  $10^8$  rads (not shown on Fig. 8.) indicates this trend continues at very high total doses. The total dose dependence of charge buildup seen here agrees qualitatively with the effects seen by Snow et al.(14) and A.G. Stanley(11) in their work on MOS devices and indicates that the study of charge buildup in MOSFET'S is feasible. Figure 8 shows the relationship

between the switching characteristic curve slope and total irradiation dose for the two cases described above. Again because of the linear accelerator beam instability during Case 2 only general trends are to be noted and no attempt was made to fit all the points with a curve. Snow et al., also report the decrease in slope with increasing irradiation dose. As pointed out in Section 5 and Fig. 4, this change in slope could be due to either an increase in the density of fast surface states or a decrease in carrier mobility. Further study of this phenomena is needed to resolve the ambiguity.

Thermal annealing one of the irradiated devices for three hours at  $150^{\circ}\text{C}$  reduced the change in  $V_T$  due to irradiation by 40%. Snow et al., and Szedon and Sandor also observed a reduction in radiation effects on charge buildup with thermal annealing after irradiation. Snow et al., were able to anneal 70% of the change in  $V_T$  in ten minutes at  $300^{\circ}\text{C}$ . Szedon and Sandor were able to fully anneal their MOS devices in 15 minutes at  $150\text{-}200^{\circ}\text{C}$ . Agreement with this previous data is not to be expected however. It seems that thermal annealing provides enough energy to electrons in the substrate to allow them to migrate into the oxide layer and combine with trapped holes. In the previous work low energy radiation was used to cause the charge buildup whereas in the present work high energy electrons were used which indicates that a different type of damage is caused by the higher energy radiation. Specifically it would indicate that the traps formed are associated with deeper energy levels or that the damage produced is much more extensive.

The work published so far on the transient effects of radiation on MOSFET'S has dealt with the primary photocurrent produced in the p-n junctions of the device. Here we have attempted to look at the photocurrent in the oxide layer of the device. Peak photocurrents of the order of  $3 \times 10^{-5}$  amps were observed when the gate electrode was negatively biased at -3 volts. With the gate positively biased at +3 volts, peak photocurrents of the order of  $2 \times 10^{-4}$  amps were observed. Doubling the magnitude of negative bias doubled the photocurrent observed indicating a linear relationship between photocurrent and negative bias potential.

Figure 9 illustrates the behavior of the photocurrent in time. The negative peak seen when a negative bias is applied to the gate is probably due to electrons being scattered from the device can and being picked up by the gate lead. This would cause a current to flow in the photocurrent monitoring circuit in a direction opposite to that of the photocurrent produced in the oxide layer. When a positive bias is applied to the gate, the current produced by the scattered electrons is in the same direction as the photocurrent and hence no negative peak is seen. By decreasing the electron beam intensity the dose rate was decreased and a decrease in the magnitude of the negative peak discussed above was observed. The decrease was much less than linear. Irradiation of an empty socket produced a trace similar to that seen in Fig. 9 in shape but about 1/5th the magnitude. The socket effects were found to be bias and polarity independent.

The above results relating bias polarity, bias magnitude and dose rate to peak photocurrent are discussed in general only because a lack of sufficient data precludes their discussion in detail. Linear accelerator run time was curtailed by breakdowns and other commitments hence only exploratory data could be taken prior to this writing. Another factor which may be involved here is package effects. Long and Baer observed package effects whose magnitude would be quite significant compared with the magnitudes observed here. They observed photocurrents in their dummy device of the order of  $2 \times 10^{-3}$  amps for a negatively biased lead and  $5 \times 10^{-3}$  amps for a positively biased lead. Their data was taken at a dose rate of  $2.3 \times 10^{10}$  rads per second from 55 MeV electrons. Since the present data was taken at a dose rate of  $2.7 \times 10^5$  rads per second from 80 MeV electrons, the difference between the peak photocurrent in the positively biased lead and that in the negatively biased lead could very easily be due to package effects. The fact that the magnitude of the negative peak seen in the case of a negatively biased gate lead varies with bias magnitude is not in agreement with the space charge buildup hypothesis of Long and Baer and should be checked more closely. An attempt to determine the actual package effects encountered was made by evacuating a device can to  $10^{-5}$  microns of mercury. Inserting a capillary tube through a hole drilled in the side of the can, however, dislodged the gate lead from its contact and the device would not function under normal conditions. Again limited time and accelerator availability prevented further attempts.

The decay times of the oxide photocurrents for two different devices with a negative bias applied to the gate were quite different even though the magnitudes were similar. In one case the decay time was quite similar to the decay time of the positively biased gate photocurrent and in the other case it was considerably longer. The pulse shape shown in Fig. 9 is an average of the two cases. Further study is needed to determine the reason for this difference but it is most likely due to manufacturing differences in the two devices.

## 7. CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

The study of charge buildup in the MOSFET oxide layer is feasible with available equipment. The fact that charge buildup is dose rate independent and that the linear accelerator is capable of high dose rates means that a large amount of data could be gathered in a relatively short period of time which could be used to statistically verify or refute the present hypothesis of charge buildup given in Section 5. More data on the variation of the switching characteristic curve slope with increasing irradiation dose might shed some light on the variation of the density of fast surface states with dose if and when more is known about the variation of carrier mobility with dose. Measurements of changes in fast surface state densities by measuring the change in capacitance across a silicon dioxide layer have been made by Szedon and Sandor.(13) Measurements of the change in capacitance between the gate and substrate of a MOSFET with increasing dose should provide the same information and could be used in conjunction with the switching characteristic curve slope change observations to learn more about the effect of fast surface state density on the slope changes.

Irradiation of a working device with an evacuated can would indicate whether the general results observed here are meaningful in regard to photocurrents and hence indicate if further work in this area would be fruitful. Also irradiation of devices whose cans have been removed would indicate the relative effect of charge scattering from the can in the electron beam.

It would be possible to measure the decay rate of the photocurrent pulse produced if the time duration of the electron pulse could be shortened from  $10^{-6}$  seconds to approximately  $10^{-7}$  seconds. The phenomena associated with photocurrent decay have a relaxation time in the neighborhood of  $10^{-7}$  seconds and hence with an electron pulse duration of  $10^{-6}$  seconds the observed photocurrent decay rate is dependent on the decay of the electron pulse.

## BIBLIOGRAPHY

1. F.P. Heiman and S.R. Hofstein, Electronics, 37, 50 (1964).
2. W. Shockley and G.L. Pearson, Phys Rev., 74, 232 (1948).
3. W. Shockley, Proceedings of the IRE, 40, 1365 (1952).
4. S.R. Hofstein and F.P. Heiman, Proceedings of the IEEE, 50, 1190 (1963).
5. L.V. Azaroff and J.J. Brophy, Electronic Processes in Materials, (New York, 1963), pp. 223-226.
6. J. Lindmayer and C.Y. Wrigley, Fundamentals of Semiconductor Devices, (New York, 1965), p. 320.
7. G.T. Wright, Solid State Electronics, 7, 167 (1964).
8. H.K.J. Ihantola and J.L. Moll, Solid State Electronics, 1, 423 (1964).
9. D.S. Peck, R.R. Blair, W.L. Brown and F.M. Smits, Bell System Technical Journal, 42, 95 (1963).
10. H.L. Hughes, IEEE Transactions on Nuclear Science, NS-12, 53 (1965).
11. A.G. Stanley, Proceedings of the IEEE, 53, 628 (1965).
12. A.J. Speth and F.F. Fang, Applied Physics Letters, 7, 145 (1965).
13. J.R. Szedon and J.E. Sandor, Applied Physics Letters, 6, 181 (1965).
14. E.H. Snow, A.S. Grove and D.J. Fitzgerald, Proceedings of the IEEE, 55, 1168 (1967).
15. K.H. Zaininger, IEEE Transactions of Nuclear Science, NS-13, 237 (1966).
16. E. Kooi, IEEE Transactions on Electron Devices, ED-13, 238 (1966).
17. S.R. Hofstein, IEEE Transactions on Electron Devices, ED-13, 222 (1966).
18. W.J. Dennehy, G.J. Brucker, A.G. Holmes-Siedle, IEEE Transactions on Nuclear Science, NS-13, 273 (1966).
19. D.M. Long, R.D. Baer, Research and Development Report ECOM-01520-F, pp. 91-126 (1967).

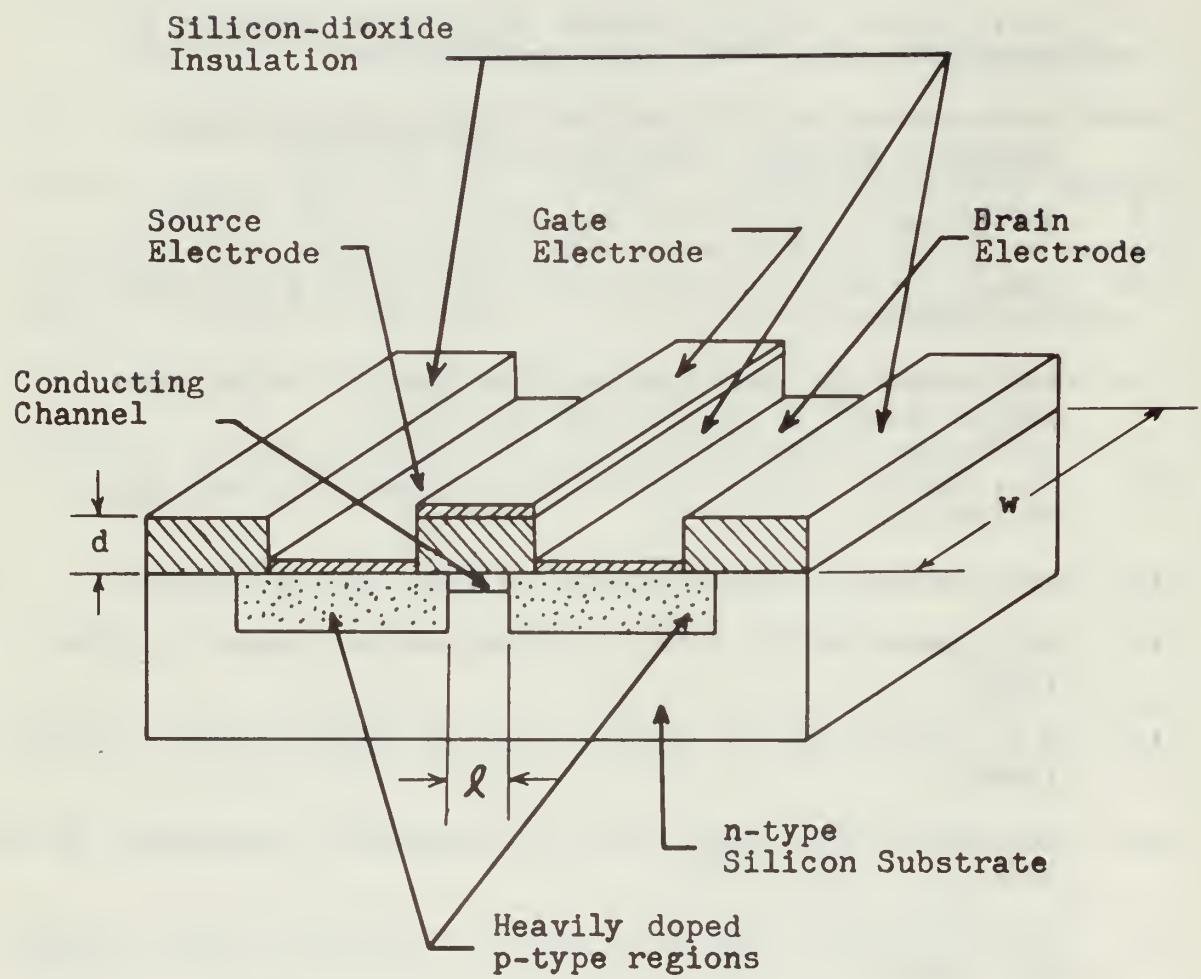


Fig. 1. INSULATED-GATE FIELD-EFFECT TRANSISTOR

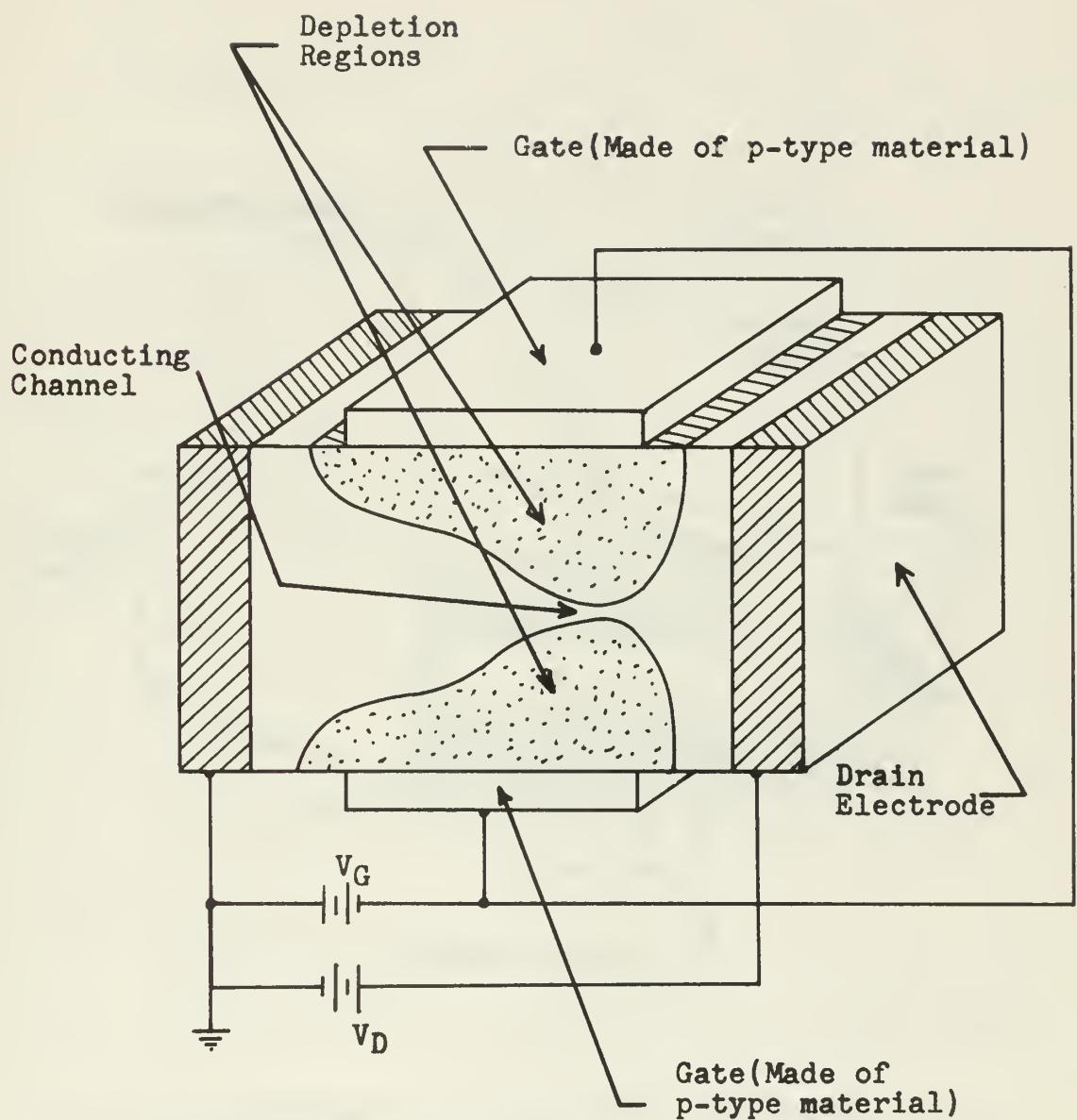


Fig. 2. BASIC UNIPOLAR TRANSISTOR STRUCTURE

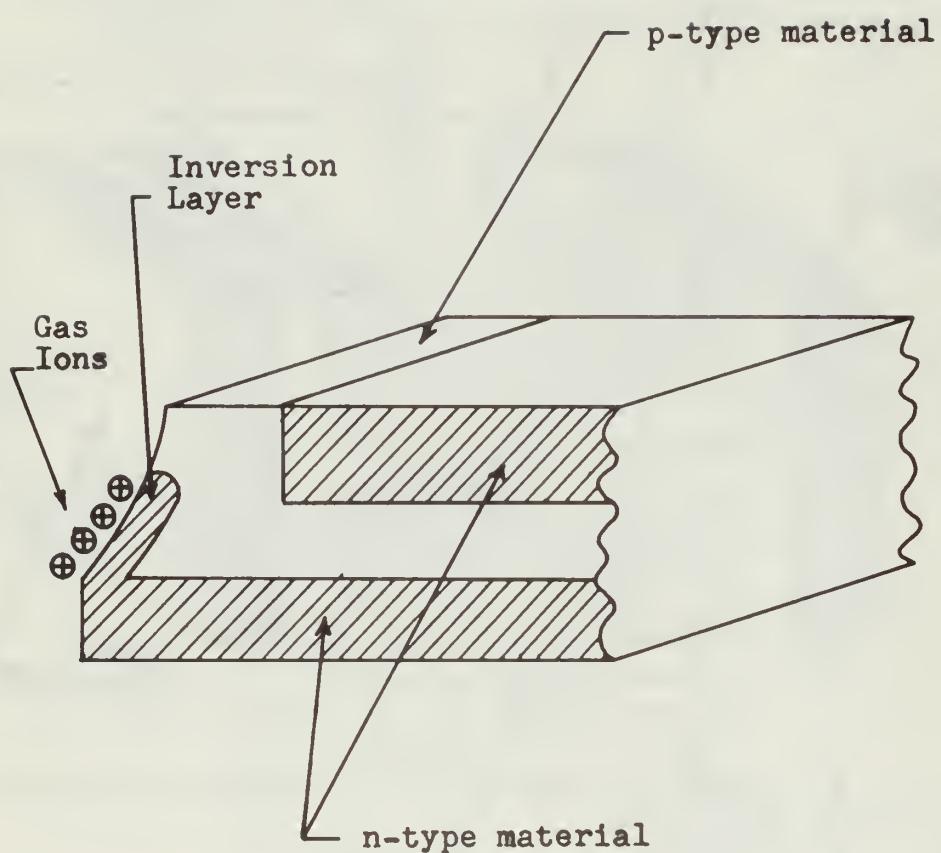
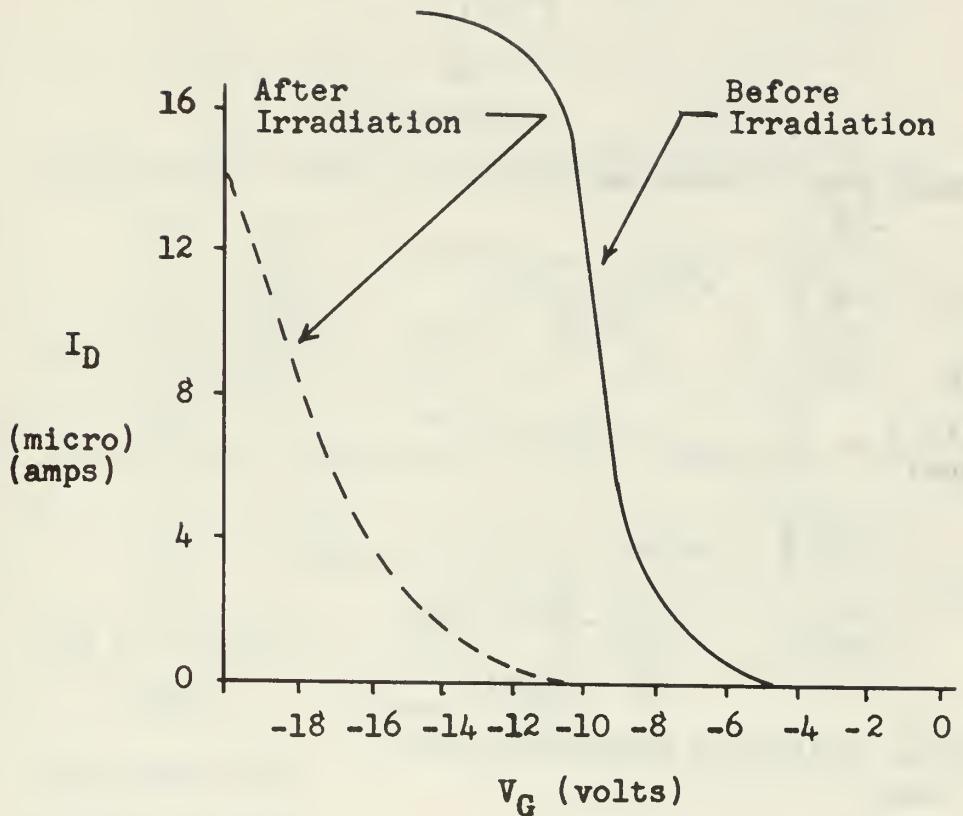


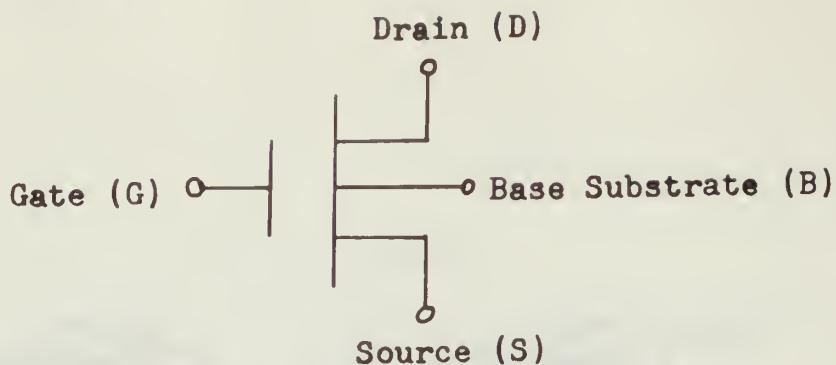
Fig. 3. INVERSION LAYER DUE TO IONIZATION OF AMBIENT GASES



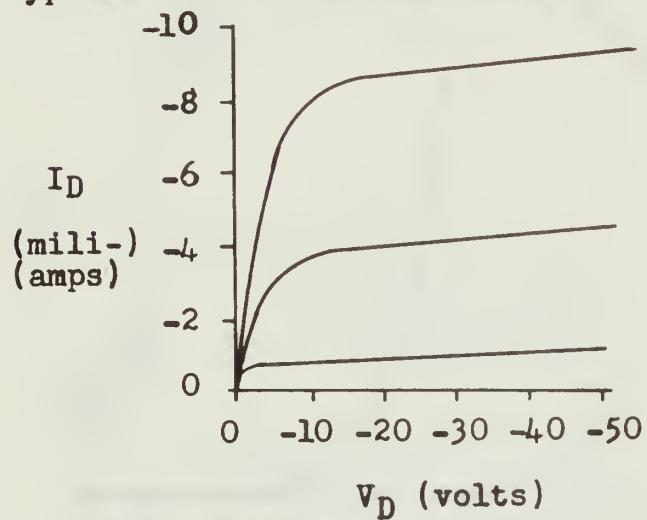
The decrease in slope after irradiation is most likely due to an increase in fast surface state density but a decrease in carrier mobility at the silicon dioxide-silicon interface would give the same effect.

Fig. 4. CONDUCTANCE CHARACTERISTICS OF A P-CHANNEL MOSFET

### Electrical Symbol



### Typical Drain Characteristics



### Typical Switching Characteristics

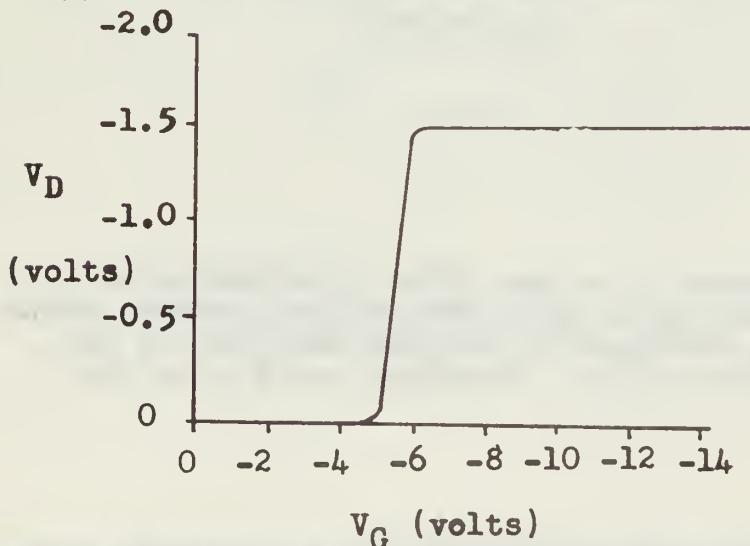
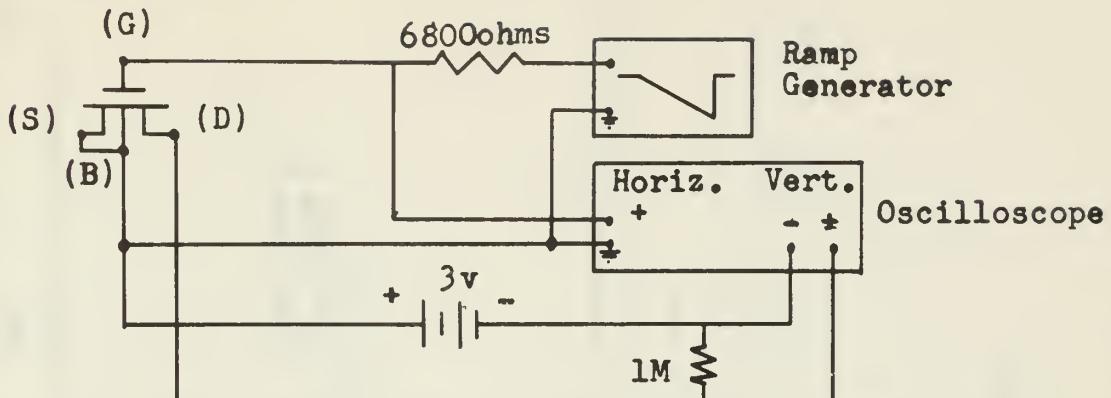
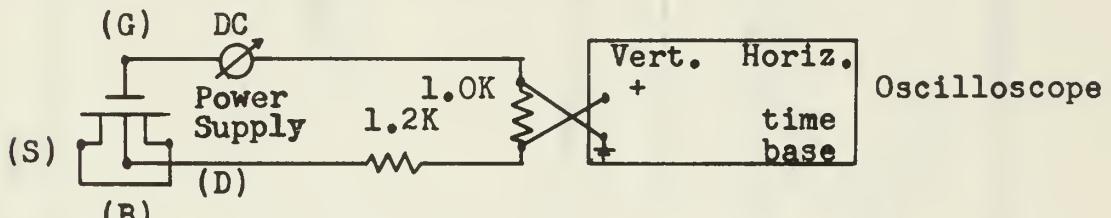


Fig. 5. TYPICAL ELECTRICAL CHARACTERISTICS

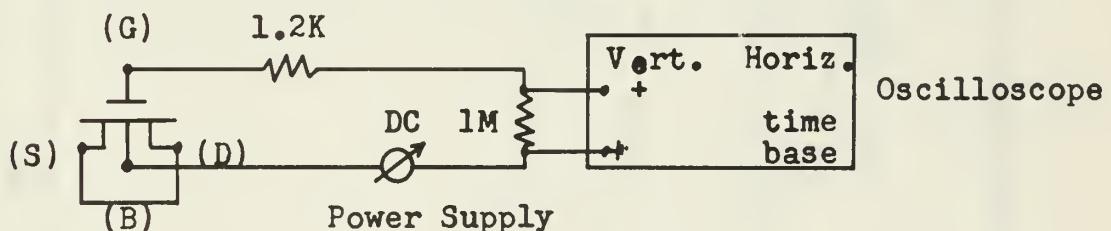
### Switching Circuit



Photocurrent Monitoring Circuit (Positive Bias)



Photocurrent Monitoring Circuit (Negative Bias)



### Equipment Data

#### Oscilloscope:

Tektronix type RM 503

Horiz. and vert. amplifier ranges - 1mv/cm to 2v/cm

Sweep rate range - 1 micro-second to 5 seconds

Input impedance - 1 megohm in parallel with 47 micro-micro farads

#### Ramp Generator:

Wavetek model 116 multi-purpose VCG

Output imped. - 50 Ohms

#### Power Supply:

Hewlett Packard model 721A

Voltage range - 0 to 30v dc, continuously variable

Output imped. - 0.2ohms in series with 30micr-henries

Fig. 6. ELECTRICAL CIRCUITS AND EQUIPMENT DATA

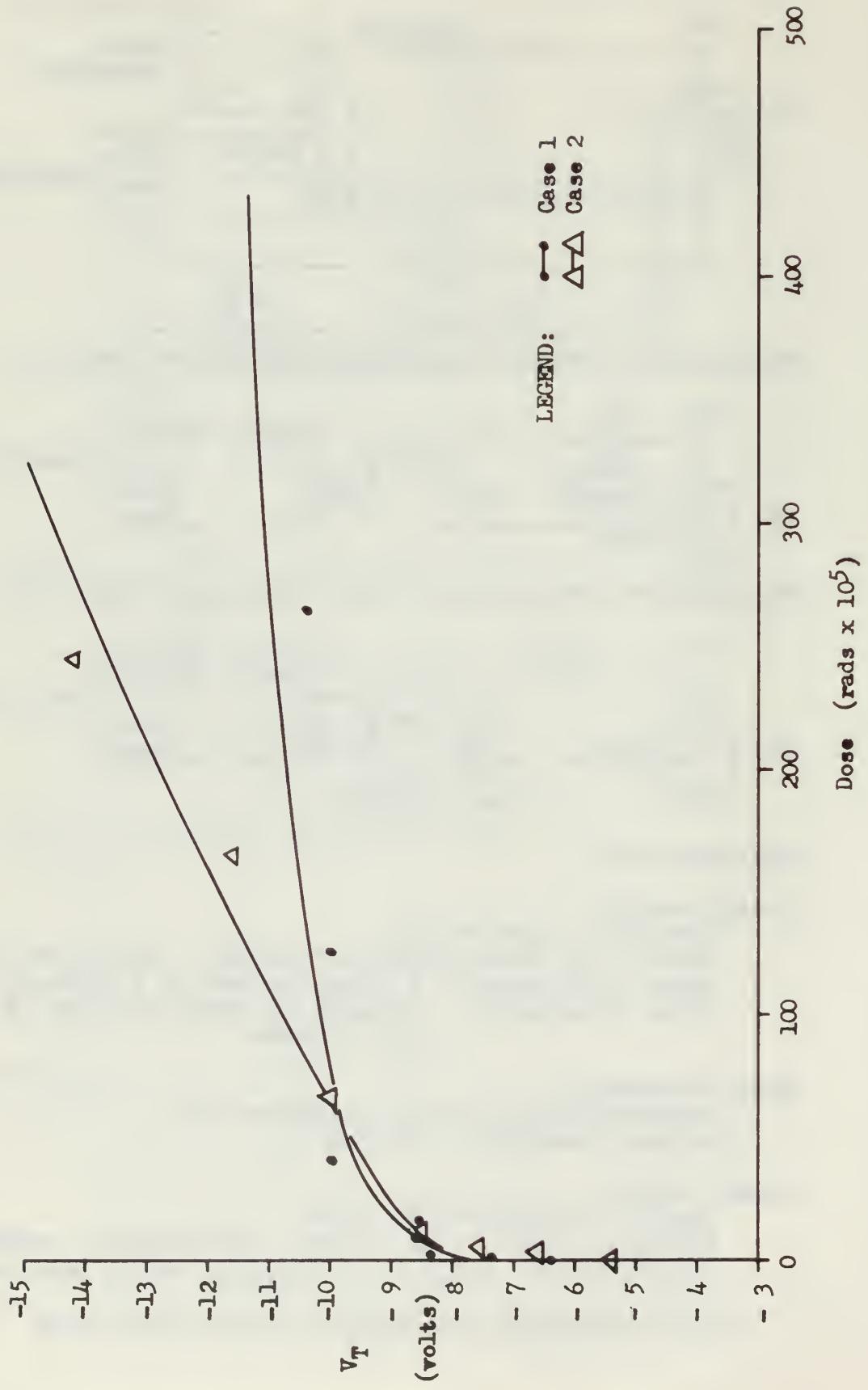


Fig. 7. THRESHOLD VOLTAGE vs. IRRADIATION DOSE

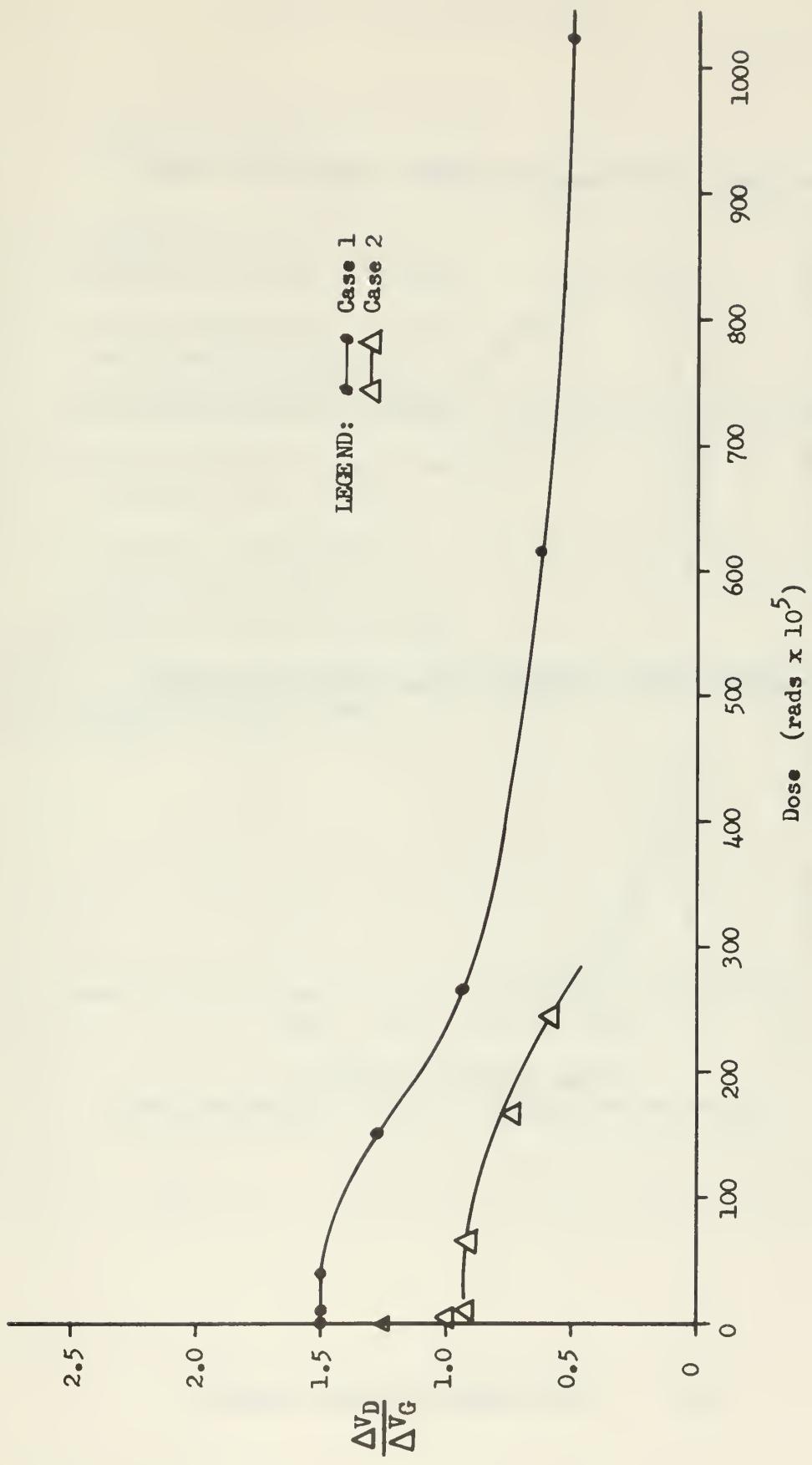
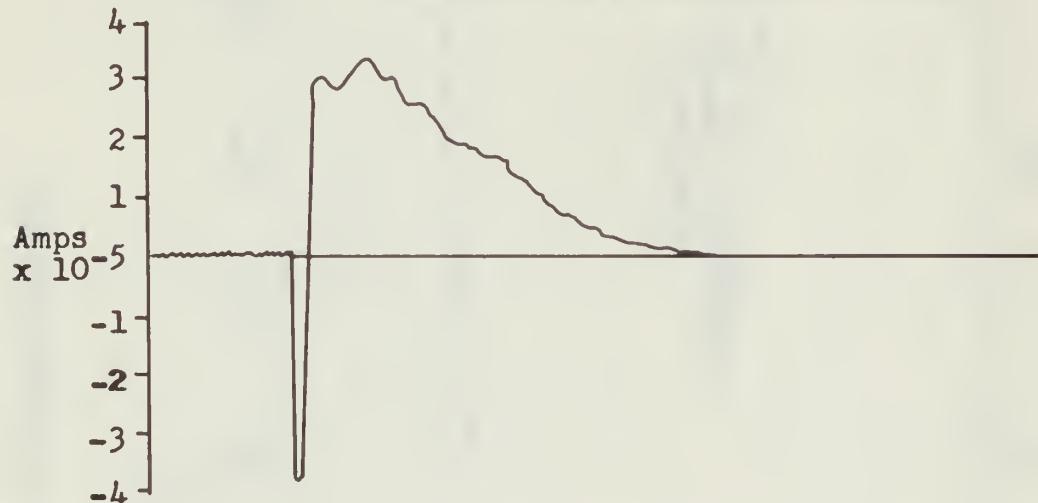
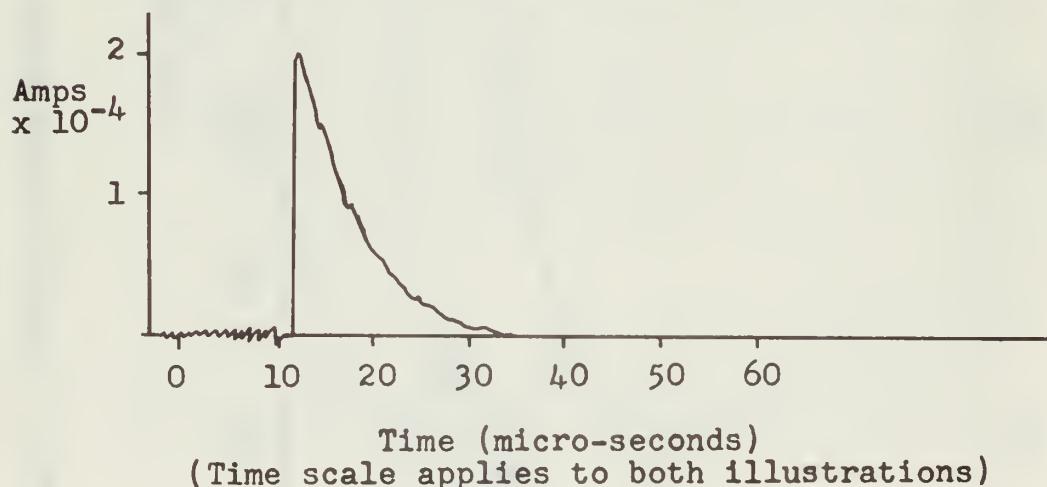


Fig. 8. SWITCHING CHARACTERISTIC SLOPE vs. IRRADIATION DOSE

Photocurrent With Negative Bias Applied to Gate



Photocurrent With Positive Bias Applied to Gate



Time (micro-seconds)  
(Time scale applies to both illustrations)

Fig. 9. PHOTOCURRENT PULSE SHAPES

INITIAL DISTRIBUTION LIST

	No. Copies
1. Defense Documentation Center Cameron Station Alexandria, Virginia 22314	20
2. Library Naval Postgraduate School Monterey, California 93940	2
3. Physics Department Library Department of Physics Naval Postgraduate School Monterey, California 93940	1
4. Defense Atomic Support Agency Washington, D.C. 20305	1
5. Professor William Reese Department of Physics Naval Postgraduate School Monterey, California 93940	2
6. Lieutenant Phillip R. Olson, USN 17950 Saticoy Street Reseda, California 91335	1



## UNCLASSIFIED

Security Classification

## DOCUMENT CONTROL DATA - R &amp; D

Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1 ORIGINATING ACTIVITY (Corporate author) Naval Postgraduate School Monterey, California		2a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED
		2b. GROUP N/A
3 REPORT TITLE Radiation Effects on Metal-Oxide-Silicon Field-Effect Transistors		
4 DESCRIPTIVE NOTES (Type of report and inclusive dates) Thesis, MS, June 1968		
5 AUTHOR(S) (First name, middle initial, last name) Olson, Phillip R., LT, USN		
6 REPORT DATE June 1968	7a. TOTAL NO. OF PAGES 41	7b. NO. OF REFS 19
8a. CONTRACT OR GRANT NO. N/A	9a. ORIGINATOR'S REPORT NUMBER(S) N/A	
b. PROJECT NO.  c.  d.	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report) N/A	
10. DISTRIBUTION STATEMENT <del>This document is subject to special export controls and each transmittal to foreign nations may be made only with prior approval of the Naval Postgraduate School.</del>		
11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY Naval Postgraduate School	
13 ABSTRACT Radiation effects on Metal-Oxide-Silicon Field Effect Transistors are studied. A brief history of development, theory of operation and survey of previous radiation effect work is given. Previous work points to a charge buildup in the oxide layer and a possible increase in fast surface state density as being the causes of semi-permanent degradation. Experimental work was done using a Fairchild FI 100 p-channel MOSFET to determine the feasibility of studying radiation effects using available equipment at the Naval Postgraduate School. It was found that the study of charge buildup is feasible. Data obtained agreed qualitatively with previous results. Thermal annealing of a device after irradiation reduced the semi-permanent degradation significantly as is seen in previous work. Transient photocurrents produced in the oxide layer were examined and problems were revealed which must be solved before such work will become meaningful. Package and charge scattering effects may be masking the real effects. Suggestions for future work are included.		

**UNCLASSIFIED**  
Security Classification

14  KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
MOSFET						
Space Charge Buildup						
Channel Conductivity						
Oxide Photocurrent						
Transient Effects						
Inversion Layer						











thes054  
Radiation effects on metal-oxide...  
DUDLEY KNOX LIBRARY



3 2768 00421953 5

DUDLEY KNOX LIBRARY