Complementary Resistive Switches

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Kurzfassung

Die Größenreduktion von Transistoren ist einer der Hauptgründe für die Leistungssteigerung von Computersystemen in den letzten Jahrzehnten. Da das Skalierungspotential von Transistoren in den nächsten Jahren an seine Grenzen stoßen wird, werden alternative Technologien, die geringeren Flächenverbrauch aufweisen und weitergehendes Skalierungspotential besitzen, benötigt. Den geringsten Flächenbedarf versprechen passive Speichermatrizen ($4F^2$), welche in Kombination mit resistiven Schaltern (auch Memristoren genannt) als Matrixelemente die Realisierung höchstintegrierter Speicher und -Logikanwendungen ermöglichen.
Resistive Schalter sind zweipolige Bauelemente, zeichnen sich durch ein nichtflüchtiges Schalten des Widerstandwertes durch kurze Spannungspulse aus und sind auf Grund des einfachen geschichteten Aufbaus leicht zu fertigen. Desweiteren besitzen diese Bauelemente sehr gute Verlustleistungseigenschaften, die allerdings bei Verwendung in einer passiven Speichermatrix verlorengehen. Dies liegt an dem Auftreten von parasitären Strompfaden, die neben einer drastischen Erhöhung der Verlustleistung auch das Auslesen in einer Matrix erschweren bzw. unmöglich machen. Als Lösungsmöglichkeit wurde bisher der Einbau eines Auswahlelements mit einer diodenähnlichen Charakteristik diskutiert. Dieser Ansatz ist allerdings mit bipolaren resistiven Schaltern, u.a. aufgrund der erforderlichen Stromdichten, nur schwer zu realisieren.
Als neuer Ansatz wird deshalb im Rahmen dieser Arbeit die Verwendung von komplementären resistiven Schaltern, Complementary Resistive Switches (CRS), welche aus zwei gegenpolig verschalteten bipolaren resistiven Schaltern bestehen, vorgeschlagen. Diese CRS-Zellen zeichnen sich durch ein durchgängig hochohmiges Verhalten unabhängig vom eingeschriebenen Speicherzustand aus, wodurch das Auftreten von parasitären Strompfaden unterbunden wird. Der Nachweis der Realisierbarkeit des Konzepts konnte sowohl mit resistiven Schaltern, die auf einem elektrochemischen Metallisierungseffekt basieren, als auch mit Schaltern, welchen ein Valenzwechselmechanismus zu Grunde liegt, erbracht werden. Um das Zusammenspiel der gegenpolig verschalteten bipolaren resistiven Schalter zu untersuchen, wurden Kompaktmodelle entwickelt. Es konnte gezeigt werden, dass einfache dynamische Memristor-Modelle nicht geeignet sind, um CRS-Zellverhalten korrekt zu simulieren, wohingegen mit komplexeren, physikalisch motivierten, memristiven Modellen gute Ergebnisse erzielt werden können.
Passive Matrizen mit CRS-Zellen eignen sich besonders für die Anwendung als Speicher. Es konnte gezeigt werden, dass die Realisierung großen $N \cdot N$-Matrizen (beispielsweise $N = 10^3$), wie sie für eine effiziente Implementierung benötigt werden, mit diesem Konzept möglich ist. Als vorteilhafte Ausleseverfahren konnten zwei destruktive Leseverfahren identifiziert werden: Das Erste basiert auf dem bedingten Schalten in den ON-Zustand, während das zweite Verfahren einen Schreibpuls zum Auslesen verwendet. Ein alternatives nichtdestruktives Leseverfahren konnte ebenfalls realisiert werden; die mögliche Größe der Matrix wird dadurch allerdings wieder verringert.
CRS-Zellen in passiven Speichermatrizen können neben ihrer Funktionalität als Speicherzellen auch für die Realisierung von rekonfigurierbaren Logikoperationen verwendet werden. Dabei kann ein komplementärer resistiver Schalter als elementarer Zustandsautomat aufgefasst werden. Basierend auf der logischen Implikation als Grundfunktion können weitere logische Operation sequentiell realisiert werden. Es konnte gezeigt werden, dass 14 von 16 Booleschen Operationen mit einer einzigen CRS-Zelle realisiert werden können, wohingegen für die Bereitstellung aller 16 Operation zwei CRS-Zellen, beispielsweise in einem gestapelten Matrixaufbau, benötigt werden.

Abstract

Size reduction of transistors has been the main reason for a successful development of computer systems over the last decades. Since the downscaling of transistors is assumed to come to an end within the next years, alternative technologies involving significantly less area consumption and an ongoing scaling potential are required. The smallest feasible area consumption ($4F^2$) can be achieved by application of passive crossbar arrays. In combination with integrated resistive switches (also referred to as memristors) at each junction, highest possible density memory and logic applications would result.

Resistive switches are two-terminal devices and offer a non-volatile switching behavior when applying short voltage pulses. Although individual devices have a low power requirement, passive crossbar arrays show significant power losses due to parasitic current sneak paths. This so-called 'sneak-path problem' does not only lead to increased power consumption, but also complicates or even prevents proper array read operations. To solve this problem, the implementation of a rectifying diode-like selection device was suggested so far. However, this approach is difficult to realize for bipolar resistive switches, since high current densities (among other factors) are required.

A completely new approach was developed within the framework of this dissertation. Here, two anti-serially connected bipolar resistive switches are applied to form a complementary resistive switch (CRS). Independent of the actual storing state, CRS cells are always high-resistive. Therefore, no parasitic sneak paths can occur. Proof-of-concept measurements were performed, showing CRS behavior for resistive switches based on both the electrochemical metalization effect and the valence change mechanism. For studying the interaction of anti-serially connected resistive switches, compact device models of resistive switches were developed. It could be shown that simple dynamic memristor-models are not suitable for simulating correct CRS behavior, whereas more complex, physics-based memristive models lead to realistic simulation results.

CRS-based passive crossbar arrays are especially well suited for memory applications. It could be shown that large $N \cdot N$-arrays (for example, $N = 10^3$), which are required for efficient implementations, are feasible with this concept. Two advantageous destructive read-out schemes could be identified: The first one is a level read scheme which is based on a conditional switching to the ON-state, whereas the second one is a spike read scheme applying a write pulse for each read operation. Additionally, an alternative non-destructive read-out could be implemented, but in that case, the possible array size is reduced.

Aside from memory functionality, CRS cells can also be used to realize reconfigurable logic operations. In this case, complementary resistive switches can be considered as elementary state machines. Based on the logic implication function, which can be regarded as the basic function, several logic operations can be performed sequentially. It was evidenced that 14 of 16 Boolean functions can be realized by a single CRS cell, whereas two CRS cells are required to allocate all 16 functions; they are provided, for example, in a folded crossbar array.

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Abbreviations

BRS	Bipolar Resistive Switch
CRS	Complementary Resistive Switch
DRAM	Dynamic Random Access Memory
ECM	Electro-Chemical Metalization
EEM	Electrostatic/Electronic Mechanism
FPGA	Field Programmable Gate Array
FPNI	Field Programmable Nanowire Interconnect
HRS	High-Resistive State
ITRS	International Technology Roadmap for Semiconductors
LRS	Low-Resistive State
LUT	Look-Up Table
MIM	Metal-Isolator-Metal
NDRO	Non-Destructive ReadOut
OTS	Ovonic Threshold Switch
PCM	Phase Change Mechanism
PLA	Programmable Logic Array
ReRAM	Redox Random Access Memory
SRAM	Static Random Access Memory
TCM	Thermo-Chemical Mechanism
URS	Unipolar Resistive Switch
VCM	Valency Change Mechanism

1 Introduction

1.1 Motivation

Scaling of transistors has been the driving force for progress in computer system development over the last decades. According to Moore's law [1], the number of components per integrated function (i.e. transistors per chip) increases exponentially with time. As a result, costs per component (transistor) also decrease exponentially if constant costs per chip area are assumed. Transistor scaling has become very challenging in the last years and there are major concerns that scaling down beyond the 16 nm node will not be achievable with economically justifiable effort [2].
Consequentially, many research activities are undertaken in order to overcome this issue. Basically, there are three research directions [3]:

- new materials and sophisticated designs for CMOS transistors ('more of Moore')
- new transistor devices ('more than Moore')
- new computing paradigms ('no more Moore')

A very promising approach is to combine the first direction with the last one. In so-called hybrid CMOS/nanoelectronic circuits, ultimately scaled CMOS is combined with novel nanoelectronic devices which are patterned in a passive crossbar array structure [4]. These crossbar arrays are easy to fabricate due to their regularity and are intended to be processed on top of the CMOS circuit [5].
In order to fit into crossbar arrays, only two terminal nanoelectronic devices can be used, making resistive switching devices the most favorite implementation [6–8]. Especially for future 3D integration, resistive switches are very attractive [9, 10] as they offer low energy and fast read/write at small volume consumption. As a figure of merit, the Energy-Space-Time product [11] reflects these properties. When comparing DRAM (Dynamic Random Access Memory) to ReRAM (Redox Random Access Memory), the benefit in terms of the Energy-Space-Time product becomes significant for lower feature size F, see Fig. 1.1.

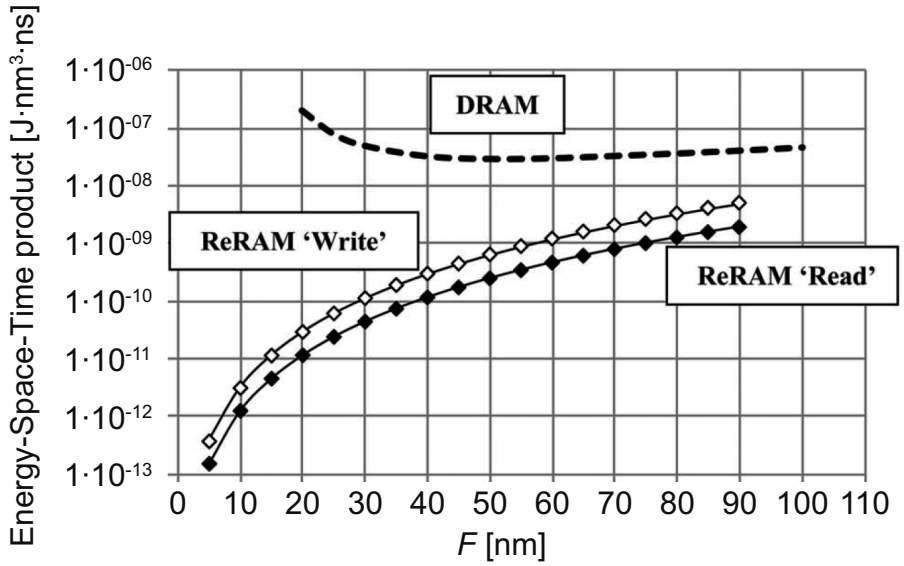


Figure 1.1: Energy-space-time product versus feature size F. From [11].

1.2 State of the Art

Resistive switches are emerging devices, and architectures based on resistive switches are in development [2]. Resistive switching can be found in many material systems [6, 7, 12]. The most important categories are valency change mechanism (VCM) devices, such as Pt/TiO_2/Pt [13], thermo-chemical mechanism (TCM) devices, such as Pt/NiO/Pt [14], and electro-chemical mechanism (ECM) devices, such as Ag/SiO_2/Pt [15]. A more general classification scheme refers to the switching polarity, either unipolar or bipolar [12].

The idea to use crossbar array architecture got a great advance by publication of the Teramac concept [16] and was picked up by several groups [17–20]. However, a major disadvantage of present passive crossbar array approaches is the lack of junction isolation, giving rise to the sneak path problem [21]. The state of the art approach to handle this problem is the implementation of a selector device. For unipolar resistive switches, *pn*-diodes [22] or Schottky diodes [23, 24] are suggested. For bipolar resistive switches, Zener-diode like devices are needed, but implementation is difficult to realize [25]. In general, the mismatch of suggested rectifying elements and resistive switches in terms of required current densities is unsolved and actual achievable current densities are much too small [26–28].

Resistive switches were recognized to offer a dynamic behavior [29] and can be

considered dynamical systems, so-called memristive systems [30, 31], for modeling purposes.

1.3 Objectives

The objective of this work is to introduce a new approach to overcome the sneak path problem by a new device, the complementary resistive switch (CRS). The complementary resistive switch consists of two anti-serially connected bipolar resistive switches which offer an overall high-resistive state in each storage state. Proof of concept measurements illustrate the feasibility of the concept. Compact basic as well as dynamic bipolar resistive switch models are derived from models given in literature and are further developed. These models are then applied to anti-serially connected bipolar resistive switches. In a next step, the properties of complementary resistive switches in passive crossbar array memories are compared to memories based on single bipolar resistive switches. Finally, a novel approach on how to realize logic operations with resistive switches as well as complementary resistive switches is presented. The thesis is structured as follows:

- In chapter 2, basic considerations on resistive switches as memory and logic devices are illustrated.
- In chapter 3, modeling bipolar resistive switches is illustrated and implementation of compact SPICE models is explained.
- In chapter 4, the complementary resistive switch is introduced. The feasibility of concept is proved by measurements of connected as well as integrated complementary resistive switches, and modeling is described by means of bipolar resistive switch models.
- In chapter 5, memory application of complementary resistive switches in passive crossbar arrays is discussed and compared to arrays based on bipolar resistive switches.
- In chapter 6, logic applications of complementary resistive switches are investigated and concepts for applications in passive crossbar array memories are developed.
- In chapter 7, the results of this thesis are summarized and an outlook is given.

2 Fundamentals

2.1 Memory Devices

There are several approaches on how to classify memory devices according to ITRS Roadmap [8]. Most relevant for the industry is technical maturity, classifying memory technologies to three classes: baseline (mature), prototypical and emerging. These categories are mainly economic ones, evaluating the actual and expected market potential of a certain memory technology. On the other hand, there are pure scientific classification schemes trying to categorize memory technologies in terms of similar physical mechanism (e.g., thermal effects), materials used (e.g., chalcogenides) or types of physical state variables (e.g., charge). Additionally, there are several engineering-related categories which can also be applied for classification: volatility, electrical polarity (unipolar or bipolar), physical structure (e.g., three layer structures) or type of memory cell layout. The most important kinds of memory cell layouts are:

- pure transistor-based (e.g., SRAM)
- layouts with at least one transistor (1T, 1T1R, 1T1C)
- transistor-less layouts (1R, 1D1R)

By having a look at future high density and 3D stackable memory architectures projected by ITRS Roadmap, the type of memory cell layout becomes very crucial, since only two terminal memory cell layouts can be used in passive crossbar arrays. Any transistor-based concept - either pure transistor-based or layouts with at least one transistor - is not passive crossbar array compatible. In Fig. 2.1 several important memory technologies are classified in terms of technical maturity (year 2011), and technologies which allow for two terminal elements are marked in red color. Note that all technologies available today as baseline or prototypical technology are not suited for fabrication of passive crossbar arrays, thus great effort is needed to bring at least one of the emerging two terminal elements to prototypical or baseline maturity. This challenge is visualized in the maturity-versus-time-graph in Fig. 2.1. Note that today's baseline technologies SRAM, DRAM and NAND FLASH are

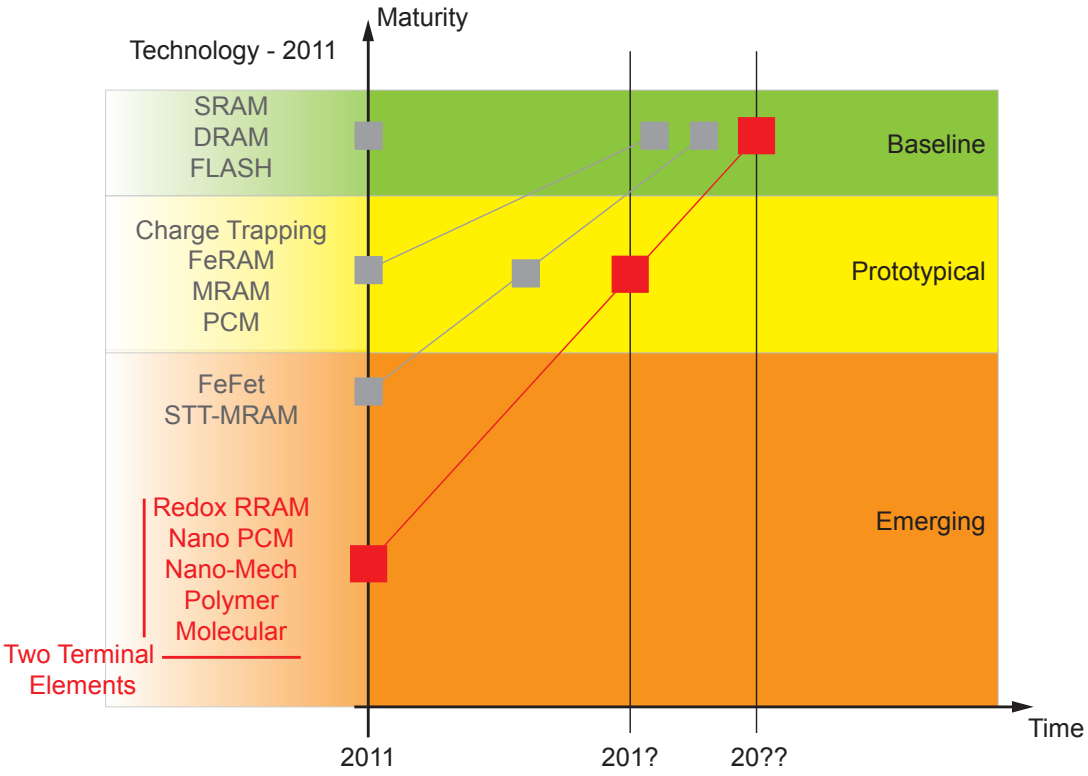


Figure 2.1: Memory classification in terms of technical maturity for 2011 and projection for the future. Technologies with need for a transistor are marked in gray color and emerging two terminal elements are marked in red color. The important question is at which point the emerging elements will reach the baseline.

projected to face severe difficulties in further downscaling when reaching the 16 nm node [2]. Also, all prototypical technologies, such as Charge Trapping, FeRAM, MRAM and PCM, or emerging technologies like FeFet and STT-MRAM in need of a transistor inside the memory cell are limited to footprints larger than the minimum footprint of $4F^2$ [8] and, due to the requirement for a transistor, 3D integration will become very demanding.

In summary, passive crossbar arrays are thought to be the best suited solution for further downscaling and future 3D stacking; bringing the emerging two terminal memory devices to prototypical stage is a very important demand for further memory development [8, 11, 16, 32].

All listed emerging memory technologies which are passive crossbar array compatible by principle are resistance-based, bringing resistive switching devices to the center of interest for future nonvolatile memory. Note that resistive switching elements

offer a metal-isolator-metal (MIM) structure which is very beneficial for layer by layer fabrication.

2.2 Resistive Switching Devices

Metal-isolator-metal (MIM) type resistive switching elements are basically two terminal devices (1R), having one bottom electrode and one top electrode contact. Adding a two-terminal rectifying element (e.g., a *pn*-diode) to a resistive memory element results in a two-terminal 1D1R memory cell [22, 23]. Alternatively, resistive switching elements can be combined with a transistor, realizing 1T1R cells [33, 34]. In contrast to 1D1R cells, 1T1R cells are three-terminal devices, thus not suited for implementation in simple crossbar arrays which only consist of orthogonal word and bit lines (for details see section 2.6).
In Fig. 2.2 a basic classification of resistive switching elements in terms of working principle is shown, clarifying that although phenomenologically similar, the origin of resistive switching strongly depends on the incorporated materials. Five classes are depicted: electrostatic/electronic mechanism (EEM), electro-chemical metalization

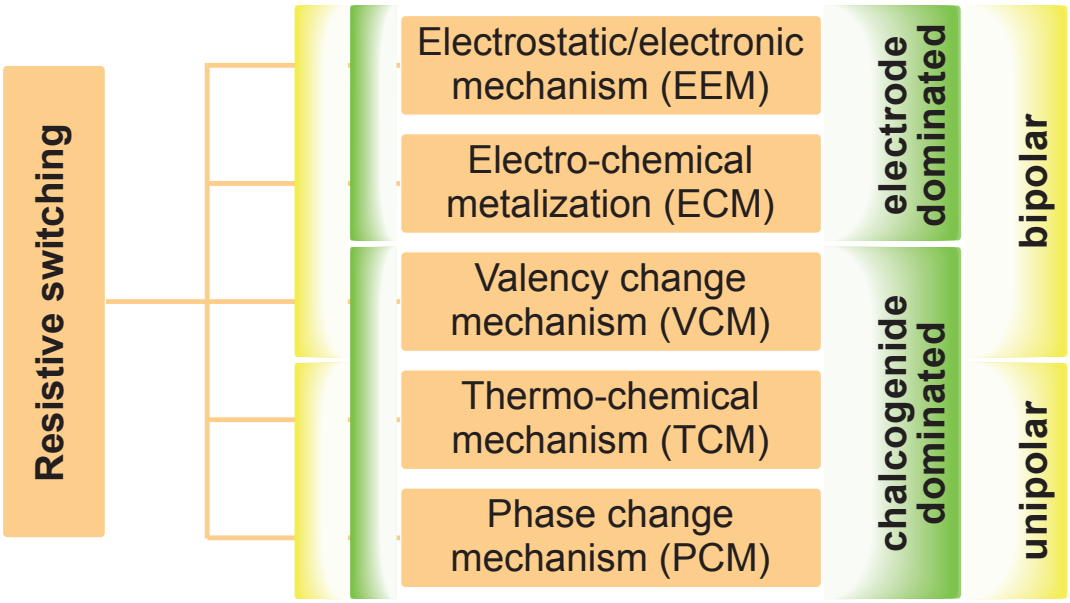


Figure 2.2: Classification of resistive switching materials. Five classes of resistive switching materials are shown here: electrostatic/electronic mechanism (EEM), electro-chemical metalization (ECM), valency change mechanism (VCM), thermo-chemical mechanism (TCM) and phase change mechanism (PCM). These classes can be assigned to super classes. 1: electrode/chalcogenide dominated, 2: unipolar/bipolar. Compare [12].

(ECM), valency change mechanism (VCM), thermo-chemical mechanism (TCM) and phase change mechanism (PCM). These classes can be combined to super classes, using either the material impact (electrode or chalcogenide dominated) or switching polarity (unipolar or bipolar) for classification. When focusing on electrical properties, it is most appropriate to use switching polarity to categorize resistive switching elements.

2.3 Unipolar Resistive Switches

Phase change memory (PCM) elements as well as thermo-chemical memory (TCM) elements are unipolar resistive switches (URS). Fig. 2.3a shows a generic unipolar I-V switching characteristic. Starting in a high-resistive state (HRS), a voltage larger than $V_{\mathrm{th,Set}}$ is needed to switch the device to the low-resistive state (LRS). Since switching to HRS is current driven, a current compliance (CC,Set) is needed to limit

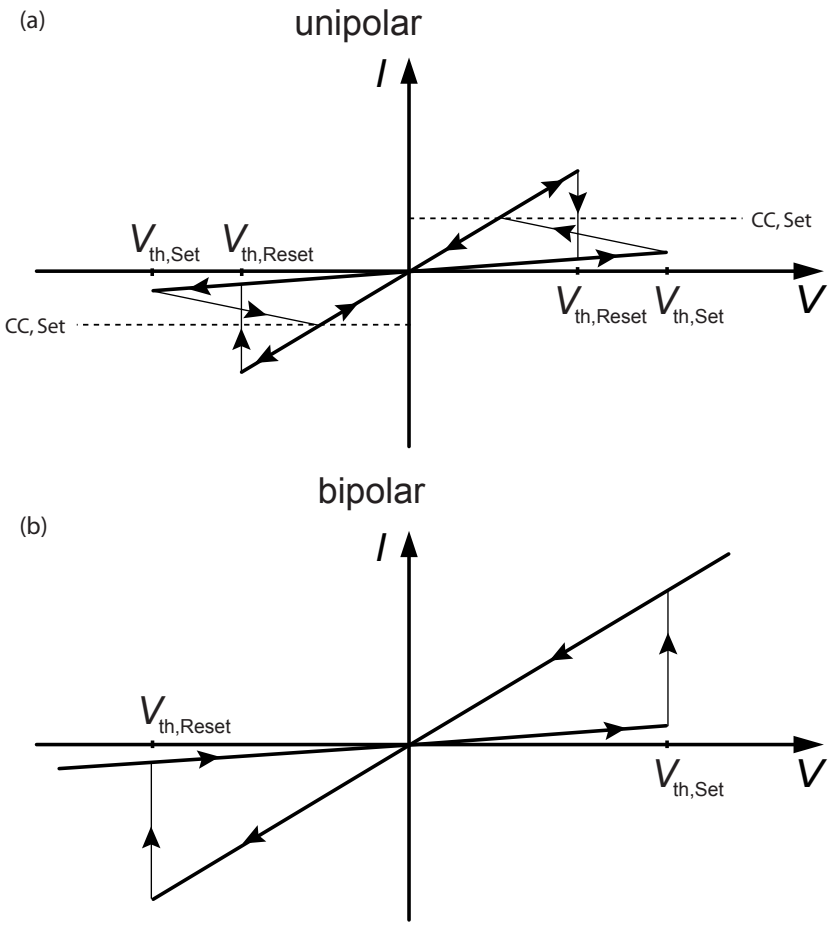


Figure 2.3: (a) Unipolar resistive switch (URS). (b) Bipolar resistive switch (BRS).

current when switching to LRS. When switching to HRS, no current compliance is applied, and switching to HRS occurs at a voltage level of $V_{\mathrm{th,Reset}}$. Because switching does not depend on voltage polarity, negative voltages can be applied for Set or Reset, too.

2.4 Bipolar Resistive Switches

Typical representatives of bipolar resistive switches (BRS) are valency change memory (VCM) elements and electro-chemical metalization (ECM) elements. Fig. 2.3b shows a generic BRS I-V curve with ohmic HRS and LRS branches. A positive voltage $V_{\mathrm{th,Set}}$ is needed for switching to LRS, since a negative voltage $V_{\mathrm{th,Reset}}$ is needed for switching to HRS. In Fig. 2.3b HRS and LRS branches are ohmic, but can also be non-ohmic, e.g., for VCM devices (see 2.4.2). Additionally, $V_{\mathrm{th,Set}}$ and $V_{\mathrm{th,Reset}}$ must not be equal in terms of absolute values, which is typical for ECM devices (see section 2.4.1), for instance. Dynamic behavior of resistive switches can differ from quasi-static I-V behavior, resulting, for example, in an increase of threshold voltages for fast pulses [29, 35], and can be understood in terms of dynamical systems (see section 3.2). A current compliance is often present when measuring BRS, but it is not necessary in many cases. Alternatively, an additional series resistor (e.g., the resistance of a select transistor) can be used [36, 37]. In some cases of VCM devices, the inherent series resistance is sufficient to limit currents in the Set process, e.g., for strontium titanate-based devices (see section 2.4.2) or tantalum oxide-based devices [38].

2.4.1 ECM Elements

A typical ECM ($\mathrm{Pt/SiO_x/GeSe/Cu}$, [39]) quasi-static I-V curve is shown in Fig. 2.4a. A series resistor of 940Ω is incorporated in this measurement [40]. Variation in terms of switching voltages is very low here, but it depends on the switching device. Note the asymmetries in switching voltages which are present in most ECM devices. The linear slope in HRS as well as in LRS and the absence of a dedicated forming cycle are also typical for ECM devices. Fig. 2.4b shows another ECM element with similar characteristics. Because of a much larger series resistor in this measurement (200 kΩ), currents are much lower.

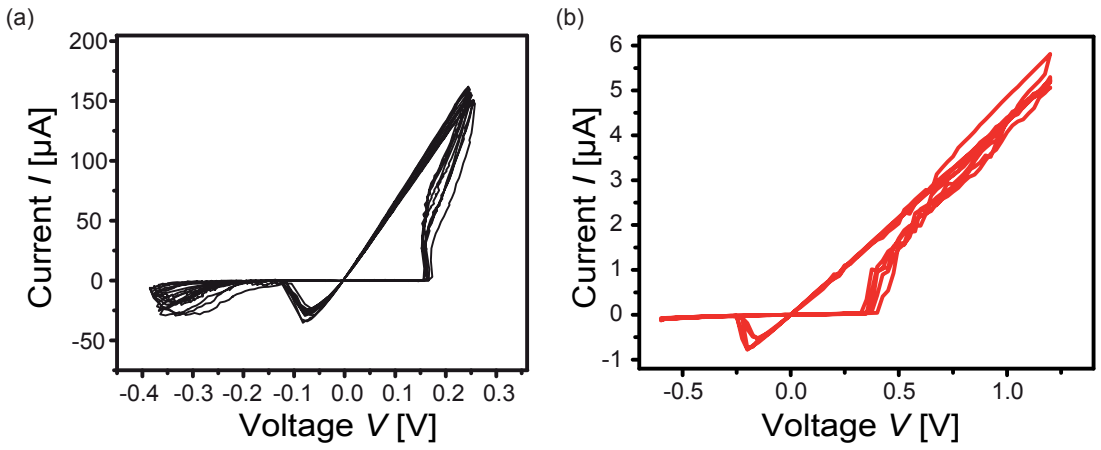


Figure 2.4: (a) $Pt/SiO_x/GeSe/Cu$ ECM element. Adapted from [40]. A series resistor of 940 Ω was used in these measurements. (b) $Cu/SiO_2/Pt$ ECM element. Adapted from [41]. A series resistor of 200 kΩ was used in these measurements.

2.4.2 VCM Elements

In contrast to ECM devices, VCM devices often need complex forming procedures [42]. For $Ti/SrTiO_3/Pt$ (Ti/STO/Pt) VCM elements, a simplified forming with just a voltage ramp as a prerequisite was shown in [43]. Such a first forming cycle (black curve) is shown in Fig. 2.5. In this case, a higher voltage for SET in the first cycle compared to the SET voltage after the first cycle is observed. The forming voltage is about $V_{\mathrm{Forming}} = 3.8\,\mathrm{V}$ while the reset voltage is $V_{\mathrm{Reset}} = 2.6\,\mathrm{V}$ and set voltage is $V_{\mathrm{Set}} = -1.4\,\mathrm{V}$. Note that voltage polarity is switched compared to Fig. 2.3b. Completely forming-free devices are also feasible by further material engineering [44–46].
In contrast to ECM devices, a non-ohmic characteristic is present in the HRS and LRS state (see Fig. 2.5).

2.5 Active Crossbar Arrays

A crossbar array is a matrix consisting of n word lines, m bit lines and $n \cdot m$ memory cells, which can be accessed individually or row by row.
In general, there are two possible ways of implementation, either active or passive. For the active implementation, each matrix element has its own activatable select transistor (1T), while for the passive implementation, only two terminal selector devices, like diodes, are allowed. When used for storage, such a structure is called random access memory (RAM). In dynamic random access memories (DRAM), for

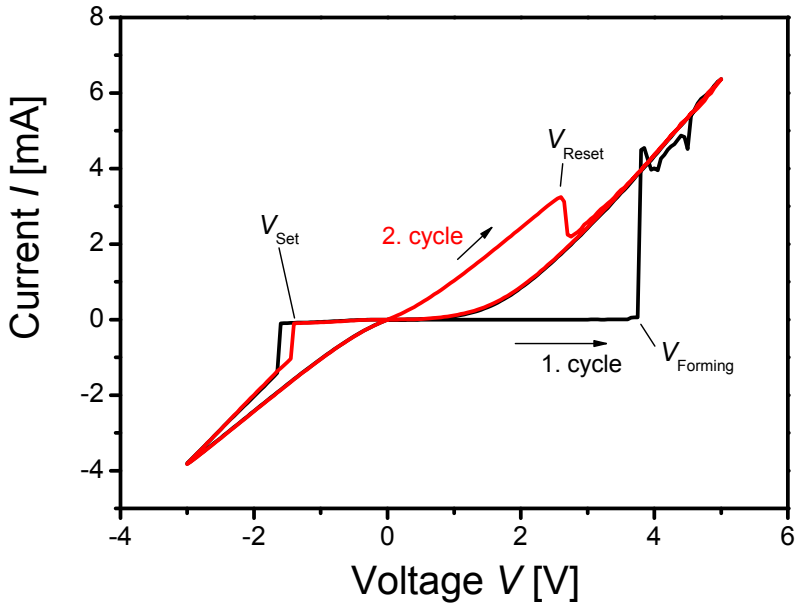


Figure 2.5: *I-V* characteristic of a VCM element (Ti/8 nm STO/Pt) with a pad size of 200 μm x 200 μm. For details on fabrication see [43].

example, every memory cell consists of a capacitor (storing device) and a transistor (selector device); this is called a 1T1C configuration. For resistive random access memory (ReRAM), a resistive switch (1R) and a transistor (1T) are used (1T1R configuration). Every resistive switching cell, either unipolar or bipolar, can be used in this approach.

The main disadvantage of active memories is the need for a select transistor (which is based on crystalline silicon) for each matrix element. This requirement limits downscaling, increases minimum feature size (to $6 - 8F^2$ [2]) and makes 3D integration difficult [11].

2.6 Passive Crossbar Arrays

In contrast to active arrays, no transistors are used in passive crossbar arrays. Passive crossbar arrays are the simplest conceivable matrices consisting only of bit and word lines and a storing element at each junction, resulting in a minimum feature size of $4F^2$. Because of the simple structure, crossbar arrays are easy to fabricate and are excellently applicable for 3D integration. Since no signal restoration can be performed in the array, an active periphery, consisting of, for

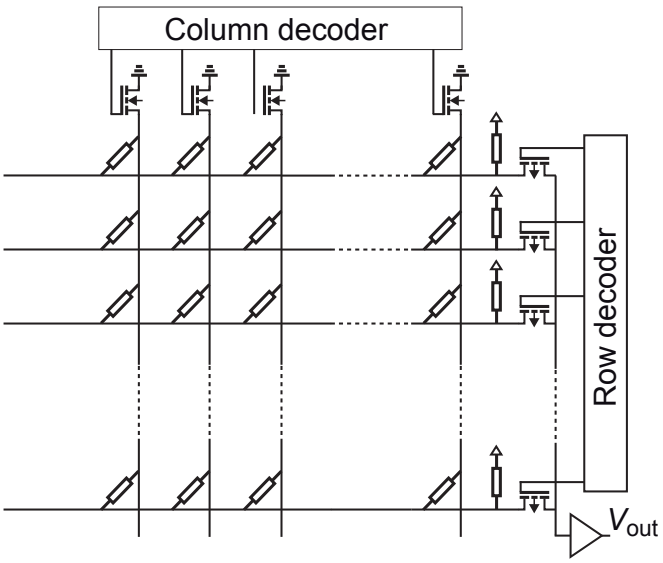


Figure 2.6: Passive crossbar array and CMOS periphery.

instance, complementary metal oxide semiconductor (CMOS) circuits, is needed to drive the array externally, resulting in a hybrid CMOS/nanoelectronics circuit (Fig. 2.6) [47]. There are two major issues in passive crossbar arrays that must be addressed for proper memory functionality:

1. It must be possible to write an array cell (or row) without inferring non-addressed cells.

2. During a read operation on an array cell (or row), a logical '0' must be distinguishable from a logical '1'.

Issue 1 can be solved by using a half-select or a third-select voltage scheme [48]. For asymmetric threshold voltages, a generalized third-select scheme can be used [49]. Fig. 2.7a illustrates the half-select voltage concept and Fig. 2.7b the third-select scheme. The addressed elements are supplied to a voltage V, while all other elements are subjected to $\pm\frac{1}{3} \cdot V$ for a third-select scheme or $\frac{1}{2} \cdot V$ and 0 V for a half-select scheme. These schemes ensure that the potential at non-addressed cells does not exceed the switching voltage.
Issue 2 is particularly challenging, because reading depends strongly on the electrical characteristics of the devices, on the used read procedure, and on the stored bit pattern. The main challenge associated with crossbar arrays results from the fact that all cells in a row are connected to each other by the top electrode, and all cells in a column are connected to each other by the bottom electrode. The resulting

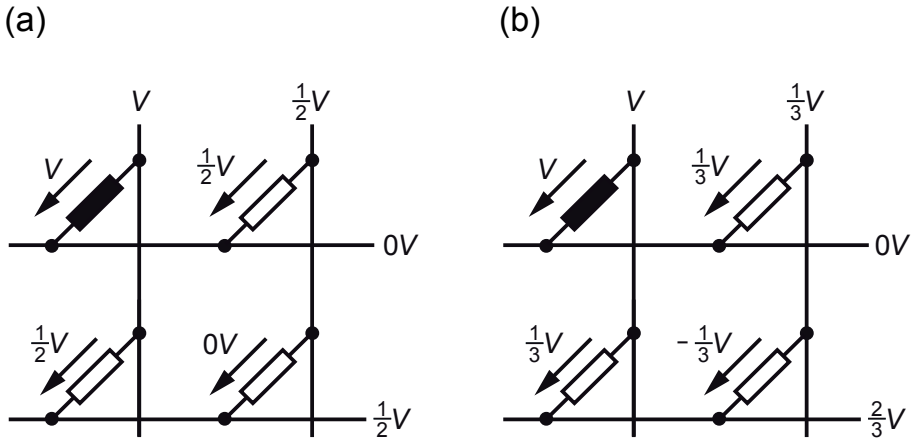


Figure 2.7: (a) Half-select voltage scheme. (b) Third-select voltage scheme.

parasitic currents superpose the read currents, and therefore limit the maximum crossbar array size. This issue is known as sneak path problem in literature [21] and is visualized in Fig. 2.8. Note that in Fig. 2.8, non-accessed lines are floating to keep any power dissipation induced by sneak path low. If we want to access the cross point junction in the middle of the array, we apply a read voltage to it. Since there is also a voltage drop at non-accessed junctions, a parasitic current is present there. If there are at least three junctions in LRS (green) and the junction which is accessed is in HRS (blue), the read current is dominated by parasitic currents (case 1). This case is hard to distinguish from case 2 where the accessed junction is in LRS because the difference between $I_{\text{sense},1}$ and $I_{\text{sense},2}$ is very small. The occurring current swing at the output of the crossbar read circuit between reading a high-impedance state (R_{HRS}) and reading a low-impedance state (R_{LRS}) must be large enough for sensing (See Fig. 2.8). In Fig. 2.6, an exemplary CMOS periphery is shown which uses a pull-up resistor to transform the current I_{sense} to a voltage level. For reading, all bit lines are pulled up and one word line is grounded, while non-addressed word lines are floating. If a voltage swing of at least 10% is assumed for distinguishing a logical '1' and '0', a maximum crossbar size of $8 \cdot 8$ (compare [21]) results. Therefore, only very small arrays can be realized. This issue is discussed in detail in section 5.3.

2.7 Solutions to the Sneak Path Problem

A major disadvantage of passive crossbar arrays directly results from the lack of an active selector device isolating memory cells from each other. There are two

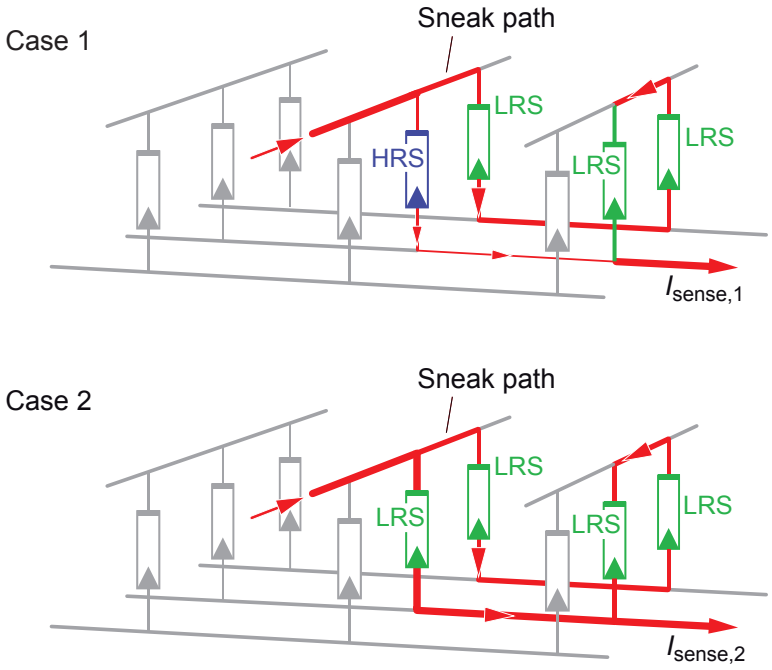


Figure 2.8: Visualization of the sneak path problem in passive crossbar arrays. Case 1 read of a HRS element and case 2 read of a LRS element in the middle of the array. Sense currents (I_{sense}) are large in both cases due to parasitic current sneak paths. Compare [50].

approaches to handle the sneak path problem, one based on circuit engineering and one based on device engineering. In the circuit engineering approach, alternative sensing concepts and readout configurations are applied, while device engineering concentrates on improving device isolation, either by implementing a diode or by trying to find resistive switching materials showing non-ohmic device characteristics.

2.7.1 Circuitry Approach

The first approach to eliminate sneak paths is shown in Fig. 2.9a. Here, a virtual ground configuration is used resulting in 0 V at non-accessed cells, thus preventing sneak paths. For a real crossbar array (see Fig. 2.6), select transistors are needed whose resistance must be considered (Fig. 2.9b). The additional resistances R_{t} of the transistors make this approach impractical because no virtual ground potential is present at the columns, and thus sneak currents result. When using a pull-up sense resistor for reading (Fig. 2.6), the additional resistance R_{t} of the transistor simply adds up to the sense resistor [48], but in this case, sneak paths are again a major issue in this configuration [21].

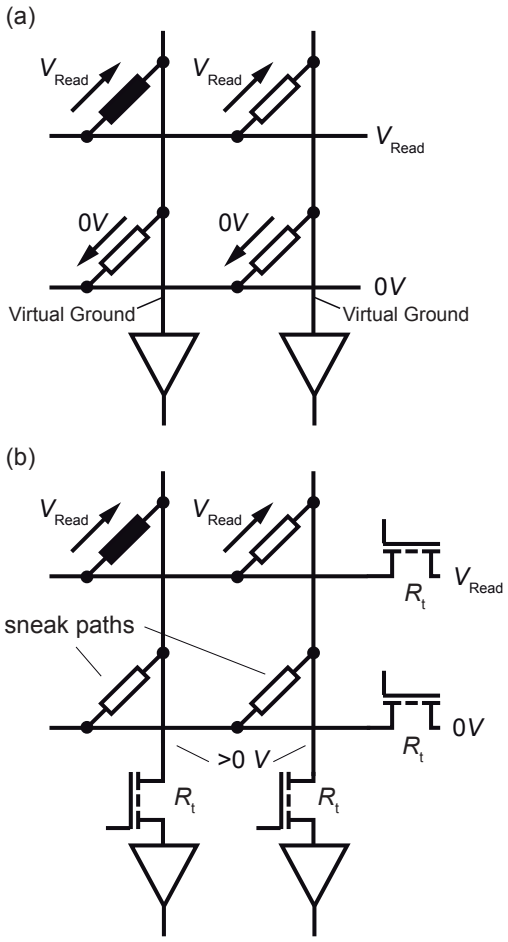


Figure 2.9: (a) Ideal virtual ground read scheme. (b) Realistic circuit model of crossbar array with virtual ground sense amplifier. Due to select transistors, the virtual ground approach is obsolete.

Instead of trying to prevent sneak paths, one can use the fact that sneak currents are constant in the read operation. This fact can be used for an adaptive read procedure [51]. For this, the selected cells are read at least three times. The actual value of the accessed cell in the first read cycle is compared to the reference values of subsequent read cycles when reading '1' or '0', respectively. Note that every read operation consists of several read and write steps, and the power consumption is high because of the currents flowing along the sneak paths to ground. Depending on the stored bit pattern, these currents can become very large, limiting the crossbar array size to low values. This read-procedure is also time-consuming, especially for large arrays where voltage margins become very small. Adaptive readout concepts are also suggested in [52].

In [53], a different approach allowing for read of crossbar arrays is suggested. To

evaluate the resistances of a m x n passive crossbar array, $p = n = m$ read phases are needed for a square crossbar array (Fig. 2.10a). Voltages applied to columns are named $V_{\mathrm{c1}}...V_{\mathrm{cn}}$, while voltages applied to rows are named $V_{\mathrm{r1}}...V_{\mathrm{rm}}$; and currents and memory elements are labeled accordingly. The voltage scheme which is applied is illustrated in Fig. 2.10b. In phase 1, the first column is set to $0.5 \cdot V_{\mathrm{read}}$, while the rows are set to $-0.5 \cdot V_{\mathrm{read}}$. All other columns are grounded. In phase 2, all columns, except the second column which is set to $0.5 \cdot V_{\mathrm{read}}$, are grounded, while all rows are again set to $-0.5 \cdot V_{\mathrm{read}}$. This read scheme is continued for all columns. The voltage at element xy (row x and column y) which is measured in phase z is labeled $V_{\mathrm{xy\_z}}$. By solving an equation system for each row, all element conductances G_{xy} can be derived. Since there are n unknown variables $G_{\mathrm{x1}}...G_{\mathrm{xn}}$ in each row, n independent equations, one resulting from each read phase, are needed:

$$\begin{pmatrix} I_{\mathrm{r1\_1}} \\ ... \\ I_{\mathrm{r1\_p}} \end{pmatrix} = \begin{pmatrix} V_{\mathrm{11\_1}} & ... & V_{\mathrm{1n\_1}} \\ ... & ... & ... \\ V_{\mathrm{11\_p}} & ... & V_{\mathrm{1n\_p}} \end{pmatrix} \cdot \begin{pmatrix} G_{11} \\ ... \\ G_{\mathrm{1n}} \end{pmatrix}$$
$$...$$
$$\begin{pmatrix} I_{\mathrm{rm\_1}} \\ ... \\ I_{\mathrm{rm\_p}} \end{pmatrix} = \begin{pmatrix} V_{\mathrm{m1\_1}} & ... & V_{\mathrm{mn\_1}} \\ ... & ... & ... \\ V_{\mathrm{m1\_p}} & ... & V_{\mathrm{mn\_p}} \end{pmatrix} \cdot \begin{pmatrix} G_{\mathrm{m1}} \\ ... \\ G_{\mathrm{mn}} \end{pmatrix} \tag{2.1}$$

This read scheme is easy to implement for measurement systems and can be used for automated crossbar array measurements, but due to complexity it is not suitable for integrated circuit applications.

2.7.2 Device Approach

One way to improve the readability of crossbar arrays is to reduce sneak paths by using resistive elements with inherent non-ohmic characteristics [54, 55], e.g., $Ti0_2$-based [24, 56, 57], a-Si-based [58, 59] or switching molecules-based [60, 61]. In Fig. 2.11a a resistive element offering ohmic branches in HRS and LRS is compared to an element with non-ohmic branches. A non-ohmic dependency in the LRS-branch helps to decrease sneak currents (compare $I_{\mathrm{sneak,lin}}$ to $I_{\mathrm{sneak,n}}$), but on the other hand, a large non-ohmic behavior in the LRS branch can reduce the current swing ($\Delta I_{\mathrm{read,n}} < \Delta I_{\mathrm{read,lin}}$). Accordingly, there is an optimum of non-linearity in the LRS branch (see [54]).

Instead of looking for materials with inherent non-ohmic behavior, an additional diode-type selector device can be implemented as well. For URS devices, a Schottky

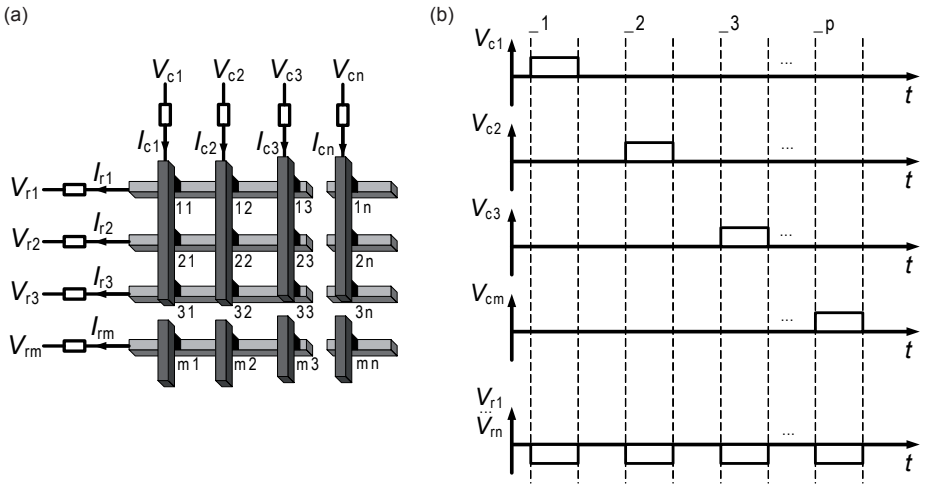


Figure 2.10: (a) Crossbar memory drawing and external wiring. (b) Read scheme consisting of p read phases. The voltage amplitudes are $0.5 \cdot V_{\text{read}}$ and $-0.5 \cdot V_{\text{read}}$, respectively.

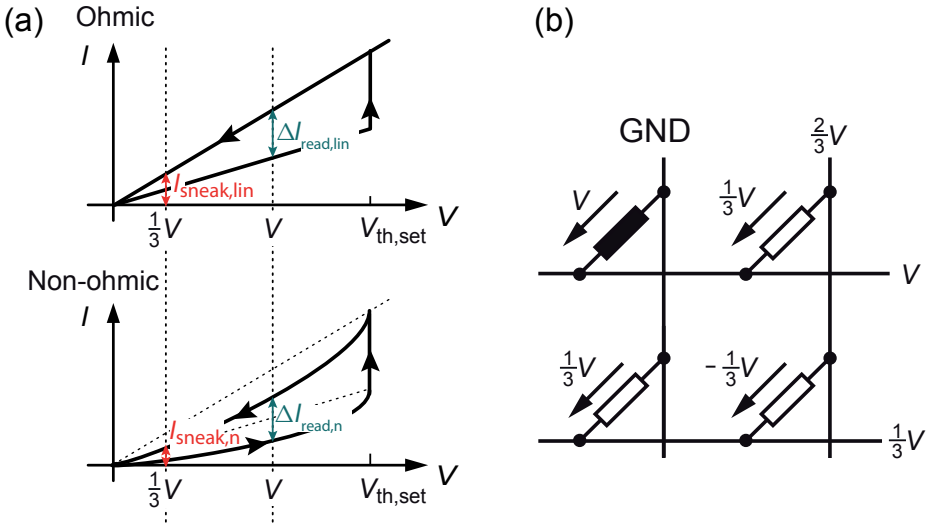


Figure 2.11: (a) Impact of non-ohmic HRS and LRS branches when applying a third voltage scheme. (b) Third voltage scheme.

[62, 63], a *pn*-diode [64] or a heterojunction diode [65, 66] could be selected. Note that these devices are difficult to integrate in crossbar arrays. For phase change memory (PCM) devices, a so-called ovonic threshold switch (OTS) was suggested as selector device [67] as well as Ge-based nanowire diodes [68] or Cu-containing mixed ionic electronic conduction materials [69]. For NiO_2 TCM devices, VO_2-based threshold switches [70] and, in line with the Versatile Project, ZnO-based Schottky diodes were proposed [23, 71, 72]. For BRS, a silicon-based Zener-diode [48] or

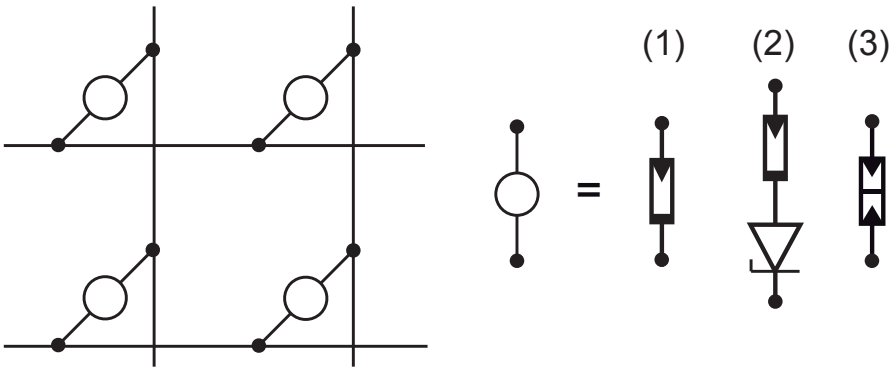


Figure 2.12: Three different types of junctions can be used for passive crossbar arrays: Pure resistive switches (1), resistive switches with a rectifying element in series (2) or complementary resistive switches (3).

a selector with a Zener-diode characteristic [25], which is based on a Schottky diode with a soft reverse breakdown characteristic, could be used. Such devices are difficult to integrate in a crossbar array and are not suitable for stacked crossbar arrays.

In general, it is hard to match the switching devices to the selector device in terms of current density, since current densities of crossbar compatible diodes are much lower ($\approx 10^4 \frac{A}{cm^2}$) than those of devices based on silicon ($\approx 10^7 \frac{A}{cm^2}$) [73, 74]. For BRS, no practical solution for stacked crossbars is present until now. A new approach based on two BRS is presented in chapter 4. All three approaches suitable for BRS elements are depicted in Fig. 2.12, i.e., (1) non-ohmic resistive element, (2) resistive element plus Zener-diode and (3) complementary resistive switch (CRS).

2.8 Resistive Switches for Logic Applications

There are several ideas how to use resistive switches for reconfigurable logic applications in hybrid CMOS - nanoelectronic circuits. Most concepts aim on realizing field programmable logic arrays (FPGA) or programmable logic arrays (PLA) by use of resistive switches. Concepts can be classified by their mode of application:

- Resistive Switches as Programmable Interconnects
- Resistive Switches as Memory Cell
- Resistive Switches as Latching Device

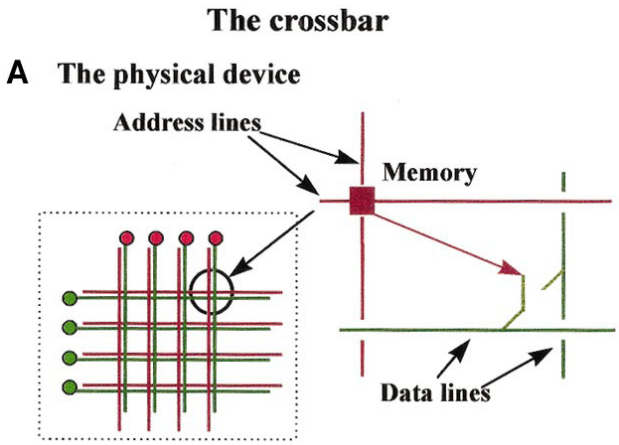


Figure 2.13: The Teramac concept. Each resistive crossbar junction is controlled by a memory element. Reproduced with permission from [16].

First concepts for resistive switch-based logic rely on the idea of using programmable interconnects. Since resistive switches are either high- or low-resistive, connections between two lines can be programmed by such non-volatile switches. In the Teramac concept [16], each memory cell of a conventional memory array controls a resistive switch in a crossbar array, which is processed on top of the memory array (see Fig. 2.13). Since one memory cell is needed for each resistive switch, this concept is not very efficient. In fact, because a CMOS-based conventional memory array is essential for the Teramac concept, no benefit compared to purely CMOS-based memory used as look-up table results from this approach [75].

PLA concepts are based on two crossbar arrays of programmable interconnects, one implementing AND to form the minterms and one implementing OR to realize all logic functions in a two level logic representation. PLAs can be used as logic blocks in FPGAs [76], but since logic blocks (and therefore the crossbar arrays) are typically small for realistic FPGA applications [77], CMOS overhead is large. On the other hand, due to the sneak path problem, the size of usable crossbar arrays is limited anyway (see section 2.7). A resistive PLA logic block realizing a crossbar full adder is given in [78] (see Fig. 2.14). There are also PLA concepts with a latching device for storage and signal regeneration integrated in the crossbar array. In [79], the use of two tunneling diodes, so-called goto pairs, was suggested as latch, while a BRS and a diode were suggested in [80] to form a crossbar latch. For these approaches, two clock signals are needed.

In the CMOL FPGA concept [75], a sea of elementary CMOS cells, each consisting of two pass transistors and an inverter, is connected to a nanocrossbar array consisting

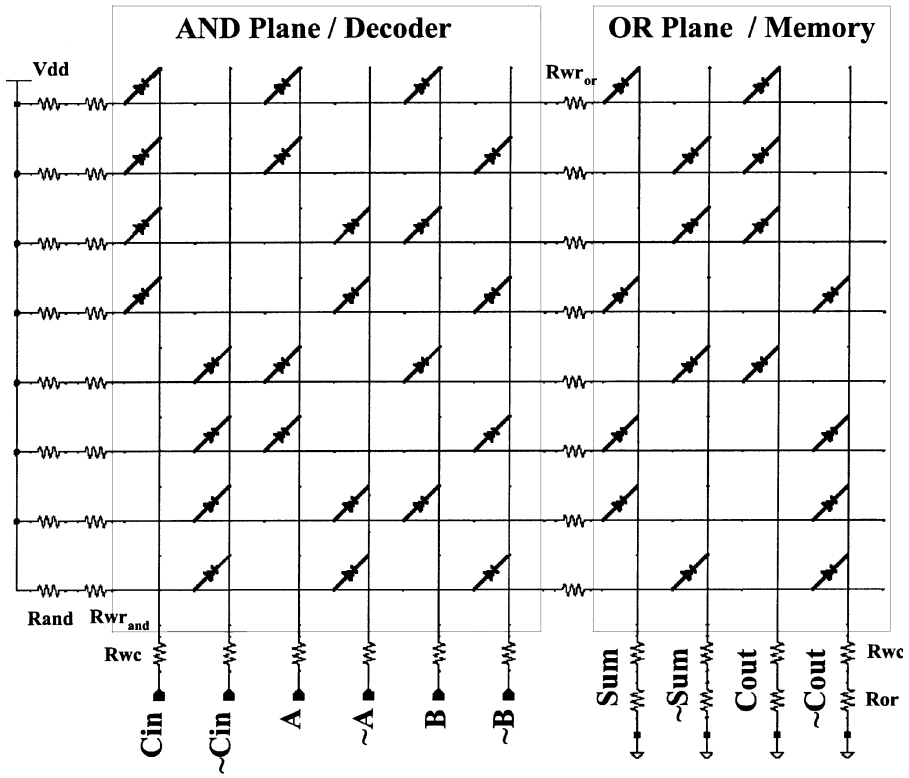


Figure 2.14: Resistive PLA crossbar full adder. Reproduced with permission from [78].

of discontinuous lines (Fig. 2.15). The elementary CMOS cells are connected to each other by programmed (BRS switched to LRS) junctions allowing for wired-or logic. Both nano crossbar layers must be connected to CMOS via nanopins, making fabrication very difficult. Since actual nanowire structure and connectivity must be evaluated after fabrication, mapping is very challenging [81].

A similar concept to CMOL is called FPNI (field programmable nanowire interconnect, see Fig. 2.15). Nano junctions are only used for routing and only one height of nano pins is needed, but crossbar array in FPNI is sparser, degrading performance to about 50% [82].

In conclusion, the common feature of these approaches is that resistive switches are configured once, or very infrequent, to adjust a logic function. In consequence, junctions are either set as a closed connection (LRS) or an open connection (HRS), making no use of the inherent memory feature of resistive switches.

A completely different approach is based on memories where, for example, resistive memories are used as look-up tables in FPGAs. In [83], 1T1R memories are suggested as replacements of SRAM-based look-up tables (LUTs). Also, crossbar memory-based LUTs are thinkable, but the overhead is large due to small array

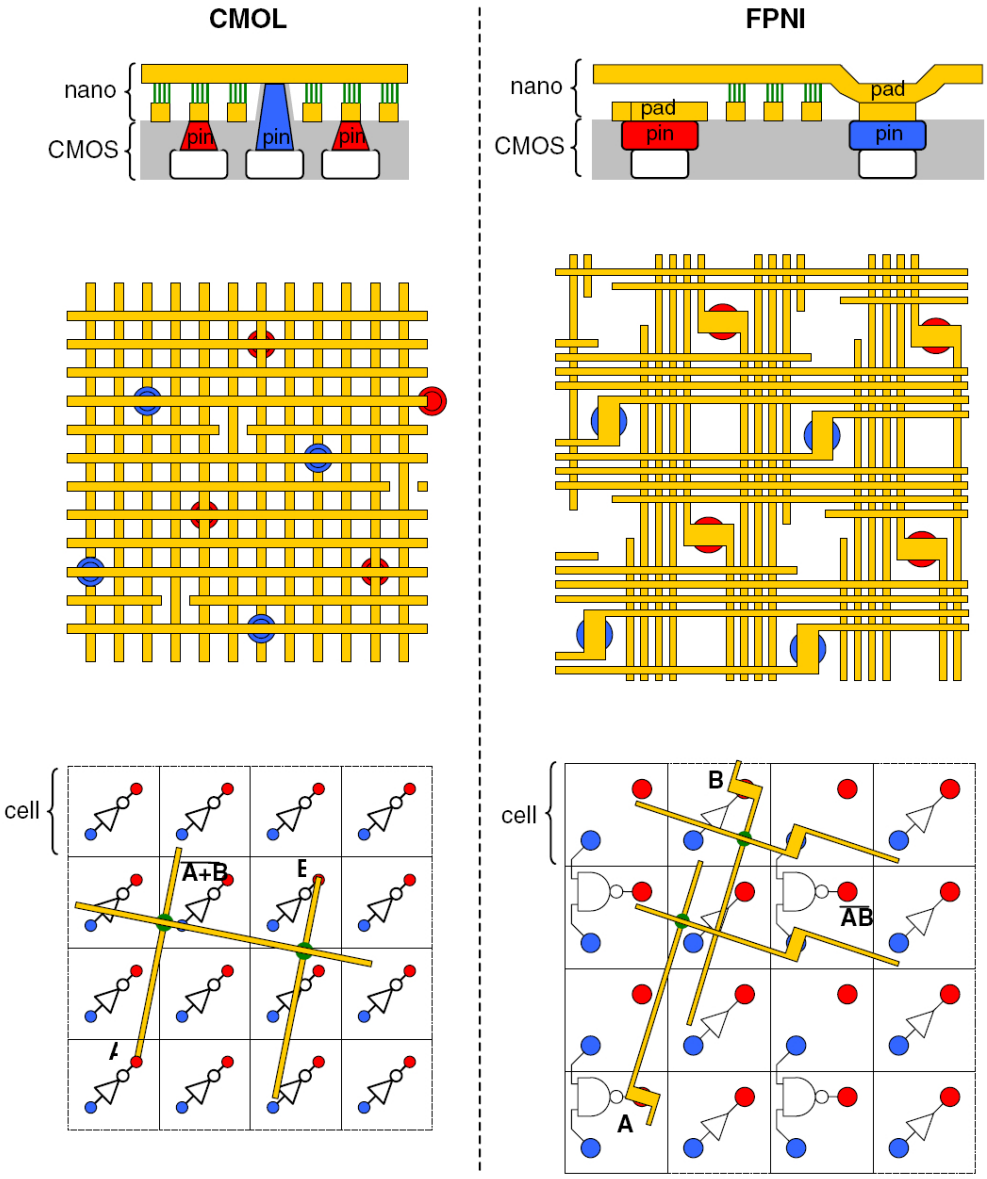
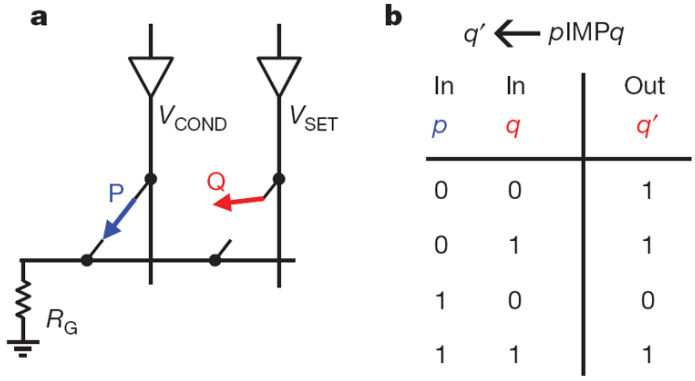


Figure 2.15: CMOL and FPNI concept. Reproduced with permission from [81].

sizes used in conventional FPGA design. In [84], another memory-based computing approach for FPGAs with need for large crossbar arrays - and thus small CMOS overhead - is suggested. In this approach, multi-input-multi-output LUTs are mapped on a large crossbar array memory simplifying routing constraints [84, 85]. In full sequential logic concepts, no combinational logic blocks are present. In [86], the (material) implication is given as a basic logic function in need of two BRS and a load resistor R_G forming the 'IMP-gate' (see Fig. 2.16 and compare latch described in [87, 88]). This operation can be performed in four steps:



In p	In q	Out q'
0	0	1
0	1	1
1	0	0
1	1	1

Figure 2.16: IMP operation realized by two bipolar resistive switches and a load resistor in four steps. Reproduced with permission from [86].

1. Set P to p ($V_P = \pm V_{Write}$)
2. Set Q to q ($V_Q = \pm V_{Write}$)
3. q' = p IMP q ($V_P = V_{COND}$ and $V_Q = V_{SET}$)
4. Read q' ($V_Q = V$READ)

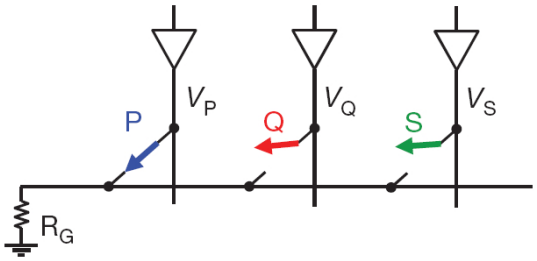
Note that the load resistor must be in the range of $R_{LRS} < R_G < R_{HRS}$. Since IMP and FALSE form a computationally complete logic class, more complex functions such as NAND can also be provided by three BRS and a load resistor in six sequential steps in [86] (see Fig. 2.17):

1. Set S to 0 ($V_S = V_{Clear}$)
2. Set P to p ($V_P = \pm V_{Write}$)
3. Set Q to q ($V_Q = \pm V_{Write}$)
4. s' = p IMP s ($V_P = V_{COND}$ and $V_S = V$SET)
5. s"= q IMP s' ($V_Q = V_{COND}$ and $V_S = V$SET)
6. Read s" ($V_S = V_{READ}$)

Due to the sneak path problem (see section 2.7), this concept is limited to word structures or very small arrays, but can be used in an optimized form for CRS cells (see chapter 6). Additionally, IMP or latch functionality is an intrinsic feature of a single BRS, thus the number of needed cells can be reduced (see section 6.1).

a

	Clocking voltages	
Step 1: $s = 0$		$V_S = V_{CLEAR}$
Step 2: pIMPs	$V_P = V_{COND}$	$V_S = V_{SET}$
Step 3: qIMPs	$V_Q = V_{COND}$	$V_S = V_{SET}$



b

Step 1	Step 2		Step 3				Steps 1, 2, 3		
$s = 0$	$s' \leftarrow p$IMPs		$s'' \leftarrow q$IMPs'				$s'' \leftarrow p$NANDq		
s	p	s	s'	q	s'	s''	p	q	s''
0	0	0	1	0	1	1	0	0	1
0	0	0	1	1	1	1	0	1	1
0	1	0	0	0	0	1	1	0	1
0	1	0	0	1	0	0	1	1	0

Figure 2.17: NAND operation performed in six steps. Reproduced with permission from [86].

3 Bipolar Resistive Switches - Modeling

In circuit simulations with SPICE, each device used is represented by a compact model. Thus, for simulation of memory or logic structures based on bipolar resistive switches, SPICE models for these elements are needed. In this work, the main focus is on a special two element network, so-called complementary resistive switches (see chapter 4), which consists of two anti-serially connected bipolar resistive switches. The main purpose of this chapter is to introduce bipolar resistive switch models, which are then used in chapter 4 for two element network simulations.
In the most basic case, bipolar resistive switches (see section 2.4) can be modeled as hysteretic switches with fixed threshold voltages. Those models are called 'basic' models in the following. Since the I-V characteristics of ECM elements (see section 2.4.1) offer linear branches, a linear branch model (see section 3.1.1) can be used, while for VCM elements (see section 2.4.2) a non-ohmic branch model (see section 3.1.3) is appropriate.
Beside these basic models, dynamic models are available, too, which also reflect frequency dependent behavior. These models are based on a system of differential equations - a dynamical system - which describes the device physics by inner state variables. In section 3.2, the general approach is described and exemplary model implementations are presented. First, a simple dynamic linear model (see section 3.2.2) is introduced, and secondly, a simple dynamic non-linear model (see section 3.2.3). To obtain more physically accurate models, an ECM model from literature is implemented as well, both in a simplified (section 3.2.4) and in a more sophisticated way (see section 3.2.5).

3.1 Basic Models

3.1.1 Basic Linear Branch Model

For simulation, an appropriate hysteretic switch model is needed. In SPICE OPUS [89], a voltage-controlled switch (model type SW), which is a four terminal device, can be used for this. By selecting the same voltage nodes for control and for the actual switch, a two terminal device results. There are four parameters which must be specified in the SW model: offset voltage (VT), hysteresis voltage (VH),

resistance when closed (RON) and resistance when open ($ROFF$). For modeling a BRS, $RON = R_{\mathrm{LRS}}$ and $ROFF = R_{\mathrm{HRS}}$ are set. The hysteresis voltage VH can be calculated from $|V_{\mathrm{Set}}|$ and $|V_{\mathrm{Reset}}|$ of the BRS by means of the arithmetic average:

$$VH = \frac{|V_{\mathrm{Set}}| + |V_{\mathrm{Reset}}|}{2}. \tag{3.1}$$

If $|V_{\mathrm{Set}}| \neq |V_{\mathrm{Reset}}|$, a non-zero offset voltage VT is needed to shift the actual threshold values to V_{Set} and V_{Reset}, respectively. VT is calculated by

$$VT = \frac{|V_{\mathrm{Set}}| - |V_{\mathrm{Reset}}|}{2}. \tag{3.2}$$

Hence, the resulting simulation model of a BRS (element A) consists only of a voltage-controlled switch model (SW) which is controlled by voltage V_{A} (Fig. 3.1a). The input voltage source V_{in} supplies a triangular voltage sweep to the BRS (see inset in Fig. 3.1b).

In Fig. 3.1b, a typical I-V characteristic of a BRS with $VT = 0.1\,\mathrm{V}$, $VH = 1\,\mathrm{V}$, which corresponds to $V_{\mathrm{Reset}} = -0.9\,\mathrm{V}$ and $V_{\mathrm{Set}} = 1.1\,\mathrm{V}$, is depicted. In this simulation, $RON = R_{\mathrm{LRS}} = 1\,\mathrm{k\Omega}$ and $ROFF = R_{\mathrm{HRS}} = 1\,\mathrm{M\Omega}$ is assumed (compare also listing 3.1). With this model, the basic properties of a ECM element in terms of threshold voltage and LRS linearity can be reproduced by simulations.

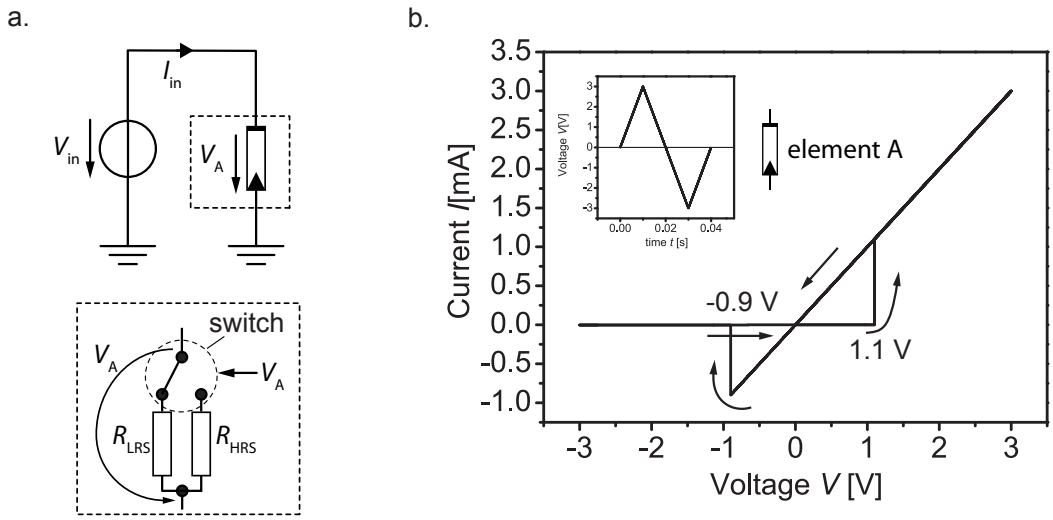


Figure 3.1: (a) The BRS is modeled as voltage controlled switch with two different resistances in ON and OFF position. (b) SPICE simulation of the bipolar resistive switch. Adapted from [90].

```
.SUBCKT BRS 1 2
s1 1 2 1 2 sm off
.ENDS
.model sm SW VT=0.1V VH=1V RON=1k ROFF=1Meg

vin1 (100 0) PWL(0ms 0V 10ms 3V 30ms -3V 40ms 0V)
x1 (100 0) BRS
```

Listing 3.1: SPICE BRS model.

3.1.2 Multilevel Modeling

It is known from experiments, that for ECM material systems the actual R_{LRS} depends on the series resistance R_{ser} connected to the BRS. This allows for multilevel applications. For Ag/GeSe-based elements, a simple correlation between R_{LRS} and R_{ser}, $R_{\mathrm{LRS}} \approx R_{\mathrm{ser}}$, was found when applying a sufficiently short voltage pulse $V \approx V_{\mathrm{Set}}$ [37]. This is coherent with data presented in [36], where a transistor-based current compliance (CC) is applied, and with data from [91], Fig. 4.22, where an active current compliance is used. Note that this correlation is only an empirical observation and $R_{\mathrm{LRS}}/R_{\mathrm{ser}} = 1$ should only be considered as a typical scenario here. The influence of a series resistance can be understood by having a closer look at the distribution of voltage drops. For a BRS in HRS, the voltage drop at the series resistor is about zero. The element resistance starts to decrease when the SET voltage is reached. When R_{element} approaches R_{ser}, the voltage drop at R_{element} is lowered due to the voltage divider's specific properties. If R_{element} equals R_{ser}, only 50% of V_{Set} drops at the BRS. Thus, due to non-linear dependency of switching kinetics on applied voltage (see [92]), switching speed is reduced strongly. Correspondingly, any further change of resistance is also decelerated. When using a current compliance, the effect is very similar. At $V = V_{\mathrm{Set}}$ an active current compliance takes effect when $R_{\mathrm{element}} \leq V_{\mathrm{Set}}/I_{\mathrm{CC}}$, lowering the element voltage V_{element} correspondingly. Since the element voltages are only $50\% \cdot V_{\mathrm{Set}}$ at $R_{\mathrm{element}} = 0.5 \cdot V_{\mathrm{Set}}/I_{\mathrm{CC}}$, the element resistance change is very slow, similar to the series resistor case. For better comparabilty, an equivalent series resistance of the current compliance can then be defined as:

$$R_{\mathrm{ser}} \approx 0.5 \cdot \frac{V_{\mathrm{Set}}}{I_{\mathrm{CC}}} \tag{3.3}$$

According to series resistance or CC influence, the model shown in Fig. 3.1 can be expanded to also model multilevel properties. In Fig. 3.2a, a BRS (element A)

with series resistance R_{ser} is shown. Here R_{LRS} is set to R_{ser} to fit experimental observations. In Fig. 3.2b, an implementation of an active current compliance circuit is depicted, lowering the applied voltage V_{in} to about $R_{\mathrm{ser}} \cdot I_{\mathrm{CC}}$ when reaching the current limit I_{CC}. The current limitation is provided by the following limiting function:

$$V\left(V_{\mathrm{in}}, I_{\mathrm{CC}}\right) = V_{\mathrm{in}} - V_{\mathrm{in}} \cdot \left(\frac{I_{\mathrm{A}}}{I_{\mathrm{CC}}}\right)^{n} \text{ with } n = 30 \tag{3.4}$$

As for the model in Fig. 3.2a, the R_{LRS} is set to R_{ser} in terms of equation (3.3). The following discussion deals with the results for both the model with a series resistor(Fig. 3.2a) and subsequently the model with a CC (Fig. 3.2b). In both cases, $V_{\mathrm{Set}} = 0.3\,\mathrm{V}$ and $V_{\mathrm{Reset}} = 0.08\,\mathrm{V}$ hold true. In Fig. 3.2c,d the resulting I-V curves for $R_{\mathrm{ser}} = 2.5\,\mathrm{k\Omega}$, $R_{\mathrm{ser}} = 5\,\mathrm{k\Omega}$ and $R_{\mathrm{ser}} = 10\,\mathrm{k\Omega}$ are depicted. Starting from HRS and eventually reaching $V_{\mathrm{Set}} = 0.3\,\mathrm{V}$ (Fig. 3.2d), the voltage V_{A} is decreased since at that point the series resistance takes half of the voltage drop. In LRS the series resistance has an additional effect: the reset voltage ($V_{\mathrm{Reset}} = 0.08\,\mathrm{V}$) is increased to $2 \cdot V_{\mathrm{Reset}}$ since only half of the applied voltage drop V_{in} is present at the element A in LRS, as can be seen in Fig. 3.2d. Note an important limitation of this modeling approach: increasing the voltage V_{in} after switching to LRS would result in a further decrease of R_{LRS} in real devices; this has not been considered in this basic model.

In Fig. 3.2e,f, I-V characteristics for simulation with an active current compliance are depicted. The selected equivalent series resistances correspond directly to values in Fig. 3.2c-d, leading to $I_{\mathrm{CC}} = 60\mu\,\mathrm{A}$, $I_{\mathrm{CC}} = 30\mu\,\mathrm{A}$ and $I_{\mathrm{CC}} = 15\mu\,\mathrm{A}$. When reaching V_{Set}, the voltage is lowered to about $0.5 \cdot V_{\mathrm{Set}}$ until the current becomes lower than the I_{CC} value. This is obvious for the I-V characteristic in Fig. 3.2f, but in cases where the x-axis visualizes the input voltage V_{in}, this fact is obscured (see Fig. 3.2e). Note that in most measurements done with active current compliances (see, for example, [29], Fig. 1) V_{in} and not the actual voltage V_{A} is depicted on the x-axis.

3.1.3 Basic Non-Ohmic Branch Model

To model a non-ohmic behavior in the LRS or HRS branch of a BRS, additional non-linearities (e.g., diodes) can be added to the model. Note: these diodes are an integral part of the BRS circuit model and do *not* represent series diodes, which could be added for a 1D1R simulation externally. The circuit model shown in Fig. 3.3a comprises a non-linear series resistance in the LRS branch (I.) as well as in the HRS branch (II.). The kind of non-linearity in LRS and HRS can be selected

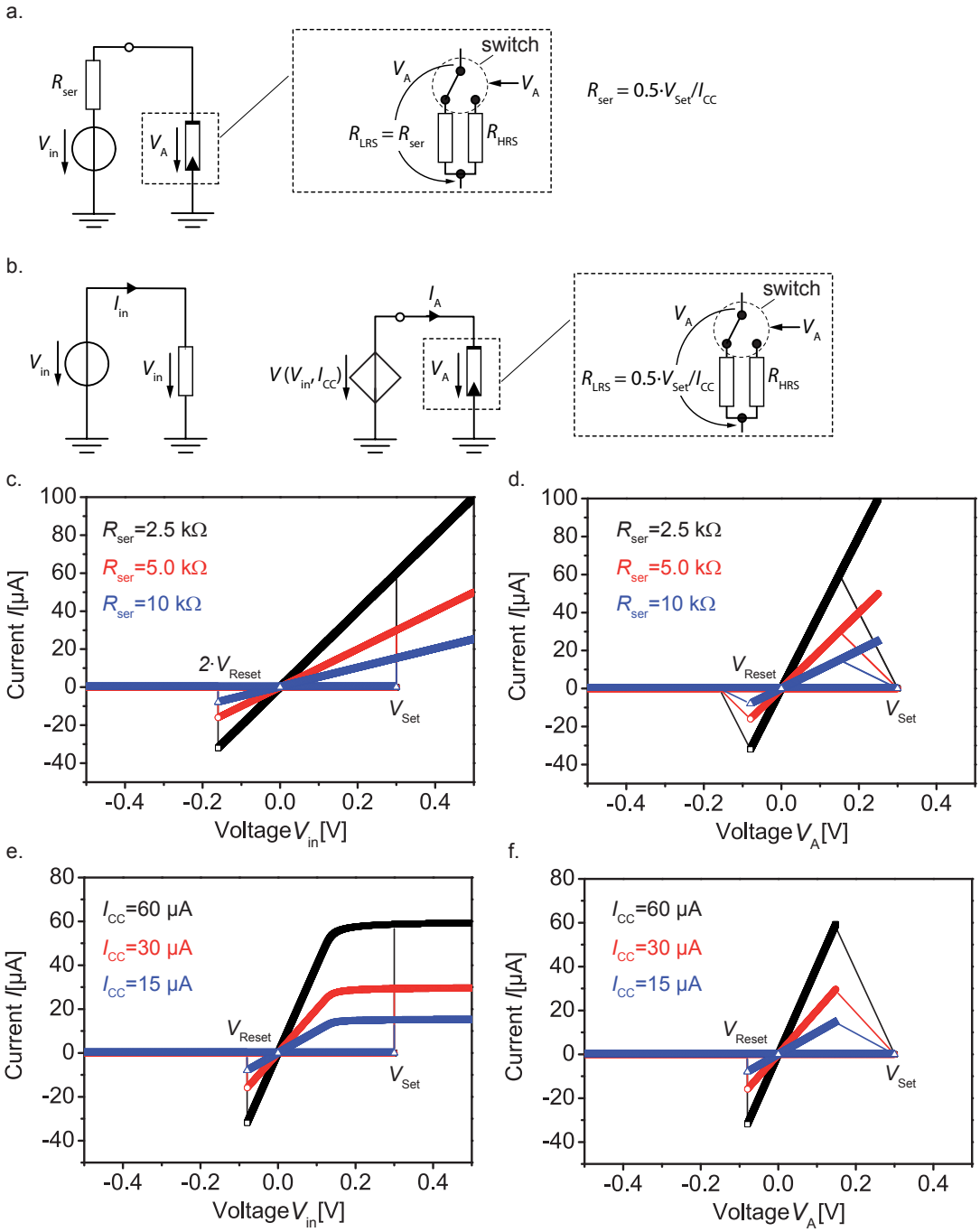


Figure 3.2: (a) Basic BRS multilevel model. The actual R_{LRS} is set to R_{ser}. (b) BRS multilevel model with current compliance. (c) I versus V_{in} for simulation with series resistor. (d) I versus V_{A} for simulation with series resistor. (e) I-V_{in} characteristic for simulation with current compliance. (f) I-V_{A} characteristic for simulation with current compliance.

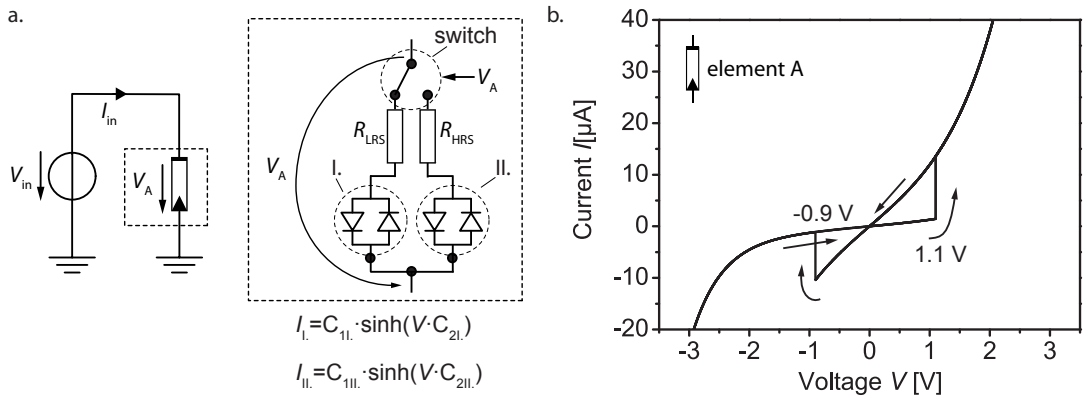


Figure 3.3: (a.) Circuit model with non-linear series resistance in LRS (I.) and HRS branch (II.). In these simulations, $C_{1I.} = 10^{-5}\,\mathrm{A}$, $C_{2I.} = 1\,\mathrm{V}^{-1}$ and $C_{1II.} = 10^{-7}\,\mathrm{A}$, $C_{2I.} = 2\,\mathrm{V}^{-1}$ were selected. (b) SPICE simulation of a resistive switch with fixed threshold voltages and built-in non-linearities.

individually (see also Fig. 3.3b):

$$I_{\mathrm{I.}} = C_{1\mathrm{I.}} \cdot \sinh(V \cdot C_{2\mathrm{I.}}) \tag{3.5}$$

$$I_{\mathrm{II.}} = C_{1\mathrm{II.}} \cdot \sinh(V \cdot C_{2\mathrm{II.}}) \tag{3.6}$$

Since threshold voltages are still fixed in this model, switching occurs at identical voltages as depicted in Fig. 3.1b. A model including non-linear behavior is useful to study the influence of non-ohmic branches on the crossbar array size [54, 55], but the I-V characteristic observed from this model differs from real devices, e.g., VCM elements (Fig. 2.5). Alternatively, dynamic modeling (see section 3.2.3) can be applied.

In conclusion, basic models of BRS elements can be developed from measured I-V data. In consequence, simulation results are always restricted to the underlying empirical instance, and thus do not reflect dynamic properties of a BRS element.

3.2 Dynamic Simulation Models

For dynamic simulations a system of differential equations describing the device behavior is needed. Such a dynamical system is then implemented in SPICE and used for simulations. Since the dynamical system should reflect the actual device physics in detail, the obtained simulation results are more general compared to basic device simulations (see section 3.1.1); but the model accuracy is crucial. For example, the dynamic model should reflect the influence of a current compliance or

series resistance (compare section 3.1.2) correctly.
Below, the dynamic systems approach is first introduced generally, and then several modeling approaches are illustrated.

3.2.1 Introduction of Dynamical Systems

A dynamical system can be represented by two equations:

$$\boldsymbol{y} = h(\boldsymbol{x}, \boldsymbol{u}, t) \tag{3.7}$$

$$\dot{\boldsymbol{x}} = f(\boldsymbol{x}, \boldsymbol{u}, t) \tag{3.8}$$

Equation (3.8) is the state equation and (3.7) the readout equation [93]. The functions $f(\cdot)$ and $h(\cdot)$ are non-linear and dependent on time t as well as on variables $\boldsymbol{x}$ and $\boldsymbol{u}$, which are multidimensional in general. The variable $\boldsymbol{x}$ stands for state of the system, the input variable $\boldsymbol{u}$ reflects external excitations, and $\boldsymbol{y}$ is the output or observation variable. This system-theoretical approach can be applied to arbitrary systems and is widely applied in electrical engineering.

Memristive Systems

A memristive system [30] is a special case of dynamical system (3.7)-(3.8) and displays a generic term for a complete class of two terminal devices. These devices are characterized by a so-called 'pinched hysteresis loop' (see Fig. 3.4, [94, 95]) and are non-linear in general. A memristive system is defined by the state-dependent Ohm's law and the state equation, which is multidimensional and time-dependent in general. Note that a memristor [96] is only a special case of a first-order memristive system where the state variable equals the flown charge ($x = q$).
The relevance of the memristive system approach results from the possibility to model dynamic device behavior of resistive switching elements. This was first recognized by the HP group in 2008 [31] and has triggered many groups to work on memristive circuit models [94]. For a memristive system, y and u are scalar values and y is a product of h and u:

$$y = h(\boldsymbol{x}, u, t) \cdot u \tag{3.9}$$

$$\dot{\boldsymbol{x}} = f(\boldsymbol{x}, u, t) \tag{3.10}$$

Equation (3.9) shows that y is always zero when u is zero, which corresponds to a Lissajous figure with a pinched hysteresis loop (Fig. 3.4). The definition of

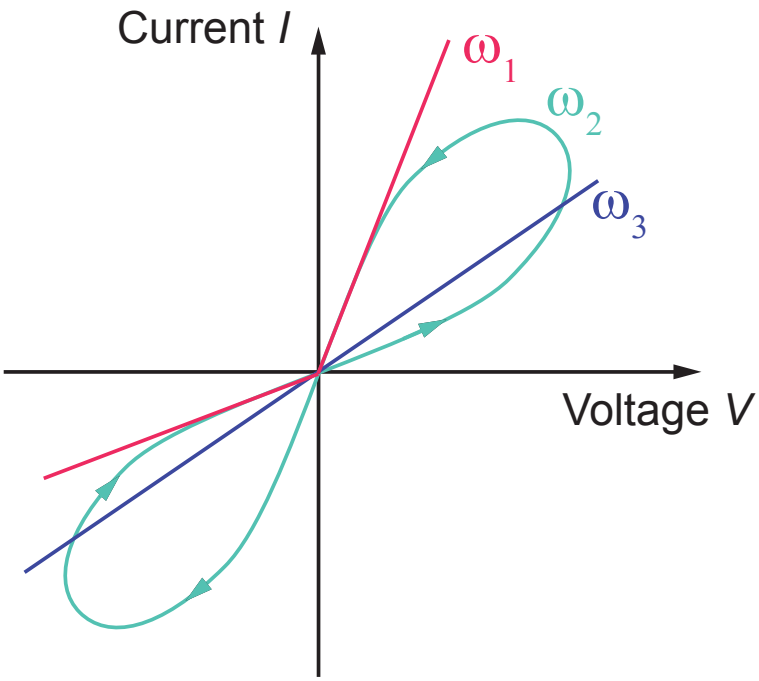


Figure 3.4: A pinched hysteresis I-V-loop is the identifying feature of a memristive system. For intermediate frequencies (e.g., ω_2) such a loop is visible. For very low frequencies ($\omega_1 \to 0$) a memristive system is indistinguishable from a non-linear resistance, while for very large frequencies ($\omega_3 \to \infty$) a memristive system is reduced to a linear resistance. For all frequencies the curves are pinched, which means that all curves run through the origin (0,0).

memristive systems was given in [30] and can be directly applied on two terminal electronic devices. Memristive systems can be either current controlled ($u = I$ and $h = R$) or voltage controlled ($u = V$ and $h = G$). In this case, u is the input variable, while y is the output variable. A current controlled memristive system reads

$$V = R(\boldsymbol{x}, I, t) \cdot I \tag{3.11}$$

$$\dot{\boldsymbol{x}} = f(\boldsymbol{x}, I, t), \tag{3.12}$$

while a voltage controlled memristive system reads

$$I = G(\boldsymbol{x}, V, t) \cdot V \tag{3.13}$$

$$\dot{\boldsymbol{x}} = f(\boldsymbol{x}, V, t). \tag{3.14}$$

Time-Invariant Memristive Systems

A memristive system is considered time-invariant when neither f nor R (or G) is time-dependent. This limitation leads to the more common description of memristive systems. A current controlled memristive system then reads

$$V = R(\boldsymbol{x}, I) \cdot I \tag{3.15}$$

$$\dot{\boldsymbol{x}} = f(\boldsymbol{x}, I). \tag{3.16}$$

The corresponding voltage controlled memristive system reads

$$I = G(\boldsymbol{x}, V) \cdot V \tag{3.17}$$

$$\dot{\boldsymbol{x}} = f(\boldsymbol{x}, V). \tag{3.18}$$

For modeling of bipolar resistive switches the time-invariant formulation is sufficient. Note that there are two additional conditions which must be fulfilled. To result in a pinched hysteresis loop

$$R(\boldsymbol{x}, 0) \neq \infty \tag{3.19}$$

and accordingly

$$G(\boldsymbol{x}, 0) \neq 0 \tag{3.20}$$

must hold [95]. Additionally, for a nonvolatile memory device

$$f(\boldsymbol{x}, 0) = 0 \tag{3.21}$$

must hold true, because no change of state should occur without external excitation. For modeling of resistive switches as a memristive system it is crucial to identify inner state variables. At least one state variable describing a structural change is needed, e.g., the length of a filament in electro-chemical metalization cells (ECM) (section 2.4.1).

Simple Time-Invariant Memristive Systems

In the simplest case the resistance R or conductance G, respectively, are only functions of the state variable $\boldsymbol{x}$ and, $\dot{\boldsymbol{x}}$ is only a function of current I or voltage V, respectively. The current controlled case is defined as

$$V = R(\boldsymbol{x}) \cdot I \tag{3.22}$$

$$\dot{\boldsymbol{x}} = f(I). \tag{3.23}$$

The voltage controlled case reads

$$I = G(\boldsymbol{x}) \cdot V \tag{3.24}$$

$$\dot{\boldsymbol{x}} = f(V). \tag{3.25}$$

This modeling approach was suggested in [31] and is used for SPICE implementation in section 3.2.2.

Memristor

A memristor is sometimes considered the forth passive circuit element [96] and is a special case of a memristive system. A memristor has only one state variable which is the flown charge $x = q$ in the current controlled case

$$V = R(q) \cdot I \tag{3.26}$$

$$\dot{q} = I. \tag{3.27}$$

In the voltage controlled case the magnetic flux is the state variable $x = \phi$

$$I = G(\phi) \cdot V \tag{3.28}$$

$$\dot{\phi} = V. \tag{3.29}$$

In general, bipolar resistive switches cannot be modeled as ideal memristors.

3.2.2 Simple Dynamic Linear Model

Several models in literature [97–100] are based on the basic memristive approach by the HP group [31], where a simple time-invariant memristive system (compare section 3.2.1) is considered. The memristive system from [31] reads:

$$V = R(w) \cdot I = ((R_{\mathrm{LRS}} - R_{\mathrm{HRS}}) \cdot \frac{w}{d} + R_{\mathrm{HRS}}) \cdot I \tag{3.30}$$

$$\dot{w} = C_1 \cdot I \text{ for } 0 \leq w \leq d \tag{3.31}$$

In this model, w is the state variable which corresponds to the length of a low ohmic region (R_{LRS}) with a maximum length of d, which is the thickness of the active layer. The region $d - w$ has a resistance of R_{HRS}, and C_1 is a fitting constant which depends on a dopant mobility in [31]. Since R_{LRS} and R_{HRS} are fixed values, linear

branches result in the LRS and HRS state, respectively. For simulation, the allowed range of w can be added to equation (3.31), as suggested in [100], leading to

$$\dot{w} = C_1 \cdot I \cdot [\sigma((d-w)\cdot \mathrm{sgn}(I)) + \sigma(-w \cdot \mathrm{sgn}(I))]\,, \tag{3.32}$$

where $\sigma(.)$ stands for the step-function and sgn(.) for the sign-function. For positive currents, w is increased until d is reached. Then, the change of state variable is set to zero until the current I changes sign. For negative currents, w decreases until $w = 0$ is reached. The change of the state variable is then set to zero until the sign of the current becomes positive again. Fig. 3.5a-b show the implemented circuit model and Fig. 3.6 shows a typical I-V characteristic resulting from this model. For simulation purposes, a triangular voltage V_{in} is applied to the element A, which

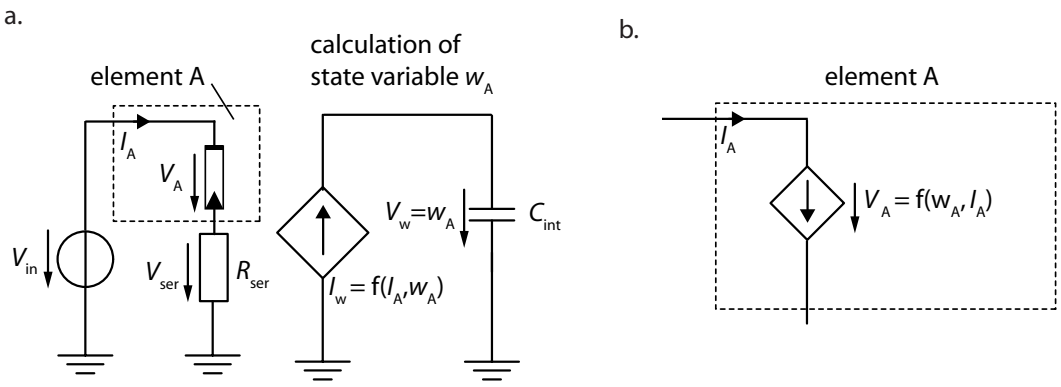


Figure 3.5: (a) Equivalent circuit. (b) The simple dynamic linear model is implemented as current-controlled voltage source.

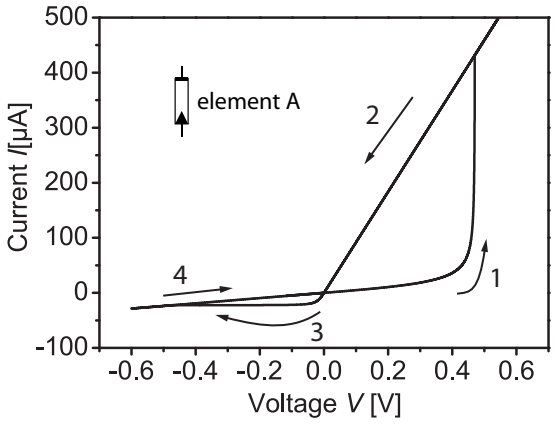


Figure 3.6: I-V characteristic of the simple dynamic linear element A. Adapted from [90].

is modeled as current controlled voltage source (equation (3.30), Fig. 3.5b). The state variable calculation is performed in an auxiliary circuit comprising a controlled current source representing equation (3.32) (with $\dot{w}_\mathrm{A} \mathrel{\widehat{=}} I_\mathrm{w}$) and an integration capacitor $C_\mathrm{int} = 1\,\mathrm{F}$ whose voltage drop V_w represents the state variable w_A:

$$V_\mathrm{w} = \frac{1}{C_\mathrm{int}} \cdot \int I_\mathrm{w} \mathrm{d}t = \frac{C_1}{1\,\mathrm{F}} \cdot \int I \mathrm{d}t \mathrel{\widehat{=}} w_\mathrm{A} \tag{3.33}$$

Within the range $0 \leq w \leq d$, equation (3.32) is reduced to

$$\dot{w} = C_1 \cdot I. \tag{3.34}$$

In consequence, the memristive system can be considered a memristor [96], which is a memristive system where the flown charge q is equal to the state variable (compare section 3.2.1):

$$V = ((R_\mathrm{LRS} - R_\mathrm{HRS}) \cdot \frac{q}{C_1 \cdot d} + R_\mathrm{HRS}) \cdot I \tag{3.35}$$

$$\dot{q} = I \tag{3.36}$$

The I-V characteristic in Fig. 3.6 looks similar to I-V characteristics of ECM elements. However, the model accuracy is limited, since there is no distinction between electronic current and ionic current in this model. As a consequence, the total current is integrated for state variable calculation; this is not realistic because only an ionic current leads to a mass transport. In section 4.3.3 the limitations of this model are highlighted by means of two element simulations.

3.2.3 Simple Dynamic Non-Linear Model

A simple dynamic model for bipolar resistive switches showing non-ohmic branches (compare section 3.1.3) can be constructed using the simple dynamic linear branch model (compare Fig. 3.7a,b). The memristive system reads:

$$I_\mathrm{A} = C_1 \cdot \sinh\left(V_\mathrm{A} \cdot C_2\right) \cdot \left(\frac{w_\mathrm{A}}{d} \cdot C_\mathrm{3,a} + \left(1 - \frac{w_\mathrm{A}}{d}\right) \cdot C_\mathrm{3,b}\right) \tag{3.37}$$

$$\dot{w}_\mathrm{A} = C_4 \cdot I_\mathrm{A} \cdot \left[\sigma\left((d - w_\mathrm{A}) \cdot \mathrm{sgn}(I_\mathrm{A})\right) + \sigma\left(-w_\mathrm{A} \cdot \mathrm{sgn}(I_\mathrm{A})\right)\right] \tag{3.38}$$

Constants are chosen as follows: $C_1 = 2.5 \cdot 10^{-7}\,\mathrm{A}$, $C_2 = 2\,\mathrm{V}^{-1}$, $C_\mathrm{3,a} = 1000$, $C_\mathrm{3,b} = 20$ and $C_4 = 3 \cdot 10^{-4}\mathrm{m/A}$. The active film thickness is $d = 10\,\mathrm{nm}$. A series resistance $R_\mathrm{ser} = 5\,\mathrm{k\Omega}$ was selected for the simulation. In Fig. 3.8a the resulting I-V characteristic is shown, while Fig. 3.8b depicts the change of state variables as

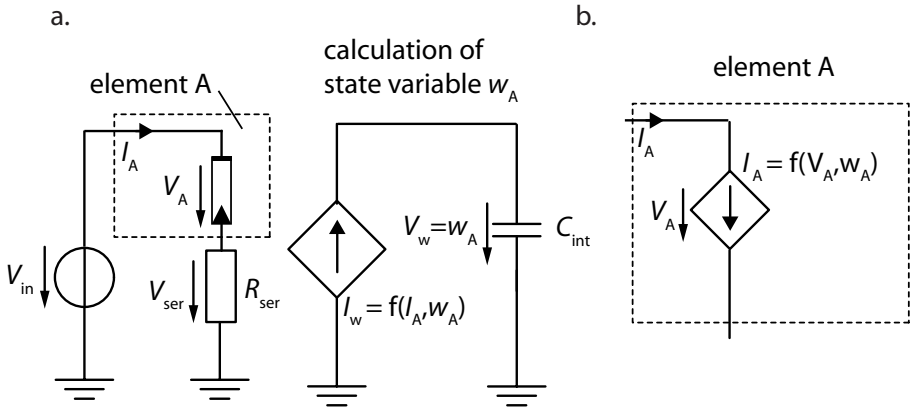


Figure 3.7: (a) The circuit model for a simple dynamic non-linear model simulation. (b) The element is modeled as a voltage-controlled current source.

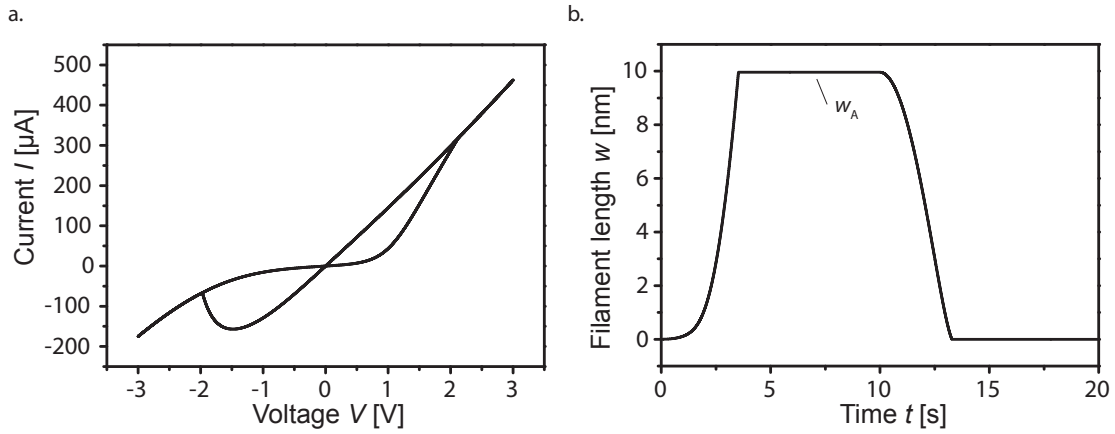


Figure 3.8: (a) I-V characteristic of a simple dynamic non-linear element. (b) State variable versus time graph.

a function of time t. The I-V characteristic has a shape similar to the measured curves of VCM elements (see Fig. 2.5), showing non-ohmic behavior in the LRS as well as HRS branch. Additionally, threshold voltage levels are also similar, but in contrast to the measured curve, there is no hard switching to LRS when reaching the set voltage in the simulated I-V characteristic.

Since no physics-based model is applied, the significance of results is limited. Additionally, a second state variable, namely the temperature, is assumed to be an important factor for VCM elements [101], and thus should be considered for dynamic modeling.

3.2.4 Dynamic ECM Model

To come up with more realistic models, the actual device kinetics must be implemented into the simulation model. With such a model, limitations of models which lack a sufficient accuracy in terms of device physics (see section 3.2.2) can be overcome. The model which is introduced here is based on simulations performed in [92] for ECM elements and assumes an electron-transfer mechanism at the interfaces which is described by the Butler-Volmer equation. Here, the same mechanisms for Set and Reset are assumed. Note that in some cases the reset mechanism could also be thermal [37].

Fig. 3.9a shows the applied equivalent circuit. The main circuit consists of a voltage source V_{in}, the dynamic ECM model (element A) and a series resistor R_{ser}. An auxiliary circuit is used for the state variable calculation with $I_{\mathrm{w}} = \dot{w}_{\mathrm{A}}$ and $V_w = w_{\mathrm{A}}$ (compare Fig. 3.5a), implementing a range limitation $0 \leq w \leq d = 2\,\mathrm{nm}$ akin to

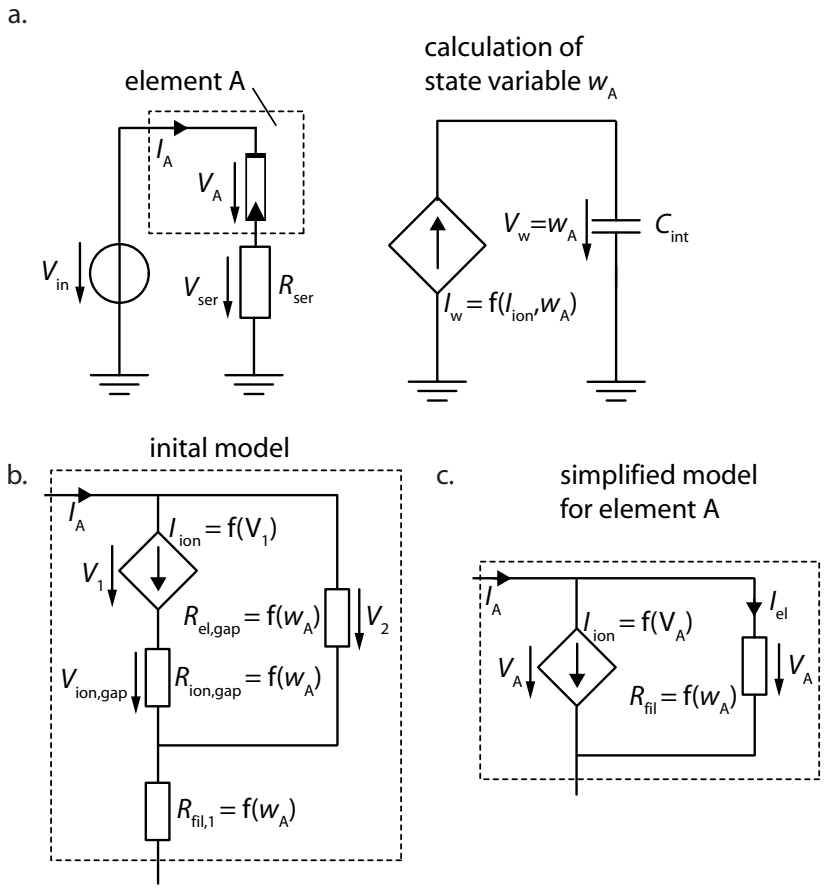


Figure 3.9: (a) Equivalent circuit for the dynamic ECM model. (b) Initial model adapted from [92]. (c) Simplified model used for simulation. Adapted from [90].

the linear model (equation (3.32)). The initial model (Fig. 3.9b) includes two paths, one for the ionic current I_{ion} and one for the electronic current I_{el}. Since two identical interfaces are assumed, both interfaces can be described by one current source (I_{ion} in Fig. 3.9b) using the Butler-Volmer equation [92]. For an asymmetry factor $\alpha = 0.5$ this results in

$$I_{\mathrm{ion}} = C_2 \cdot \sinh\left(\frac{z \cdot \eta}{2 \cdot V_{\mathrm{T}}}\right). \tag{3.39}$$

V_{T} is the temperature voltage ($\approx 25.8\,\mathrm{mV}$ at room temperature), $z = 2$ the number of involved electrons and $\eta = V_1/2$ the voltage at each interface. In the gap between filament and electrode the ionic resistance and the electronic resistance are given as

$$R_{\mathrm{ion,gap}} = \left(1 - \frac{w_{\mathrm{A}}}{d}\right) \cdot R_{\mathrm{ion},0} \tag{3.40}$$

and

$$R_{\mathrm{el,gap}} = \left(1 - \frac{w_{\mathrm{A}}}{d}\right) \cdot R_{\mathrm{fil,max}}, \tag{3.41}$$

respectively. The resistance of the filament is then

$$R_{\mathrm{fil}} = \frac{w_{\mathrm{A}}}{d} \cdot R_{\mathrm{fil},0}. \tag{3.42}$$

In equations (3.41) and (3.42) a linear dependence of resistance on the state variable w_{A} is assumed. This assumption was adopted from [31], where one high-resistive region (here: the gap) and one low-resistive region (here: the filament) were suggested for resistive switch modeling. Note that the validity of this assumption is limited to devices in which no tunneling barrier is present. In general, $R_{\mathrm{el,gap}}$ will be a highly non-linear function when tunneling is considered (see model refinement in section 3.2.5).
The resulting current equation reads:

$$I_{\mathrm{A}} = I_{\mathrm{ion}} + I_{\mathrm{el}} = C_2 \cdot \sinh\left(\frac{V_1}{2 \cdot V_{\mathrm{T}}}\right) + \frac{V_2}{R_{\mathrm{el,gap}}} \tag{3.43}$$

with

$$V_1 = V_{\mathrm{A}} - I_{\mathrm{ion}} \cdot R_{\mathrm{ion,gap}} - I_{\mathrm{A}} \cdot R_{\mathrm{fil}} \tag{3.44}$$

and

$$V_2 = V_{\mathrm{A}} - I_{\mathrm{A}} \cdot R_{\mathrm{fil}}. \tag{3.45}$$

For ease of simulation, the ECM model can be further simplified. By two simplifications, implicit dependencies in the equation (3.43) are removed, resulting in an explicit memristive system (compare section 3.2.1). The first one concerns the voltage drop $V_{\mathrm{ion,gap}}$ at $R_{\mathrm{ion,gap}}$. This voltage drop is small compared to V_1, the voltage drop at the interfaces, if the input voltage V_{in} is not too large. Correspondingly, the voltage drop $V_{\mathrm{ion,gap}}$ will be neglected for small to moderate input voltages. The second simplification is also related to a voltage drop resulting from the ionic current I_{ion}, in this case at the filament ($R_{\mathrm{fil},1}$). Since the voltage drop due to ionic current I_{ion} at $R_{\mathrm{fil},1}$ is small, this voltage drop can be neglected as well. This simplification is also valid for small to moderate input voltages. The resulting circuit model is depicted in Fig. 3.9c. The resistance R_{fil} is the sum of $R_{\mathrm{fil},1}$ and $R_{\mathrm{el,gap}}$:

$$R_{\mathrm{fil}} = R_{\mathrm{fil},1} + R_{\mathrm{el,gap}} = \frac{w_{\mathrm{A}}}{d} \cdot R_{\mathrm{fil},0} + (1 - \frac{w_{\mathrm{A}}}{d}) \cdot R_{\mathrm{fil,max}} \tag{3.46}$$

$R_{\mathrm{fil},0}$ ($= 1\,\mathrm{k\Omega}$) is the minimum resistance value and $R_{\mathrm{fil,max}}$ ($= 1\,\mathrm{M\Omega}$) is the maximum resistance value. For the sake of simplicity, a cylindric filament with a radius of 2 nm is assumed (compare [102]). The constant C_2 is calculated from an assumed exchange current density $j_0 = 10^{-2}\mathrm{A/m^2}$ and a filament area $A_{\mathrm{fil}} = \pi \cdot (2\,\mathrm{nm})^2 = 1.257 \cdot 10^{-17}\,\mathrm{m^2}$ to

$$C_2 = 2 \cdot j_0 \cdot A_{\mathrm{fil}} = 2.5 \cdot 10^{-19}\,\mathrm{A}. \tag{3.47}$$

C_1 depends on the elementary charge e, the atomic mass of Cu $M_{\mathrm{Cu}} = 63.546\,\mathrm{g\ mol^{-1}}/N_{\mathrm{A}}$, the mass density of Cu $\rho_{\mathrm{Cu}} = 8.92 \cdot 10^6 \frac{\mathrm{g}}{\mathrm{m^3}}$, and the filament area A_{fil}

$$C_1 = \frac{M_{\mathrm{Cu}}}{2 \cdot e \cdot \rho_{\mathrm{Cu}} \cdot A_{\mathrm{fil}}} = 2.93 \cdot 10^6 \frac{\mathrm{m}}{\mathrm{A}}. \tag{3.48}$$

Due to applied simplifications, $V_1 = V_{\mathrm{A}}$ and $V_2 = V_{\mathrm{A}}$ hold true, leading to the final memristive system (compare Fig. 3.9c)

$$\begin{aligned} I_{\mathrm{A}} &= G(w_{\mathrm{A}}, V_{\mathrm{A}}) = C_2 \cdot \sinh\left(\frac{V_{\mathrm{A}}}{2 \cdot V_{\mathrm{T}}}\right) + \frac{V_{\mathrm{A}}}{R_{\mathrm{fil}}} \qquad (3.49)\\ &= \left(\frac{C_2}{V_{\mathrm{A}}} \cdot \sinh\left(\frac{V_{\mathrm{A}}}{2 \cdot V_{\mathrm{T}}}\right) + \frac{1}{\frac{w_{\mathrm{A}}}{d} \cdot R_{\mathrm{fil},0} + \left(1 - \frac{w_{\mathrm{A}}}{d}\right) \cdot R_{\mathrm{fil,max}}}\right) \cdot V_{\mathrm{A}} \\ \dot{w}_{\mathrm{A}} &= f\left(w_{\mathrm{A}}, V_{\mathrm{A}}\right) = C_1 \cdot I_{\mathrm{ion}} \cdot \left[\sigma\left((d - w_{\mathrm{A}}) \cdot \mathrm{sgn}(I_{\mathrm{ion}})\right) + \sigma\left(-w_{\mathrm{A}} \cdot \mathrm{sgn}(I_{\mathrm{ion}})\right)\right] \qquad (3.50)\\ &\text{with } I_{\mathrm{ion}} = C_2 \cdot \sinh\left(\frac{V_{\mathrm{A}}}{2 \cdot V_{\mathrm{T}}}\right) \qquad (3.51) \end{aligned}$$

which results in an ECM I-V characteristic, as shown in Fig. 3.10a. This system is in accordance with equation (3.17) and (3.18) and satisfies equation (3.21) since

$\sinh(0) = 0$. Because of $\lim_{x \to 0} (\sinh(x)/x) = 1$ equation (3.20) holds true, too. Note that the change of state variable ($\dot{w}_{\mathrm{A}}$) in equation (3.50) is controlled by the ionic current I_{ion}, and the readout current I_{A} in equation (3.49) is dominated by the electronic current I_{el}.

The influence of a series resistor on I-V characteristics is shown in Fig. 3.10b. A small R_{ser} results in a very asymmetric I-V characteristic, while a larger R_{ser} leads to a more symmetric I-V characteristic.

In order to suit certain circumstances, this model can also be used to simulate multilevel properties (see Fig. 3.11a). In case of a large current compliance (e.g.,

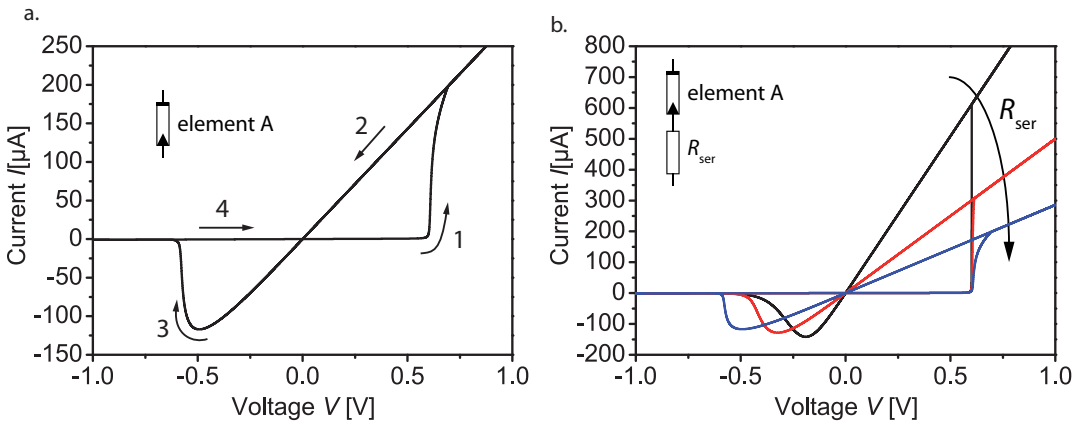


Figure 3.10: (a) I-V characteristic of a single element with $R_{\mathrm{ser}} = 2500\ \Omega$ using the dynamic ECM model. (b) I-V characteristic of a single element for $R_{\mathrm{ser}} = 0\ \Omega$, $R_{\mathrm{ser}} = 1000\ \Omega$ and $R_{\mathrm{ser}} = 2500\ \Omega$. Adapted from [90].

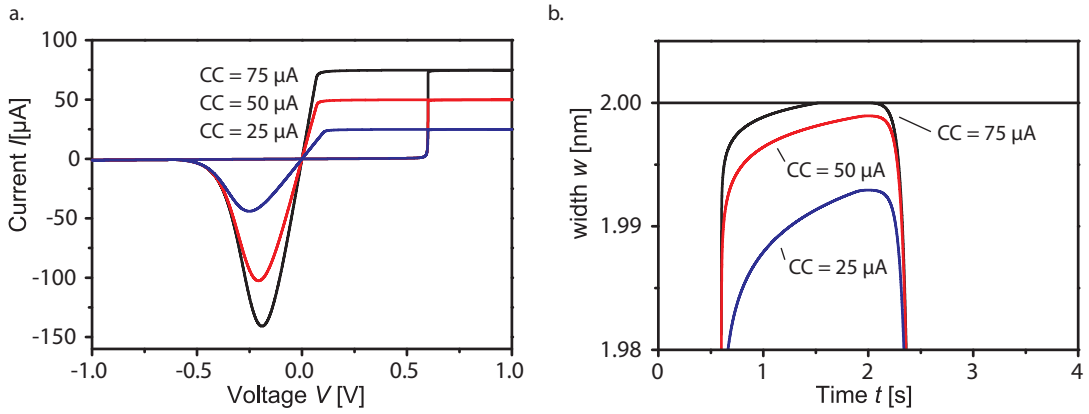


Figure 3.11: Dynamic ECM model simulations with different current compliance values. (a) I-V characteristic of a single element for CC of 25 μA, 50 μA and 75 μA. (b) Width w versus time t. For CC of 25 μA, 50 μA very small gap sizes remain, while for 75 μA the filament reaches the counter electrode completely.

75μA in Fig. 3.11a) or a small series resistor, a direct contact results, while for large R_{ser} or low current compliance (25μA and 50μA in Fig. 3.11a) values the filament does not reach the counter electrode directly (Fig. 3.11b). But the remaining gap sizes are unrealistically small and there is still a strong change in gap size after reaching the current compliance which is not present in real devices (see Fig. 3.11b). In conclusion, this model is capable of modeling BRS dynamics, including the shift in threshold voltages, while electronic resistance is not correctly modeled for systems having a tunneling barrier. This issue is solved with the refined model in the next paragraph.

3.2.5 Refined Dynamic ECM Model

In [102], a refined ECM model was proposed which accounts for a tunneling barrier, and hence reflects a more accurate physics-based model. This model modification is used below for reimplementation of the electronic current I_{el} as a tunneling current. According to [103], the tunnel equation for intermediate voltages reads:

$$\begin{aligned} I_{\mathrm{el}} =& \frac{e^2}{2\pi h} \cdot \frac{1}{g^2} \cdot \exp\left(-\frac{4\pi\sqrt{2mE_{\mathrm{b}}}}{h} \cdot g \cdot \sqrt{1-\frac{eV}{2E_{\mathrm{b}}}}\right) \cdot \left(E_{\mathrm{b}} - \frac{eV}{2}\right) \\ & - \frac{e^2}{2\pi h} \cdot \frac{1}{g^2} \cdot \exp\left(-\frac{4\pi\sqrt{2mE_{\mathrm{b}}}}{h} \cdot g \cdot \sqrt{1+\frac{eV}{2E_{\mathrm{b}}}}\right) \cdot \left(E_{\mathrm{b}} + \frac{eV}{2}\right) \end{aligned} \tag{3.52}$$

For better comparability the same parameters as provided in [102] are assumed for the SPICE implementation. In equation (3.52), $E_{\mathrm{b}} = 3.6\,\mathrm{eV}$ is the barrier height, $m = 0.86 \cdot m_0$ is the effective electron mass and h is the Planck constant. Note that equation (3.52) is dominated by the exponential dependency on the gap width $g = d - w$, leading to large tunneling currents for small gap sizes. Thus, if a series resistor or current compliance is present, the voltage at the ECM element decreases at a certain point. This decrease of the voltage drop leads to a strong self-limitation of the minimum gap width due to an exponential decrease of the ionic current I_{ion} (equation (3.51)) accompanied by a change of the gap size $\dot{g}$ (compare equation (3.50)).

The resistance of the electrodes as well as the filament resistances add up to $R_{\mathrm{ser}*}$ and are not considered separately (Fig. 3.12a,b). The assumed geometry is depicted in Fig. 3.12c with an oxide thickness of $d = 20\,\mathrm{nm}$ SiO_2. The filament radius is again assumed to be $r = 2\,\mathrm{nm}$, hence C_1 and C_2 have the same values as defined in

equation (3.47) and (3.48). With equation (3.52) the new memristive system reads (compare Fig. 3.12a,b):

$$I_{\mathrm{A}} = G(w_{\mathrm{A}}, V_{\mathrm{A}}) = C_2 \cdot \sinh\left(\frac{V_{\mathrm{A}}}{2 \cdot V_{\mathrm{T}}}\right) + \frac{V_{\mathrm{A}}}{R_{\mathrm{tun}}} \tag{3.53}$$

$$\dot{w}_{\mathrm{A}} = f\,(w_{\mathrm{A}}, V_{\mathrm{A}}) = C_1 \cdot C_2 \cdot \sinh\left(\frac{V_{\mathrm{A}}}{2 \cdot V_{\mathrm{T}}}\right) \tag{3.54}$$

To assure that the filament length cannot turn negative and to include the contact case with a fixed LRS value, a range limit for g, e.g., $g_{\min} = 0.142\,\mathrm{nm} \leq g \leq d$, can be added to equation (3.54) (compare equation (3.50)).
Fig. 3.13a shows a typical I-V characteristic with a current compliance of 10 μA for voltage ramps of 0.1 V/s, 1 V/s and 10 V/s. The curve for 1 V/s resembles the

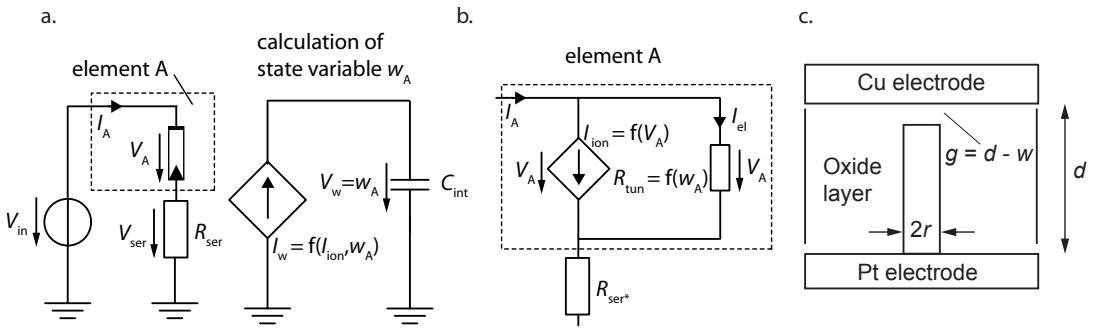


Figure 3.12: (a),(b) Equivalent circuit model for the refined dynamic ECM model. (c) Geometry of electrodes and filament assumed.

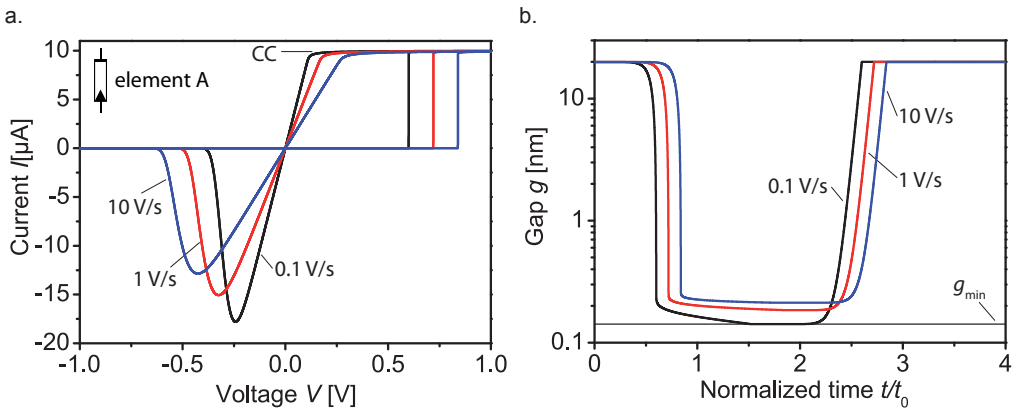


Figure 3.13: (a) Single element simulation with $I_{\mathrm{CC}} = 10\mu$A for the refined dynamic ECM model. Simulation is conducted for voltage ramps of 0.1 V/s, 1 V/s and 10 V/s. (b) Gap size g versus normalized time t/t_0. Values for t_0 are $t_0 = 10\,\mathrm{s}$, $t_0 = 1\,\mathrm{s}$ and $t_0 = 0.1\,\mathrm{s}$. Note that in the non-normalized depiction the slopes of g in CC are identical.

curve shown in [102], Fig. 2a. In Fig. 3.13b the gap size is depicted showing a self limitation depending on applied voltage ramps. For the slowest ramp (0.1 V/s) there is contact ($g = g_{\mathrm{min}}$), while for faster ramps a tunneling gap remains. This is because of different dwell times in current compliance.

In Fig. 3.14 the fast switching capability of ECM elements becomes visible. In Fig. 3.14a the input voltage V_{in} is a pulse with a width of 1 ns and an amplitude of 2 V. For this simulation a series resistor of $R_{\mathrm{ser}} = 25\,\mathrm{k\Omega}$ was applied. In Fig. 3.14a the voltage drop V_{A} at the element A as well as the voltage drop at the series resistor V_{ser} are depicted, showing a switching from HRS to LRS in less than one nanosecond. Due to the series resistor, the voltage drop at element A is lowered when the switching takes place, which leads to a deceleration in resistance change. By having a look at Fig. 3.14b, this property becomes obvious for a 10 ns pulse with the same amplitude of 2 V. After the initial switching event, there is a decrease in voltage drop at element A. Correspondingly, the resistance of element A is lowered continuously. From this behavior, the empirical observations which were used in section 3.1.2 for multilevel modeling ($R_{\mathrm{element}} \approx R_{\mathrm{ser}}$) can be understood.

In Fig. 3.15a the correlation between current compliance and R_{LRS} is depicted showing a very good agreement of this model with respect to experimental data [102]. Hence, arbitrary multilevel simulations are possible with this dynamic model by setting a current compliance or using a series resistor.

Beside multilevel property, the change in threshold voltage (compare Fig. 3.13a) is a direct result of the dynamic model. In Fig. 3.15b the simulated threshold voltages $V_{\mathrm{th,Set}}$ for several sweep rates s are shown (black squares). For a given sweep rate s,

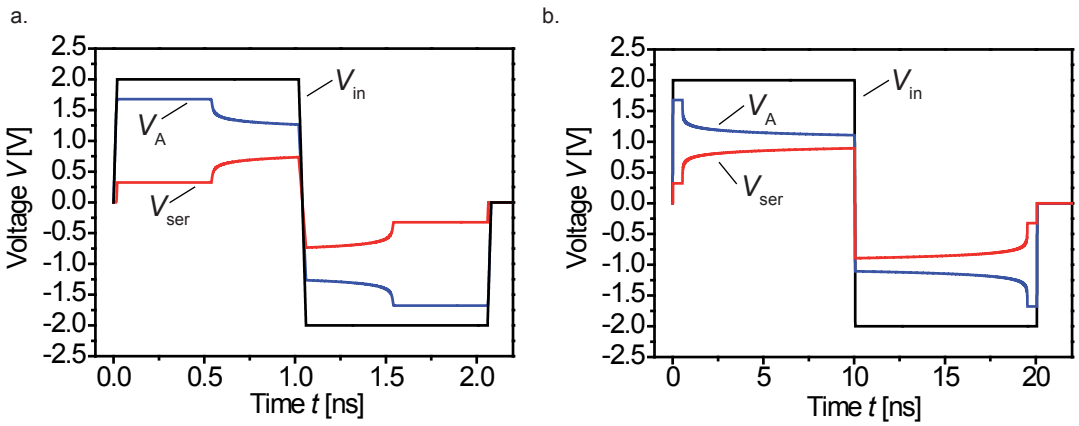


Figure 3.14: (a) 2 V, 1 ns pulse simulation of an ECM element A using the refined dynamic ECM model. A series resistor of $R_{\mathrm{ser}} = 25\,\mathrm{k\Omega}$ is applied. (b) 2 V, 10 ns pulse simulation.

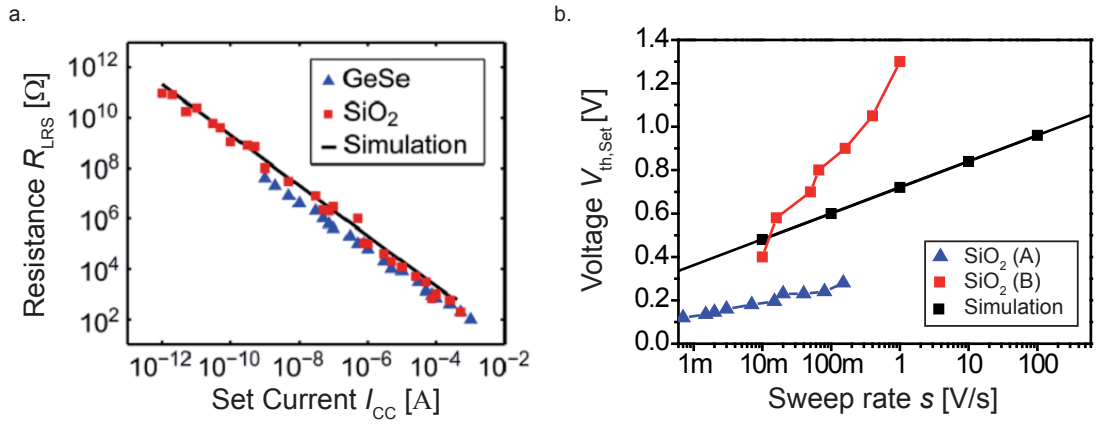


Figure 3.15: (a) Low resistance R_{LRS} versus set current I_{CC} for the refined dynamic ECM simulation model and measurements from Ag/GeSe and Cu/SiO_2 ECM elements. Reproduced with permission from [102]. (b) $V_{\mathrm{th,Set}}$ as function of sweep rate s for the Cu/SiO_2 ECM simulation model and Cu/SiO_2 measurement data from [104] (SiO_2 (A)) and [91] (SiO_2 (B)).

$V_{\mathrm{th,Set}}$ can also be calculated analytically (black line in Fig. 3.15b). The equation reads

$$V_{\mathrm{th,Set}} = \ln\left(\frac{s \cdot d}{C_1 \cdot C_2 \cdot V_{\mathrm{T}}}\right) \cdot 2 \cdot V_{\mathrm{T}}. \tag{3.55}$$

This equation is derived from the following considerations. First, the ionic current I_{ion} in equation (3.50) is replaced by equation (3.51). Next, the state variable w is calculated by integration as follows:

$$w_{\mathrm{Set}} = C_1 \cdot C_2 \cdot \int_0^{t_{\mathrm{Set}}} \sinh\left(\frac{s \cdot t}{2 \cdot V_{\mathrm{T}}}\right) \mathrm{d}t \tag{3.56}$$

$$s \cdot w_{\mathrm{Set}} = C_1 \cdot C_2 \cdot 2 \cdot V_{\mathrm{T}} \cdot \left(\cosh\left(\frac{s \cdot t_{\mathrm{Set}}}{2 \cdot V_{\mathrm{T}}}\right) - 1\right) \tag{3.57}$$

$$\frac{s \cdot d}{C_1 \cdot C_2 \cdot 2 \cdot V_{\mathrm{T}}} \approx 0.5 \cdot \exp\left(\frac{s \cdot t_{\mathrm{Set}}}{2 \cdot V_{\mathrm{T}}}\right) \tag{3.58}$$

Note that $w_{\mathrm{Set}} \approx d = 20\,\mathrm{nm}$ holds true for switching to LRS, and $\cosh(.) - 1$ is approximated by $0.5 \cdot \exp(.)$ in equation (3.58). With $V_{\mathrm{th,Set}} = s \cdot t_{\mathrm{Set}}$ and a transposition of equation (3.58), the final equation (3.55) results. As depicted in Fig. 3.15b the analytical curve fits the simulated values very well.
Additionally, empirical data from [104] and [91] is included to Fig. 3.15b, showing a strong mismatch between measurement data for Cu/SiO_2-based ECM elements from both [104] (SiO_2 (A)) and [91] (SiO_2 (B)) as well as the simulation data. The

large mismatch in measurement data evokes questions concerning the underlying reasons. Firstly, the measurement data for Cu/SiO_2-based ECM elements offers a great variation in actual values (compare [91]), thus data reliability is low for this kind of measurements. Secondly, although using Cu/SiO_2 plus an inert electrode in both cases, differences in device fabrication seem to have an essential impact on device behavior, thus further studies on device fabrication are needed. However, as a result it can be noted that simulations show the same trend as the measurement data, which is an increase of threshold voltage with the sweep rate. Note that in equation (3.39) an asymmetry factor $\alpha = 0.5$ was assumed to keep considerations simple. By adjusting this asymmetry factor, the slope in Fig. 3.15b could be fitted to each measurement data, either SiO_2 (A) or SiO_2 (B).

3.3 Conclusion

In this chapter, two basic and four dynamic models for bipolar resistive switches were introduced. All models are implemented in SPICE and can be used for circuit simulations.

The basic linear branch model is suited to describe ECM element behavior for quasi-static conditions. Multilevel properties can be emulated for a known current compliance or a series resistor, but no dynamic simulations are available. The basic non-ohmic branch model can be used to study the influence of non-ohmic branches, but simulated I-V characteristics differ from VCM element measurements.

For dynamic simulation, the simple dynamic linear model introduced by Strukov [31] is presented as a reference model. Although very simple, the model is capable of approximating bipolar resistive switching behavior. Note: it will be demonstrated in the course of chapter 4 that this model is not capable of simulating two anti-serially connected elements correctly, revealing the limitations of this model.

The simple dynamic non-linear model is educed from the linear model to provide non-ohmic behavior in the I-V characteristic to reproduce VCM element behavior. Simulation results can be improved by this model, but since physical accuracy of the model is lacking, the applicability is limited.

To allow for more realistic simulations, a dynamic ECM model based on a physical model by Menzel [92] was implemented. In this first ECM model, the linear dependency of resistance on the state variable is retained, leading to one stable ON state. The resulting I-V characteristics show the suitability of this approach, but a more sophisticated modeling of the electronic current is needed.

The refined dynamic ECM model as is an implementation of Menzel's novel ECM

model [102], which uses a tunneling equation for electronic current modeling, hence no linear dependency of the resistance on the state variable is assumed. By comparison to measurement data, it can be seen that this model is capable of simulating multilevel behavior with very high accuracy. As in measurements, the threshold voltage increases logarithmically with the voltage sweep rate, but more accurate measurements are required to be able to extract the correct model parameters.

All models presented in this chapter will be used in chapter 4 for a simulation of anti-serially connected bipolar resistive switches and will be reviewed in terms of their ability to reproduce the expected behavior.

4 Complementary Resistive Switches

Complementary resistive switches (CRS) are a completely new concept to address the sneak path problem (see section 2.7) in passive crossbar arrays [50]. A CRS cell can be built of any bipolar resistive switch, either ECM (see section 2.4.1) or VCM elements (see section 2.4.2).
The chapter is organized as follows: in section 4.1, the basic properties of a CRS cell are illustrated, and in section 4.2 proof-of-concept measurements are shown. In section 4.3, models from chapter 3 are then used for analysis of anti-serially connected elements.

4.1 Basic Sweep Properties

The following will illustrate the basic functionality by means of an ECM-based CRS cell. Initially, a symmetric I-V characteristic with $|V_{\mathrm{Set}}| = |V_{\mathrm{Reset}}|$ is assumed. ECM element A consists of a Pt-bottom electrode, a solid electrolyte layer and an oxidizable top electrode like Cu (Fig. 4.1a) with a bipolar I-V characteristic (Fig. 4.1b). If we apply a triangular voltage sweep and start in the high-resistive state (HRS), the element switches to the low-resistive state (LRS) when the set Voltage V_{Set} is reached (① in Fig. 4.1b). For voltages larger than V_{Reset} the element stays low-resistive. To reset the element to the high-resistive state, a negative voltage $V < V_{\mathrm{Reset}}$ is needed (② in Fig. 4.1b). If considering an element B with reversed layer order, i.e., Cu-bottom electrode, solid electrolyte layer and Pt-top electrode (Fig. 4.1c), an I-V characteristic which is anti-symmetric with respect to the origin results (Fig. 4.1d). Starting from the LRS, the element switches to the HRS when reaching the reset voltage V_{Reset} (Fig. 4.1d ①). For positive voltages and voltages larger than V_{Set} the element stays high-resistive. At V_{Set} the element switches back to LRS (Fig. 4.1d ②).
Merging the two resistive elements to one CRS (Fig. 4.1e) results in a superimposed I-V characteristic (Fig. 4.1f). The CRS constitutes a voltage divider and if, for example, element B is in the LRS and element A in the HRS, almost all voltage drops at element A until $V_{\mathrm{th},1}$ is reached. At this point (Fig. 4.1f ①), element A switches to the LRS (see Fig. 2d) and element B remains in the LRS (see Fig. 2b),

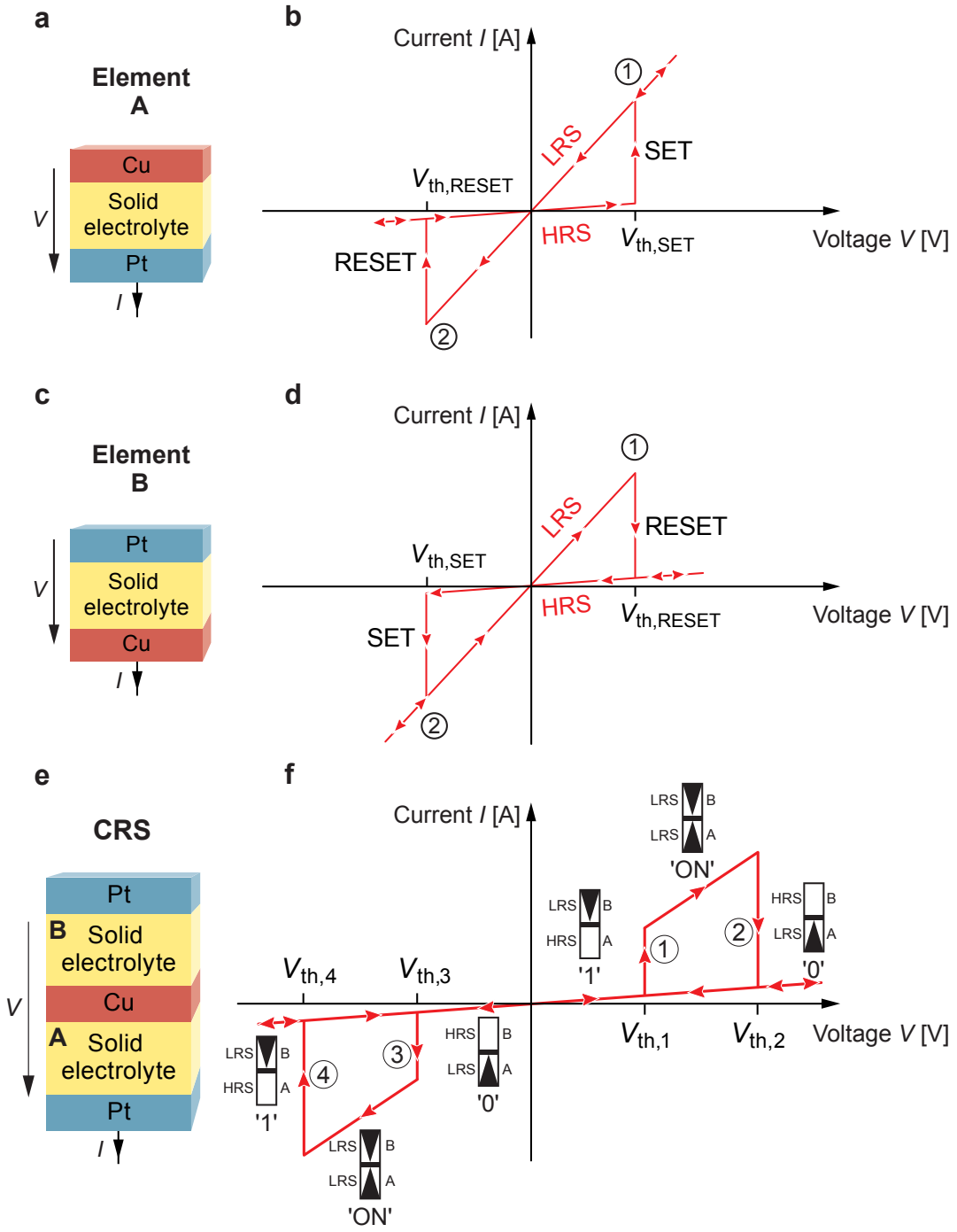


Figure 4.1: (a) Element A with a Cu / solid electrolyte / Pt stack. (b) *I-V* characteristic of element A. The resistance can be toggled between the LRS and HRS by exceeding V_{SET} and V_{RESET}. (c) Bipolar resistive element B with a Pt / solid electrolyte / Cu stack. (d) *I-V* characteristic of element B. e) CRS resulting from the combination of element B and A. f) *I-V* characteristic of the CRS cell. Adapted from [50].

because the potential drop at B is far below $V_{\mathrm{th,RESET}}$. The CRS state is defined as 'ON' with now both elements being low-resistive and having an equal voltage drop. If the voltage reaches $V_{\mathrm{th},2}$ (Fig. 4.1f ②) element B becomes high-resistive, because this is equivalent to a voltage drop of $V_{\mathrm{th,RESET}}$ at element B. This state is defined as '0'. For voltages larger than $V_{\mathrm{th},2}$, the element B stays high-resistive and element A low-resistive. If a potential V comes within range of $V_{\mathrm{th},4} < V < V_{\mathrm{th},3}$ (Fig. 4.1f ③), the high-resistive element B switches to the low-resistive state and both elements in the CRS are in LRS (state 'ON'). If the negative potential exceeds $V_{\mathrm{th},4}$, element A switches back to HRS (Fig. 4.1f ④) and the resulting state is '1'. If a CRS is in the 'OFF' state initially, an initialization process is needed to switch the CRS to state '1' or '0' by application of a voltage $V < 2V_{\mathrm{th},3}$ or $V > 2V_{\mathrm{th},1}$, respectively (see section 4.3.1 for details on initialization). All possible states are summarized in table 4.1. The overall small-voltage resistance of a CRS, no matter if a '0' or '1' is stored, is always high:

$$R_{\mathrm{CRS}} = R_{\mathrm{HRS}} + R_{\mathrm{LRS}} \sim R_{\mathrm{HRS}} \tag{4.1}$$

The CRS utilizes essentially the same principle as a CMOS inverter, where one of the transistors is always OFF, which led to the tremendous success of the CMOS technology in the last thirty years. It follows that, in contrast to previous crossbar concepts (2.6), the total resistance of the memory becomes independent of the stored information pattern and is well defined from the beginning. More details on crossbar arrays can be found in chapter 2.6.
To understand the quasi-static I-V characteristic of a CRS cell in detail, it is favorable to take a closer look at the voltage drop at each bipolar resistive element. The

CRS state	Element A	Element B	CRS
1	HRS	LRS	≈ HRS
0	LRS	HRS	≈ HRS
ON	LRS	LRS	LRS+LRS
OFF	HRS	HRS	>> HRS

Table 4.1: CRS logic states.

same threshold voltages are assumed for Set and Reset to simplify the consideration. In Fig. 4.2 a triangular voltage sweep is shown, and characteristic threshold voltage levels are marked by colored circles and are numbered from ① to ④. In Fig. 4.2b corresponding points of the CRS I-V characteristic are marked. Because switching takes place at the marked points, two circles are needed to identify the point before switching (a.) and after switching (b.). These numbers correspond directly to the numbers in Fig. 4.1f and can also be found in the detailed I-V characteristics of element A and B in Fig. 4.2c and 4.2d, respectively. Initially, element A is high-resistive and element B is low-resistive, hence the complete voltage drop is at element A, while there is almost no voltage drop at element B. When reaching point (① a.), element A switches to the LRS and both elements suffer an identical voltage drop of $0.5 \cdot V_{\mathrm{th},1}$ (① b.). Thus, the switching of element A leads to a sudden voltage jump at element B. A further increase in voltage V results in a current increase until point (② a) is reached. Element B switches to the HRS at this point, hence

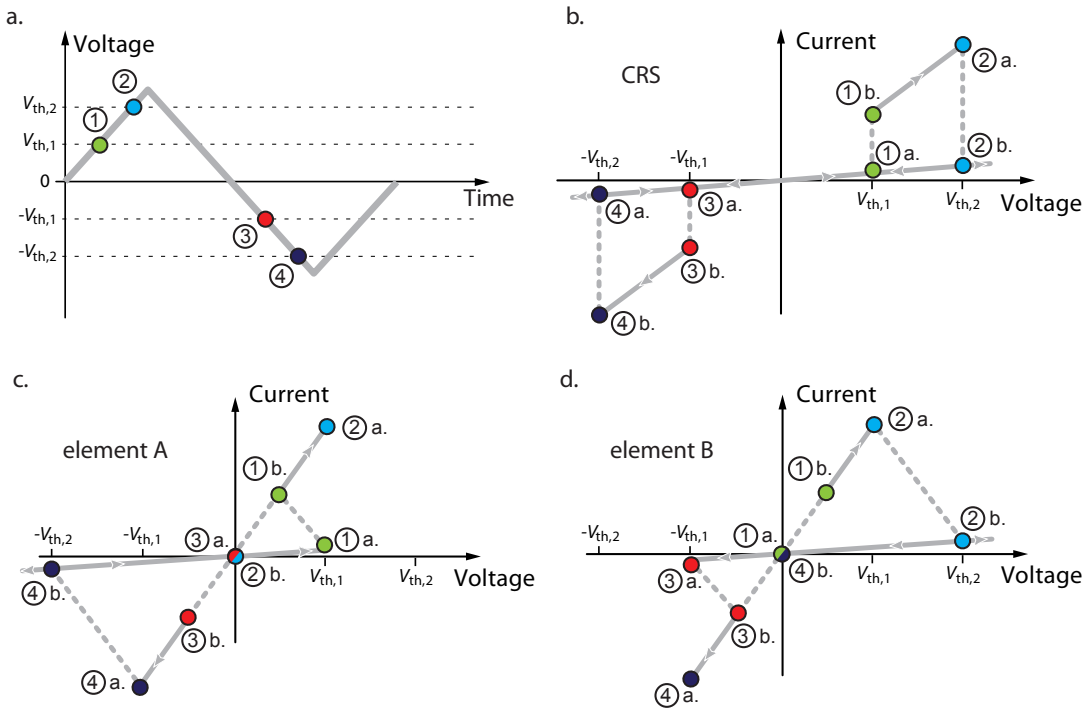


Figure 4.2: (a) Triangular voltage sweep. Relevant switching voltages $V_{\mathrm{th},1}$, $V_{\mathrm{th},2}$, $-V_{\mathrm{th},1}$ and $-V_{\mathrm{th},2}$ are marked with numbers ① to ④. (b) CRS I-V switching curve. Numbers correspond to numbers in (a). Dotted lines indicate a current jump from, e.g., (① a.) to (① b.). (c) Detailed current voltage curve of element A in CRS configuration. Changes in voltage drop at switching events ① to ④ become visible. (d) Detailed current voltage curve of element B in CRS configuration.

the complete voltage drop is at element B, while there is no voltage drop at element A (②b.). When the voltage sweep reaches point (③a.), element A switches to the LRS and the voltage drop at element B is suddenly increased to $-0.5 \cdot V_{\mathrm{th},1}$, while voltage at element A is lowered to $-0.5 \cdot V_{\mathrm{th},1}$ (③b.). Further increase in voltage results in linear current increase until (④a.) is reached. At this point, element A switches to the HRS, resulting in a complete voltage drop at element A.

4.2 Experimental Verification

4.2.1 Connected ECM Elements

To prove the CRS concept, single GeSe-based ECM elements (30 nm Pt / 3 nm SiO_2, 25 nm GeSe / 70 nm Cu) were connected anti-serially [50]. Details on the fabrication of single elements can be found in [39], and a typical characteristic of such elements is shown in Fig. 2.4a. In the CRS setup, a triangular voltage sweep is applied to the series connection of two ECM elements with opposite resistance state and an additional series resistor R_{ser} (Fig. 4.3a). The I-V measurement in Fig. 4.3b shows exactly the predicted characteristic (compare Fig. 4.1) with threshold voltages of $|V_{\mathrm{th},1}| \approx |V_{\mathrm{th},3}| \approx 0.58\,\mathrm{V}$ and $|V_{\mathrm{th},2}| \approx |V_{\mathrm{th},4}| \approx 1.3\,\mathrm{V}$. The series resistor (in this case 940 Ω) is needed for devices with asymmetric I-V characteristic to achieve a stable 'ON' state (see section 4.3.1 for details). Additionally, the series resistor acts as a current-limiting device, which can be used to set a specific R_{LRS} value [36, 37]. The HRS to LRS ratio can be calculated according to Fig. 4.4a.

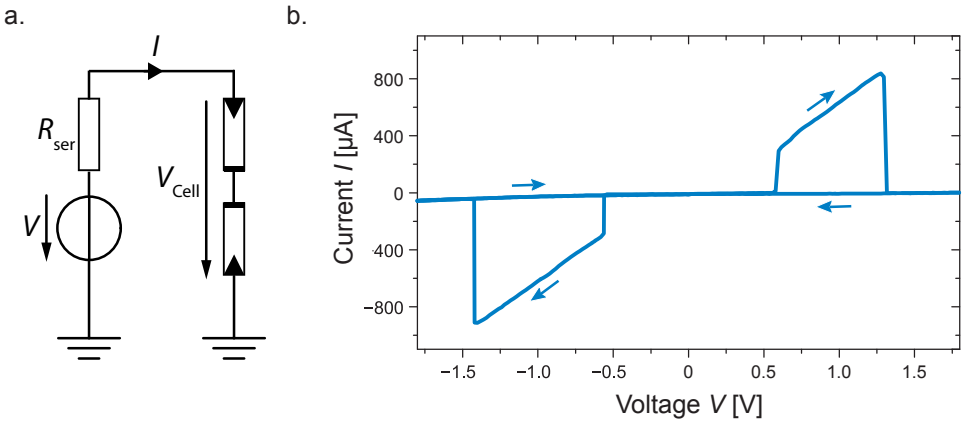


Figure 4.3: (a) Equivalent circuit of the CRS measurement setup. (b) Proof of concept measurement of two connected GeSe-based ECM elements. The characteristic corresponds to Fig. 4.1f. The CRS cell is in state '1' initially, and sweep rate is 20 V/s. Arrows indicate the cycling direction. Adapted from [50].

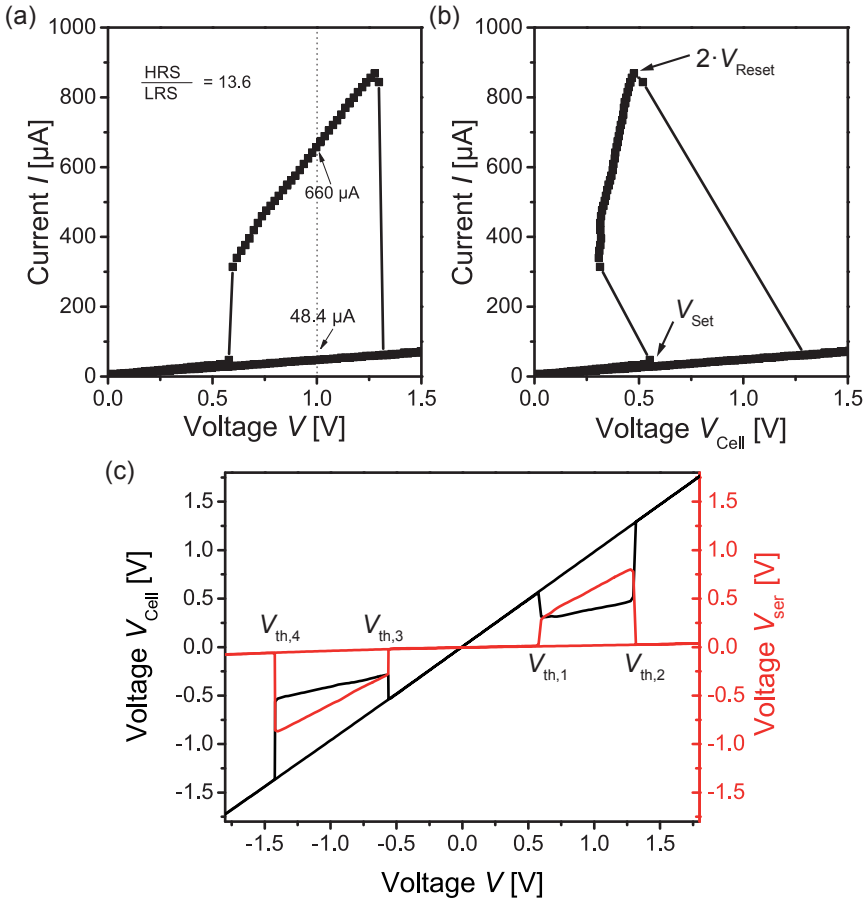


Figure 4.4: (a) Calculation of HRS to LRS ratio resulting from currents at a read voltage of $V = 1\,\mathrm{V}$. (b) When depicting the current as a function of the actual cell voltage V_{Cell}, threshold voltages of individual elements can be derived. (c) In this figure the voltage drop at the cell V_{Cell} (black curve) as well as the voltage drop at the series resistor V_{ser} is presented. Adapted from [50].

When applying a read voltage of $V = 1\,\mathrm{V}$, either 660 μA ('ON' state) or 48.4 μA (state '0') result, which corresponds to a HRS to LRS ratio of 13.6. In Fig. 4.4b the cell voltage V_{Cell} is plotted on the x-axis. The actual cell voltage differs from applied voltage in the 'ON' state due to the series resistor (compare Fig. 4.3a). From this measurement, the actual single element threshold voltages can be calculated: $V_{\mathrm{Set}} \approx 0.58\,\mathrm{V}$, while $V_{\mathrm{Reset}} \approx \frac{0.47\,\mathrm{V}}{2} \approx 0.24\,\mathrm{V}$. In Fig. 4.4c the voltage portioning is visualized. The applied voltage is displayed on the x-axis; the left y-axis depicts the cell voltage V_{Cell} (black curve) while the right y-axis depicts the voltage drop at the series resistor R_{ser} (red curve). A significant voltage drop at the series resistor is only present in the 'ON' state where both CRS elements are in the LRS. If the CRS is in state '0' or '1', almost no voltage drop is present at the series resistor.

On the other hand, the cell voltage V_{Cell} is equal to the applied voltage in all cases, despite the possibility of both elements being in the LRS (compare black curve).

4.2.2 Connected VCM Cells

As CRS behavior is not restricted to ECM-based cells, VCM-based CRS cells can also be connected to CRS cells. In Fig. 4.5 such a Ti / 8 nm STO / Pt - Pt / 8 nm STO / Ti (Pad size $100\mu m$ x $100\mu m$) is shown. The I-V characteristic of these cells (Fig. 4.5a) is quite different compared to ECM-based CRS cells (Fig. 4.3b), which results directly from the single device characteristics (Fig. 2.5). In Fig. 4.5 the CRS cell is in state '1' initially ①. When reaching the first threshold voltages $V_{\mathrm{th},1}$, the CRS switches to the 'ON' state ② and to state '0' when reaching the second threshold voltages $V_{\mathrm{th},2}$ ③. For negative voltages the CRS cell in state '0' ④ switches again to the 'ON' state at $V_{\mathrm{th},3}$ ⑤ and to state '1' at $V_{\mathrm{th},4}$ ⑥. Due to a non-linearity in the HRS branch of VCM cells, the current flow is relatively large if higher voltages are applied. In state '1' or '0' the actual characteristic is determined by the high-resistive element (either A or B). At first glance, the CRS device characteristic is symmetric with respect to the origin for voltages below $V_{\mathrm{th},1}$ or $V_{\mathrm{th},3}$. In fact, this is not the case, as can be seen in the logarithmic I-V plot (Fig. 4.5b). Fig. 4.5b shows that currents depend on the actual CRS state, either state '0' or '1', for voltages below $V_{\mathrm{th},1}$ or $V_{\mathrm{th},3}$. This asymmetry gives rise to a non-destructive readout procedure which is not present in ECM-based CRS cells (see section 5.4.2).

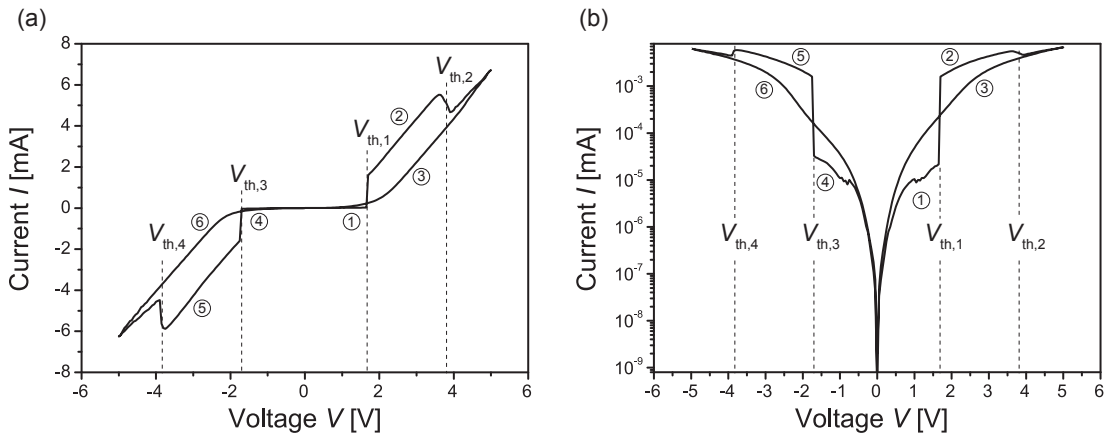


Figure 4.5: Ti/STO/Pt-based connected VCM elements. (a) Linear plot. (b) Semi-logarithmic plot.

4.2.3 Integrated ECM Cells

In principle, all bipolar resistive switches are suited to construct vertically integrated CRS cells. In order to reduce fabrication complexity, Cu/SiO_2/Pt-based ECM elements were used instead of GeSe-based ECM elements for integration [105], which offer CMOS compatibility as well as good memory properties [106, 107]. A large HRS to LRS ratio of about 1530 is present in these cells. Fig. 4.6 shows the *I-V* characteristic (black curve) of the fully vertically integrated CRS cell. For testing reasons, an externally accessible middle electrode was implemented (see section A.1) at which the voltage of the bottom element (sense voltage) was measured. The red curve in Fig. 4.6 depicts this sense voltage, showing that the voltage drops completely at the bottom element at first (state '1'). In the 'ON' state, the voltage drop is lowered to about 50% of the applied voltage, and in state '0' the voltage drop is almost zero. Hence, by having access to the middle electrode, the voltage division property of CRS cells could be verified.

The initial resistance state of ECM elements depends on the fabrication process and can be either LRS or HRS. If the latter applies, a corresponding CRS cell is in the state HRS/HRS ('OFF' state), which is not present in normal CRS operations. As described in section 4.3.1, a positive voltage in the first semi-cycle switches the CRS cell to state '0'. Since no 'ON' state occurs, no significant current increase can be observed (Fig. 4.7a ①). In the second semi-cycle (Fig. 4.7a ②), correct switching to state '1' occurs. Note that the current characteristic is slightly different

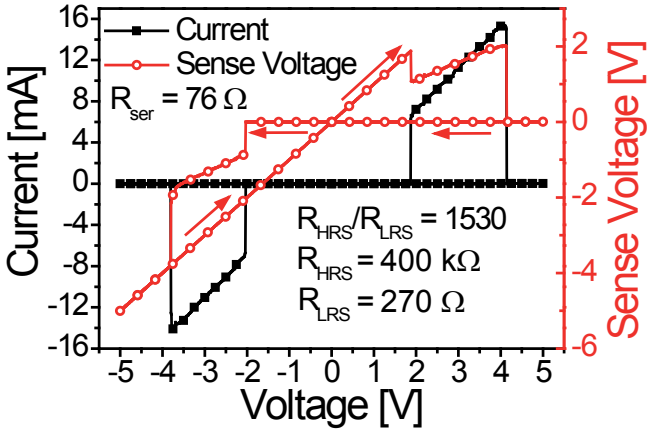


Figure 4.6: *I-V* characteristic (black squares) of an integrated CRS cell (Pt / SiO_2 / Cu / Pt / Cu / SiO_2 / Ti / Pt) and measured sense voltage at the middle electrode (red circles). Area is $3\mu m \cdot 3\mu m$ and a series resistor of 76Ω is used for this measurement. From [105].

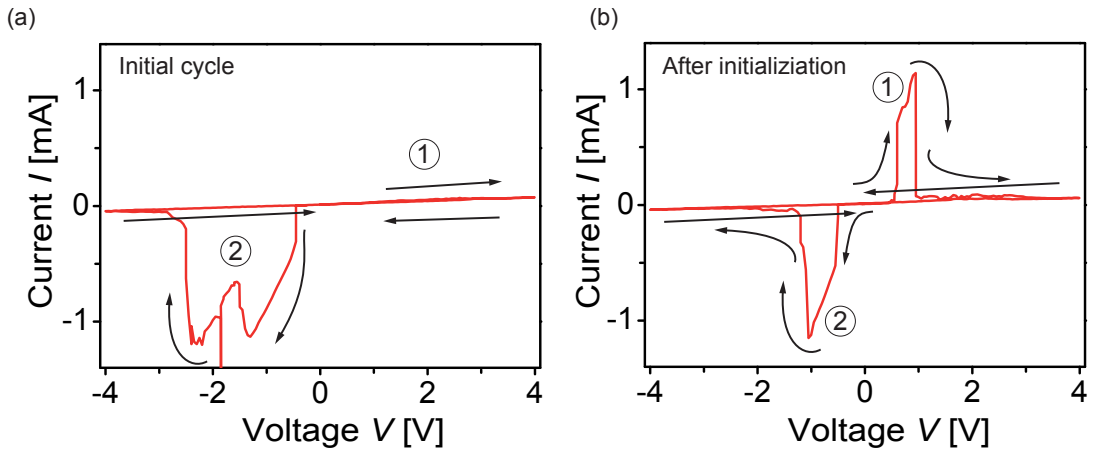


Figure 4.7: (a) First cycle at a virgin Pt/SiO_2/Cu-based CRS cell. (b) A subsequent cycle. Adapted from [41].

compared to normal switching (Fig. 4.7b ②). Since resistive switching elements are often in a high-resistive state initially, a special first switching cycle is needed to switch from HRS/HRS to LRS/HRS or HRS/LRS, respectively.

4.2.4 Integrated VCM Cells

Similar to ECM elements, a parallel layout (compare Fig. A.1) can also be used for VCM-based integrated CRS cells. The bottom electrode here is Ti, while the active layer material is STO (compare section 4.2.2). In [108], several top electrode materials are investigated. It can be shown that integrated CRS cells do not need special forming treatment when using Ir or Pt as top electrode (see Fig. 4.8).

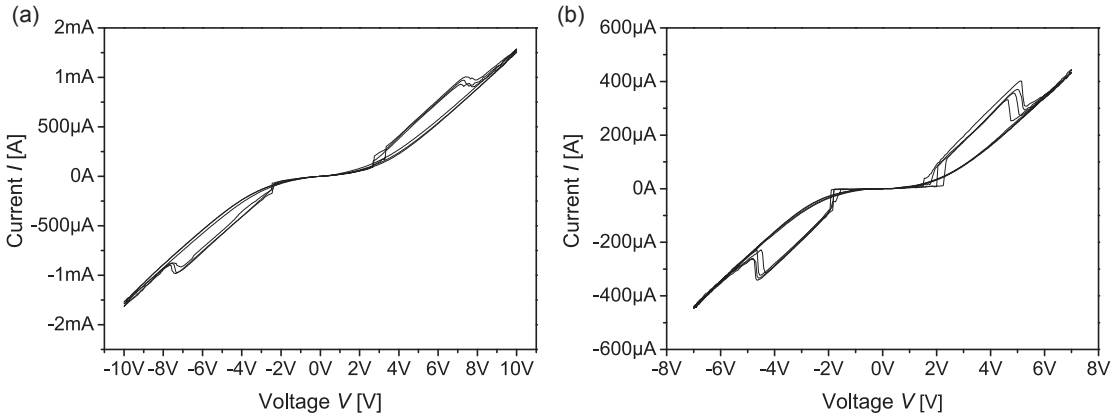


Figure 4.8: (a) Ti/STO/Ir-based CRS cell and (b) Ti/STO/Pt-based CRS cell. Adapted from [108].

Hence, those cells can be used as fabricated with no need for complex forming procedures. In Fig. 4.8a several cycles of a Ti/STO/Ir-based CRS cell are shown, while in Fig. 4.8b several cycles of a Ti/STO/Pt-based CRS cell are depicted. These measurements show that by selecting an appropriate electrode material, integrated STO-based CRS cells are also feasible for VCM materials.

4.3 Analysis of Anti-Serially Connected Circuit Models

In chapter 3 several modeling approaches for bipolar resistive switches were described. Here, these compact models are used for circuit simulation of a network of two anti-serially connected bipolar resistive switches, a complementary resistive switch. This approach is straightforward and can be performed for any basic or dynamic model. Simulation results are then contemplated with regard to the measurement results shown in section 4.2. First, the results for the basic models are presented, and then the dynamic simulation results are considered.

4.3.1 Connected Basic Linear Branch Models

In section 3.1.1 the basic linear branch model was introduced, which is now used for simulation of two anti-serially connected elements. In Fig. 4.9 the equivalent circuit model is depicted. Both elements A and B are defined by the same fixed threshold voltage model, exemplarily shown for element A in Fig. 4.9 (also compare Fig. 3.1). As for single element simulations, a triangular voltage sweep is used for input voltage V_{in}.
Below,the exemplary element from section 3.1.1 with $V_{\mathrm{Reset}} = -0.9\,\mathrm{V}$ and $V_{\mathrm{Set}} =$

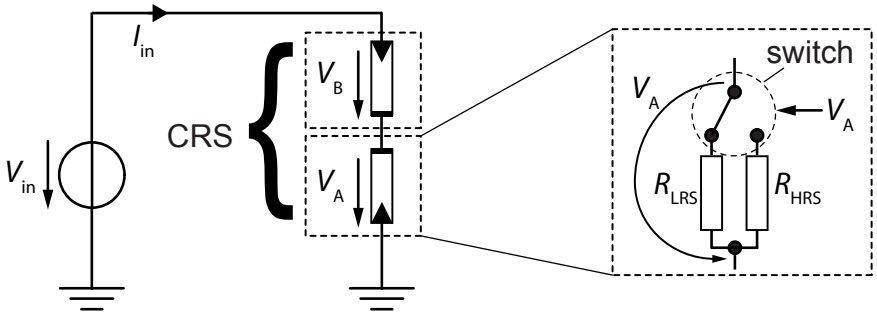


Figure 4.9: The circuit model of a CRS consisting of two elements A and B connected anti-serially.

1.1 V (Fig. 4.10a) is used. For each element A and B, $R_{\mathrm{LRS}} = 1\,\mathrm{k\Omega}$ and $R_{\mathrm{HRS}} = 1\,\mathrm{M\Omega}$ is assumed. In Fig. 4.10b the corresponding I-V characteristic of two anti-serially connected BRS is shown. The first threshold voltage is $V_{\mathrm{th,1}} = |V_{\mathrm{th,3}}| = V_{\mathrm{Set}} = 1.1\,\mathrm{V}$, while the second threshold voltage is $V_{\mathrm{th,2}} = |V_{\mathrm{th,4}}| = 2 \cdot V_{\mathrm{Reset}} = 1.8\,\mathrm{V}$. Starting from state '1', the CRS cell is switched to state 'ON' at $V_{\mathrm{th,1}}$ ① and changes to state '0' at $V_{\mathrm{th,2}}$ ②. At ③ the CRS cell then switches to state 'ON' again and, finally, at ④ back to state '1' (compare chapter 4). In LRS/LRS state (state 'ON') a resistance of $R_{\mathrm{state\_ON}} = 2 \cdot R_{\mathrm{LRS}}$ is present, while in state HRS/LRS (state '1') and LRS/HRS (state '0') $R_{\mathrm{state\_0,1}} \approx R_{\mathrm{HRS}}$ is present. Due to an HRS to LRS ratio of 10^3, the voltage drop at the low-resistive element in state '1' and '0' can be neglected.

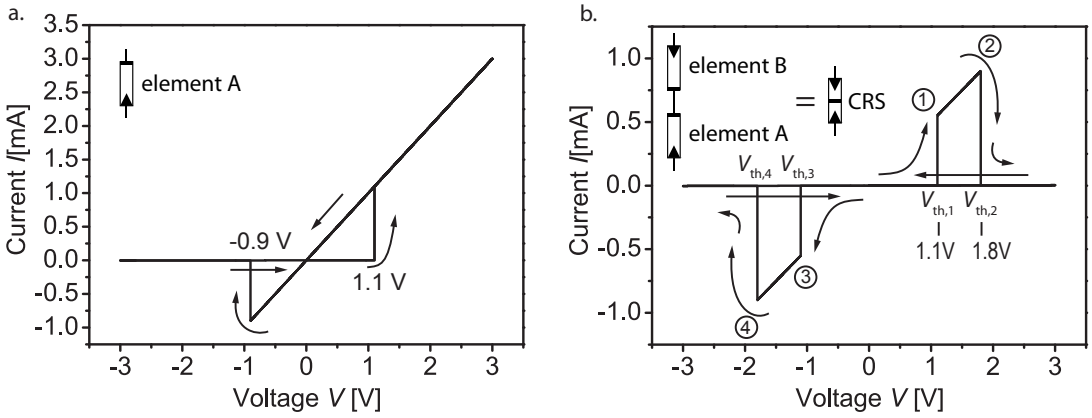


Figure 4.10: (a) Single element I-V characteristic and (b) resulting CRS I-V characteristic using the basic linear branch model for simulation. Adapted from [90].

Asymmetric I-V Characteristics

In Fig. 4.10 the effect of a slight asymmetry on the CRS characteristic is depicted. The asymmetry influences the 'ON' window which is defined as

$$\Delta V_{\mathrm{ON}} = V_{\mathrm{th,2}} - V_{\mathrm{th,1}}, \tag{4.2}$$

while $V_{\mathrm{th,1}}$ and $V_{\mathrm{th,2}}$ are defined as:

$$V_{\mathrm{th,1}} = -\,V_{\mathrm{th,3}} = |V_{\mathrm{Set}}|, \tag{4.3}$$

$$V_{\mathrm{th,2}} = -\,V_{\mathrm{th,4}} = 2 \cdot |V_{\mathrm{Reset}}|. \tag{4.4}$$

During the slight asymmetry in Fig. 4.10 $\Delta V_{\mathrm{ON}} = 0.7\,\mathrm{V}$ is present, while in Fig. 4.11, where a stronger asymmetry is assumed, the 'ON' window is only $\Delta V_{\mathrm{ON}} = 0.1\,\mathrm{V}$. Speaking from experience (see section 2.4.1) and according to the literature [29, 37, 39], ECM elements exhibit even more asymmetric SET and RESET threshold voltages. Thus, exceeding a certain non-symmetry will lead to a non-stable 'ON' state. By using a resistor in series to the CRS with a resistance in the range of the LRS, the threshold voltages $V_{\mathrm{th,2}}$ and $V_{\mathrm{th,4}}$ will be fortunately shifted to larger absolute values. As a result, the I-V characteristic allows for a stable 'ON' state since it becomes symmetric within the tolerable limits. A very asymmetric I-V characteristic with ($|V_{\mathrm{Set}}| \geqslant |V_{\mathrm{Reset}}|$) is shown in Fig. 4.12a. To

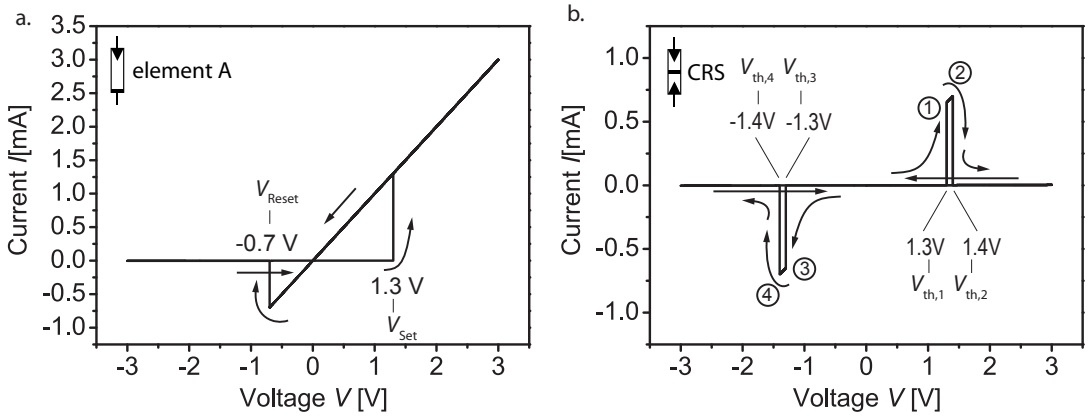


Figure 4.11: Simulations using the basic linear branch model. (a) Element A with asymmetric threshold voltages of $V_{\mathrm{Set}} = 1.3\,\mathrm{V}$ and $V_{\mathrm{Reset}} = -0.7\,\mathrm{V}$. (b) CRS characteristic resulting from two connected elements. The 'ON' window is reduced to $\Delta V_{\mathrm{ON}} = 0.1\,\mathrm{V}$.

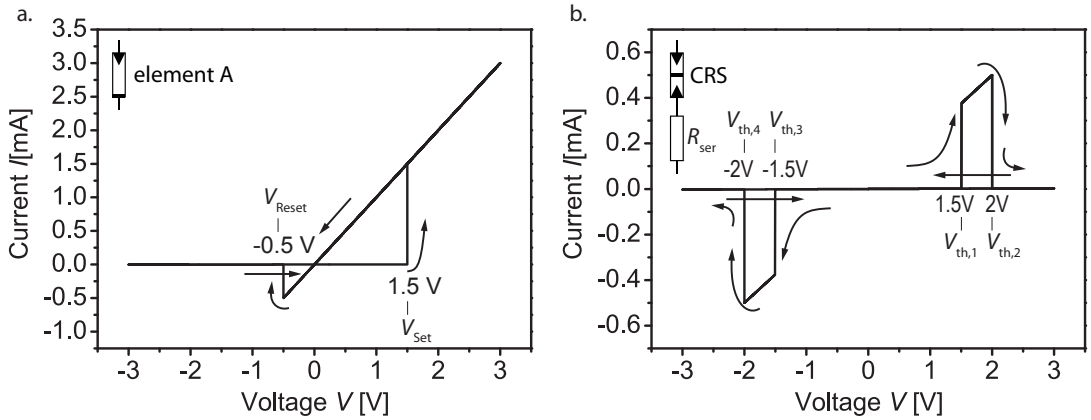


Figure 4.12: Basic linear branch model simulations. (a) Asymmetric I-V characteristic of an element A with $V_{\mathrm{Set}} = 1.5\,\mathrm{V}$ and $V_{\mathrm{Reset}} = -0.5\,\mathrm{V}$. (b) Resulting CRS characteristic for $R_{\mathrm{ser}} = 2R_{\mathrm{LRS}} = 2000\ \Omega$. The 'ON' window is $\Delta V_{\mathrm{ON}} = 0.5\,\mathrm{V}$.

counterbalance this asymmetry and to get an 'ON' window, a series resistor R_{ser} can be applied (Fig. 4.12b). Equations (4.3), (4.4) and (4.2) show that no 'ON' window results for $V_{\mathrm{Set}} = 1.5\mathrm{V}$ and $V_{\mathrm{Reset}} = -0.5\mathrm{V}$:

$$\Delta V_{\mathrm{ON}} = 2 \cdot |V_{\mathrm{Reset}}| - |V_{\mathrm{Set}}| = 1\,\mathrm{V} - 1.5\,\mathrm{V} = -0.5\,\mathrm{V} < 0\,\mathrm{V} \tag{4.5}$$

For the 'ON' state $R_{\mathrm{A}} = R_{\mathrm{B}} = R_{\mathrm{LRS}}$ must hold true, hence the voltage drop during the 'ON' state at the series resistor V_{ser} is:

$$V_{\mathrm{ser,ON}} = \frac{R_{\mathrm{ser}}}{R_{\mathrm{A}} + R_{\mathrm{B}} + R_{\mathrm{ser}}} \cdot V_{\mathrm{in}} = \frac{R_{\mathrm{ser}}}{2R_{\mathrm{LRS}} + R_{\mathrm{ser}}} \cdot V_{\mathrm{in}} \tag{4.6}$$

In state '1' or '0', the voltage drop at R_{ser} can be neglected for $R_{\mathrm{HRS}} >> R_{\mathrm{ser}}$:

$$V_{\mathrm{ser},1/0} = \frac{R_{\mathrm{ser}}}{R_{\mathrm{A}} + R_{\mathrm{B}} + R_{\mathrm{ser}}} \cdot V_{\mathrm{in}} = \frac{R_{\mathrm{ser}}}{R_{\mathrm{LRS}} + R_{\mathrm{HRS}} + R_{\mathrm{ser}}} \cdot V_{\mathrm{in}} \approx 0\,\mathrm{V} \tag{4.7}$$

The first threshold voltage $V_{\mathrm{th},1}$ is therefore not affected by the series resistor:

$$V_{\mathrm{th},1} = |V_{\mathrm{Set}}| \tag{4.8}$$

Only the second threshold voltage $V_{\mathrm{th},2}$ is manipulated by implementing a series resistor. In the 'ON' state, the maximum input voltage V_{in} is defined as the new threshold voltage $V_{\mathrm{th},2^*}$. Taking equations (4.4) and (4.6) into account leads to

$$V_{\mathrm{th},2^*} = 2 \cdot |V_{\mathrm{Reset}}| + V_{\mathrm{ser,ON}} = 2 \cdot |V_{\mathrm{Reset}}| + \frac{R_{\mathrm{ser}}}{2R_{\mathrm{LRS}} + R_{\mathrm{ser}}} \cdot V_{\mathrm{th},2^*} \tag{4.9}$$

$$V_{\mathrm{th},2^*} = \frac{2 \cdot |V_{\mathrm{Reset}}|}{1 - \frac{R_{\mathrm{ser}}}{2R_{\mathrm{LRS}} + R_{\mathrm{ser}}}}. \tag{4.10}$$

Hence, if $R_{\mathrm{HRS}} >> R_{\mathrm{ser}}$ holds true, the 'ON' window $\Delta V_{\mathrm{ON}} = V_{\mathrm{th},2^*} - V_{\mathrm{th},1}$ can be set in a wide range by changing the series resistance:

$$\Delta V_{\mathrm{ON}} = \frac{2 \cdot |V_{\mathrm{Reset}}|}{1 - \frac{R_{\mathrm{ser}}}{2R_{\mathrm{LRS}} + R_{\mathrm{ser}}}} - |V_{\mathrm{Set}}| \tag{4.11}$$

$$R_{\mathrm{ser}} = R_{\mathrm{LRS}} \left(\frac{\Delta V_{\mathrm{ON}} + |V_{\mathrm{Set}}|}{|V_{\mathrm{Reset}}|} - 2 \right). \tag{4.12}$$

If V_{Reset} and V_{Set} are known, a desired ΔV_{ON} is attainable by implementing a series resistance according to equation (4.12). To achieve a $\Delta V_{\mathrm{ON}} = 0.5\,\mathrm{V}$ for the asymmetric device in Fig. 4.12a, a series resistance of $R_{\mathrm{ser}} = 2R_{\mathrm{LRS}}$ must be selected (Fig. 4.12b). Thus, a stable LRS/LRS state can also be established for bipolar

resistive switching materials showing an asymmetric I-V characteristic.
The results presented in this section can be applied to reproduce measurement results shown in section 4.2.1 (see Fig. 4.13). In this case, a series resistance of $R_{\mathrm{ser}} = 940\ \Omega$ was used and a total resistance in the 'ON' state of $R_{\mathrm{total}} = 2 \cdot R_{\mathrm{LRS}} + R_{\mathrm{ser}} = 1515\Omega$ was measured, which corresponds to $R_{\mathrm{LRS}} \approx 290\ \Omega$. With measured values of $V_{\mathrm{th},1} = 0.58\,\mathrm{V}$ and $V_{\mathrm{th},2^*} = 1.3\,\mathrm{V}$, the set and reset voltages of a single element can be calculated. From equation (4.8), $V_{\mathrm{Set}} = 0.58\,\mathrm{V}$ and equation (4.10) follows:

$$V_{\mathrm{Reset}} = 0.5 \cdot V_{\mathrm{th},2^*} \cdot \left(1 - \frac{R_{\mathrm{ser}}}{2R_{\mathrm{LRS}} + R_{\mathrm{ser}}}\right). \tag{4.13}$$

For the given values, $V_{\mathrm{Reset}} \approx 0.25\,\mathrm{V}$ is obtained (compare Fig. 4.4b). By using these values, a simulation of two anti-serially connected elements plus series resistor can reproduce the measured curve in Fig. 4.3. In Fig. 4.13 the measured I-V characteristic as well as the simulated I-V characteristic are depicted.

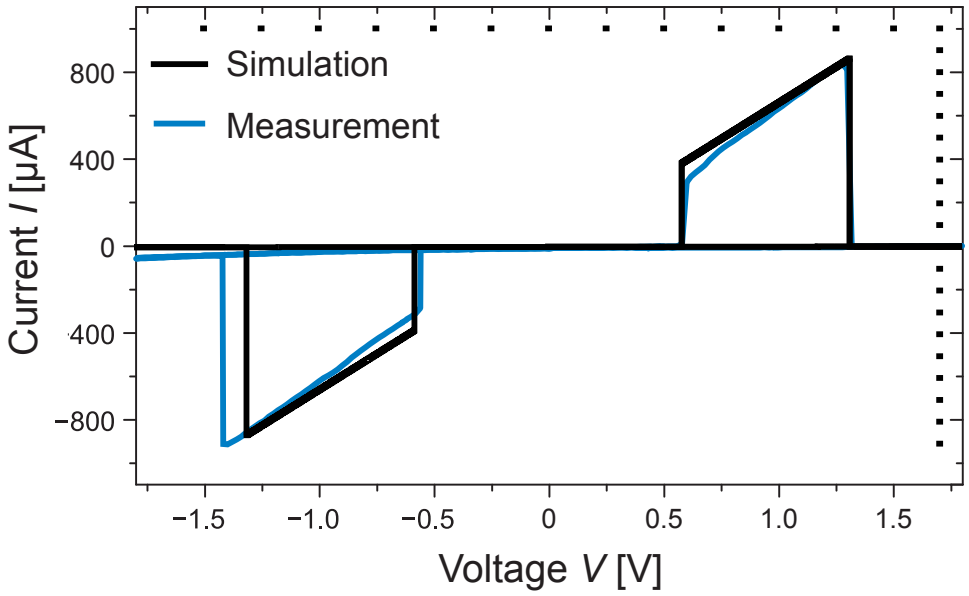


Figure 4.13: Measurement and corresponding simulated I-V characteristic for a GeSe-based ECM CRS cell (compare section 4.2.1). The basic linear branch model is used for this simulation.

Initial Behavior

For virgin CRS cells, all four CRS states are possible initial states, depending on the fabrication process. For any state '0', '1' or 'ON' the cell can be set to state '0' with

a positive write voltage, and to state '1' with a negative write voltage. But, if the CRS cell is in the 'OFF' state (HRS/HRS) initially, a special first switching cycle is needed to switch the CRS cell to '0' or '1'. To illustrate this issue, a simulation of a virgin cell starting from HRS/HRS was conducted (see Fig 4.14). Fig. 4.14a shows the same CRS cell considered in Fig. 4.11a,b ($V_{\mathrm{Set}} = 1.1\mathrm{V}$ and $V_{\mathrm{Reset}} = -0.9V$), but being in state 'OFF' instead of '1', initially. $R_{\mathrm{HRS}} = 1\,\mathrm{M\Omega}$ and $R_{\mathrm{LRS}} = 1\,\mathrm{k\Omega}$ are assumed for this simulation. To switch the cell to state '0' in the first semi-cycle, a voltage of

$$V_{\mathrm{th,init}} = 2 \cdot |V_{\mathrm{Set}}| \tag{4.14}$$

must be applied, which in this case is $V_{\mathrm{th,init}} = 2.2\,\mathrm{V}$. To make this clear, a cutout (I.) from Fig. 4.14a is drawn to a larger scale in Fig. 4.14b. The resistance changes from $R_{\mathrm{CRS,init}} = 2R_{\mathrm{HRS}}$ to $R_{\mathrm{CRS,0}} = R_{\mathrm{HRS}} + R_{\mathrm{LRS}} \approx R_{\mathrm{HRS}}$ at a voltage of $V = 2.2\,\mathrm{V}$. After this initial switching to state '0', the CRS cell behaves in the conventional way in the second and following cycles.

Experimental data on such an initialization process was presented in Fig. 4.7a for an integrated Pt/SiO_2/Cu-based CRS cell. Like the simulation predicted, no switching to state 'ON' was observed in the positive semi-cycle, thus only a switching from 'OFF' to '0' occurred. In the negative semi-cycle a switching to state 'ON' is present, verifying a prior state '0'.

The initialization process can also be understood by considering a dynamic CRS model (see section 4.3.6).

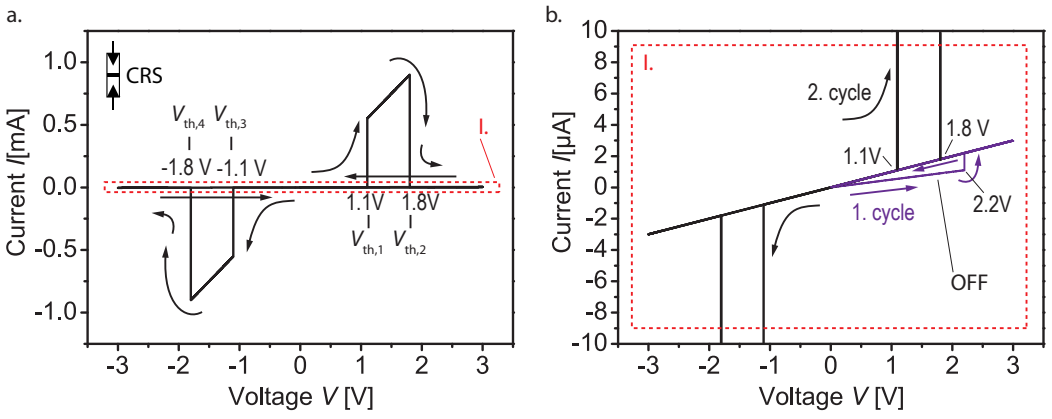


Figure 4.14: Initialization simulations using the basic linear branch model. (a) Initially, the CRS cell is in state HRS/HRS, hence no switching to LRS/LRS occurs at the first positive slope. (b) Cutout (I.) from (a). In the first semi-cycle the cell switches from HRS/HRS ('OFF') to state LRS/HRS ('0').

4.3.2 Connected Basic Non-Ohmic Branch Models

In section 3.1.3, a basic BRS model offering non-ohmic branches was suggested for modeling (compare Fig. 4.15a). For assumed parameters, an anti-serially connected element simulation can be conducted, leading to a CRS I-V characteristic (Fig. 4.15b). Due to the non-ohmic characteristic of the HRS branch, the initial switching from HRS/HRS to LRS/HRS in the first cycle is visible in Fig. 4.15b (compare Fig. 4.14a).
In the next step, parameters are adjusted the fit to measurements of VCM-based CRS cells (compare section 4.2.2 and Fig. 4.16). The following equations define the LRS (I.) and HRS (II.) branch:

$$I_{\mathrm{I.}} = C_{1\mathrm{I.}} \cdot \sinh(V \cdot C_{2\mathrm{I.}}) \tag{4.15}$$

$$I_{\mathrm{II.}} = C_{1\mathrm{II.}} \cdot \sinh(V \cdot C_{2\mathrm{II.}}) \tag{4.16}$$

The parameters to model the non-ohmic behavior in LRS are $C_{1\mathrm{I.}} = 4 \cdot 10^{-3}\,\mathrm{A}$, $C_{2\mathrm{I.}} = 0.8\,\mathrm{V}^{-1}$ and the parameters to model non-ohmic behavior in HRS are assumed as $C_{1\mathrm{II.}} = 10^{-5}\,\mathrm{A}$, $C_{2\mathrm{I.}} = 2.5\,\mathrm{V}^{-1}$. The fixed threshold voltages for each element are selected as $V_{\mathrm{th,Set}} = 1.6\,\mathrm{V}$ and $V_{\mathrm{th,Reset}} = 1.9\,\mathrm{V}$. The resulting I-V characteristic is depicted in Fig. 4.16, showing that the measured characteristic can indeed be approximated from such a two element simulation. Note that fixed threshold voltages were assumed for this simulation, which is not the case for the simple dynamic non-linear model (see section 4.3.4).

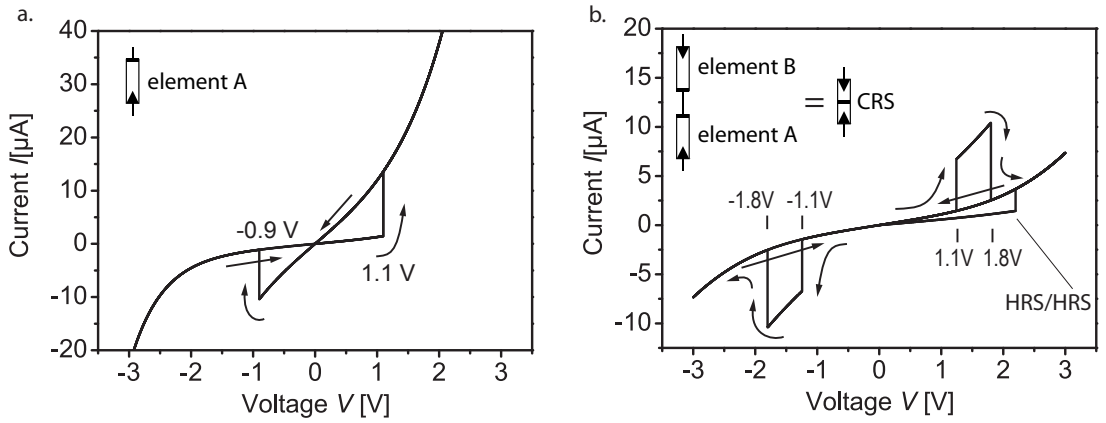


Figure 4.15: Basic non-ohmic branch model simulations. (a) SPICE simulation of a single element. (b) Resulting CRS cell simulation. Due to non-linearity in the HRS-branch, the initial HRS/HRS to LRS/HRS switching is visible in the first cycle.

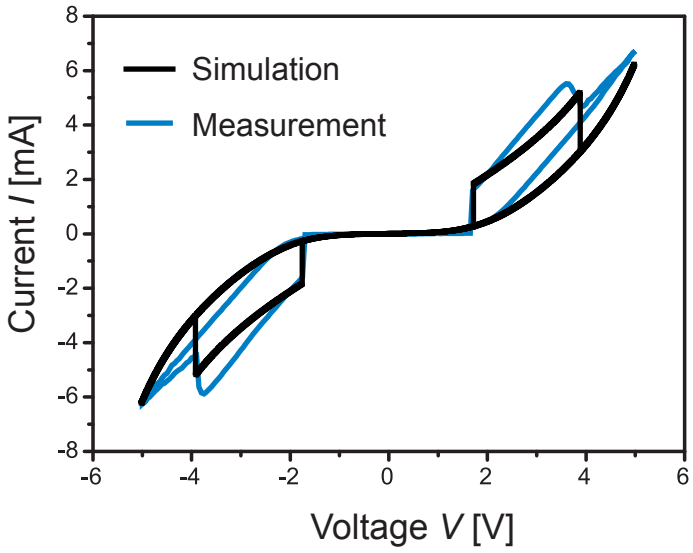


Figure 4.16: Measurement and corresponding simulated I-V characteristic for an STO-based VCM CRS cell (compare section 4.2.2). The basic non-ohmic branch model is used for this simulation.

4.3.3 Connected Simple Dynamic Linear Models

In section 3.2.2, the simple dynamic linear model, which is a memristive system (compare section 3.2.1), was introduced. In this section, that model (compare Fig. 4.17a) is used for simulation of two elements A and B which are connected anti-serially. As we will see, the model is not suitable to reproduce CRS behavior, thus its application for dynamic simulations is limited.
Remember the dynamical system representing one element which was defined by equations (3.30) and (3.31). Two of those elements, A and B, are connected anti-serially in the following. The equations for element A read

$$V_\mathrm{A} = (R_\mathrm{LRS} - R_\mathrm{HRS}) \cdot \frac{w_\mathrm{A}}{d} + R_\mathrm{HRS} \cdot I_\mathrm{A} \tag{4.17}$$

$$\dot{w}_\mathrm{A} = C_1 \cdot I_\mathrm{A} \cdot (\sigma((d - w_\mathrm{A}) \cdot I_\mathrm{A}) + \sigma(-w_\mathrm{A} \cdot I_\mathrm{A})) \tag{4.18}$$

and for element B

$$V_\mathrm{B} = (R_\mathrm{LRS} - R_\mathrm{HRS}) \cdot \frac{w_\mathrm{B}}{d} + R_\mathrm{HRS} \cdot I_\mathrm{B} \tag{4.19}$$

$$\dot{w}_\mathrm{B} = C_1 \cdot I_\mathrm{B} \cdot (\sigma((d - w_\mathrm{B}) \cdot I_\mathrm{B}) + \sigma(-w_\mathrm{B} \cdot I_\mathrm{B})). \tag{4.20}$$

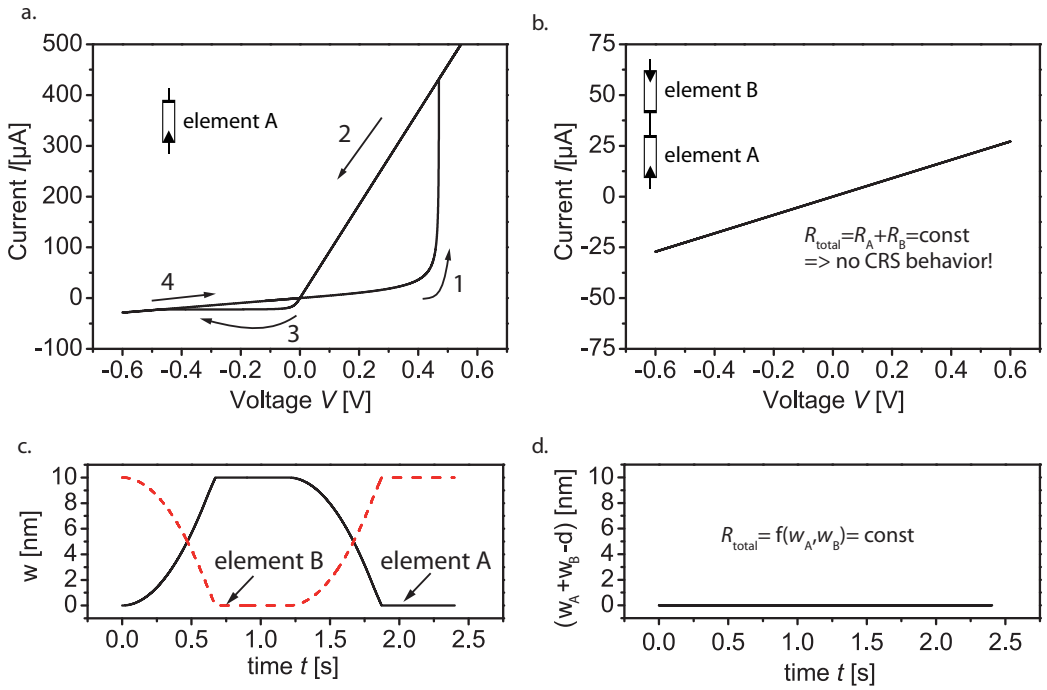


Figure 4.17: Simulations using the simple dynamic linear model. (a) I-V characteristic of element A. (b) I-V characteristic of corresponding anti-serial connection where no CRS behavior is present. (c) State variable w_A and w_B as function of time t. (d) w_A and w_B even up, hence $w_\mathrm{A} + w_\mathrm{B} - d$ is constant. Adapted from [90].

Note that $I_\mathrm{A} = -I_\mathrm{B}$ holds true for equations (4.19) and (4.20) because of the serial connection. To start simulation in state '1' (HRS/LRS), the following initial values,

$$w_\mathrm{A}(t = 0) = 0 \tag{4.21}$$

and

$$w_\mathrm{B}(t = 0) = d, \tag{4.22}$$

are selected. From experiments (Fig. 4.3) and basic simulations (Fig. 4.10) we expect a resulting CRS I-V characteristic. Instead, a straight line corresponding to a linear resistance rather than a CRS behavior (Fig. 4.17b) is observed. This is a direct consequence of the linear dependency of R on the state variable w and the fact that $\dot{w}$ is an odd function of the input current I, as will be shown below.
The total resistance of two anti-serially connected elements A and B reads

$$R_\mathrm{total} = R(w_\mathrm{A}) + R(w_\mathrm{B}). \tag{4.23}$$

For the given equations (compare equation (3.30) and (3.31)),

$$R(w) = (R_{\mathrm{LRS}} - R_{\mathrm{HRS}}) \cdot \frac{w}{d} + R_{\mathrm{HRS}} \tag{4.24}$$

$$\dot{w} = C_1 \cdot I, \tag{4.25}$$

the total resistance R_{total} can be derived. By integrating of equation (4.25) and using the initial conditions (4.21) and (4.22), the following applies:

$$w_{\mathrm{A}} = C_1 \cdot \int I_{\mathrm{A}} \mathrm{d}t \tag{4.26}$$

$$w_{\mathrm{B}} = d - C_1 \cdot \int I_{\mathrm{A}} \mathrm{d}t \tag{4.27}$$

$$w_{\mathrm{A}} + w_{\mathrm{B}} - d = 0. \tag{4.28}$$

Since w_{A} and w_{B} even up (Fig. 4.17c,d), a constant total resistance R_{total} (equation (4.23)) results from equation (4.24) and (4.25):

$$R_{\mathrm{total}} = (R_{\mathrm{LRS}} - R_{\mathrm{HRS}}) + 2 \cdot R_{\mathrm{HRS}} = R_{\mathrm{LRS}} - R_{\mathrm{HRS}} = \mathrm{const.} \tag{4.29}$$

Given that the total resistance is constant, no CRS behavior can result from such a linear memristive model.

We can systematically understand this fact by having a closer look at the dynamical system, which can be transformed into a second order linear system. The equations modeling a single element (equation (4.24) and (4.25)) can be reformulated with two state variables w_1 and w_2, specified as $w_1 = d - w_2 = w$:

$$\dot{w_1} = C_1 \cdot I \tag{4.30}$$

$$\dot{w_2} = C_1 \cdot I \tag{4.31}$$

$$R(w_1, w_2) \cdot I = R_{\mathrm{LRS}} \cdot \frac{w_1}{d} + R_{\mathrm{HRS}} \cdot \frac{w_2}{d}. \tag{4.32}$$

Because changes of w_1 and w_2 in both elements A and B are always identical in an anti-serial configuration due to a direct dependency on I and the linear dependency of R_{A} and R_{B} on w_1 and w_2, respectively, no CRS behavior can result from this linear model.

Therefore, this linear model is too simple to render correct bipolar resistive switch behavior as well, and more realistic models (see section 4.3.5 and 4.3.6) are needed to obtain more accurate simulation results [90].

4.3.4 Connected Simple Dynamic Non-Linear Models

In this section, the simple dynamic non-linear model is used for anti-serially connected element simulations. Fig. 4.18a,c recaps the single element simulation result from section 3.2.3, and Fig. 4.18b shows the corresponding CRS I-V curve. In contrast to the simple dynamic linear model simulations in section 4.3.3, a CRS-like characteristic is present. Although I-V characteristics do not apply perfectly - the switching to LRS/LRS state is smooth while in measurements a direct switching to LRS/LRS is observed (compare Fig. 4.5) - a CRS-like behavior is present in an anti-serially connected element simulation. This is due to the added sinus hyperbolic dependency of current I_A on voltage V_A,

$$I_\mathrm{A} = C_1 \cdot \sinh\left(V_\mathrm{A} \cdot C_2\right) \cdot \left(\frac{w_\mathrm{A}}{d} \cdot C_{3,\mathrm{a}} + \left(1 - \frac{w_\mathrm{A}}{d}\right) \cdot C_{3,\mathrm{b}}\right) \tag{4.33}$$

$$\dot{w}_\mathrm{A} = C_4 \cdot I_\mathrm{A} \cdot \left(\sigma\left(\left(d - w_\mathrm{A}\right) \cdot I_\mathrm{A}\right) + \sigma\left(-w_\mathrm{A} \cdot I_\mathrm{A}\right)\right), \tag{4.34}$$

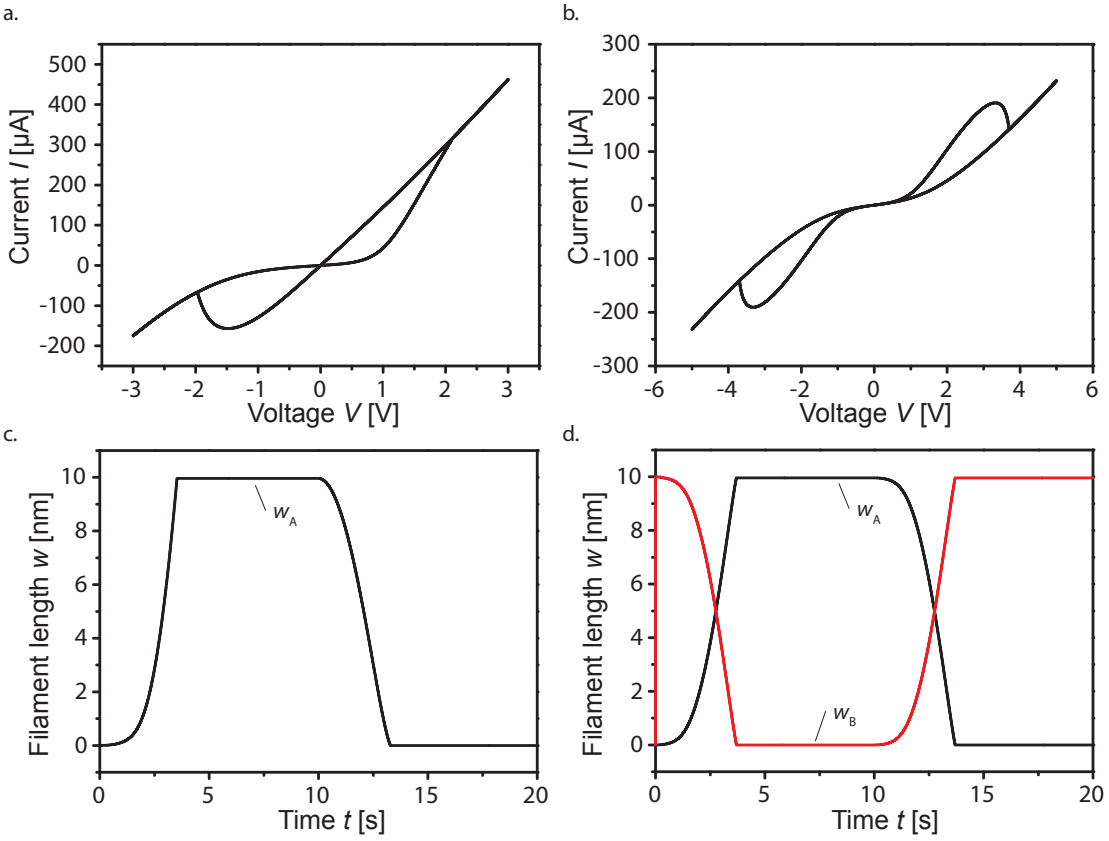


Figure 4.18: Simulations using the simple dynamic non-linear model. (a) I-V characteristic of a single element (compare section 3.2.3), and (b) corresponding I-V characteristic of a CRS cell. (c) State variable versus time for single element simulation. (d) State variables versus time for anti-serially connected element simulation.

leading to a non-linear dependency of the element resistance on the state variable w, although the two state variables vary uniformly (see Fig. 4.18d).
Because of a lack of physical motivation, this model and corresponding simulation results will differ from real device behavior. Note, that at least one additional state variable, the temperature, is required for correct modeling of VCM [101].

4.3.5 Connected Dynamic ECM Models

A physical-based dynamical model was described in section 3.2.4 for modeling of ECM elements. A typical I-V characteristic is depicted in Fig. 4.19a.
Although no tunneling equation is used in this model, the CRS principle can be studied with its help (Fig. 4.19b); by contrast, this is not possible with the simple dynamic model, as derived in section 4.3.3.
For the simulation shown in Fig. 4.19b, a series resistor $R_{\mathrm{ser}} = 2500\ \Omega$ for each element was applied. This I-V characteristic resembles the characteristic shown in Fig. 4.3 qualitatively. But, since Cu/SiO_2 instead of Cu/GeSe is assumed in

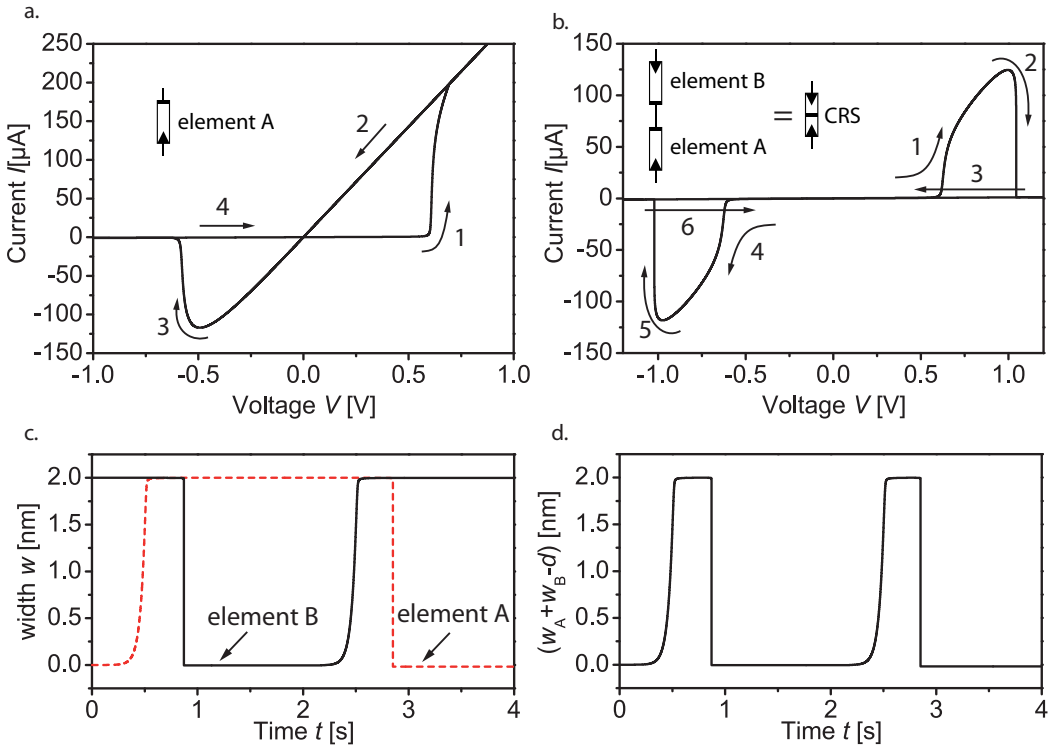


Figure 4.19: Dynamic ECM model simulations. (a) I-V characteristic of a single element with $R_{\mathrm{ser}} = 2500\ \Omega$. (b) I-V characteristic of the corresponding CRS with $R_{\mathrm{ser}} = 5000\ \Omega$. (c) State variables w_{A} and w_{B} as functions of time t. (d) $w_{\mathrm{A}} + w_{\mathrm{B}} - d$ as function of time. Adapted from [90].

simulation, results cannot be transfered to measurement directly. Additionally, several parameters used in simulation, for instance, the filament radius r or the exchange current density j_0 (compare equation 3.47), are not known at all.
The characteristics of the inner state variables w_A and w_B, which correspond to the filament length in each element, are shown in Fig. 4.19c. In contrast to the linear model (compare Fig. 4.17c), the state variables of element A and B do not even up for this non-linear model (Fig. 4.19d).
The different dynamics can be understood by having a closer look at the voltage divider which applies for the CRS. First, almost all voltage drops at element A, which is in HRS. Since state change is a non-linear function of V_A, the filament growth velocity increases with applied voltage V_{in}. When the filament reaches the counter electrode ($w_A = d$), element A switches to LRS. Now, both elements A and B are in LRS, suffering an equal voltage drop, which may be additionally reduced by a series resistor. This voltage drop is too low to result in a decrease of the filament of element B. With further increase of applied voltage V_{in}, the voltage V_B becomes large enough to induce a fast decrease of filament, thus switching element B to HRS.
The influence of a series resistor on the I-V characteristics of single elements as well as CRS cells is shown in Fig. 4.20. For small R_{ser} the very asymmetric I-V characteristic of an ECM element (Fig. 4.20a) only results in a current spike in the CRS configuration (Fig. 4.20b). For larger R_{ser} a stable LRS/LRS state can be obtained for CRS cells built up of asymmetric ECM elements.

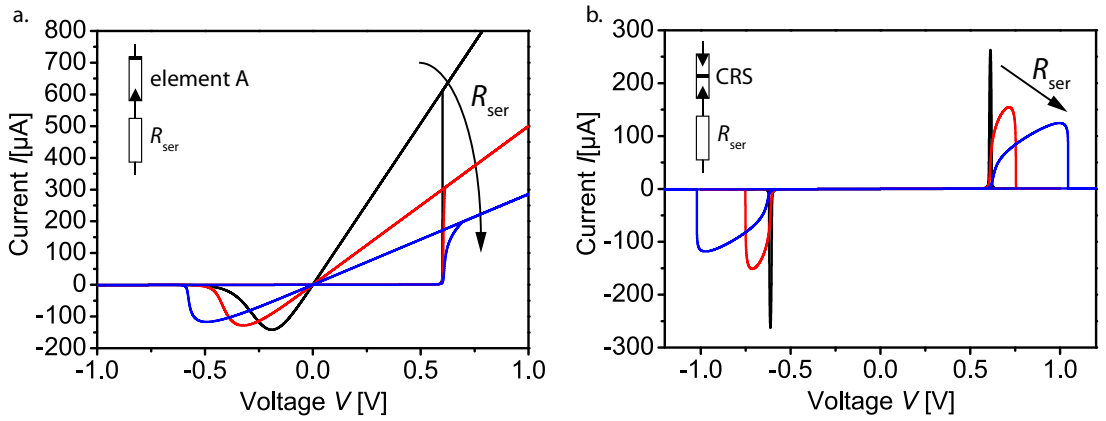


Figure 4.20: Variation of series resistance using the dynamic ECM model. (a) I-V characteristic of a single element for $R_{ser} = 0\ \Omega$, $R_{ser} = 1000\ \Omega$ and $R_{ser} = 2500\ \Omega$. (b) I-V characteristic of corresponding CRS cells with $R_{ser} = 0\ \Omega$, $R_{ser} = 2000\ \Omega$ and $R_{ser} = 5000\ \Omega$. Adapted from [90].

In conclusion this model is capable of modeling anti-serially connected elements, including the influence of a series resistor. With the refined dynamic model in the next paragraph, more advanced CRS properties can be studied, too.

4.3.6 Connected Refined Dynamic ECM Models

In the refined dynamic ECM model a tunneling equation was added to model the electronic current (compare section 3.2.5). This refined model is used for CRS simulations below. To allow a comparison to the single element simulation, corresponding results are depicted in Fig. 4.21a and Fig. 4.21c. In Fig. 4.21b a typical CRS curve with $R_{\mathrm{ser}} = 25\,\mathrm{k\Omega}$ for 0.01 V/s, 0.1 V/s and 1 V/s is depicted. For CRS, there is an inherent self limitation, which is a result of the initial value of the gap width at element B $g_{\mathrm{B,init}} = 0.2\,\mathrm{nm}$ (Fig. 4.21d).

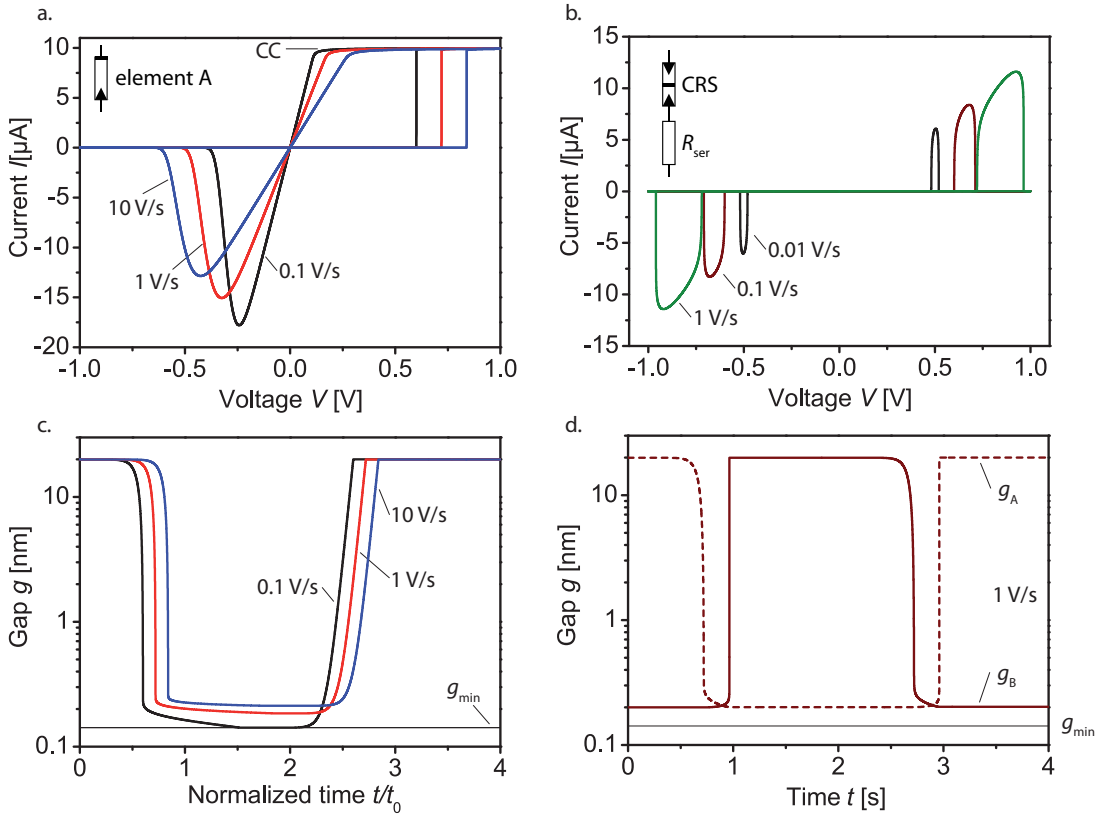


Figure 4.21: Simulation of different voltage ramps using the refined dynamic ECM model. (a) Single element simulation with $I_{\mathrm{CC}} = 10\mu\mathrm{A}$. Simulation is conducted for voltage ramps of 0.1 V/s, 1 V/s and 10 V/s. (b) CRS simulation with $R_{\mathrm{ser}} = 25\,\mathrm{k\Omega}$ and ramps of 0.01 V/s, 0.1 V/s and 1 V/s. (c) Gap size g versus normalized time t/t_0. Values for t_0 are $t_0 = 10\,\mathrm{s}$, $t_0 = 1\,\mathrm{s}$ and $t_0 = 0.1\,\mathrm{s}$. (d) CRS simulation of g_{A} and g_{B} for 1 V/s.

For series resistances $R_{\mathrm{ser}} = 2500\ \Omega$ (black curve), $R_{\mathrm{ser}} = 7500\ \Omega$ (red curve) and $R_{\mathrm{ser}} = 12500\ \Omega$ (blue curve), the I-V characteristics are depicted in Fig. 4.22a. Due to a voltage drop at R_{ser}, the reset voltage is shifted to higher values for larger series resistances. In Fig. 4.22b the influence of a series resistance $R_{\mathrm{ser}} = 5000\ \Omega$ (black curve), $R_{\mathrm{ser}} = 15000\ \Omega$ (red curve) and $R_{\mathrm{ser}} = 25000\ \Omega$ (blue curve) on an initialized CRS ($g_{\mathrm{B,init}} = 0.2\,\mathrm{nm}$) cell is shown. An increase in series resistances leads to a larger 'ON' state region (compare Fig. 4.20).

In simulations shown above, initialized CRS cells were used. In the next step the initialization of a CRS cell from an arbitrary initial state to a specific LRS/HRS is described. In this simulation, $g_{\mathrm{A,init}} = 2\,\mathrm{nm}$ and $g_{\mathrm{B,init}} = 1\,\mathrm{nm}$ are selected for a device with an active layer thickness of $d = 2\,\mathrm{nm}$, and a voltage sweep up to $2\,\mathrm{V}$ is applied in the first cycle (Fig. 4.23a). After initialization, voltage sweeps up to $\pm 1\,\mathrm{V}$ are applied. The resulting current is depicted in Fig. 4.23b and the corresponding I-V characteristic is shown in Fig. 4.23c. The initial voltage controls the remaining gap size $g > g_{\mathrm{min}}$, or, more precisely, the ionic current; thus, a current compliance could be used for control. In Fig. 4.23d, $g = 0.3\,\mathrm{nm}$ results from this initialization, and due to the time- and voltage-dependent self-limiting property of element A and B, this gap size is present in all LRS states occurring after the initialization process. For applied voltages larger than $V_{\mathrm{in}} = 2\,\mathrm{V}$, the contact case could be selected as LRS state, too.

In Fig. 3.14, a high switching speed ($< 1\,\mathrm{ns}$) for a pulse simulation could be shown for single ECM elements. For anti-serially connected elements, a similar pulse

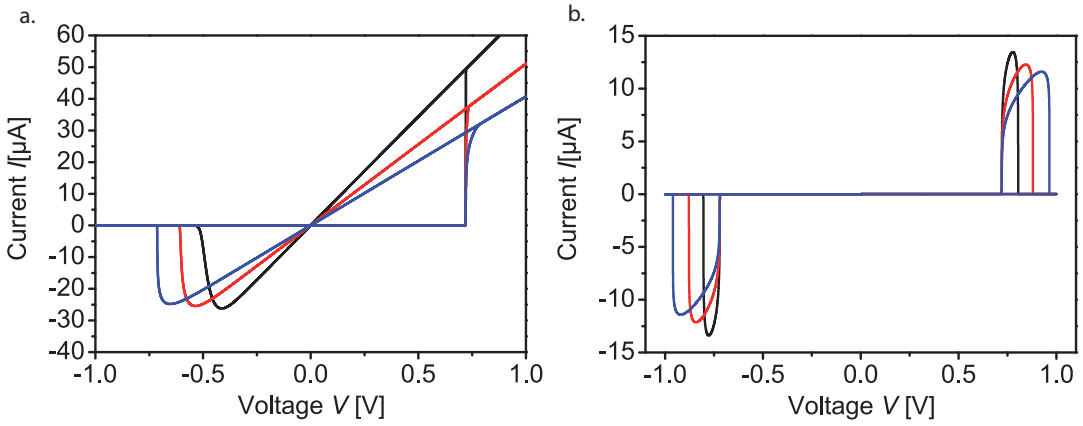


Figure 4.22: (a) Simulation of series resistor variation for the refined dynamic ECM model. $R_{\mathrm{ser}} = 2500\ \Omega$ (black curve), $R_{\mathrm{ser}} = 7500\ \Omega$ (red curve) and $R_{\mathrm{ser}} = 12500\ \Omega$ (blue curve). (b) The corresponding anti-serially connected element simulations. $R_{\mathrm{ser}} = 5000\ \Omega$ (black curve), $R_{\mathrm{ser}} = 15000\ \Omega$ (red curve) and $R_{\mathrm{ser}} = 25000\ \Omega$ (blue curve).

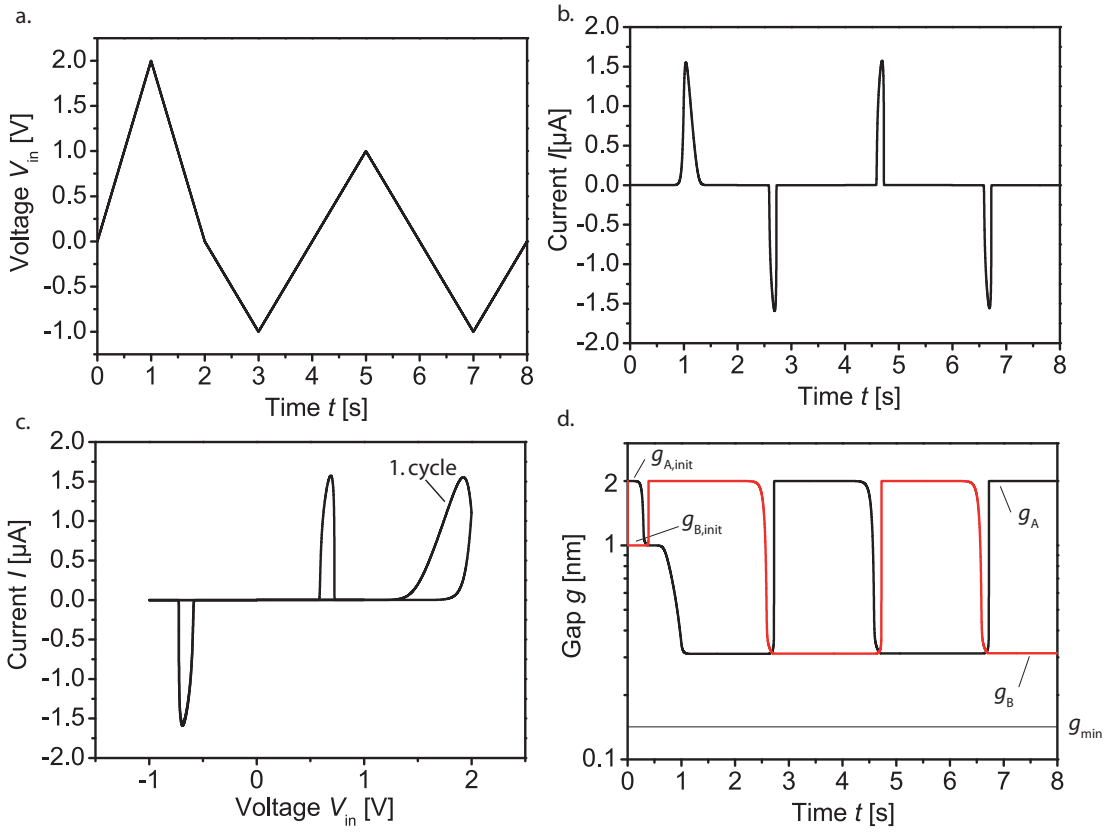


Figure 4.23: Initialization of a CRS using the refined dynamic ECM model for simulation. (a) Applied voltage V_{in}. (b) Current versus time. (c) CRS I-V characteristic. (d) Gap sizes of elements A and B versus time.

simulation can be performed as well. In Fig. 4.24a, fast switching to LRS/LRS is considered first. A voltage V_{in} with a pulse width of 1 ns and an amplitude of 2 V is applied. In Fig. 4.24a the voltage V_{A} at element A (HRS) and V_{B} at element B (LRS) are also depicted, showing a switching to LRS/LRS after about 250 ps, which is very fast. In Fig. 4.24b the corresponding gap sizes are shown. A strong change in gap size is present for element A (g_{A}), which corresponds to a switching from HRS to LRS, while the gap size of element B (g_{B}) is not affected by this pulse.
To realize a fast switching from A:HRS/B:LRS to A:LRS/B:HRS, a larger voltage amplitude is needed. Such a simulation, with $V_{\mathrm{in}} = 3\,\mathrm{V}$ and a pulse width of 1 ns, can be seen in Fig. 4.24c. The switching takes place very fast ($< 1\,\mathrm{ns}$) and no stable LRS/LRS state is reached. In Fig. 4.24d the change in gap size for both elements A and B is depicted, showing an almost simultaneous switching of both elements. Note that fast switching (about 120 ns) was achieved according to recent measurements [105].

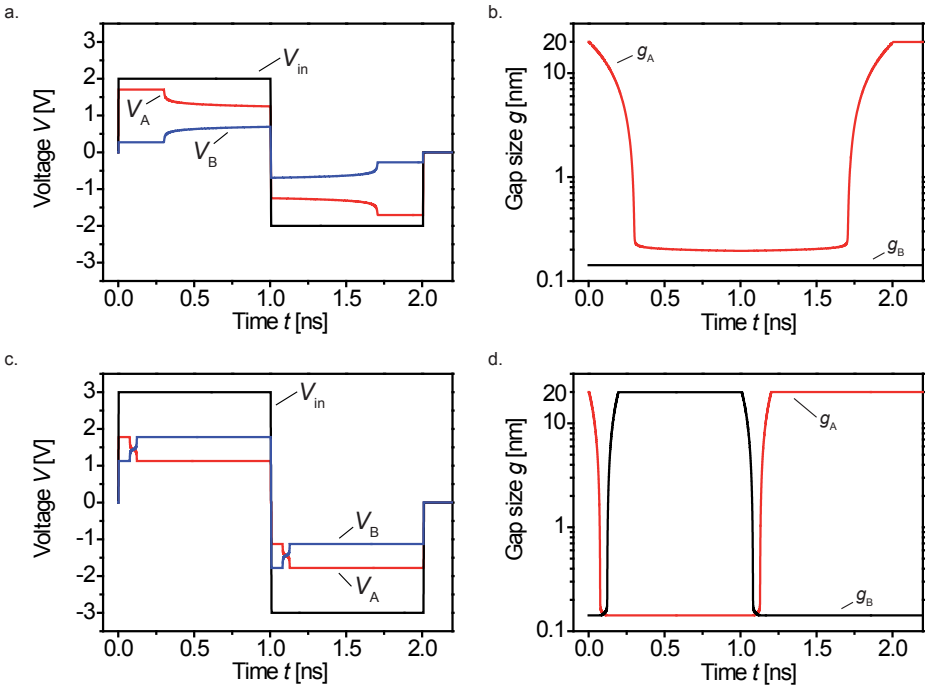


Figure 4.24: CRS fast pulse simulations using the refined dynamic ECM model. (a) 1 ns pulse with amplitude of $V_{\mathrm{in}} = 2\,\mathrm{V}$ leading to a switching to LRS/LRS. (b) The corresponding gap sizes g_{A} and g_{B}. (c) Using a 1 ns pulse with amplitude of $V_{\mathrm{in}} = 3\,\mathrm{V}$, a fast switching of both elements occurs. (d) Corresponding gap sizes of elements A and B versus time. The thickness of the active layer is $d = 20\,\mathrm{nm}$.

4.4 Conclusion

In this chapter, the concept of complementary resistive switches has been presented. Complementary resistive switches can be made out of any bipolar resistive switches by combining two elements in an anti-serial fashion. The basic concept was made clear by means of the sweep properties of CRS cells made up of symmetric BRS elements.

It was shown that CRS cells offer an overall high-resistive state in states '0' and '1'. As we will see in chapter 5, this property paves the way to large passive crossbar array memories by solving the sneak path problem.

Measurements verifying the proposed CRS behavior were conducted for simply connected BRS elements as well as for integrated CRS cells. The CRS behavior was shown for two different classes of resistive switches, ECM and VCM type switches. In the next step, simulation results were reviewed with respect to these measurement results.

The basic idea of CRS simulation is to combine two BRS element models anti-

serially. The basic non-ohmic branch model is suited to reproduce VCM-based CRS I-V characteristics. Similarly, with the basic linear branch model, the measured characteristics of an ECM-based CRS cell can be reproduced. The influence of a series resistor on the 'ON' window as well as the initialization of virgin CRS cells can be understood using this model. An equation which allows the dimensioning of series resistors in order to equilibrate asymmetries of BRS elements, making a stable LRS/LRS state feasible for any BRS elements, was derived.
Alternatively, sophisticated dynamic models can be used for CRS simulations. It is important to note that the simple linear dynamic model is not suited for CRS modeling, since neither a parallel current path nor a non-linear dependency of R on the state variable w is present in this model.
To achieve correct CRS simulation results, a non-linear dynamic model is needed. By introducing a non-linear dependency of R on the state variable w, the simple dynamic non-linear model is capable of reproducing a CRS-like characteristic similar to VCM-based CRS cells. The simulations illustrate the need for a non-linearity, but the significance of the results is limited because there is no underlying physical model.
The dynamic ECM model and the refined dynamic ECM model are two physics-based models which can be used for CRS modeling for arbitrary input signal frequencies. Quasi-static as well as fast pulse simulations were performed and the influence of both a series resistor and the sweep rate were studied. For dynamic models the simulation accuracy highly depends on the use of the actual material system parameters, which are not know completely, and thus must be approximated by literature values. In consequence, absolute values which result from dynamic simulations do not match measurement results perfectly, but qualitative device behavior can be investigated in detail, which is not possible via basic models.
The advantage of basic models is the direct availability from empirical data, in contrast to dynamical models which are much more complex to obtain. On the other hand, dynamic models offer a greater range of operations by reflecting the actual device physics. It is important to note that dynamic models must reflect the strong non-linearity which is present in resistive switches to obtain correct simulation results, hence simple dynamic linear models are not usable for simulation.
In conclusion, complementary resistive switches can be considered as a single two-terminal device, thus offering excellent properties for passive crossbar array implementation (1CRS). The concept is not limited to a specific material system, and can be applied on all bipolar resistive switches, thereby giving this device a wide area of applications.

5 Complementary Resistive Switches - Memory Applications

In section 2.1, several candidates for future non-volatile memory applications were introduced. Especially bipolar resistive switches (see section 2.2) offer high potential for ultimately scaled memory devices. In combination with the memory architecture with the highest possible density, which is the passive crossbar array (see section 2.6), the best results can be expected. But, due to the sneak path problem (section 2.7), the performance of BRS-based crossbar arrays is limited. One option to arrive at the expected high performance is to replace BRS by CRS.
This chapter is organized as follows: Before making a comparison between BRS- and CRS-based arrays in section 5.3, the basic memory operations and needed constraints for crossbar array implementations are introduced in section 5.1 and 5.2, respectively. Finally, in section 5.4 an alternative readout concept based on a capacitive voltage divider setup with no need for a writeback step is presented.

5.1 Basic Memory Operation

For CRS cells, the write operation is similar to the BRS write operation (see section 5.1.1), while the read operation is very different from a BRS read. Basically, there are two possibilities for read, either level read (see section 5.1.2) or spike read (section 5.1.3). In section 5.1.4, the differing properties of CRS cells consisting of asymmetric elements are discussed, and in section 5.1.5 experimental results showing the basic memory operations are provided.

5.1.1 Write Operation

Starting from the quasi-static I-V characteristics of a symmetrical cell, a procedure can be deduced which allows the use of these cells as memory storage cells. As listed in table 4.1, state HRS/LRS is assigned to storing state '0' and LRS/HRS to storing state '1'. To write a CRS memory cell to one of these storing states, a write voltage $V_{\mathrm{Write1}} < V_{\mathrm{th,4}}$ or $V_{\mathrm{Write0}} > V_{\mathrm{th,2}}$ is needed (see Fig. 5.1a). Hence, the write operation is comparable to the write operation for bipolar resistive switches. In Fig. 5.1a, the required write voltage levels are marked.

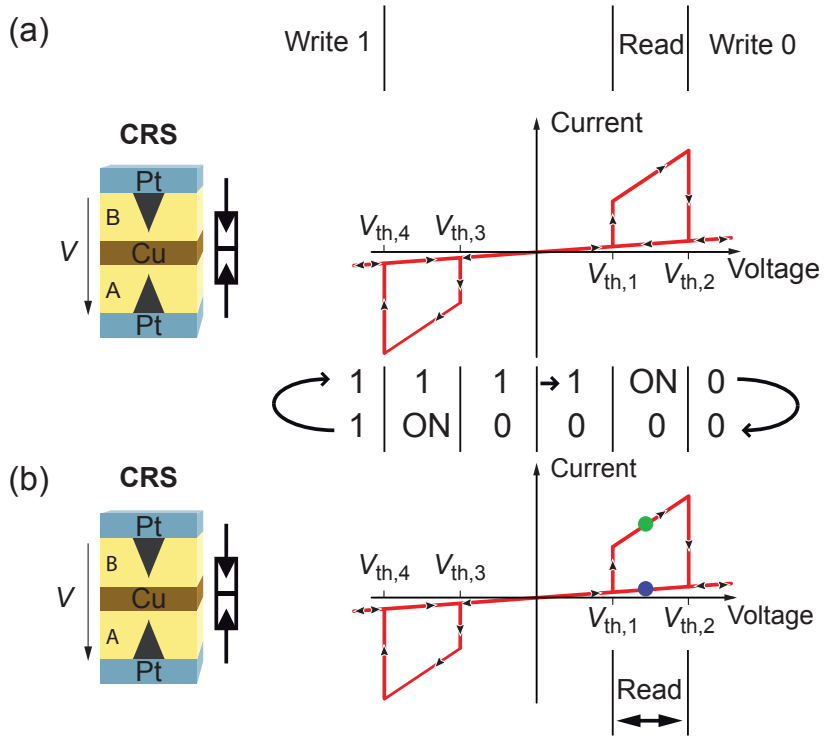


Figure 5.1: (a) Voltage levels needed for a symmetrical CRS cell. (b) Level read of a symmetrical CRS cell.

5.1.2 Level Read

For bipolar resistive switches, a small read voltage is applied to the BRS element and the resulting read current is measured. To read CRS cells, a different read scheme is needed since CRS cells are high-resistive in both states, '0' and '1'. For CRS cells a read voltage is required which must be sufficiently large to switch the CRS cell to state 'ON', but smaller than the write voltage. Thus, $V_{\mathrm{th},1} < V < V_{\mathrm{th},2}$ must hold true (Fig. 5.1b). A switching to the 'ON' state only occurs if state '1' applies (Fig. 5.1b, green circle), while no switching occurs for state '0' (Fig. 5.1b, blue circle). As for bipolar resistive switches, a current level detection is used to distinguish logic states in the read phase. Because reading is destructive for CRS cells, a write-back is needed. Therefore, after reading a '1', a negative write pulse is needed to restore the information.

In Fig. 5.2 a typical memory operation scenario is shown. Here, the basic linear branch model is used (compare section 4.3.1). Starting from a CRS cell in state '0', a first read operation is performed ①. Since no switching occurs, the CRS cell stays high-resistive (state '0') and no current flows. In step ② a negative write pulse is applied to switch the CRS cell to state '1'. Next, in step ③ a read

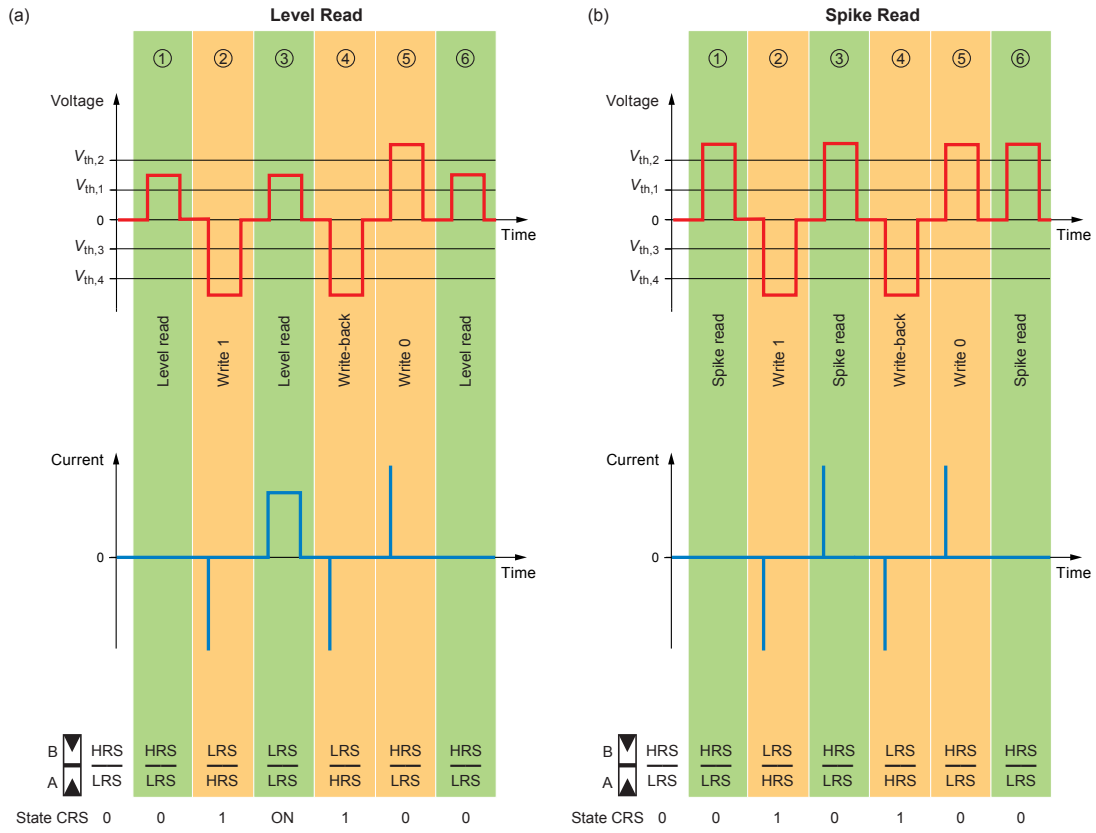


Figure 5.2: a) Exemplary pulses showing the level read operation. (b) Corresponding spike read operation. Adapted from [50].

operation ($V_{\mathrm{th},1} < V < V_{\mathrm{th},2}$) switches element B to LRS, thus overall resistance is low (state 'ON'). In order to restore information, a write-back step ④ is needed to set the cell to state '1' again. In step ⑤ the memory cell is set to state '0', hence the reading result in step ⑥ is the same as in step ①.

5.1.3 Spike Read

Beside the level read scheme, there is a second feasible read approach which does not need a special read voltage. Instead of a current level detection a current spike detection is used. Current spikes always appear when CRS cells switch, thus they allow for state detection. In Fig. 5.2b an example for a memory operation with spike read detection is given. The memory operation corresponds directly to the operation depicted in Fig. 5.2a and starts with a CRS cell in state '0'. Instead of switching to the 'ON' state, the CRS is directly switched to '0' if the cell was in state '1' before. The current spike resulting from switching from '1' to '0' is used for state detection.

The pulse train starts again with a read operation. To do this, a read voltage identical to the positive write voltage is applied ①. Because no switching occurs for the CRS cell in state '0' by application of a positive write voltage, no current spike is present. In step ② the CRS cell is switched to state '1'. For reading ③ a positive write voltage is applied, which results in a current spike; thus, CRS state '1' is detected. In step ④ a write-back of state '1' is performed, while state '0' is written in step ⑤. This state is identical to the initial state, hence reading in step ⑥ again results in no current spike. As for the level read, a write-back step is needed after the read operation.
According to measurements, switching times of $< 200\mu$s for $Cu/SiO_2/Pt$-based CRS cells are known [109]. Simulations also show the feasibility of nanosecond switching times (compare Fig. 4.24), which would lead to very short current spikes, allowing for fast spike read operations.

5.1.4 Asymmetrical BRS-based CRS Cells

For CRS cells built up of very asymmetric BRS elements ($|2 \cdot V_{\mathrm{Reset}}| < |V_{\mathrm{Set}}|$) there is no stable LRS/LRS state (compare section 4.3.1), which is why $V_{\mathrm{th},1} \approx V_{\mathrm{th},2}$ and $V_{\mathrm{th},3} \approx V_{\mathrm{th},4}$ holds true if no series resistor is inserted. Thus, for write '0' a voltage $V_{\mathrm{Write0}} > V_{\mathrm{th},1}$ is applied, while for write '1' a voltage $V_{\mathrm{Write1}} < V_{\mathrm{th},3}$ is needed. The spike read is the straight forward approach for reading. By selecting $V_{\mathrm{Read}} = V_{\mathrm{Write0}}$ a spike read operation can be performed. If connecting a series resistor to the CRS cell for read, level read can be established as well. In this case, the read voltage $V_{\mathrm{Read}} = V_{\mathrm{Write0}}$ is the same as for the spike read, but, due to the series resistor, it leads to a level read operation (see Fig. 5.3b). Note that this specific series resistor is not part of the cross point junction, but is present in the external circuitry.

5.1.5 Pulsed Measurements on CRS Cells

To prove the read and write properties of CRS cells, anti-serially connected ECM elements were used. In Fig. 5.4, applied voltage pulses as well as the corresponding current response are depicted. Write voltages of $V_{\mathrm{Write0}} = 5\,\mathrm{V}$ and $V_{\mathrm{Write1}} = -7\,\mathrm{V}$, respectively, were selected, and a read voltage of $V_{\mathrm{Read}} = 1.2\,\mathrm{V}$ was applied. A pulse width of 100 ms applies in these pulse experiments. Note that in contrast to simulation (compare Fig. 5.2), a non-zero current in the write phases occurs, but is not relevant for read (compare Fig. 5.2). Additionally, lower write voltages should be selected for use in crossbar arrays (see section 5.2). The level read scheme enables the detection of former '1' states via a current flow in the read phase because of

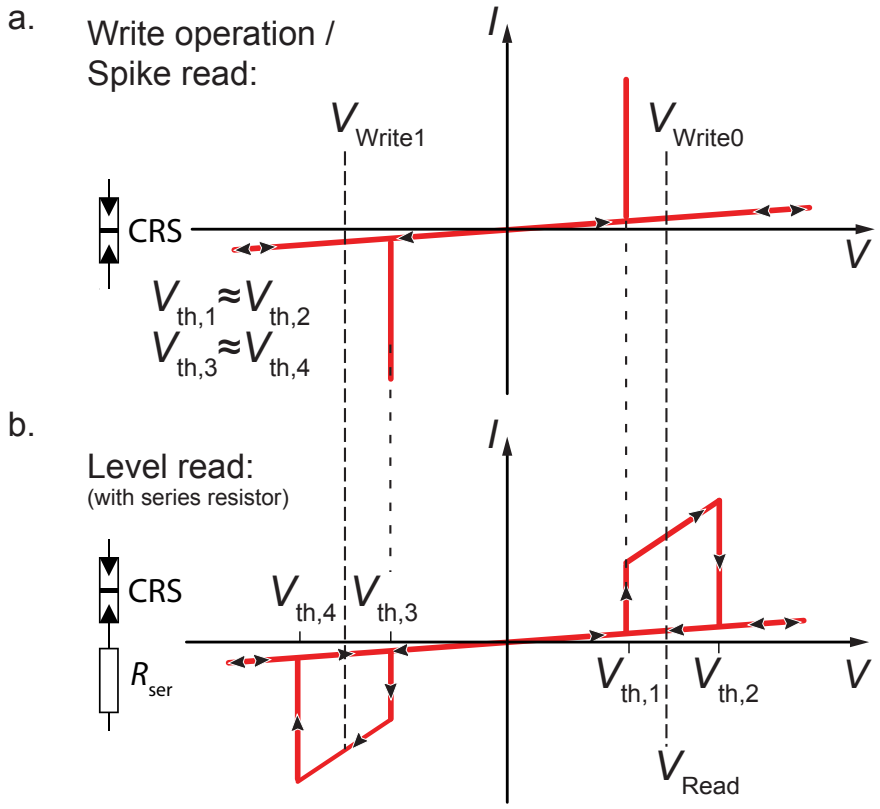


Figure 5.3: CRS cell consisting of two asymmetric BRS elements. (a) Write operation / Spike read. (b) Level read with series resistor.

switching the CRS cell to state 'ON'. Since the CRS is initially in state '1' (Fig. 5.4, left pulse train), the first read step directly switches the cell to the 'ON' state. The next positive write step changes the cell state to '0', hence no current flow is present in the succeeding read phase. The application of further write '0' attempts and read pulses does not affect this state. Starting from state '0' (Fig. 5.4, right pulse train) no significant current flows during the first read cycle, since the CRS is in state '0'. The first negative write pulse switches the CRS to state '1' and the large current response during the following positive read pulse proves the state to be 'ON'. To restore the information, a negative write pulse switches the CRS to state '1'.

The feasibility of the spike read scheme is also visible in Fig. 5.4, since there is a current spike whenever switching from state '0' to '1' or vice versa occurs. An arrow indicates current spikes in the current trace. In these measurements a series resistor of 940 Ω was implemented to assure that a stable LRS/LRS state occurs, since used ECM elements ($Pt/SiO_2/GeSe/Cu$) show a very asymmetric I-V characteristic, as already described for quasi-static triangular sweep operation in section 4.2.1.

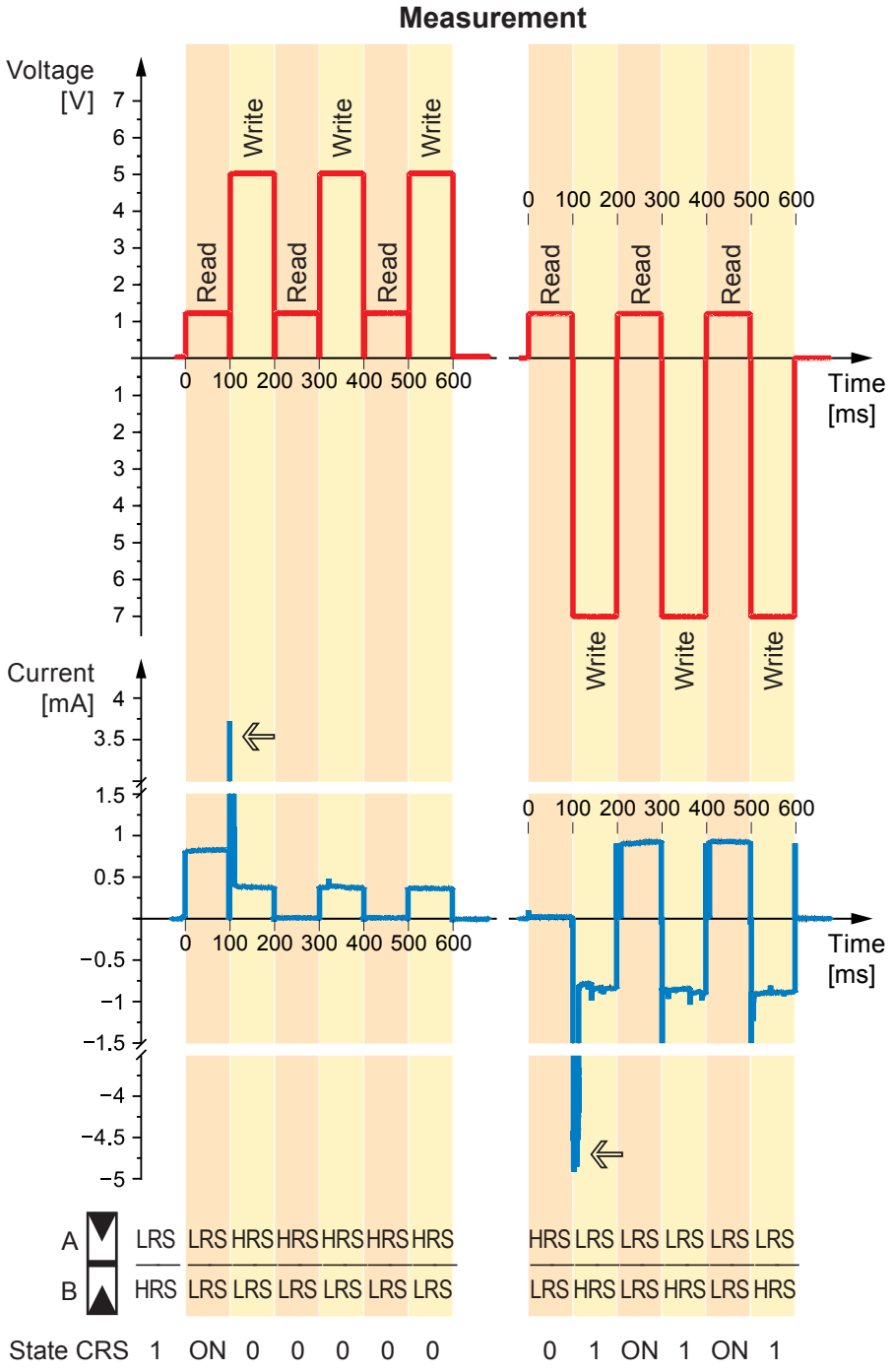


Figure 5.4: Measured CRS behavior of two Pt/SiO_2/GeSe/Cu elements with a 940 Ω current limiter resistance in series. Initially, the CRS is in state '1'. Each read pulse is followed by a write pulse with positive or negative polarity, respectively. The following voltage amplitudes were applied: 5 V (write '0'), 7 V (write '1') and 1.2 V (read). It should be noted that if the cell state changes during a write step, short current spikes occur (indicated by arrows). From [50].

Pulse measurements were also carried out with integrated CRS cells. In these structures an accessible middle electrode was processed (compare Fig. A.1) to access individual voltage drops at elements A and B (Fig. 5.5a). By tracing the applied voltage pulse train (Fig. 5.5b) as well as element voltages V_A (Fig. 5.5c) and V_B (Fig. 5.5d), the correct switching behavior of the CRS cell is visible. The applied voltage amplitude is $V = \pm 4\,\mathrm{V}$ with a pulse width of 5 ms. Due to the large HRS to LRS ratio, almost the entire voltage drop is present at the high-resistive element. When applying a positive write pulse (4 V) the CRS cell switches to state '0' (A:LRS/B:HRS) and for a negative write pulse ($-4\,\mathrm{V}$) the CRS cell switches to '1' (A:HRS/B:LRS). In Fig. 5.5c-d, the corresponding voltage drops at elements A and B are shown. Integrated cells do not require an accessible middle electrode, but for a CRS proof of concept study such a middle electrode is advantageous for the cell state check.

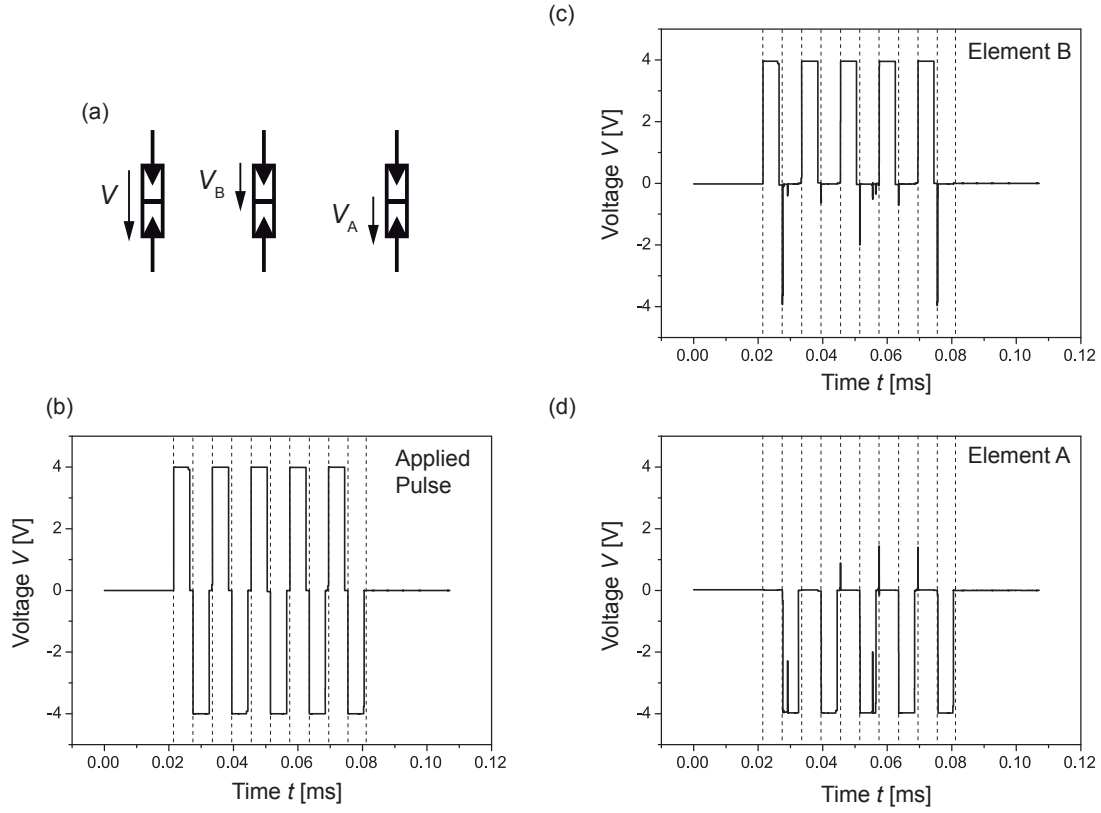


Figure 5.5: (a) Voltage measurement with accessible middle electrode. (b) Pulse train to $Pt/SiO_2/Cu$-based integrated CRS cells with accessible middle electrode. (c) Voltage drop at element B. (d) Voltage drop at element A. Compare [41].

5.2 Constraints for CRS in Crossbar Arrays

The major benefit of using CRS cells instead of BRS elements ensues from the fact that CRS cells are always high-resistive (see chapter 4). In Fig. 5.6 a cutout of a passive crossbar array is shown to illustrate this property. Here, a level read operation for reading the cell in the middle of the array is considered. In case 1 the cell is in state '0' (marked as blue cell), while in case 2 the cell is in the 'ON' state (marked as green cell). A low-resistive 'ON' state only occurs if state '1' was present before the application of the read voltage. Thus, a large current is only present when reading a '1' (thick red line in case 2, see also section 5.1.2). Since all non-accessed cells are either in state '0' or '1' (marked as blue cells), and are therefore high-resistive, sneak currents are low (thin red line). Note that in order to keep the example simple, only one sneak path is drawn. The difference of currents between case 1 and 2 is large, which is why the state detection is very straight forward compared to BRS-based arrays (compare Fig. 2.8). However, CRS-based as well as BRS-based crossbar arrays share one important constraint, which is the voltage scheme needed to prevent non-accessed cells from switching.

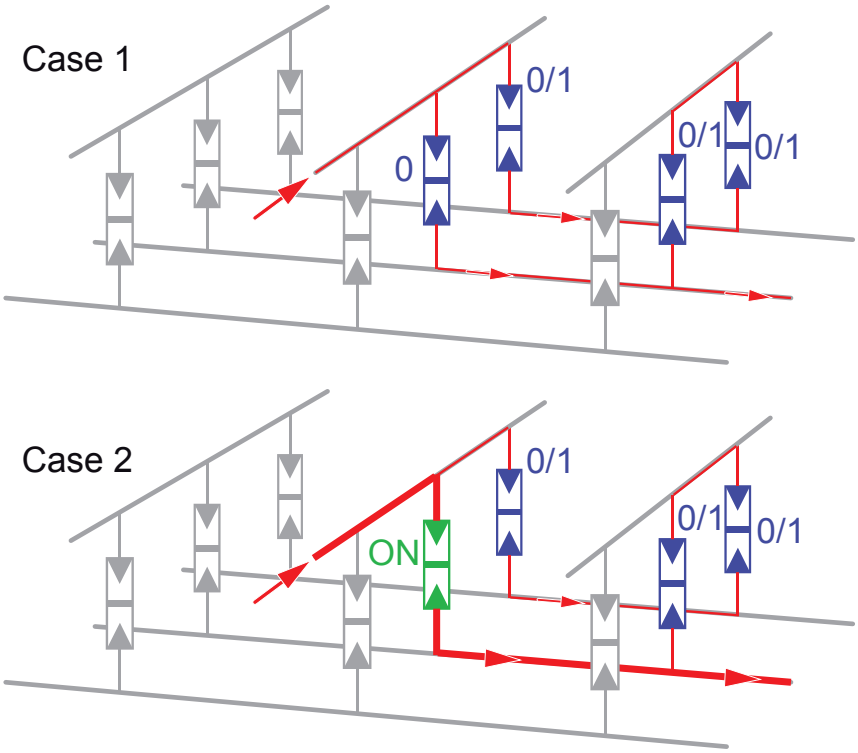


Figure 5.6: Sneak path in CRS-based arrays. The cell in the middle is either in state '0' (Case 1) or in state '1'/'ON' (Case 2).

In BRS-based crossbar arrays non-accessed cells can be prevented from switching by selecting either a $\frac{1}{2} \cdot V$ voltage scheme or a $\frac{1}{3} \cdot V$ scheme (compare Fig. 2.7) when writing a state. For CRS it is important that voltages at all non-accessed cells are limited to values below the threshold voltage $V_{\mathrm{th},1}$ and $V_{\mathrm{th},3}$, respectively. To achieve this for arrays based on CRS consisting of two symmetrical BRS elements, a $\frac{1}{3} \cdot V$ voltage scheme is needed for the write operation. This results from the fact that a voltage larger than $V_{\mathrm{th},2}$ is needed for the write-operation. For the level read, either a $\frac{1}{2} \cdot V$ voltage scheme or a $\frac{1}{3} \cdot V$ scheme can be applied. Fig. 5.7 shows the voltage drop at non-accessed cells, either positive or negative, for the same pulse train as shown in Fig. 5.2a when applying a $\frac{1}{3} \cdot V$ scheme for write as well as for level read. The voltage level for non-accessed cells must stay in the range marked with 'no change' in Fig. 5.7.

For CRS cells formed by asymmetric BRS elements (compare section 5.1.4) different properties hold true: As for pure symmetrical BRS elements, a $\frac{1}{2} \cdot V$ voltage scheme is also applicable for the write operation. This feature results from the fact that $V_{\mathrm{th},1} \approx V_{\mathrm{th},2} \approx V_{\mathrm{Set}}$ as well as $|V_{\mathrm{th},3}| \approx |V_{\mathrm{th},4}| \approx V_{\mathrm{Set}}$ (see section 5.1.4). As a result, voltage margins are improved by putting asymmetric BRS elements into a CRS configuration instead of merely using asymmetric BRS elements (compare voltage scheme described in [49]).

In general, if the HRS values of the elements A and B are all identical, the use of a special voltage scheme is not needed. Thus, non-accessed rows and columns can be left floating. This can be understood by having a look at Fig. 5.6. If all non-accessed cells have the same resistance (which is HRS) the voltage drop at each cell is $\frac{1}{3} \cdot V$, which is why no switching occurs at those cells. This property is a

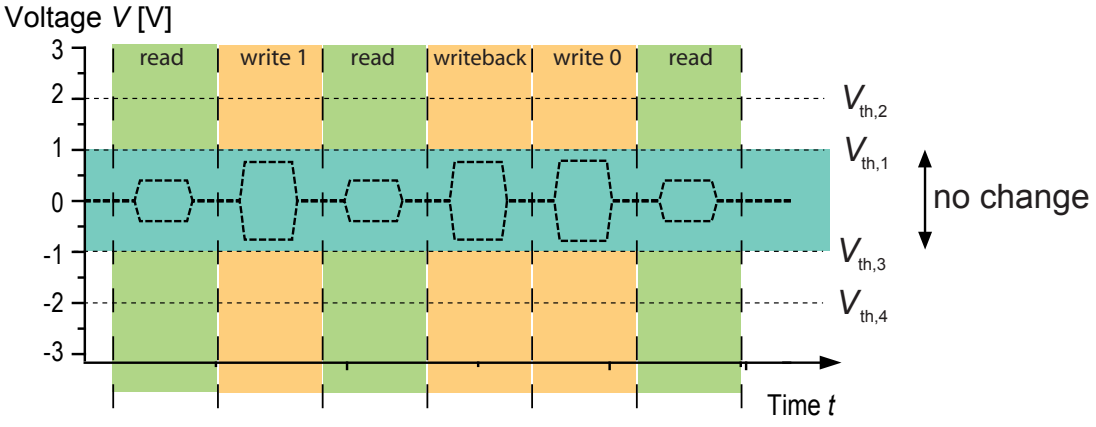


Figure 5.7: Pulse simulation of non-accessed CRS cells in a crossbar array.

direct consequence of the absence of pattern dependency, which is not present in BRS-based crossbar arrays.

5.3 Comparison BRS-based Array - CRS-based Array

It is a basic operation for a memory array to read information stored in the array. For passive crossbar arrays there are patterns which make it easy to restore information, while others will complicate the retrieval of the correct information.
To illustrate this issue, two crossbar arrays, one made of BRS elements (Fig. 5.8a) and one made of CRS cells (Fig. 5.8c), are considered. Both arrays consist of N

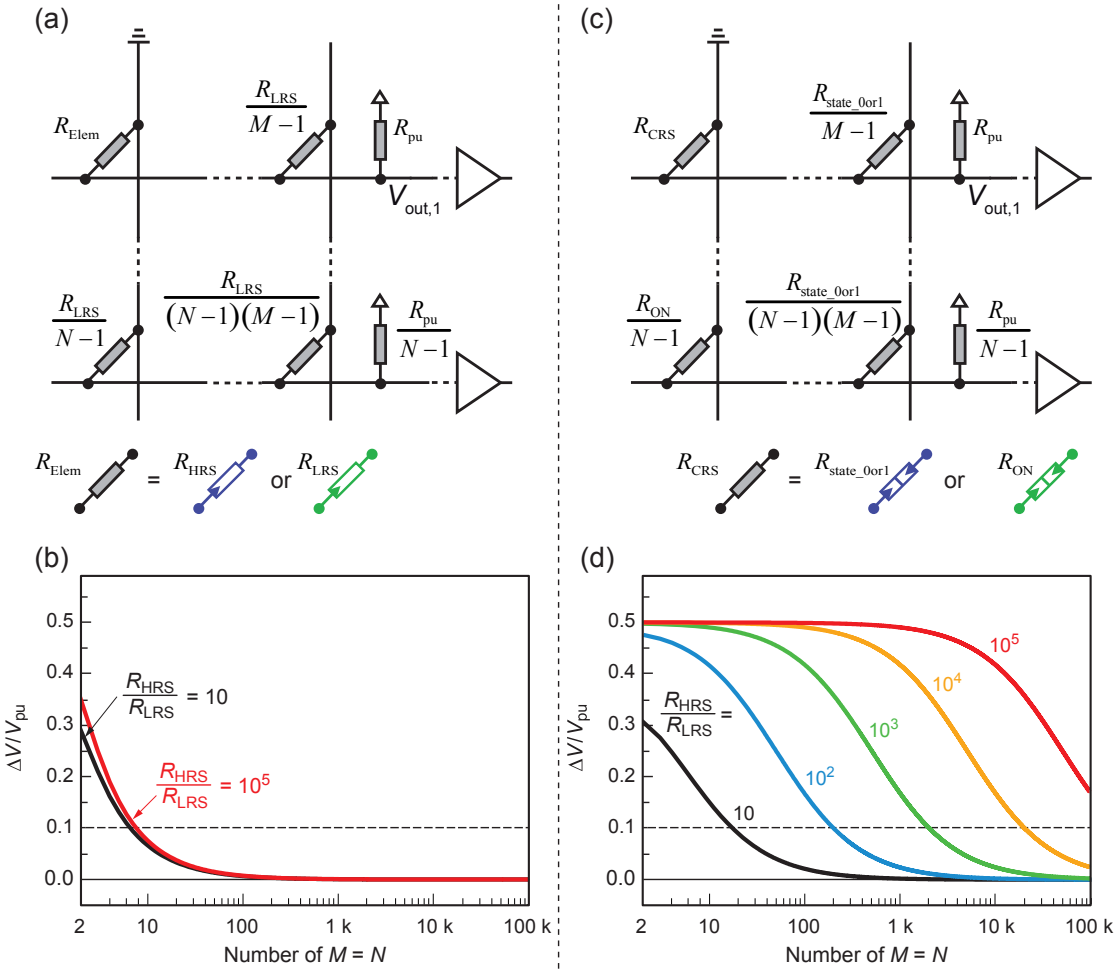


Figure 5.8: (a) Reduced BRS crossbar array. (b) BRS array voltage swing as function of $N \cdot M$ array. (c) Reduced CRS crossbar array. (d) CRS voltage swing as function of $N \cdot M$ array. Adapted from [50].

rows and M columns. To simplify matters, $N = M$ is assumed in the calculations. To allow for a better comparison, both arrays store the same digital information, which is a worst-case pattern in this case.

As depicted in Fig. 2.8, a situation in which a high-resistive element is surrounded by low-resistive elements is such a worst-case. For a BRS element array this means that all matrix elements are in LRS, while for CRS cells at worst only those cells that are in one column are in state 'ON' if reading a complete word. For those patterns the corresponding circuit model can be simplified to a four resistor matrix as shown in Fig. 5.8a,c with N = number of columns and M = number of rows. One element/cell (the upper left) is considered to be toggled between HRS and LRS (BRS-based array) and state '0' and state 'ON' (CRS-based array), respectively. For BRS arrays this means $R_{\mathrm{Elem}} = R_{\mathrm{HRS}}$ or $R_{\mathrm{Elem}} = R_{\mathrm{LRS}}$. For all $N - 1$ non-considered elements, the column which is read is then assumed to be low-resistive, represented by the lower left element. Similarly, all $M - 1$ elements in the row of the considered element are represented by the upper right element. The lower right element represents all other $(N - 1) \cdot (M - 1)$ matrix elements which are low-resistive as well. For a CRS array, $R_{\mathrm{CRS}} = R_{\mathrm{state\_0or1}}$ or $R_{\mathrm{CRS}} = R_{\mathrm{ON}}$ holds true for the considered cell in the upper left position. In contrast to BRS arrays, only the cells in the accessed column can be low-resistive (state 'ON'), whereby all other cells are high-resistive ($R_{\mathrm{state\_0or1}}$).

For comparison of BRS and CRS arrays, the voltage swing ΔV is evaluated (compare [21]). Voltage swing here means the change in V_{out} and is sensed at the pull-up resistor R_{pu}, where the voltage V_{pu} is applied as supply voltage. The output voltage V_{out} results from the voltage divider with the element/cell which is read, either R_{Elem} or R_{CRS}.

To simplify matters, the output voltage is normalized with V_{pu}. Fig. 5.8b shows the resulting voltage swing normalized to V_{pu} as function of the array size (for $N = M$) for BRS element arrays, and Fig. 5.8d shows the normalized voltage swing for CRS-based arrays. R_{pu} is set to $R_{\mathrm{LRS}} = 1\,\mathrm{k\Omega}$ or $R_{\mathrm{ON}} = 2R_{\mathrm{LRS}}$, respectively. By doing so, the maximum voltage swing is half of the applied voltage V_{pu}. Due to a strong sneak path presence for BRS element arrays, the array size is limited to 8 by 8 when assuming $0.1 \cdot \frac{\Delta V}{V_{\mathrm{pu}}}$ as minimum voltage margin, almost independent of the HRS to LRS ratio. In Fig. 5.8b,

$$\frac{\mathrm{HRS}}{\mathrm{LRS}} = 10 \text{ (black) and } \frac{\mathrm{HRS}}{\mathrm{LRS}} = 10^5 \text{ (red)}$$

are depicted. For CRS-based arrays the situation is much better, since cells in non-accessed columns are always high-resistive. In Fig. 5.8d the influence of the resistance ratio is shown, increasing the possible array size from about $N = 10$ by $M = 10$ for

$$\frac{\text{HRS}}{\text{LRS}} = 10$$

to over $N = 10,000$ by $M = 10,000$ for

$$\frac{\text{HRS}}{\text{LRS}} = 10^4.$$

Note that there is a trade-off between array size and performance in terms of access time because of an increasing RC delay for larger arrays, and there is an additional constraint for the line resistance: R_{Line} should be lower than R_{ON}, for instance, $R_{\text{Line}} \leq 10\%\ R_{\text{LRS}}$, to prevent significant voltage drop on the word and bit lines.
Below, the equation of the line resistance R_{Line} is derived (compare [11]). To achieve a realistic result, the size effect of the wire is accounted for by application of the Fuchs-Sondheimer approximation [110]:

$$\rho_{\text{Cu}}(F) = \rho_{\text{Cu,0}} \left(1 + \frac{3}{4}\frac{\lambda_0}{F}(1-p)\right) \tag{5.1}$$

F is the feature size, $\rho_{\text{Cu,0}}$ is the bulk resistivity of copper ($\rho_{\text{Cu,0}} = 2.37\ \mu\Omega\text{cm}$), λ_0 is the bulk mean free path ($\lambda_0 = 28\,\text{nm}$) and p is the specularity ($p = 0.5$); the values are taken from [11]. So the worst-case line resistance R_{Line} for an element in the middle of an array and an assumed aspect ratio of the interconnect line of ten is:

$$R_{\text{Line}} = \rho_{\text{Cu}}(F)\frac{L}{A} = \rho_{\text{Cu}}(F)\frac{2 \cdot N \cdot F}{F \cdot 10F} = \rho_{\text{Cu}}(F)\frac{2 \cdot N}{F \cdot 10} \tag{5.2}$$

For $F = 20\,\text{nm}$ and an array size of N by N, a line resistance of $R_{\text{Line}}(N) = N \cdot 0.36\ \Omega$ results. For $N = 10^4$ a line resistance $R_{\text{Line}} = 3.6\,\text{k}\Omega$ is present, which leads to $R_{\text{ON}} \geq 36\,\text{k}\Omega$ reaching $R_{\text{Line}} \leq 10\%\ R_{\text{ON}}$. The total resistance is $R_{\text{total}} = R_{\text{Line}} + R_{\text{ON}} \approx 40\,\text{k}\Omega$.
The line capacitance C_{Line} for $N = 10^4$ and $F = 20\,\text{nm}$ can be estimated to be $C_{\text{Line}} \approx 1\,\text{pF}$ (see [11]), whereby the RC time constant is approximately $R_{\text{total}} \cdot C_{\text{Line}} \approx 40\,\text{ns}$ in this case. Since there is a square dependency on N, performance in terms of access time can be improved by a factor of 100 for $N = 10^3$, which is a more realistic array size than $N = 10^4$.
Below, the calculation of V_{out} and the output voltage swing ΔV is derived. For these considerations, the line resistance R_{Line} is again neglected, but it should be

kept in mind that this is only valid for $R_{\mathrm{Line}} \ll R_{\mathrm{ON}}$. For the minimum output voltage swing, the output voltage V_{out} for both storage states must be considered. All bit lines are pulled up, which was found to be advantageous for reading [21]. The equivalent circuit of the crossbar array can be seen in Fig. 5.9a, which can be simplified to Fig. 5.9b when considering reading the upper left element R_{Elem}. The derivation is done for a BRS array, but due to the same structure, results can be directly transfered to CRS arrays. In the first calculation step, a star-mesh transformation is needed, resulting in circuit model Fig. 5.9c. The resistances can

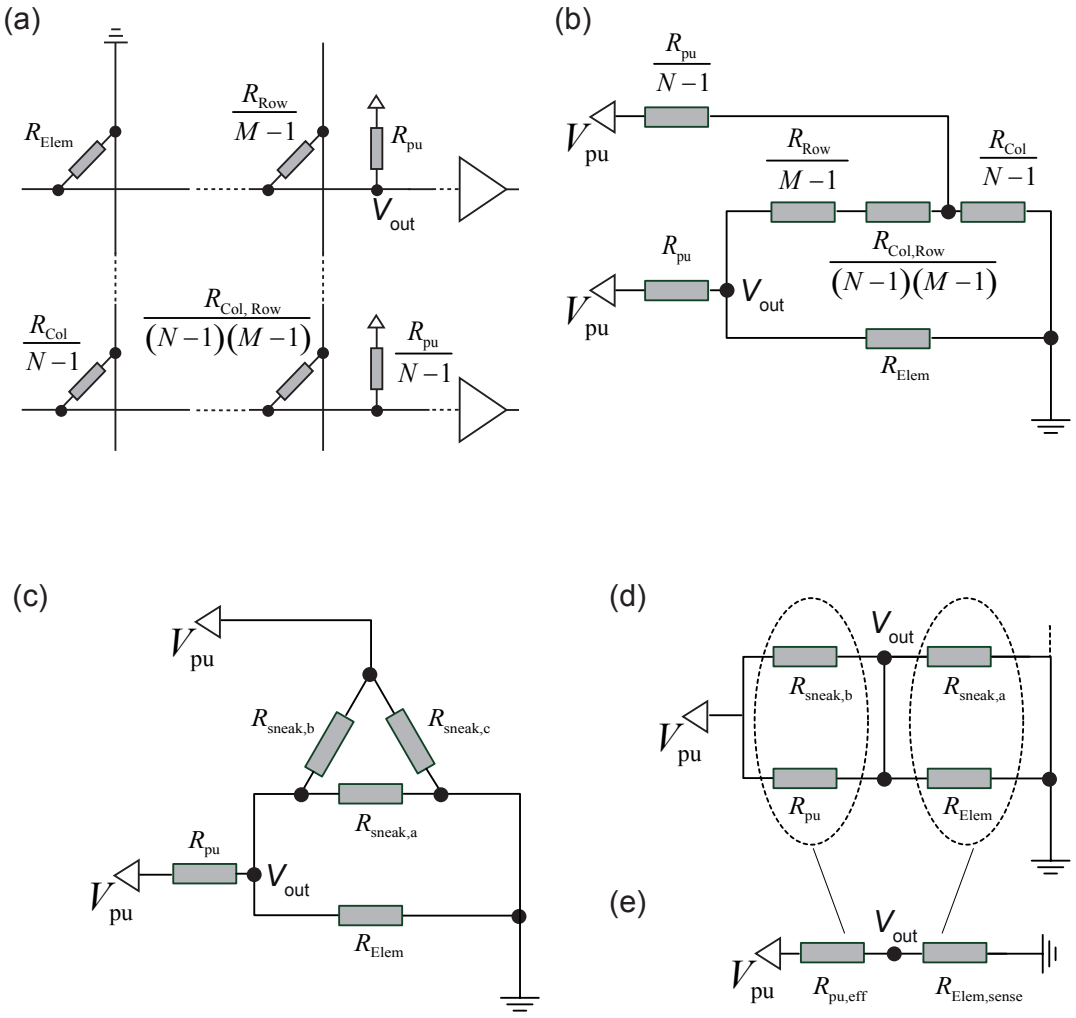


Figure 5.9: (a) Equivalent crossbar array for worst-case consideration. (b) The circuit can be redrawn for circuit analysis. (c) After star-mesh transformation this new circuit is present. (d) By rearranging of elements, circuit analysis is simplified. (e) For simplified equivalent circuit, parallel resistances are combined.

be calculated as follows:

$$R_{\text{sneak\_a}} = \frac{\left(\frac{R_{\text{LRS}}}{M-1} + \frac{R_{\text{LRS}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{LRS}}}{N-1} + \frac{R_{\text{pu}}}{N-1} \cdot \frac{R_{\text{LRS}}}{N-1} + \left(\frac{R_{\text{LRS}}}{M-1} + \frac{R_{\text{LRS}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{pu}}}{N-1}}{\frac{R_{\text{pu}}}{N-1}} \tag{5.3}$$

$$R_{\text{sneak\_b}} = \frac{\left(\frac{R_{\text{LRS}}}{M-1} + \frac{R_{\text{LRS}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{LRS}}}{N-1} + \frac{R_{\text{pu}}}{N-1} \cdot \frac{R_{\text{LRS}}}{N-1} + \left(\frac{R_{\text{LRS}}}{M-1} + \frac{R_{\text{LRS}}}{(N-1)(M-1)}\right) \cdot \frac{R_{\text{pu}}}{N-1}}{\frac{R_{\text{LRS}}}{N-1}} \tag{5.4}$$

The resistance $R_{\text{sneak,c}}$ is not needed for the calculation, and therefore not derived here. For calculation of V_{out} the resistance of the parallel resistors $R_{\text{sneak,a}}$ and R_{Elem} as well as $R_{\text{sneak,b}}$ and R_{pu} is needed (compare Fig. 5.9c,d,e):

$$R_{\text{Elem,sense}} = \frac{R_{\text{sneak\_a}} \cdot R_{\text{Elem}}}{R_{\text{sneak\_a}} + R_{\text{Elem}}} \tag{5.5}$$

$$R_{\text{pu,eff}} = \frac{R_{\text{sneak\_b}} \cdot R_{\text{pu}}}{R_{\text{sneak\_b}} + R_{\text{pu}}} \tag{5.6}$$

The corresponding voltage divider leads to the output voltage:

$$V_{\text{out}} = \frac{R_{\text{Elem,sense}}}{R_{\text{Elem,sense}} + R_{\text{pu,eff}}} \cdot V_{\text{pu}}. \tag{5.7}$$

In the case of a BRS array considered in Fig. 5.8b

$$\frac{\Delta V_{\text{out}}}{V_{\text{pu}}} = \frac{R_{\text{HRS,sense}}}{R_{\text{HRS,sense}} + R_{\text{pu,eff}}} - \frac{R_{\text{LRS,sense}}}{R_{\text{LRS,sense}} + R_{\text{pu,eff}}} \tag{5.8}$$

holds true. For the CRS array case considered in Fig. 5.8d, the output voltage swing can be calculated with a corresponding equation, doing a recalculation with cell resistances shown in 5.8c:

$$\frac{\Delta V_{\text{out}}}{V_{\text{pu}}} = \frac{R_{\text{state\_0,sense}}}{R_{\text{state\_0,sense}} + R_{\text{pu,eff}}} - \frac{R_{\text{ON,sense}}}{R_{\text{ON,sense}} + R_{\text{pu,eff}}}. \tag{5.9}$$

Until now, a special worst-case pattern was considered. To calculate the smallest possible voltage swing, two different worst-case scenarios - one for reading each state - must be considered for the BRS array. For $R_{\text{Elem}} = R_{\text{HRS}}$ all other elements are in LRS. This corresponds to $R_{\text{Row}} = R_{\text{Col}} = R_{\text{Col,Row}} = R_{\text{LRS}}$ in Fig. 5.9a. But, in the worst-case for reading an element in LRS ($R_{\text{Elem}} = R_{\text{LRS}}$), all other elements are in HRS. In Fig. 5.9a this corresponds to $R_{\text{Row}} = R_{\text{Col}} = R_{\text{Col,Row}} = R_{\text{HRS}}$. So, since

patterns are different for reading HRS and LRS, $R_{\text{sneak,a}}$ (see equation (5.3)) and $R_{\text{sneak,b}}$ (see equation (5.4)) differ, too. Therefore, two different effective pull-up resistances $R_{\text{pu,eff,HRS}}$ and $R_{\text{pu,eff,LRS}}$ result. Now, the minimum normalized voltage swing for BRS-based arrays reads (see Fig. 5.10a):

$$\frac{\Delta V_{\text{out}}}{V_{\text{pu}}} = \frac{R_{\text{HRS,sense}}}{R_{\text{HRS,sense}} + R_{\text{pu,eff,HRS}}} - \frac{R_{\text{LRS,sense}}}{R_{\text{LRS,sense}} + R_{\text{pu,eff,LRS}}}. \tag{5.10}$$

Similarly, for a CRS array all other cells in a column are in the 'ON' state for reading state '0', while they are in state '0' for reading an 'ON' state in the worst-case scenario. The effective pull-up resistances $R_{\text{pu,eff,state\_0}}$ and $R_{\text{pu,eff,ON}}$ are consequently state dependent. Cells in the non-accessed columns can either be '1' or '0', but do not effect the voltage swing, since both states have the same

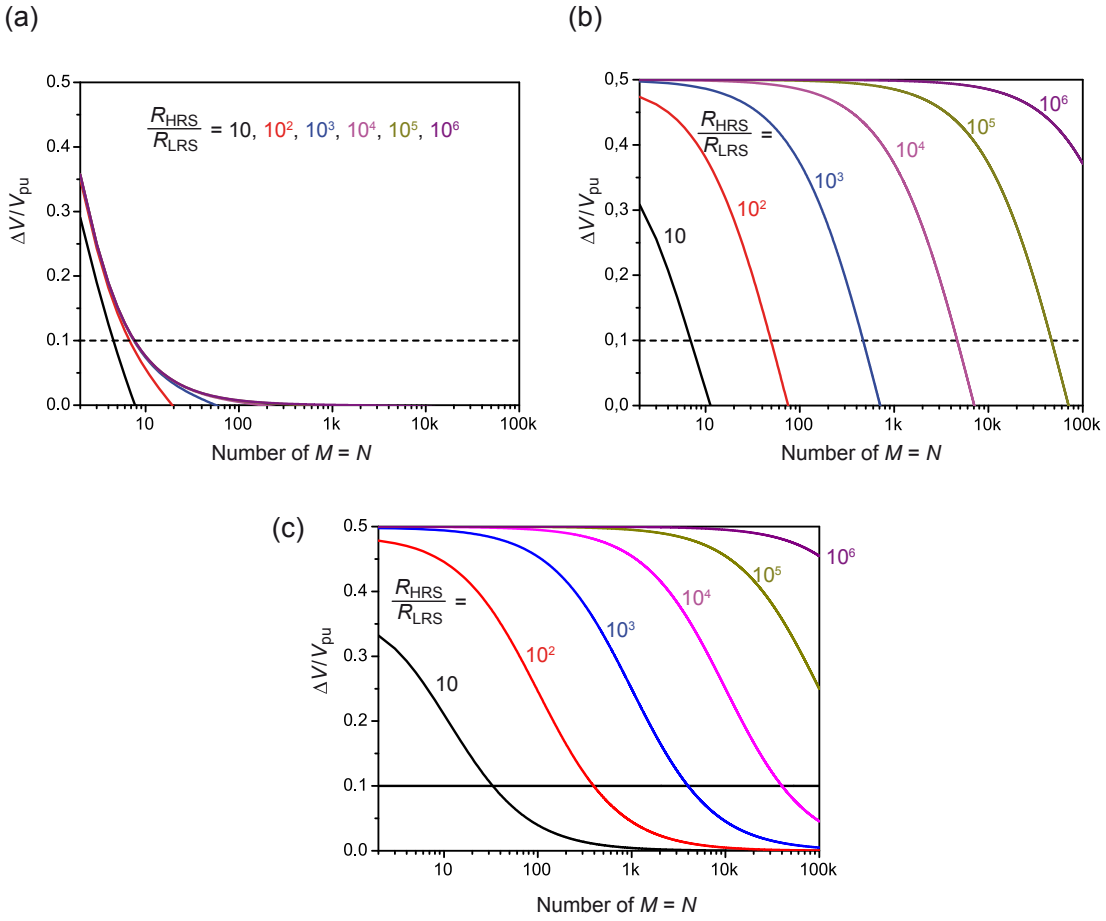


Figure 5.10: Minimum normalized voltage swing for BRS array (a) and CRS array (b) when reading a word. (c) Minimum normalized voltage swing for reading a single CRS cell.

high-resistance (compare table 4.1). Hence, the minimum normalized voltage swing for CRS-based arrays reads:

$$\frac{\Delta V_{\mathrm{out}}}{V_{\mathrm{pu}}} = \frac{R_{\mathrm{state\_0,sense}}}{R_{\mathrm{state\_0,sense}} + R_{\mathrm{pu,eff,state\_0}}} - \frac{R_{\mathrm{ON,sense}}}{R_{\mathrm{ON,sense}} + R_{\mathrm{pu,eff,ON}}}. \tag{5.11}$$

Fig. 5.10a and b depict the minimum normalized voltage swing for a BRS-based array and a CRS-based array, respectively, for

$$\frac{\mathrm{HRS}}{\mathrm{LRS}} = 10, 10^2, 10^3, 10^4, 10^5, 10^6.$$

When considering the read of a single CRS instead of a complete word, the normalized voltage swing can be further increased since there is no pattern dependency. This means that the voltage swing is always the same and depends only on the array size. Fig. 5.10c shows the normalized voltage swing for reading a single CRS cell for

$$\frac{\mathrm{HRS}}{\mathrm{LRS}} = 10, 10^2, 10^3, 10^4, 10^5, 10^6.$$

5.4 Non-Destructive Readout

To overcome the limitations of a destructive readout (compare section 5.1.2 and 5.1.3), alternative approaches for reading CRS cells can be applied. Below, two concepts allowing for a non-destructive readout are presented, one based on elements with different capacitances and one based one non-ohmic branches in VCM-based CRS devices.

5.4.1 Capacitive Voltage Divider-Based Readout

The basic idea for this approach is that resistive switches are not pure resistive elements, but - since structured in a metal-isolator-metal structure (compare section 2.2) - can also be considered a capacitor. Hence, the equivalent circuit model of a resistive switch MIM structure consists of a resistor (either HRS or LRS) and a capacitor (compare, e.g., [111]). Note that the element capacitance is short-circuited in the LRS state, while the HRS state is capacitance-dominated in general (see Fig. 5.11).

For CRS cells this property can be used for an alternative readout scheme [112]. By considering two resistive switching elements with similar switching behavior but different capacitances, a non-destructive capacitive readout is possible. To obtain different capacitances, different geometries, e.g., electrode areas or electrode

distances, or materials with different dielectric constants are needed. When using a parallel layout CRS configuration, the simplest way to obtain different capacitances is by different electrode areas. In Fig. A.3 such a modified parallel layout is shown, offering a ratio of three to one in terms of capacitances ($C_\mathrm{A} = 3 \cdot C_\mathrm{B}$). In Fig. 5.11a,b the equivalent circuit models of a CRS cell in state '0' and '1' are depicted. In state '0' the high-resistive element B is dominated by capacitor C_B, while low-resistive element A is ruled by R_LRS. Accordingly, in state '1' (Fig. 5.11b) the element B is dominated by R_LRS while element A is governed by capacitor C_A. The overall capacitance is then either C_A or C_B, depending on the CRS state, allowing for a non-destructive readout by evaluating a capacitive voltage divider. In Fig. 5.11a,b, a capacitor C_out is used to form a capacitive voltage divider with the CRS cell capacitance C_cell. For the readout, the output voltage V_out is measured by a sense amplifier.

In the following lines the applicability of this readout approach is first derived theoretically and then proved by measurement results. Starting from the initial equivalent circuit model, the capacitive voltage divider leads to this equation:

$$\frac{V_\mathrm{out}}{V_\mathrm{in}} = \frac{\left(1 + \frac{\omega^2 R_\mathrm{A}^2 C_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2} + \frac{\omega^2 R_\mathrm{B}^2 C_\mathrm{B} C_\mathrm{out}}{1+\left(\omega C_\mathrm{B} R_\mathrm{B}\right)^2}\right) - j\left(\frac{\omega R_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2} + \frac{\omega R_\mathrm{B} C_\mathrm{out}}{1+\left(\omega C_\mathrm{B} R_\mathrm{B}\right)^2}\right)}{\left(1 + \frac{\omega^2 R_\mathrm{A}^2 C_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2} + \frac{\omega^2 R_\mathrm{B}^2 C_\mathrm{B} C_\mathrm{out}}{1+\left(\omega C_\mathrm{B} R_\mathrm{B}\right)^2}\right)^2 + \left(\frac{\omega R_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2} + \frac{\omega R_\mathrm{B} C_\mathrm{out}}{1+\left(\omega C_\mathrm{B} R_\mathrm{B}\right)^2}\right)^2} \tag{5.12}$$

If a large HRS to LRS ratio is assumed while the ratio of C_B to C_A is much smaller, equation (5.12) can be reduced. For state '1' ($R_\mathrm{B} C_\mathrm{B} << R_\mathrm{A} C_\mathrm{A}$)

$$\frac{V_\mathrm{out,1}}{V_\mathrm{in}} \approx \frac{1 + \frac{\omega^2 R_\mathrm{A}^2 C_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2} - j\left(\frac{\omega R_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2}\right)}{\left(1 + \frac{\omega^2 R_\mathrm{A}^2 C_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2}\right)^2 + \left(\frac{\omega R_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2}\right)^2} \tag{5.13}$$

holds true. For high frequency signals (i.e., a read pulse) equation (5.13) can be further simplified:

$$\frac{V_\mathrm{out,1}}{V_\mathrm{in}} \approx \frac{1 + \frac{\omega^2 R_\mathrm{A}^2 C_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2}}{\left(1 + \frac{\omega^2 R_\mathrm{A}^2 C_\mathrm{A} C_\mathrm{out}}{1+\left(\omega C_\mathrm{A} R_\mathrm{A}\right)^2}\right)^2} \approx \frac{1}{1 + \frac{C_\mathrm{out}}{C_\mathrm{A}}} = \frac{C_\mathrm{A}}{C_\mathrm{A} + C_\mathrm{out}}. \tag{5.14}$$

This is the result which was assumed initially, showing that C_{cell} is dominated by the capacitance of element A (C_{A}). For state '0' the corresponding property holds true, leading to

$$\frac{V_{\mathrm{out},0}}{V_{\mathrm{in}}} \approx \frac{C_{\mathrm{B}}}{C_{\mathrm{B}} + C_{\mathrm{out}}}. \tag{5.15}$$

To verify the readout procedure, $Cu/TiO_2/Pt$- as well as $Cu/SiO_2/Pt$-based CRS cells were selected for capacitive measurements. The electrode areas of element A were $A_{\mathrm{B}} = 50\ \mu\mathrm{m}^2$ and $A_{\mathrm{A}} = 150\ \mu\mathrm{m}^2$. The voltage pulse level was $V_{\mathrm{in}} = 0.5\,\mathrm{V}$ and the serial capacitor $C_{\mathrm{out}} = 24\,\mathrm{pF}$. For TiO_2 $R_{\mathrm{LRS}} \approx 130\ \Omega$ and $R_{\mathrm{HRS}} \approx 1\,\mathrm{M}\Omega$ were present while $R_{\mathrm{LRS}} \approx 130\Omega$ and $R_{\mathrm{HRS}} \approx 10\,\mathrm{M}\Omega$ occurred for SiO_2-based ECM cells. In Fig. 5.12a, measurement results for TiO_2-based cells show that state '1' and '0' can be distinguished, offering a normalized voltage margin of about

$$\frac{\Delta V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{V_{\mathrm{out},1} - V_{\mathrm{out},0}}{V_{\mathrm{in}}} = 8.1\%. \tag{5.16}$$

With equations (5.15) and (5.14), the capacitance ratio can be directly calculated from measurement results:

$$\frac{C_{\mathrm{B}}}{C_{\mathrm{A}}} = \frac{V_{\mathrm{out},0}}{(V_{\mathrm{in}} - V_{\mathrm{out},0})} \cdot \frac{(V_{\mathrm{in}} - V_{\mathrm{out},1})}{V_{\mathrm{out},1}} \approx 3. \tag{5.17}$$

By additionally using geometry data, absolute values $C_{\mathrm{A}} \approx 3.8\,\mathrm{pF}$ and $C_{\mathrm{B}} \approx 1.3\,\mathrm{pF}$ can be calculated, too. These values correspond to a dielectric constant of approximately 23. For comparison, a measurement for an initial CRS cell (HRS/HRS) was conducted for TiO_2-based cells. The result is in accordance with an analytical calculation of the serially connected capacitors C_{A} and C_{B}:

$$C_{\mathrm{cell}} = \frac{C_{\mathrm{A}} C_{\mathrm{B}}}{C_{\mathrm{A}} + C_{\mathrm{B}}} = 0.95\,\mathrm{pF}. \tag{5.18}$$

From evaluated resistance and capacitance values, a SPICE simulation was conducted, fitting well to measurement results (dashed lines in Fig. 5.12). In Fig. 5.12b the same measurements were carried out for $Cu/SiO_2/Pt$-based CRS cells. The normalized voltage margin was 2.4% and $C_{\mathrm{A}} \approx 0.9\,\mathrm{pF}$ as well as $C_{\mathrm{B}} \approx 0.3\,\mathrm{pF}$ resulted for a dielectric constant of 5.5. Measurements show that the voltage margin for SiO_2 is much smaller than for TiO_2. This is due to a greater mismatch between

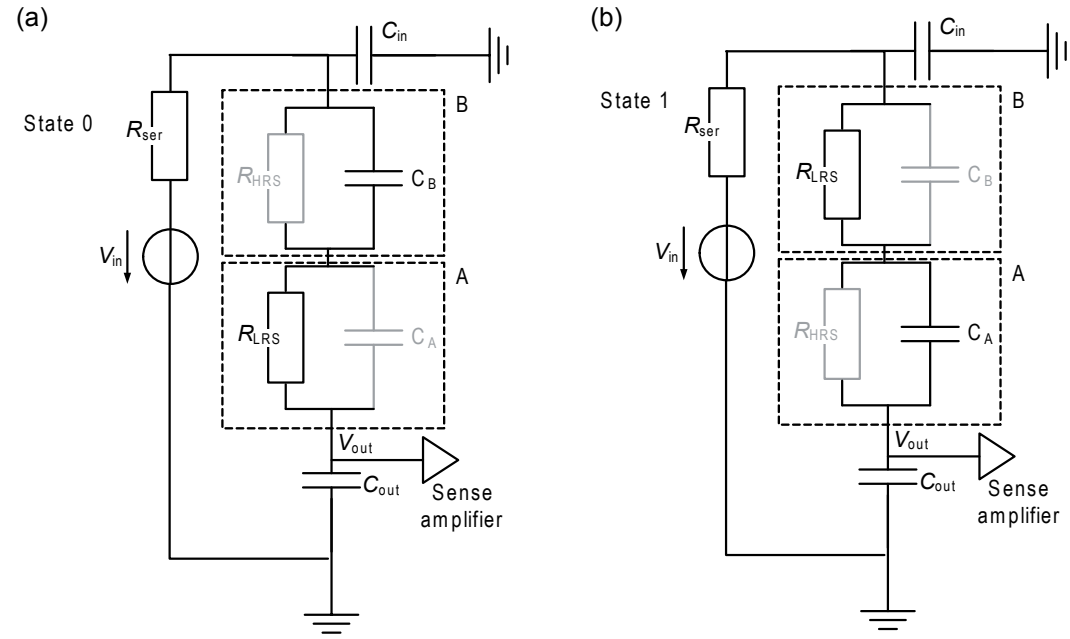


Figure 5.11: Equivalent circuit of a CRS cell in state '0' (a) and '1' (b). Adapted from [112].

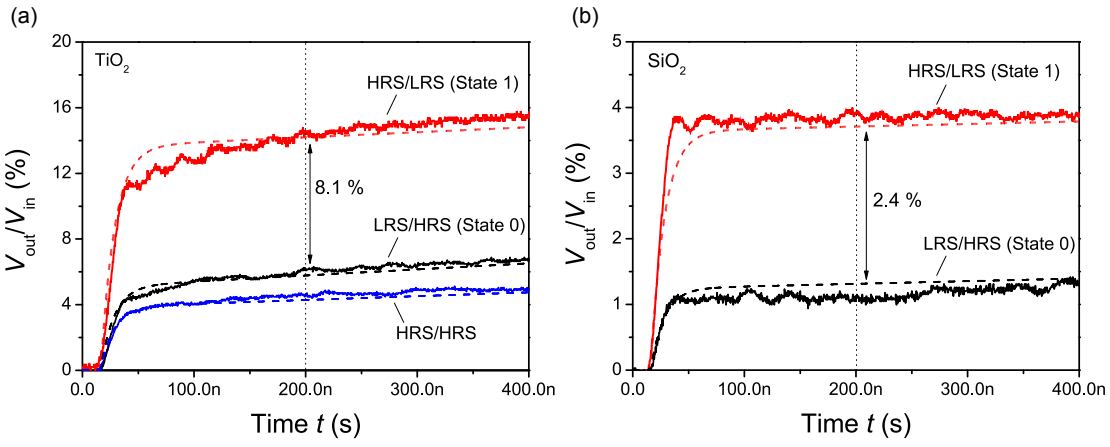


Figure 5.12: Capacitive measurements of (a) Cu/TiO_2/Pt-based and (b) SiO_2-based CRS cells in the modified parallel layout. Adapted from [112].

device capacitance and C_{out}. The optimum capacitor $C_{\mathrm{out,opt}}$ can be found by maximizing the (normalized) voltage margin, which is generally

$$\frac{\Delta V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{C_{\mathrm{max}}}{C_{\mathrm{max}} + C_{\mathrm{out}}} - \frac{C_{\mathrm{min}}}{C_{\mathrm{min}} + C_{\mathrm{out}}} \tag{5.19}$$

The optimum $C_{\mathrm{out,opt}}$ for a given $C_{\mathrm{max}} = C_{\mathrm{A}}$ and $C_{\mathrm{min}} = C_{\mathrm{B}}$ is

$$C_{\mathrm{out,opt}} = \sqrt{C_{\mathrm{A}} C_{\mathrm{B}}} \tag{5.20}$$

By replacing C_{out} with $C_{\mathrm{out,opt}}$ in equation (5.19), the biggest achievable normalized voltage margin results:

$$\left[\frac{\Delta V_{\mathrm{out}}}{V_{\mathrm{in}}}\right]_{\mathrm{max}} = \frac{1}{1 + \sqrt{\frac{C_{\mathrm{min}}}{C_{\mathrm{max}}}}} - \frac{1}{1 + \sqrt{\frac{C_{\mathrm{max}}}{C_{\mathrm{min}}}}}. \tag{5.21}$$

For a capacitance ratio of three to one, the optimum value is 26.8%, which is why the results in Fig. 5.12 could be improved for a matched $C_{\mathrm{out,opt}}$.
So far only single CRS cells were considered. Since CRS cells are intended to be used in passive crossbar arrays, the readout constraints for the crossbar array size must be derived. Fig. 5.13a shows a CRS crossbar array with a capacitive readout scheme. Non-accessed lines are grounded, while the accessed row is connected to the input voltage V_{in}, and the accessed column is connected to the series capacitor C_{out}. All capacitances of the accessed column add up to C_{out} (comprises constant bit line capacitance), while all capacitances in the accessed row add up to C_{in} (comprises constant word line capacitance), hence readout is very similar to the reading of a single CRS cell described above. The normalized voltage margin for the worst-case of a m x m array is

$$\frac{\Delta V_{\mathrm{out,worst\_case}}}{V_{\mathrm{in}}} = \frac{C_{\mathrm{max}}}{m \cdot C_{\mathrm{max}} + C_{\mathrm{out}}} - \frac{C_{\mathrm{min}}}{m \cdot C_{\mathrm{min}} + C_{\mathrm{out}}}. \tag{5.22}$$

With this, the optimum C_{out} is

$$C_{\mathrm{out,opt}} = m \cdot \sqrt{C_{\mathrm{min}} C_{\mathrm{max}}}. \tag{5.23}$$

Hence, the achievable normalized voltage margin for the worst-case is

$$\left[\frac{\Delta V_{\mathrm{out}}}{V_{\mathrm{in}}}\right]_{\mathrm{max}} = \frac{1}{m + m \cdot \sqrt{\frac{C_{\mathrm{min}}}{C_{\mathrm{max}}}}} - \frac{1}{m + m \cdot \sqrt{\frac{C_{\mathrm{max}}}{C_{\mathrm{min}}}}}. \tag{5.24}$$

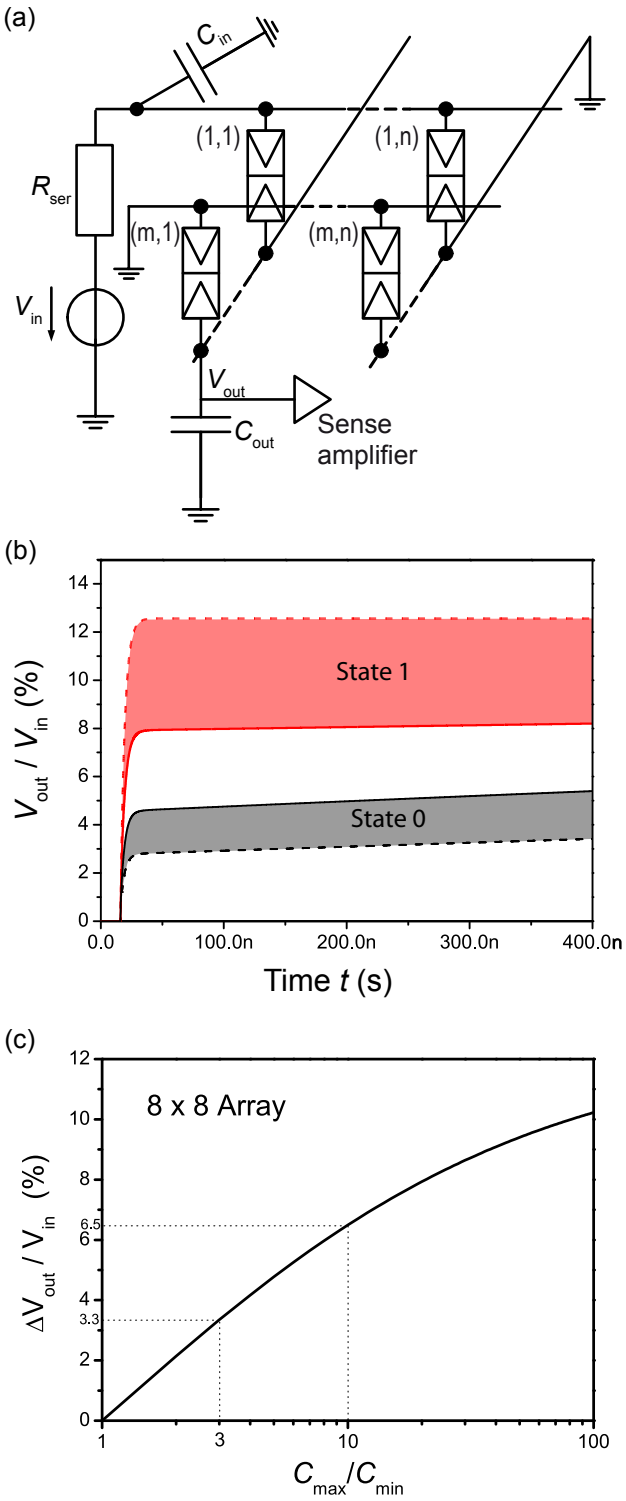


Figure 5.13: (a) Equivalent circuit of crossbar array and capacitive readout scheme.(b) Simulation of a 8 x 8 array of TiO_2 cells. (c) Influence of capacitance ratio on normalized voltage margin for an 8 x 8 array. Adapted from [112].

In Fig. 5.13b the data taken from TiO_2 cells is used to simulate an 8 x 8 array. C_{out} equals 17.5 pF and the normalized voltage margin is 3.3%. The possible voltage levels for reading a '1' are situated between the red straight and dashed line and the voltages for reading a '0' are located between the black straight and dashed line. Possible levels in between are shaded. Note that for memory arrays with higher element number, the voltage margin is decreased significantly. This property is very similar to the current sneak path problem which is present in BRS crossbar arrays (compare section 5.3) and therefore, this capacitive non-destructive readout scheme is only applicable for small to medium sized passive memory arrays. However, by increasing the capacitance ratio the achievable normalized voltage margin can be increased. For a ratio of ten to one, for example, a normalized voltage margin of 6.5% is achievable (see Fig. 5.13c). This capacitance ratio is still easily achievable at the minimum feature size in common semiconductor fabrication using the same material system for both elements but different thickness of the insulator (e.g., 5 nm vs. 50 nm). Larger differences in capacitances the increase voltage margins, but nevertheless, the preparation of a fast sense amplifier with a desirable small input capacity as well as high input resistance optimized for a small voltage margin is challenging.

5.4.2 Non-Destructive Read for VCM-based CRS Cells

For VCM-based CRS cells a different non-destructive readout method is feasible. If there is an asymmetry in HRS with respect to the origin of the I-V characteristic (Fig. 5.14a), this asymmetry is also present in the CRS configuration (Fig. 5.14b). Fig. 5.14a shows that for a given voltage, the current flow in HRS depends on the sign of voltage. Since a CRS characteristic is dominated by the high-resistive element, the asymmetry is observed in Fig. 5.14b as well. This property can be used for a non-destructive readout at a read voltage V_{read} which is below the first threshold voltage $V_{th,1}$. Because either the positive HRS branch (state '0', larger current) or the negative HRS (state '1', smaller current) is dominating the CRS, a current level detection reveals the correct state.
Note that in a crossbar array, this property comes with drawbacks. Because states '0' and '1' are distinguishable, a pattern dependency is present, just as in pure BRS crossbar arrays. In consequence, compared to using a destructive readout scheme, the feasible maximum crossbar array size is smaller if this non-destructive readout scheme is applied.

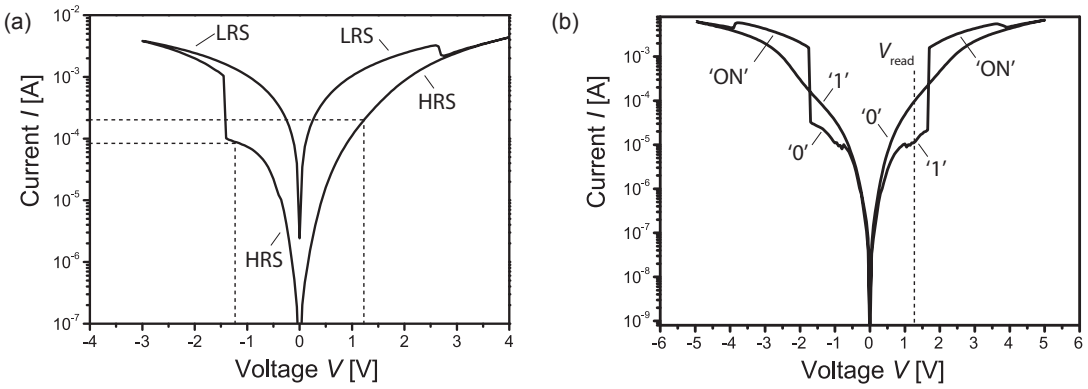


Figure 5.14: Asymmetry of HRS in VCM elements. (b) Non-destructive readout for VCM-based CRS cells.

5.5 Conclusion

In this chapter, the basic write and read operations for CRS-based passive crossbar arrays were shown. Especially the read operations level read and spike read, which are needed for CRS, were introduced and verified by pulse measurement experiments. Asymmetric ECM elements were shown to be promising elements for building CRS cells with larger safety margins than those of symmetric BRS elements. Possible voltage schemes for a crossbar array design were discussed. The major advantage of a CRS cell compared to a single BRS element is the prevention of sneak paths and, therefore, the feasibility of large passive crossbar arrays as shown in a detailed comparison of BRS- and CRS-based crossbar arrays. Finally, two possibilities of a non-destructive readout, one capacitive and one based on HRS asymmetry in VCM elements, were introduced, lowering the requirements for high endurance cells, but decreasing the possible array size significantly. In consequence, a non-destructive readout is required when large passive crossbar arrays are to be applied.
In summary, CRS-based arrays solve the sneak path problem, since all CRS always exhibit the same high resistance independent of the stored binary information. It is associated with a drastic reduction of the static power consumption and makes the application of large passive crossbar array memory architectures feasible.

6 Complementary Resistive Switches - Logic Applications

In literature, most logic concepts use resistive switches as programmable interconnects, e.g., CMOL [75] or FPNI [81] (compare section 2.8). Due to the fact that CRS cells are always high-resistive, any logic approach requiring programmed (low-resistive) cells is not feasible with CRS cells, which is why different approaches must be selected.
Since CRS cells are favorable devices for high-density passive crossbar memory arrays, every logic concept that requires high-density memories is a possible field of use for CRS-based crossbar arrays. As such, it is straight forward to suggest CRS-based arrays for LUTs in FPGA logic blocks. But, since look-up tables in conventional FPGA design approaches are small, CMOS overhead would be large [77]. In contrast, for the memory-based computing approach [84, 85], which is an alternative FPGA approach requiring large arrays, large scale CRS-based arrays are a promising candidate for realizing this alternative FPGA approach (compare also section 2.8).
A new approach for logic implementations with resistive switches was suggested in [86], focusing on the implication (IMP) property. In general, the implication p IMP q, which is also called material implication or material conditional, is true for any value of p and q except for $p =$ '1' and $q =$ '0'. In [86] three elements, two BRS and a load resistor, are used to form an IMP operation (see 2.8 for details). In section 6.1.1, by understanding a single BRS as a Moore machine, the number of elements needed for IMP is reduced to one, but due to the lack of crossbar array compatibility, BRS-based logic is still limited.
In section 6.1.2 it will be shown that the IMP property is also available for CRS cells by considering CRS cells as Mealy machines. By introducing a special readout scheme, CRS Moore logic is feasible, too, implementing 14 out of 16 possible logic functions with a single CRS cell. For an arbitrary logic functionality, a stacked or folded CRS concept is suggested in section 6.3, realizing all 16 logic functions in $4F^2$ with two CRS devices. By considering CRS cells as state machines, logic operations can be conducted in crossbar memory, storing the calculation result directly to the

memory. Since memory and logic operations can be performed in the same crossbar array, a new reconfigurable computer architecture is feasible.

6.1 BRS and CRS - Basic State Machines for Logic Operations

Each BRS as well as CRS can be considered as an atomic unit for logic operations. In case of the BRS, a consideration as Moore machine (see section 6.1.1) is evident, while in case of the CRS, the essential functionality can best be described by means of a Mealy machine (see section 6.1.2) [109].

6.1.1 BRS Moore Logic

The idea to use BRS for implication functionality was suggested in [86]. There, two BRSs and a resistor are needed (see section 2.8 for details). In [109] it was shown that a single BRS is sufficient for IMP functionality. A BRS is considered a two-state device. For the BRS, the first state ($Z =$ '0', LRS) is marked by an orange cube, while the second state ($Z =$ '1', HRS) is marked by a yellow cube (see Fig. 6.1a).
The IMP operation for a bipolar resistive switch can be divided into three steps (Fig. 6.1c). In the first step, the BRS must be initialized to state $Z' =$ '1' (HRS). This is necessary since the logical operation depends on the previous device state Z'. In step two, the logic variables p and q are applied to terminal 1 (T_1) and terminal 2 (T_2), respectively. If the variables p and q are at the same potential - either '0' (low potential) or '1' (high potential) -, no potential difference V exists across the devices and thus the device state remains unchanged, which results in $Z =$ '1' (HRS). The same is true when T_2 (variable q) is set to a high potential and T_1 (variable p) is set to a low voltage level. The bipolar resistive switch remains at the initial state ($Z =$ '1'), since this polarity of the voltage drop does not change the state of the device. However, if p is logic '1' and q is logic '0', a voltage drop across the device is present, with a polarity that induces a change in the state of the switch. Due to this operation, the resistive switch ends up in state $Z =$ '0' (LRS), completing the truth table of the IMP operation (Fig. 6.1b):

$$Z = p \text{ IMP } q \tag{6.1}$$

The actual readout is conducted by a small read voltage (level read) after this logic operation.
To clarify this behavior, the bipolar resistive switch can be considered as a Moore

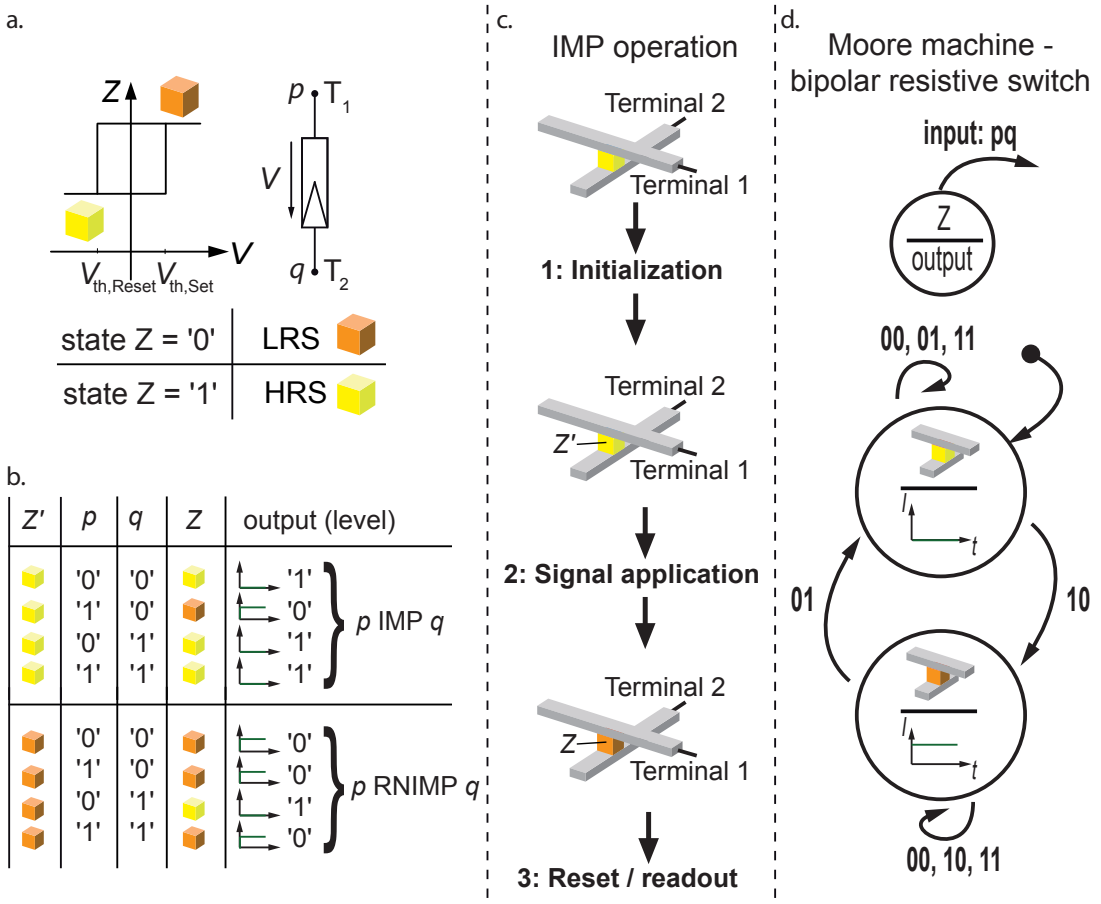


Figure 6.1: (a) BRS with terminals T_1 and T_2. Input signal p is applied to T_1 and q is applied to T_2. The resistive state $Z =$ '0' (orange cube) corresponds to the LRS, and $Z =$ '1' (yellow cube) corresponds to the HRS. The output is defined by the current level. (b) Truth table for BRS IMP and RNIMP operation. (c)Three steps of the logic IMP operation. (d) Moore machine representation of a BRS. Adapted from [109].

machine (Fig. 6.1d) [113, 114]. The state variable Z is retained and the transitions are labeled with the input variables p and q. For state $Z =$ '1' (HRS) a low-current output level ('1') and for state $Z =$ '0' (LRS) a high-current output level ('0') is assigned. From Fig. 6.1d, it can be concluded that the negation of the implication (NIMP) for reversed signals p and q can also be conducted by initializing the switch to $Z' =$ '0'.

$$Z = q \text{ NIMP } p = p \text{ RNIMP } q \tag{6.2}$$

In general, a reset step (step three) is needed before a new logic operation can be started. Since BRS are low-resistive in state $Z =$ '0', logic applications in crossbar arrays are difficult to realize due to high resulting currents. Thus, an application is limited to small arrays (compare section 5.3).

6.1.2 CRS Mealy Logic

CRS cells can also be used for logic operations by considering them as two-state devices. Similar to the BRS consideration, the first state (HRS/LRS) is marked by a red cube while the second state (LRS/HRS) is marked by a blue cube (Fig. 6.2a). Note that a CRS is indeed a two-state device for asymmetric BRS elements (see section 4.3.1).

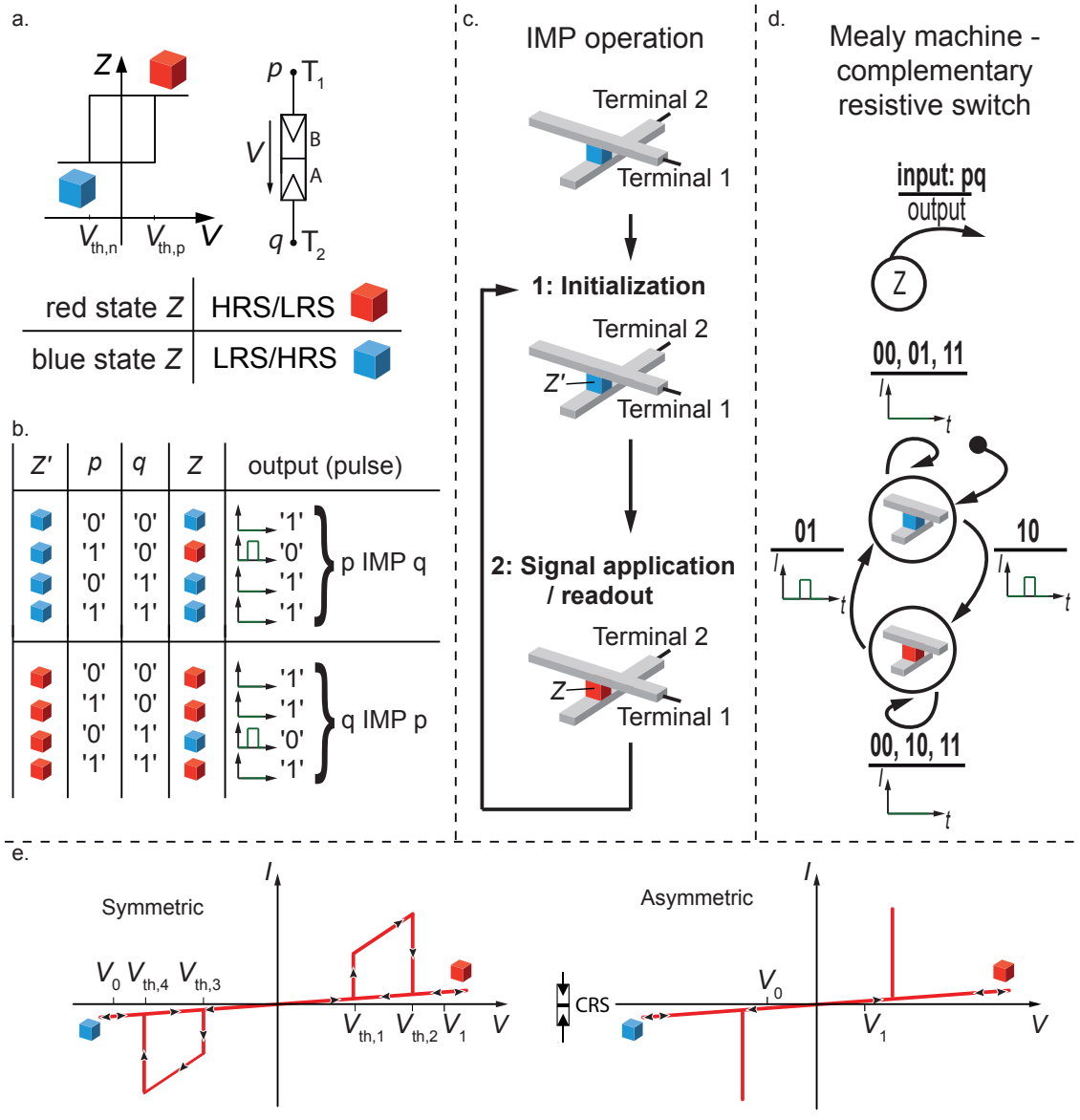


Figure 6.2: (a) CRS as a two-state device with HRS/LRS (red state) and LRS/HRS (blue state). (b) Truth table for transition-based IMP and RIMP operation. (c) Two steps of the logic IMP/RIMP operation. (d) Mealy machine representation of a CRS. The output current pulse occurs while in state transition, which is why no special readout is needed. Adapted from [109].

Additionally, CRS cells based on symmetric BRS elements can offer two-state behavior, too, if voltage levels leading to the LRS/LRS state ('ON' state) are avoided.
For CRS cells, the operational steps are similar to those of bipolar resistive switches (Fig. 6.2c), but no special readout step is needed. Please note that Z is not stored as LRS or HRS as shown for the BRS, but as a distinct combination of resistances. The potentials allowed for p and q, as well as the truth tables for IMP and RIMP, are depicted in 6.2b. No special readout cycle is needed here because the current pulse which occurs when switching the CRS cell can be used for readout (compare spike read in section 5.1.3). Because in this case the output is not only state-dependent, but also input-dependent, a CRS cell can be considered a Mealy machine (Fig. 6.2d) [114, 115]. The output is then assigned to the state transitions, where a current pulse indicates a '0' and the absence of a pulse indicates a '1' (Fig. 6.2b). From Fig. 6.2d we see that by selecting the HRS/LRS (red state) as initial state, an implication with reversed input variables (RIMP) results.
Note that for $V_0 = 0\,\mathrm{V}$ and $V_1 = V_{\mathrm{write}}$, a possible race condition for $p = q =$ '1' is present for symmetric CRS cells (compare Fig. 6.2e). For asymmetric BRSs (see section 4.3.1) race conditions can be avoided by selecting $V_0 = -0.5 \cdot V_{\mathrm{write}}$ and $V_1 = 0.5 \cdot V_{\mathrm{write}}$ (Fig. 6.2e). Note that, due to the transition-dependent logic evaluation, the actual CRS state Z does not correspond to the result of the logic operation. Thus, a direct information storage, as is the case for BRS Moore logic, is not available.
This disadvantage can be overcome (see section 6.2).

6.1.3 Experimental Proofs

Fig. 6.3 shows experimental results of a bipolar resistive switch IMP operation. All combinations of p and q are applied to a bipolar resistive switch ($Cu/SiO_2/Pt$) and the current flow is detected during the readout step.
In Fig. 6.3b, an experimental result of a CRS IMP gate based on electro-chemical metalization-type ($Cu/SiO_2/Pt$, [105]) resistive switches is shown. In this case, the switching time was $< 200\ \mu$s.
All combinations of p and q are applied to a CRS in Fig. 6.3b and the current is monitored. It should be noted that the overall resistance of the CRS is high in all Z states. Thus, no sneak paths exists for CRS-based arrays and with this, logic operations in large arrays are feasible (compare section 5.3).

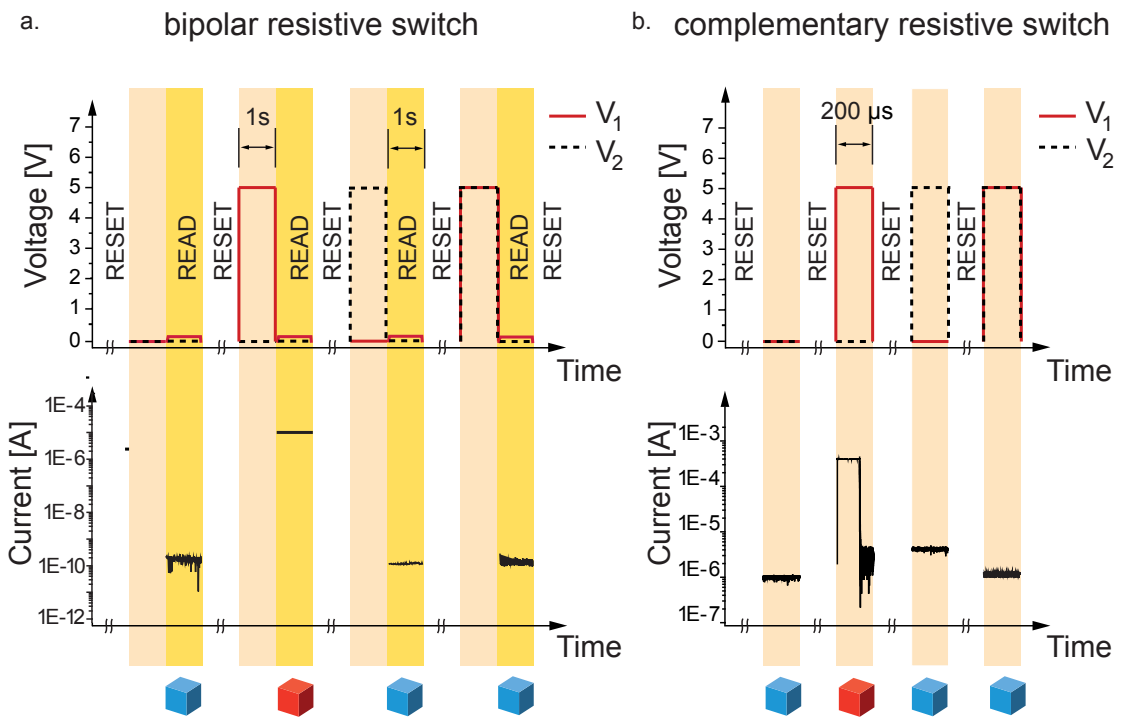


Figure 6.3: a. Measurement of a bipolar resistive switch performing a logical IMP operation. b. Measurement of a CRS performing logical IMP operation. Adapted from [109].

6.2 CRS Moore Logic

In section 6.1.2 the inherent Mealy machine functionality of CRS was shown. With the use of additional read operations, a CRS can be transfered to Moore machine representations, enabling direct storage of results. In section 6.2.1 a three-state approach for symmetric CRS cells is presented, while in section 6.2.2 a two-state approach for asymmetric CRS cells is shown.

6.2.1 Three-State CRS Moore Logic

In section 6.1.2, voltages of $V_0 = -0.5 \cdot V_{\text{write}}$ and $V_1 = 0.5 \cdot V_{\text{write}}$ were selected as logic input. For a three-state Moore machine implementation, $V_0 = -0.5 \cdot (V_{\text{th},1} + V_{\text{th},2})$ and $V_0 = 0.5 \cdot (V_{\text{th},1} + V_{\text{th},2})$ are used, realizing the same logic functions, IMP and RIMP, but assigning both HRS/LRS as well as LRS/HRS to $Z =$ '1' and LRS/LRS to $Z =$ '0' (Fig. 6.4a). The LRS/LRS (green cube) acts like a third state, as depicted in Fig. 6.4b. Since the voltages V_0 and V_1 (Fig. 6.4c) are smaller than the first threshold voltage $V_{\text{th},1}$, no switching can occur for only one signal applied, but

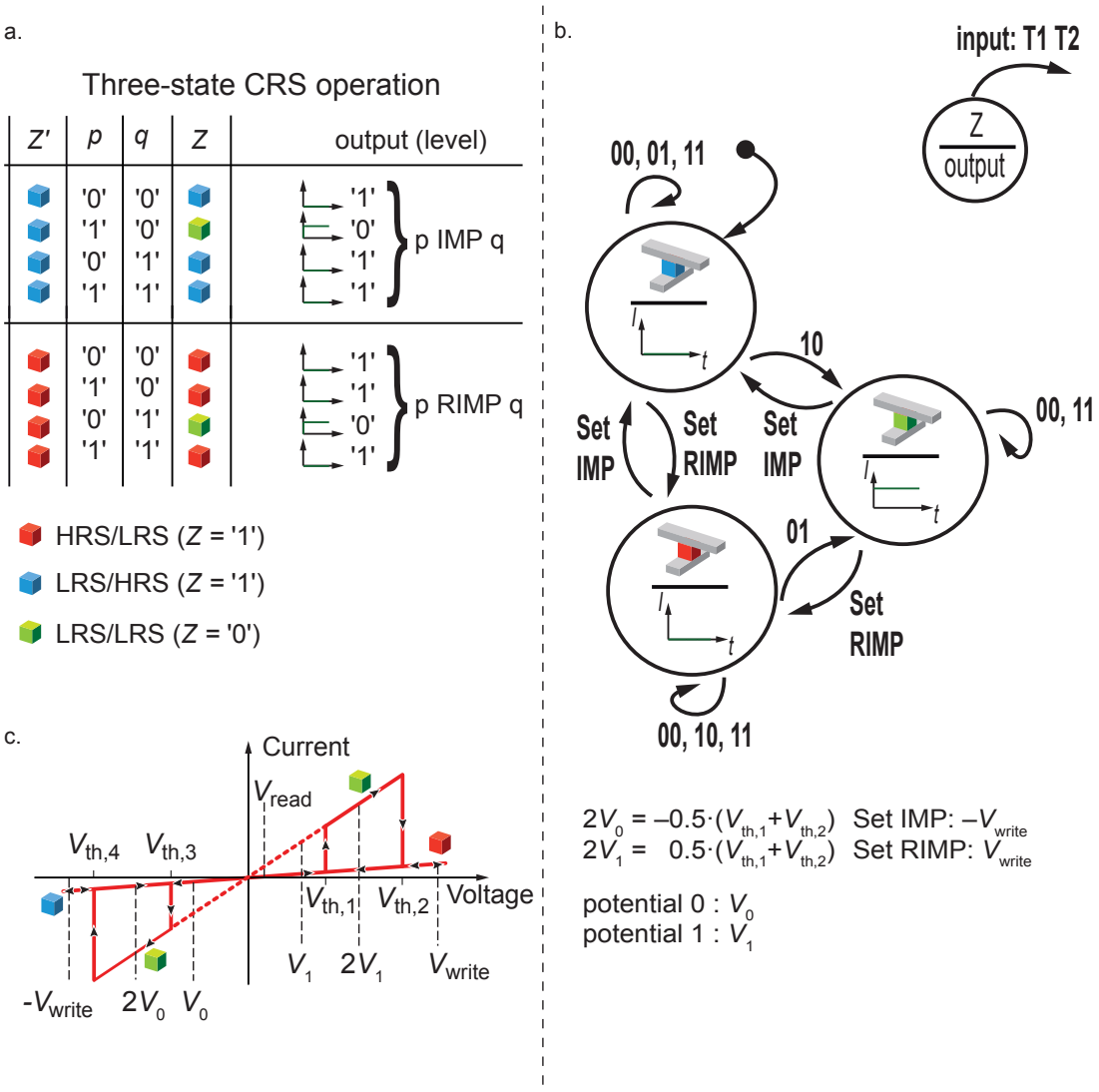


Figure 6.4: (a) Truth table for three-state CRS Moore logic realizing IMP and RIMP operation. (b) Moore machine representing the CRS cell. (c) Visualization of applied voltages.

with $V = |V_0| + |V_1|$, switching to LRS/LRS can occur. Only symmetric CRS or asymmetric CRS permanently connected to a series resistor can be used for this approach (see Fig. 6.4c) and an additional write voltage V_{write} is needed. With the negative write voltage $-V_{\text{write}}$ applied to the CRS, it is set as implication (set IMP), whereas with a positive write voltage V_{write} applied, the CRS is set as reverse implication (set RIMP).

After initialization to LRS/HRS or HRS/LRS, the logical variable p is applied to terminal T_1 and q is applied to terminal T_2, or vice versa. In contrast to the previous operation, the CRS is switched to the stable LRS/LRS state instead of

switching from one high-ohmic state to the other. Starting from state LRS/HRS (blue cube) the CRS is only switched to LRS/LRS for $p =$ '1' and $q =$ '0', whereas when starting from HRS/LRS (red cube) the CRS is only switched to LRS/LRS for $p =$ '0' and $q =$ '1'.
Since a Moore machine is assumed, the read operation is an independent step after the application of logic variables. A current level can be detected at a small read voltage V_{read}, as is the case with single BRS elements (compare section 6.1.1). After the readout, a set - either to LRS/HRS (set IMP) or HRS/LRS (set RIMP) - is performed and the next operation can be started.
A general disadvantage of this approach is the presence of the LRS/LRS state after the logic operation as a final state, which will lead to a sneak path in crossbar array applications, rendering this approach non-preferable for crossbar array applications.

6.2.2 Two-State CRS Moore Logic

By use of asymmetric CRS cells with a separated read cycle, the disadvantages of Mealy CRS logic as well as three-state CRS Moore logic can be avoided: By adding an additional readout step, multi cycle operations can be performed, allowing for a larger set of logic operations. Additionally, due to the separation of logic operation and readout, the result is directly stored in one of the high-resistive CRS states, allowing readout at any time after the logic operation.
In Fig. 6.5a the CRS state machine which is present for the logic operation is depicted. The functionality is exactly the same as for the Mealy representation (see Fig. 6.2d), but current pulses occurring during state transitions are ignored. Logic input voltages are '0' $= V_0 = -0.5 \cdot V_{\mathrm{write}}$ and '1' $= V_1 = 0.5 \cdot V_{\mathrm{write}}$, and possible states are either LRS/HRS (blue cube) or HRS/LRS (red cube). Since both states are indistinguishable in terms of resistance, a special readout step is required to read the actual state. Asymmetric CRS cells (compare section 4.3.1) are assumed, enabling a spike read (compare section 5.1.3) as well as a level read (compare section 5.1.2 and Fig. 6.5b).
For a level read, a series resistor (marked by dots in Fig. 6.5c) is needed in the sensing circuit leading to a stable LRS/LRS (green cube) state instead of a current pulse, as is the case with the spike read. As shown in Fig. 6.5c, there are two possible read operations which can be applied, either reading with positive voltage ($T_1 =$ '1' and $T_2 =$ '0', called 'read 10', green background) or negative voltage ($T_1 =$ '0' and $T_2 =$ '1', called 'read 01', gray background). For read 10, the blue cube is assigned to $Z =$ '0' and the red cube to $Z =$ '1', while for read 01, the blue cube is assigned to $Z =$ '1' and the red cube to $Z =$ '0'. Below, read 10 is selected

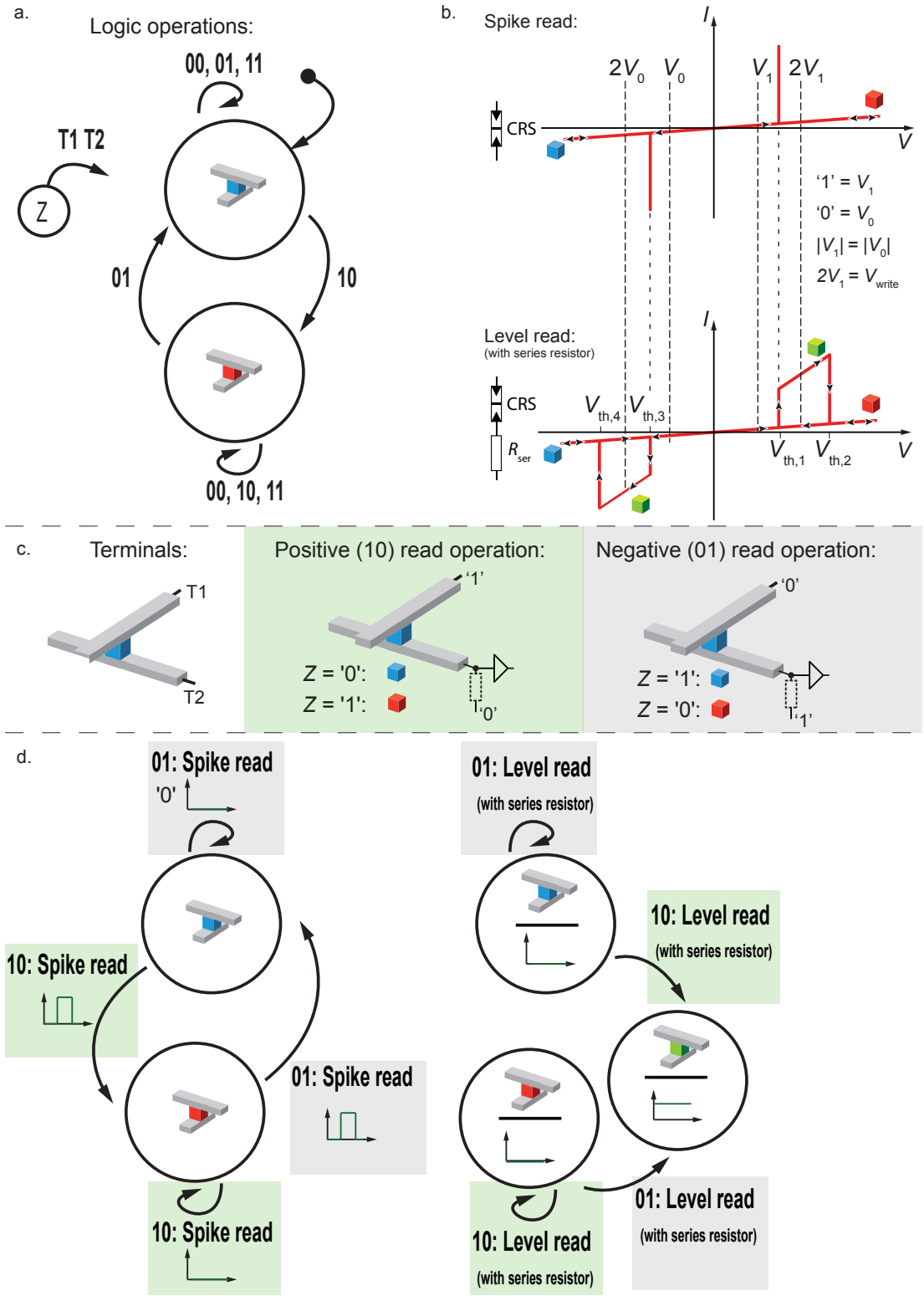


Figure 6.5: (a) State machine for logic operation (b) Two possible read schemes (c) Terminal configuration for read 10 (green background) and read 01 (gray background). (d) State machines for spike read and level read, respectively, showing read 10 as well as read 01.

(read 01 is used in combination with read 10 in folded CRS Moore logic only, see section 6.3.2). In Fig. 6.5d, the spike read as well as the level read are depicted in terms of state machines for read 10 as well as read 01. Since spike and level readout methods lead to the same result, both methods are discussed jointly in the next paragraph.
The basic logic operation which is performed by the CRS in read 10 mode is defined by the following equation (compare Fig. 6.6a):

$$Z = (T_1 \text{ RIMP } T_2) \cdot Z' + (T_1 \text{ NIMP } T_2) \cdot (\text{not } Z'). \tag{6.3}$$

For read 01 mode, which is not used here, following equation holds true (Fig. 6.6a):

$$Z = (T_1 \text{ IMP } T_2) \cdot Z' + (T_1 \text{ RNIMP } T_2) \cdot (\text{not } Z'). \tag{6.4}$$

Since the logic operation depends on the previous state Z', a stateful logic is possible. In general, a defined initial state Z' is needed for any logic operation; thus, the first logic operations needed are FALSE and TRUE, which must always be performed in a first cycle. With FALSE ($T_1 =$ '0' and $T_2 =$ '1') the CRS is set to $Z =$ '0' (blue cube), while with TRUE ($T_1 =$ '1' and $T_2 =$ '0') the CRS is set to $Z =$ '1' (red cube):

$$Z = \text{TRUE} = (\text{'1' RIMP '0'}) \cdot Z' + (\text{'1' NIMP '0'}) \cdot (\text{not } Z') = \text{'1'} \tag{6.5}$$

$$Z = \text{FALSE} = (\text{'0' RIMP '1'}) \cdot Z' + (\text{'0' NIMP '1'}) \cdot (\text{not } Z') = \text{'0'} \tag{6.6}$$

The pin assignment for T_1 and T_2 as well as the logic table of TRUE and FALSE are depicted in Fig. 6.6b.
With equation (6.3) and either TRUE or FALSE in the first cycle, the implication-based operations can be implemented (Fig. 6.6b):

$$Z = p \text{ IMP } q = (q \text{ RIMP } p) \cdot (Z' = \text{'1'}) \tag{6.7}$$

$$Z = p \text{ NIMP } q = (p \text{ NIMP } q) \cdot (\text{not } Z' = \text{'0'}) \tag{6.8}$$

$$Z = p \text{ RIMP } q = (p \text{ RIMP } q) \cdot (Z' = \text{'1'}) \tag{6.9}$$

$$Z = p \text{ RNIMP } q = (q \text{ NIMP } p) \cdot (\text{not } Z' = \text{'0'}) \tag{6.10}$$

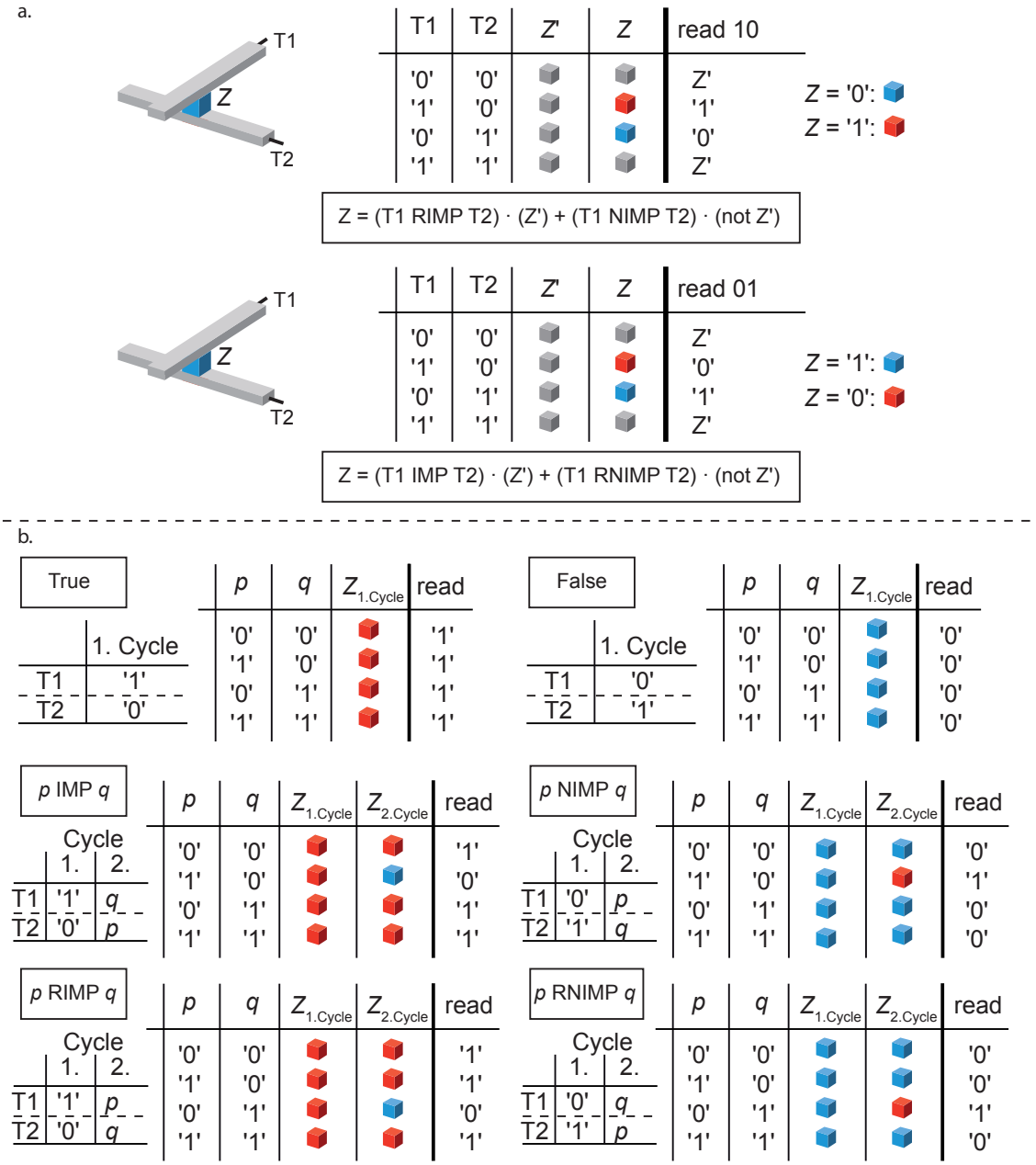


Figure 6.6: (a) Comparison of 10 read and 01 read. (b) Logic operations with CRS I.

Note that with TRUE ($Z' = 1$) the operation for the next cycle is set to RIMP, while with FALSE ($Z' = 0$) the operation for the next cycle is set to NIMP.
Four other operations are possible in two cycles as well (Fig. 6.7):

$$Z = p = (p \text{ RIMP } \text{`1`}) \cdot \text{`1`} \tag{6.11}$$

$$Z = \text{not } p = (\text{`1`} \text{ NIMP } p) \cdot (\text{not } \text{`0`}) \tag{6.12}$$

$$Z = q = (q \text{ RIMP } \text{`1`}) \cdot \text{`1`} \tag{6.13}$$

$$Z = \text{not } q = (\text{`1`} \text{ NIMP } p) \cdot (\text{ not } \text{`0`}) \tag{6.14}$$

With a third cycle (Fig. 6.7), OR, NAND, NOR and AND can be realized, too:

$$Z = p \text{ OR } q = (q \text{ RIMP } \text{`0`}) \cdot p + (q \text{ NIMP } \text{`0`}) \cdot (\text{not } p) \tag{6.15}$$

$$Z = p \text{ NAND } q = (\text{`1`} \text{ RIMP } p) \cdot (\text{not } q) + (\text{`1`} \text{ NIMP } p) \cdot q \tag{6.16}$$

$$Z = p \text{ NOR } q = (\text{`0`} \text{ RIMP } p) \cdot (\text{not } q) + (\text{`0`} \text{ NIMP } p) \cdot q \tag{6.17}$$

$$Z = p \text{ AND } q = (q \text{ RIMP } \text{`1`}) \cdot p + (q \text{ NIMP } \text{`1`}) \cdot (\text{not } p) \tag{6.18}$$

Since no low-ohmic state (LRS/LRS) is present in any step (apart from the reading process), this procedure is the most favorable crossbar array implementation. But there are two functions which cannot be realized with a single CRS: XOR and XNOR. This can be understood by having a closer look at equation (6.3). A combination of NIMP and RNIMP after a FALSE operation would lead to XOR, but since the whole equation (6.3) must be considered in a third cycle, no XOR functionality results.

$$Z_{1.\text{cycle}} = \text{FALSE} \tag{6.19}$$

$$Z_{2.\text{cycle}} = (p \text{ NIMP } q) \tag{6.20}$$

$$Z_{3.\text{cycle}} = (q \text{ RIMP } p) \cdot (p \text{ NIMP } q) + (q \text{ NIMP } p) \cdot (\text{not } (p \text{ NIMP } q)) \tag{6.21}$$

$$Z_{3.\text{cycle}} = (p \text{ RNIMP } q) \neq (p \text{ XOR } q) \tag{6.22}$$

In the case of, $p =$ ‘1‘ and $q =$ ‘0‘, a back-switching to $Z =$ ‘0‘ occurs in the third cycle preventing a XOR operation. Due to this property, no function in need of switching if $p \neq q$ can be implemented. To realize a device which is capable of performing all 16 boolean functions, a two-CRS ’folded’ configuration is required (see section 6.3).

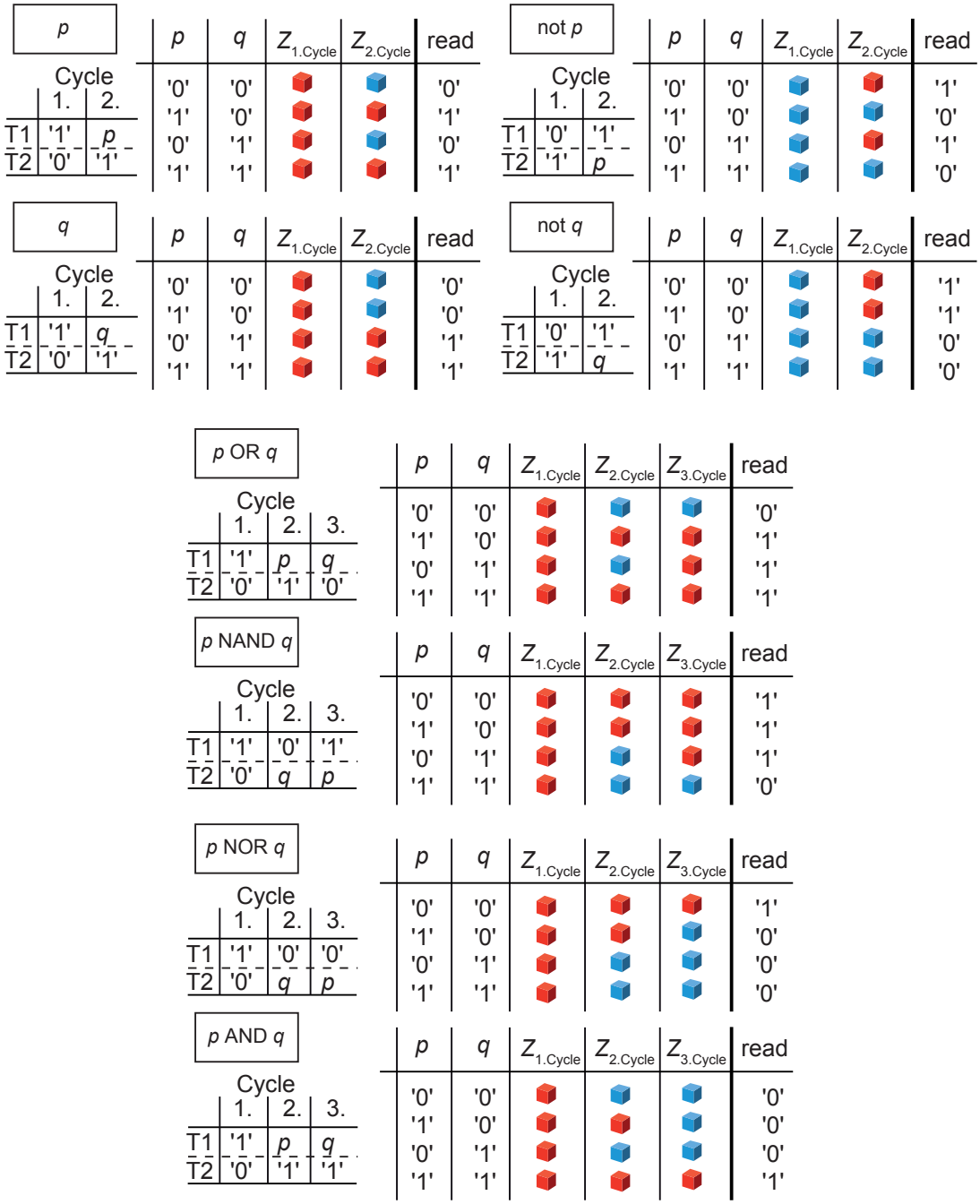


Figure 6.7: Logic operations with CRS II.

6.3 Folded CRS Logic

A folded crossbar structure consists of two crossbar arrays folded to a five-layer structure, consisting of the top electrode bars (terminal T_1), the first CRS cell, the orthogonal electrode bars (terminal T_3) in the middle, the second CRS cell and the bottom electrode bars (terminal T_2) which are parallel oriented towards the top electrode bars (see Fig. 6.8a).
Below, the combination of two stacked CRS cells is considered to be the basic unit for the logic operation. Note that the functionalities exist on the same footprint area as in case of single CRS cells.
The basic idea behind using two CRS cells connected to a common (middle) electrode is to build a wired AND ('&') connection. Thereby, the variety of realizable logic functions can be increased for the transition-based CRS Mealy logic as well as for the state-based CRS Moore logic. For the CRS Moore logic, all 16 two-input boolean logic functions can be realized.

6.3.1 Folded CRS Mealy Logic

The CRS Mealy logic is transition-based, which is why there is only one cycle present for the logic operation. By using two CRS cells, NOR, AND and XNOR can be implemented (Fig. 6.8).
The actual logic function depends on the initialization process where, in a first step, the two CRS cells are reset to state HRS/LRS (red cube) and LRS/HRS (blue cube), depending on the application.
For the NOR operation, in the first step, the top CRS is set to LRS/HRS and the bottom CRS is set to HRS/LRS. The signals p and q are applied to terminal T_1 and terminal T_2, while terminal T_3 is kept at '0' in the second step, and the output current spike is detected (Fig. 6.8a). In Fig. 6.8b the truth table of the NOR operation is shown, realizing

$$p \text{ NOR } q = p \text{ IMP } \text{`0`} \ \& \ \text{`0`} \text{ RIMP } q \tag{6.23}$$

(compare Fig. 6.2b). The wired AND is marked by ("&") in equation (6.23). Note: since both CRS cells switch for $p =$ '1' and $q =$ '1', a larger current pulse will result in this case.
The AND functionality results from initializing the top switch to HRS/LRS and

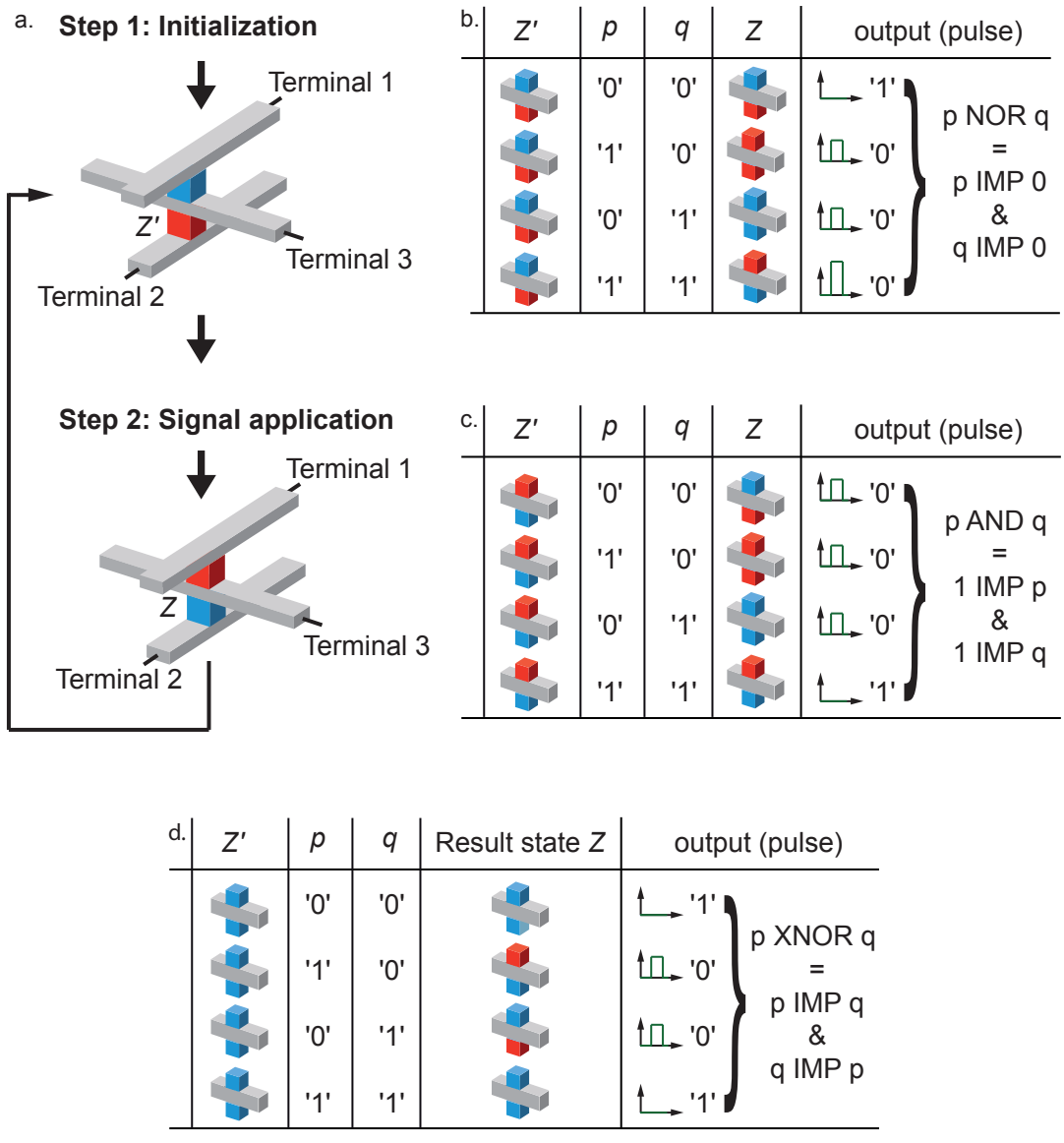


Figure 6.8: (a) Two-step CRS Mealy logic in folded crossbars. (b) NOR realization. (c) AND realization. (d) XNOR realization. Adapted from [109].

the bottom switch to LRS/HRS and applying p to terminal T_1, q to terminal T_2 and '1' to terminal T_3 (Fig. 6.8c):

$$p \text{ AND } q = p \text{ RIMP } \text{`1`} \ \& \ \text{`1`} \text{ IMP } q \tag{6.24}$$

For XNOR functionality, both CRSs are set to LRS/HRS, initially. p is applied to terminal T_1 and terminal T_3 while q is applied to terminal T_2. Note that the same functionality results if both CRSs are set to HRS/LRS (Fig. 6.8d):

$$p \text{ XNOR } q = p \text{ IMP } q \ \& \ q \text{ IMP } p \tag{6.25}$$

With a folded crossbar design, commonly used boolean functions can be implemented, making this structure attractive for crossbar array operations with a low number of cycles.

6.3.2 Folded CRS Moore Logic

In the two-state CRS Moore logic (compare section 6.2.2), neither XNOR nor XOR could be realized. With two stacked CRS cells, arbitrary logic functions can be performed, since all 16 logic functions are feasible. The readout used is a combination of 10 read and 01 read (Fig. 6.6a), since '1' is applied to terminal T_1 and T_2, implementing 10 read for the top CRS cell and 01 read for the bottom CRS cell (Fig. 6.9a). The basic functions are:

$$Z_{\text{top}} = (T_1 \text{ RIMP } T_3) \cdot Z'_{\text{top}} + (T_1 \text{ NIMP } T_3) \cdot (\text{not } Z'_{\text{top}}) \tag{6.26}$$

$$Z_{\text{bottom}} = (T_2 \text{ IMP } T_3) \cdot Z'_{\text{bottom}} + (T_2 \text{ RNIMP } T_3) \cdot (\text{not } Z'_{\text{bottom}}) \tag{6.27}$$

$$Z = Z_{\text{top}} \ \& \ (\text{not } Z_{\text{bottom}}) \tag{6.28}$$

The top cell (equation (6.26)) and bottom cell (equation (6.27)) can be manipulated independently, but are jointly evaluated at the readout (equation (6.28)). Depending on whether or not a series resistor is selected for read, a level readout as well as a spike readout is feasible.

Due to the wired '&'-connection, there are three combinations representing a logical '0' (blue background) and one representing a logical '1' (yellow background) (compare Fig. 6.9b).

Note that the states blue/blue and red/red representing '0' are put in parentheses, since they only occur for the XNOR and XOR operation and are not needed for any other operations. Since all operations start with TRUE or FALSE in the first

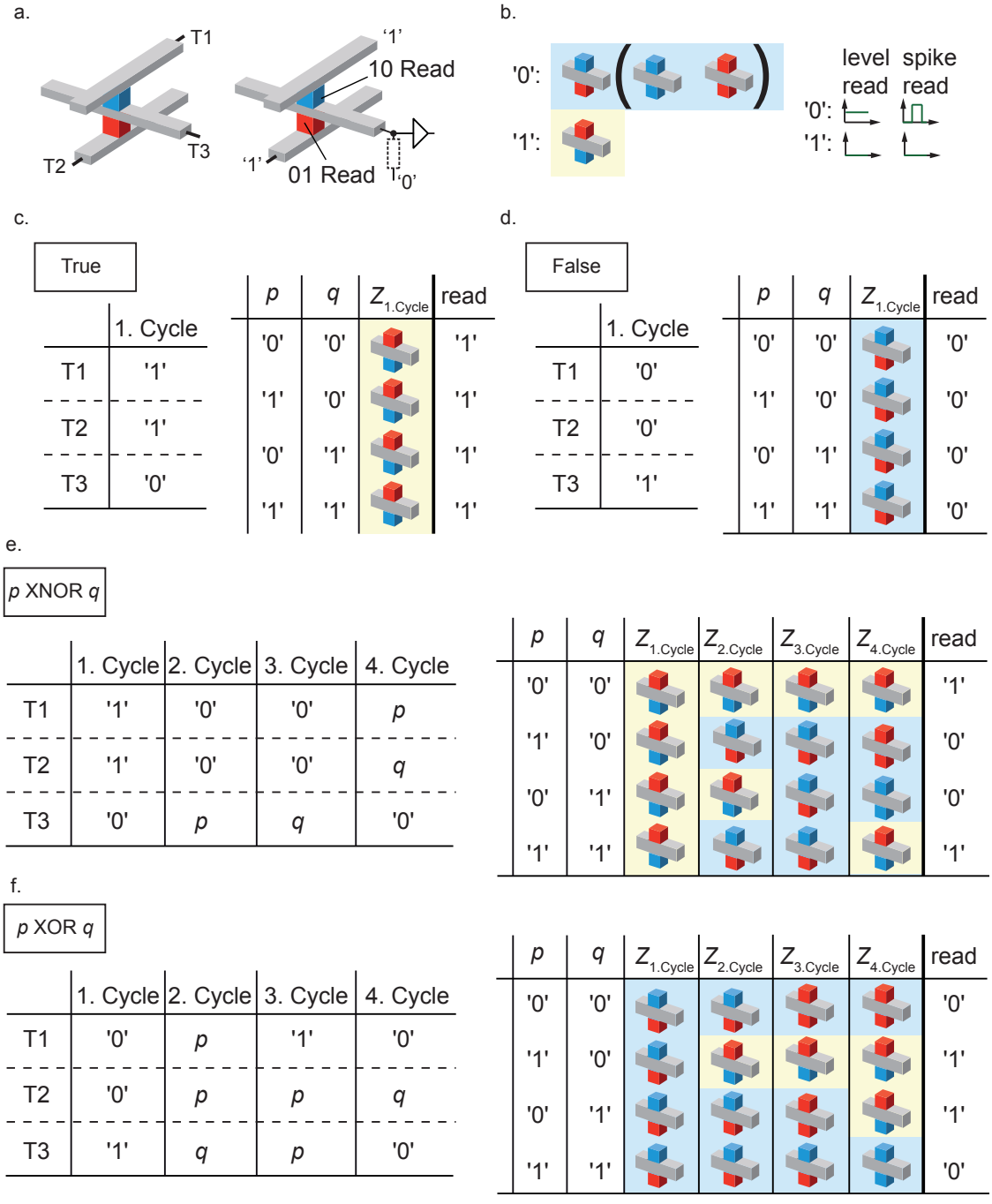


Figure 6.9: Logic operations with folded CRS I.

cycle, these operations are depicted first. The TRUE operation is defined as follows (Fig. 6.9c):

$$Z_{\text{top}} = \text{TRUE} = (\text{`1`} \text{ RIMP } \text{`0`}) \cdot Z'_{\text{top}} + (\text{`1`} \text{ NIMP } \text{`0`}) \cdot (\text{not } Z'_{\text{top}}) \tag{6.29}$$

$$Z_{\text{bottom}} = \text{FALSE} = (\text{`1`} \text{ IMP } \text{`0`}) \cdot Z'_{\text{bottom}} + (\text{`1`} \text{ RNIMP } \text{`0`}) \cdot (\text{not } Z'_{\text{bottom}}) \tag{6.30}$$

$$Z = \text{TRUE} = \text{TRUE } \& \text{ (not FALSE)} \tag{6.31}$$

There is only one FALSE operation defined (Fig. 6.9d), which realizes FALSE in one cycle and sets the top cell as well as the bottom cell to '0':

$$Z_{\text{top}} = \text{FALSE} = (\text{`0`} \text{ RIMP } \text{`1`}) \cdot Z'_{\text{top}} + (\text{`0`} \text{ NIMP } \text{`1`}) \cdot (\text{not } Z'_{\text{top}}) \tag{6.32}$$

$$Z_{\text{bottom}} = \text{TRUE} = (\text{`0`} \text{ IMP } \text{`1`}) \cdot Z'_{\text{bottom}} + (\text{`0`} \text{ RNIMP } \text{`1`}) \cdot (\text{not } Z'_{\text{bottom}}) \tag{6.33}$$

$$Z = \text{FALSE} = \text{FALSE } \& \text{ (not TRUE)} \tag{6.34}$$

Except for XOR and XNOR, all functions are identical to functions discussed in section 6.2.2, the difference being the twofold result storage. These functions are not considered here, but can be found in the Appendix B for the sake of completeness. For XNOR the first three steps are equivalent to NOR (compare equation (B.36) and see Fig. 6.9e). In the forth cycle, the following signals are applied:

$$Z_{\text{top,4.}} = (p \text{ RIMP } q) = (p \text{ RIMP } \text{`0`}) \cdot (p \text{ NOR } q) + (p \text{ NIMP } \text{`0`}) \cdot (p \text{ OR } q) \tag{6.35}$$

$$Z_{\text{bottom,4.}} = (p \text{ NIMP } q) = (q \text{ IMP } \text{`0`}) \cdot (p \text{ OR } q) + (q \text{ RNIMP } \text{`0`}) \cdot (p \text{ NOR } q) \tag{6.36}$$

$$Z = p \text{ XNOR } q = (p \text{ RIMP } q) \text{ \& (not } (p \text{ NIMP } q)) \tag{6.37}$$

For XOR the first two steps are equivalent to NIMP (compare equation (B.21) and Fig. 6.9f). In the third and forth cycle, the following signals are applied:

$$Z_{\text{top,3.}} = p \text{ NAND } q = (\text{`1`} \text{ RIMP } p) \cdot (p \text{ NIMP } q) + (\text{`1`} \text{ NIMP } p) \cdot (p \text{ IMP } q) \tag{6.38}$$

$$Z_{\text{bottom,4.}} = p \text{ NOR } q = (q \text{ IMP } \text{`0`}) \cdot (p \text{ IMP } q) + (q \text{ RNIMP } \text{`0`}) \cdot (p \text{ NIMP } q) \tag{6.39}$$

$$Z = p \text{ XOR } q = (p \text{ NAND } q) \text{ \& (not } (p \text{ NOR } q)) \tag{6.40}$$

With this folded CRS Moore logic, all 16 boolean logic functions can be realized.

6.4 Conclusion

In summary, bipolar resistive switches as well as complementary resistive switches can be considered as basic units for logic operations in passive crossbar arrays. They can be systematically understood as Moore or Mealy machines. Due to better array compatibility, CRSs are the cells of choice. CRS Mealy logic, especially folded CRS Mealy logic, is advantageous if a low cycle count is needed. But, since the logic result is directly outputted and not stored, this approach is best suited for joint logic and memory arrays.
For joint memory and logic arrays, the two-state CRS Moore logic is preferable. With this approach, 14 out of 16 boolean logic functions can be realized in at most three cycles and the logic result is directly stored to the memory.
If all 16 logic functions are to be present, folded CRS Moore logic, implemented on the same footprint as a single CRS, is the most suited approach. Note that both CRS cells are only needed for XNOR and XOR operations, which is why for most operations only one CRS cell is needed.

7 Conclusions

7.1 Summary

Complementary resistive switches are a very interesting option for future non-volatile passive nanocrossbar arrays. In combination with ultimately scaled CMOS, the resulting hybrid CMOS/nanocrossbar circuits are an opportunity to realize further downscaling of memory and logic devices, and paving the way to three-dimensional array structures.
A major aim of this work was to find a way to overcome the sneak path problem, which is present in passive crossbar arrays. With complementary resistive switches this goal could be achieved. The following paragraphs summarize the main achievements.

- Bipolar Resistive Switches - Modeling
  Several bipolar resistive switch models were introduced and corresponding compact modeling was described. First, two basic models using fixed parameters for threshold voltages and resistive states were considered. Then, the dynamical system approach was introduced and four dynamic models were implemented, including the initial memristive model. The most sophisticated model implemented was a refined ECM model, which is capable of reproducing measured multilevel behavior. For this model, the impact of the current compliance as well as the series resistor were studied in detail.

- Complementary Resistive Switches
  Complementary resistive switches can be constructed from any two terminal bipolar resistive switch, either ECM or VCM elements, by combining two elements anti-serially. The basic concept was introduced in this chapter and was illustrated by means of symmetric anti-serially connected bipolar resistive switches. As proof of concept, the device behavior was illustrated experimentally for anti-serially connected and integrated ECM as well as VCM elements. These measurements prove the universality of the concept, which is not limited to a specific material system.
  For CRS modeling, two bipolar resistive switches are connected anti-serially. For simulation, the bipolar resistive switch models from chapter 3 were used.

It was shown that the basic models, which offer a fixed threshold voltage, are suited for quasi-static simulations. Linear branch simulations as well as non-ohmic branch simulation were conducted. The impact of asymmetry on I-V characteristics was studied and simulations were conducted to reproduce measurements. It was illustrated that a stable 'ON' state, even for bipolar resistive switches offering a very asymmetric I-V characteristic, is feasible by application of a resistor in series to the CRS cell. In the next step dynamic models were considered. It was demonstrated that linear memristive models cannot be applied for principle reasons. Only dynamic non-linear models can be applied for CRS simulations. Realistic CRS results were obtained from dynamic ECM simulations. Simulations with different voltage ramps as well as several series resistance values verified the appropriateness of this model.

- Complementary Resistive Switches - Memory Applications
  Since CRS cells offer a high-resistive state in each storing state, the sneak path problem present in passive crossbar arrays can be solved. By comparing bipolar resistive switch-based arrays to complementary resistive switch-based arrays, this advantage was elaborated. The operation modes for passive arrays in terms of read and write voltage schemes as well as size limitations were discussed. For the readout of CRS cells, spike as well as level read operations can be performed. These pulse operations were verified by measurements. To avoid a destructive readout, an alternative capacitive divider-based readout scheme was introduced. By application of a non-destructive readout, BRS elements with low endurance values come into scope of application for CRS cells, but the possible array size is limited.

- Complementary Resistive Switches - Logic Applications
  Complementary resistive switches can not only be used as memory, but also as logic devices. It was shown that bipolar resistive switches as well as complementary resistive switches can be understood in terms of finite state machines, implementing the material implication (IMP) as a basic logic function. A low cycle count logic implementation considers CRS a Mealy machine using generated spikes for output. In CRS Moore logic, an additional read step - either level read or spike read - is needed for the readout. With folded CRS Moore logic, arbitrary logic functions can be realized in crossbar arrays in a footprint area of $4F^2$, while folded CRS Mealy logic allows for low cycle count NOR, XOR and AND implemention. A universal memory, allowing for logic operations in the memory itself, becomes feasible with CRS

Moore logic. With this approach, 14 out of 16 boolean functions can be realized in a single passive CRS crossbar array.

7.2 Outlook

The impact of the first publication on the CRS concept in 2010 in Nature Materials [50] lead to great interest in this topic. The relevance of the CRS concept is reflected by citations referring to [50]. In [55, 73, 116–126] a direct reference to CRS concept as a solution for the sneak path elimination is drawn. Additionally, in [127] read and write schemes for CRS cells in passive crossbar arrays are simulated, confirming CRS memory applications as described in [50]. In [128] CRS device modeling as well as read/write schemes are addressed, asserting the feasibility of future CRS-based passive crossbar arrays. In [129, 130] amorphous carbon (a-C) in combination with carbon nanotubes (CNT) was used to show CRS switching in anti-serially connected Au/a-C/CNT memory elements. The resulting I-V characteristics are very similar to those of ECM-based CRS cells. There are also reports of CRS switching in single VCM-type BRS cells [131, 132], assuming two anti-serial switching layers in such a single cell, while in [133, 134] Pt/ZrO_x/HfO_x/metal elements were connected anti-serially to form a CRS device showing VCM-type CRS switching. Another example of VCM-type CRS switching was given in [38], where Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt elements were used to verify CRS switching in this material system.
There are also ideas to use CRS for content-addressable memory [135] or for implementation of logical blocks [136] based on CRS material implication functionality (compare [109]). The CRS concept was incorporated into 2010 ITRS Roadmap ([137], ERD - Table 8) and is listed there as a selector device solution for future passive crossbar array-based memories.
Bringing CRS from the status of am emerging device to the status of a baseline device must be the goal of future research. In order to do this, several questions must be answered. The most important ones are:

- Which material class (ECM or VCM) is best suited?
- Which material system offers the lowest variations/best yield/highest endurance?
- Which computing paradigm is best suited for hybrid CMOS/CRS-nanocrossbar arrays?
- Are three-dimensional CRS arrays realizable in the future?

Appendix

A Fabrication

For verification measurements of complementary resistive switches, germanium selenide (GeSe)-based ECM elements as well as strontium titanate ($SrTiO_3$, STO for short)-based VCM devices were selected. Used GeSe elements consist of a Pt bottom electrode (30 nm), a rf-sputtered $Ge_{30}Se_{70}$ thin film (25 nm), a rf-sputtered SiO_2 (3 nm) and a 70 nm Cu top electrode, deposited by thermal evaporation. Details on fabrication can be found in [138, 139]. Used STO elements consist of a Ti bottom electrode, 8 nm high pressure sputtered STO, and a Pt top electrode. Details on fabrication can be found in [43].

A.1 Integrated CRS Cells

For integration, Pt/SiO_2/Cu-based elements were selected. Fig. A.1a shows a vertically stacked Pt/SiO_2/Cu/Pt/Cu/SiO_2/Ti/Pt CRS cell. Fig. A.1a shows the implemented stack. For testing reasons, the middle electrode can be accessed (Fig. A.1b). For study of device behavior, a parallel layout (Fig. A.1c-d) can be used instead of fully vertical integrated cells; this provides completely identical cells. Fig. A.1e shows a CRS crossbar array with fully vertical integrated cells, while Fig. A.1f depicts a crossbar array for parallel layout. Instead of SiO_2, other switching material systems as well as different electrode materials can be used in variable film thicknesses.

Fig. A.2a shows a SEM picture of a fully vertical integrated CRS cell with accessible middle electrode (compare Fig. A.1b). Fig. A.2b shows a fully vertical integrated CRS without middle electrode (compare Fig. A.1e). For capacitive non-destructive readout (NDRO), a modified parallel layout is selected (see section 5.4). Fig. A.3a shows a layout sketch and Fig. A.3b a SEM picture. In the modified parallel layout, external CRS connects are labeled with 'Terminal 1' and 'Terminal 2'. The Cu bottom electrode is only needed for single element access. The area of element B is $10\ \mu m \cdot 5\ \mu m$ and the area of element A is $15\ \mu\text{m} \cdot 10\ \mu\text{m}$, thus the area differs by a factor of 3. To increase dielectric constant instead of SiO_2 also TiO_2 as applied in the modified parallel layout [112]. Further details on fabrication of integrated cells can be found in [41].

The lithography masks for parallel CRS layout were also applied for VCM type CRS cells (see [108] for fabrication details).

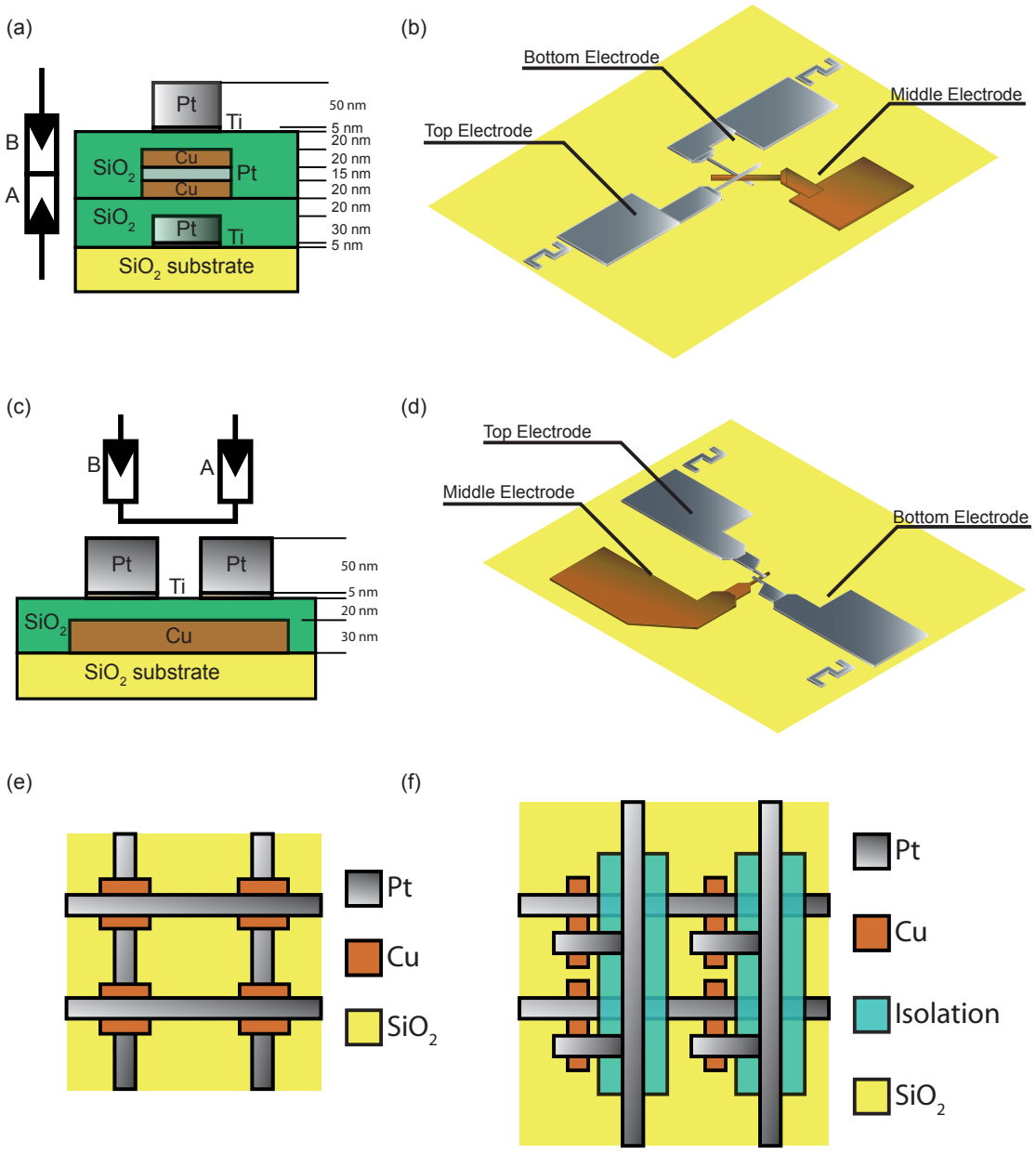


Figure A.1: (a) Element A ($Pt/SiO_2/Cu$) and element B ($Cu/SiO_2/Ti/Pt$) form a vertically integrated CRS cell. (b) Layout sketch of a CRS stack from (a). For testing reasons, the middle electrode can be contacted externally. (c) Instead of a fully vertical integration, a parallel CRS cell can be constructed, offering completely identical elements. (d) Layout sketch of a parallel CRS cell. (e) Sketch of a CRS crossbar array layout for vertical integrated CRS cells. (f) Layout sketch of a parallel CRS cell-based crossbar array. An additional layer for isolation is need in this layout. Adapted from [41].

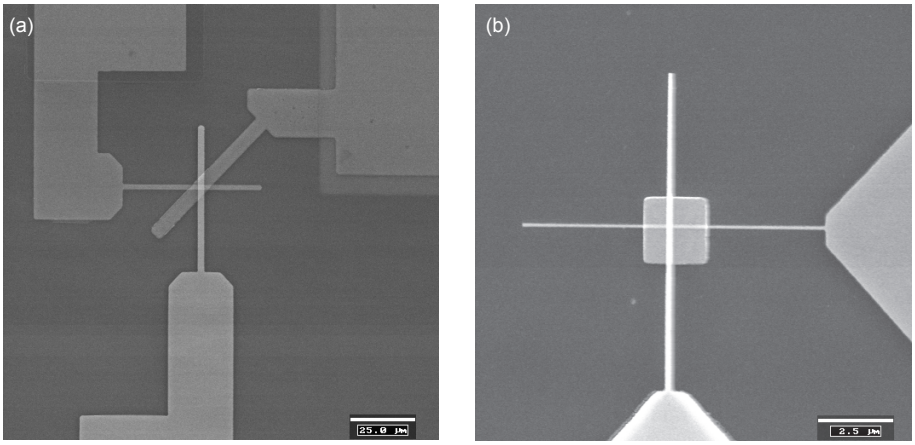


Figure A.2: (a) SEM picture of a fully integrated CRS cell with an accessible middle electrode taken from [41]. (b) SEM picture of a fully integrated CRS cell without an accessible middle electrode. This implementation style is usable for crossbar array memories, compare A.1e.

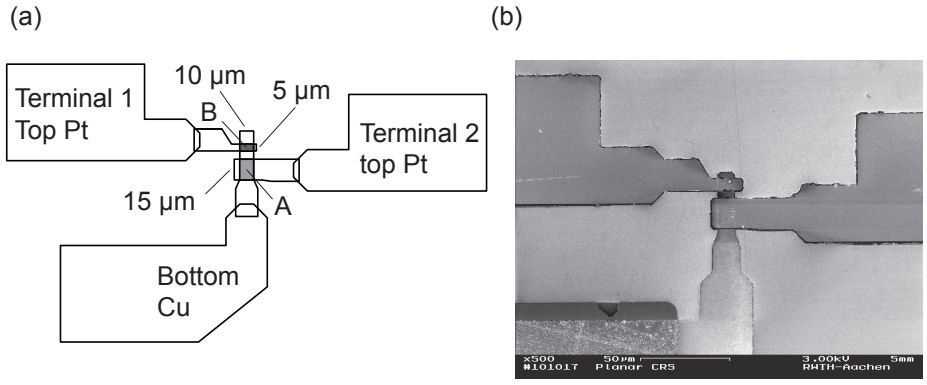


Figure A.3: (a) Layout sketch of the modified parallel layout. (b) SEM image of the modified parallel layout.

B Folded CRS Moore Logic

In this section, two-state folded CRS logic functions, which are analogous to single CRS operations in section 6.2.2, are presented for the sake of completeness. In Fig. B.4a, the function p is depicted. After execution of the TRUE operation in the first cycle, p is realized in the second cycle:

$$Z_{\text{top}} = p = (p \text{ RIMP '1'}) \tag{B.1}$$

$$Z_{\text{bottom}} = \text{not } p = (p \text{ RNIMP '1'}) \tag{B.2}$$

$$Z = p = p \,\&\, (\text{not not } p). \tag{B.3}$$

Correspondingly, the q operation reads (see Fig. B.4b):

$$Z_{\text{top}} = q = (q \text{ RIMP } \text{`1`}) \tag{B.4}$$
$$Z_{\text{bottom}} = \text{not } q = (q \text{ RNIMP } \text{`1`}) \tag{B.5}$$
$$Z = q = q \ \& \ (\text{not not } q). \tag{B.6}$$

Similarly, the negation (not p, not q) can be realized after an initial TRUE operation (see Fig. B.4c,d):

$$Z_{\text{top}} = \text{not } p = (\text{`0`} \text{ RIMP } p) \tag{B.7}$$
$$Z_{\text{bottom}} = p = (\text{`0`} \text{ RNIMP } p) \tag{B.8}$$
$$Z = \text{not } p = \text{not } p \ \& \ \text{not } p. \tag{B.9}$$

$$Z_{\text{top}} = \text{not } q = (\text{`0`} \text{ RIMP } q) \tag{B.10}$$
$$Z_{\text{bottom}} = q = (\text{`0`} \text{ RNIMP } q) \tag{B.11}$$
$$Z = \text{not } q = \text{not } q \ \& \ \text{not } q. \tag{B.12}$$

In Fig. B.5a,b, the operations p IMP q and p RIMP q are shown. After an initial TRUE operation, the IMP operation is executed in the second cycle:

$$Z_{\text{top}} = (q \text{ RIMP } p) \tag{B.13}$$
$$Z_{\text{bottom}} = (p \text{ RNIMP } q) \tag{B.14}$$
$$Z = p \text{ IMP } q. \tag{B.15}$$

Correspondingly, the RIMP operation reads:

$$Z_{\text{top}} = (p \text{ RIMP } q) \tag{B.16}$$
$$Z_{\text{bottom}} = (p \text{ RNIMP } q) \tag{B.17}$$
$$Z = p \text{ RIMP } q. \tag{B.18}$$

For the NIMP and RNIMP operation, the FALSE operation is applied in the first cycle (see Fig. B.5c,d). The NIMP operation is realized in the second cycle as follows:

$$Z_{\text{top}} = (p \text{ NIMP } q) \tag{B.19}$$
$$Z_{\text{bottom}} = (p \text{ IMP } q) \tag{B.20}$$
$$Z = p \text{ NIMP } q. \tag{B.21}$$

Correspondingly, the RNIMP operation reads:

$$Z_{\text{top}} = (q \text{ NIMP } p) \tag{B.22}$$
$$Z_{\text{bottom}} = (q \text{ IMP } p) \tag{B.23}$$
$$Z = p \text{ RNIMP } q. \tag{B.24}$$

Based on presented two cycle operations, NAND, OR, AND and NOR operations can be realized in three cycles. The NAND operation (see Fig. B.6a) is realized in the third cycle as follows:

$$Z_{\text{top}} = (\text{`1`} \text{ RIMP } p) \cdot (\text{ not } q) + (\text{`1`} \text{ NIMP } p) \cdot q \tag{B.25}$$
$$Z_{\text{bottom}} = (\text{`1`} \text{ IMP } p) \cdot q + (\text{`1`} \text{ RNIMP } p) \cdot (\text{ not } q) \tag{B.26}$$
$$Z = p \text{ NAND } q. \tag{B.27}$$

The OR operation (see Fig. B.6b) reads:

$$Z_{\text{top}} = (q \text{ RIMP } \text{`0`}) \cdot p + (q \text{ NIMP } \text{`0`}) \cdot (\text{not } p) \tag{B.28}$$
$$Z_{\text{bottom}} = (q \text{ IMP } \text{`0`}) \cdot (\text{ not } p) + (q \text{ RNIMP } \text{`0`}) \cdot p \tag{B.29}$$
$$Z = p \text{ OR } q. \tag{B.30}$$

The AND operation (see Fig. B.6c) reads:

$$Z_{\text{top}} = (p \text{ RIMP } \text{`1`}) \cdot q + (p \text{ NIMP } \text{`1`}) \cdot (\text{not } q) \tag{B.31}$$
$$Z_{\text{bottom}} = (p \text{ IMP } \text{`1`}) \cdot (\text{ not } q) + (p \text{ RNIMP } \text{`1`}) \cdot q \tag{B.32}$$
$$Z = p \text{ AND } q. \tag{B.33}$$

Finally, the NOR operation (Fig. B.6d) reads:

$$Z_{\text{top}} = (\text{`0`}\ \text{RIMP}\ q) \cdot (\ \text{not}\ p) + (\text{`0`}\ \text{NIMP}\ q) \cdot p \tag{B.34}$$

$$Z_{\text{bottom}} = (\text{`0`}\ \text{IMP}\ q) \cdot p + (\text{`0`}\ \text{RNIMP}\ q) \cdot (\ \text{not}\ p) \tag{B.35}$$

$$Z = p\ \text{NOR}\ q. \tag{B.36}$$

a. p

	1. Cycle	2. Cycle
T1	'1'	p
T2	'1'	p
T3	'0'	'1'

p	q	$Z_{1.Cycle}$	$Z_{2.Cycle}$	read
'0'	'0'			'0'
'1'	'0'			'1'
'0'	'1'			'0'
'1'	'1'			'1'

b. q

	1. Cycle	2. Cycle
T1	'1'	q
T2	'1'	q
T3	'0'	'1'

p	q	$Z_{1.Cycle}$	$Z_{2.Cycle}$	read
'0'	'0'			'0'
'1'	'0'			'0'
'0'	'1'			'1'
'1'	'1'			'1'

c. not p

	1. Cycle	2. Cycle
T1	'1'	'0'
T2	'1'	'0'
T3	'0'	p

p	q	$Z_{1.Cycle}$	$Z_{2.Cycle}$	read
'0'	'0'			'1'
'1'	'0'			'0'
'0'	'1'			'1'
'1'	'1'			'0'

d. not q

	1. Cycle	2. Cycle
T1	'1'	'0'
T2	'1'	'0'
T3	'0'	q

p	q	$Z_{1.Cycle}$	$Z_{2.Cycle}$	read
'0'	'0'			'1'
'1'	'0'			'1'
'0'	'1'			'0'
'1'	'1'			'0'

Figure B.4: Logic operations with folded CRS II.

a. p IMP q

	1. Cycle	2. Cycle
T1	'1'	q
T2	'1'	q
T3	'0'	p

p	q	$Z_{1.Cycle}$	$Z_{2.Cycle}$	read
'0'	'0'			'1'
'1'	'0'			'0'
'0'	'1'			'1'
'1'	'1'			'1'

b. p RIMP p

	1. Cycle	2. Cycle
T1	'1'	p
T2	'1'	p
T3	'0'	q

p	q	$Z_{1.Cycle}$	$Z_{2.Cycle}$	read
'0'	'0'			'1'
'1'	'0'			'1'
'0'	'1'			'0'
'1'	'1'			'1'

c. p NIMP q

	1. Cycle	2. Cycle
T1	'0'	p
T2	'0'	p
T3	'1'	q

p	q	$Z_{1.Cycle}$	$Z_{2.Cycle}$	read
'0'	'0'			'0'
'1'	'0'			'1'
'0'	'1'			'0'
'1'	'1'			'0'

d. p RNIMP q

	1. Cycle	2. Cycle
T1	'0'	q
T2	'0'	q
T3	'1'	p

p	q	$Z_{1.Cycle}$	$Z_{2.Cycle}$	read
'0'	'0'			'0'
'1'	'0'			'0'
'0'	'1'			'1'
'1'	'1'			'0'

Figure B.5: Logic operations with folded CRS III.

a.

p NAND *q*

	1. Cycle	2. Cycle	3. Cycle
T1	'1'	'0'	'1'
T2	'1'	'0'	'1'
T3	'0'	*q*	*p*

p	*q*	$Z_{1.Cycle}$	$Z_{2.Cycle}$	$Z_{3.Cycle}$	read
'0'	'0'				'1'
'1'	'0'				'1'
'0'	'1'				'1'
'1'	'1'				'0'

b.

p OR *q*

	1. Cycle	2. Cycle	3. Cycle
T1	'1'	*p*	*q*
T2	'1'	*p*	*q*
T3	'0'	'1'	'0'

p	*q*	$Z_{1.Cycle}$	$Z_{2.Cycle}$	$Z_{3.Cycle}$	read
'0'	'0'				'0'
'1'	'0'				'1'
'0'	'1'				'1'
'1'	'1'				'1'

c.

p AND *q*

	1. Cycle	2. Cycle	3. Cycle
T1	'1'	*q*	*p*
T2	'1'	*q*	*p*
T3	'0'	'1'	'1'

p	*q*	$Z_{1.Cycle}$	$Z_{2.Cycle}$	$Z_{3.Cycle}$	read
'0'	'0'				'0'
'1'	'0'				'0'
'0'	'1'				'0'
'1'	'1'				'1'

d.

p NOR *q*

	1. Cycle	2. Cycle	3. Cycle
T1	'1'	'0'	'0'
T2	'1'	'0'	'0'
T3	'0'	*p*	*q*

p	*q*	$Z_{1.Cycle}$	$Z_{2.Cycle}$	$Z_{3.Cycle}$	read
'0'	'0'				'1'
'1'	'0'				'0'
'0'	'1'				'0'
'1'	'1'				'0'

Figure B.6: Logic operations with folded CRS IV.

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