Ion-sensitive field-effect transistors fabricated in a commercial CMOS technology

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Abstract:

The fabrication of pH-sensitive ISFET devices in an unmodified two-metal commercial CMOS technology (1.0 μm from Atmel-ES2) is reported. The ISFET devices have a gate structure compatible with the CMOS process, with an electrically floating electrode consisting on polysilicon plus the two metals. The passivation oxynitride layer acts as the pH-sensitive material in contact with the liquid solution. The devices have shown good operating characteristics, with a 47 mV/pH response. The use of a commercial CMOS process allows the straightforward integration of signal-processing circuitry. An ISFET amplifier circuit has been integrated with the ISFET sensors.

Keywords: ISFETs, CMOS sensors, silicon oxynitride

1. Introduction

Ion-sensitive field-effect transistors (ISFETs), first described by Bergveld in the early 1970's [1], have experienced a strong development. The ISFET has advantages over ion selective electrodes (ISE), such as small size, low cost and robustness. However, to be useful for chemical analysis, these properties must also be achieved for the complete analytical instrument. A small system size with a low cost is required, for example, for portable analytical applications. The integration of the ISFET measurement circuitry with the ISFET sensor in the same silicon chip can be advantageous in order to obtain a small system size and a low cost (if the production volumes are relatively high). A typical circuit that can be integrated for the measurement of the ISFETs is the ISFET amplifier, also known as source-drain follower [2]. A higher level of integration also results in a higher system reliability.

The integration of pH-sensitive ISFETs and electronic circuitry requires the fabrication of the ISFET devices in a CMOS technology. This, however, is not a straightforward task. The main problem is that a standard ISFET has only insulating materials in its gate region, which must be in contact with the liquid solution. By contrast, in a CMOS process a polycrystalline silicon (polysilicon) electrode in the gate region is required to define the self-aligned source and drain regions for the MOS transistors. This means that specific processes or design structures must be used to fabricated the ISFETs in a CMOS process. A first approach is to use dedicated CMOS processes with specific "ISFET steps" [3,4,5]. However, to fabricate integrated sensors it is desirable to use standard CMOS processes, as this has a number of advantages. The system design can be greatly simplified if a commercial process from a CMOS foundry is used, as in this

case the foundry well established design environment can be used. This includes all existing signal-processing circuit standard cells, which can be directly applied to the design of the system [6].

To obtain the source and drain regions of the ISFET in a standard CMOS process, a polysilicon electrode must be left in the gate area. A successful ISFET operation can be obtained in this case if an insulating pH-sensitive layer is located on top of the polysilicon. This is because an ISFET can be, in principle, considered as an ISE with FET detection [7]. Using this concept, extended gate ISFET structures were developed [8,9], in which a chemically-sensitive layer was deposited over a metal, which was connected by a metal line to the gate of a MOSFET. A particular case of this structure would have the metal interconnect length reduced to zero, in which case a vertical structure “sensitive layer / metal / FET gate oxide” is obtained. This structure would be the same as the “sensitive layer / polysilicon / gate oxide” structure that is required for the CMOS-compatible ISFET.

ISFET devices with an electrically-floating polysilicon gate were fabricated in a modified CMOS process by Bousse et al. [10]. The polysilicon was used to define the source and drain regions, and was covered by a silicon nitride layer, used as the pH-sensitive material. To obtain good chemical sensing properties, the silicon nitride was deposited by the low-pressure chemical vapour deposition technique at a high temperature. The silicon nitride was also used as the CMOS passivation, and was therefore deposited after the metal layer. This precluded the use of a standard CMOS metallisation based on aluminium. Thus a specific metallisation scheme based on tungsten silicide, able to withstand high temperatures, was used in that process. A

similar device structure had been considered previously by Smith et al. [11] for electrostatic protection of the ISFET gate, but in that case the polysilicon gate was not completely floating, as it was connected via a MOSFET switch to the external measurement circuitry. The use of a polysilicon layer on the ISFET gate has also been shown to be useful for achieving a low light sensitivity [12].

In this work the fabrication of pH-sensitive ISFETs in an unmodified 2-metal commercial CMOS process is presented. The ISFET devices have a gate structure compatible with the CMOS process, with an electrically-floating conducting electrode consisting on polysilicon plus the two metals. The silicon oxynitride CMOS passivation layer acts as the pH-sensitive material of the ISFETs. The device structure is presented in section 2. An ISFET amplifier circuit has been integrated in the same chip. The circuit is based on existing standard circuit cells from the foundry circuit cell library. Section 3 discusses the experimental conditions that have been used for the electrical and chemical characterisation of the ISFET devices. The resulting electrical and chemical operating characteristics of the devices is presented and discussed in section 4.

2. Device structure

The ISFETs have been fabricated in the 1.0 μm commercial CMOS technology from Atmel-ES2, Rousset, France. This process has two metal levels and one polysilicon layer. The source and drain regions of the MOS transistors are defined by self-aligned ion implantations using the gate polysilicon as a mask, which is a common feature of all standard CMOS processes. The process includes a lightly-doped drain (LDD) extension

for the NMOS transistors. In order to fabricate the source and drain regions of the ISFETs, a polysilicon electrode must therefore be present in the gate area.

The dielectric layer in contact with the liquid solution must be one of the dielectrics used in the CMOS process. The material that would have better pH-sensing properties is the 1.5 μm-thick silicon oxynitride passivation. Additionally, as it is the last layer of the process, its surface properties would not be affected by further processing. The pH-sensitive passivation layer can therefore be deposited on the polysilicon gate electrode, which can then be left electrically floating [10], thus obtaining in the gate region of the ISFET a series combination of the passivation oxynitride capacitance and the oxide gate capacitance. In this way, the pH-dependent electrical charge in the surface of the oxynitride insulator in contact with the liquid solution is detected by the silicon surface. This approach, which seems straightforward, has however a technological problem. It is not possible to obtain a polysilicon-passivation structure if the standard CMOS process is followed. The fabrication of such structure requires the removal of the two inter-metal oxides and the two metal layers from the polysilicon area. However, the etching of these layers destroys the underlying polysilicon. Fortunately, there is a way to circumvent this problem. An electrically-floating conducting electrode can be obtained in the gate region if the two metal layers are left on top of the polysilicon. The cross-section of the resulting structure is shown in Fig. 1.a.

The multi-conductor gate structure allows some degrees of freedom for the geometrical dimensions of the different conductive layers. A number of ISFETs with different geometries have been designed and fabricated, as shown in table 1. In all cases the channel length is 2.5 μm. Device types 1 and 2 have a standard linear gate structure,

following the cross-section of Fig. 1.a. To obtain a high transistor channel width, and thus a high transconductance, in a small silicon area, an interdigitated source and drain layout has been used in device types 3 to 5. In device 3 the metals are just located over the polysilicon, with basically the same dimensions. Device types 4 and 5 have been designed with a continuous rectangular metal layer on top of the polysilicon strips that define the interdigitated sources and drains. Fig.1.b. shows a schematic top view of their layout. Fig. 1.c. shows a schematic cross-section of these “continuous metal” devices. This structure has one advantage from the technological point of view. It is more similar to the structures that appear in CMOS circuits, where metal interconnects are on top of the inter-metal oxides and contact the polysilicon only at specific points. Also, it allows to use standard CMOS dimensions for the metal-1 to polysilicon contact holes and the metal-2 to metal-1 vias, although we have used higher contact dimensions in our devices. Fig. 2 shows a photograph of a chip that includes all ISFET types. Two versions, corresponding to NMOS and PMOS ISFETs have been fabricated, but only the NMOS devices are reported here.

3. Experimental

To allow the ISFET devices to be immersed in a liquid solution during measurements, the ISFET chips were mounted near the tip of a 110 mm x 6 mm printed circuit board (PCB) and wire-bonded in the usual manner. The chips, wire-bonding and copper tracks of the PCB were then encapsulated by hand using an epoxy resin (Epo-Tek H77, from Epoxy Technology Inc.) so that only the ISFET gate was exposed to the environment, while all electrical contacts were insulated by the epoxy encapsulant.

The electrical characteristics of the ISFETs have been measured by using an HP-4145B semiconductor parameter analyser. For the chemical pH-sensitivity measurements, the ISFETs have been connected to an ISFET-amplifier system allowing the source voltage (V_S) to be measured while the drain current (I_D) and the drain-to-source voltage (V_{DS}) is kept constant [2], with the reference electrode grounded. In this way the variations of the V_S voltage give directly the variations of the threshold voltage. Values of V_{DS} = 0.5 V and I_D = 100 μA have been used.

As discussed in the introduction, one of the advantages of fabricating the ISFETs in a commercial CMOS process is that all the existing circuit standard cells can be used to integrate with the ISFET the circuitry required to measure it. We have therefore designed an integrated version of the ISFET-amplifier circuit by using standard cells from the Atmel-ES2 1.0 CMOS process. The ISFET amplifier (Fig. 3) has been integrated in the same chip as two “continuous metal” (type 5) ISFETs. The system chip is shown in Fig. 4. Most of the contacting pads that can be seen in the circuit are only for circuit testing purposes during the prototype stage.

In all the experiments the voltage has been measured vs. a double junction Ag-AgCl reference electrode (Orion 900200) with the outer chamber filled with a 0.1 M KNO_3 solution. The pH-sensitivity measurements have been made at a constant temperature (25 ºC) and in a 2 % tris(hydroxymethyl)aminomethane buffer solution to which HCl has been added to obtain different pH values. The electrical characteristics of the ISFETs have been measured on a pH 7 solution. The pH of the test solution has been monitored continuously with a digital pH-meter (micropH 2002) and a glass electrode,

calibrated with standard buffer solutions. Prior to the sensitivity measurements, all ISFETs have been immersed in a 2% HF solution for 15 s, in order to eliminate any silicon dioxide existing on the silicon oxynitride surface.

4. Results and discussion

The electrical characterisation has shown that all the ISFETs have good characteristics as field-effect transistors. An example is shown in Fig. 5. The drain current and the transconductance versus the gate-to-source voltage for one type 5 device are shown, for different pH values of the liquid solution. The experimental conditions have been described in section 3.

The fabricated ISFET devices have a non standard gate structure. It is therefore interesting to discuss their threshold voltage values V_T. Table 1 shows the mean threshold voltage values obtained from five different devices of each type. The devices of types 1, 2 and 3 have a linear structure for the gate floating electrode, shown in cross-section in Fig. 1.a. All of them have similar threshold voltages (within the dispersion error) of the order of 6.5 V. The threshold voltage of the ISFETs can be calculated using the standard site-binding model [13] adapted to insulators having both amphoteric and basic sites [14], such as the silicon nitride and oxynitride, and using also the standard semiconductor device theory [15]. The high positive threshold voltage value obtained in our case can be explained by the big thickness (1.5 μm) of the oxynitride layer. The devices of types 4 and 5 have a continuous metal over polysilicon lines (Fig.1., b and c). The values obtained for the threshold voltage of these devices is different from the

previous ones. These ISFETs have a metal-to-solution capacitor area greater than the polysilicon gate area. The area relationships are about 3.1 for the device type 4 and 4.4 for the device type 5. The measurements have shown that there is a negative threshold voltage shift from the linear structure devices which is greater when this area relationship is higher. A possible explanation of this behaviour is that the fixed positive charge that exists in the passivation oxynitride over the metal area is seen as a higher charge per unit transistor gate area by the “continuous metal” devices. When this effect is included in the threshold voltage calculation discussed above, the experimental behaviour can be qualitatively reproduced. A quantitative discussion with this model is difficult as we don’t know the real values of many material property parameters, but the calculation is compatible with the 14 V threshold voltage span between the different designs that has been found experimentally. Note that device 5 has a negative threshold voltage, and therefore is a depletion MOSFET that can be operated near 0 V of gate to source voltage, thus within the 0 to 5 V available for the CMOS circuitry.

The pH-sensitivity results for a type 5 device are shown in Fig. 6. A sensitivity of 47 mV/pH has been obtained. The pH-sensitivity of silicon oxynitride layers depends on their composition and more precisely on the ratio between surface silanol sites and amine sites[16], and this value is within the expected range. The ISFETs have been operating satisfactorily for more than two months.

The integrated ISFET amplifier circuits, shown in Figs. 3 and 4, have been electrically characterised, and good operational characteristics have been obtained. They have been successfully used to continuously measure the gate to source voltage of ISFETs located in a liquid solution of varying pH.

5. Conclusions

pH-sensitive ISFET devices have been fabricated in a commercial CMOS technology, with no modifications. A specific gate structure has been used which includes an electrically floating electrode consisting on polysilicon plus the two metals. This structure has allowed the design of devices with continuous metals on top of interdigitated sources and drains. For these devices, the threshold voltage depends on the ratio of the area of the continuous metals to the area of the polysilicon. The ISFETs have operated satisfactorily, with a 47 mV/pH response, corresponding to the silicon oxynitride passivation that has been used as the pH-sensitive material.

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Biographies:

Joan Bausells was born in Barcelona, Spain, in 1957. He graduated in Physics in 1980, and received M.S. (1982) and Ph.D. (1986) degrees in Solid-State Physics, all from the University of Barcelona. From 1981 to 1986 he worked as a process and R&D engineer in the semiconductor industry. In 1986 he joined CNM, where he is a permanent researcher from 1988. At CNM he has worked in ion implantation technology, and has been manager of Clean Room Operations and head of the Sensor and Actuator Group. His current research interests are silicon sensor and actuator devices and their applications to silicon microsystems.

Jordi Carrabina was born in Manresa, Spain, in 1963. He graduated in physics in 1986, and received M.S. degree (1988) in Microelectronics and Ph.D. degree (1991) in Computer Science, all from the University Autonoma of Barcelona. From 1986 to 1991 he held a grant in the National Microelectronics Center (CNM) in Barcelona. In 1991 he joined the University Autonoma of Barcelona, where he is an Associate Professor since 1992. His main research interests are CAD tools and design methodology for system design, including silicon microsystems and hardware-software codesign.

Abdelhamid Errachid was born in Khenifra, Morocco, in 1966. He graduated in Physics from the University M. Ismail, Meknes, in 1992, and has received a Ph.D. in Electronic Engineering from Universitat Autònoma de Barcelona in 1998. His research interests are the development of ISFET devices for the measurement of different ions, and integrated instrumentation for ISFETs.

Angel Merlos was born in Sabadell (Barcelona), Spain, in 1965. He received the Ph.D. degree in 1993 from the Autonomous University of Barcelona. In 1988 he joined the CNM's Silicon Technology and Microsystems Department. His areas of interest include silicon micromachining technologies and their applications to integrated sensors and actuators, and silicon optoelectronics integrated technologies.

Table 1. Gate structure and dimensions of the fabricated devices and their measured threshold voltages

Device type	Gate structure	Channel width (μm)	V_T (V) (at pH=7)
1	Linear	250	6.4 ± 1.4
2	Linear	500	7.1 ± 1.0
3	Interdigitated – Linear metal	2 x 250	6.3 ± 0.4
4	Interdigitated – Continuous metal	2 x 250	3.6 ± 0.5
5	Interdigitated – Continuous metal	10 x 250	-7.0 ± 0.8

Figure captions:

Fig. 1. a) Schematic cross section of the linear ISFET structure; b) Top view of the interdigitated “continuous metal” ISFET; c) Schematic cross section of the interdigitated “continuous metal” ISFET.

Fig. 2. Photograph of the ISFET chip, with the 5 types of ISFET devices. Types 1 to 5 appear from top to bottom.

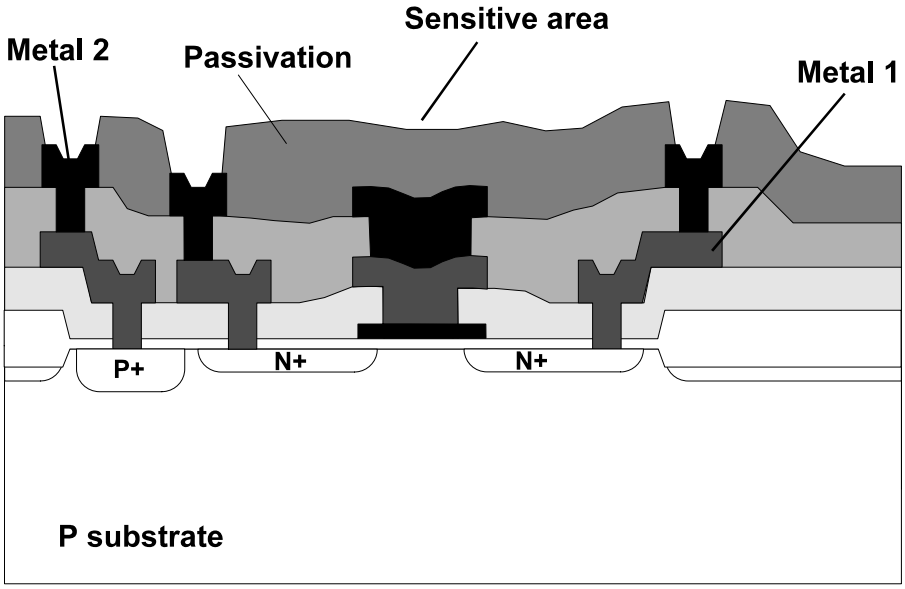
Fig. 3. Circuit schematic of the ISFET amplifier (source and drain follower).

Fig. 4. Photograph of a chip containing two type 5 ISFETs (the rectangular structures on the left side) and an integrated ISFET-amplifier circuit.

Fig. 5. Drain current (I_D) and transconductance (g_m) versus gate-to-source voltage for a type 5 ISFET, for different pH values of the liquid solution.

Fig. 6. pH-sensitivity results for a typical type 5 ISFET, plotted as the threshold voltage shift from the pH=7 value.

a)



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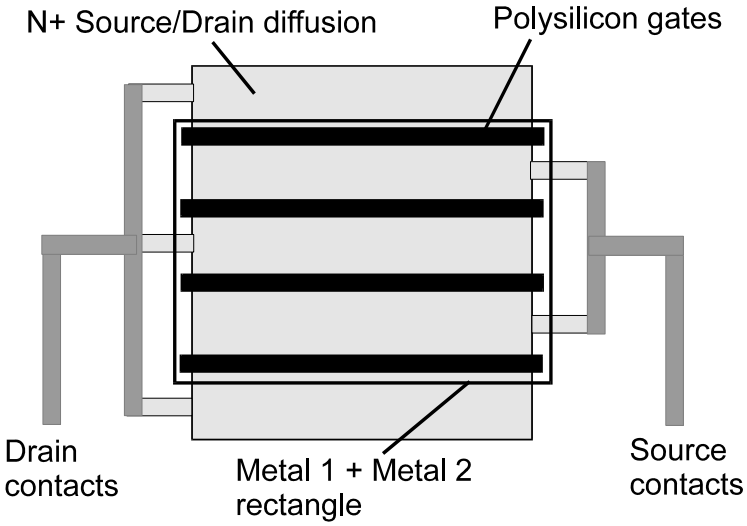

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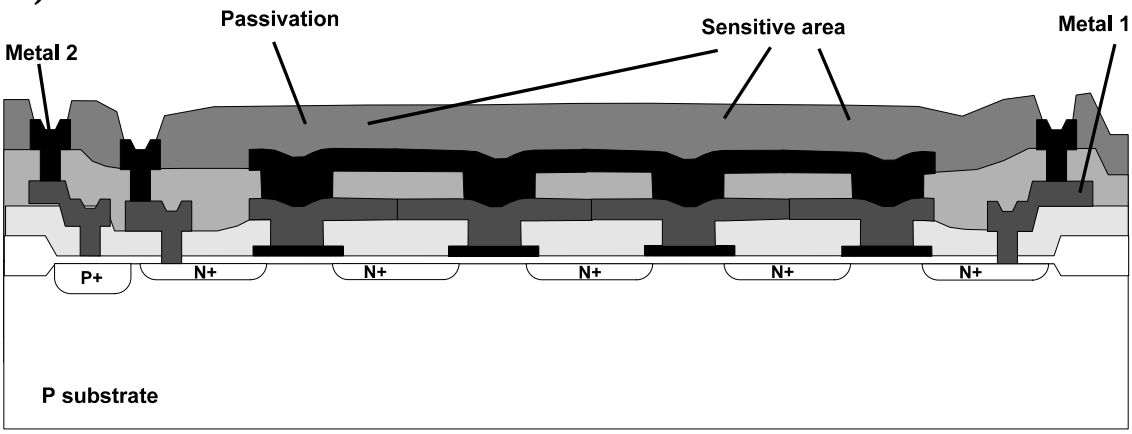
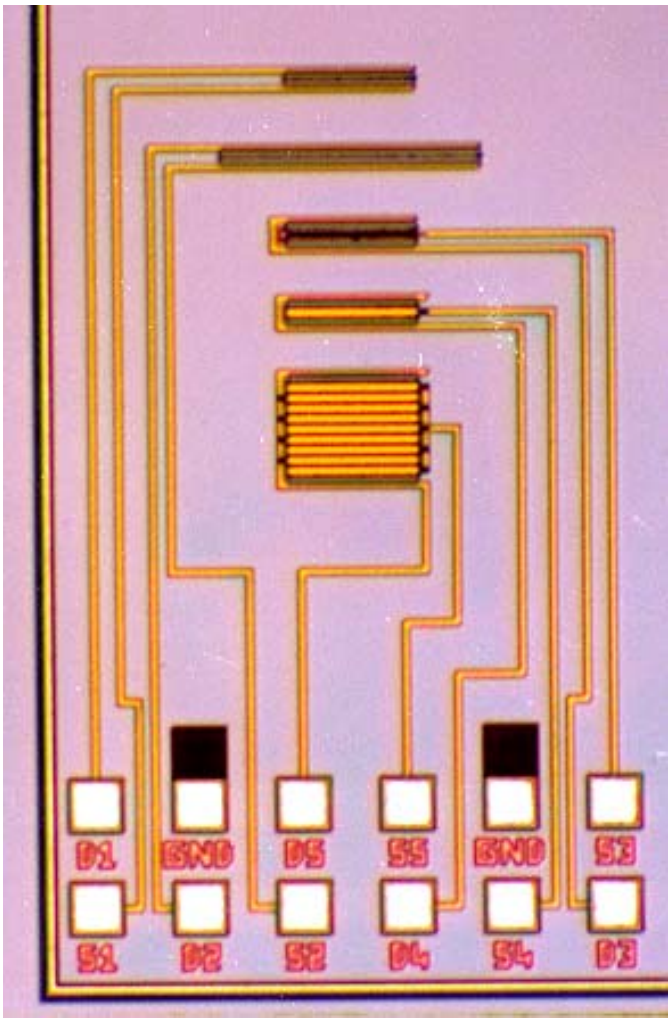


Bausells et al., Fig. 1



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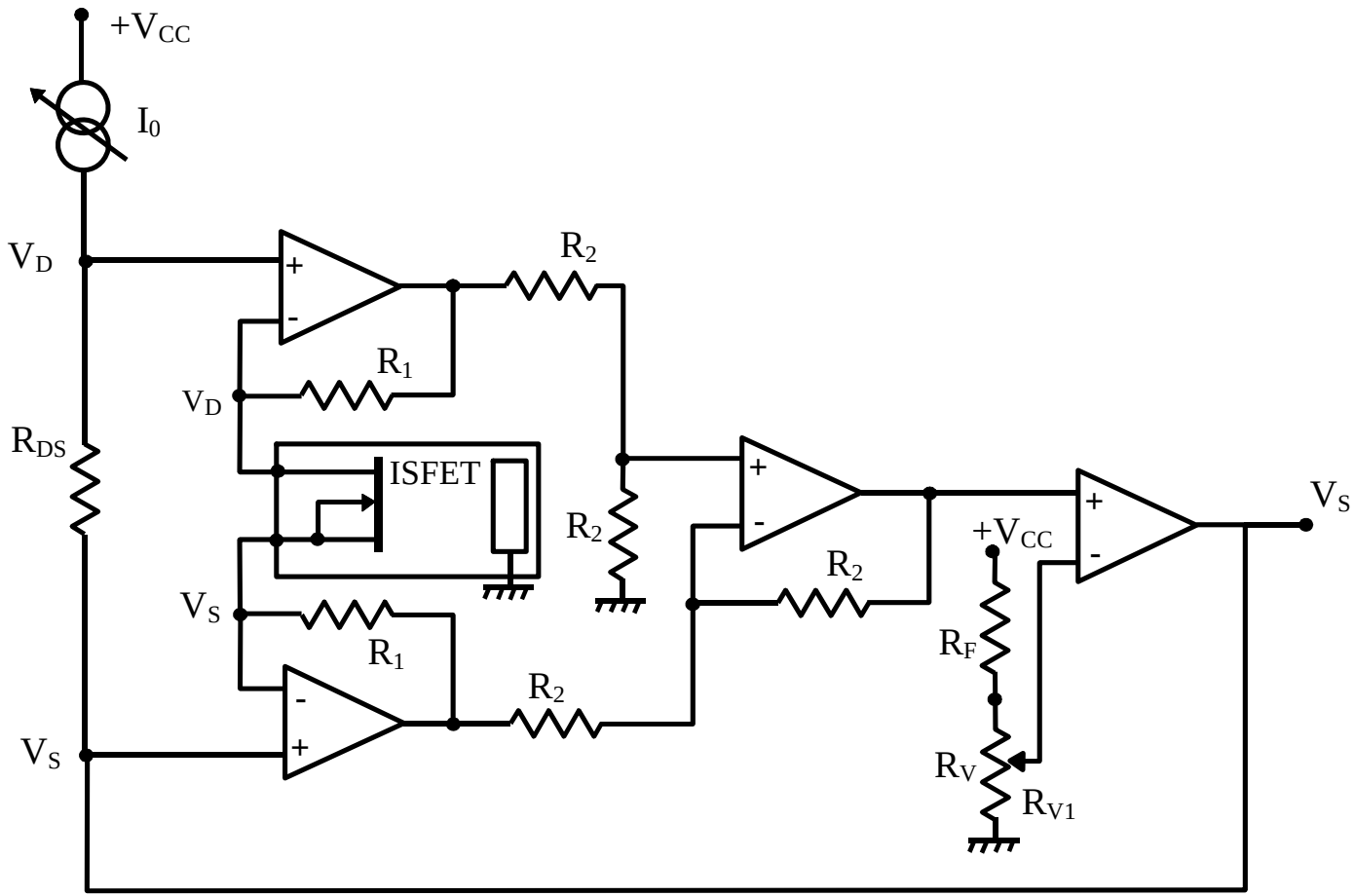

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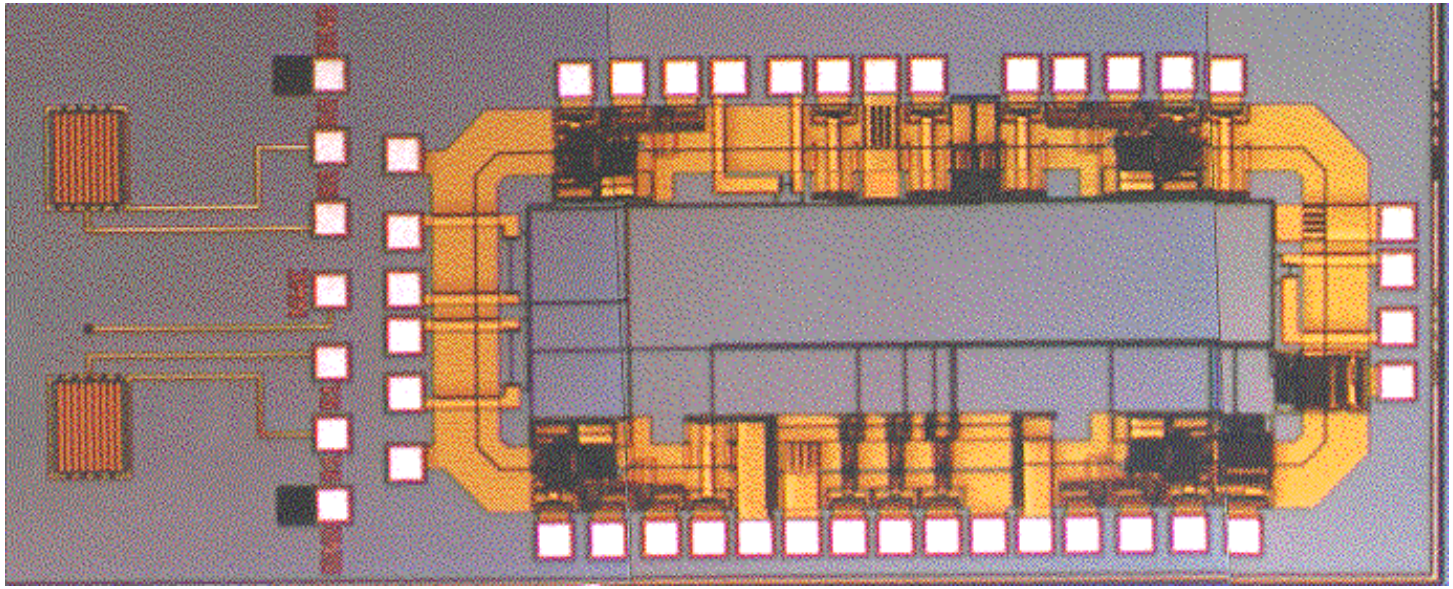

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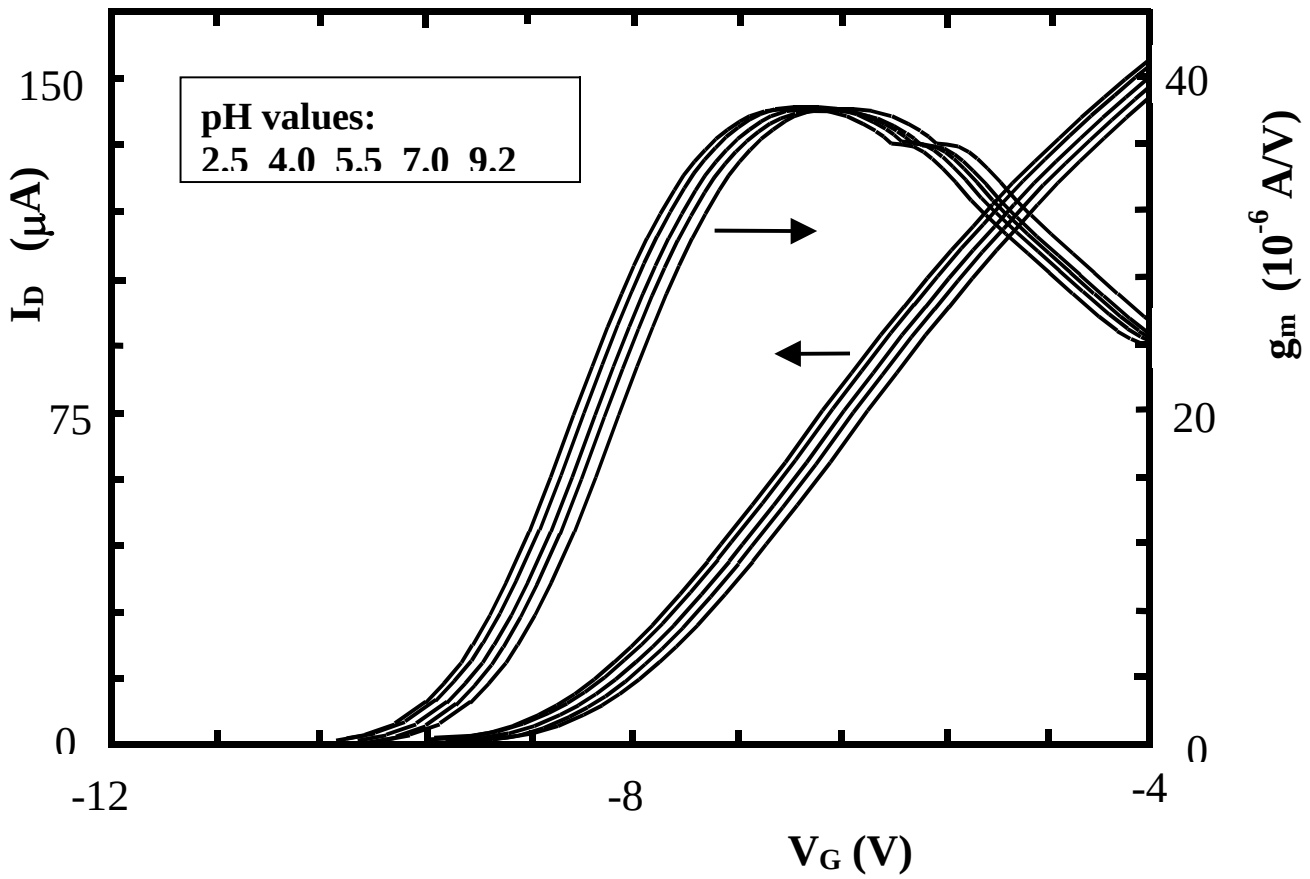

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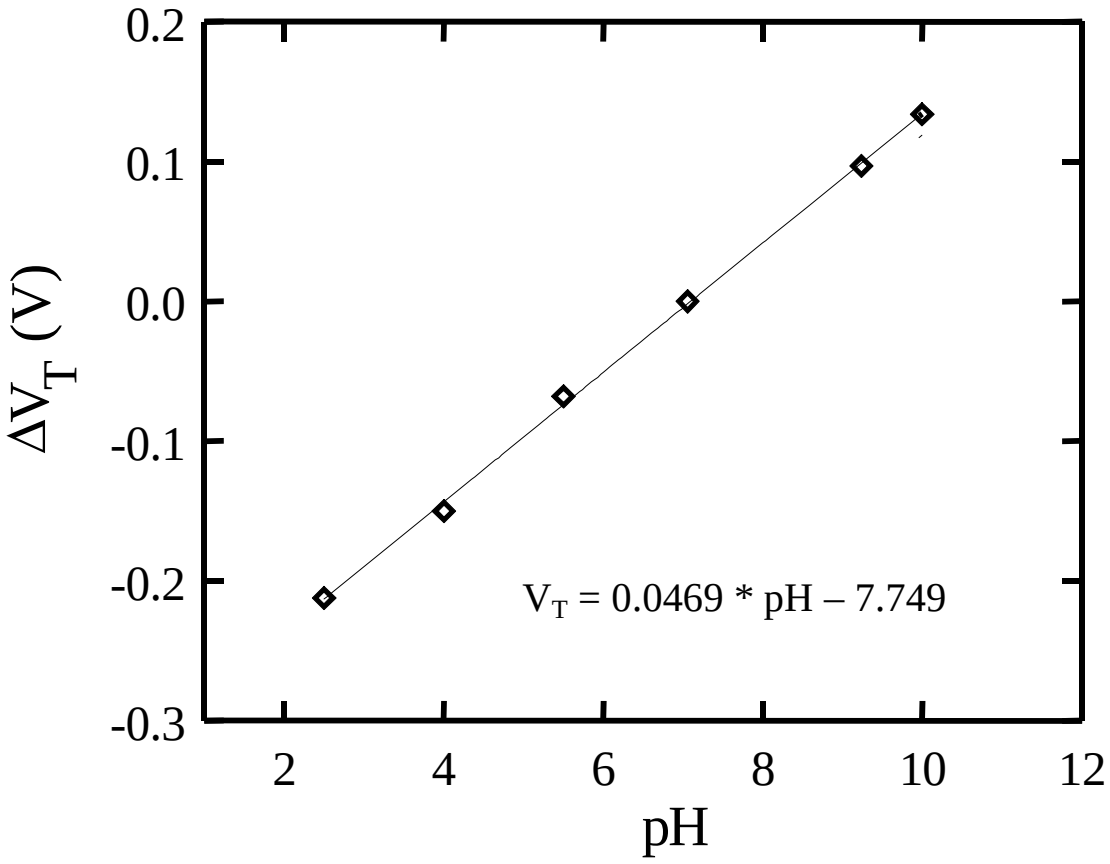

Bausells et al., Fig. 6