Improving the accuracy of RF alternate test using multi-V_{DD} conditions: application to envelope-based test of LNAs

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***Abstract*—This work demonstrates that multi-V_{DD} conditions may be used to improve the accuracy of machine learning models, significantly decreasing the prediction error. The proposed technique has been successfully applied to a previous alternate test strategy for LNAs based on response envelope detection. A prototype has been developed to show its feasibility. The prototype consists of a low-power 2.4GHz LNA and a simple envelope detector, integrated in a 90nm CMOS technology. Post-layout simulation results are provided to verify the functionality of the approach.**

I. Introduction

Nowadays, advances in RF CMOS technologies have enabled the integration of complete transceivers in a single chip, which provides a significant reduction in production cost. However there is a simultaneous increase in the cost of testing and diagnosing these devices. Their diverse specifications and high operating frequency, as well as the large impact of process variations in current deep submicron technologies, make necessary extensive tests and dedicated high-frequency test equipment. RF testing exhibits the same difficulties present in analog testing, but adding the problem of handling high-frequency signals. That is, RF testing is based on functional characterization, while fault-model-based tests, very successful in the digital test domain, are difficult to standardize in the RF field since each circuit type demands its own custom fault model.

Reducing RF test complexity and cost is still an open research topic that has been addressed in a number of different approaches. Recent work in this area includes defect modeling and failure diagnosis [1], [2], alternate test [2]–[5], DfT and BIST techniques [6]–[8], etc.

In particular, the combination of BIST techniques with the statistical analysis of alternate test seems to be a promising solution to mitigate most RF test drawbacks. On one hand, moving some of the testing functions to the device under test (DUT) would reduce test equipment cost, and eliminate the problem of transporting high-frequency test signals. On the other hand, alternate test strategies take advantage of advanced statistical tools to find correlations between a reduced number of observables (signatures), and the diverse DUT specifications, thus reducing the number of necessary test measurements and configurations.

However, although statistical tools are very powerful, they do not solve the test problem. Knowledge and experience are still needed to propose the best input space to feed these statistical tools. Thus, finding an appropriate set of signatures to extract meaningful models is usually a matter of creativity based on a precise knowledge of the DUT. This work proposes a simple method that can be used to improve the accuracy of alternate test at almost no extra engineering cost. It takes advantage of the variation of the DUT performance under multiple power conditions to add an extra layer of information to the input space of observables. In order to show the feasibility of the proposed technique, it is applied to a test strategy for LNAs, previously published by the authors, based on ensemble learning of digital envelope signatures [5].

This paper is organized as follows. Section II describes the theoretical basis of our proposal. Then Section III presents an application example. Section IV discusses some relevant experimental results to validate the proposal. Finally, Section V summarizes the main contributions of this work.

II. Theoretical basis

Testing a circuit under multiple power supply conditions is not new. Even during its design stage a circuit is simulated under different power supplies, V_{DD}, to assure its functionality in the technology process corners. The use of Multi-V_{DD} and V_{DD} ramping have been also explored as a reliable way of detecting defects in analog and RF circuits [9]–[11]. In this work we will show that performing classical alternate test strategies under multiple power supply conditions has the potential to significantly improve the accuracy of the test results at a low added cost.

A. Alternate test under multiple power supply conditions

Let us consider the set of performance specifications, $\mathbf{p} = [p_1, p_2, ..., p_k]$, of a certain DUT, and let $\mathbf{s} = [s_1, s_2, ..., s_m]$ be a set of signatures corresponding to the same DUT, where $\mathbf{p}$, and $\mathbf{s}$ belong to the space of possible specification sets, P^k, and to the space of possible signature sets, S^m, defined by process variations, respectively. Alternate test strategies use statistical processing to find a mapping function f defined as $f : S^m \longrightarrow P^k$ that verifies:

$$\|f(\mathbf{s}) - \mathbf{p}\| \to 0 \tag{1}$$

for each $\mathbf{s} \in S^m$ and $\mathbf{p} \in P^k$. Let us assume as hypothesis that such a function f exists, and let us now consider the measurement of the set of observables $\mathbf{s}$ under a different power supply. In a first order approximation, the supply variation will affect each signature in $\mathbf{s}$ as,

$$s_{i\Delta} \simeq s_i + \frac{\partial s_i}{\partial V_{DD}} \Delta V_{DD} \tag{2}$$

where $s_{i\Delta}$ corresponds to signature s_i measured under power supply $V_{DD} + \Delta V_{DD}$, and V_{DD} is the nominal power supply of the DUT. Equation (2) can be expanded as,

$$s_{i\Delta} \simeq s_i + \sum_{j=1}^{k} \frac{\partial s_i}{\partial p_j} \frac{\partial p_j}{\partial V_{DD}} \Delta V_{DD} \tag{3}$$

Given that the $k \times m$ matrix $\left[\frac{\partial s_i}{\partial p_j}\right]$ has to be different from the $k \times m$ null matrix by our initial hypothesis (that is, mapping function f exists), in the case that the sensitivity vector $\left[\frac{\partial p_1}{\partial V_{DD}}, ..., \frac{\partial p_k}{\partial V_{DD}}\right]$ is different from the null vector, then signature set $\mathbf{s_\Delta} = [s_{1\Delta}, ..., s_{m\Delta}]$ contains functional information about the sensitivity of the DUT specifications to changes in its supply voltage.

Let S^m_Δ be the space of possible signature sets defined by process variations and measured under supply $V_{DD} + \Delta V_{DD}$. Space S^m_Δ can be used to complement the functional information about the DUT contained in S^m in such a way that a new mapping function, f_Δ, can be defined as $f_\Delta : S^m \cup S^m_\Delta \longrightarrow P^k$. If we compare mapping functions f and f_Δ, given that the space of observables $S^m \cup S^m_\Delta$ contains more information about the DUT behavior than the space S^m alone, it should be clear that,

$$\|f_\Delta(\mathbf{s}, \mathbf{s_\Delta}) - \mathbf{p}\| \leq \|f(\mathbf{s}) - \mathbf{p}\| \tag{4}$$

for each $\mathbf{s}, \mathbf{s_\Delta} \in S^m \cup S^m_\Delta$ and $\mathbf{p} \in P^k$. That is, as a result of measuring under different supply conditions, the mapping model may be improved, but, interestingly, it cannot degrade.

B. Some metrics for measuring the quality of mapping models

Obviously, the particular cases that verify inequality (4) under a strictly less condition, are of great interest in the field of test. Under these circumstances, the mapping models are improved by repeating the measurement at different supply voltages, at the cost of increasing test time but without any significant changes to the hardware or test configuration. Nevertheless, finding an *a priori* analytical criterion to distinguish this situation is beyond the scope of this paper. Instead of that, we propose some simple metrics to compare, *a posteriori*, the quality of the mapping functions before and after stressing the DUT.

Comparing the performance of regression models is not always an easy task. The standard deviation of the estimation error is a straightforward metric of the quality of a mapping model, but it cannot be interpreted independently from the measurement. The standard deviation of the relative error could be seen as a good alternative, but it is also highly misleading. For instance, if the performance under consideration is close to zero the relative error will be high, even if the absolute precision is good. In the same way, if the performance under consideration is large in average the relative error will appear to be small, even if the estimation is not very accurate.

For these reasons, we proposed in [5] the following Figure Of Merit (FOM) for model-based test,

$$FOM = \sqrt{\frac{\sum_{i=1}^{N_s} \left(Y_{actual,i} - \bar{Y}_{actual}\right)^2}{\sum_{i=1}^{N_s} \left(Y_{pred,i} - Y_{actual,i}\right)^2}} \tag{5}$$

where N_s is the number of tested circuits, $Y_{pred,i}$ is the performance of circuit i predicted by the model, and $Y_{actual,i}$ is the real performance of circuit i. The hat symbol stands for the mean value, as usual.

We propose this FOM as a way to capture and evaluate the difference between the performance predicted by a model for a set of tested circuits, and the actual performance of the circuits. If the estimations are good, that is, if the predicted performances are close to the actual ones, the FOM will tend to infinite. On the other hand, if there is no clear correlation between signatures and performance figures, a well-built model will usually output the mean value of the data set, and hence the FOM will tend to unity. This FOM actually measures the improvement of the proposed model over the information inherently present in the data, being this information the variation range of the data. Thus, if the data variation range is small, even a very good model will not improve much the prediction, and the FOM would remain close to unity.

III. Case study

The previous discussion is completely general, and can thus be applied to any alternate test approach. Indeed, it has the potential to improve many already published alternate test strategies. In order to show the feasibility of this approach, we have applied it to the alternate test of a LNA designed in a 90nm CMOS technology. In particular, our case study is the alternate test strategy published by the authors in [5]. Our goal is to show that multi-V_{DD} conditions will improve the accuracy in this case study, while using the same set of observables and the same statistical tools. For the sake of completeness, this section describes briefly the test strategy in [5], and presents the DUT design. The sensitivity of the LNA performance specifications to power variations is also analyzed in detail.

A. Alternate test of LNAs through ensemble learning of on-chip digital envelope signatures

Figure 1a shows a standard two-tone test set-up traditionally used to characterize LNAs. The LNA is excited by two high-frequency tones closely spaced. The system response is then acquired and processed to characterize the DUT. Our

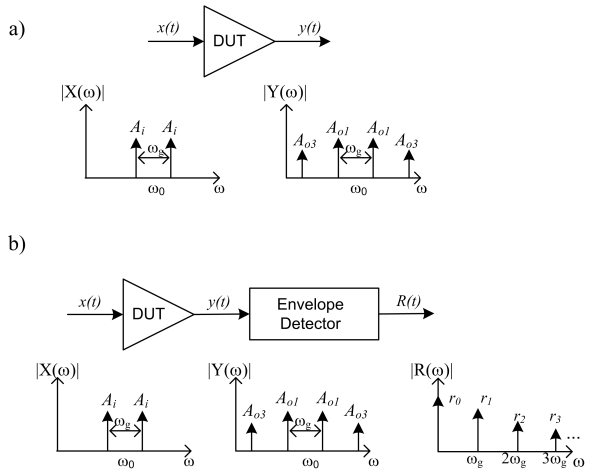

Fig. 1. a) Traditional two-tone test; b) Two-tone response envelope detection

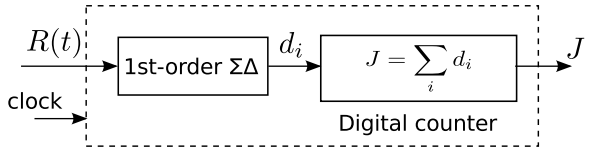

Fig. 2. Block diagram of the proposed signature extractor

approach, depicted in Fig. 1b is similar to the traditional scheme, but in this case the LNA response is driving an envelope detector. The envelope of the response signal is a low-frequency periodic function that contains information about the high frequency response of the DUT.

We propose the use of the area under a period of the response envelope curve as a simple test signature. This test signature can be easily computed in the digital domain using the signature extractor in Fig. 2. It consists of a 1^{st}-order $\Sigma\Delta$ modulator, which provides a simple A/D conversion of the envelope signal $R(t)$, followed by a digital counter that integrates the output bit-stream of the modulator. The state of the counter, J, is a digital measure of the area under the $R(t)$ curve. The set of computed signatures J are then processed using an ensemble learning model implemented using the ENTOOL Matlab toolbox [12], to extract the functional information about the DUT contained in the digital signatures.

Ensemble learning builds a mosaic model from a collection of statistical tools. It implements a routine that trains different models using cross-validation principles to deduce the expected prediction error. The final model is a weighted average of a subset of all the trained models. The different model families that are trained by the toolbox include polynomial models, nearest-neighbors models, diverse families of neural networks, and Multivariate Adaptive Regression Splines (MARS).

Results in [5] show that the proposed signature exhibits a good correlation with some important performance figures of LNAs, such as Gain, Noise Figure, 3^{rd}-order Input Intercept Point, and the scattering parameters S_{11}, and S_{22}.

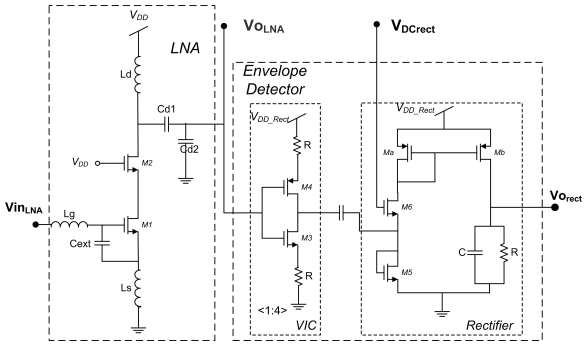

Fig. 3. Schematic of the designed LNA with built-in envelope detector

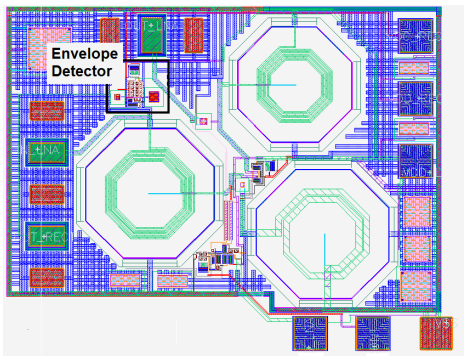

Fig. 4. Layout of the LNA with the envelope detector

B. Device under test: LNA with codesigned envelope detector

Our test vehicle is a LNA design that complies with the IEEE 802.15.4 standard. The schematic of the implemented demonstrator is depicted in Fig. 3 (LNA bias circuitry is not shown for simplicity), while Fig. 4 shows the layout of the complete design. It comprises a CMOS LNA codesigned together with an envelope detector in a 90nm CMOS technology. It occupies an area of 760μm $\times$ 700μm, excluding pads.

The LNA is a single-ended design with inductive source degeneration. It has been adapted to load and source impedances of 50Ω, and has a power consumption of 1.44mW for a supply voltage of 1.2V. Table I summarizes its main performance characteristics obtained by post-layout simulations.

The envelope detector has been adapted from [13]. It is formed by a voltage-to-current converter (VIC) followed by an AC-coupled half-wave current-mode rectifier with a passive low-pass output filter. It features an independent power supply to be turned off when test is not performed, and drains a mean current below 300μA from a 1.2V supply when operating at 2.4GHz.

TABLE I
LNA NOMINAL PERFORMANCE FIGURES

Specification	Value	Specification	Value
Gain (dB)	12.4	S_{11} (dB)	-24.9
NF (dB)	3.65	S_{22} (dB)	-10.5
IIP3 (dBm)	-1.40	S_{12} (dB)	-26.4

C. Sensitivity of the LNA performance to power supply variations

A necessary condition for the application of the proposed technique is that the sensitivity of the target specifications to power supply variations has to be different from zero. The following discussion, based on analytical results in [14], explores these sensitivity coefficients for the selected DUT and its specifications.

Gain: The gain, G, of the LNA in Fig. 3 can be expressed as

$$G = g_{m1} Q_{in} Z_{out}/2 \tag{6}$$

where g_{m1} is the transconductance of transistor M1, Q_{in} is the LNA quality factor, and Z_{out} is its output impedance seen from node V_{OLNA}. Hence, the sensitivity of the LNA gain to power supply variations can be easily expressed as,

$$\frac{\partial G}{\partial V_{DD}} = \frac{Q_{in} Z_{out}}{2} \frac{\partial g_{m1}}{\partial V_{DD}} \neq 0 \tag{7}$$

It should be clear that this derivative is not zero since g_{m1} depends on the voltage overdrive of transistor M1.

Noise characteristics: The noise factor, F, of the LNA under study can be approximated as

$$F \approx 1 + \frac{\gamma}{\alpha} \frac{1}{4 R_s g_{m1} Q_{in}^2} \tag{8}$$

where γ and α are technological constants, and R_s is the source resistance. Again, the corresponding sensitivity coefficient can be derived as

$$\frac{\partial F}{\partial V_{DD}} = \frac{-\gamma}{4 \alpha R_s Q_{in}^2 g_{m1}^2} \frac{\partial g_{m1}}{\partial V_{DD}} \neq 0 \tag{9}$$

which, again, is different from zero.

3^{rd} order intercept point: For the LNA in Fig. 3, the 3^{rd} order intercept point occurs for an input amplitude [14]

$$A_{IP3} = \sqrt{\frac{4}{3} \frac{V_{ov1}}{\Theta} \left(2 + \Theta V_{ov1}\right) \left(1 + \Theta V_{ov1}\right)^2} \tag{10}$$

where V_{ov1} corresponds to the voltage overdrive of transistor M1, and Θ is a technology dependent parameter defined as the inverse of the voltage where the transition between strong inversion and velocity saturation occurs. It should be clear from (10) that A_{IP3} is an increasing function of V_{ov1}, hence, it is straightforward to conclude that $\frac{\partial A_{IP3}}{\partial V_{DD}} \neq 0$.

Scattering parameter S_{11}: this parameter accounts for the voltage reflection at the input port of the LNA. It is related to the input impedance of the amplifier, Z_{in}, given by

$$Z_{in} = \frac{g_{m1} L_s}{C_{gs1} + C_{ext}} + s(L_s + L_g) + \frac{1}{s\left(C_{gs1} + C_{ext}\right)} \tag{11}$$

where C_{gs1} is the gate to source capacitance of transistor M1. The sensitivity of the input impedance to supply variations can be easily approximated as

$$\frac{\partial Z_{in}}{\partial V_{DD}} = \frac{L_s}{C_{gs1} + C_{ext}} \frac{\partial g_{m1}}{\partial V_{DD}} \neq 0 \tag{12}$$

Given that scattering parameter S_{11} is directly related to Z_{in}, it can be concluded that $\frac{\partial S_{11}}{\partial V_{DD}} \neq 0$.

Scattering parameter S_{22}: This scattering parameter is a function of the output impedance of the LNA, Z_{out}. It can be proved that, in a first-order approximation, Z_{out} is independent from the power supply voltage [14], so in this case the sensitivity coefficient $\frac{\partial S_{22}}{\partial V_{DD}} = 0$. Hence, no improvement is expected for the mapping model of this performance due to the application of different power supplies.

Scattering parameter S_{12}: According to the results in [5], the considered signature J is not correlated to S_{12}, or, recalling the formalism in (3): $\frac{\partial J}{\partial S_{12}} = 0$, where J and S_{12} are the considered signature and performance, respectively. Then, whether or not this performance is sensitive to power supply changes, it would not be captured by the ensemble learning model, and hence the mapping model corresponding this parameter should not change.

IV. Results and discussion

The DUT described in the previous section has been fabricated and will be characterized soon. Unfortunately, like most academic institutions we do not have access to industrial volumes. The closest to experimentation was thus to perform Monte Carlo simulation on the extracted layout view.

A set of 200 instances of the DUT was obtained by post-layout Monte Carlo simulation. Out of the 200 instances, 150 were used to train the ensemble model, while 50 randomly chosen instances were taken apart as test set to verify the accuracy of the prediction. Model training was performed firstly under nominal power supply, for comparison, and it was repeated under different power supply conditions. The supply voltages of LNA and envelope detector (labelled V_{DD} and V_{DDRect} in Fig. 3, respectively) are connected together. A trade-off arises in the choice of $|\Delta V_{DD}|$: it has to be high enough to maximize the change in the selected DUT specifications, but it has to be sufficiently low for not turning off the DUT (if $\Delta V_{DD} < 0$), or producing a permanent damage to the DUT (if $\Delta V_{DD} > 0$). In this particular example, we have chosen two power conditions according to this trade-off: $\Delta V_{DD} = +10\%$, and $\Delta V_{DD} = -10\%$. In any case, it is important to notice that a precise value of ΔV_{DD} is not important, it only has to be the same for all the instances.

A set of signatures J was extracted in the same test conditions than [5], and ensemble models were trained under nominal and stressed supplies for Gain, Noise Figure, 3^{rd}-order input referred intercept point (IIP3), and scattering parametes S_{11}, S_{12}, and S_{22}. Table II presents the obtained standard deviation of the estimation errors for the test set, σ_{error}, and the computed model FOM (5), for both nominal supply and multi-V_{DD} test conditions. Figure 5 shows a direct comparison of the obtained FOMs, and Fig. 6 shows the variation in σ_{error} due to the application of the proposed multi-V_{DD} technique. As predicted, when power supply variation is introduced, the

TABLE II
MODEL PREDICTION ERROR FOR THE SPECIFICATIONS

Specs	Nominal power supply σ_{error}	FOM	Multi-V_{DD} conditions σ_{error}	FOM
Gain	0.32 dB	3.90	0.20 dB	6.11
NF	0.097 dB	2.98	0.074 dB	3.76
IIP3	0.90 dBm	2.17	0.60 dBm	3.06
S_{11}	2.09 dB	1.47	1.62 dB	1.87
S_{22}	0.96 dB	1.52	0.95 dB	1.51
S_{12}	0.311 dB	1.13	0.312 dB	1.12

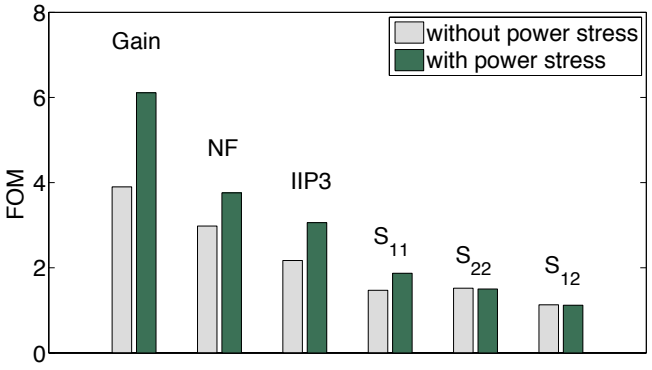

Fig. 5. FOM variation under multi-V_{DD} conditions

figure of merit increases significantly for Gain, NF, IIP3, and S_{11} models, while it remains practically unchanged for S_{22} and S_{12} models. There is also a significant reduction, around a 30%, in the estimation error for Gain, NF, IIP3, and S_{11} estimations, while the estimation error for S_{22} and S_{12} remains constant. In order to make a direct comparison, Fig. 7 gathers the scatterplots of the estimated versus measured values for Gain, NF, IIP3, and S_{11} specifications, obtained under nominal supply (left side plots) and multi-V_{DD} conditions (right side plots). Dot markers stand for the complete set of samples–both training and test sets–and triangle markers highlight the samples of the test set.

The obtained results are in a good agreement with the theoretical results discussed in the previous section. Thus, it was demonstrated that Gain, NF, IIP3, and S_{11} parameters have a non-zero sensitivity to power supply variations, so different power conditions add an extra layer of information to the signature set that is extracted by the ensemble learning models and improve the estimations. On the other hand, as it was anticipated, the estimations of parameters S_{12} and S_{22} do not improve, due to two different causes. Parameter S_{22} is not sensitive to power variation, hence no improvement in its estimation was expected. Parameter S_{12} is not correlated to the signature set, as it is clearly shown by its close to unity associated FOM, which also explains why its estimation does not improve either. Also as predicted, the estimations of S_{22} and S_{12}, do not degrade due to the application of power variations, but remain constant.

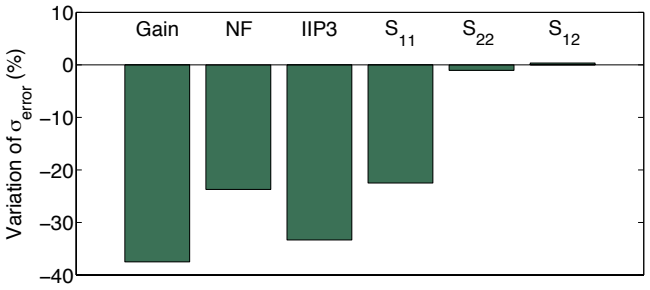

Fig. 6. Relative variation of σ_{error} under multi-V_{DD} conditions

V. CONCLUSIONS

Alternate test is undoubtedly an interesting path to mitigate the ever increasing cost of testing embedded analog, mixed-signal and RF blocks. In this paper, we have presented a simple technique, based on varying the power supply of the DUT, to improve the quality of alternate test techniques. It has the potential to improve many existing test strategies at a very low cost. In order to assess the relevance of statistical regressions, we have also proposed a new Figure of Merit for alternate test that measures the amount of additional information that a regression is able to extract from the original data. As a practical example, the proposed methodology has been successfully applied on an envelope-based test for RF LNAs, achieving a significant improvement of the mapping models for Gain, NF, IIP3, and S_{11} specifications.

ACKNOWLEDGMENT

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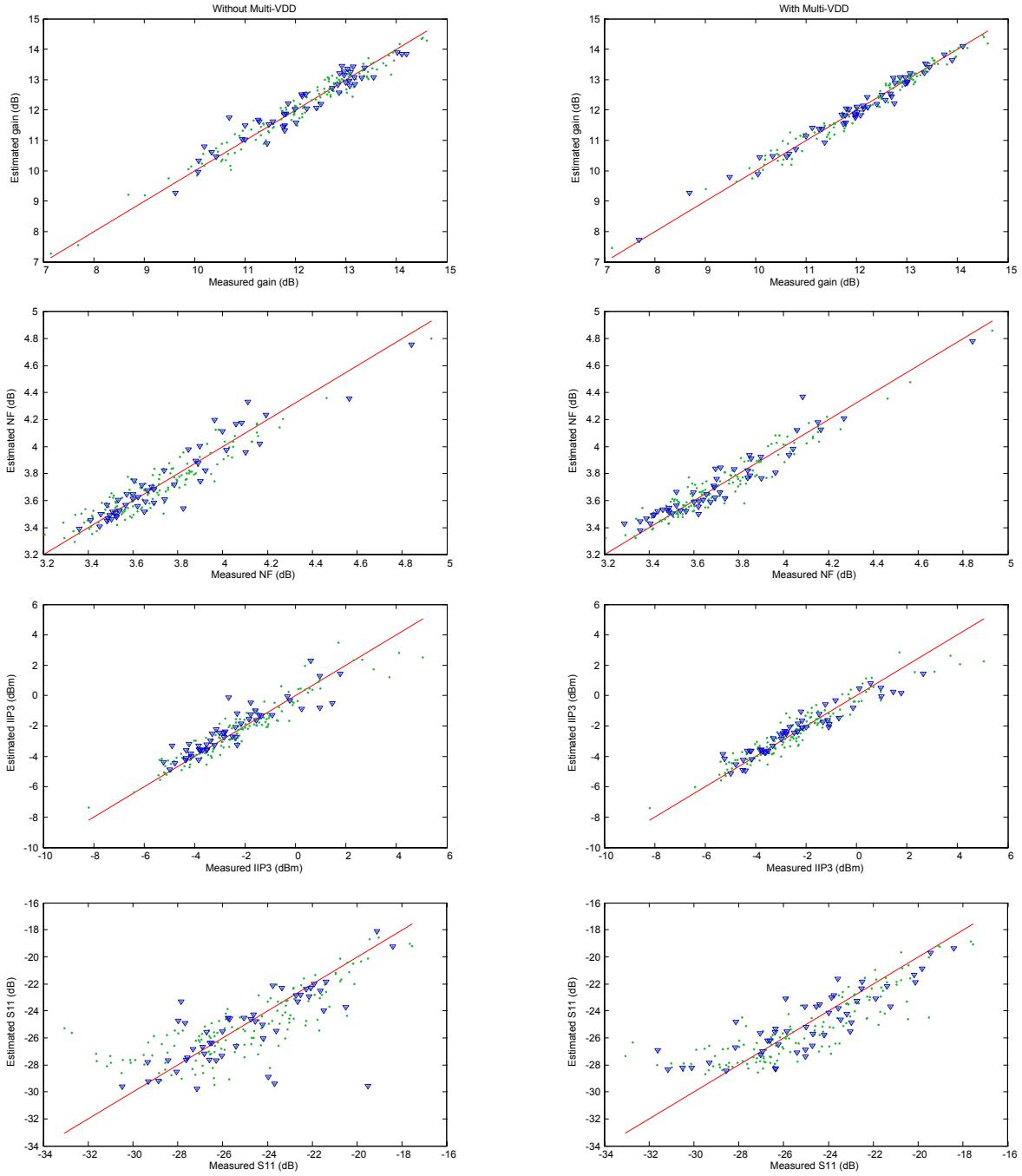

Fig. 7. Scatterplots of estimated versus measured performance specifications

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