GaN metal-oxide-semiconductor field-effect transistor inversion channel mobility modeling

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Lateral *n*-channel enhancement-mode GaN metal-oxide-semiconductor (MOS) field-effect transistors and lateral capacitors have been fabricated on a *p*-type epi-GaN substrate semiconductor and electrically characterized at different temperatures. A clear positive behavior of the inversion channel mobility with temperature has been obtained. A physics-based model on the inversion charge and charge trapped in interface states characteristics has been used to investigate the temperature dependence of the inversion MOS channel mobility. The field-effect mobility increase with temperature is due to an increase in the inversion charge and a reduction in the trapped charge for a given voltage gate. Then, for larger gate bias and/or higher temperatures, surface roughness effects become relevant. The good fitting of the model with the experimental data leads us to consider that the high density of charged acceptor interface traps together with a large interface roughness modulates the channel mobility due to scattering of free carriers in the inversion layer. A closed form expression for the experimental inversion MOS channel mobility is proposed.
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I. INTRODUCTION

Nowadays, the most widely used power switching devices are the silicon (Si) power enhancement-mode metal-oxide-semiconductor field-effect transistor (MOSFET) and the MOS controlled insulated gate bipolar transistor due to their well-known advantages. However due to the limitations of these Si devices for high temperature, high frequency, and high power applications, wide bandgap semiconductors such as gallium nitride (GaN) (Ref. 1) and silicon carbide (SiC) (Ref. 2) have attracted much interest as potential candidates to extend the microelectronic revolution. The use of GaN devices for high switching speed and high power applications can provide many benefits for the end-user including low switching losses, increased efficiency, and improved temperature performance.[3] For these applications, enhancement-mode GaN MOSFETs have the key advantages of normally off operation and low leakage current.[4] However, inversion MOS based GaN MOSFET currently exhibits modest inversion channel mobility. As in the case of SiC,[5] the key issue relating to the performance of inversion MOS devices is the quality and reliability of the gate dielectric, closely related to a large insulator/semiconductor interface state density. In this sense, a very promising structure for an improved GaN power switch could be the hybrid MOS–high electron mobility transistors (HEMTs).[6] This hybrid MOS-HEMT concept is based in the incorporation of an AlGaN/GaN heterostructure[7] into the reduced surface field region of lateral enhancement-mode GaN MOSFETs. A hybrid MOS-HEMT has the advantage of both, the MOS gate control and the high mobility Two Dimensional Electron Gas (2DEG) (Refs. 8 and 9) in the AlGaN/GaN drift region.

Power converter designers planning to use those GaN-based switching devices require accurate device models, particularly the temperature dependence of device behavior and power dissipation. Nevertheless, enhancement-mode GaN MOSFET device reports are scarce in the literature.[10–12] This is due to specific GaN MOSFET difficulties including the starting material quality, the surface preparation, and the lack of native oxide. Various gate dielectric materials have been used, such as SiO_2,[12] MgO,[13] and $Ga_2O_3(Gd_2O_3)$.[14] Furthermore, there is a relevant lack of understanding of the physics of such devices and, in particular, studies concerning device operation at elevated temperatures. In this paper, we try to bring a more physical insight into the inversion MOS channel mobility behavior of enhancement-mode GaN MOSFET by means of physics-based modeling. First, we report the fabrication of an enhancement-mode lateral GaN MOSFET with deposited SiO_2. Then, the effect of temperature on the field-effect mobility of the fabricated device is investigated. Next, in order to explain the obtained results, we have used an inversion mobility physics-based model that includes parameters for the Coulomb scattering at charged interface traps and free carrier screening along with surface roughness analysis. The results obtained from this model are compared with the experimental data.

II. EXPERIMENTAL DETAILS

Enhancement-mode GaN MOSFETs and capacitors have been fabricated on a *p*-type (0001) 2*H*-GaN epilayer grown on a *c*-plane sapphire substrate, supplied by TDI Inc. The *p*-epilayer was 6 μm thick Mg doped ($N_a=1.9\times10^{17}$ cm^{-3}). A high resistivity Zn compensated buffer layer was grown between the sapphire substrate and the *p*-layer. After solvent clean steps, a Si^+ implantation at 160 keV with a dose of 3.0×10^{15} cm^{-2} was performed to define source and drain regions. The activation annealing process of the

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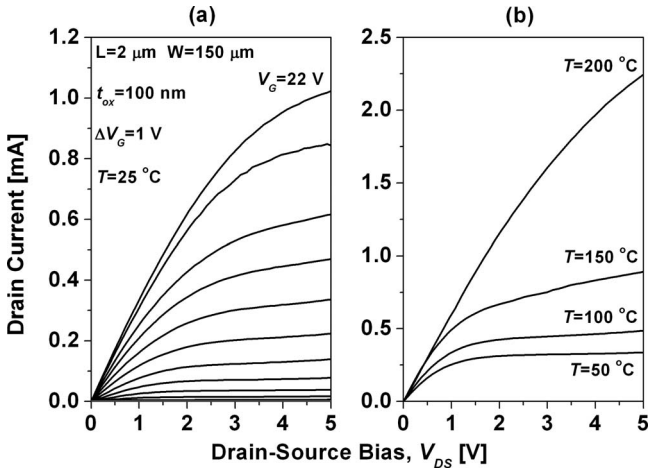

FIG. 1. Drain current vs drain voltage, (a) varying gate voltage, (b) varying temperature.

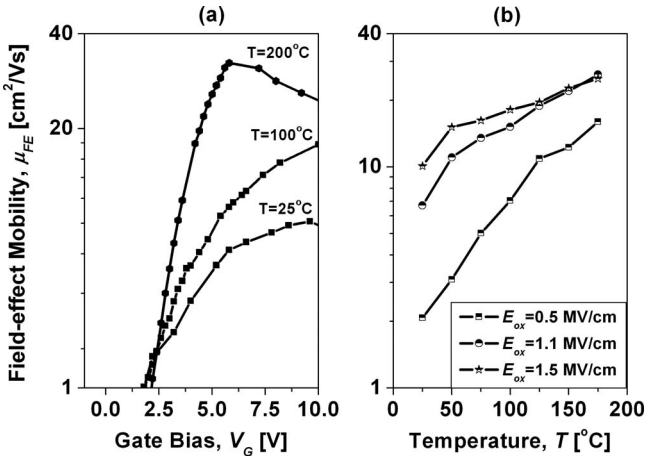

FIG. 2. (a) Temperature influence of the experimental field-effect mobility vs gate voltage. (b) Field-effect mobility vs temperature (for different insulator electric fields).

Si-implanted GaN was carried out with a 60 nm thick SiO_2 cap protection layer deposited by plasma-enhanced chemical vapor deposition (PECVD). The postimplantation annealing consisted of a two-step method: first at 1000 °C for 1 min and then at 1150 °C for 10 s. After removing the protection cap layer using SiO etch, a chemical Radio Corporation of America Clean (RCA Clean) based cleaning process was performed. A 100 nm thick (t_{ox}) SiO_2 layer was then deposited by PECVD as a gate oxide and annealed at 750 °C for 9 min in Ar ambient. Titanium and aluminum were then deposited by sputtering and patterned by lift-off. The source and drain contacts were annealed at 700 °C for 90 s in Ar ambient. The contact resistance of the source and drain electrodes was determined[15] to be lower than 10^{-5} Ω cm^2. MOSFET characterization was performed with a set of Keithley units. Lateral *p*-type MOS capacitors were also fabricated to determine the density of interface traps within the bandgap close the valence band. The area of the gate electrode was 4.5 $\times 10^{-3}$ cm^2. Capacitance-voltage measurements were performed in dark using a Keithley K82 system.

III. EXPERIMENTAL RESULTS

Figure 1(a) shows the drain current-voltage characteristics of the lateral GaN MOSFET with a channel length (L) of 2 μm and a channel width (W) of 150 μm at room temperature for different gate voltages. The output current is around 1 mA for a gate voltage of 22 V. The drain current (I_D) as a function of gate voltage (V_G) was also measured at constant drain voltage (V_D) of 0.5 V. From these characteristics, the threshold voltage V_{th} was estimated by extrapolating the linear region down the voltage axis to be about −2.5 V. The direct drain-source characteristics were measured in the temperature range of 25–200 °C. Figure 1(b) shows the drain characteristics at different temperatures for a gate voltage of 14 V. The current increased significantly with temperature, in contrast to other reported results[10,11] where high stability operation up to 200 °C was observed. The field-effect mobilities of the fabricated MOSFETs have been evaluated from the derivation of the transconductance curve using

$$\mu_{\mathrm{FE}} = \frac{L}{WC_{\mathrm{ox}}V_D}\left(\frac{\partial I_D}{\partial V_G}\right) = \mu_{\mathrm{inv}}\left[1+\frac{Q_{\mathrm{inv}}}{\mu_{\mathrm{inv}}}\frac{d\mu_{\mathrm{inv}}}{dQ_{\mathrm{inv}}}\right]\left[1+\frac{dQ_{\mathrm{trap}}}{dQ_{\mathrm{inv}}}\right]^{-1}, \quad (1)$$

where C_{ox} is the insulator capacitance per unit area. For MOSFETs with a large density charge trapped at interface states (Q_{trap}), the values of field-effect mobility μ_{FE} will not correspond to the true inversion mobility μ_{inv} due to the presence of additional interface charge. Quantitatively, this correction introduces small difference in the computation of μ_{FE} from μ_{inv},[16] where Q_{trap} and Q_{inv} are the trapped and the inversion charge per unit area, respectively. Figure 2 shows the field-effect mobility evolution with temperature. As it can be seen from Fig. 2(a), the field-effect mobility increases with V_G up to a certain gate bias, which depends on the temperature. The mobility increases more than three times [Fig. 2(b)] for operation at 200 °C compared to room temperature for an effective insulator field of 0.5 MV/cm. The insulator field is defined by $E_{\mathrm{ox}}=V_G/t_{\mathrm{ox}}$, where t_{ox} is the oxide thickness. Since the bulk mobility decreases when temperature increases (see next section), other mechanisms have to be responsible of this behavior.

IV. DESCRIPTION OF THE MODEL

A. Inversion channel mobility model

The bulk carrier mobility (μ_B) for any semiconductor is a function of the temperature and doping concentration. The bulk mobility can be described by the well-known empirical derived formulation of Caughey–Thomas

$$\mu_B(N_A,T) = \mu_0 + \frac{\mu_{\max}(T)-\mu_0}{1+(N_A/C_r)^{\alpha 1}}, \quad (2)$$

$$\text{with } \mu_{\max}(T) = \mu_{\max}\left(\frac{T}{300}\right)^{-\gamma}, \quad (3)$$

where N_A is the acceptor impurity concentration (in the case of a *p*-type semiconductor) and μ_0, $\mu_{\max}$, C_r, $\alpha 1$, and γ are

fitting parameters.[17] The mobility of carriers in the inversion channel of a MOSFET device is always a part of the carrier mobility in the semiconductor bulk. This is due to a collection of surface effects in the semiconductor/insulator interface. Lombardi *et al.*[18] proposed a physics-based model where carrier mobility is described by the sum of several mobility contributions following the Matthiessen's rule:

$$\mu_{\text{inv}} = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{\text{AC}}} + \frac{1}{\mu_{\text{SR}}} + \frac{1}{\mu_C} \right]^{-1}. \tag{4}$$

The widely accepted model consisting of the first three terms in Eq. (4) provides a good description of channel mobility for silicon MOSFETs. There, μ_{AC} is the carrier mobility limited by the acoustic phonons scattering, and μ_{SR} is the carrier mobility limited by surface roughness scattering.

1. Surface acoustic phonons

The surface acoustic phonons mobility coming from the quantized mode of vibration occurring in the crystal lattice is given by[18]

$$\mu_{\text{AC}}(E_\perp, T) = \frac{B}{E_\perp} + \frac{CN_A^{\alpha 2}}{TE_\perp^{1/3}}, \tag{5}$$

where B and C are two fitting parameters that allow adjusting the degree of mobility reduction due to the electric field normal to the current flow and temperature, respectively. The dependency of μ_{AC} on the impurity concentration is given by $\alpha 2$.

2. Surface roughness

Matsumoto and Uemura[19] reported a very simple and popular approximation for the surface roughness mobility,

$$\mu_{\text{SR}}(E_\perp) = \frac{\delta}{E_\perp^2}, \tag{6}$$

where $E_\perp$ is the perpendicular electric field and δ is a fitting parameter. Based on detailed numerical calculations of the surface-roughness-limited mobility, it has been demonstrated[20] that the exponential of the perpendicular electric field ($\alpha 3$) and δ are not independent of the surface quality and temperature. A more general formulation of the surface roughness linking the mobility value with the interface quality is given by

$$\mu_{\text{SR}}(E_\perp, T) = \frac{A(\Delta\Lambda)^{-2}}{(E_\perp/E_o)^{\alpha 3}} \left(1 - \frac{T}{T_o} \right), \tag{7}$$

where Δ is the root mean square (rms) surface roughness of the asperities and Λ is the correlation length. A, T_0, and E_0 are fitting parameters depending on the doping and the semiconductor material.

3. Interface traps Coulomb scattering

The classical Lombardi model ($\mu_{\text{inv}}^{-1} = \mu_B^{-1} + \mu_{\text{SR}}^{-1} + \mu_{\text{AC}}^{-1}$) is successfully used for modeling the channel properties of MOSFETs with a properly *passivated* insulator/semiconductor interface. There, the oxide and interfacial traps are negligible. These traps, when charged, are responsible for the disturbing Coulomb scattering of free carriers in the inversion layer. In a prior work,[21] we proposed a mobility model for describing the mobility degradation observed in MOSFET devices including Coulomb scattering effects at interface traps. This model assumes a fixed charge distribution of ionized traps on the interface treating the random spatial fluctuations of charge density as a quantum mechanics perturbation. The free carrier screening effect introduces the dependence on the inversion charge. An additional term is then included to account for the Coulomb scattering at interface traps μ_C,

$$\mu_C(E_\perp, T) = NT^{\alpha 4} \frac{[Q_{\text{inv}}(E_\perp, T)]^\beta}{Q_{\text{trap}}(E_\perp, T)}, \tag{8}$$

where N is proportionality constant, $\alpha 4$ a temperature coefficient, and β an empirical coefficient. In order to compute the field-effect mobility model [Eq. (4)] it is necessary to determine $E_\perp$ along with the trapped and inversion charges for each gate voltage at a given temperature, and this will be described in the next sections.

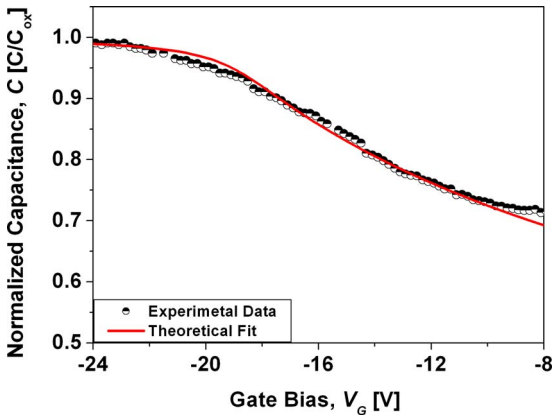

FIG. 3. (Color online) Normalized capacitance-voltage at 100 kHz.

B. GaN/SiO_2 MOS interface properties Q_{trap}

Figure 3 shows the high frequency C-V curve for a MOS capacitor with deposited SiO_2 on p-type GaN. The significant flatband shift suggests that fixed positive oxide charges are present in the deposited SiO_2 bulk or at the GaN/SiO_2 interface. From the C-V and conductance characteristics, it is possible to determine the interface state density (D_{it}). In this case, D_{it} has been extracted by means of Terman method.[22] This method is based on the quantification of the interface-trap-induced distortion on the experimental C-V when compared to a theoretical C-V curve (displayed in Fig. 4 for $N_A = 1.9 \times 10^{17}$ cm^{-3}). Solid points in Fig. 4 are the experimentally derived interface trap density within the bandgap. An interface state density close the valence band of 1.3×10^{12} cm^{-2} eV^{-1} has been extracted at $E_T - E_V = 0.25$ eV. Inversion carrier mobility will depend on the amount of charge trapped at these interface traps. For a continuous energy distribution of interface states, the trapped charge in the interface states may be approximated by[22]

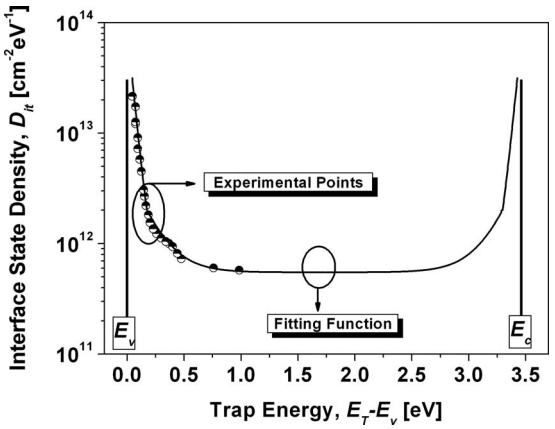

FIG. 4. Interface state density vs Fermi energy. Experimental data from *p*-type GaN capacitors with deposited SiO_2.

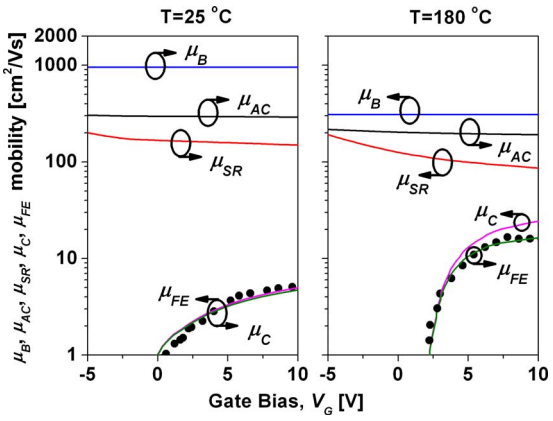

FIG. 5. (Color online) Simulated (solid lines) μ_B, μ_{AC}, μ_{SR}, μ_C, and μ_{FE} and experimental μ_{FE} (symbols) vs gate bias for 25 and 180 °C.

$$Q_{\text{trap}}(E_F) = \int_{E_i}^{E_F} D_{\text{it}}(E)dE, \tag{9}$$

where E_F is the surface Fermi level and E_i is the intrinsic level. As it can be seen from Fig. 4, the experimental D_{it} values increase significantly toward the valence band edge. For fitting that D_{it} distribution versus the trap energy E_T, we have used the following analytical function:

$$D_{\text{it}}(E_T) = \begin{cases} a_1 + a_2 e^{(E_V - E_T/\xi_1)}, & E_T - E_V > E_0 \\ b_1 + b_2 e^{(E_V - E_T/\xi_2)}, & E_T - E_V < E_0, \end{cases} \tag{10}$$

where a_1, a_2, b_1, b_2, ξ_1, and ξ_2 are parameters fitting the experimental interfacial trap spectra within the bandgap. E_V is the valence band energy. $E_0 = E_T - E_V = 0.15$ eV is an energy level chosen for describing the rapid increase in interface state density when approaching the valence band at the GaN/SiO_2 interface. The values of the fitting parameters are listed in Table I.

The fitting function for the D_{it} together with the experimental data is presented in Fig. 4. Here, D_{it} values near the conduction band are assumed to be symmetrical respect to the midgap. Traps are considered to be acceptors in the upper midgap region and donors in the lower midgap region.[21] This assumption of D_{it} band symmetry appears to underestimate somehow the D_{it} value near the conduction band.[23] The temperature dependence of the bandgap energy was taken from the expression[17] $E_G(T) = E_{G0} - \alpha_G[T^2/(T+\beta_G)]$, where E_{G0} is the bandgap energy at 0 K and α_G and β_G are experimental constants.

TABLE I. Interface traps simulation parameters values.

Parameter	Units	2*H*-GaN	References
D_{it} profile fitting parameters			
a_1	$cm^{-2}\,eV^{-1}$	5.1×10^{11}	This work
a_2	$cm^{-2}\,eV^{-1}$	4×10^{12}	This work
b_1	$cm^{-2}\,eV^{-1}$	3.45×10^{10}	This work
b_2	$cm^{-2}\,eV^{-1}$	8.55×10^{13}	This work
ξ_1	eV	0.160	This work
ξ_2	eV	0.040	This work
E_0-E_i	eV	0.69	This work
Bandgap vs T			
E_{G0}	eV	3.47	17
α_G	eV/K	7.7×10^{-4}	17
β_G	K	600	17

C. GaN charge sheet computation, V_G, $E_\perp$, and Q_{inv}

A charge sheet model[16] of the MOS system was used for calculating the dependence of the inversion layer charge density on Fermi energy E_F and gate voltage V_G, thus serving as a starting point for the description of current transport in MOS transistors. The model simplifies the calculation of inversion charge, assuming that the inversion layer is a charge sheet of infinitesimal thickness. The charge sheet model equations are also used to compute the average effective field in the inversion layer $E_\perp$ required to calculate μ_{AC} and μ_{SR}. The solution for Q_{inv}, for an arbitrary value of V_G, is rather unwieldy. To compute the inversion channel mobility versus gate voltage, it is simpler in practice to calculate values of Q_{inv}, Q_{trap}, $E_\perp$, and V_G for any arbitrary value of the Fermi potential u_S. The inversion charge can be simplified by the difference between the total space charge Q_{sc} and the charge within the depletion layer Q_{dep}. Analogously, the effective field at the interface could be determined with $E_\perp = \varepsilon_s^{-1}(Q_{\text{inv}}/2 + Q_{\text{dep}})$, where ε_s is the semiconductor dielectric constant. All the equations and variables used in the calculation of the inversion charge are detailed elsewhere.[24] The parameters used in the computation were $N_A = 2\times10^{17}$ cm^{-3}, $E_A - E_V = 0.2$ eV, $E_C - E_D = 0.1$ eV, $m_{d,e} = 0.2m_0$ (m_0 is the electron mass), $m_{d,h} = 1.5m_0$, $\varepsilon_s = 9.5$, $\varepsilon_{\text{ox}} = 3.9$, and $t_{\text{ox}} = 100$ nm.

V. DISCUSSION

The experimental and simulated field-effect mobility of the fabricated MOSFET is presented in Fig. 5 at 25 and 180 °C. The computed values for μ_B, μ_{SR}, μ_{AC}, and μ_C are depicted in this figure using the parameters detailed in Table II. In a semiconductor bulk, the two main carrier scattering mechanisms limiting the mean free path of carriers (at low electric fields) are ionized impurity and lattice scattering.[18] The effect of both mechanisms increases with temperature, and hence, μ_B diminishes with temperature. Analogously, the mobility due to surface acoustical phonon scattering (μ_{AC})

TABLE II. Model parameter values for the four terms: μ_B, μ_{SR}, μ_{AC}, and μ_C.

Parameter	Units	2*H*-GaN	References
Low field channel mobility			
μ_0	$cm^2/V\ s$	100	17, 25, and 26
C_r	cm^{-3}	3×10^{17}	17, 25, and 26
$\alpha1$		0.7	17, 25, and 26
μ_{max}	$cm^2/V\ s$	1600	17, 25, and 26
γ		3.0	17, 25, and 26
Acoustic phonon scattering			
B	cm/s	1.0×10^6	21 and 26
C	$K\ cm/s(V/cm)^{-2/3}$	3.23×10^6	21 and 26
$\alpha2$		0.0284	21 and 26
Surface roughness scattering			
A'	$cm^{4-\alpha3}\ V^{\alpha3-1}/s\ K$	1570	This work
$\alpha3$		2.3	This work
T_0	K	700	This work
Coulomb scattering			
$\alpha4$		1	21
β		1	21
N	$cm^2/V\ s\ K^{\alpha4}$	0.2336	This work

diminishes with temperature. The three most important phonon-scattering processes[9] are deformation potential acoustic, piezoelectric acoustic, and polar optical. It is usually assumed that acoustic phonons can propagate freely in all three dimensions, though electrons are confined to a thin inversion layer near the interface. There, the relaxation time depends on piezoelectric and lattice properties.

Hence, we could assume that neither μ_{AC} nor μ_B depend on the insulator/semiconductor interface properties. They depend on semiconductor material properties ($\mu_{mat}^{-1}\equiv\mu_B^{-1}+\mu_{AC}^{-1}$). Using parameters reported in the literature (due to the lack of data for 2*H*-GaN, we have considered μ_{AC} values from 4*H*-SiC);[17,25,26] both μ_B and μ_{AC} were computed to be above 150 $cm^2/V\ s$ up to 300 °C. This mobility value was significantly higher than the experimental field-effect mobility for our MOSFETs and the computed values of μ_{SR} and μ_C; thus their effect is considerably feeble following Eq. (4). At room temperature, it is clear that for our MOSFET, Coulomb scattering at charged interface traps dominates, and the mobility increases as a function of the gate voltage. This is due, as previously pointed out, to a density of traps at the SiO_2/GaN interface relatively high. μ_C increases with temperature. Our modeling suggests that this improvement is due to two coupled effects, regardless of the linear temperature dependence for μ_C. When the temperature increases, for a given gate bias, the trapped charge is reduced due to screening of interface states by bandgap narrowing. On the other hand, a significant increase in inversion charge (a higher number of free carriers reduces the Coulomb scattering effect at interface traps) is a decisive factor for collecting more electrons in the drain of the device [Fig. 5(b)].

However, for temperatures higher than 150 °C and/or sufficiently high insulator electric field (i.e., effective field in the inversion layer), the field-effect mobility cannot be entirely fitted by the Coulomb scattering term (Fig. 6). This is due to the fact that surface roughness is gradually becoming more and more relevant. Therefore, the mobility model simplifies to

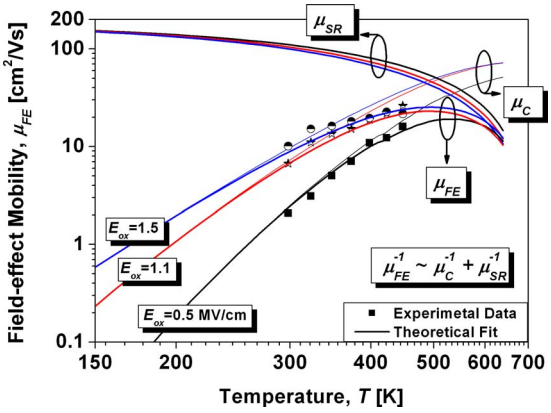

FIG. 6. (Color online) Simulated (solid lines) and experimental field-effect mobility (symbols) as a function of temperature. We have good agreement between the computational results and experimental mobility measurements.

$$\mu_{inv}\approx\left[\frac{1}{\mu_{SR}}+\frac{1}{\mu_C}\right]^{-1}=\left[\frac{\Delta^2}{A'}\frac{E_\perp^{\alpha3}}{(T-T_o)}+\frac{1}{NT^{\alpha4}}\frac{Q_{trap}}{Q_{inv}^{\beta}}\right]^{-1}. \tag{11}$$

This is a closed form expression for the experimental channel mobility for a MOSFET suffering interface collisions and scattering events. It explicitly depends on the interface quality main parameters: Δ, the surface rms roughness, and Q_{trap}, the charge trapped in the interface states. A' (where $A'=AE_o^{\alpha3}\Lambda^{-2}T_o^{-1}$), T_o, and N are fitting parameters. $\alpha4$ and β are empirical constants for describing the screening of the scattering charges by the mobile charges in the inversion layer and experimentally determined to be $\alpha4=\beta\approx1$. Q_{inv} and $E_\perp$ are related to V_G by means of a charge sheet model. The exponential of the perpendicular electric field has been experimentally determined to be $\alpha3=2.3$. High temperature postimplantation annealing leads to significant GaN surface dissociation together with a severe degradation of the surface. Although a protective SiO_2 cap layer has been used, a significantly pit density has been observed.[15] The rms surface roughness of the GaN surface before the gate oxide deposition, measured using an atomic force microscope, was 130 Å. A' is determined to be 1570 $cm^{4-\alpha3}\ V^{\alpha3-1}/s\ K$ from this value. Therefore, it is clear that for our fabricated MOSFET, interface trap charge along with surface roughness plays a major role. In a GaN MOSFET device with a *perfect* insulator/semiconductor [i.e., (i) $\Delta=0$ and (ii) $D_{it}<10^{10}\ cm^{-2}$ and hence $Q_{trap}/Q_{inv}\to0$], the field-effect mobility would tend to μ_{mat}. Improved GaN surface preparation and postimplantation annealing at high temperature are critical fabrication steps to achieve a good and smooth MOS interface.

VI. CONCLUSIONS

A compact channel mobility model has been used to study the on-state and temperature dependence of a fabricated enhancement-mode lateral GaN MOSFET device suffering interface collisions and scattering events. Interface

trap density and surface roughness have been investigated, and their dependence on the channel mobility has been reported. In our case, at low temperatures and/or insulator electric fields the channel mobility was well explained by Coulomb scattering at interface traps, taking into account their screening effect. When increasing the temperature and/or insulator electric field the surface roughness becomes relevant. We have good agreement between the computational results and experimental mobility measurements. A simple closed form expression for the experimental channel mobility is proposed, which allows extracting interesting physical parameters related to surface roughness and MOS interface trap properties.

ACKNOWLEDGMENTS

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