Multi-bit Cascade ΣΔ Modulator for High-Speed A/D Conversion with Reduced Sensitivity to DAC Errors

Indexing terms: Multi-bit ΣΔ Modulators, High-speed, high-resolution A/D conversion.

This paper presents a ΣΔ modulator (ΣΔM) which combines single-bit and multi-bit quantization in a cascade architecture to obtain high resolution with low oversampling ratio. It is less sensitive to the non-linearity of the DAC than those previously reported, thus enabling the use of very simple analog circuitry with neither calibration nor trimming required.

Introduction: At present, there is an increased interest in the use of ΣΔ conversion in mixed-signal CMOS telecom chips [1]. New architectures are required to achieve high resolution with low oversampling ratio M. Two non-exclusive strategies can be adopted to this end [2]: *high-order filtering* of the quantization noise, and *multi-bit* (MB) quantization. They make the in-band quantization noise power P_Q inversely proportional to, respectively, M^{2L+1} (L=filter order) and $(2^b-1)^2$ (b=number of bits in the internal quantizer). Examples of low-oversampling ratio ΣΔM's using both strategies are reported elsewhere [2]-[7].

These advanced architectures are grouped according to the techniques used to: a) guarantee stable operation of the high-order filter; b) attenuate the errors due to the MB DAC non-linearity. A common strategy for the latter case involves using calibration [2][3][5], while the former requirement can be solved through the proper choice of scaling factors or resetting circuitry [2][3]. However, some architectures overcome these problems with neither calibration nor resetting required. The basic idea consists of: first, performing the high-order filtering through a cascade structure to guarantee unconditional stability for any input level and initial condition [4][6][7]; secondly, using MB quantization only at the last stage of the cascade to attenuate the influence of the MB DAC non-linearity [6][7].

Previous MB cascade ΣΔM's [6][7] are intended to attenuate the DAC error power by a factor M^5. The architecture in this Letter obtains a M^7 attenuation

factor. We show that this can be achieved through proper choice of the architecture coefficients and that the degradation due to mismatch is tolerable for up to $b = 3$. Hence, this modulator is feasible for obtaining up to 13-bit resolution with oversampling ratios as low as 16.

Modulator architecture: Fig. 1 shows a generic dual-quantization *N*-stage cascade ΣΔM [8]. It includes single-bit quantization in all the stages except in the last one which incorporates a MB quantizer. After digital cancellation of the quantization error of the former, the following is obtained for the Z-domain output:

$$Y(z) = X(z)z^{-L_T} + d(1-z^{-1})^{L_T}E_N(z) + d(1-z^{-1})^{(L_T-L_N)}E_D(z) \qquad (1)$$

where $X(z)$ is the Z-transform of the modulator input, d is an scalar larger than unity (needed to prevent overloading in the cascade), $E_N(z)$ is the last stage quantization error, $E_D(z)$ is the error induced in the last stage DAC, and $L_T = L_1 + \ldots + L_N$. Note that $E_D(z)$ is $(L_T - L_N)$th -order shaped, which may significantly reduce the linearity requirement of the DAC.

Based on this idea, two MB ΣΔM architectures have been proposed. The one in [6] uses a 2-stage 2-1 cascade ($L_1 = 2, L_2 = 1$), while the one in [7] uses a 2-stage 2-2 cascade ($L_1 = 2, L_2 = 2$). In both cases, following (1), $E_D(z)$ is 2nd-order shaped. With the same principle, Fig. 2 shows a novel MB cascade ΣΔM architecture that better exploits the dual-quantization technique. It is a 3-stage 2-1-1 cascade ($L_1 = 2, L_2 = 1, L_3 = 1$) with single-bit quantization in the first two stages and MB quantization in the last one. Table 1 shows the transfer functions of the digital blocks in Fig. 2 and the relationships between analog and digital coefficient that cancel the quantization noise in the first two stages. The analog coefficients (integrator weights) must be properly chosen to avoid premature overloading of the stages in the loop and maximize the dynamic range (*DR*). We propose the following: $g_1 = g_1' = 0{,}25,\ g_2 = g_3 = g_4' = g_4'' = 1, g_2' = g_3' = g_3'' = 0{,}5,\ g_4 = 2$, so that $d_0 = -1, d_1 = 2, d_2 = 0, d_3 = 2$. Such a choice can be realized by using

only 2-branch SC integrators with reduced output swing and dynamic requirements. After digital cancellation, the Z-domain modulator output results:

$$Y(z) = z^{-4}X(z) + 2(1-z^{-1})^4 E_3(z) + 2(1-z^{-1})^3 E_D(z) \tag{2}$$

Note that the DAC errors are 3rd-order shaped. Thus, the in-band noise power at the modulator output results:

$$P_{2\text{-}1\text{-}1MB} = 4\left(\sigma_Q^2 \frac{\pi^8}{9M^9} + \sigma_D^2 \frac{\pi^6}{7M^7}\right) \tag{3}$$

where σ_Q^2 and σ_D^2 represent the power of the last stage quantization and DAC error, respectively. The latter contribution is attenuated by M^7 (instead of M^5 as in [6][7]).

Influence of Other Non-Idealities: In practice, integrator weight mismatch and finite DC-gain produce incomplete cancellation of the quantization noise in the first stages of the cascade, thus degrading the signal-to-(noise+distortion) ratio (*SNDR)*. This imposes an upper limit on the useful resolution of the last stage quantizer. Above this limit, the benefits of finer quantization in the last stage may be masked by the un-cancelled portion of the quantization noise of the previous stages. Fig. 3 shows the half-scale *SNDR* obtained by behavioural simulation for the new modulator as a function of the last quantizer resolution. These simulations include integrator weight mismatch (sigma = 0.1%) and finite DC-gain (1000); according to them, using quantizers with more than 3-bit resolution does not make sense. However, this is enough to significantly reduce the required oversampling ratio respect to the single-bit case. Fig. 4 compares the worst-case *SNDR* (sigma = 0.1%) as a function of the input level for the 2-1-1 3bit ΣΔM with that of those in [6][7], always using optimized integrator weights; for completeness, we also make a comparison with the 2-1-1 single-bit. Compared to the 4th-order architectures, the new one features the largest *DR* with the lowest oversampling ratio. Particularly, to reach similar performance with the single-bit approach, *M* must be at least 24.

In summary, because the new architecture tolerates the analog non-idealities for 3-bit quantization (with no calibration needed), it is feasible for high-frequency ΣΔ

ADC's with low oversampling ratio and, hence, low-power consumption.

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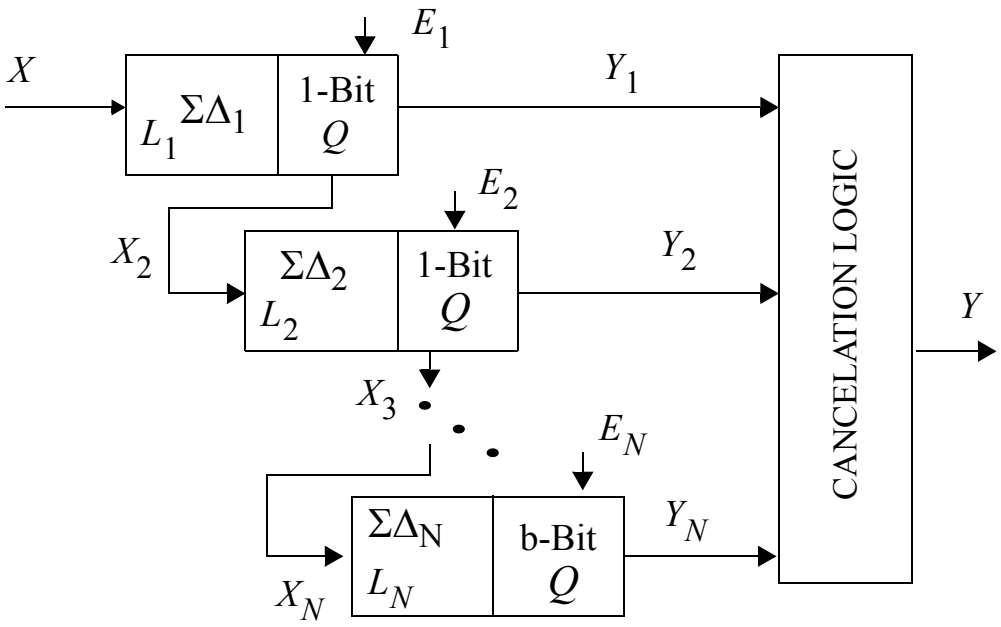

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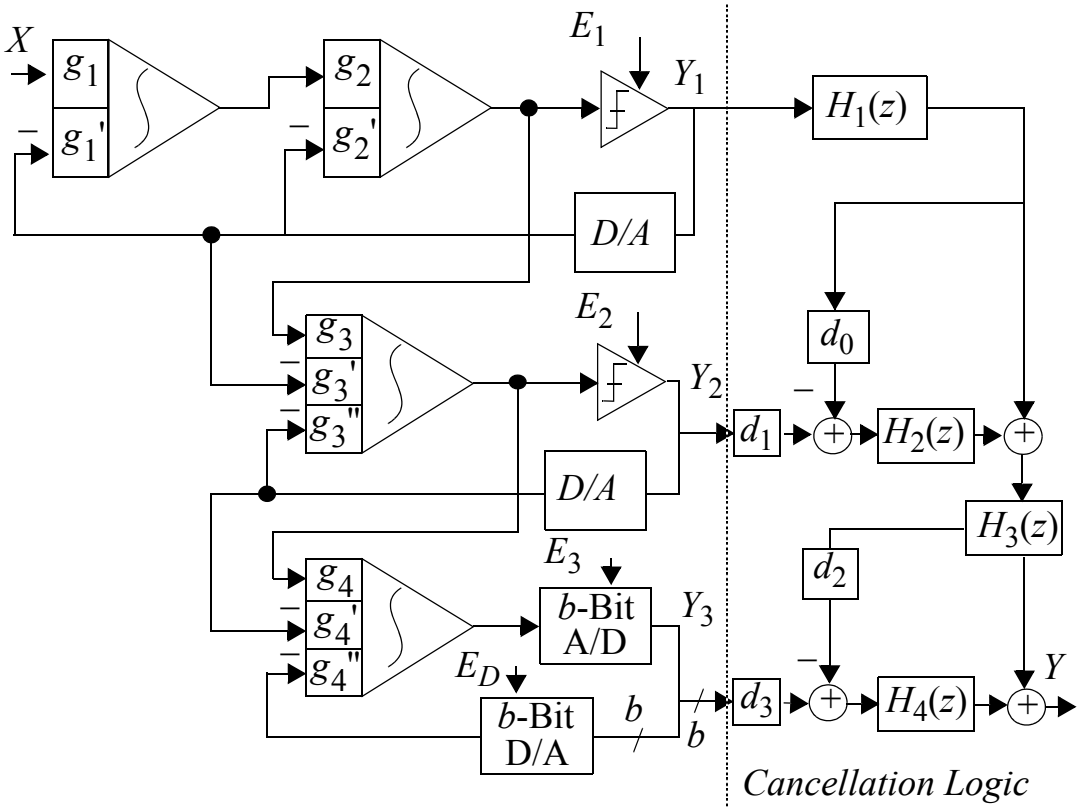

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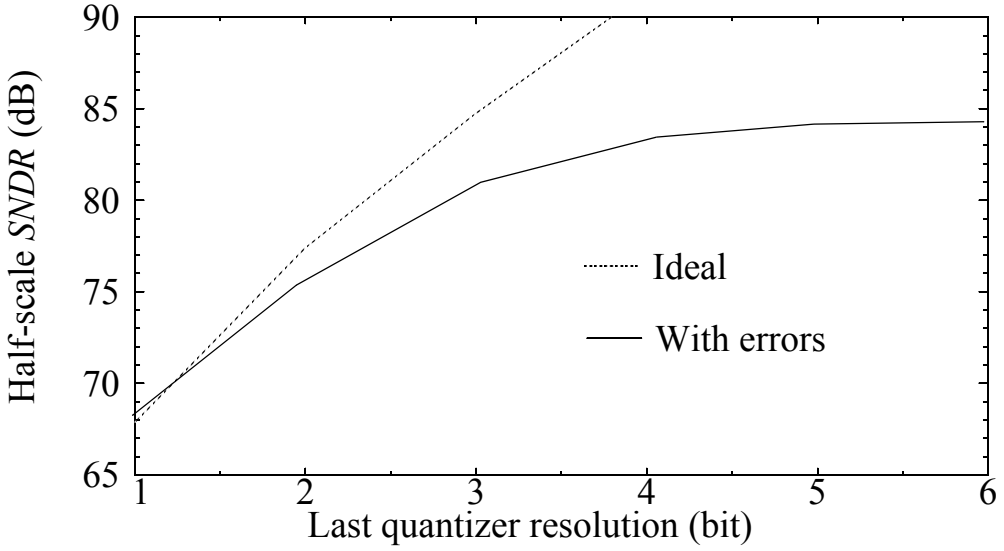

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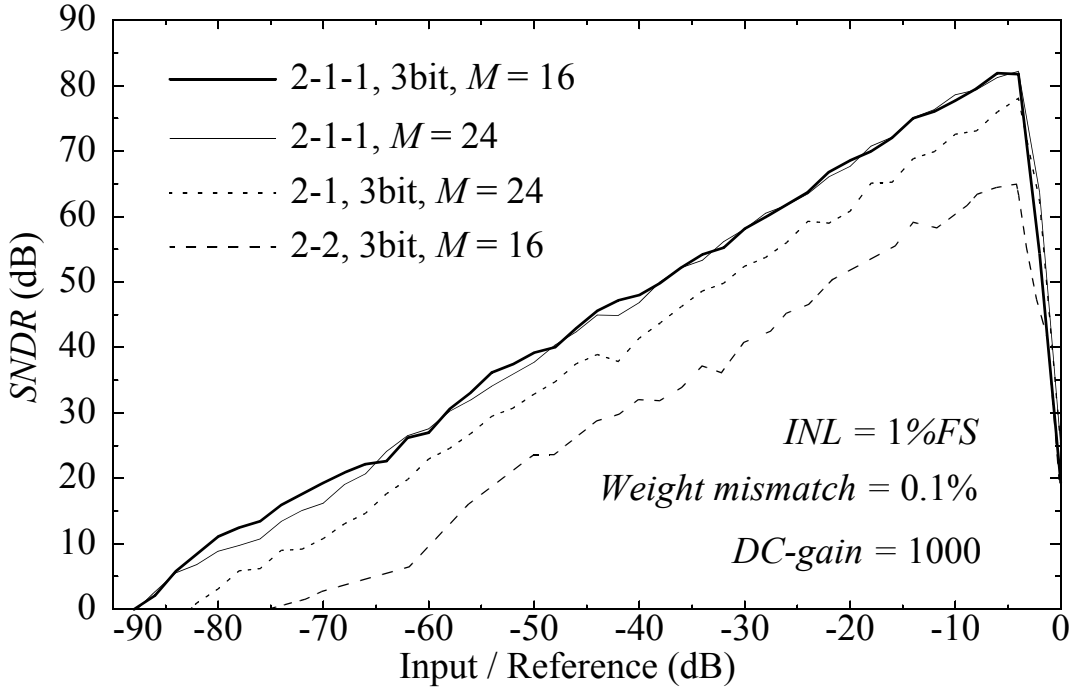

Fig. 4 Worst-case *SNDR* vs. input level in presence of capacitor mismatch and finite integrator DC-gain

Table 1: Coefficient relationships in Fig. 2

Digital	Digital/Analog	Analog
$H_1(z) = z^{-1}$	$d_0 = 1 - g_3' / (g_1 g_2 g_3)$	$g_1' = g_1$
$H_2(z) = (1 - z^{-1})^2$	$d_1 = g_3'' / (g_1 g_2 g_3)$	$g_2' = 2 g_1' g_2$
$H_3(z) = z^{-1}$	$d_2 = 0$	$g_4' = g_3'' g_4$
$H_4(z) = (1 - z^{-1})^4$	$d_3 = g_4'' / (g_1 g_2 g_3 g_4)$	