A CMOS 0.8μm FULLY DIFFERENTIAL CURRENT MODE BUFFER FOR HF SI CIRCUITS

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We present a high-frequency fully-differential current-mode buffer to interface off-chip currents with no significant degradation of the frequency response, and to measure current-mode ICs using standard equipment. This unit has been incorporated to the front end of a Switched-Current BandPass ΣΔ modulator which can in its turn be used to interface bandpass signals from on-chip current-mode sensors, and to interface RF signals for telemetry applications.

Introduction: Current-mode circuits may be advantageous for applications involving sensors whose outputs are currents such as light and radiation sensors, some temperature and magnetic sensors, and many others found in biomedicine [1]. For these cases, processing directly in the current domain avoids using current-to-voltage converters and may hence yield faster operation than voltage-mode circuits. However, the speed advantages are only realized at fully if the input currents are generated on-chip. Otherwise, the circuit dynamics may become severely degraded due to parasitic time constants at the chip pads. This letter presents a CMOS current buffer to interface single-ended off-chip currents into on-chip fully-differential current-mode circuitry and include experimental results showing its performance as a stand-alone unit and as part of a CMOS 0.8μm BandPass ΣΔ SI modulator [2].

Illustrating the Speed Degradation in SI Interfaces: Consider the SI second-generation memory cell of Fig. 1(a). We have implicitly assumed that this memory is on-chip and that the capacitance of the driving stage is negligible as compared to the gate-to-source capacitance of the memory transistor C_{gs} -- bear in mind that mismatch considerations force using large channel area transistors. During phase ϕ_1 (sampling phase) this capacitance is charged with a time constant C_{gs}/g_m. Assume now that the memory cell is placed at the chip front-end, and we use the simplest possible interface: an off-chip linear resistor with resistance much larger than $1/g_m$ (see Fig. 1(b)). Consequently the time constant changes from C_{gs}/g_m to $(C_{gs} + C_{pad})/g_m$. Because the pad equivalent capacitance C_{pad} is typically large as compared to the inner capacitance, the high-frequency behavior of the memory cell becomes degraded. The same problem is observed for other enhanced SI memory cells, including those with low input impedance.

Consider now Fig. 1(c), where a current buffer has been incorporated at the front-end of a SI circuit. The input current i_{in} is first processed by the buffer and then the resulting current i'_{in}, is applied to the SI circuit. From Fig. 1(c) the following transfer function is found,

$$\frac{I'_{in}(s)}{I_{in}(s)} = \frac{1}{(1 + sC_{pad}R_{in\_buf})} \qquad (1)$$

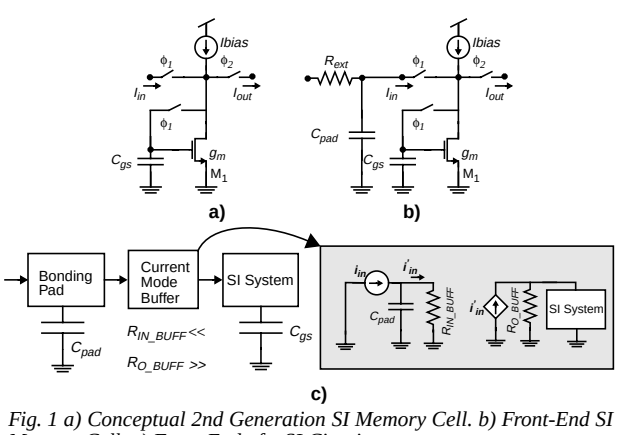

Fig. 1 a) Conceptual 2nd Generation SI Memory Cell. b) Front-End SI Memory Cell. c) Front-End of a SI Circuit.

from where a condition is derived to render the influence of this capacitance negligible,

$$C_{pad}R_{in\_buf} \ll T_{in} \qquad (2)$$

where T_{in} is the input signal period. This constitutes a basic specification to design of the buffer. Other specifications refer to the SNR and the output swing, which must be in compliance to the SI circuit. In the case of the BandPass ΣΔ modulator the input frequency is 2.5MHz, the resolution is 10bit and the output swing is ±50μA.

Circuit Description: Fig. 2 shows the schematic for the proposed current mode buffer. It has fully differential structure, but can be used either with single-ended input or with differential input. If voltage-to-current conversion is needed, it can be implemented using an external resistance connected to any of the two input nodes. This block has three major stages: the input stage ($M_{1,2,5,6,9,10,17,18}$); the output stage ($M_{3,4,13,14}$) and the Common Mode FeedBack stage (CMFB) ($M_{7,8,11,12,15,16}$).

Fig. 2 shows that the input stage incorporates a local input feedback to obtain a very low input resistance, R_{in_buff} given by

$$R_{in\_buff} = \frac{g_{ds17} + g_{ds18}}{(g_{m1} + g_{m3})g_{m18}} \qquad (3)$$

This is needed to satisfy (2) under the constraint imposed by the value of the bonding capacitance -- not controllable by the designer. Note R_{in_buff} is controlled by changing either the transconductance of transistor M_1, g_{m1} (= g_{m3}) or the inverter gain. This extra degree of freedom is convenient because as g_{m1} increases, the output thermal noise Power Spectral Density (PSD), given by

$$S_o = \frac{16}{3}K_B T(g_{m1} + g_{m3} + 2g_{m5} + g_{m13} + g_{m17} + g_{m18}) \qquad (4)$$

increases as well. The output stage scales the input current by a factor of either 0.5 or 1.0 depending on whether the input current is single-ended or differential, respectively.

The CMFB stage operates as follows. Assuming a positive (negative) input common mode flowing into the input nodes, then M_8 gate voltage increases (decreases) causing $M_{11,12,15,16}$ drain current increases (decreases) subtracting (adding) the common mode current to the input and output stages. The most important parameter in the design of this stage is hence the common mode gain given by g_{ds9}/g_{m15}.

The different design trade-offs of this buffer have been handled by our circuit optimization tool FRIDGE [3]. Table 1 shows a summary of the simulated performance. High output resistance is not needed because the SI memory cells used are regulated-folded cascode.

Experimental results: This circuit has been integrated in a test chip together with other sub-blocks of the mentioned Fourth Order BandPass ΣΔ SI modulator. The current buffer active area is 175 x 105 μm^2 and consumes 22 mW from a 5V power supply. Table 1 summarizes measurements made on an isolated buffer using a single-ended input. DC measurements have been realized with the semiconductor parameter analyser HP4145. Fig. 3 shows the measured DC input/output transfer characteristics illustrating the rejection of the output common mode. Fig. 4(a) shows the AC buffer measurement set-up. The output of the buffer is sensed through a virtual ground realized with an off-chip high-speed amplifier, (AD844) implemented as a second generation current conveyor with gain +1 (CCII+) [4]. In the configuration of Fig. 4(a), this amplifier features 37MHz bandwidth; hence, it can be expected to dominate the high-

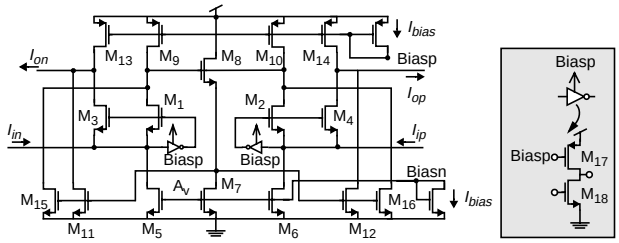

Fig. 2 Schematic of the Current Mode Buffer.

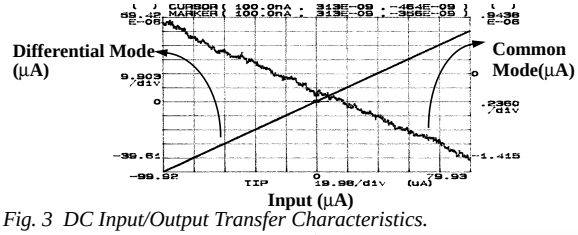

Fig. 3 DC Input/Output Transfer Characteristics.

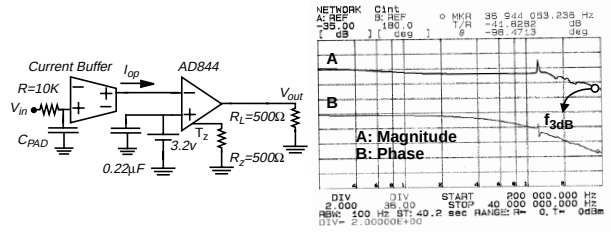

Fig. 4 a) AC Measurement Set-Up. b) Experimental Bode Plot.

frequency response. This is actually confirmed by the measurements realized with the network analyser HP4195. Fig. 4(b) shows an experimental Bode plot for C_{pad} about 10pF (the whole parasitic capacitance in the experimental board). The measured 3dB frequency is the one of the current conveyor, 37MHz, thus confirming that the frequency bandwidth of the buffer is much larger (around 90MHz).

Conclusions: A high-frequency fully-differential current mode buffer has been designed to interface off-chip currents into on-chip fully-differential current-mode circuitry. It has been fabricated in a 0.8 μm double-poly double-metal CMOS technology and features more than 37MHz bandwidth for a pad capacitance of about 10pF. This buffer isolates the on-chip circuitry from the parasitic time constants at the chip input pads, and allows us to take full advantage of the speed capabilities of current-mode circuits. It has been included at the front-end of a redesign of a fourth-order BandPass ΣΔ SI modulator [2] featuring 9 bit dynamic range at 10MHz clock frequency @30kHz signal bandwidth centered on 2.5MHz.

References

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Table 1: Performance Summary of the Current-Mode Buffer

Parameter	Simulated	Measured	Unit
Differential Gain (A_{DIFF})	0.497	0.496	--
Common Mode Ratio Rejection (*CMRR*)	38	30	dB
Output Offset	0.3	0.8	μA
Output Swing	±50	±50	μA
Input Resistance (R_{in})	213	200	Ω
Output Resistance (R_{out})	68	54	KΩ
-3dB-Frequency (f_{3dB})	>37	>37	MHz
Total Harmonic Distortion (*THD*)	0.2	0.3	%