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Abstract: For ultra-high speed communication systems at high center frequencies above 100 GHz, we propose a disruptive change in system architecture to address major issues regarding amplifier chains with a large number of amplifier stages. They cause a high noise figure and high power consumption when operating close to the frequency limits of the underlying semiconductor technologies. Instead of scaling a classic homodyne transceiver system, we employ repeated amplification in single-stage amplifiers through positive feedback as well as synthesizer-free self-mixing demodulation at the receiver to simplify the system architecture notably. Since the amplitude and phase information for the emerging oscillation is defined by the input signal and the oscillator is only turned on for a very short time, it can be left unstabilized and thus come without a PLL. As soon as gain is no longer the most prominent issue, relaxed requirements for all the other major components allow reconsidering their implementation concepts to achieve further improvements compared to classic systems. This paper provides the first comprehensive overview of all major design aspects that need to be addressed upon realizing a SPARS-based transceiver. At system level, we show how to achieve high data rates and a noise performance comparable to classic systems, backed by scaled demonstrator experiments. Regarding the transmitter, design considerations for efficient quadrature modulation are discussed. For the frontend components that replace PA and LNA amplifier chains, implementation techniques for regenerative sampling circuits based on super-regenerative oscillators are presented. Finally, an analog-to-digital converter with outstanding performance and complete interfaces both to the analog baseband as well as to the digital side completes the set of building blocks for efficient ultra-high speed communication.

Keywords: front-end circuits and systems, wireless RF components and systems, high-data-rate communications, superregenerative receivers.

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I Introduction

For ultra-high speed communication, high center frequencies above 100 GHz are targeted. The large available bandwidth at these frequencies – although regulatory band definitions are still missing for such wideband applications – enables high throughput with moderate spectral efficiency (e. g., using 16-QAM at 25 GBaud) and thus also moderate requirements regarding the employed circuit elements. However, implementation and operation typically occur much closer to the technological limits of the underlying semiconductor process than in current commercial systems at lower frequencies. Scaling conventional homodyne transceiver architectures thus comes with several drawbacks, most notably significantly lower gain due to the limited f_T/f_{max} given by currently available technologies. In consequence, amplifier chains with many amplifier stages are necessary for sufficient gain (e. g. [1],), which leads to high noise figures, large implementation size and cost as well as high power consumption. These drawbacks can be considered a major obstacle towards ultra-high speed mobile communication when it comes to handset implementation.

In order to overcome these frequency scaling issues, alternative transmitter and receiver architecture paradigms have to be considered. Particularly regarding low single-stage amplifier gain, repeated amplification

through positive feedback like in a super-regenerative oscillator (SRO [2–5],) promises notable advantages. They are enabled by a very high overall gain that can be achieved with very low hardware effort using only a single amplifier stage.

This paper is organized as follows: Section II summarizes the most important aspects of the proposed system concept. An analysis of expected data rates, noise performance and system behavior is given in III. Afterwards, an overview of component concepts and implementation techniques with regard to the proposed architecture is provided. Section IV focuses on transmitter components, V on the SRO-based frontend and VI on receiver baseband circuits. Section VII concludes the paper.

II System concept

The general idea behind the "simultaneous phase and amplitude regenerative sampling" (SPARS) approach is to employ SRO-based repeated amplification through positive feedback wherever a conventional amplifier chain would be placed in order to reduce hardware complexity and to relax the requirements for other parts of the transmitter and receiver. In particular, alternative modulation and demodulation concepts are rendered feasible due to specific benefits from the regenerative sampling architecture (see Figure 1) in terms of gain and gain control range. From a signal processing point of view, the regenerative sampling technique employs sampling of phase and amplitude from the input signal like a sample-and-hold stage and recreates a strongly amplified (~20–45 dB) version of the signal without gain compression at its own oscillation frequency.

At the transmitter side, the SRO with its high gain replaces the power amplifier, which allows relaxing the magnitude requirements for the local oscillator signal. Hence, it could be at least partially synthesized with passive components in combination with an efficient RFAC-based modulator, which is designed to allow for low power level signals (see Section IV).

In the proposed receiver architecture, a local oscillator signal is not necessary for phase-sensitive demodulation. Thus, a synthesizer can be omitted. Instead, a self-mixing approach is employed where the current symbol is mixed and thus demodulated using the previous symbol, which was delayed by one period. This technique is known from ultra-wideband systems ("delay-hopped transmitted reference receiver" [6],), but increases the requirements on supporting a large range of output amplitudes dramatically since it squares the input amplitude. However, with a SRO as an LNA replacement, which features inherent gain tuning over a large range of gain values through pulse width variation, an optimal operating point can be guaranteed for the self-mixing circuit.

During operation, the transmitter generates a sequence of phase and amplitude modulated pulses. On the receiver side, the SRO is started synchronously always when the incoming pulses reach their maxima. Although the oscillators are free-running and thus may differ in their oscillation frequency, phase and amplitude are preserved in both regeneration stages due to operation in the linear (i. e., small-signal) domain of oscillator device. The modulation introduced by frequency offsets is eliminated through differential demodulation by the self-mixing stage.

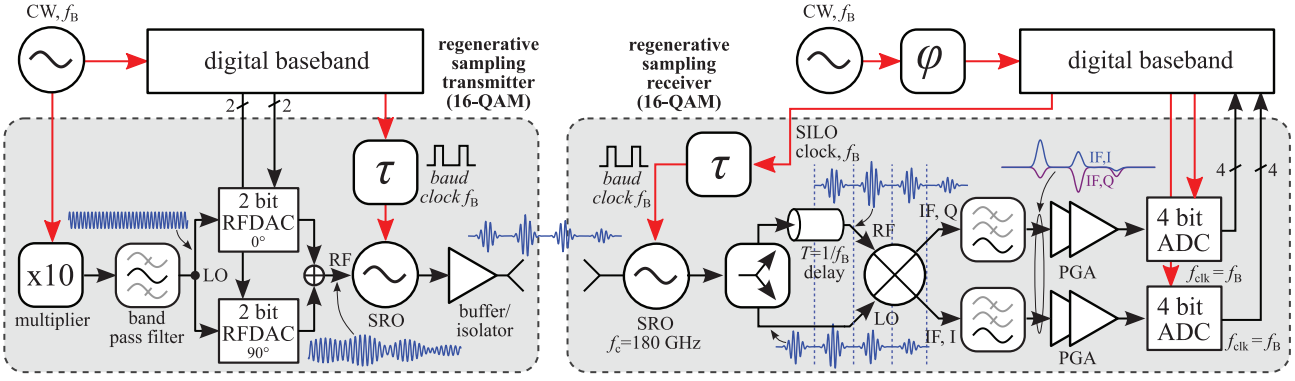

Figure 1: System architecture concept for a transmitter and receiver based on simultaneous phase and amplitude regenerative sampling.

III System level analysis

A Symbol rate and noise performance

Since the SRO-based regeneration of the individual symbols each requires an oscillation to rise and decay, the achievable data rate strongly depends on the choice of parameters as well as on the desired overall gain. In order to regenerate the signal of an incoming symbol (i. e., its amplitude and phase), the oscillator is turned on at the center of the symbol (when its maximal SNR is reached). The SRO regenerates phase and amplitude of the low power level input signal, which is injected into the oscillator's feedback loop. The signal defines the initial condition for the emerging oscillation instead of noise like in normal oscillators. Since the oscillator is quenched (turned off) before reaching saturation, the system stays in linear domain and thus preserves a linear relationship between output and input amplitude and phase. The oscillation rises exponentially until the required gain is reached. Until the beginning of the next cycle, the oscillation magnitude must decay below the input power level minus a margin, which at least accounts for the minimum SNR of the modulation scheme. In total, the minimum period that accounts for rise, decay and margin determines the maximum symbol rate (also see Figure 2 top). How long rise and decay will take depends on two parameters: the active element's gain M (higher means faster) and the quality factor Q_0 (higher means slower) of the oscillator's resonant tank. Since it is targeted towards operation close to technological limits, low single-stage gain (typically 3 dB or less) can be expected. Consequently, a very low quality factor (typically 3 or less) is a major design goal for the oscillator.

Figure 2 (bottom left) shows the dependency of the maximum achievable symbol rate (relative to the carrier frequency) on the quality factor and single-stage gain for two overall gain goals (25 dB and 45 dB). The plots are based on a simulation using the well-known

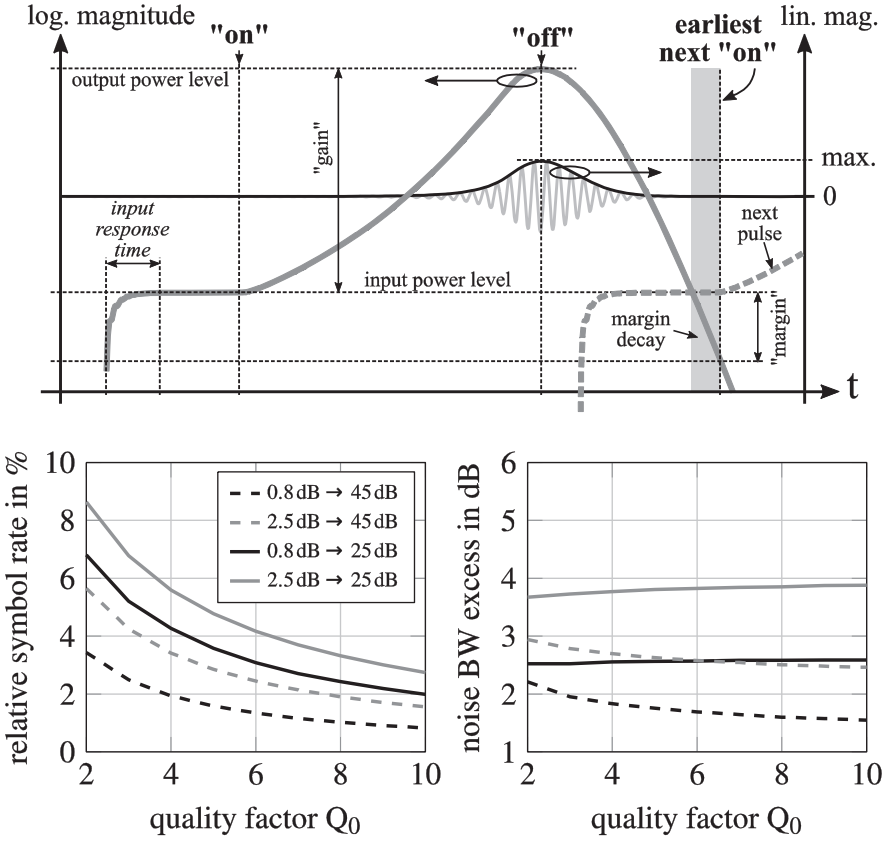

Figure 2: Analysis of achievable data rate and receiver bandwidth.

parallel resonator model (G_0, L_0, C_0 and $-G$ as active element) [2] and assuming modulation through an RC filter with a time constant of $\tau = 2/f_0$. As a result, very high symbol rates between 2 and 10 % of the carrier frequency can be expected, which easily enables data rates of up to 100 Gbit/s with moderate bandwidth efficiency (e. g. 16-QAM) above 100 GHz.

Apart from symbol and data rate, the expectable noise performance is a crucial figure of merit for high center frequency systems. Since the oscillator needs to rise and decay, its input bandwidth will be notably higher than needed for classic systems with the same symbol rate. Figure 2 (bottom right) depicts the amount of this "bandwidth excess" as a function of quality factor, single-stage gain and overall gain. It can be seen that the excess ranges somewhere between 2 and 4 dB. This would be a notable disadvantage compared to conventional amplifiers. However, repeated amplification in the SRO adds additional input signal power after each round to the amplified feedback signal, which limits the overall noise figure to that of a single amplifier stage. In a mm-wave amplifier chain, the noise figure successively degrades with each stage. This degradation may quickly sum up to values around 3 dB (e. g. [7, 8],) and leads to total noise figures ranging from 5 to 10 dB. Consequently, the SRO-based amplifier replacement can be considered comparable to the noise performance of a receiver chain with a large number of amplifying stages. However, it comes with a significantly reduced complexity and power consumption, since it is built from a single amplifier stage.

B Demonstration experiments

In order to highlight the achievable benefits of the proposed architecture, several experiments and demonstrations with scaled demonstrator implementations have been conducted, which are fully accessible for measurement. On the modulator side, passive frequency upconversion [9] and phase modulation [10] have been studied as a method to exploit the relaxed gain requirements. Regarding the receiver, the capability of SRO-based QAM sampling and regeneration was investigated [3]. Finally, a complete demonstrator is analyzed in [11]. In the following, the verification of the core concept based on [3] is briefly provided. It includes the regeneration of a 16-QAM signal using the SRO as an energy-efficient replacement for long amplifier chains.

For experimental verification, a 21 GHz SRO based on microstrip circuit elements using a lumped JFET amplifier (11 dB gain) has been designed and implemented. Its frequency is high enough to observe similar hardware limitations like when operating close to the transition frequency of a semiconductor technology, such as low gain and high losses. In general, high data rates require fast rise and decay of the emerging oscillation. Given that the single-stage amplifier gain is low (< 6 dB), a very low resonator Q is necessary. Fortunately, this is often inherently provided at very high frequencies. For this demonstration (see Figure 3 center, left), a directional coupler with ~6 dB insertion loss in the feedback loop path is employed to ensure low Q and fast decay. As a side effect, the injection and output signals are hardly attenuated, which is optimal for low noise figure, high gain and high output power. In this case, 5 dB open loop gain would lead to a relative data rate of 9 % according to the aforementioned model (20 dB total gain, $Q_0 = \sim 3$), which is limited to ~2.3 % since the feedback loop exhibits a group delay of four oscillation periods, which increases the rise and decay times by four. Consequently, the demonstration of 343 MBaud at 21 GHz (1.63 %) is already quite close to the theoretical limit despite the limitations of PCB-based technology compared to integrated

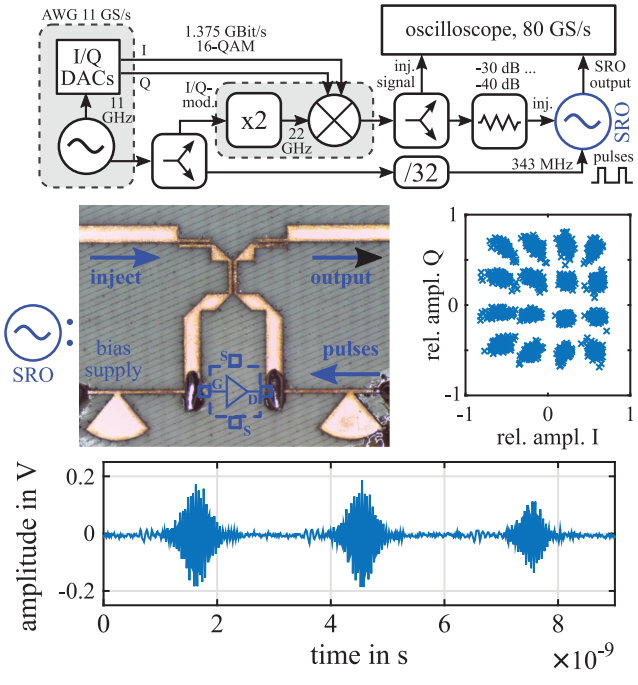

Figure 3: Demonstration experiment for SRO-based regenerative sampling of 16-QAM modulated communication signals [3].

circuits. However, when targeting frequencies above 100 GHz at very high switching rates compared to the center frequency, special attention is required regarding a differential design with good common mode suppression (to prevent switching harmonics from interfering with the input signal) as well as regarding a sufficiently fast drive circuitry to allow fast switching and thus high symbol rates.

Experimental validation of SROs at high frequencies requires special attention towards a coherent measurement setup. In order to enable output versus input phase measurements (e. g. to determine the transfer function or for coherent demodulation), switching clock, input carrier phase and symbol clock require low jitter synchronization. Thus, a common intermediate frequency clock source is used (11 GHz AWG source, see Figure 3 top), from which an arbitrary waveform generator drives the modulation digital-to-analog converters (DACs). The carrier for modulation is derived by frequency multiplication (here: subharmonic mixer) and for the SRO sampling clock, dividers are employed. This approach is sufficiently flexible to be transferred to the target frequency (180 GHz) by using frequency extenders/mixers for modulation and downconversion.

Finally, the results (Figure 3 bottom, center right) clearly demonstrate the capability to sample and to regenerate 16-QAM modulated symbols with only slight nonlinearities. The total gain of 20 dB constitutes a 4x improvement over the single amplifier stage with minimal additional hardware efforts.

IV Transmitter components

High speed DACs come in several architectures ranging from current scaling to voltage or charge scaling. For high-speed DAC designs, the current scaling approach is the most fitting one, utilizing the current steering or the switched current principle. In addition to these traditional architectures, there is another suitable one for our system concept: the radio frequency digital-to-analog converter (RF-DAC). It combines digital-to-analog plus frequency upconversion and therefore reduces the transmitter components needed in comparison to a homodyne transmitter [12,13].

Besides the obvious advantage of reducing the number of components, namely mixers, filters and intermediate frequencies, conventional DAC and mixer architectures are only usable for non-return to zero (NRZ) coding schemes, thereby making them sensitive to inter symbol interference (ISI) and DAC sampling clock jitter.

It also fits the specifications of the proposed SPARS concept very well. For high data rates the combination of DAC plus IQ-mixer is very inefficient, because it will need sufficient signal power levels to run optimally. In a RF-DAC based concept, the constraints for the power levels are quite relaxed. A low output power after the RF-DAC is no problem, since the following SRO can sample signals as low as −40 dBm (see Section II), which also enables a design for low power consumption.

An example of a RF-DAC can be seen in Figure 4. It shows the schematic of a seven-stage distributed RF-DAC as in [14]. Each of the seven cells consists of two current steering output stages. One of these output stages looks basically like a double balanced Gilbert cell configured as a BPSK modulator. The frequency upconversion is done by modulating the current source at the bottom with a LO signal at the differential input pairs. The digital-to-analog conversion is done by the switching quad above, which multiplies the signal with +1 or −1 respectively.

By connecting two output stages in parallel and properly binary weighting their tail currents and transistor sizes, a RF-DAC cell is formed in which one output stage accounts for the MSB (most significant bit) and one for the LSB (least significant bit). This increases the resolution, while keeping the cell number reasonably low, to ensure good integration on silicon.

A Parameters

The following section will give an overview of parameters and design considerations regarding RF-DACs. The

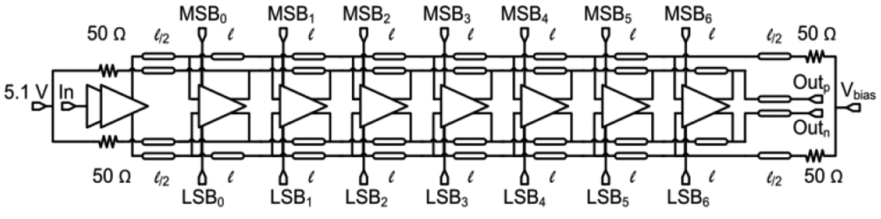

Figure 4: Schematic of a RF-DAC consisting of seven DAC cells [13].

architecture of choice for high speed applications is the current-steering principle. It is advantageous over switched currents and delta-sigma digital RF modulation, because of spectral purity and wider bandwidth. The switched current approach lacks very high spectral purity, because of the disturbances when turning on/off big currents and the delta-sigma RF-to-digital architecture trades of bandwidth for better spectral purity [15, 16].

1 Glitches

Glitches in normal current steering DACs mainly occur when switching between currents, especially when switching between large currents (e. g. data switches from 0111 ... to 1000 ...). The same holds true when you look at RF-DACs and their behavior when the MSBs switch. Hence full segmentation of a distributed RF-DAC is desirable. Let's say the goal is to design an n-bit DAC, then it would consist of $i = 2^n$ - 1 cells. The segmentation of the n most significant MSBs is achieved by default (see Figure 5). Minimizing the glitches would mean a large n, which at some point gets unrealistic to integrate on silicon, both because of chip size and difficulty of layouting. By realizing an output stage as two current-steering output stages connected in parallel with a ratio of 2^n:1 the overall bit resolution can be elevated to $n = 2i$, hence maintaining a lower RFDAC cell number [13]. Additionally, the sinusoidal LO and the DAC sampling data bits should be aligned so that the switching occurs in the zero regions of the clock/carrier frequency, making it a return to zero (RZ) behavior which alleviates ISI. This can easily be done by timing alignment via flip-flops.

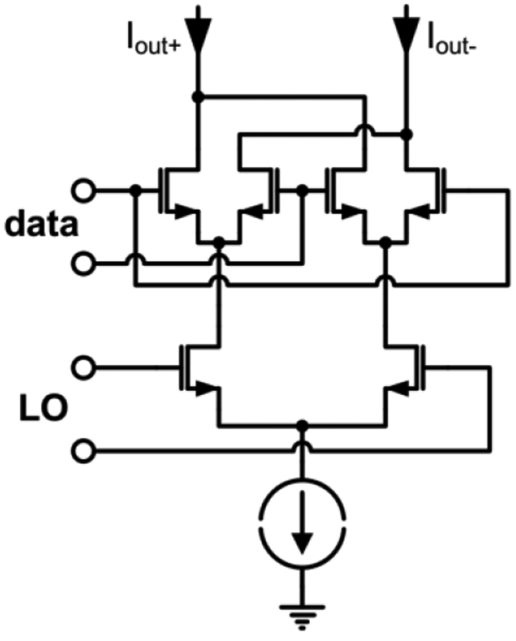

Figure 5: Schematic of an output stage of a DAC cell.

2 Linearity

A traditional Gilbert cell has its baseband inputs at the lower differential input pairs and the LO at the switching squad. The transconductance nonlinearities limit the dynamic range of the signal and cause spurs and harmonic distortions. The RF-DAC output stage however has its inputs reversed and all transistors, excluding the current source, act as switches with no linearity constraints. This means, that the linearity of the output is determined by the resolution of the DAC, the output impedance modulation of the DAC cells and mismatches in timing and amplitude.

To further improve linearity, local cascode transistors or transformers can be employed at the output of the DAC cells [17]. While the former needs additional voltage headroom, the latter increases power consumption and chip area. A local cascode transistor adds additional isolation between output signal and mixer common source node, hence improving linearity. Transformers introduce common-mode isolation between DAC and the load and filter the low-frequency offset and the unwanted higher frequency components. By choosing a turn ratio of $n > 1$ the output current in the transformer is increased and because the output noise of the RF-DAC is mainly caused by the current source transistors, the SNR (signal-to-noise ratio) will also increase.

3 Output Impedance

An important advantage using a double-balanced Gilbert cell as the output stage of a DAC cell is that it maintains a constant dc level and a constant impedance at its output independently of the digital input word, thus preventing code-dependent errors. This means that only the output transmission line, which acts as a current summer for all DAC cells, much like in distributed amplifiers (DA), must have a flat broadband frequency response. However, there is one problem as described in [13]: traditional DAs operate in linear mode so the sum of the input and output transmission line losses is identical for each cell. But since the DAC operates in limiting mode, cells which are closer to the input will see a higher attenuation until

the output than cells which are placed nearer to the output. This will introduce systematical integral nonlinearity (INL) and differential nonlinearity (DNL) errors, especially with higher clock/carrier frequencies, which will reduce the effective resolution of the RF-DAC, if it is not compensated by the LSBs.

B Design of a 180 GHz RF-DAC

Since the SPARS project stipulates a 16-QAM modulation, two RF-DACs with a resolution of two bits have been designed, one for the in-phase and one for the quadrature component (see Figure 1). A distributed architecture has been chosen, featuring three identical RF-DAC cells as seen in Figure 6.

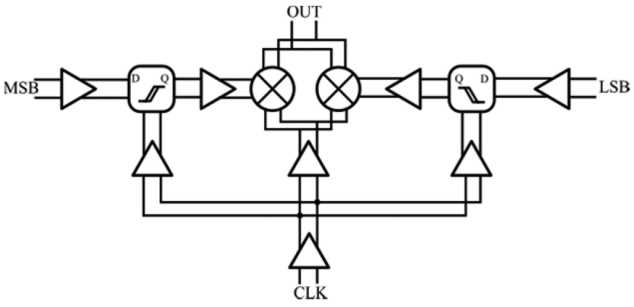

Figure 6: Schematic of a RFDAC cell (after [13]).

Those cells consist of several buffers for signal boosting purposes, two retiming flip-flops, and its main parts, the two current-steering output stages. These serve as upconversion mixers and binary phase shift keying modulators at the same time. As described before, retiming flip-flops are needed to make sure switching occurs in the zero regions of the clock signal. However, this necessitates two additional buffers between the flip-flops and the output stages to avoid clock feed-through.

The current-steering output stages in Figure 7 consist of two parallel connected Gilbert cells. On the right side is the MSB modulator and on the left the LSB modulator. The ratio between the MSB and the LSB transistors, as well as the currents I2 and I1, which are also realized as transistors, is 3:1. Each transistor is biased at peak f_T to achieve fast switching and high bandwidth. This biasing condition is ensured for the case that all current is switched to one side.

At the output, a transformer is used for the summation, which ensures high linearity and SNR. The summation of the three RF-DAC cells is done via transmission

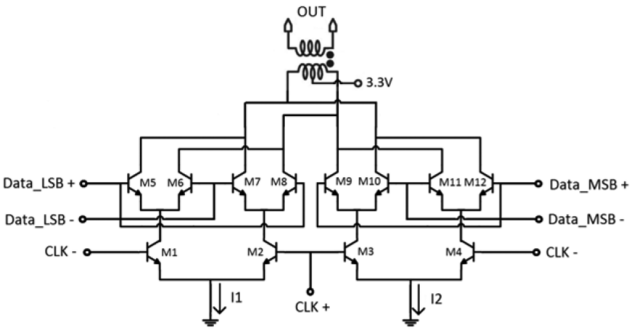

Figure 7: Schematic of the RFDAC output stage.

lines, which have been designed to show a flat and broadband response. Active current summation has been discarded, because it would result in output swing limitation and higher noise. Thus a 2-bit RF-DAC has been designed with a carrier frequency of 180 GHz and a modulation rate of up to 18 GBit/s.

V mm-wave frontend components

A Integrated mm-wave SROs

The design of integrated mm-wave regenerative sampling circuits based on SROs faces many of the same challenges known to designers of mm-wave VCO ICs. The transistor's voltage gain falls at high frequency, whereas the resistive losses in the passive network increase due to the skin effect. This leads to low on-chip component quality factors, as well as the interconnect and pad parasitics presenting significant impedance transformations at the frequency of operation. These are all effects that have to be taken into consideration when designing integrated circuits above 100 GHz in any modern semiconductor technology. These effects eventually lead to the inability to achieve a sufficient loop gain to start an oscillation in the circuit beyond a certain frequency, thus violating the Barkhausen criteria for oscillation. This puts a limit on the attainable fundamental oscillation speed from a certain topology and technology, which is always less than what is theoretically possible.

Conveniently for SRO design, however, several of those design constraints are relaxed by the proposed system architecture in Section II, and some can even be turned around to become favorable design goals. This presents many advantages for high-frequency design versus conventional homodyne receiver blocks. The low resonator quality factor leads to faster oscillator startup, thus leading to

higher achievable symbol rates. This occurs at the cost of higher phase noise in the oscillator, which is not as directly critical as for local oscillator use. The low transistor gain translates to low feedback loop gain, which has been found to lead to better phase locking to injected signals through model simulations [18], and consequently, fewer phase modulation errors. Moreover, the low small-signal gain of the oscillator core transistors is multiplied through repeated amplification by positive feedback to achieve a much higher large-signal regenerative gain. This is done without the need for cascading of several gain stages, thus no cost of increased dc power consumption is incurred (excluding that for input and output buffers).

Regarding noise, phase noise like traditionally considered in oscillators is not relevant for this system; since the oscillator is only turned on for a very short time (40 ... 100 ps), the relevant frequency offset would be in the GHz-range, which corresponds to thermal noise. Thus the achievable Q value and the corresponding noise bandwidth in conjunction with the noise figure of the amplifier stage determine the noise performance of the system.

However, designing dangerously close to the oscillation limit also means that accurate circuit and EM simulations have to be performed to guarantee functionality, which can be time-consuming. The accuracy of the transistor models and their ability to correctly predict large-signal effects also becomes very critical. Circuit topologies have to also be carefully chosen for fundamental oscillation at a certain target frequency, as not all oscillator topologies can be successfully implemented at mm-wave frequencies. In the following sections, the design of two integrated LC SRO circuits based on two different topologies is presented. One is based on a single-ended Colpitts oscillator topology, and the second is based on the cross-coupled topology. Both circuits were implemented in a 0.13-µm SiGe BiCMOS technology with peak values for $f_T = 300$ GHz and $f_{max} = 500$ GHz.

The goal is to integrate all mmW components on a single chip. For early stage verification, frequency domain analysis allows for a performance estimation of the single circuit.

B Regenerative Sampling Circuit Design

1 Single-Ended Colpitts SRO

The common-collector Colpitts topology is one of the simplest oscillator topologies that can be adopted for operation at frequencies above 100 GHz. It has the advantage that it can be used to build single-ended oscillators, thus reducing the component count as well as the dc power consumption. For SROs, this also means eliminating the need for baluns at both the input and output for interfacing with the rest of the system and/or measurement equipment. For optimum high- frequency operation of the circuit, the core transistor Q_1 in Figure 8 is sized at 4-times the minimum size as a compromise between gain and parasitic capacitance. The transistors are biased at the collector current for peak-f_T operation. The feedback capacitance between base and emitter is omitted, as the device's own intrinsic base-emitter capacitance is sufficient for that purpose, and a small capacitor C_1 of 10 fF is connected between emitter and ground. This capacitor is added to the interconnect parasitics at this node, which are simulated using EM tools. The resonator inductor also becomes small enough to be implemented as a short transmission line TL_2 connected between the base and ac-ground. Similarly, the load inductor is also implemented as TL_1. Transistors Q_4 and Q_6 are used to bias the current through that branch, and transistor Q_2 is added for quenching the supply through the input *SW*.

Additionally, transistor Q_3 and its bias transistor Q_5 form the injection input buffer, which is not quenched in order to guarantee the presence of the injection signal at the onset of oscillation. Thus, the actual bias current through transistor Q_1 is the sum of the currents in both branches, but the larger current component flows through the quenched branch, so the circuit gain falls below what is required for sustaining oscillation during the off-phase, but is not completely off. The injection input is matched using transmission line stubs TL_3 and TL_4 to the source impedance of 50 Ω, whereas the switch input is resistively matched using the resistor R_m and capacitor C_m.

To overcome the difficulty of controlling the impedance presented to the dc bias points at mm-wave frequencies, due to the inductances of the bias distribution lines becoming more significant, especially for a single-ended design, zero-Ohm lines are employed, which present a very low input impedance that is only dependent on the line dimensions [20], as shown in Figure 9. The circuit core and interconnects were simulated using an EM solver tool and optimized to have an operation frequency of 180 GHz.

2 Cross-Coupled SRO

The common-emitter cross-coupled topology is another very common topology in the domain of mm-wave

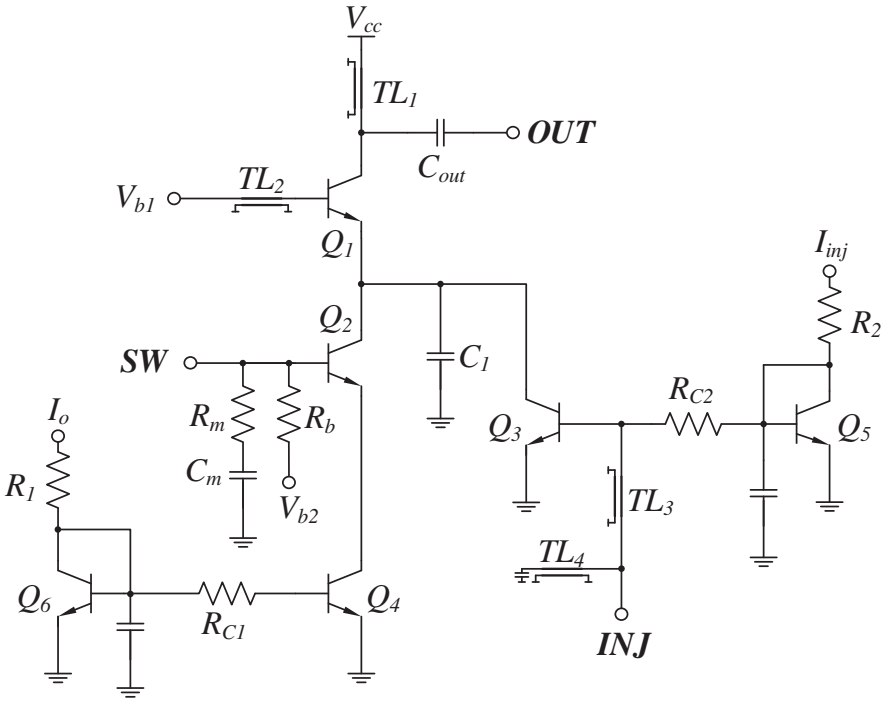

Figure 8: Schematic of SRO regenerative sampling circuit based on the single-ended common-collector Colpitts topology [19].

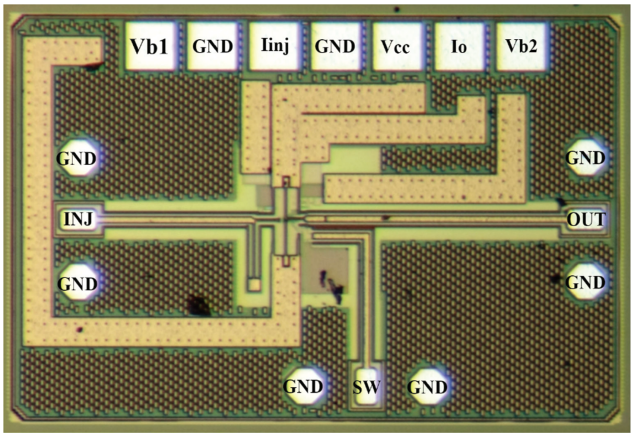

Figure 9: Colpitts SRO regenerative sampling chip photo for mm-wave range operation with total area of 990 µm × 650 µm [19]. Distribution of dc bias is done using multi-layer zero-Ohm lines.

oscillator design. Differential by nature, it enables oscillation from a small core cell through the interconnection of two transistors Q_1 and Q_2, as shown in Figure 10. However, it suffers from an inherent upper limit on its attainable oscillation frequency [22]. This can be alleviated, however, with the help of the series feedback capacitors C_f to reduce the influence of the base-collector capacitance and reach higher speeds. A cascode input stage is implemented as a buffer for injection, and also acts as an active balun through differential operation, enabling injection from a single port, provided that the second port is properly terminated. Two common-collector stages are also added as output buffers for each of the differential outputs. Switching is, again, applied only to the current sources of the core and output buffers, but not to the injection input circuit. Zero-Ohm lines were also used for dc bias distribution, and transmission lines were used for inductor realization (Figure 11). The circuit was simulated using an EM solver and targeted towards an oscillation frequency of 180 GHz.

VI Analog baseband receiver

The baseband I and Q components of the receive signal in Figure 1 are digitized by an analog baseband receiver. Figure 12 depicts the receiver architecture for one of its two channels, which consists of a programmable gain amplifier (PGA), an analog-to-digital converter (ADC) and a field programmable gate array (FPGA) interface. To give more insight into the purpose and function of these receiver components, a brief overview is given in the following. For future integration of the full SPARS receiver in Figure 1, the baseband receiver components are designed in the same SiGe BiCMOS technology as the SROs in Section V.

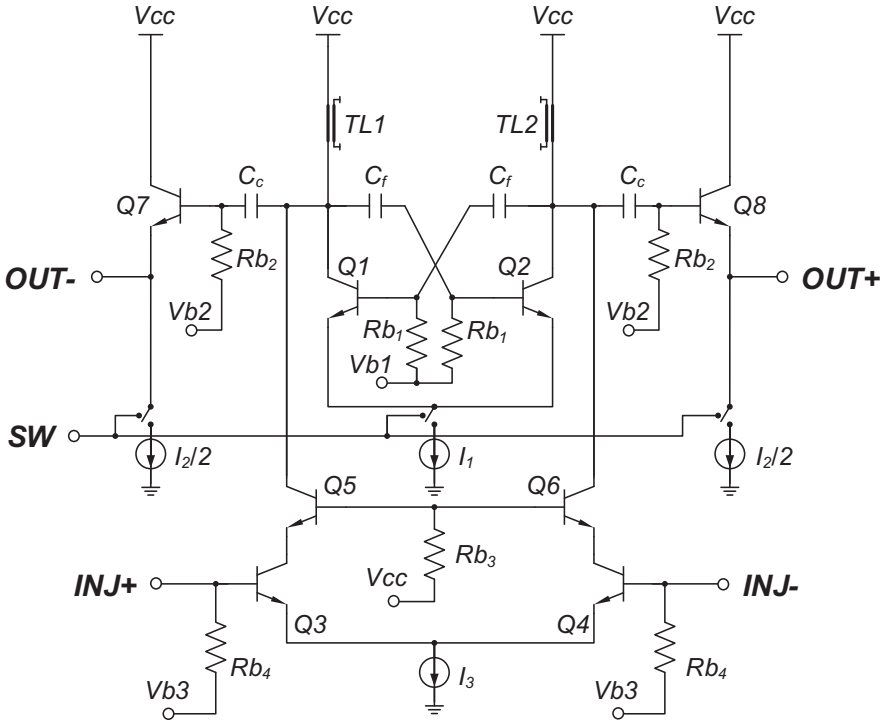

Figure 10: Schematic of SRO regenerative sampling circuit based on the cross-coupled topology [21].

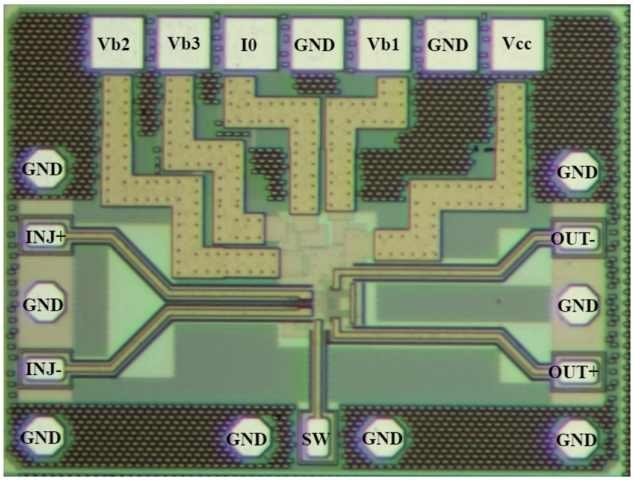

Figure 11: Cross-coupled SRO regenerative sampling chip photo with a total area of 940 µm × 700 µm [21].

A Programmable gain amplifier

The PGAs in the baseband receiver are used for dynamic range improvement (DR) by employing programmable pre-amplification of the ADC input signals. The gain control of the PGAs is realized by a simple, yet effective idea: to overcome gain restrictions in low power supply applications, amplifier designs often exploit multi-stage configurations, as the gains of the individual stages (on a logarithmic scale) sum up in an amplifier chain. If a gain adjustability to either 0 dB or a binary weighted value is now incorporated into each stage, a programmable gain function with 1 dB step size can be implemented. The total gain then is:

$$G = a_{N-1} \cdot 2^{N-1} + \ldots + a_1 \cdot 2^1 + a_0 \cdot 2^0 \ (\mathrm{dB}). \qquad (1)$$

The parameter N denotes the number of stages and the coefficient a_N describes the adjusted gain setting in stage N (a_N = '0' for 0 dB and a_N = '1' for 2^N dB). With this approach a gain range of $2^N - 1$ dB can be covered in 1 dB steps. The PGA with the described circuit concept has been demonstrated as a five-stage amplifier in [24] and [25]. Figure 13 depicts the measured gain of the amplifier for different gain settings and compares the results against RLC extracted simulations. The PGA covers a gain range of 31 dB and exhibits a measured gain accuracy of −0.19/0.46 dB at low input frequencies. At a maximum gain of 25 dB the 3-dB bandwidth is measured to 10.1 GHz, at the minimum gain setting of −6 dB the bandwidth is extrapolated to 14.8 GHz.

B Baseband receiver ADC

The baseband receiver ADC introduced in [23] is designed to enable conversion rates at one tenth of the carrier frequency

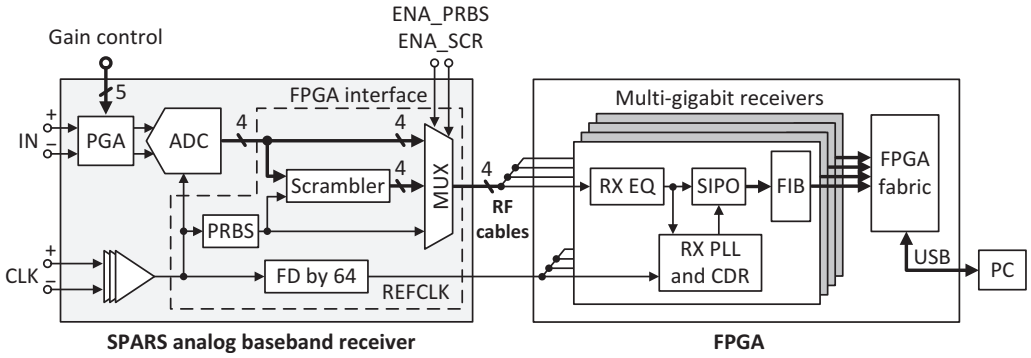

Figure 12: SPARS analog baseband receiver (one channel) connected to FPGA measurement setup [23].

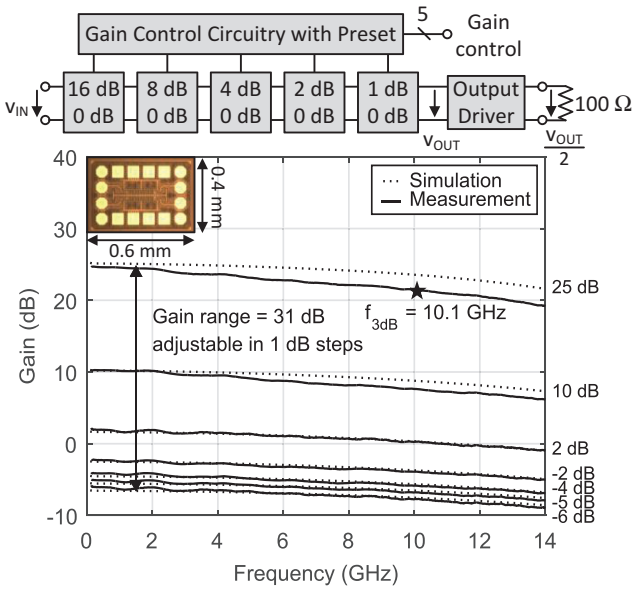

Figure 13: Simulated vs. measured PGA gain [24].

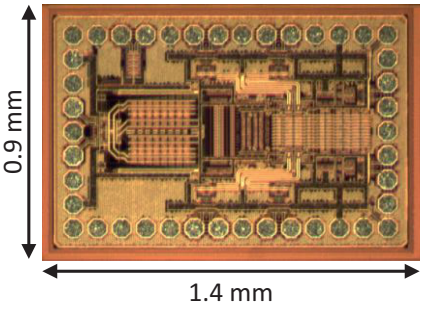

Figure 14: SPARS ADC with integrated FPGA interface.

and beyond. For highest operation speed with one core, the converter uses a flash architecture. Contrary to conventional signal distribution with a track-and-hold amplifier (THA) at the converter front-end, the SPARS ADC uses a traveling wave concept based on delay-matched transmission lines, where input and clock signals travel synchronously from one comparator to the other. Since this concept does not require a high-speed THA with fast settling time, the overall circuit complexity and power dissipation can significantly be decreased at cost of higher data-to-clock skew requirements. To overcome latter timing issues, the ADC incorporates an advanced signal splitting technique with U-shaped comparator positioning. Figure 14 depicts the ADC implementation with the integrated FPGA interface. In experimental tests, the ADC could be demonstrated up to a sampling rate of 42 GS/s. To the best knowledge of the authors, this is the highest sampling rate that has been reported for single-core ADCs up to date. The measurement results and the comparison of the ADC performance against current state-of-the-art ADCs are elaborated in [26]. With the strong system knowledge provided in Section III and the sophisticated mm-wave SRO implementations in Section V, the high-speed ADC can be used for first multi-chip SPARS receiver demonstrator experiments at the target carrier frequency of 180 GHz.

C FPGA interface

After digitization, the receive samples are transmitted at full data speed to four independent multi-gigabit FPGA receivers, which deserialize the incoming bit streams for data storage in the following FPGA fabric. A classical approach with on-chip ADC memory is omitted, as it would require massive ADC parallelization to overcome the speed constraints of the CMOS node in this technology. Furthermore, the circuit complexity and costs of the baseband receiver would significantly be higher with an integrated memory solution, as a sufficiently high number of receive samples has to be stored for system demonstration experiments and for the evaluation of link synchronization parameters (e. g., carrier frequency offset, I/Q phase

misalignment, etc.). Real-time communication between the baseband receiver and FPGA is realized with the help of an integrated FPGA interface consisting of a scrambler, pseudo random bit sequence (PRBS) generator, frequency divider (FD) and multiplexer (MUX). The main function of the FPGA interface is to synchronize the multi-gigabit receivers and to support their clock data recovery (CDR) units. Synchronization is mainly required, because the deserializers (SIPOs) in the FPGA receivers are driven by separate phase-locked loops (PLLs). Due to different PLL lock times and undefined initial flip-flop states in the PLL frequency dividers, the RX SIPOs start operations at different time instants, which manifests as data skew between the multi-gigabit receiver outputs. If the lock times of the PLLs, for instance, only differ by one reference clock cycle, data skew can already be in the range of several bits. To address these issues, the baseband receiver can be set into a PRBS mode prior to SPARS data transmission. In this mode, the receiver sends a synchronous 2^{11}–1 PRBS to all of its four data outputs to enable FPGA-based deskewing. For CDR support, the baseband receiver can be operated in a scrambling mode. This mode ensures that the output data streams of the receiver contain sufficient bit transitions for the CDR units to work reliably. The bit transition density is increased with exclusive-OR (XOR) operations of the ADC outputs and the on-chip generated PRBS. Due to the scrambling of the ADC outputs, the transmitted signal power is spread over several frequency components, which greatly reduces electromagnetic interference (EMI) between adjacent signal lines on the FPGA board. The scrambled ADC outputs can be recovered in the FPGA by equivalent XOR operations of the scrambled data and the PRBS of the baseband receiver, as exemplarily shown in Figure 15 for one ADC output.

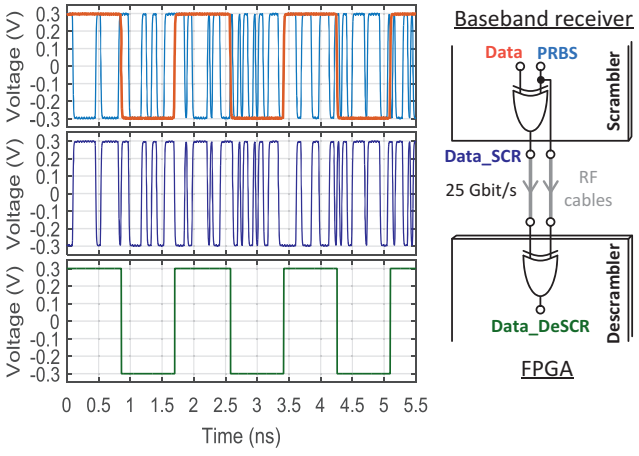

Figure 15: Recovered baseband receiver output in FPGA.

VII Conclusion

During the first project phase, the proposed SPARS concept has been thoroughly analyzed in theory and experimentally verified using scaled demonstrators that allow measurement access to all interfaces. For mm-wave implementation at 180 GHz, component architectures, concepts and prototypes have been investigated in order to exploit the benefits of regenerative-sampling-based amplification in the proposed system architecture. Ongoing research is focused on system integration with the goal to assemble a transmitter and receiver prototype at the target frequency as well as to consider options to extend the concept towards multichannel systems.

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