Lebanese University
Doctoral School of sciences and technologies

Università degli Studi di Cagliari

# DOTTORATO DI RICERCA

IN INGEGNERIA ELETTONICA E INFORMATICA DRIEE

Ciclo XXVI

# TITOLO TESI

REDUNDANT ANALOG TO DIGITAL CONVERSION ARCHITECTURES IN CMOS TECHNOLOGY

Settore/i scientifico disciplinari di afferenza

ING-INF/01(ELETTRONICA)


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Esame finale anno accademico 2013 - 2014

# Acknowledgment

First of all, I would like to say Alhamdulillah, for giving me the strength and health to do this project work until it was done. I am heartily thankful to my supervisors, Prof. Massimo Barbaro, Prof. Hussein Chible and Prof. Luigi Raffo, whose encouragement, guidance and support from the initial to the final level enabled me to develop an understanding of the subject. Finally, I offer my regards and blessings to all those who supported me in any aspect during the completion of this project.

# Dedication

To my parents, who have sacrificed so much for me.

To my sisters and brothers, who have provided the extra motivation to finish my PhD.

To everyone, who helped me during my thesis period.

# Author’s Declaration

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# Abstract

The operation of modern electronic devices in different fields as communications, signal processing, and sensor interface is critically affected with robust, high performance and scalable Analog-to-Digital Converter (ADCs), that can be considered as one of the main blocks in many systems, since they are mandatory to make the link between the analog outside world and the evermore-ubiquitous digital computer world. The design of these ADCs come distinct tradeoffs between speed, power, resolution, and die area embodied within many data conversion architectural variations.

The flash ADC structure are often the base structure for high-speed operation and simple architecture analog-to-digital converters (ADCs). As the input signal is applied to $(2^N - 1)$ comparators generating N bits as resolution of converter, which leads to exponentially increase of the number of comparators and die area occupied when ADC resolution increase. Normally Flash resolution is limited to 6 - 8 bits.

To reduce hardware complexity flash converters can be extended to multi-step ADCs, by using $m \times 2^n$ instead of $2^{m \times n}$ comparators for a full flash implementation assuming $n_1$, $n_2$, ..., $n_m$ are all equal to n. Pipeline,

algorithmic, and SAR structures have been widely used converters medium to high-resolution application such as video and wideband radio, benefiting from their flexibility and effective trade off among power dissipation, speed and resolution.

To correct the non-linearity errors, different types of redundancy are proposed in literatures for different ADCs architectures, specially pipeline and multi-stages ADCs [1]. They having the same role of correcting and tolerate over-range errors coming from non-idealities resulting from capacitor mismatches and finite Op-amp gain , by adding extra quantization levels of redundancy performed the input to an ADC stage while maintain the same overall resolution.

This thesis proposed a user adjustable conventional restoring Analog to Digital converter circuit with Z added levels (CRZ) of redundancy [2]. The proposed circuit will be able to take predetermined values of Z. A fat-tree encoder allows flash converter to benefit from Z-additional levels to make the conversion of ($2^M$-1+Z) thermometric code to (M+1) bits (number of bits per stage); an additional extra bit is generated each cycle to perform the additional levels of references Z. The extra bit will used to tolerate Multi-bit Digital to

Analog Converter MDAC for the second stage of conversion by applying a digital correction at the final binary output code. A 5-bits analog to digital converter will be designed and simulated using Cadence virtuoso.

**Index Terms**: Analog-to-digital converter, Flash ADC, Multi-stage ADCs, redundant sign digit (RSD), Z-additional levels of redundancy, fat-tree encoder, and digital correction.

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# List of abbreviation

ADC: Analog to digital converter.
A/D: Analog to digital conversion.
CRZ: Conventional Restoring converters with Z additional levels.
CMRR : Common-mode rejection ratio.
DAC: Digital to Analog converter.
D/A: Digital to Analog conversion.
DNL: differential nonlinearity.
ENOB: Effective number of bits.
fs: Sampling frequency
FoM: Figure of Merit.
FFT: Fast Fourier Transfer.
K: scaling factor.
INL: integral nonlinearity.
LSB: last significant bit.
MSB: most significant bit.
MDAC: multi-stages digital to analog converter.
MS/s: Mega-samples per second.
N: Number of bits/resolution of converter
Nb: number of bits.
Nfs: effective resolution.
RMS: root mean square
SNR: signal to noise ratio.
SINAD: Signal-to-Noise and Distortion.
SFDR: Spurious Free Dynamic Range.
$u_e$ : unit element
$V_{FS}$: Full-scale reference Voltage.

# Chapter 1: Introduction

## *1.1- Analog-to-Digital Converter*

Nowadays electronics equipment is the most frequently used in different fields such as communication, transportation, entertainment, etc. This evolution is led by the evolution of the integrated circuits especially at the level of digital signal processing.

Continuous scaling of integrated circuits technology accordance with respect to Moore's law (figure 1) lead to great advancements in cost, performance and power of digital integrated CMOS circuits. Unfortunately, it is not the case of analog circuits, where some performance improvement have occurred, nevertheless, they were not as rapid and fruitful as they were for digital circuits.

Whereas, to earn the same benefits for analog circuits, a large number of blocks have to be redesigned in accordance with the new technology parameters. In addition, to overcome analog imperfections some innovations at the circuit level are always necessary.

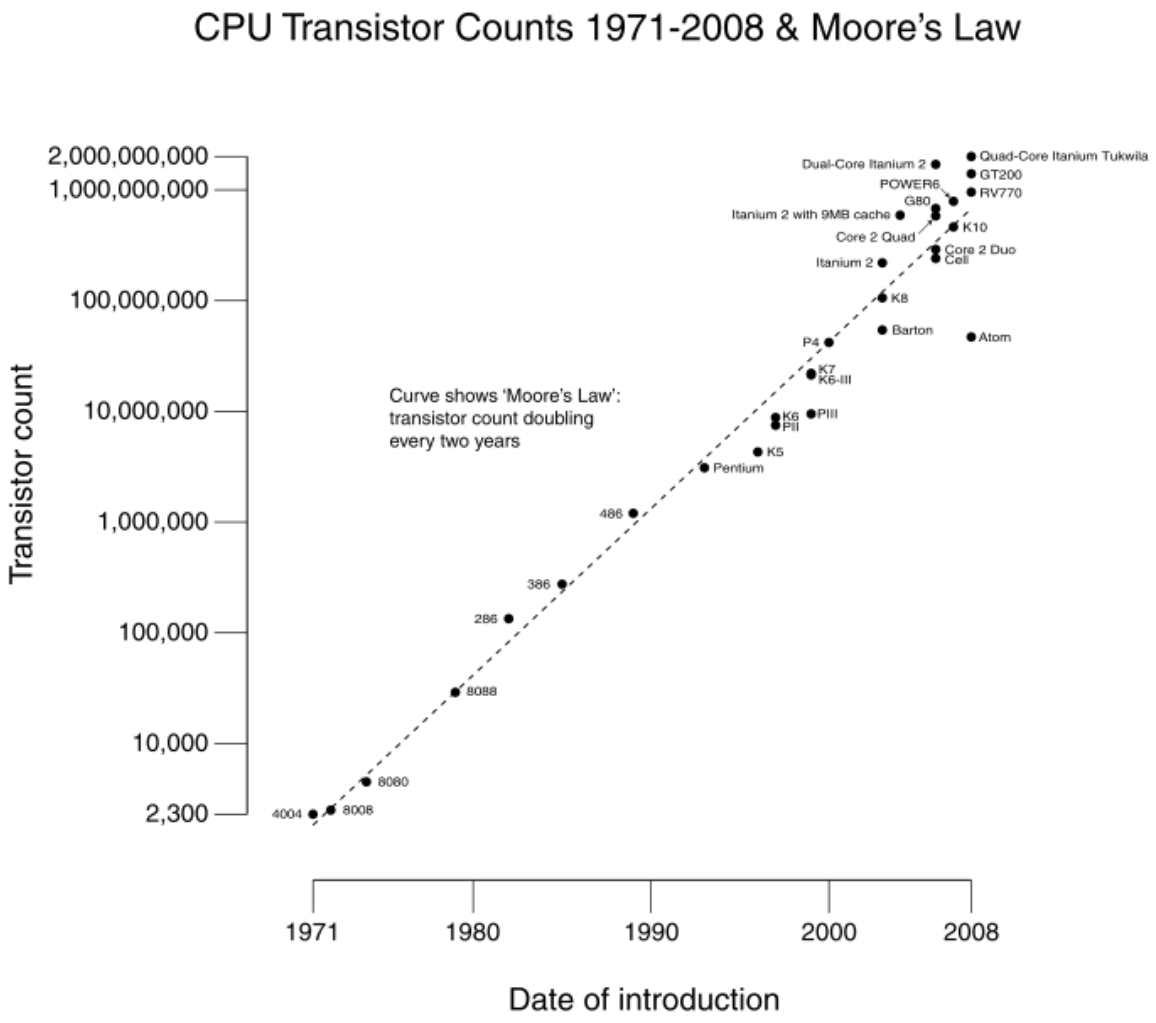



*Figure 1: Moore's law*[1]

Hence, digital circuits are more attractive not only form economics point of view, but also it become more advanced and achieving higher operating speeds. As result, designers have always tried to migrate more circuit functionality from analog into the digital domain where the most of analog operations can be equally performed digitally.

[1] *(http://en.wikipedia.org/wiki/File:Transistor_Count_and_Moore%27s_Law_-_2008.svg)*

That is supposed theoretically, all circuits should become digital circuits. However, most of the signals are analog by nature, meaning that in order to capture or produce such signals they must be in an analog form. As analog-to-digital (ADCs) conversion and digital-to-analog (DACs) conversion consist of the interface between analog and digital worlds, allow the using of modern signal processing systems to handle a complex signal by digital circuitry as showing in figure 2. Therefore, no matter how much functionalities are performed digitally, it will be always remain a need for data converters in both forms, analog-to-digital converters (ADCs), and digital-to-analog converters (DACs). Generally, Analog to digital conversion (A/D) requires more power and circuit complexity than digital to analog conversion (D/A) to achieve a given speed and resolution, ADCs frequently limit performance in signal processing systems [3].

ADC converters are extensively used in various applications as showing in table 1. Those applications can be divided according to speed or frequency and resolution as showed in Table.2.

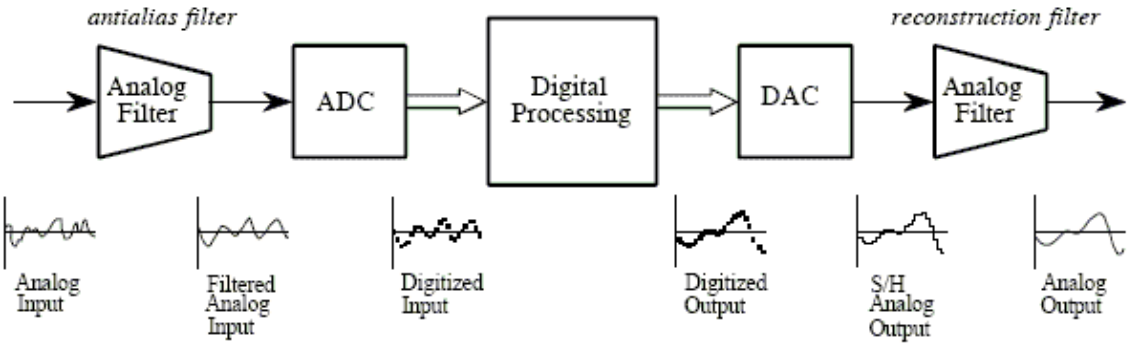



*Figure 2: Digital Processing of Analog Signals (The Scientist and Engineer's Guide to Digital Signal Processing).*

In order to benefit from technology advance and digital systems scalability and integrability, it necessary to scale down also the ADCs. That is impose the using of pipelined or multi-stages ADCs. The reason for pipeline ADCs efficiency is the concurrent operation of the pipelined stages. Each stage processes a new sample as soon as its residue is sampled by the following stage, which leads to a high throughput of one sample per clock cycle.

By resolving a certain number of bits per stage, the operation speed and resolution are decoupled from each other [4]-[5]. Non-idealities such as static device mismatch and dynamic timing mismatch, in different architectures of multi-steps analog to digital converter affect the redundancy and performance at the output of an instrument. That is impose the using of digital output correction at each cycle allows large offset error in the comparator. Hence,

fairly simple dynamic latch-type comparators can be employed to further reduce power consumption.

*Table 1: Various application analog to digital converters vs numbers of bits and frequency*

| **Application** | **ADC specifications** | |
|---|---|---|
| | **Nb of bits** | **Frequency** |
| Instruments | >20b | < 1kHz |
| Digital Audio | 16-18b | > 44kHz |
| Medical Imaging | > 12b | > 5MHz |
| Communication | > 14b | > 65MHz |
| Digital Camera | > 12b | > 20MHz |
| HD TV | 10b | > 150MHz |
| Cam coders | 10b | > 15MHz |
| Disk Drivers | 6b | > 500MHz |

A pipeline architecture ADCs is the better choice for medium resolution approximately 8 to 14 as showed the figure 3 , medium speed sampling ranging from a few Mega-simple/second (MS/s) to hundreds of MS/s, which have many applications, e.g. video, wireline and wireless communications. For such applications, pipelined ADC has great advantage compared to flash and sigma-delta ADCs.

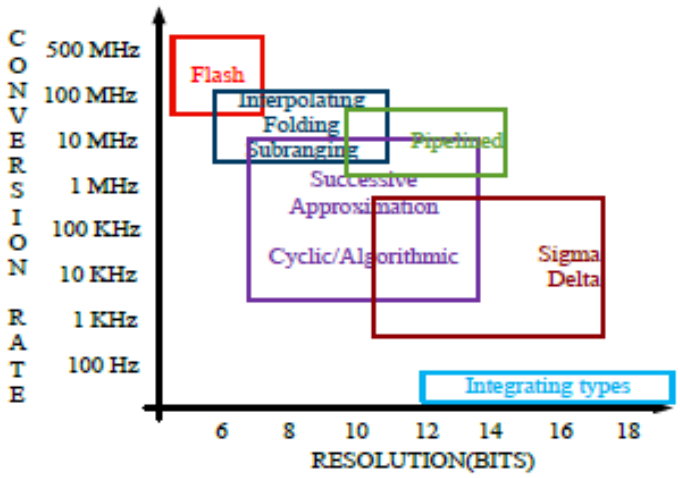



*Figure 3: Comparison of ADC Architectures vs. Resolution and Sample rate (Willy Sansen).*

*Table 2: Domains of using analog to digital converters.*

| | | |
|---|---|---|
| Medical imaging | Direct Conversion | VDSL, XDSL & HPNA |
| Antenna Array Position | Radar, Infrared Imaging | Tape drives |
| Portable instrumentation (battery) | Medical scan converters | Film Scanners |
| Positron Emission Tomography | Digital Receiver | Power amplifier linearization |
| IF sampling | Single Channel Radar, Sonar and Satellite Subsystems | Phased Array Receivers |
| Handheld oscilloscope | Optical networking | Data Acquisition |
| MRI receivers | Communication Subsystem | Broadband wireless |
| CDMA2k, WCDMA, TD-SCDMA. Digital oscilloscope | Power-sensitive military applications | Secure Communications |
| Nondestructive ultrasound | Broadband access | Bill Validation |
| IS95, CDMA-One, IMT2000 | Wideband Carrier Frequency System | Quadrature radio receivers |
| Spectrum analyzers | Astronomy | Digital Receivers |
| Ultrasound | Broadband LAN | Motor Control |
| BS Infrastructure | Point to Point Radio | Cable ReversePath |
| Communications instrumentation | Flat panel displays | Antenna array processing |
| Ultrasound beam forming system | Communications (modems) | Industrial Process Control |
| AMPS, IS136, (W)-CDMA, GSM | GPS Anti-jamming Receiver | Communications receivers |
| Instrumentation | Projection systems | Antenna array processing |
| X-ray imaging | Powerline networking | Optical Sensor |
| Wireless Local Loop, Fixed Access | MMDS base station | Diversity radio receivers |
| I & Q Communications | CCD imaging | Digital Receivers |
| Vsat terminal / receiver | Home phone networking | Cable Head-End Systems |
| | Wireless Local Loop (WLL) | Viterbi decoders |
| | Set-Top Boxes | Video Imaging |
| | DSP front-end | Test & measurement equipment |
| | | Multimedia |
| | | WLAN |

## *1.2- Motivation and Objectives*

With the outgrowth of pipelined ADCs in many consumer products, improving the performance of such ADCs has enticed much attention. Areas of improvement include linearity enhancement, and power reduction.

Linearity enhancement has been an active area of research as with deeper sub-micron technology low intrinsic gain and low supply voltages have made achieving very linear data converters (i.e.>10-bit linear) challenging using conventional pipelined ADC design techniques.

Low power consumption, on the other hand, is motivated by two main situations, (1) for battery operated systems, low power consumption means prolonged battery lives, and (2) for wired systems, where many ADCs can be integrated on-chip in parallel, large net power consumption can generate high amounts of heat requiring expensive packaging for heat dissipation. Thus techniques to reduce power consumption in pipelined ADCs enable more cost effective integrated circuits for both mobile and wired systems.

The aim of this work is investigating solutions on architecture, system, and circuit levels that guarantee the redundancy of the final output of multi-stages ADCs.

We propose to study and compare the characterization of CRZ (Conventional Restoring converters with Z additional levels) and RSD (Redundant Sign Digit) multi-stage A/D converters, by estimating the errors introduced by each of the internal blocks. In addition, designing and simulating a Z-configurable or adjustable circuit able to do conversation A/D with Z addition levels of redundancy.

In an attempt to address these issues, this thesis specifically, focus on:

i) Modulation of analog to digital based at two models, behavioural and circuital model, in order to improve the redundancy of MADC (multi-stage analog to digital converters), based on two methods of correction, conventional restoring with additional levels (CRZ), and Redundant Signed Digit (RSD).

ii) Development of CMOS configurable circuit able to applied predefined values of Z-additional of redundancy in the same circuit will be a great enhancement in testing and verifying the theoretically results produced by modulations models.

## *1.3- Thesis Organization*

The next chapters of this thesis will be as follows:

Chapter 2 demonstrates the analog to digital conversion process fundamentals with a brief about different ADC architectures. Then different ADC performance metrics and error sources are mentioned.

Chapter 3 presented briefly the flash converter and the multi-stages analog to digital converters (MDAC), then the two methods of redundancy CRZ and RSD.

Chapter 4 introduced a behavioral model for pre-simulated the circuit design with different proposed sources of errors.

Chapter 5 presents two different approaches for design and study the MDAC based in circuital model and AMS technology.

Chapter 6 shows the full custom design of chip by using cadence design.

Chapter 7 presents the general conclusion and the future work.

# Chapter 2: ADC Performance Metrics

This chapter discussed briefly the basic procedure of analog to digital conversion and shortly presented the basic operations such as sampling and quantization. We defined also the different metrics used to characterize Static and dynamic performance of ADCs converters. Finally, the sources of errors common to the process of analog to digital conversion are presented and explained.

## *2.1- Basic Conversion Process*

Converting an analog signal that is continuous in time and amplitude into a digital signal that is discrete in both time and amplitude is the main function of an ADC.

Sampling, quantizing and binary encoding are fundamental operations of digital convertion, a pre-filter is a necessary to limit the input signal bandwidth of the ADC. The final digital output of an N bits ADC, where N is the resolution of the converter, is a bit sequence ranging from the most significant bit $b_{N-1}$(MSB) to the least significant bit $b_0$ (LSB) can be represented as: Dout = $b_{N-1}$, $b_{N-2}$, ...., $b_1$, $b_0$

The equivalent analog counterpart of the digital word can be defined as:

$$V \cong V_{FS} * \sum_{i=0}^{N-1} b_i \,.\, 2^i$$

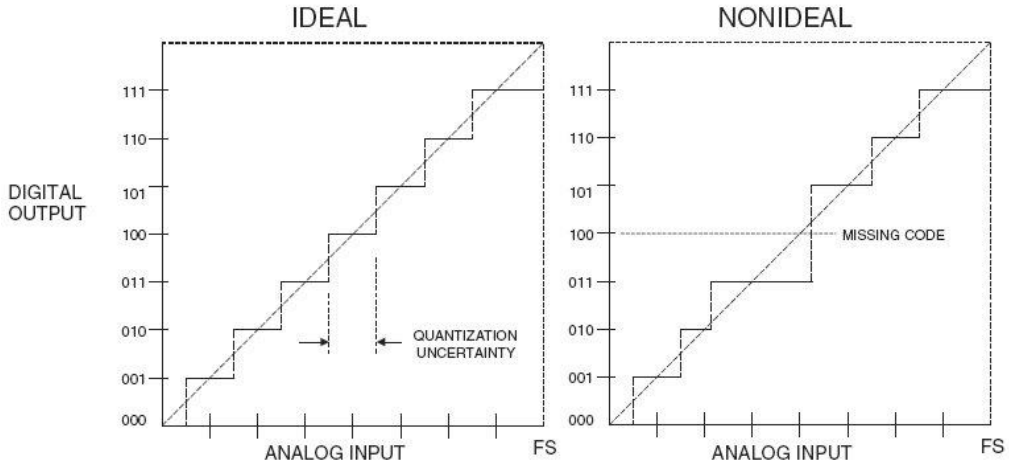
The full-scale range $V_{FS}$ is the maximum analog input range that can be quantized. An ideal N bits quantizer divides this full scale into uniform quantization levels. The quantization step size represents the analog equivalent of 1 LSB of the quantizer and is given by: $\frac{V_{FS}}{2^N}$

New challenges introduced in the integrated design created by technology scaling where the reduction of $V_{FS}$ bonded by the power supply lead to tight LSB step.

## *2.2- ADC Performance Metrics*

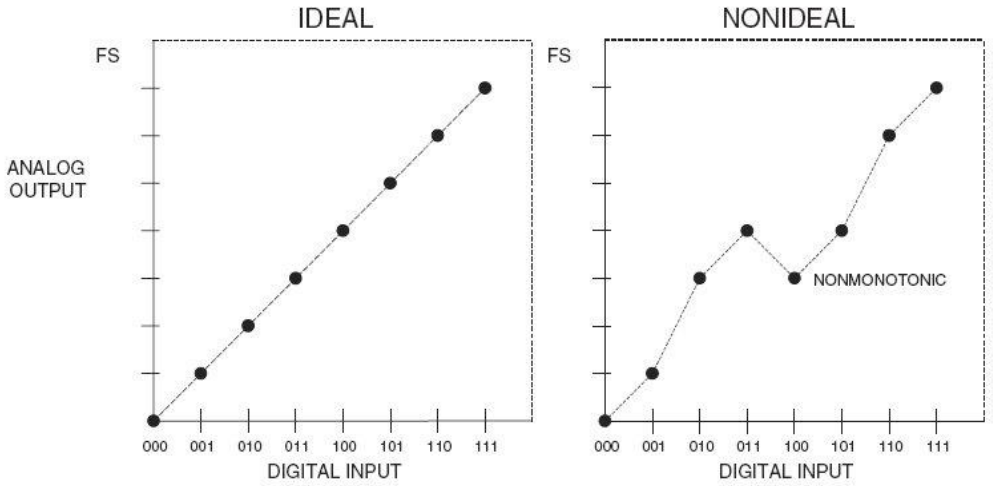
The real input-output transfer characteristics of ADCs and DACs almost have a deviation from the ideal one. There are almost random and uncorrelated errors in the input-output of the quantization intervals as shows in the figure 4 and figure 5. The figures show ideal characteristics of ADC and DAC figure 4.a and figure 5a.a respectively; where in figure 4.b and figure 5.b a real case (non-ideal) is presented with a missing code in case of ADC and no monotonic errors in DAC characteristics. These features are quantified

by the integral nonlinearity (INL) and differential nonlinearity (DNL), two of the static ADC performance metrics defined below.




*(a)* *(b)*

*Figure 4: ADC transfer curve (a) ideal (b) real.*




*(a)* *(b)*

*Figure 5: DAC transfer curve (a) ideal (b) real.*

### 2.2.1- Basic Performance Metrics

#### *2.2.1.1- Accuracy*

Accuracy is defined as the total error of converting a known voltage with an ADC converter, including the effects of quantization error, gain error, offset error, and nonlinearities.

#### *2.2.1.2- Resolution*

The resolution of the converter describes the number of discrete values it can produce over the range of analog values. The resolution of a n-bit ADC is a base 2 logarithm in function of how many parts the full scale input signal can be divided into. The formula to calculate resolution is $2^n$. Thus, high resolution that ADC can resolve smaller signals leads to output that is more accurate.

#### 2.2.1.3- Input Signal Swing

Input signal swing indicates the allowable range of values for the input. The input signal swing indicates the maximum and minimum values that the input signal may have without driving the ADC out of range or resulting in an unacceptable level of distortion.

#### 2.2.1.4- Conversion Speed

Conversion speed, or sampling rate of ADC, indicates the rate the input signal is sampled per second.

#### *2.2.1.5- Power Dissipation*

This is the total power dissipated by an ADC under normal operation. Reducing power dissipation can reduce system consummation and improve battery life, also make it easier to keep the temperature of the ADC at a reasonable level.

### 2.2.2-Static Performance Metrics

#### *2.2.2.1-Offset Error*

Offset error also known as Zero Scale Error or Zero Scale Offset Errors showed in figure 6 is the difference between the first measured transition point and the first ideal transition point. This error can be positive or negative

depends on position of the first transition point with respect to ideal one, it is positive for higher transition than the ideal and negative for lower transition.

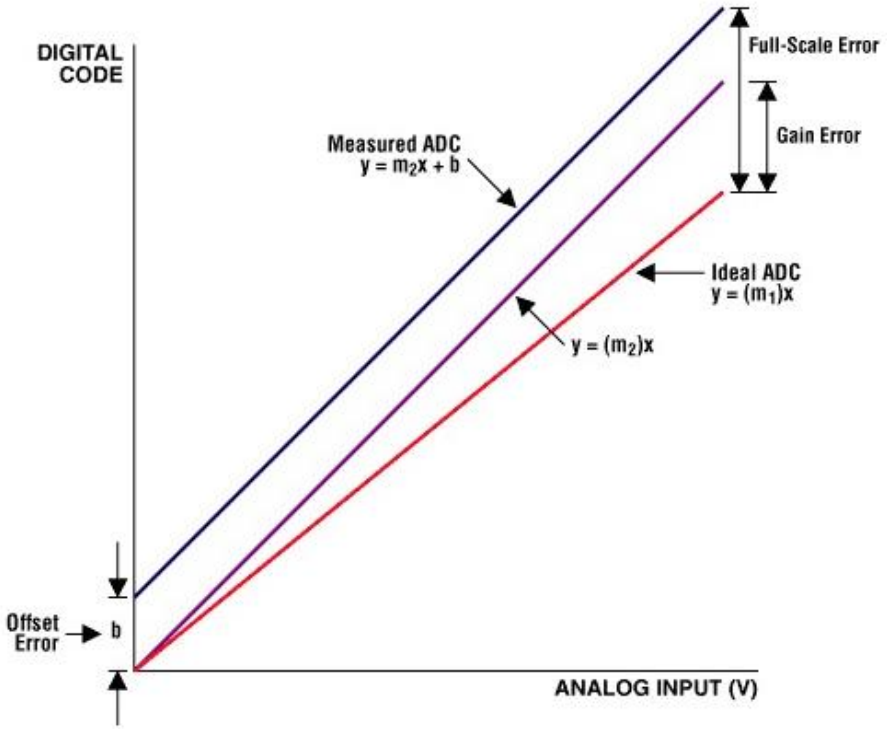



*Figure 6: ADC offset, full scale, and gain errors, (m1 and m2 are the slopes of ideal and measured function respectively).*

### *2.2.2.2- Full-Scale Error*

Full-scale error is the difference between the actual last transition voltage and the ideal last transition voltage. As figure 6 show, it measured at the last ADC

transition on the transfer-function curve and compared against the ideal ADC transfer function.

#### *2.2.2.3- Gain Error*

Gain Error or Adjusted Gain Error is the difference in the slope of the Actual and the Ideal Straight-Line Transfer Functions. The error is not measured as a slope but rather as the difference in the total available input range from the first to the last conversions between the Ideal and Adjusted Straight-Line Transfer Functions as presented in figure 6. It is usually expressed in LSB or as a percent of full-scale range (% FSR), and it can be calibrated out with hardware or in software.

It is important to notice that gain and offset errors are not considered as linearity errors, since the ADC code transitions behavior still occur at uniformly spaced paces forming an ideal straight line.

### *2.2.3- Differential Non Linearity (DNL)*

DNL is affected by the internal design of the ADC and DAC, it resulting of internal capacitor mismatch, dielectric absorption and leakage, settling, as well as internal reference settling, and comparator performance.

The difference between the actual input code width and that of an ideal code as presented in Eq.2.1 is defined as DNL. Input code width is a range of given input values that produces the corresponding digital output code. In general, the difference between the ideal 1 LSB and the actual 1 LSB step is very small. The DNL error is shown in the figure 6.

$$DNL(k) = \frac{((S_{i+1} - S_{i}) - V_{LSB})}{V_{LSB}} \quad (2.1)$$

Where S(i) is the ADC transfer function at a single code (i) and VLSB is the ADC's LSB

### *2.2.2.4- Integral Non Linearity (INL)*

Unlike DNL, INL introduced by non-idealities resulting of the limitations in common-mode rejection ratio (CMRR), slew rate, and settling from the signal chain preceding an ADC or DAC. Integral non-linearity error (INL) is the

difference between the ideal code transition point and that of an actual code transition point. The INL representation shows the sum of the DNL errors eq.2.2. The figure 7 and figure 8 shows the INL and DNL errors, horizontally and vertically measured in ADC and DAC respectively.

$$INL(k) = \sum_{i=1}^{k-1} DNL(i) \qquad (2.2)$$

The equation tells that the INL of code k is equal to the integration of DNL from code 1 to code k-1.

If the INL specification is less than or equal ± 1/2 LSB there no missing codes in ADC. When the ADC is specified to have no missing codes, then this specification does not automatically imply an INL error smaller than or equal ± 1/2 LSB.

### 2.2.3- Dynamic Performance Metrics

Static errors do not include any information about noise and high frequency effects. Static error is tested by a DC signal. Dynamic error provides additional information of ADC performances such as SNR, SFDR, SINAD and ENOB. Dynamic error is tested with a periodic waveform.

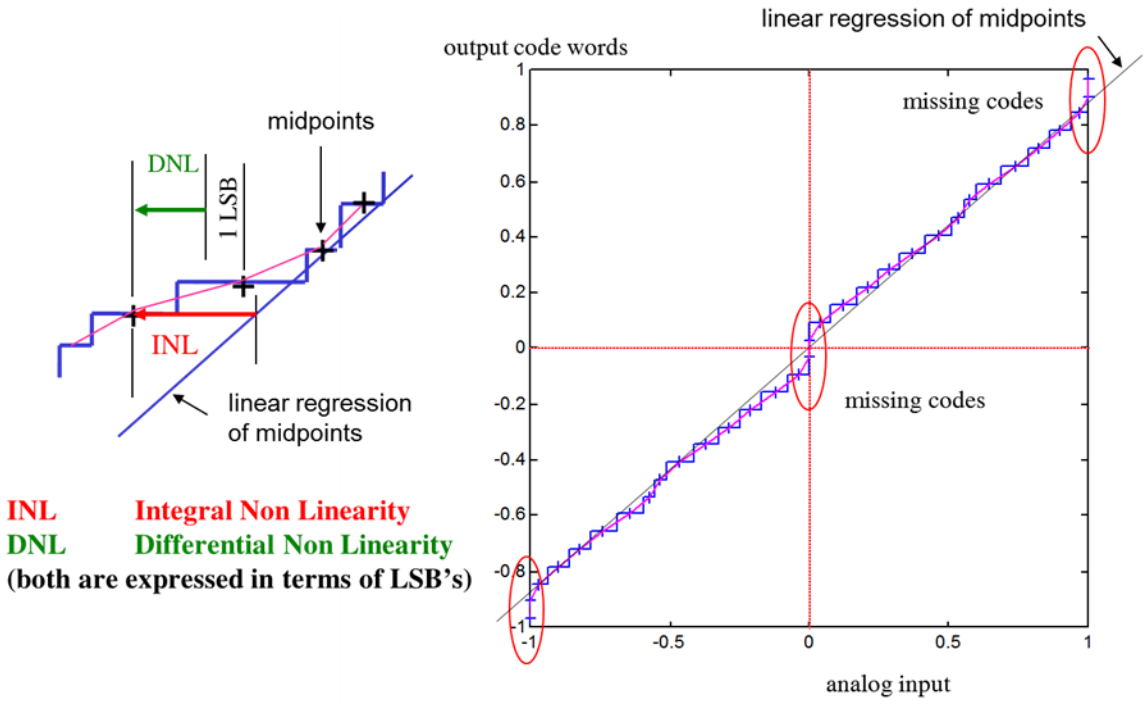



*Figure 7: ADC linearity errors INL & DNL. (P.G.A. Jespers).*

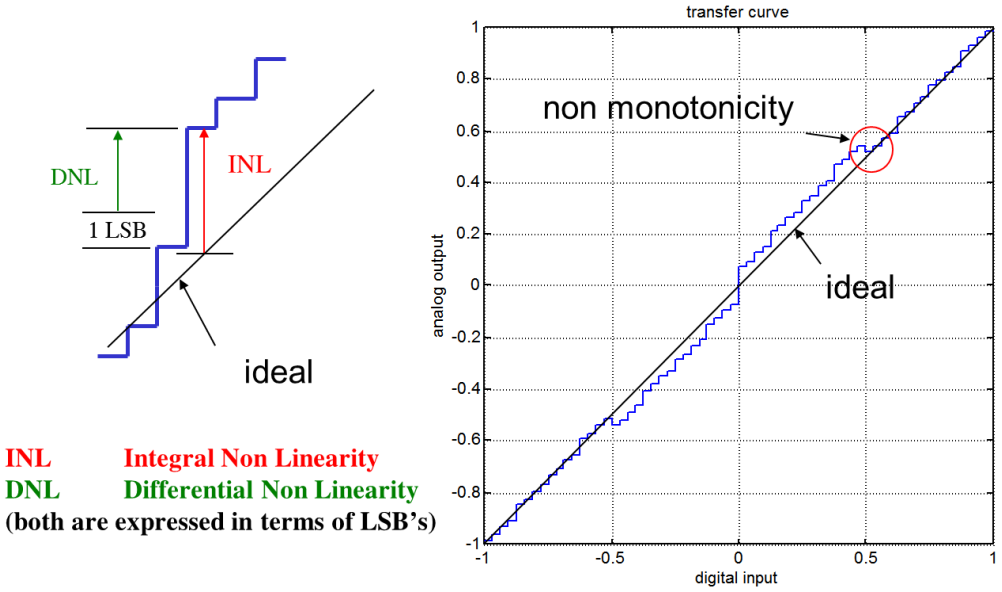



*Figure 8: DAC linearity errors INL & DNL.( P.G.A. Jespers).*

### *2.2.3.1- Signal-to-Noise Ratio (SNR)*

SNR ratio can be defined in terms of the power of a full-scale input signal to total noise power present at the output of a converter. SNR included the quantization noise and the circuit noise, but not the harmonics of the signal. As the accuracy of the comparator(s) in the ADC degrades with higher input slew rates tends to degrade the SNR as the frequency increases.

The SNR can be measured by performing the fast Fourier transform (FFT) of the digital output yield of sinusoidal signal applied at the input of the converter, mathematically expressed as in equation 2.3, 2.4 and 2.5.

$$SNR = 10 * log\ (\frac{S}{N}) \tag{2.3}$$

Where S is the signal power, and N is the total noise power. The maximum achievable theoretical SNR is given by:

$$SNR = 20 * \log\left(2^{(n-1)} * \sqrt{6}\right) \tag{2.4}$$

$$SNR_{max}(dB) = (6.02n + 1.76) \tag{2.5}$$

### *2.2.3.2- Signal-to-Noise-and-Distortion Ratio (SNDR)*

Signal-to-Noise And Distortion (SINAD) can also be referred to Signal-to-Noise and Distortion Ratio (SNDR) or Signal-to-Noise Plus Distortion (S/N+D). A combination of SNR and THD specifications, SINAD is the ratio of the power of a full-scale input signal to total noise power present at the output of a converter including that of the harmonics.

As it compares all undesired frequency components with the input frequency, it is said to be an overall measure of ADC dynamic performance. Mathematically, SINAD is expressed as in equation 2.3.

$$SINAD = 10 * log(\frac{S}{N+D}) \quad (2.6)$$

Where D is the distortion power due to all harmonics in the interested band.

### *2.3.3- Spurious Free Dynamic Range (SFDR)*

SFDR is defined as the strength ratio of the fundamental signal to the strongest spurious in the output. The spur is generally an harmonic of the input tone as

showed in figure 9 In general SFDR is measured in terms of dBc (with respect to carrier frequency amplitude) or in dBFS (with respect to ADC full-scale range).

$$SFDR = 10 \cdot log(\frac{A_1^2}{A_{spur}^2}) \quad (2.7)$$

Where $A_1$ and $A_{spur}$ are the RMS values of the fundamental and spurious component respectively.

### *2.2.4- Total Harmonic Distortion (THD)*

THD is the ratio of the RMS total of the first given number harmonic components to the RMS value of the output signal and relates the RMS sum of the amplitudes of the harmonics to the amplitude of the fundamental. It is usually specified up to a certain number k of harmonics. The $k^{th}$ order THD is expressed in (2.8)

$$THD_k = 10.\log \sum_{i=2}^{k} \frac{A_i}{A_1} \quad (2.8)$$

where $A_i$ is the rms of the $i^{th}$ component.

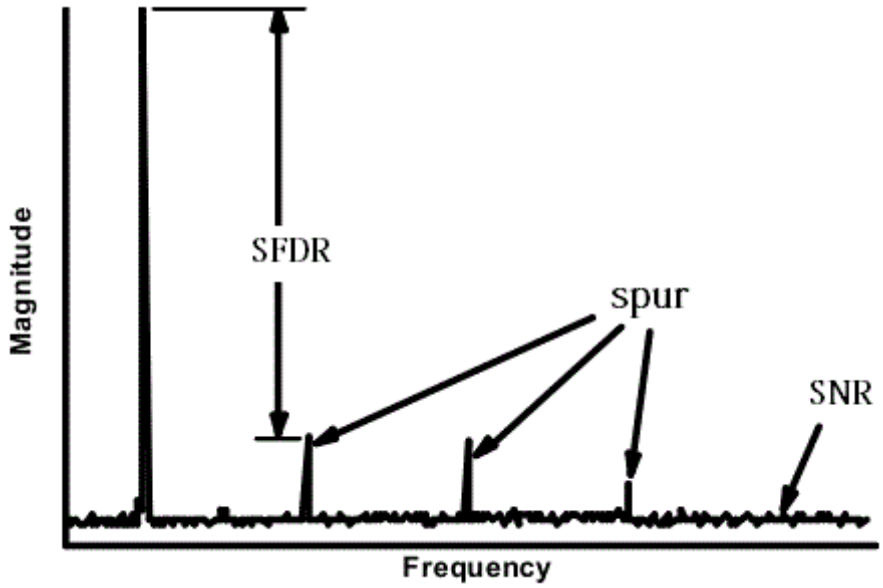



*Figure 9: Spurious Free Dynamic Range.*

### *2.3.5- Effective Number of Bits (ENOB)*

ENOB known as Effective Number of Bits or Effective Bits at low signal frequency is another specification that helps in measuring the dynamic performance and the accuracy of ADC. The resolution of the ADC is usually specified in terms of bits that represents the analog value. It means that the ADC is equivalent to N bits as far as SINAD is concerned. That is, a converter with an ENOB of 7.0 has the same SINAD as a theoretically perfect 7-bit converter. Mathematically, ENOB can be calculated as shown in equation 2.9.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (2.9)$$

### *2.3.5- Effective resolution (Nfs)*

Will the ENOB is a measure of the signal-to-noise and distortion ratio used to compare actual analog-to-digital converter (ADC) performance to an ideal ADC extrapolating the SNR from small to full-scale signal [6]. The effective resolution ($N_{fs}$) measure from the SNR taking into account the loss of resolution due to the large signal distortions computed for a full-scale input signal as showed in figure 10 . $N_{fs}$ in general less than ENOB number.

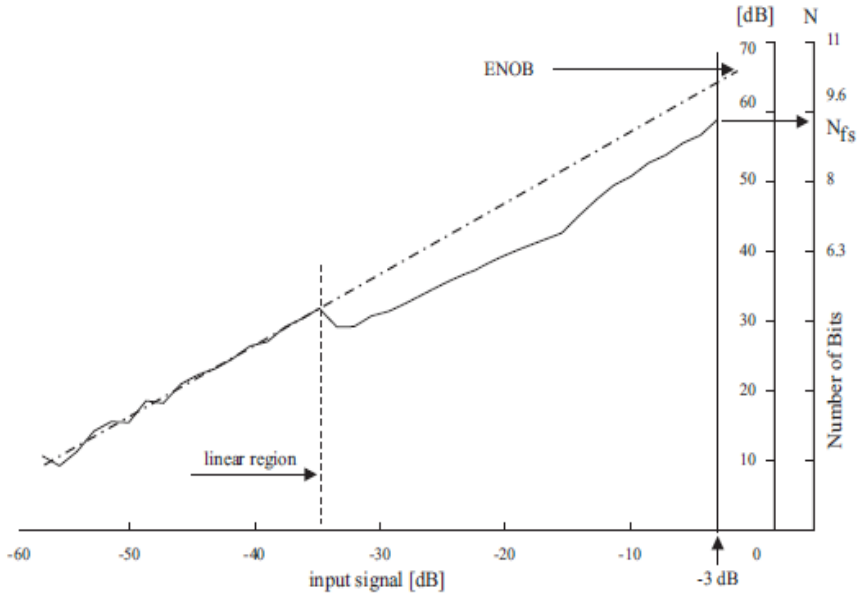



*Figure 10: ENOB versus Nfs.*

### 2.2.4- Figure of Merit (FOM)

The performance of the ADC's can be evaluated fairly, based on the figure of merit, which combines the contradicting parameters in the design. The most common FOM used is defined as:

$$FOM = \frac{Power}{2^{ENOB} \times f_s} \quad (pJ/step) \tag{2.8}$$

Where $f_s$ is the sampling frequency of ADCs.

In order to compare high resolution ADCs limited by thermal noise, a slight variation of equation (2.8) is proposed in equation (2.9) where the ENOB is multiplied by 2 to account for the fact that due to thermal noise limitations, to achieve twice the resolution × 4 the power is required.

$$FOM = \frac{Power}{2^{2 \times ENOB} \times f_s} \quad (pJ/step) \tag{2.9}$$

In general similar FOMs can be achieved with different ADC topologies, however it is noted that ADCs with lower resolutions tend to be able to achieve better FOMs using equation (2.8).

## *2.3- Conclusion*

In this chapter, basic A/D and D/A conversions definitions and concepts are explained showing a comparison of the real transfer curve of ADC and DAC. The Basic static and dynamic ADC performance metrics have been identified. Finally a figure of merit is presented to evaluate different performance of ADCs.

# Chapter 3: Multistage Analog to Digital Converter

## *3.1- Introduction*

Since the existence of digital signal processing, ADCs have been playing a very important role to interface analog and digital worlds as we introduced before. They perform the digitization of analog signals at a fixed time period, which is generally specified by the application. The A/D conversion process involves sampling the applied analog input signal and quantizing it to its digital representation by comparing it to reference voltages before further signal processing in subsequent digital systems. Depending on how these functions are combined, different ADC architectures can be implemented with different requirements on each function. To implement power-optimized ADC functions, it is important to understand the performance limitations of each function before discussing system issues.

Many architectures of A/D converters are proposed in the literature, each with their own set of characteristics and capabilities to be used in different applications.

Multi-stage or mutli-steps analog-to-digital converters are the dominant choice of cyclic converters in applications that require both mid speed and

high accuracy, such as video and wideband radio, making compromise between minimizing the die area of the chip and power consumption.
Non-idealities such as static device mismatch and dynamic timing mismatch, in different architectures of multi-steps analog to digital converter affect the redundancy and performance at the output of an instrument.

In this Chapter, we would like to introduce the structure and basic operation of flash converter and multi-stage ADC. In addition, the different common errors source that affect the conversion process.

After we understand the basic ideas of the pipeline ADC, in the second part of this chapter, we will discuss the redundant sign digit (RSD) and the conventional restoring with Z additional levels of redundancy (CRZ) redundancy methodologies lead to an accurate A/D conversion process.

## *3.2- Flash ADC*

Flash ADCs know also as Direct-Conversion or parallel ADCs is the fastest converter topology available today. However, the main drawbacks of the conventional flash is the number of necessary hardware requirement to complete the A/D conversion procedure, it increases exponentially as the

number of bits increase because a bank of comparators also the linear voltage ladder which is used to compare the input voltage with consecutive reference voltages [7]. The reference ladder is generally made from resistors. The number of comparators required for N bit ADC is $(2^N - 1)$. The typical schematic for flash converter is show in figure 11.

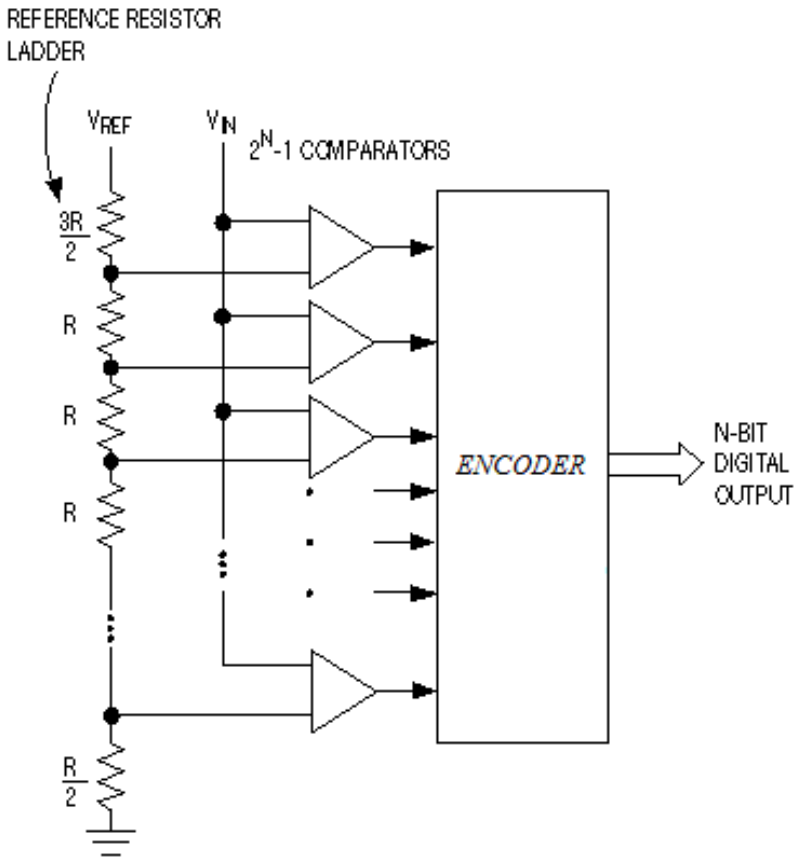



*Figure 11: the generic flash A to D converter.*

For example, a 10-bit flash ADC requires 1023 comparators, occupying a very large chip area and dissipating large amounts of power. Moreover, each

comparator must have an offset voltage smaller than $(\frac{1}{2^{10}}) * V_{FS}$, which is extremely difficult to implement. Typically, flash ADC do not exceed 8 bits of resolution.

## *3.3- Multi-stage analog to digital converter*

To reduce hardware complexity, power dissipation and die area, and to increase the resolution but to maintain high conversion rates, flash converters can be extended to a multi-step analog to digital architecture also called algorithmic (cyclic) converter.

Conceptually, these types of converters, as the name indicates, quantizes the input sample in an algorithmic or repetitive manner. Its principle of operation consist of sampling and quantized of the input, then generating an amplified residue, and then the quantization and residue amplification process is repeated by subsequent stages reutilizing the same physical space or area . Using a $m \times 2^n$ instead of $2^{m \times n}$ comparators for a full flash implementation assuming $n_1$, $n_2$, ..., $n_m$ are all equal to n.

However, the conversion in multi-step ADC does not occur instantaneously like a flash ADC, Here $\boldsymbol{M = N/C}$ bits are produced each time a new cycle is launched, starting from the MSB until the LSB, **N** being the resolution of the converter and **C** the number of cycles needed to produce the whole

conversion. The input has to be held constant until the sub-quantizer finishes its conversion. Therefore, a sample-and-hold circuit is required to improve the performance. The conversion process is splited into two steps as shown in figure 12.

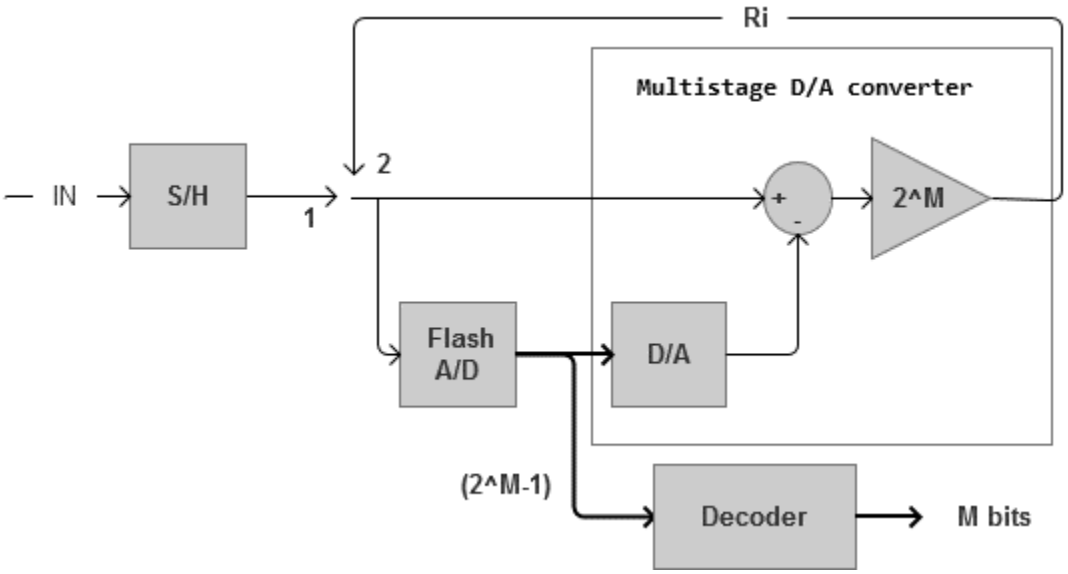



*Figure 12: Architecture of multi-step converters.*

The first ADC flash converter performs a coarse conversion generating $(2^M - 1)$ thermometric code word (D) produced simultaneously as the output of Flash ADC that correspond to the sampled input signal. A parallel DAC converter is used to convert the digital output word $D = [b_1 \cdots b_{2^M-1}]$ of the ADC converter back into the analog domain working as weighted adders, the weights are the unit elements ($u_e$), whose amplitude equal to $V_{LSB}$ is set by the resolution of the converter, as summarized by the following relation:

$$V = \sum_{i=1}^{2^M-1} b_i \, . \, u_e$$

The output of the DAC is then subtracted from the analog input. The resulting signal, called the residue R ($R_1$ is the input signal), is amplified and fed into a second cycle of ADC which takes over the fine conversion to full resolution of the converter. The amplification between the two stages is not strictly necessary but is carried out nevertheless in most of the cases. With the help of this amplifying stage, the second ADC can work with the same signal levels as the first one, and therefore has the same accuracy requirements.

The thermometric-coded inputs delivered by the flash A to D converter is converted to an equivalent M-bit binary-coded word through digital encoder. The resultant N-bit code word is reconstructed concatenating the M-bit code words delivered at each cycle applying a digital correction at the binary digital output yield.

## *3.4- Error Sources in Multi-Step A/D Converter*

Although the considerable amount of digital logic used in Multi-step ADC most of its signal-processing functions still executed in the analog domain.

Therefore, the conversion process is susceptible to analog circuit and device impairments. Besides **timing errors**, the primary error sources present in a multi-step A/D converter [1, 2]:

- **Transition position errors**, which originated at the A to D conversion.
- **Transition magnitude errors**, from the D to A parallel converter offset.
- The **gain error** group includes all the errors in the amplifying circuit, including technology variations and finite gain
- **Offset** of the operational amplifier.

The error in transition and magnitude positions is supposed to be a standard deviation ($\sigma$) of normal distribution with zero mean value ($\mu$). Figure 13 represent the transition positions for analog to digital converter, where the real transition positions in red differ the ideal value in blue, overlapping between

adjacent thresholds is avoided , and hence missing codes, one must assure that: $V_{lsb} \geq 6 * \sigma$ .

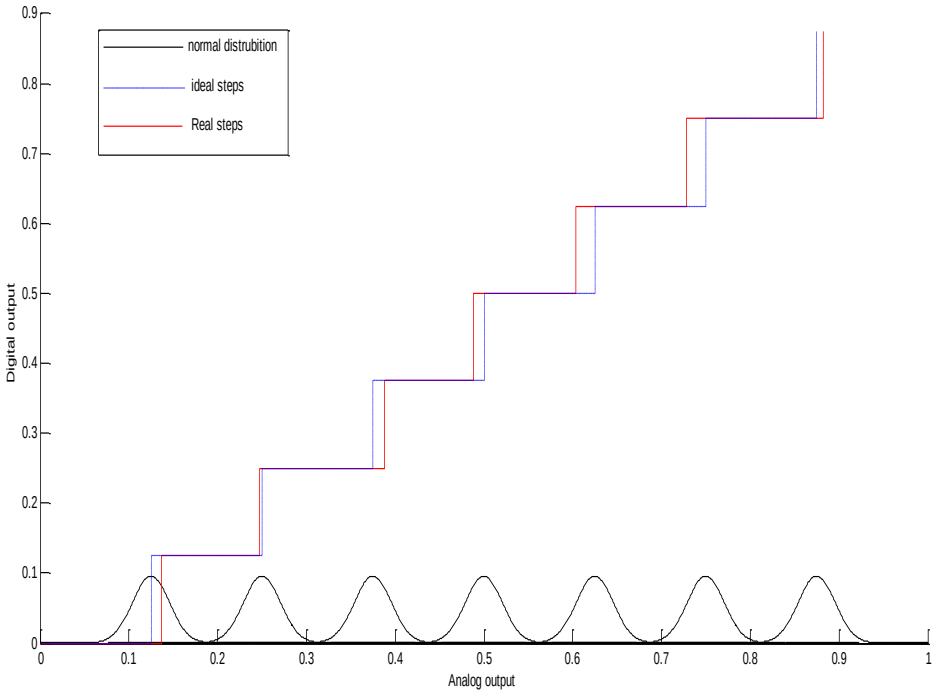



*Figure 13: transition positions for ADC*

## *3.5- Redundancy and Digital Correction*

To achieving a great tolerance to component non-idealities caused over range error in multi-step ADCs, redundancy is introduced by the act of performing the input stages of ADC by an extra quantization levels [8], making the sum of the individual stage resolutions greater than the total resolution.

Digital-correction algorithms are applied at the digital output to eliminate the redundancy correcting the digital yield and maintaining the same overall ADC resolution [9]. Applying digital correction are based on either increasing the input range of the next stage and using extra comparators or using the partial codes in the next stages to correct the code of the present stage.

With digital correction, the effects of offset, gain and coarse A/D converter nonlinearity are reduced or eliminated; therefore, the D/A converter nonlinearity and residue amplifier gain and offset errors limit the performance of multi-step converters.

Different redundancy are proposed in literature [1], in this thesis we will discuss and compere the CRZ and RSD.

### 3.5.1- The CR converters with Z additional levels (CRZ)

The Conventional Restoring converters with Z additional levels (CRZ) consisting of converter obtained from the conventional CR adding Z additional levels, in order to reduce the sensitivity against transition position errors by automatic correction that occurs while cycling. The concept of this

converter explained by Robertson plot, a graphical tool that illustrates the way residue calculation perform used to interprets the cyclic algorithm [2]. The algorithm to calculate Ri's remainders or residues:

$$R_{i+1} = 2^i.\{R_1 - \sum_{j=1}^{i} \left(b_j.2^{-j}\right).V_{ref}\} \quad (3.1)$$

With $b_j$ = - 1 or 1, and $R_1$= $V_{in}$

$$\lim_{i\to\infty} \sum_{j=1}^{i}(b_j.2^{-i}) = \frac{V_{in}}{V_{ref}}.$$

$$R_1 = 2^2 * (V_{in} - 3 * \frac{1}{2^2})$$

An example of ideal 3-steps is presented in figure 14, 6 bits converter to convert Vin= +0.57. The first step, the input signal is reported along the Y-direction until it reaches the line D = (1 1 1); the point of intersection implements the first remainder $R_1$ giving the input for the second step which must be now reported along the X-direction until it reaches the line D = (-1 -1 -1). The procedure repeated in this way until the least significant bits are produce.

In real, errors will be affect the conversion in each cycle and the correctness of the conversion process, because residues will be not necessary stay inside the region bounded by the dashed square. Figure 15 showing for $V_{in}$ but 5%. Due to this error, the signature departs progressively from the ideal as the

cycle count increases: error on transition position the trajectory leaves the conversion region and the converter saturates after R1.

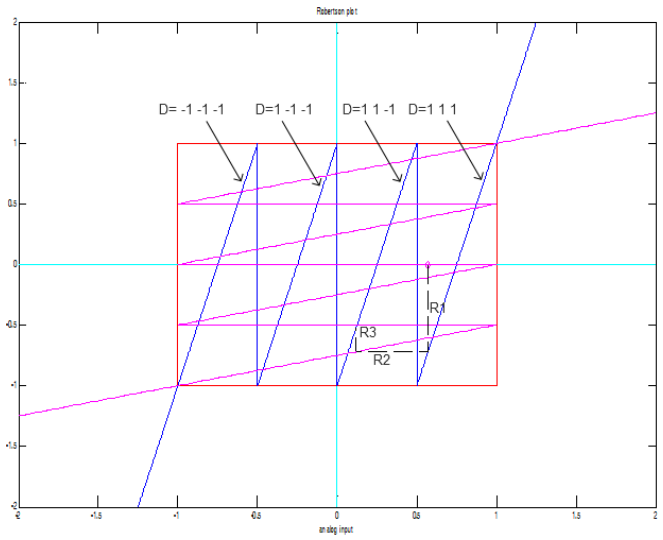



*Figure 14: Robertson plots of a 6-bit, 3-cycles conventional CR converter ideal case.*

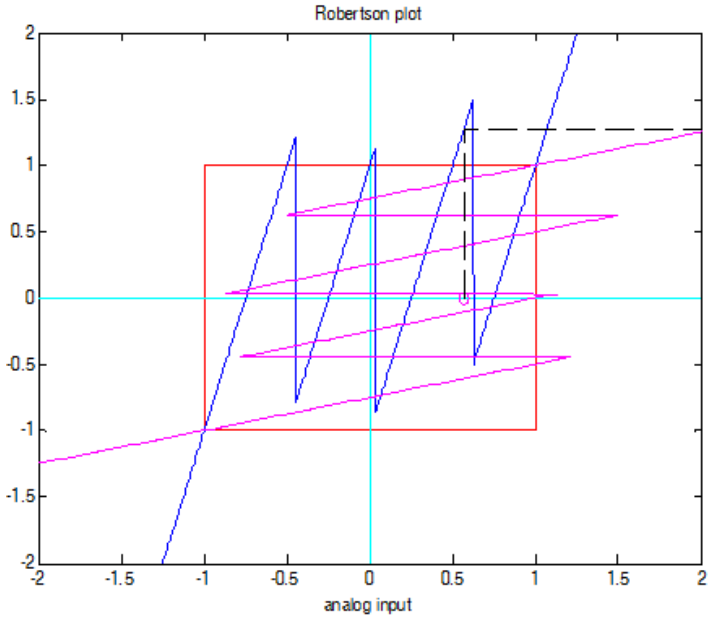



*Figure 15: Robertson plots of a 6-bit, 3-cycles conventional CR converter real case.*

To reduce of the sensitivity of the converter some additional levels are introduce and that allowed defining a larger convergence region in order to improve the redundancy of converter. In figure 16 and figure 17 a two additional level are introduce to the previous case called Z levels. Owing to the dynamic range of residues, which is bound in practice by the power supply, it is necessary to consider a scale factor K (eq. 3.2) that multiplies both the reference scale of the flash converter and the unit elements of the D to A parallel converter as showed in figure 18:

$$K = \frac{2^M - 1}{2^{M-1+Z}} \qquad (3.2)$$

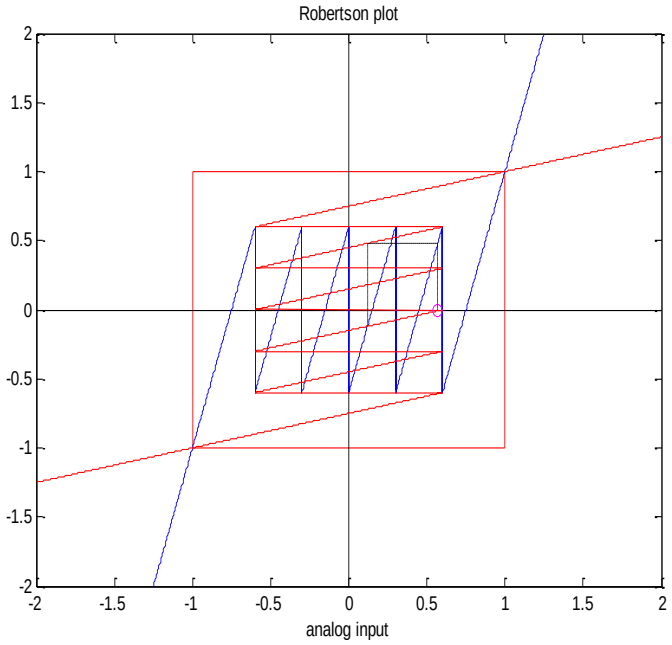



*Figure 16: Robertson plots of 6-bit, 3-cycles conventional CR with two additional level (Z=2) converter ideal case.*

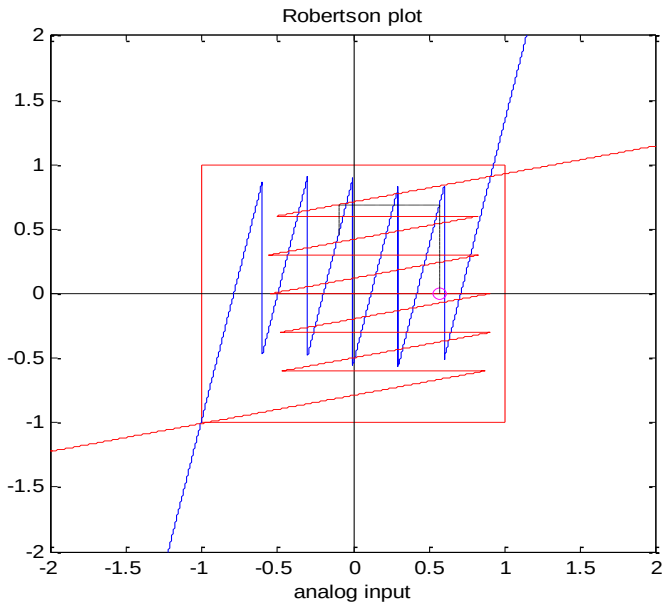



*Figure 17: Robertson plots of 6-bit, 3-cycles conventional CR with two additional level (Z=2) converter real case.*

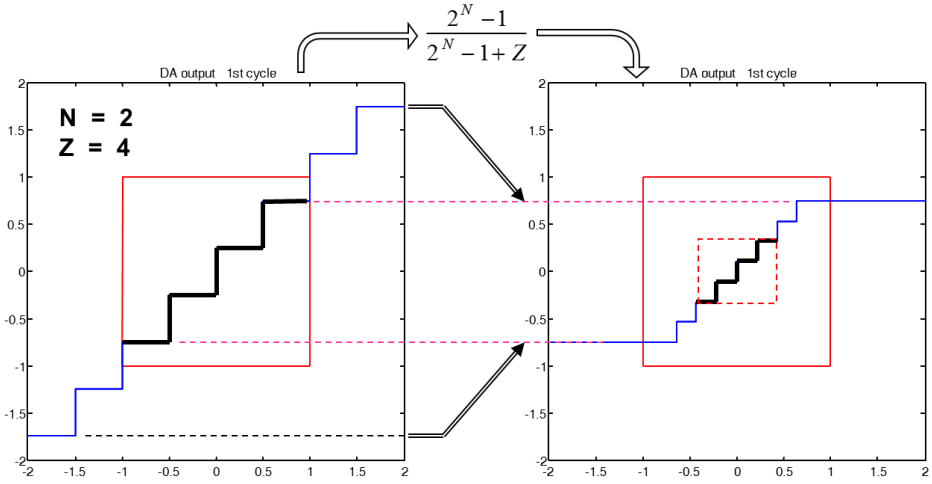



*Figure 18: In order to keep the dynamic range within the power supply scale compression is required.*

It is important to notice that CRZ converters with an odd or an even number of additional levels show different response to transition magnitude errors.

### 3.5.2- RSD algorithm

The RSD (Redundant Signed Digit) used with new architecture by [2] as showed in figure 19, to overcome the offset errors in the conventional Cyclic ADC, and to facilitate high-resolution conversion without having to use accurate voltage comparators.

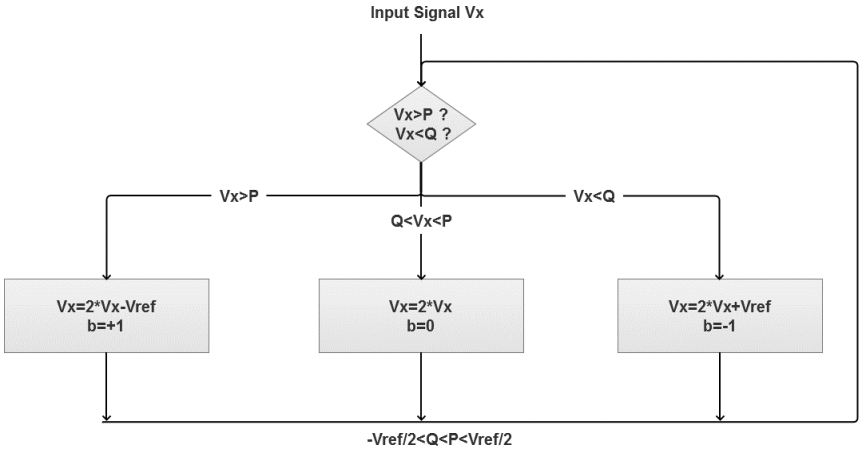



*Figure 19: RSD cyclic conversion algorithm.*

The analog input is compared simultaneously with two thresholds (P and Q) as showed in figure 20 , and a single RSD digit is produced [9]-[15], the selection signal is now also allowed to be equal to 0, and the decision rule changes following the Robertson diagram represent in figure 4.

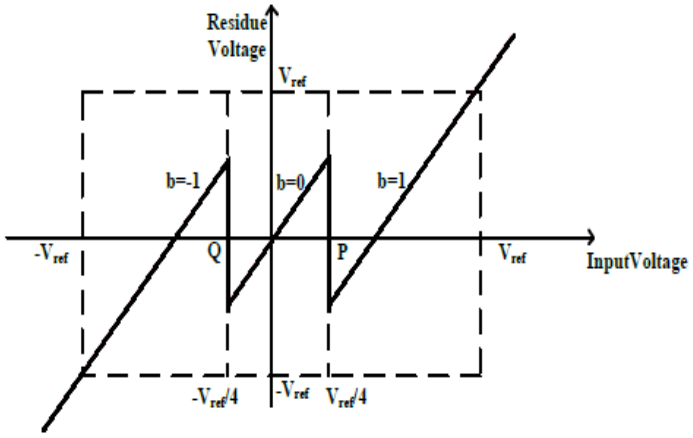



*Figure 20: Residue Plot of a 1.5-bit/stage Architecture.*

## *3.7- Relation between RSD and CRZ*

While the number of comparators needed, in case of CRZ, to detect the position of the input signal are $(2^M - 1 + Z)$ comparators respect to the thresholds defined by resistors of the $(2^M - 1)$ reference divider. The RSD mythology produce a double threshold concept underlying the redundant single-bit converter as explain before, that mean a $2 * (2^M - 1)$ comparators are needed to detect the position of the analog input with respect to the thresholds defined by $(2^M - 1)$ resistors of the reference divider. For Z = $2^M$ -1 the CRZ and RSD flash reference are identical meaning that the impact of transition position errors is the same for both converters, because

the transition positions and the number of comparators and resistors of the reference divider are the same. However, because of the different coding algorithms, the D to A parallel converters differ. In particular, since the input signal is compared simultaneously with two thresholds to produce a single RSD digit, the output thermometric code from the RSD converter requires half the digits of the equivalent CRZ converter. As a result, the number and the magnitude of unit elements required by the D to A parallel converter is different. Table 1 compares the characteristics of the two converters in terms of the number of components [with K defined by (3.2)].

*Table 3: comparison between CRZ and RSD*

| | Comparators | Resistors | ue (h) | ue size |
|---|---|---|---|---|
| CRZ | $(2^M - 1 + Z)$ | $(2^M + Z)$ | $(2^M - 1 + Z)$ | $\frac{1}{2^M} \times K$ |
| RSD | $2 * (2^M - 1)$ | $(2^{M+1} - 1)$ | $(2^M - 1)$ | $\frac{1}{2^M}$ |

# Chapter 4: Behavioral Model

## *4.1- Introduction*

Due to the increasing complexity of circuits and systems the using a behavioural models suitable for both CRZ and RSD converters, helps in achieving the target, and it is useful to understand how a real converter behaves when non-idealities such transition position and transition magnitude errors appears without considering circuit design aspects. Behavioural simulators work much faster than the transistor level counter parts thus permitting to explore all the regions of operation. The proposal Behavioural Simulator of multi-stage analog to digital converter consists of three main parts: input data consist of input signal, the parameters, and voltage references and OpAmp gain, the simulation blocks that contain analog to digital flash converter and parallel digital to analog converter, finally the output consist of database SNR as showed in figure 20. Where each block is modulated by a corresponding matlab function. The bold lines indicated a digital output.

For two cycles analog to digital converter, the input signal $V_{in}$, read from a data base containing the sampled pure sine wave, is applied to the flash converter (1). The flash references are introduced the impairments on transition positions of A/D by means of the parameter $\sigma_{comp}$ included in flash

reference, which portrays the standard deviation of a standard distribution with zero mean value. The thermometric code delivered by the flash converter is temporarily stored in a register (coarse conversion) before being sent to a parallel D/A converter.

The impairments on the D/A conversion are introduced through unit element by the parameter $\sigma_{ue}$: unit elements differ from the ideal value by an error which is described also by means of a standard distribution with zero mean value and standard deviation $\sigma_{ue}$. The residue, computed as the difference between the input signal $V_{in}$ and the analog counterpart of the coarse conversion, is amplified before being recycled for the fine conversion (2). Finally, the gain error of the amplifier is set by the parameter relGain.

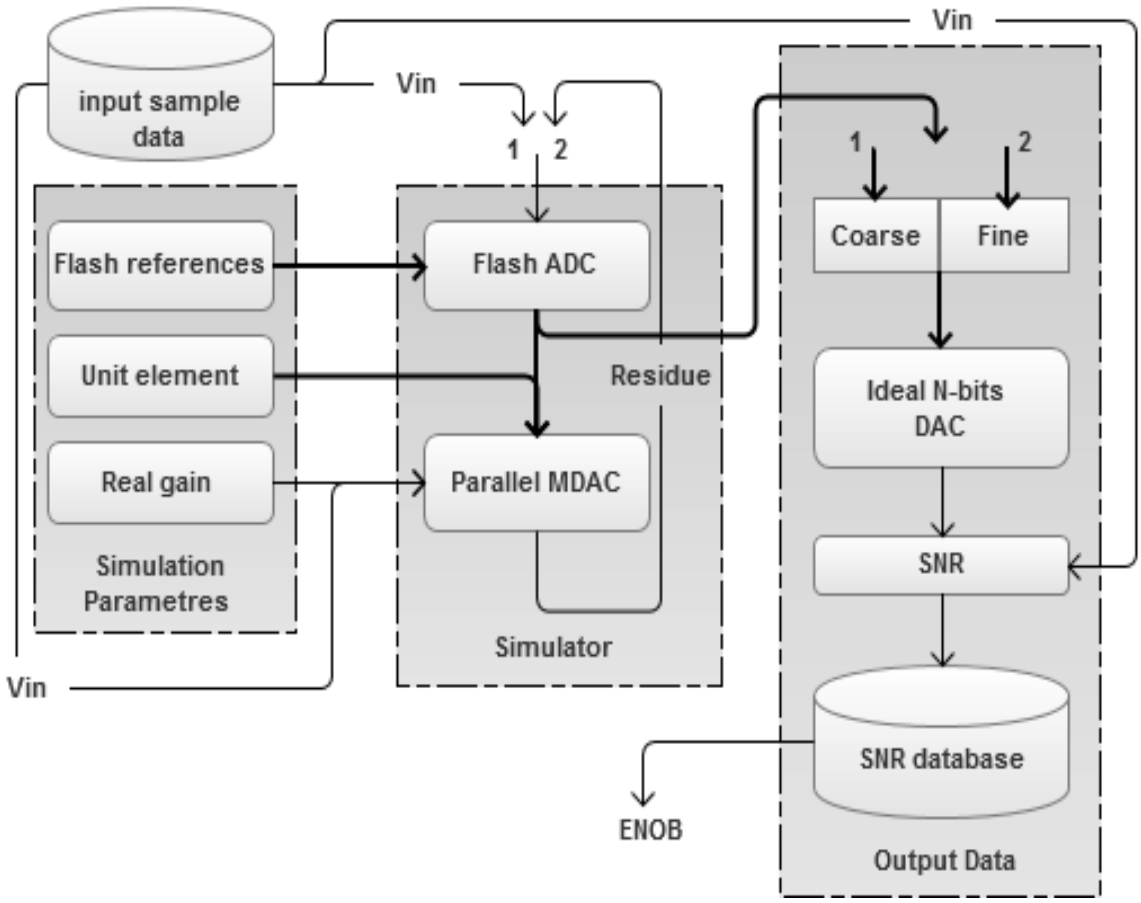



*Figure 21: Behavioural model of multi-step analog to digital converter.*

## *4.2- Effect of Different Sources of Errors*

### 4.2.1- Effect of transition Position Errors

The results of the analysis concerning the impact of transition position errors on CRZ converters are presented in the figure 22. While the ENOB remains above 10-bit whichever Z and $\sigma_{comp}$, the $N_{fs}$ drops dramatically when few additional levels are considered. The dashed black lines on both curves portray the locus of larger $\sigma_{comp}$ lead to references overlapping, and errors cannot be corrected anymore.

The spectral signatures for several CRZ converters with respect to different values of $\boldsymbol{\sigma_{comp}}$, $\boldsymbol{\sigma_{comp}}$=0.003 and $\boldsymbol{\sigma_{comp}}$=0.01 in figure 23. The impact of transition position errors drops at the output response with larger Z as derived from the analysis of the SNR loci, thanks to the automatic correction occurring in the fine conversion. Notice that transition position errors do not introduce any spurious frequency in the output spectra.

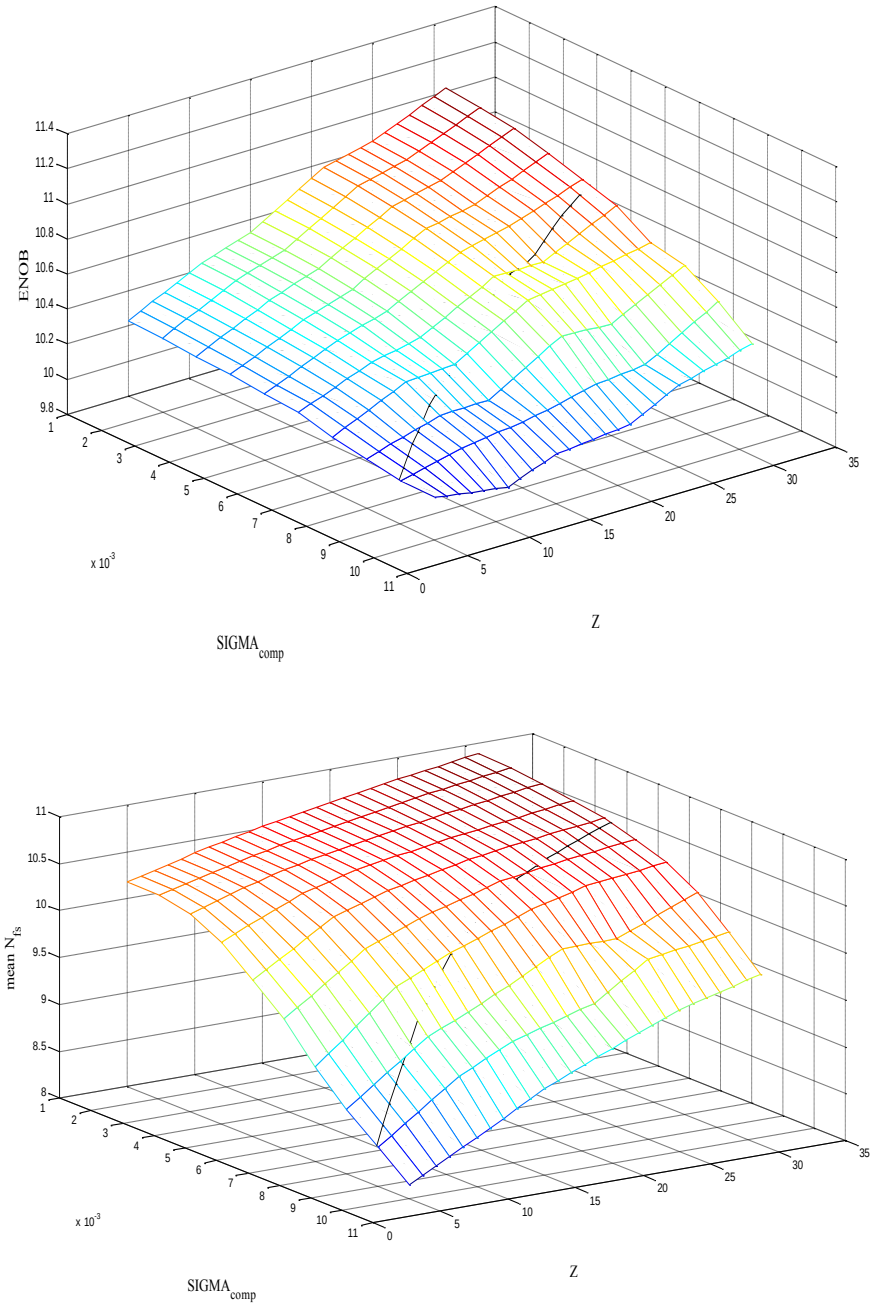



*Figure 22: Impact of transition position errors on CRZ converters.*

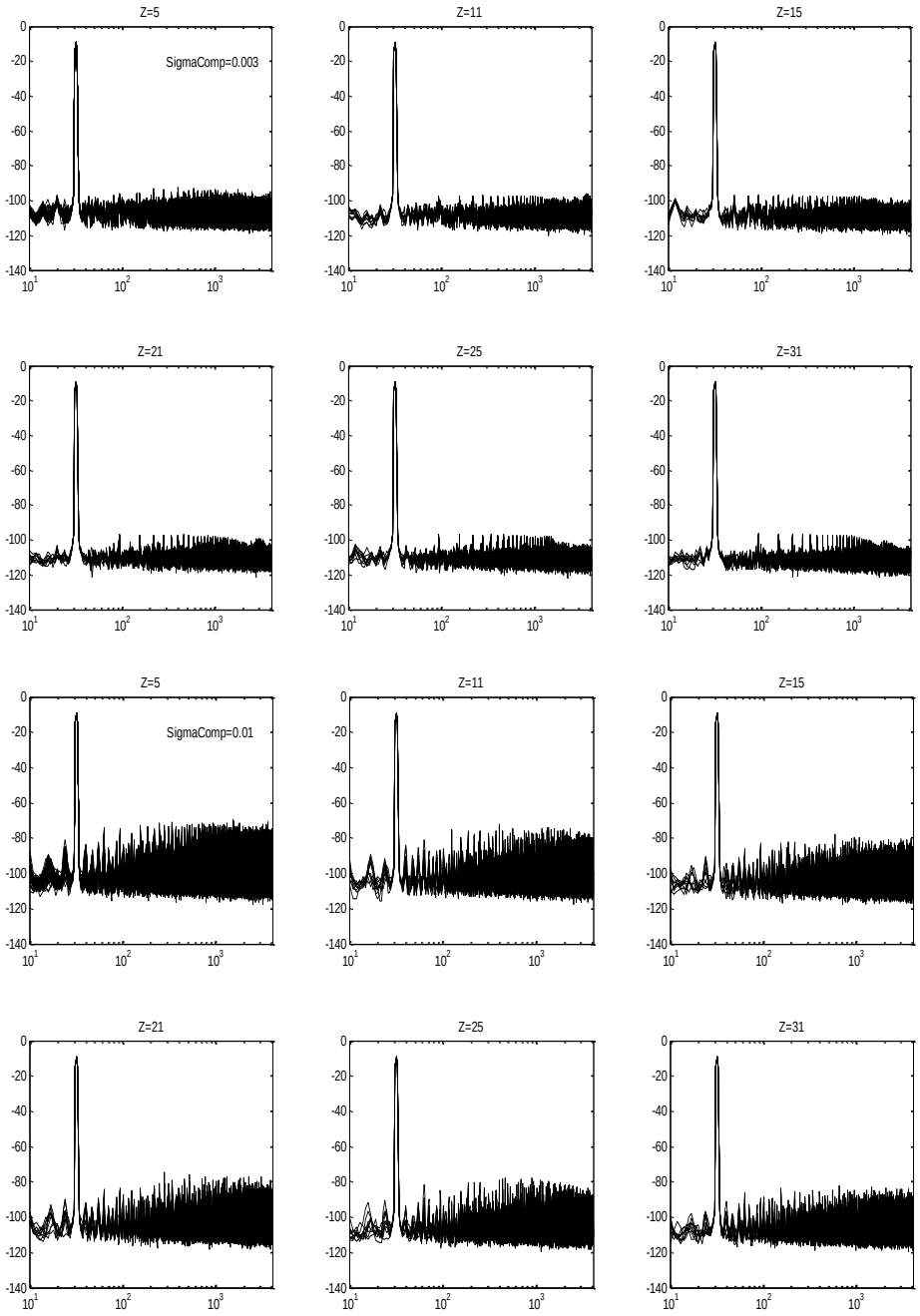



*Figure 23: Spectral signatures of several CRZ converters in presence of transition position errors σ_comp=0.003 and σ_comp=0.01 respectively.*

### 4.2.2- Effect of transition magnitude errors

The CRZ converters are less sensitive with odd Zs magnitude errors when small input signals are considered; as result, the ENOB is not affected by transition magnitude errors. Again, as figure 24 the ENOB grows with the number of additional levels, and for $Z = 2^M - 1$ the accuracy of the converter is one-bit larger. The impact of transition position errors becomes visible for larger input-signals, as shown by the $N_{fs}$, which drops for larger $\sigma_{ue}$. As for transition position errors, again, the dashed lines portray the locus of $\sigma_{\mathrm{ue}}$, where larger $\sigma_{\mathrm{ue}}$ lead to non-monotonicity errors.

The FFT test shows that transition magnitude errors add some spurious frequencies, which are well above the noise floor in the spectra of the considered CRZ converters. In figure 25 are reported two cases with $\sigma_{\mathrm{ue}}$ = 0.003 and $\sigma_{\mathrm{ue}}$ = 0.01. Notice that transition position errors do not introduce any spurious frequency in the output spectra

### 4.2.3- Effect of the Gain Error

The effect of gain error will affect the response of multi-step analog to digital converter if few bits are produced each cycle, as showed the simulation in figure 26 with same additional level Z but with at two different levels of real

gain = 1.01 and 1.1 the $N_{fs}$ is case of 1.01 is highest by 1.7 bits approximately than 1.1.

In addition, the number of cycle increase the accuracy of the gain factor that it is affected the fine part of conversation.

The FFT test shows that gain errors does not affect at the spectra at the output of the converter, figure 27.

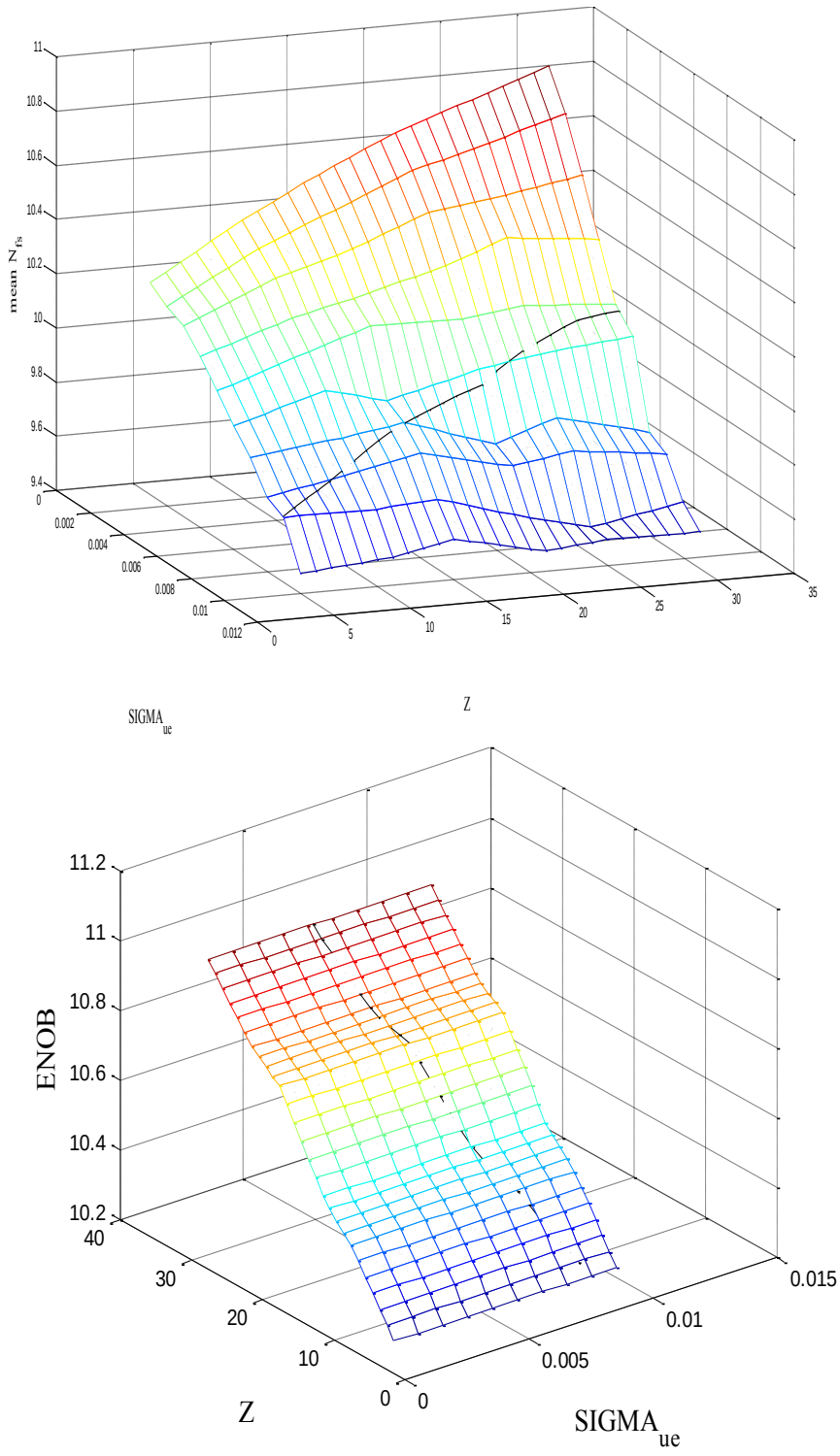



*Figure 24: Impact of transition magnitude errors on CRZ converters.*

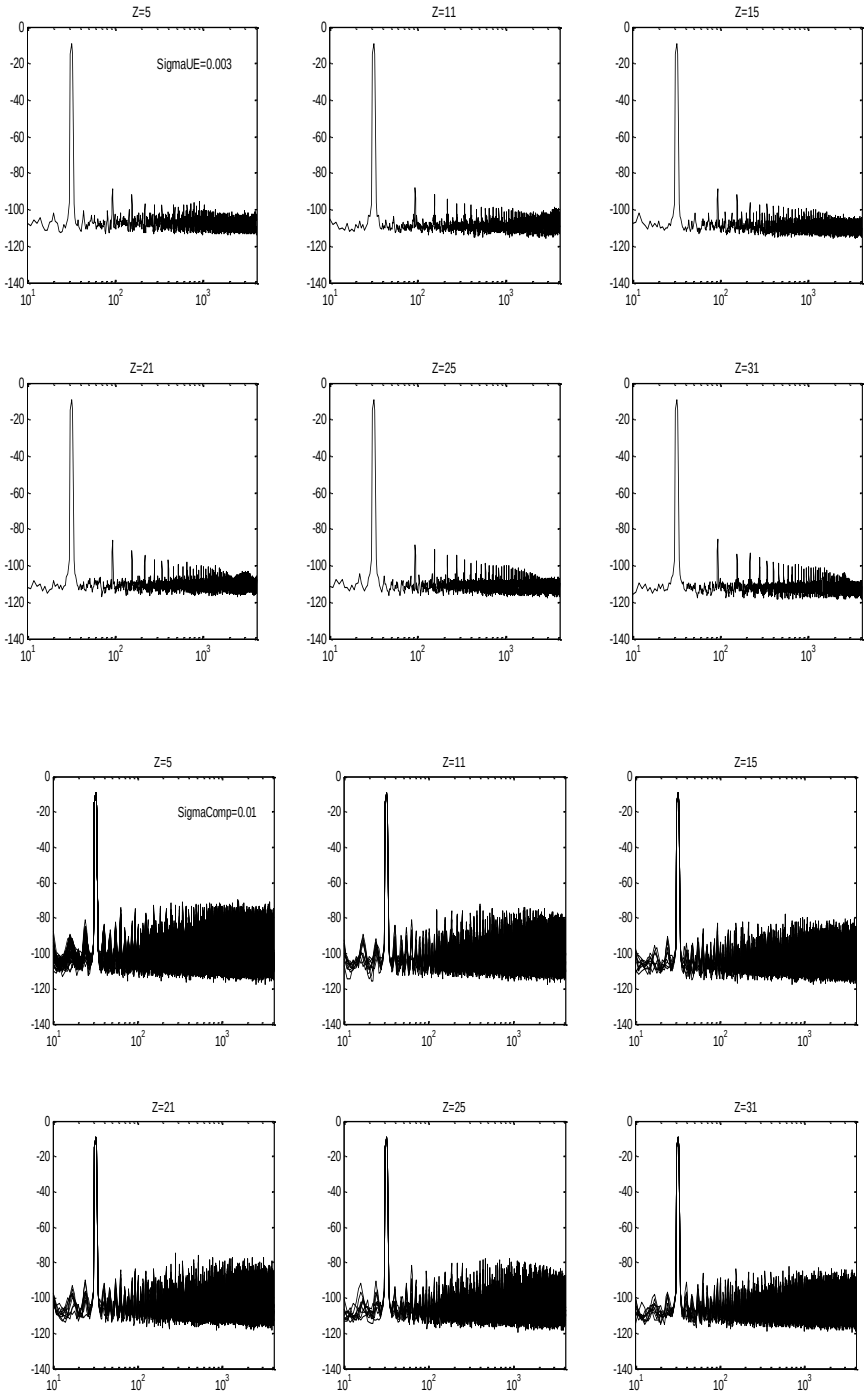
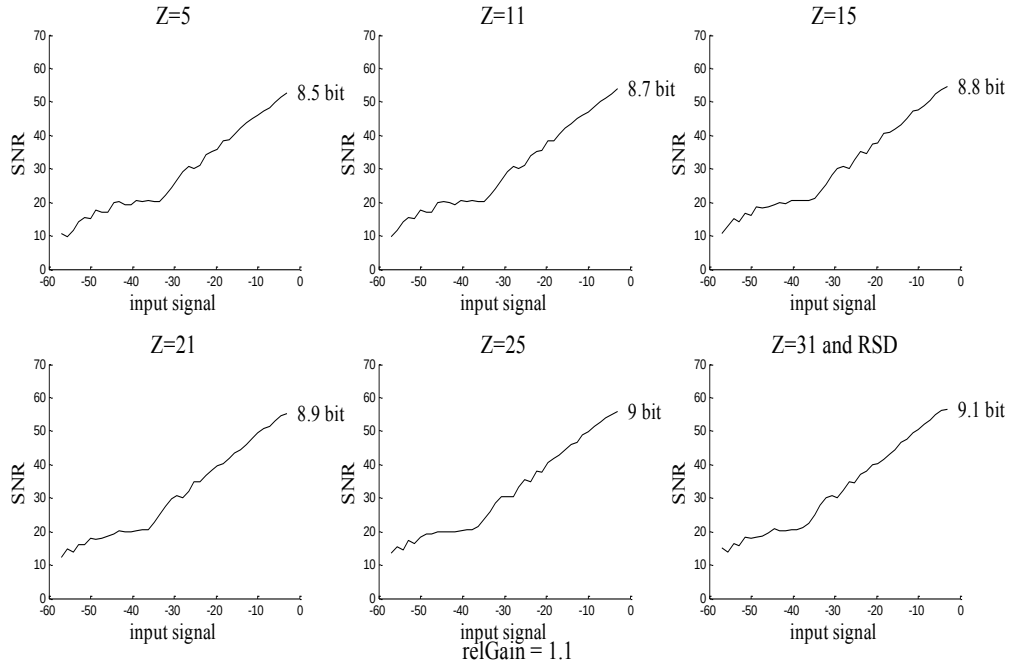



*Figure 25: Impact of transition magnitude errors on CRZ converters for σ_ue = 0.003 and σ_ue = 0.01 respectively.*



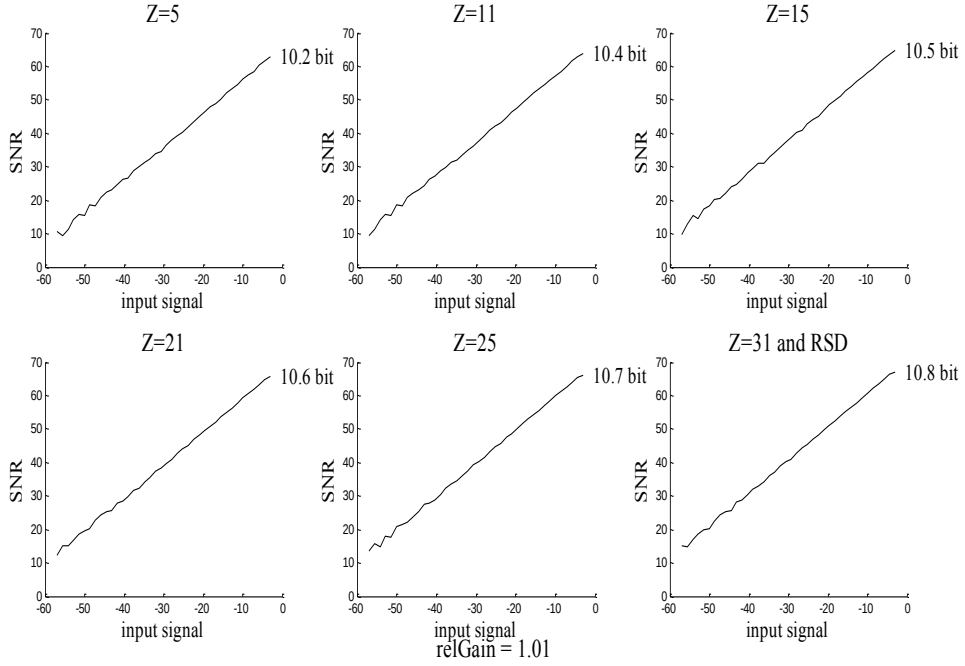




*Figure 26: Impact of real gain errors on CRZ converters relgain = 1.01 and relgain = 1.1.*

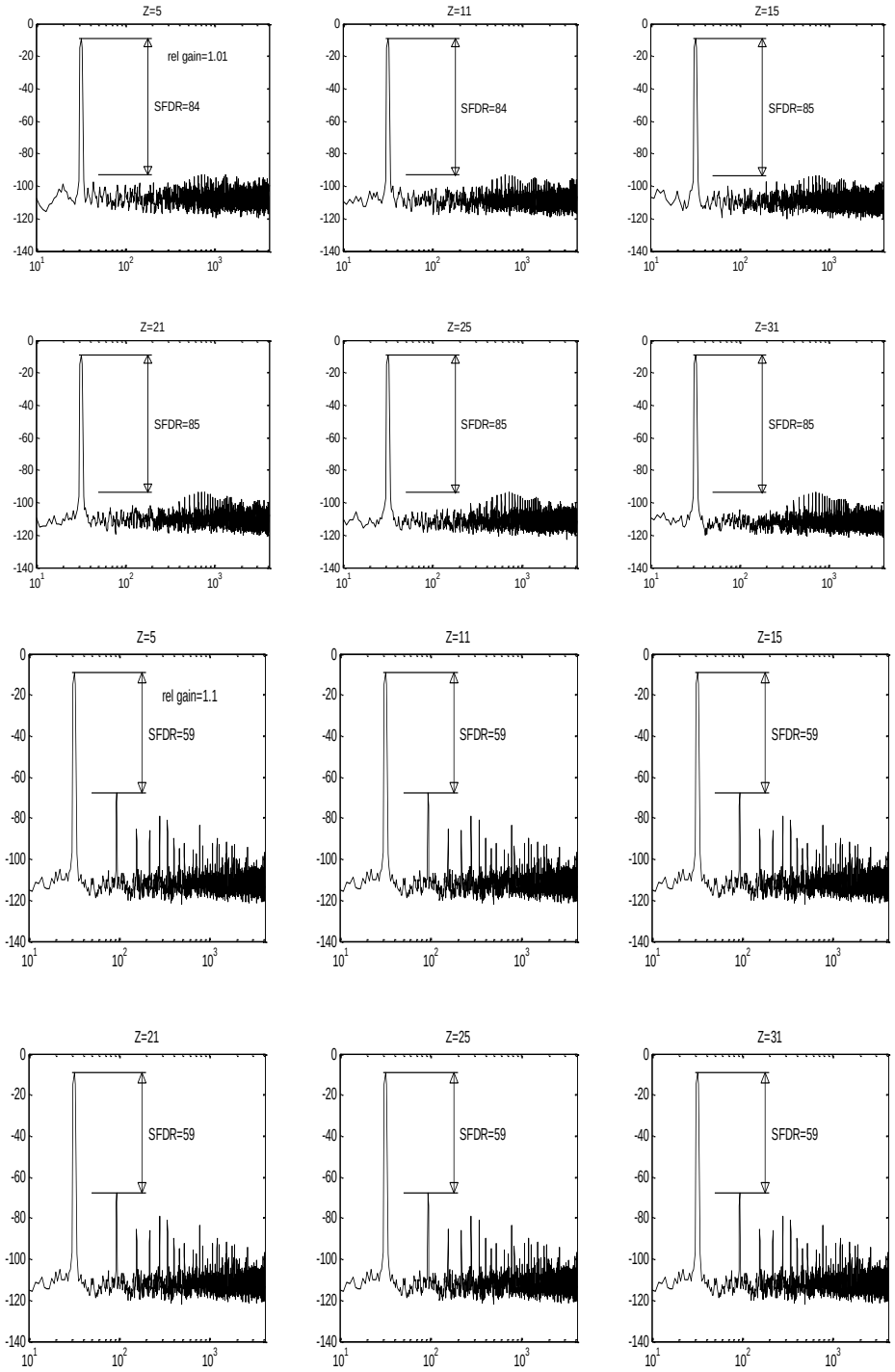



*Figure 27: Impact of the interstage gain error on several CRZ converters.*

## *4.3- Comparison between RSD and CRZ$_{Z=31}$ converters*

As result, the RSD present the same performance as CRZ especially at the levels of A/D where ENOB and Nfs are equals in the two converter as presented in figure 28, which have been inspect from previous. However, a different situation in D/A converter where the ENOB still the same the Nfs of RSD drop more than CRZ 31 with the increasing of sigma ue ($\sigma_{ue}$) as presented in figure 29. Since the D to A act as weight adder, the error will be more clear if the number of weight are smallest because in this case RSD used less weight adder to do the same conversion with compere to CRZ.

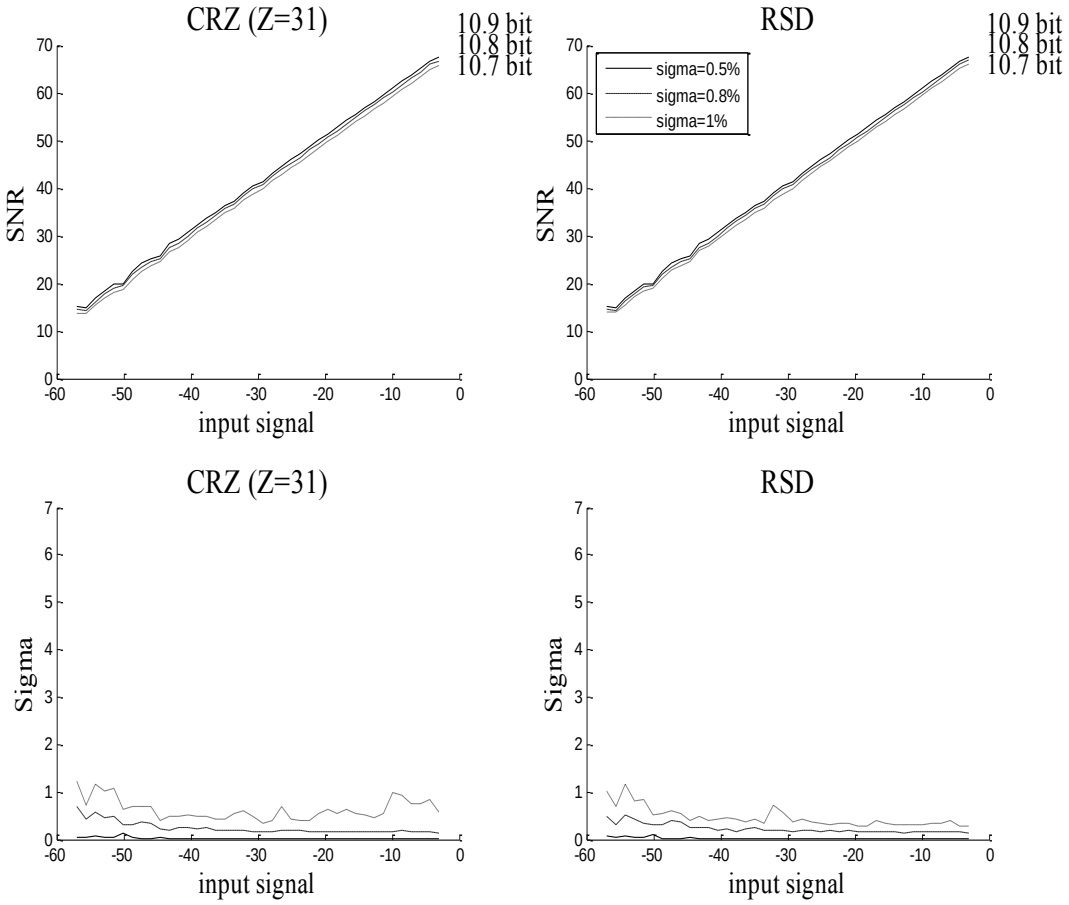



*Figure 28: ENOB and Nfs with standard versus transition position errors.*

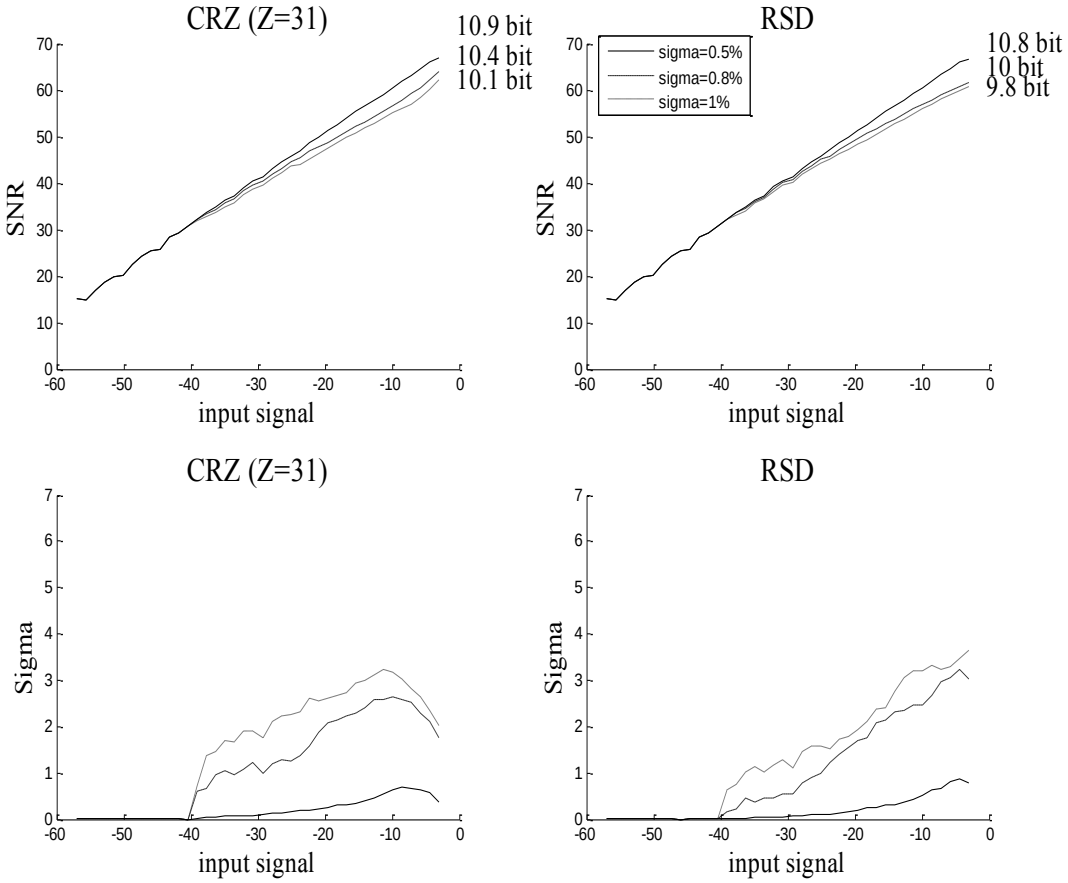



*Figure 29: ENOB and Nfs in presence of transition magnitude Errors.*

# Chapter 5: Circuital Model and Design for Adjustable Configuration combing CRZ converter

## *5.1- Introduction: Circuit design for CRZ-converter*

The Circuit design of multi-stages A/D conventional restoring converter with Z additional levels CRZ is applied by configured the circuit in order to simulate with the same chip different additional levels of Z taking in account the variation of the levels in the second one.

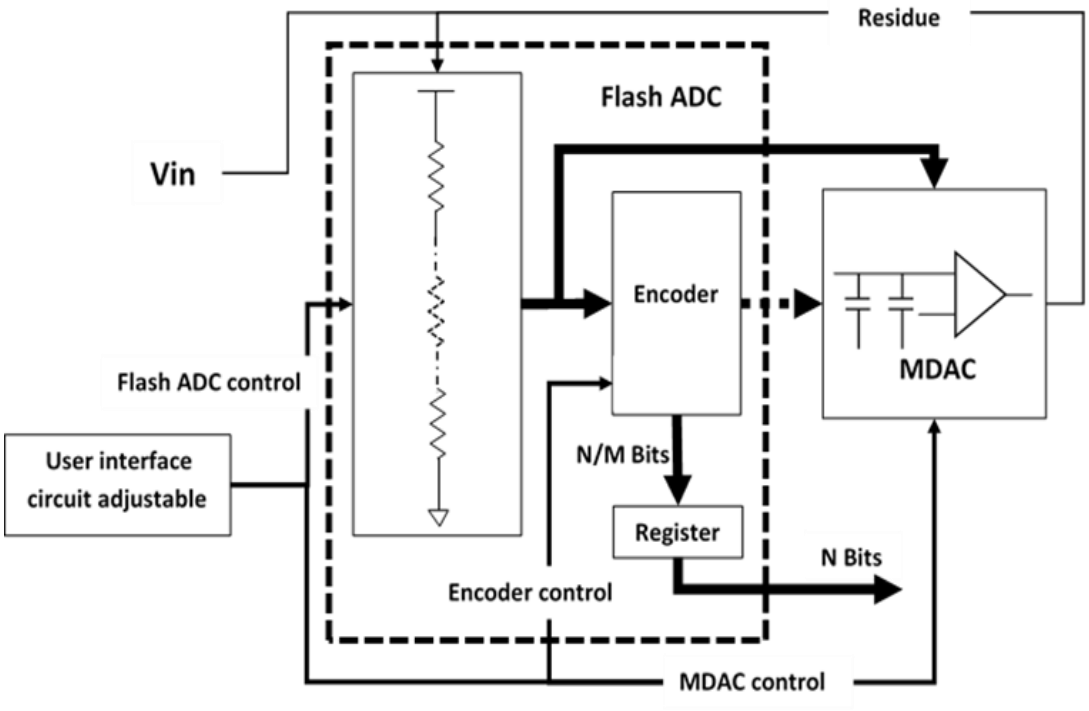



*Figure 30: Circuital model.*

The new configuration as showed figure 30, user has the free choice between the two methodologies and controlling the numbers of Z depending on power limitations and the accuracy of the analog to digital converter.

The behavioural model previous introduced will slightly change, in order to sizing the passive components with real parameters and the non-idealities related to devices mismatch , according to matching impairments, and named here after **Circuital model** in figure 31. The standard deviation $\sigma(\Delta P) = \frac{A_P}{\sqrt{W.L}}$ ,which describes a specific class of errors (transition position, transition magnitude or gain error), where, $\sigma(\Delta P)$ represents the standard deviation of the electrical parameter P, $A_P$ is the process-dependent matching parameter describing the area dependence, and W and L are the width and the length of the device.

We derive from it the size of the passive component needed to comply the required accuracy for 10 bits two cycles analog to digital converter, by using the technological parameter from the AMS technology for the 0.35 CMOS process.

The results obtained from different converters are compared, as done for the behavioral model, in the [σ, Z] plane using as figures of merit both the ENOB

and the Nfs. The area needed by passive components to meet the required accuracy is also used to evaluate the impact in terms of area of mismatch issues on the considered converters.

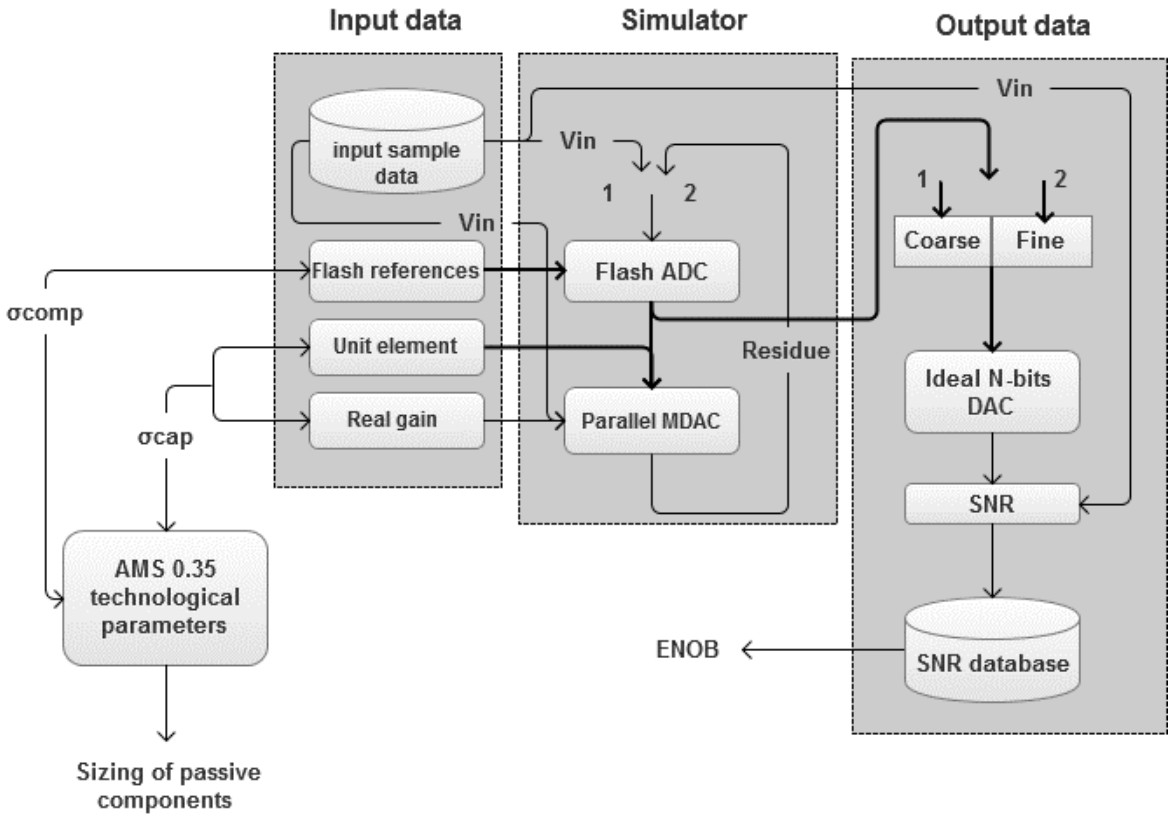



*Figure 31: Circuital model of multi-step analog to digital converter.*

## *5.2- Circuit design for CRZ converter*

### 5.2.1- A to D flash converter (flash references)

An adjustable configuration of flash A/D converter figure 32 is proposed to manipulate the adjustable circuit configuration, where in the conventional

flash converter consist of $2^N$ resistances to generated N bits, Z-resistances is added to resistances chain of CRZ to generate ($2^N - 1 + Z$ ) references levels.

The magnitude of peripheral resistors in the resistors chain is modified by X factor as will be represent in (5.3) depending on the number of additional levels Z, in order to control the $V_{LSB}$ in the new configured circuit equation (5.1). Figure 33 show the variation of X and $V_{LSB}$ in function of Z.

Where the $\boldsymbol{V_{LSB}} = \frac{\boldsymbol{V_{ref}}}{\boldsymbol{2^M}}$ in the conventional circuit of flash converter, the $\boldsymbol{V_{LSB}}$ in the proposed circuit is equal to

$$\boldsymbol{V'_{LSB}} = \frac{V_{ref}}{2^M - 2 + 2X + Z} = \frac{\boldsymbol{V_{ref}}}{\boldsymbol{2^M}} * \boldsymbol{K} \quad (5.1)$$

K is scaling factor defined to bounding the dynamic range of residues by power supply

$$\boldsymbol{K} = \frac{2^M - 1}{2^M - 1 + Z} \quad (5.2)$$

As result

$$\boldsymbol{X} = \boldsymbol{1} + \frac{\boldsymbol{Z}}{\boldsymbol{2(2^M - 1)}} \quad (5.3)$$

The resistors must have the same magnitude in the circuit design that propose to switches control a parallel chain of resistors to achieve the theoretical value of peripheral resistors with an error in the real equivalent one less than sigma R mismatch parameter given by AMS technology, also the chain series resistors adapted with a different values of Z. The number of serial resistors

also controlled with a second series of switches, the two series are modified automatically with the user choice.

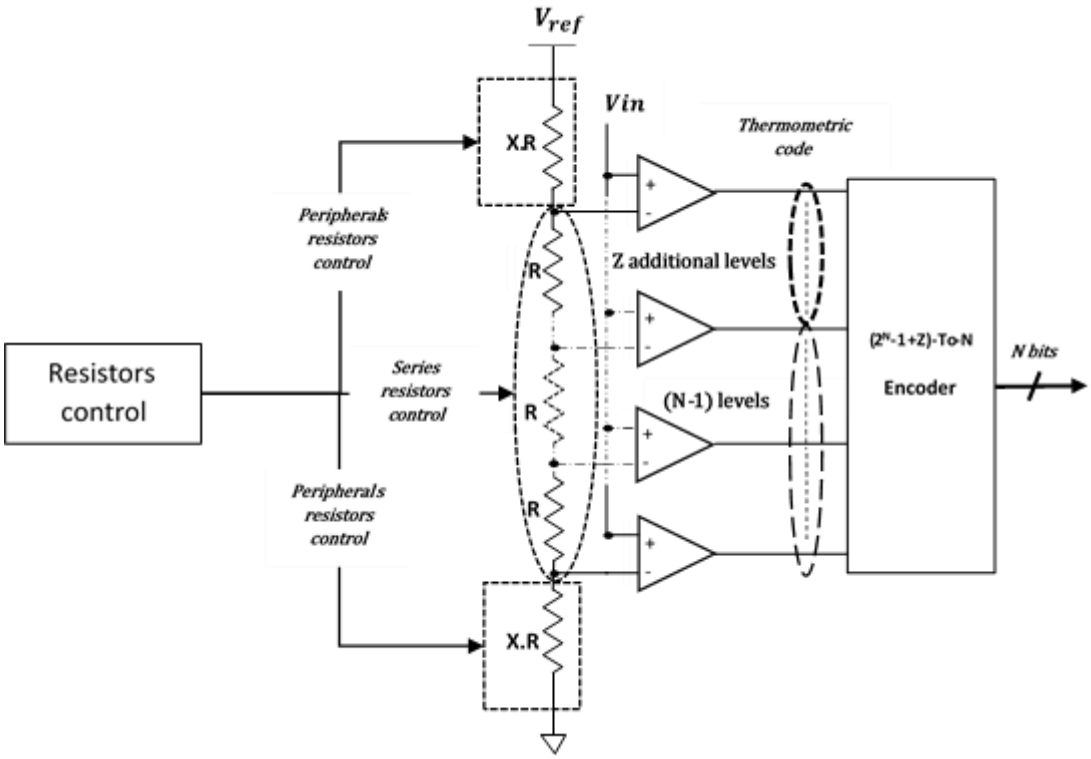



*Figure 32: Adjustable configuration of flash A/D converter.*

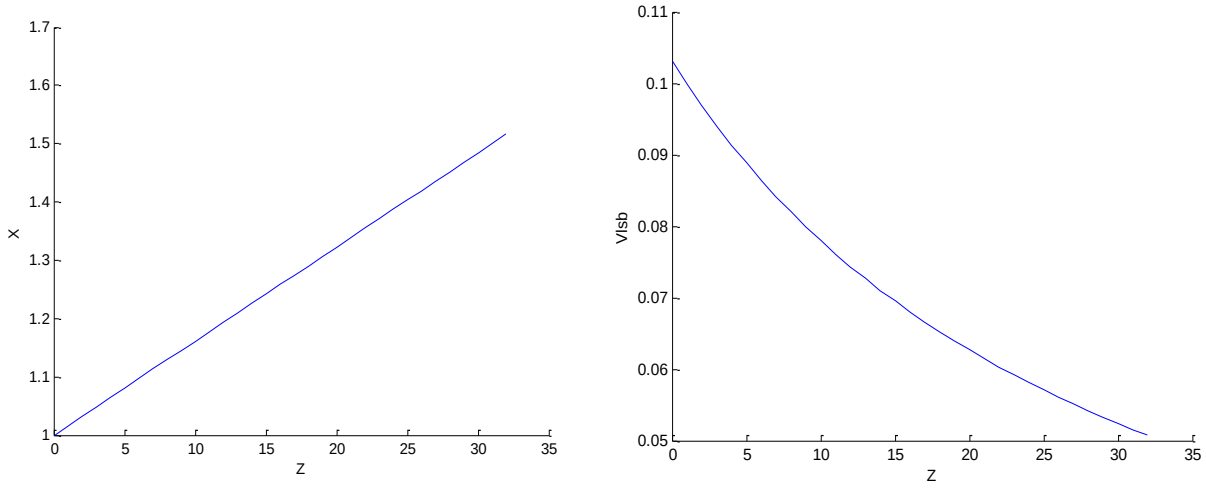



*Figure 33: Variation of X and Vlsb in function of the additional levels Z.*

Typically, comparators are implemented by means of the Track & Latch stage, whose off-set is fixed by the ratio W/L of the input differential pair of the preamplifier stage: the larger the aspect ratio the smaller the off-set. The use of flash converters is limited by the large input capacitance due to the high number of comparators put in parallel in order to simultaneously compare the input voltage with the references. If a large accuracy is required this input capacitance becomes very large, with a strong impact on the power consumption of the amplifier stage used to achieve the $2^M$ gain factor. To avoid the use of large devices, and hence all the related issues, AC coupling was preferred to DC coupling.

In figure 34 is reported the scheme of an AC coupled comparator [18]. Two phases are needed to perform comparisons: during the first phase (F1 high) the off-set of the input differential pair is sampled and held to be canceled during the comparison that take place in the second phase (F2 high). The insensitivity against the off-set of the preamplifier stage allows to use smaller devices without affecting the output response of the converter, with a significant saving of area (and power of the amplifier stage).

In order to investigate the impact of non-idealities, we defined a model where the mismatch of capacitors C as well as the impairments of the switches are

taken into account. During the first phase, (F1) the charges stored in the node X:

$$Q_X^{(1)} = (V_{out} - S_i).C + V_{out}.C_p + \varepsilon \quad (5.4)$$

$C_p$ being the parasitic capacitances seen at the input nodes of the OpAmp. Because of the non-idealities of the switches, phase 1 results in an error $\varepsilon = \varepsilon^{ck} + \varepsilon^{ci}$ which is given by the contribution of the clock feed-through and of the charge injection.

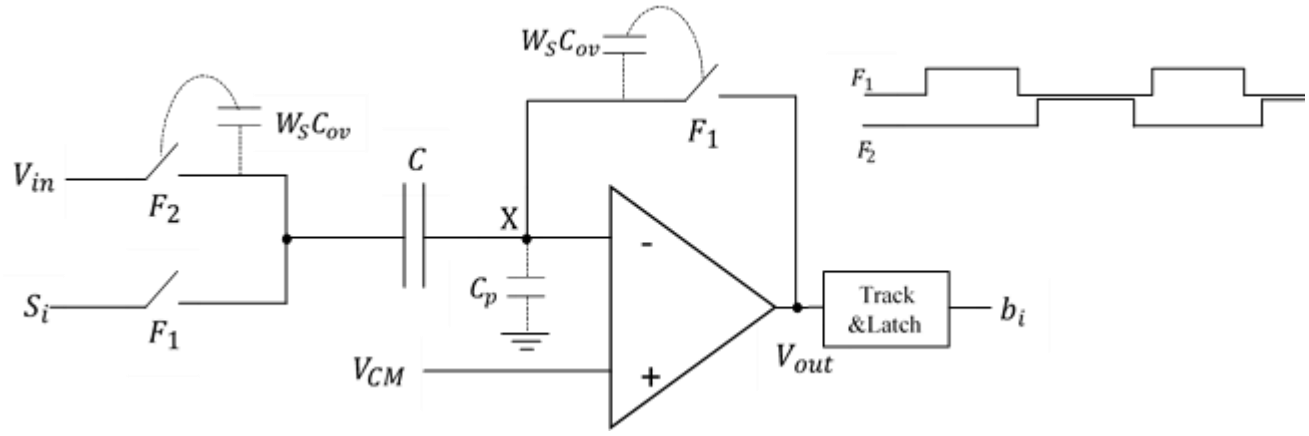



*Figure 34: A single ended comparator with offset cancellation with Track &latch circuit.*

$C_{ov}$ represents the gate-source/gate-drain overlap capacitance per channel width (Ws) and $\beta = \mu C_{ox}$.

During the second phase, the charge in the node X is:

$$Q_X^{(2)} = (V_x - V_{in}).\mathrm{C} + V_x.C_p \quad (5.5)$$

Since charges cannot change between phase F1 and F2, one has

$$Q_X^{(1)} = Q_X^{(2)} \tag{5.3}$$

From the previous two equations, we can derive the voltages at the input nodes of the OpAmp at the end of the second phase:

$$V_X = (V_{in} - S_i).\frac{C}{C+C_p} - \frac{V_{os}}{2} + \varepsilon.\frac{1}{C+C_p} \tag{5.6}$$

Notice that the use of minimum size transistors for the input differential pair of the preamplifier stage also reduces the impact of the parasitic capacitor $C_p$. From the model emerges that three sources of error are at the origin of transition position errors:

- Mismatch of the resistors of the reference divider.
- Mismatch of capacitors C.
- Switches non-idealities (clock feed-through and charge injection).

### *5.2.2- Thermometric to binary encoder*

Thermometer to binary code converter is one of the main design issues of ADC especially for flash ADC encoder. The followings equations gives the relation between the thermometric code and the binary code for 6-bit encoder.

The idea is to create an additional bit to benefits from the Z additional levels in redundancy of the converter to generated 5 bits in this case.

$$\mathbf{B_5 = I_{31}}$$

$$\mathbf{B_4 = I_{15}.\overline{I_{31}} + I_{47}}$$

$$\mathbf{B_3 = I_7.\overline{I_{15}} + I_{23}.\overline{I_{31}} + I_{39}.\overline{I_{47}} + I_{55}}$$

$$\mathbf{B_2 = I_3.\overline{I_7} + I_{11}.\overline{I_{15}} + I_{19}.\overline{I_{23}} + I_{27}.\overline{I_{31}} + I_{35}.\overline{I_{39}} + I_{43}.\overline{I_{47}} + I_{51}.\overline{I_{55}} + I_{59}}$$

$$\mathbf{B_1 = I_1.\overline{I_3} + I_5.\overline{I_7} + I_9.\overline{I_{11}} + I_{13}.\overline{I_{15}} + I_{17}.\overline{I_{19}} + I_{21}.\overline{I_{23}} + I_{25}.\overline{I_{27}} + I_{29}.\overline{I_{31}} + I_{33}.\overline{I_{35}} + I_{37}.\overline{I_{39}} + I_{41}.\overline{I_{43}} + I_{45}.\overline{I_{47}} + I_{49}.\overline{I_{51}} + I_{53}.\overline{I_{55}} + I_{57}.\overline{I_{59}} + I_{61}}$$

$$\mathbf{B_0 = I_0.\overline{I_1} + I_2.\overline{I_3} + I_4.\overline{I_5} + I_6.\overline{I_7} + I_8.\overline{I_9} + I_{10}.\overline{I_{11}} + I_{12}.\overline{I_{13}} + I_{14}.\overline{I_{15}} + I_{16}.\overline{I_{17}} + I_{18}.\overline{I_{19}} + I_{20}.\overline{I_{21}} + I_{22}.\overline{I_{23}} + I_{24}.\overline{I_{25}} + I_{26}.\overline{I_{27}} + I_{28}.\overline{I_{29}} + I_{30}.\overline{I_{31}} + I_{32}.\overline{I_{33}} + I_{34}.\overline{I_{35}} + I_{36}.\overline{I_{37}} + I_{38}.\overline{I_{39}} + I_{40}.\overline{I_{41}} + I_{42}.\overline{I_{43}} +$$

$$\mathbf{I_{44}}.\overline{\mathbf{I_{45}}} + \mathbf{I_{46}}.\overline{\mathbf{I_{47}}} + \mathbf{I_{48}}.\overline{\mathbf{I_{49}}} + \mathbf{I_{50}}.\overline{\mathbf{I_{51}}} + \mathbf{I_{52}}.\overline{\mathbf{I_{53}}} + \mathbf{I_{54}}.\overline{\mathbf{I_{55}}} + \mathbf{I_{56}}.\overline{\mathbf{I_{57}}} +$$

$$\mathbf{I_{58}}.\overline{\mathbf{I_{59}}} + \mathbf{I_{60}}.\overline{\mathbf{I_{61}}} + \mathbf{I_{62}}$$

While a $2^5$ thermometric code are mandatory to make transformation to 5 bits binary code, with the additional levels there are $(2^5 + Z)$ thermometric code prose using 6 bits algorithm in order to make conversion.

### *5.2.3- MDAC*

The MDAC is the module that compute the residue and the amplification in Digital to Analog CMOS technology conversion [25]-[27]. In figure 35 is depicted a typical switched capacitor circuit of the MDAC.

Three cycles are needed to produce the whole conversion:

- Sample phase (F1)
- Hold phase (F2)
- Amplification phase (F3).

The word produced by the flash during the hold phase (the so-called coarse conversion) is used to drive the MDAC during the amplification phase when the D to A conversion, the residue computation and amplification take place simultaneously

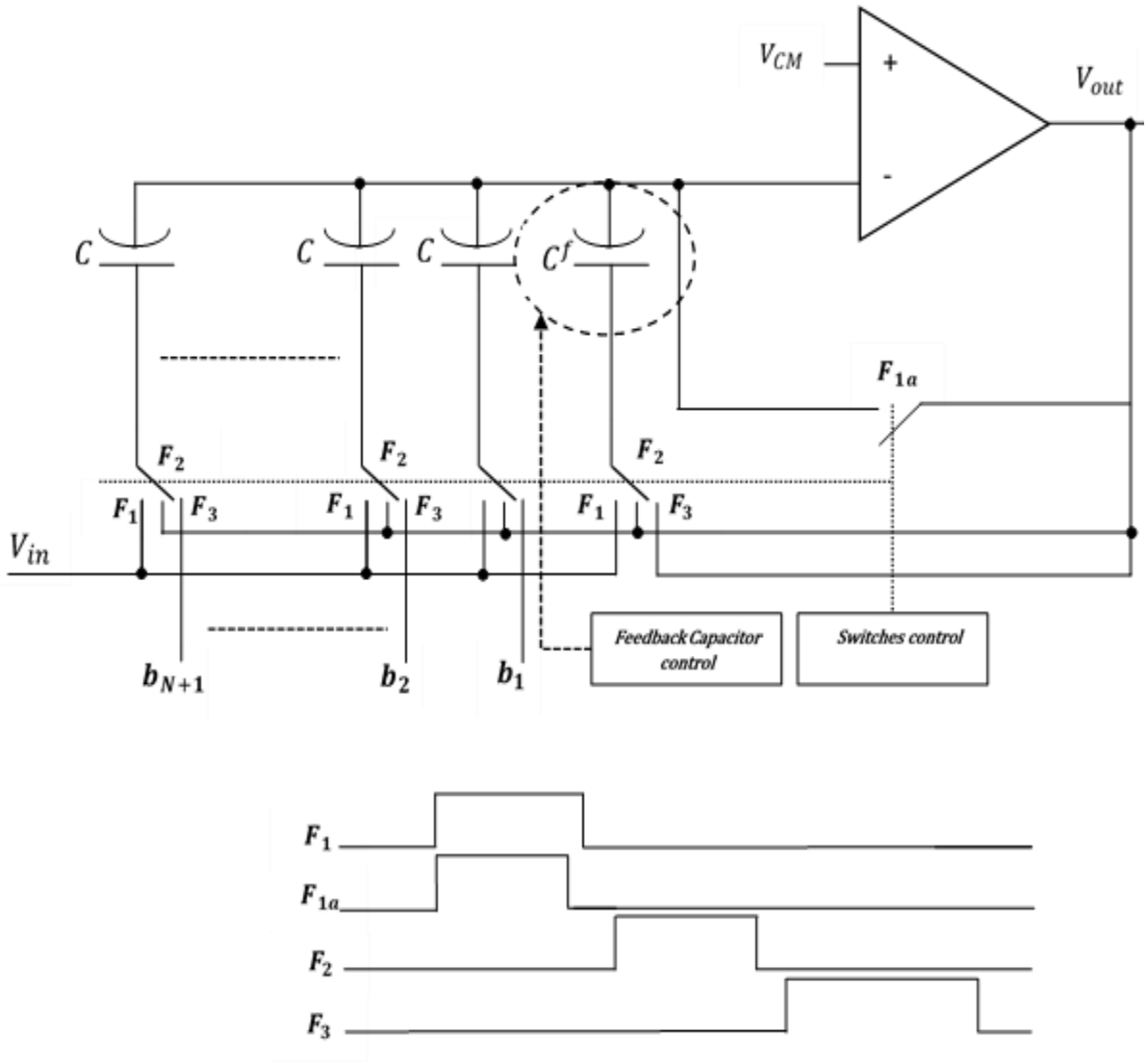



*Figure 35: Controllable Switched capacitors circuit of the MDAC with switching diagram*

### *Sampling phase (F1):*

During sampling phase, the input voltage $V_{in}$ is connected to capacitors as presented in figure 36.

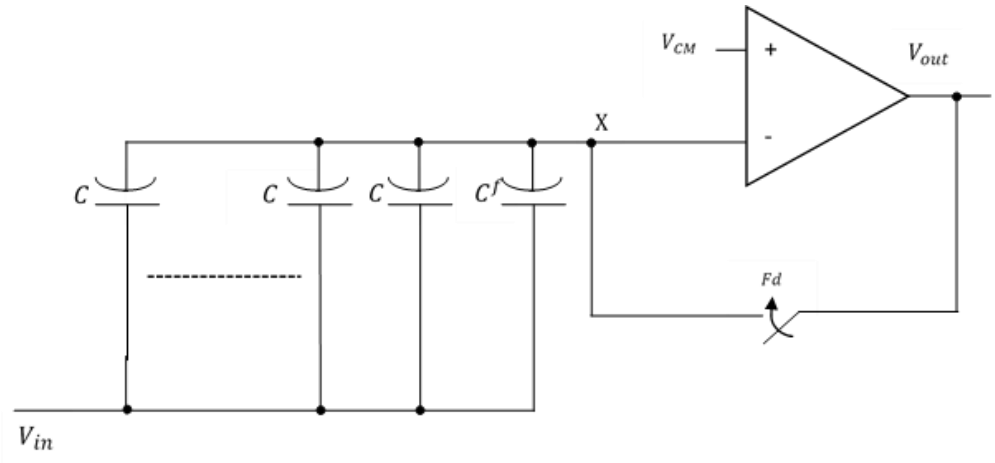



*Figure 36: MDAC in sampling phase.*

The charge at point X is given by: $Q_1 = (V_{in} - V_{CM})(\sum_{i=1}^{h} C_i + C^f)$ (5.7)

### *Amplification phase*

In the amplification phase figure 37, the charge at X is given by:

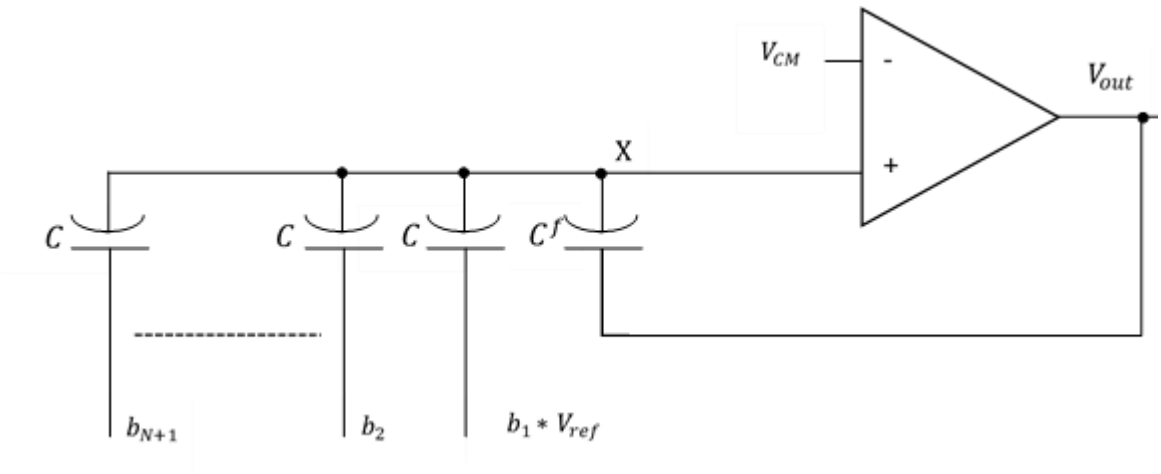



*Figure 37: MDAC in amplification phase.*

$$Q_2 = (V_{ref} - V_{CM})\left(\sum_{i=1}^{h} C_i b_i\right) - V_{CM}\sum_{i=1}^{h} C_i + (V_{out} - V_{CM})C^f$$

$$Q_2 = -V_{CM}\left(\sum_{i=1}^{h} C_i b_i + \sum_{i=1}^{h} C_i + C^f\right) + V_{out}C^f; \quad (5.8)$$

$$V_{CM} = \frac{V_{ref}}{2} \ ;$$

$$Q_2 = \left(\frac{V_{ref}}{2}\sum_{i=1}^{h} C_i b_i\right) - \frac{V_{ref}}{2}\sum_{i=1}^{h} C_i + \left(V_{out} - \frac{V_{ref}}{2}\right)C^f; \quad \mathbf{(5.9)}$$

Based on charge conservation principle the output of the MDAC at the end of the amplification phase is given by:

$$Q1 = Q2 \ ; \qquad V_{out} = V_{in}\frac{\left(\sum_{i=1}^{h} C_i + C^f\right)}{C^f} + \frac{V_{ref}}{2}\frac{\left(\sum_{i=1}^{h} C_i b_i\right)}{C^f}$$

$$\boldsymbol{V_{out} = \frac{\sum_{i=1}^{h} C_i + C^f}{C^f}\left(V_{in} + \frac{V_{ref}}{2}\frac{\sum_{i=1}^{h} C_i b_i}{\sum_{i=1}^{h} C_i + C^f}\right)} \quad \mathbf{(5.10)}$$

Where $\boldsymbol{h} = (\mathbf{2}^{\boldsymbol{M}} - \mathbf{1} + \boldsymbol{Z})$ is the number of unit elements depending on the actual converter.

The expressions for the magnitude of the unit elements of the parallel D to A converter and for the gain factor can be extract for (5.10):

$$\boldsymbol{ue[i]} = \frac{\boldsymbol{C[i]}}{\boldsymbol{C^f} + \sum_{\boldsymbol{i=1}}^{\boldsymbol{h}} \boldsymbol{C[i]}} \tag{5.11}$$

$$\boldsymbol{gain} = \frac{\boldsymbol{C^f} + \sum_{\boldsymbol{i}}^{\boldsymbol{h}} \boldsymbol{C[i]}}{\boldsymbol{C^f}} \tag{5.12}$$

The accuracy of the unit elements and of the relative gain are both related to the capacitor's matching of the MDAC. We define the feedback capacitor as $C_f = m.C_{ref}$ and the other capacitors as $C_{[i]} = n.C_{ref}$ , $C_{ref}$ being the unit capacitor, in order to rewrite ( 5.11) and ( 5.12) respectively as:

$$ue[i] = \frac{n.C_{ref}}{m.C_{ref} + \sum_{i=1}^{h} n.C_{ref}} \tag{5.13}$$

$$gain = \frac{m.C_{ref} + \sum_{i}^{h} n.C_{ref}}{m.C_{ref}} \tag{5.14}$$

From the definition of the unit elements given in table 3.1 and from (5.13) we can derive the relationship between the magnitude of the feedback capacitor

and the magnitudes of the bank of capacitors in CRZ (5.10) and in RSD (5.11) converters:

$$\frac{n}{m}|_{CRZ} = \frac{2^M - 1}{2^M - 1 + Z} \tag{5.16}$$

$$\frac{n}{m}|_{RSD} = 1 \tag{5.17}$$

While for the RSD converter all capacitors must be equal (m=n), the relative sizes between $C_f$ and the other capacitors are a function of the number of additional levels for CRZ converters. There are two ways to meet the (5.16):

- m-driven design-area matching : choosing m = 1 the capacitors C [i] must be equal to:

$$C_i = n.C_f = \frac{2^M - 1}{2^M - 1 + Z} \cdot C_f$$

Notice that since the size of C[i] is inversely proportional to Z while the number of unit elements (and then the number of capacitors C[i]) grows with Z, this choice implies that the occupation of area and the capacitive loading of the OpAmp (i.e. the power consumption) are independent by Z. However, the reduction of the size of C[i] with the introduction of additional levels makes this solution highly sensitive to mismatch errors (transition magnitude and gain errors).

- n-driven design- mismatch matching: On the contrary, choosing n = 1, the capacitors C[i] are all equal to the unit capacitor while $C_f$ is:

$$C_f = m.Ci = \frac{2^M - 1 + Z}{2^M - 1}.C_i$$

Now both area and power grow with Z but the introduction of additional levels effectively reduces the sensitivity of the converter against mismatch errors as we will see in section 5.3.2.

## *5.3- Simulation Results*

In this section we present the results of system level simulations concerning the impact of the non-idealities on the considered two-steps A to D algorithmic converters. The impairments of the flash A to D converter and of the MDAC are related to the matching of the passive components in order to find the best sizing for a given resolution. A clear distinction is made between CRZ MDAC with m-driven (m=1) and n-driven (n=1) design.

### *5.3.1- Impact of transition position errors*

As declaring before, transition position errors are due to the contribution of three sources of error:

Mismatch of the resistors of the reference divider, non-idealities of the switches and mismatch of capacitors C. Simulations showed how switches impairments as well as the mismatch of capacitors C have negligible effects on the output response of the converters, while the matching of the resistors strongly influences its effective resolution. Figure 38 shows the results of simulations concerning the impact of matching impairments among the resistors of the reference divider.

All the switches of the scheme in figure 33 are designed as transmission gates using minimum size transistors while capacitors C are modeled as poly1-poly2 capacitors with mean magnitude C = 5 [$f$ F] and standard deviation $\sigma_C^{comp} = 6\%$.

The results coming from the behavioral model are here confirmed, but now the matching of the resistors of the reference divider is related with their sizes. figure 39 also shows the estimation of the area needed by the reference divider for CRZ converters, $\sigma_R$ being the standard deviation of the single resistor.

### *5.3.2- Impact of MDAC matching impairments*

Mismatches among any of the capacitors $C_i$ and $C_f$ in the scheme of figure 34 result in transition magnitude and gain errors. As derived from the behavioral model, when CRZ converters with odd Zs are considered, transition magnitude errors do not affect the ENOB as showed in figure 40, but only the $N_{fs}$.

Figure 40 show the results of simulations for CRZ converters affected by capacitors mismatch issues. Two different solutions have been considered: the upper picture in figure 40 optimizes the matching while the second one optimizes the area. The dashed lines on both curves portray the locus of the$\sigma_{cap}$, beyond which non-monotonicity errors are experienced. Finally, the upper picture in figure 41 show the estimated occupation of area for the capacitors for both n-driven and the second showed for m-driven design in the [$\sigma_{cap}$, Z] plane (notice that they differ for two order of magnitude).

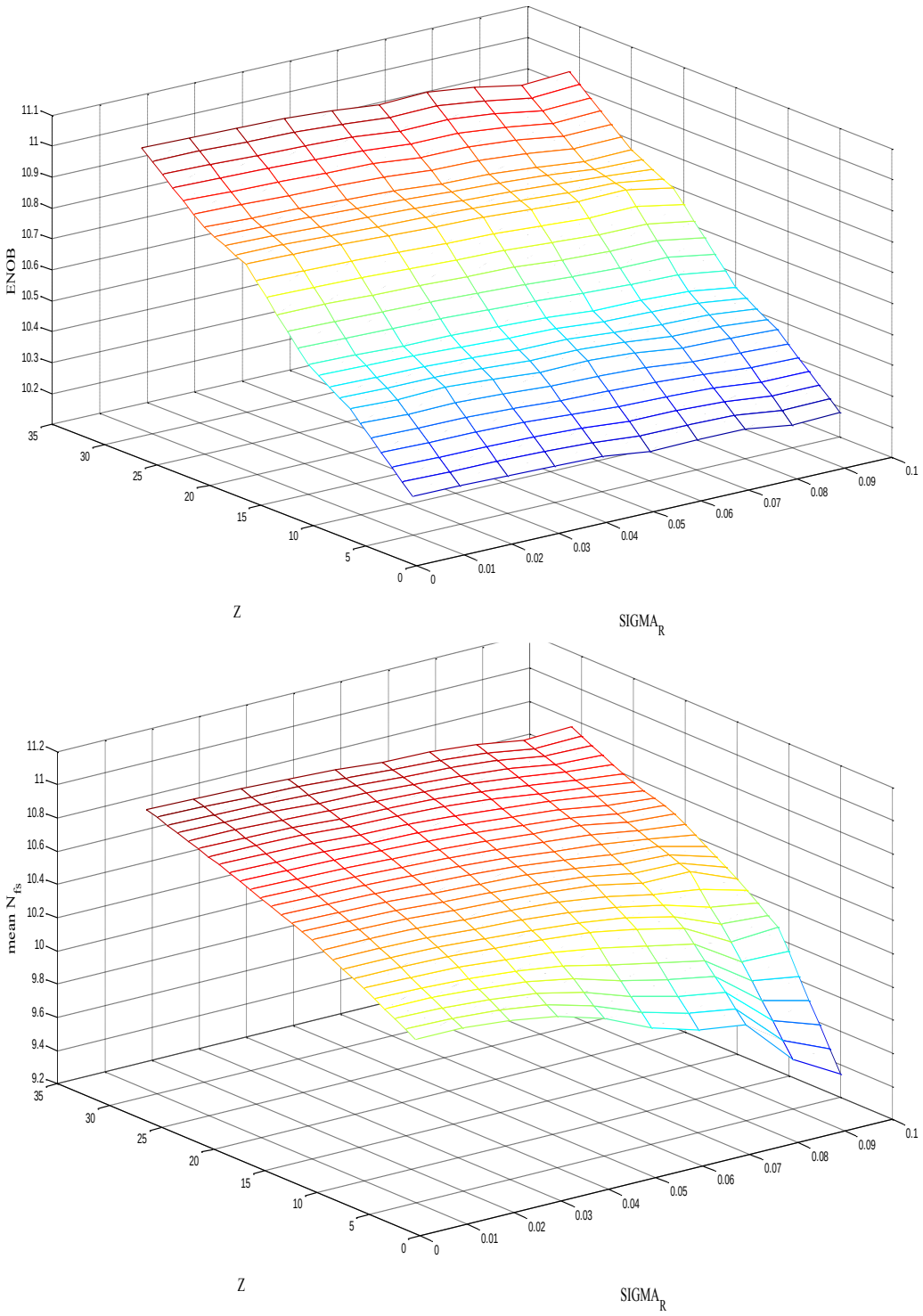



*Figure 38: Impact of resistor's mismatch on CRZ converters.*

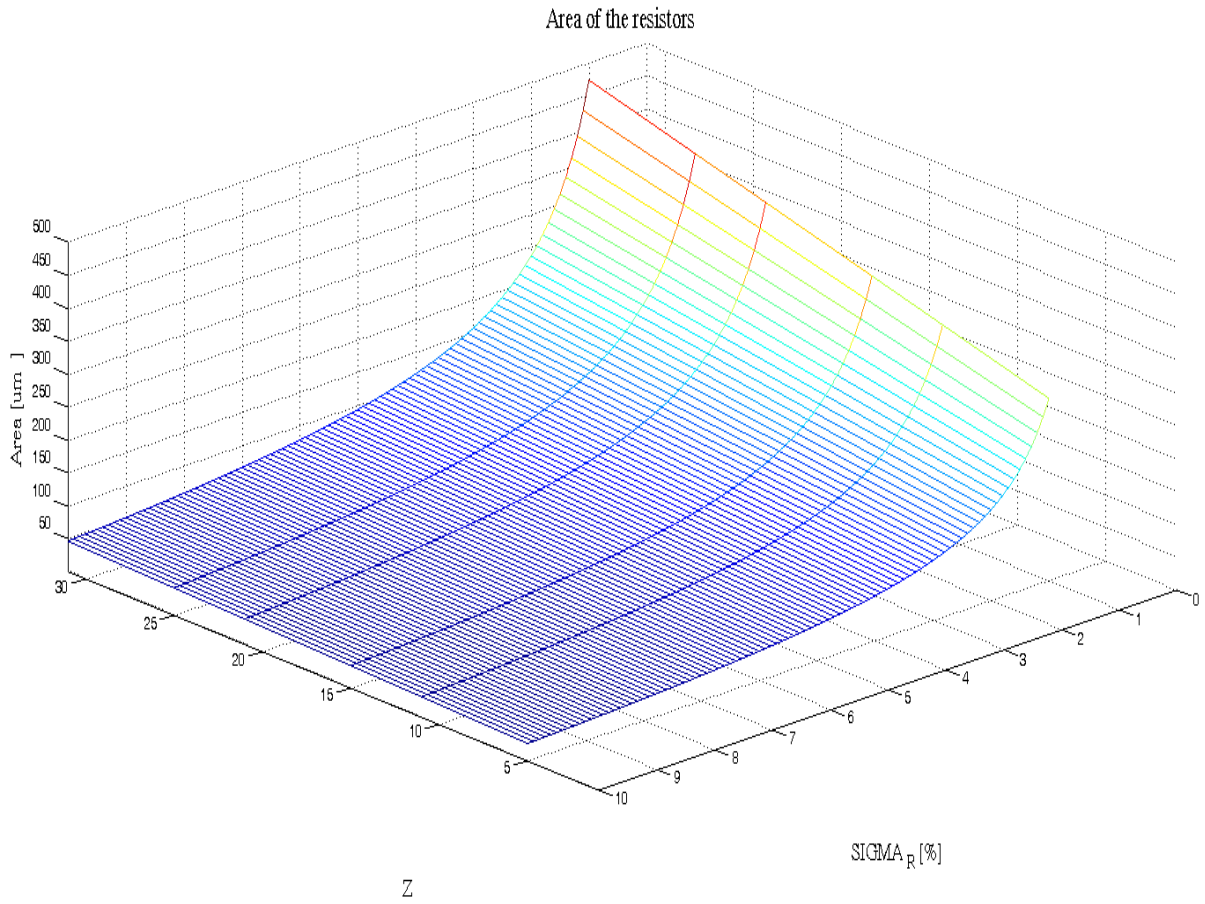



*Figure 39: Estimated area needed by the resistors of the reference divider, as a function of the error* $\boldsymbol{\sigma_R}$ .

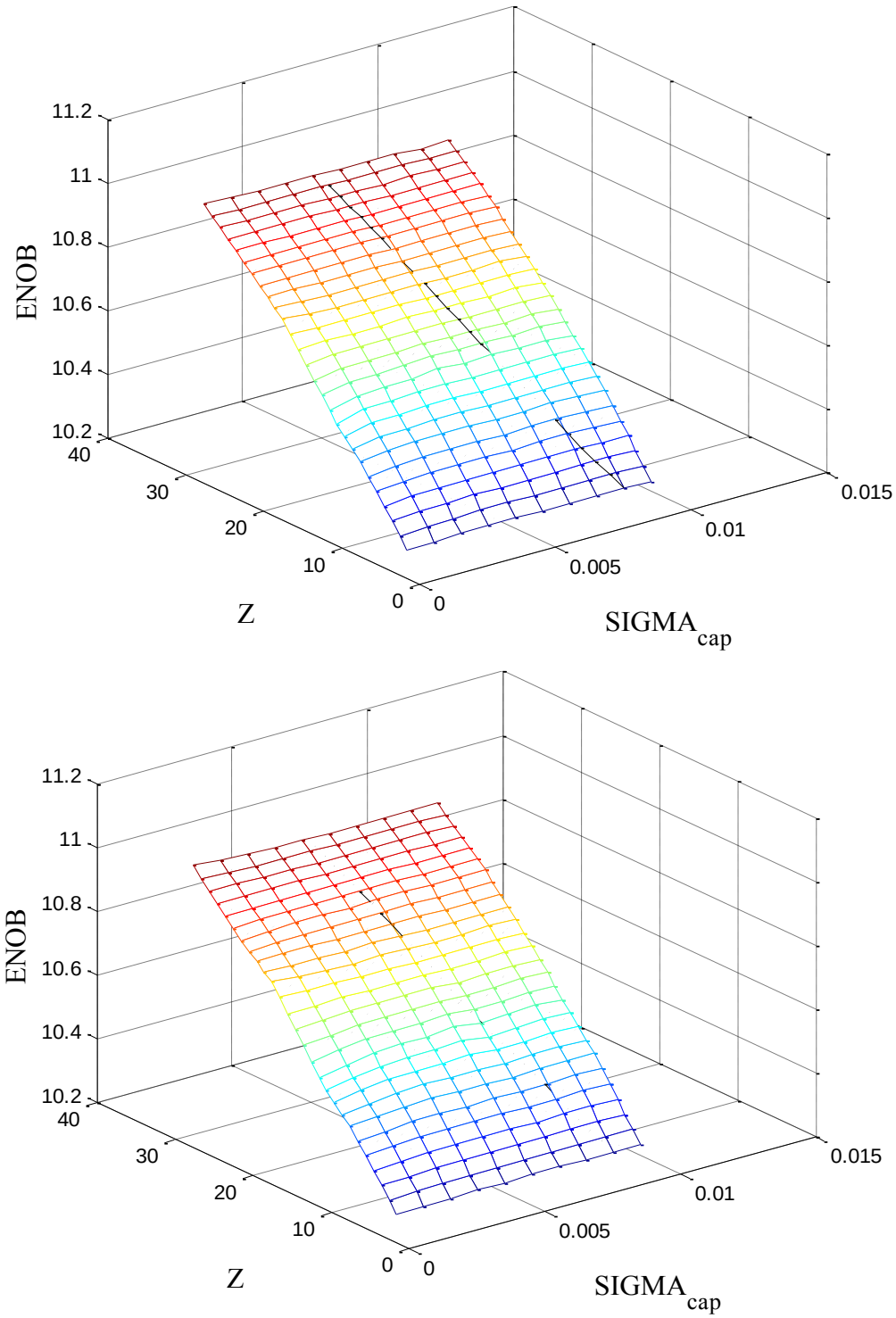



*Figure 40: Impact of capacitors mismatch at ENOB on CRZ converters.*

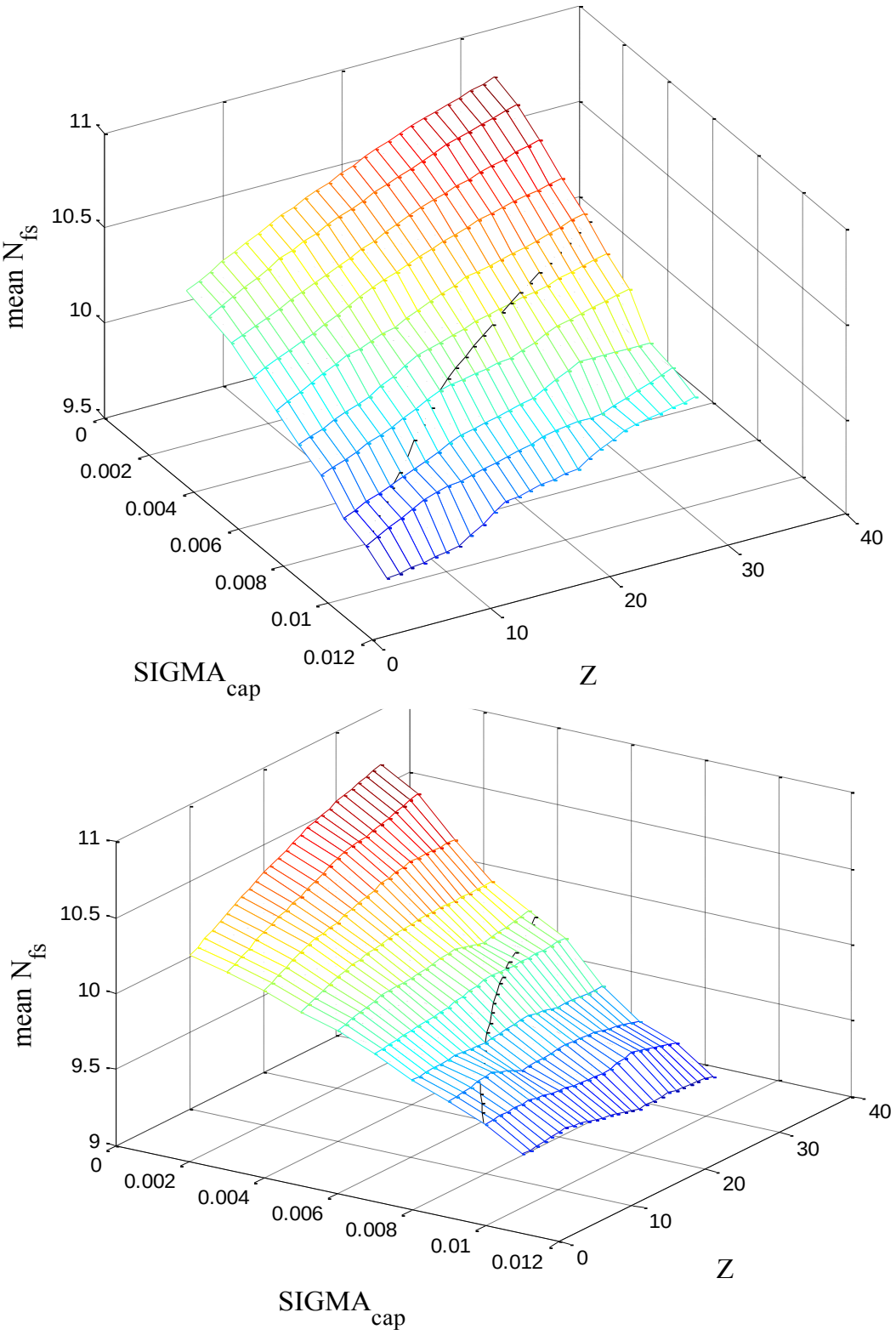



*Figure 41: Impact of capacitor mismatch at ENOB on CRZ converters.*

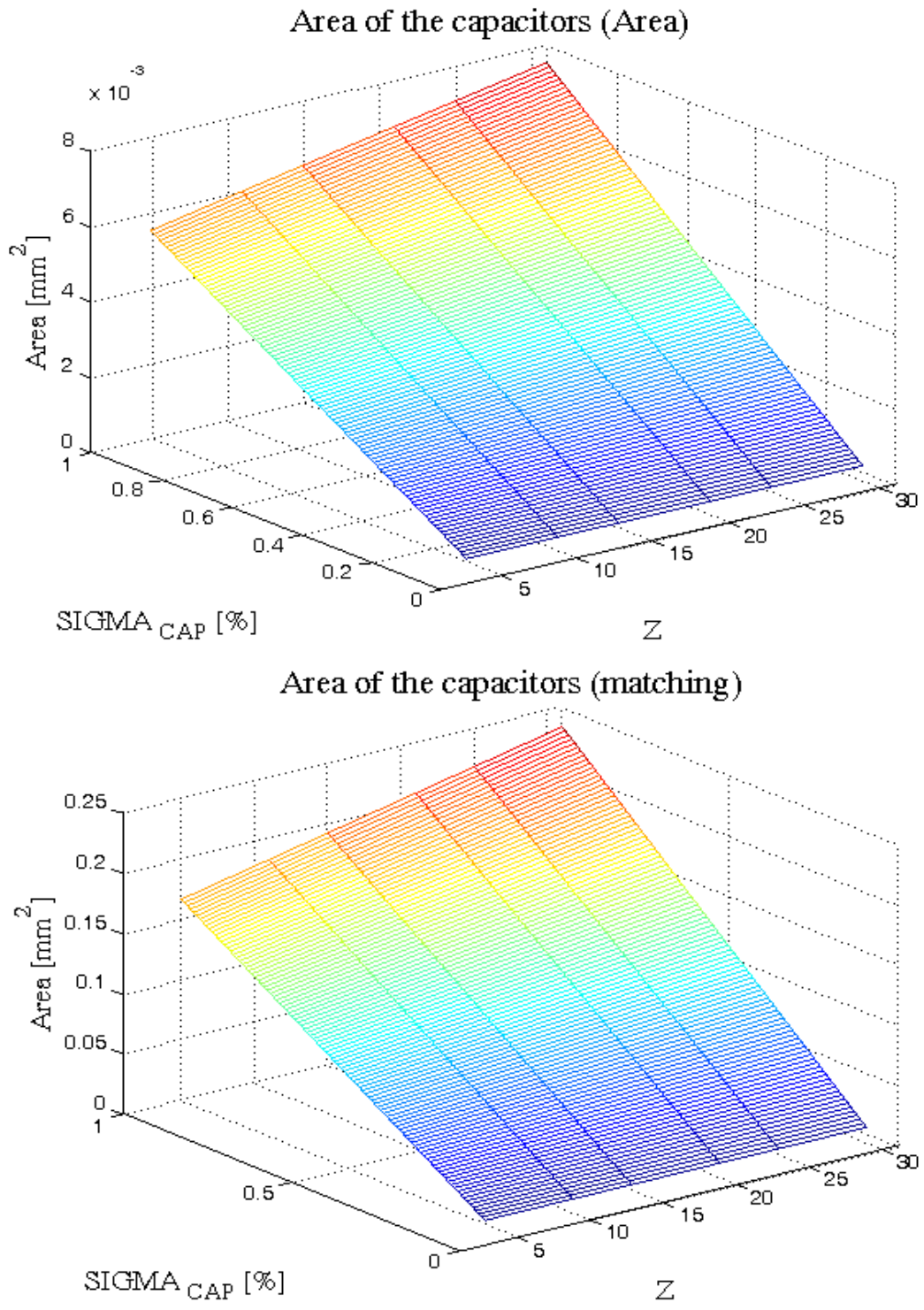



*Figure 42: Estimation of the area needed by the bank of capacitors for CRZ.*

## *5.4- Comparison between CRZ and RSD converters*

As discussed in section 3.7, the RSD and the CRZ converter with $Z = 2^M - 1 = 31$ are characterized by the same occupation of area and by the same sensitivity against transition position errors. On the contrary, mismatches among any of the capacitors of the MDAC provide a different impact on the output response of CRZ and RSD converters. As derived from the behavioral model, converters affected by transition magnitude errors differ for the Nfs but not for the ENOB. In particular, simulations from the circuital model showed that the RSD and the equivalent CRZ converter with n-driven design show the same sensitivity against impairments derived from capacitors mismatch issues ( see figure 43), while the m-driven design, although allows to minimize the area, shows a larger sensitivity against the same errors.

Finally, figure 44 shows the estimated area needed by the bank of capacitors against the error $\sigma_{cap}$.

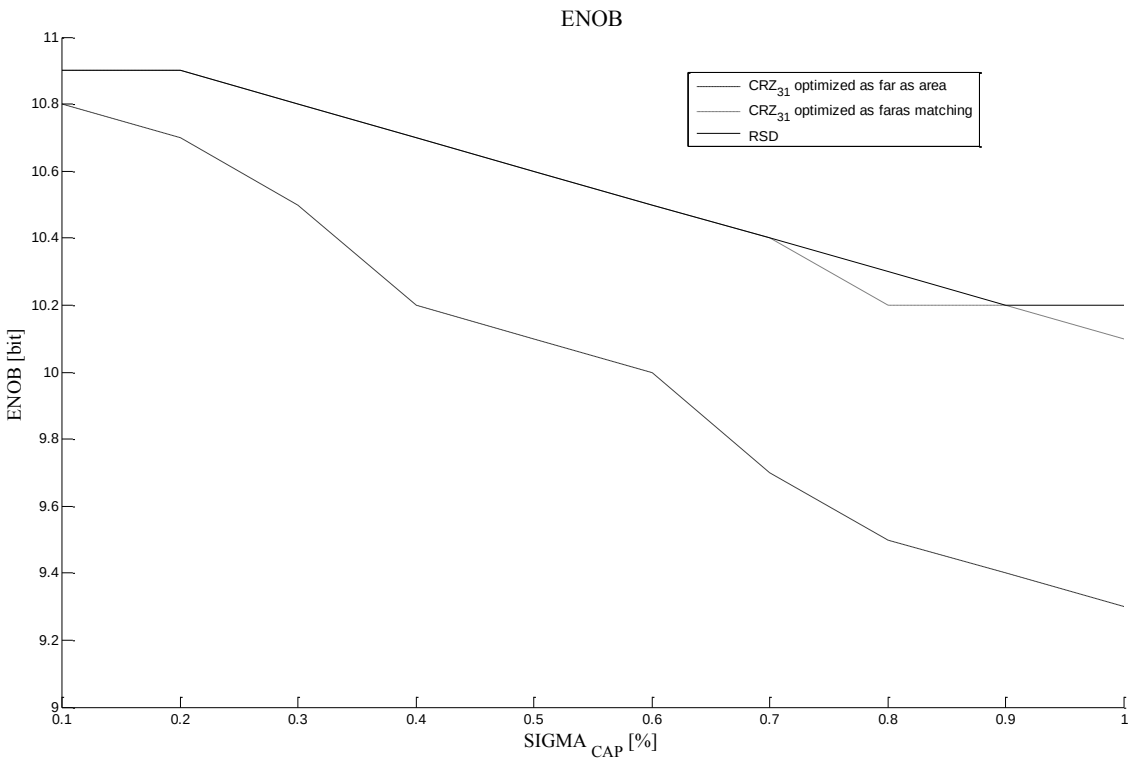



*Figure 43: Comparison of the Nfs for two-step RSD and CRZ (Z=31) converters for both n-driven and m-driven designs.*

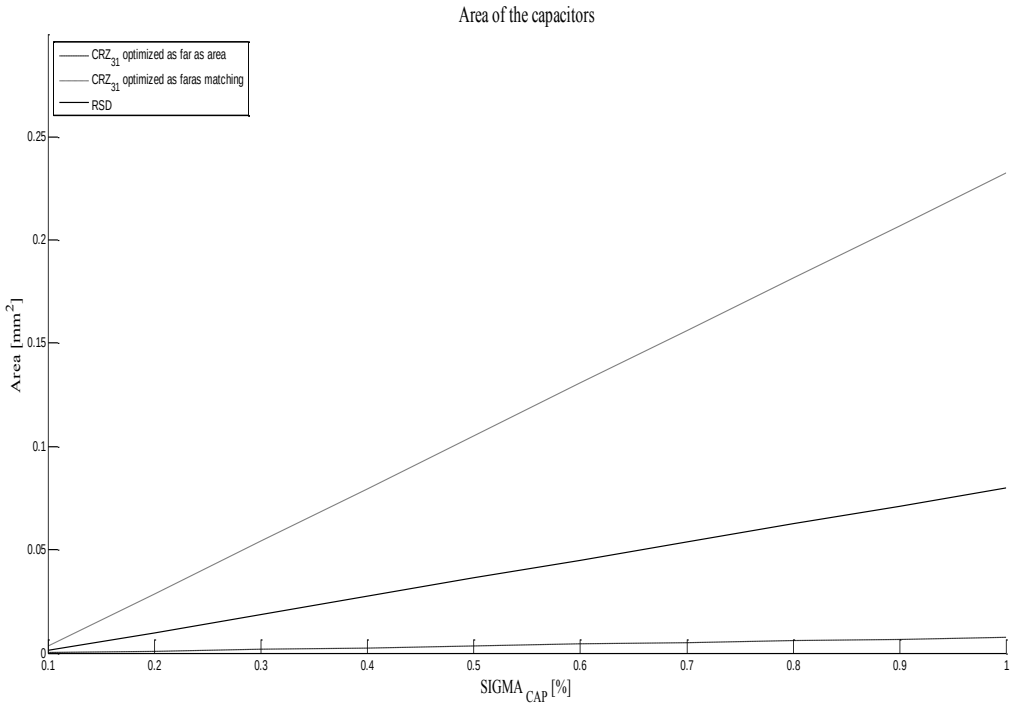



*Figure 44: Comparison of the area for two-step RSD and CRZ (Z=31) converters for both n-driven and m-driven designs .*

# 6- Cadence Design

## *Introduction*

The Cadence Spectre circuit simulation platform, built on an advanced infrastructure, combines industry-leading simulation engines to deliver a complete design and verification solution. It meets the changing simulation needs of designers by preserving design intent as they progress through the design cycle—from architectural exploration, to analog and RF block-level development with flexible and reliable abstraction, to final analog and mixed-signal full-chip verification for increased productivity and throughput.

This chapter presented the cadence schematics design of different circuit presented in previous chapter also a complete simulation circuit test is presented in order to simulate the hole design.

## *6.1- Flash resistances chain*

A resistor in integrated technology is made of a thin strip of resistive layer. The total resistor R is defined $R = 2R_{cont} + \frac{L}{W} R_{\square}$ . Where $R_{cont}$ is a localized resistance describing the endings and metal connection contacts, and $R_{\square}$ is the sheet resistor.

Design a modifiable chain propose using configurable switches allow the controlling of peripheral resistors XR as well as the length of series resistors to generate the adequate references values for each additional level of redundancy Z as presented in the fig.44. Buffers are used between flash references and comparators.

The resistors matching defined by $\sigma(\Delta R) = \frac{A\_R}{\sqrt{W.L}}$ , $A\_R = 6.5\,\%$ for RPOLYH using AMS technology

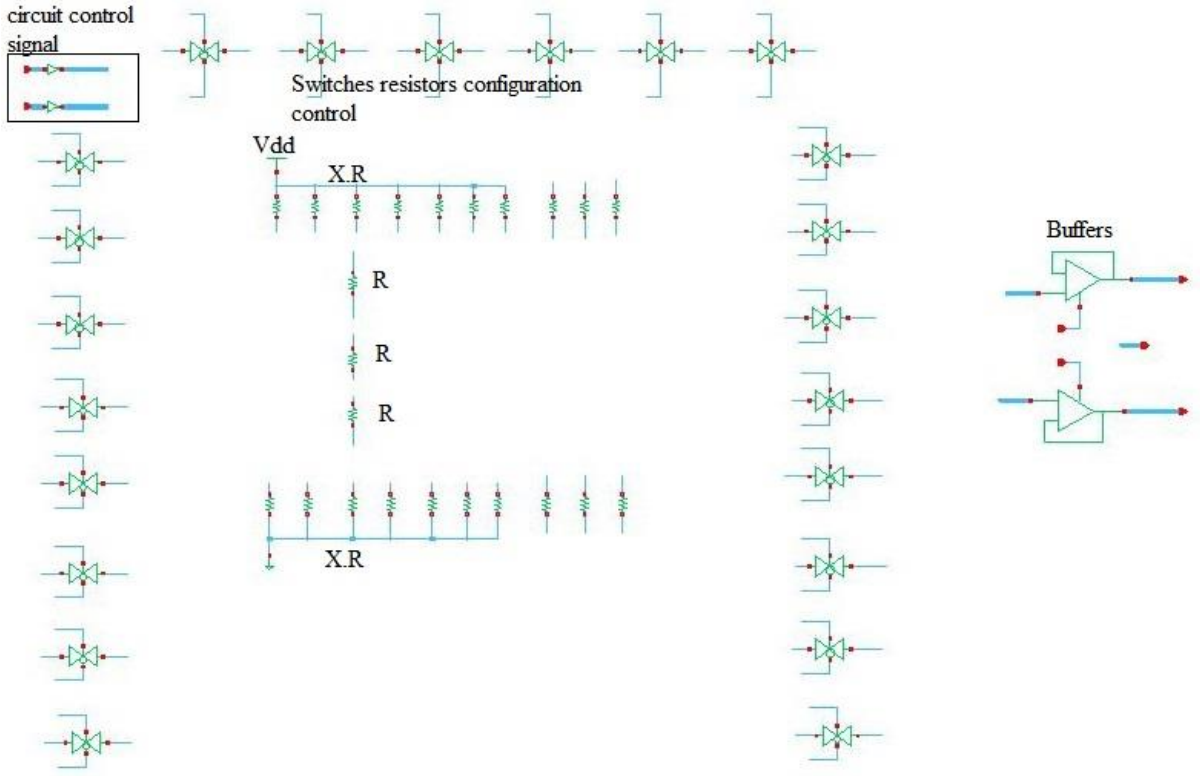



*Figure 45: Conventional Restoring analog to digital with Z added levels of redundancy (CRZ).*

## *6.2- Flash converter comparator*

The design of flash comparators as we introduced in section 5.2.1 is presented in figure 46. Two cycles are necessary to performing the thermometric code through latches.

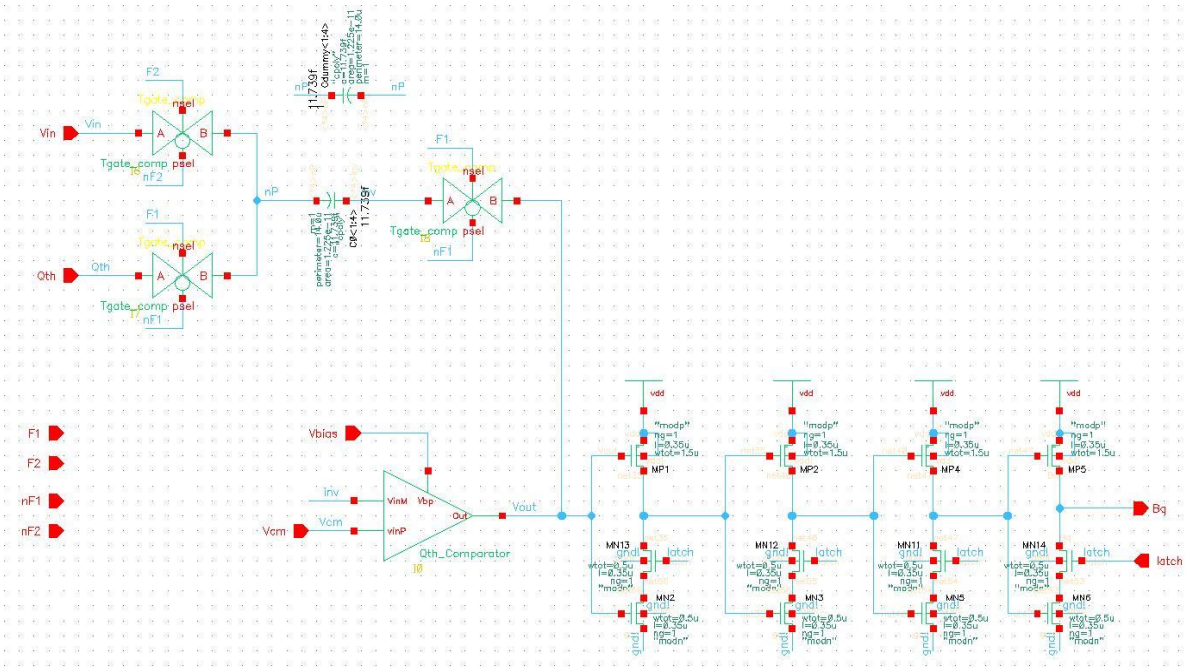



*Figure 46: Flash Comparator with Latch.*

## *6.3- MDAC*

As mentioned before MDAC is the module that compute the residue and the amplification in Digital to Analog. Figure 47 show the mains blocks of MDAC consisted of modifiable bank of capacitor figure 48 depending in the given value of Z, and two stages amplifier where the output is the amplified residue of the previous stage that will consist the input of the next stage.

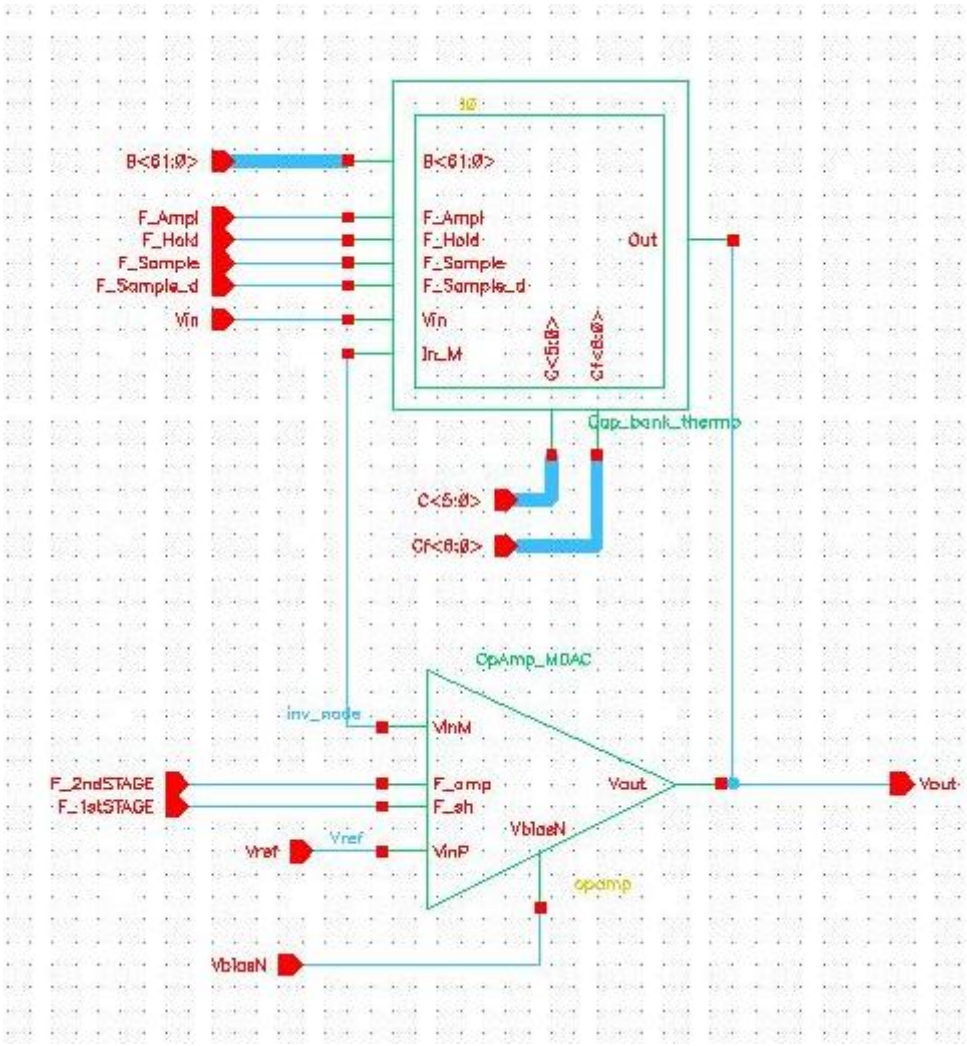



*Figure 47: MDAC schematic.*

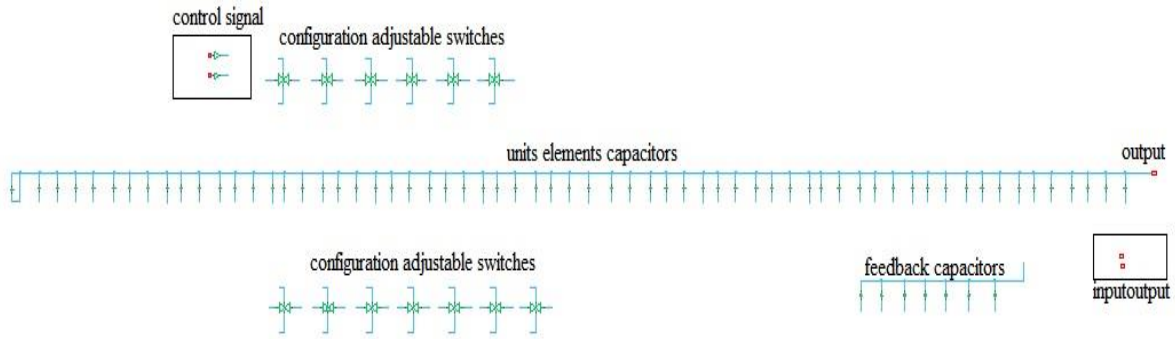



*Figure 48: Bank Capacitor schematic.*

## *6.4- Control block*

Generating different signals of control and coordinate different phase of A/D conversion process is mainly accomplished by a Verilog control unit block, based at clock signal , reset , and start as input signal of this block as showed Figure 49.

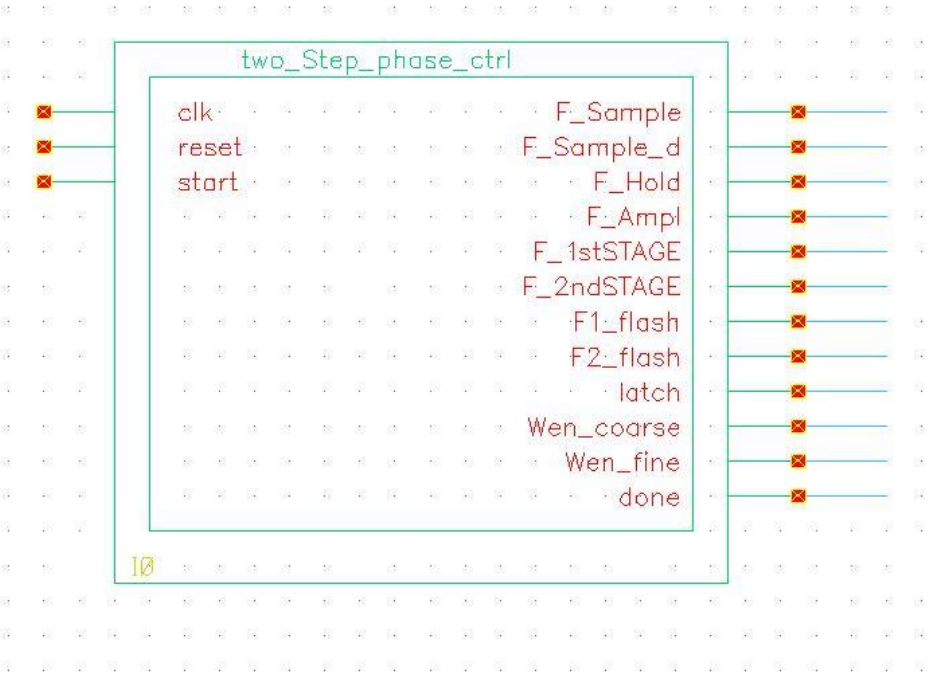



*Figure 49: Control unit of 2-steps A/D.*

## *6.5- Simulation Results*

Figure 50 is the schematic view for the test bench circuit used to simulate the two steps A/D converter. Where also presented the different previous schematics in addition a Verilog block that control the additional levels of redundancy , an ideal Analog to digital converter in order to make a comparison of the produced results with the ideal one and a biasing block that generate the different biasing currents in the hole circuit.

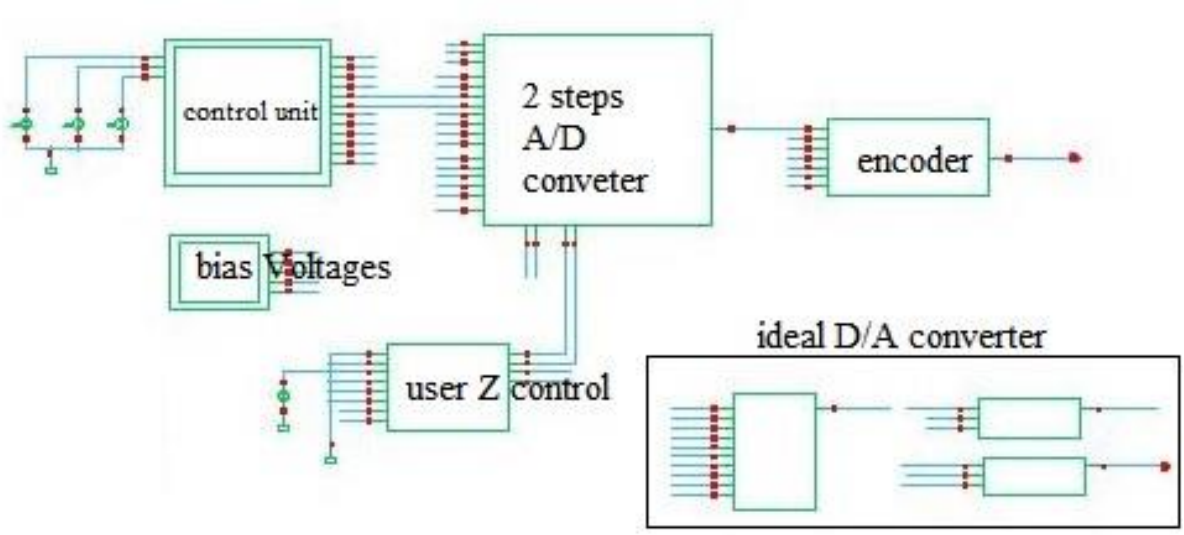



*Figure 50: Test bench circuit schematic.*

The simulation of such circuit produced a different output signals with corresponding of the different stages of conversion.

The output of the control unit introduced in previous paragraph is presented in figure 51 where different control signals are generated controlling different parts of the converter.

While figure 52 and figure 53 is just showing the different reference levels for flash converter CRZ here Z=0 and Z=15 respectively.

The most import output is the digital output of the encoder that corresponding to the entrance input held. Figure 54 and figure 55 are the digital output of held voltage

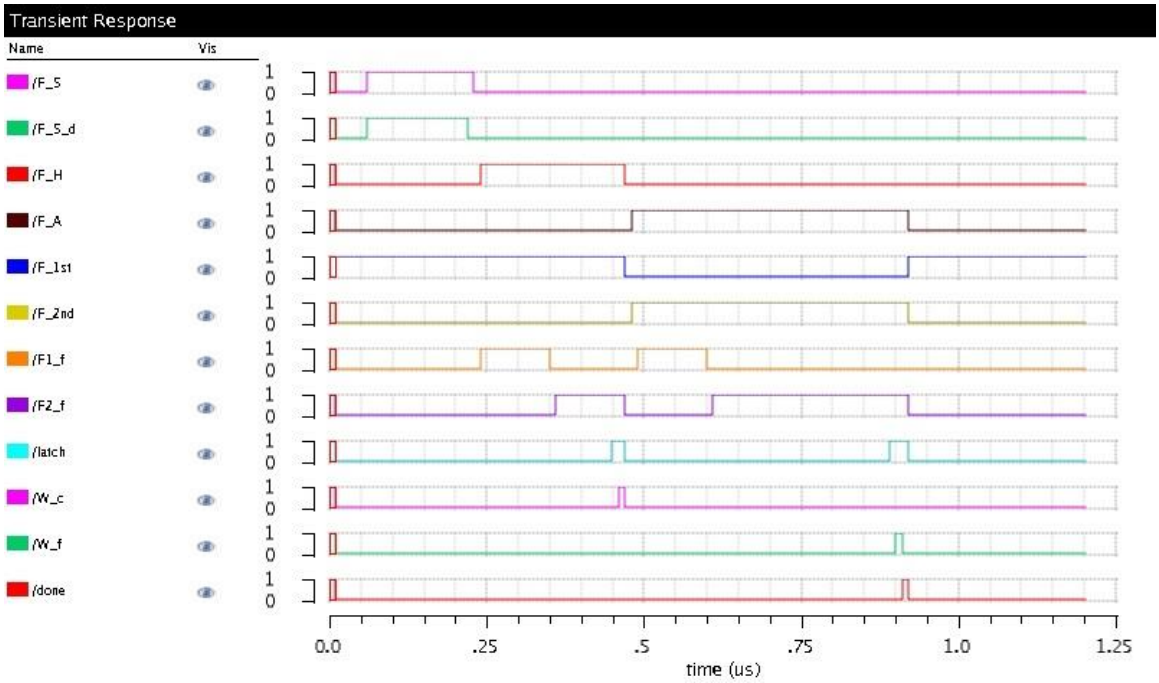



*Figure 51: Signals control of control unit.*

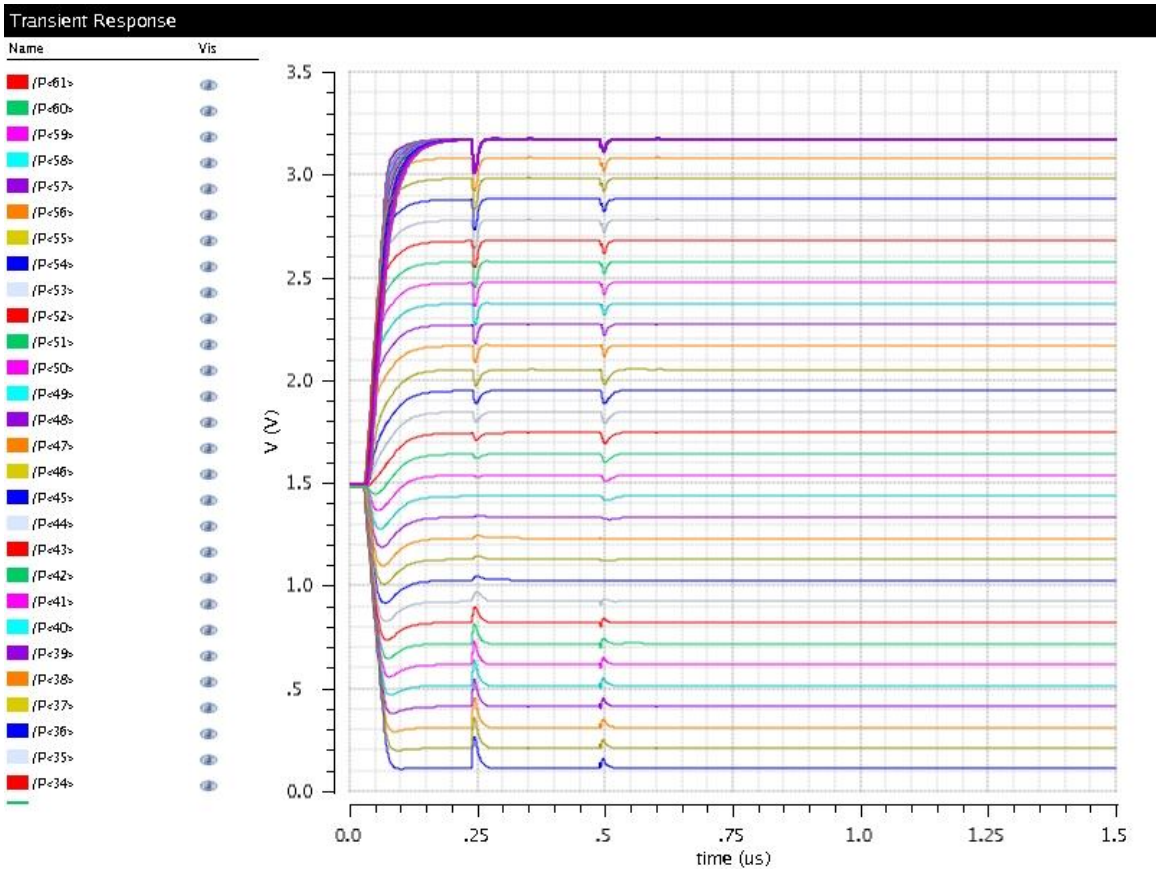



*Figure 52: Flash references for Z=0.*

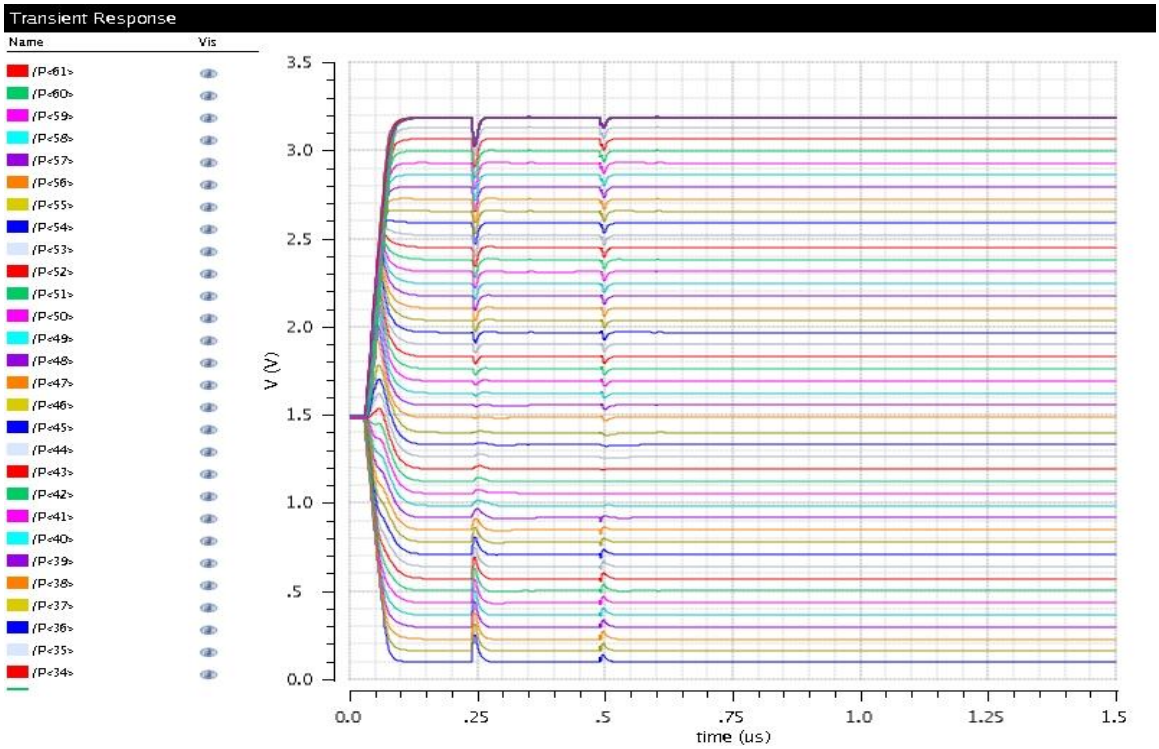



*Figure 53: Flash references for Z=15.*

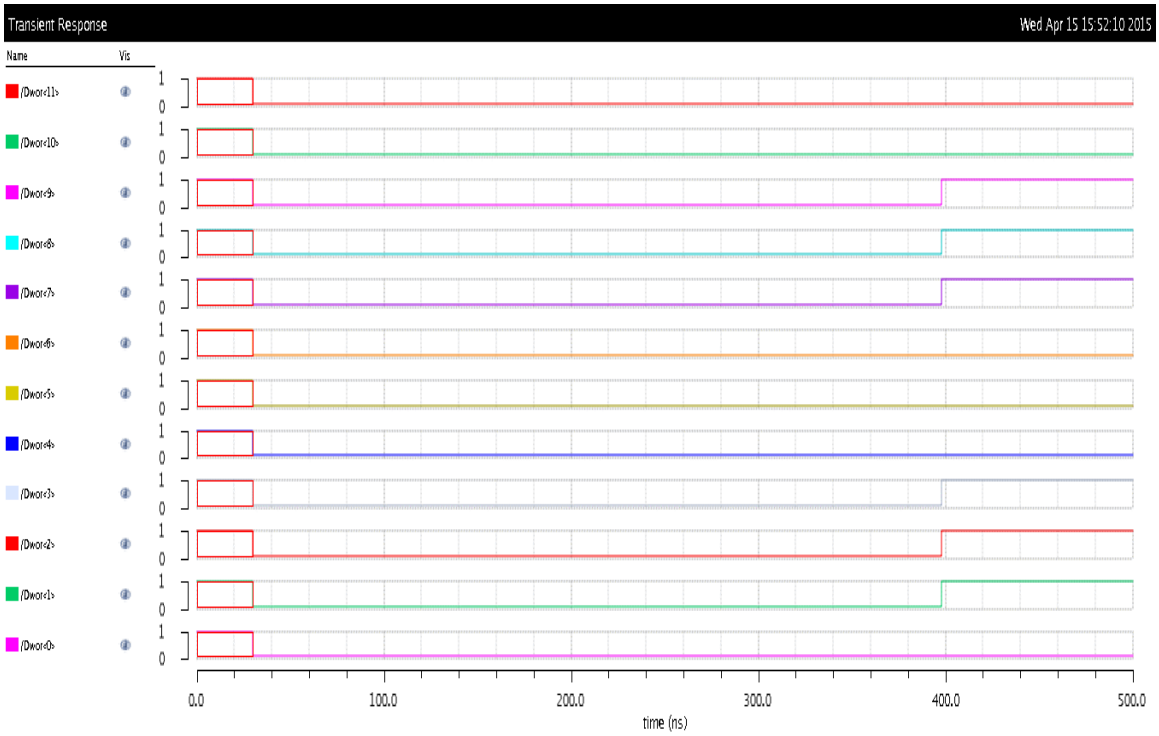



*Figure 54: Digital output for V=1v, Z=15.*

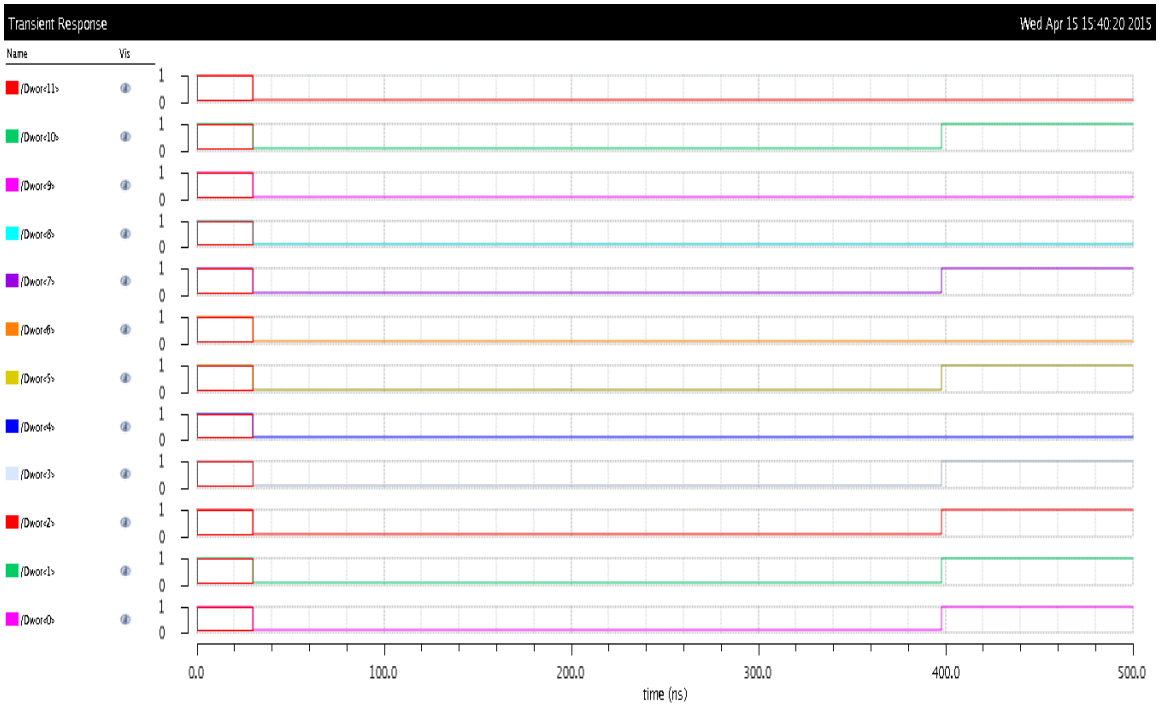



*Figure 55: Digital output for V=1v, Z=31.*

## *6.6- Conclusion and Results Discussion*

In this thesis, designing of circuit-modified structure is successfully applied to different part of analog to digital structure by making allow the user control the modification by just choosing the value of the additional levels Z the circuit automatically modified allow us testing a different predefined value of Z as showing figures 50-54.

The equivalent analog part for digital is approximately equal to V=1 volt with an error $<< \frac{V_{lsb}}{2^{N+2}}$ . The arbitrary digital code depending on Z levels , that propose to utilize a digital correction methodology in order to generate a unique digital output whatever the additional level of redundancy used.

# CHAPITER 7: CONCLUSIONS OF FUTURE WORK

This is a continuous work of previous of thesis, which mainly focus on the study of CRZ and RSD, and design a CMOS circuit based on RSD redundancy. We reproducing all previous results in this thesis, in addition, we study of the two different design of a high-level approach to assess how the introduction of redundancy in the output code can improve the effective resolution of two-step converters. Investigating the impact of several sources of errors on CRZ converters, which were derived from the conventional CR converter with the introduction of Z additional decision levels, as well as on the RSD converter, used earlier only in cyclic algorithm converters.

Two levels of abstraction are modeled each converters. First, a behavioural is used to identify the effect of transition position, transition magnitude, and gain errors on the effective resolution of the converters, in terms of ENOB and Nfs. Simulations on the behavioral model showed that transition position errors are corrected automatically during the fine conversion, referred to the redundancy in the output code, while the impact of transition magnitude errors on the ENOB can be reduced using an odd number of additional levels. Redundancy

has a weaker impact on the gain error, which must be kept under control when large number of cycles are contemplated.

A circuital model of the converters was introduced to find the optimum sizing of passive components meeting a given resolution at an early design stage. Here non-idealites are related to mismatch impairments of passive components, using the technological parameters from the AMS035 technology.

The results coming from the behavioural model have been confirmed by simulations on the circuital model, which also allow to estimate the area needed by the passive components. The impact of transition position errors can be reduced in the CRZ domain by increasing the number of additional levels, but this occurs at the expense of area and power consumption. The same circuitry for the MDAC has been considered for both classes of converters, investigating the impact of the capacitor's mismatch. We proposed two solutions for the design of the MDAC in the CRZ domain, showing how the m-driven design allows to reduce area and power consumption but at the expenses of a larger sensitivity against these errors. The sensitivity of the RSD converter is comparable with the one shown by the n-driven $CRZ_{31}$ converter, but the latter needs more power and surface.

The cadence designed of the circuit-modified structure is successfully applied to different part of analog to digital structure by making allow the user control the modification by just choosing the value of the additional levels Z the circuit automatically modified allow us testing a different predefined value of Z as showing previously. In other hand the circuit still suffer from the error that come from the fact the $V_{lsb}$ is depend of the number of additional levels Z that lead to produce arbitrary digital code and propose to utilize a digital correction methodology in order to generate a unique digital output whatever the additional level of redundancy used.

Now we work to design an adjustable silicon circuit that can able to producing both RSD and CRZ with more than Z levels, and let the user to choose depending on application and number of bits, resolution and redundancy of the converter.

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