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**ELECTRONIC BIDIRECTIONAL INTERFACES TO THE PERIPHERAL
NERVOUS SYSTEM FOR PROSTHETIC APPLICATIONS**

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Introduction

Human beings have always been fascinated by the sophisticated and intricate nervous system that regulates and coordinates our organism. The possibility to extract and elaborate the information generated by the brain is a gripping idea that has inspired a lot of science-fiction writers and movie directors over the years. Obviously, the possibility to "read minds" is still confined in the science-fiction field, but combining together the impressive advancements in microelectronics, robotics and biomaterials achieved in last decades, many of those ideas thought to be impossible to fulfill up to ten years ago, are now closer to become reality. One of these subjects is the possibility to extract neural signals from the Peripheral Nervous System (PNS) and to use them outside of the human body: this is precisely the goal of the present thesis. The final aim of the project in which this work is involved is in fact the realization of a prosthetic hand controlled using neural signals. In particular in this thesis the focus has been put on the development of special electronic devices for neural signal acquisition and PNS stimulation. The commercially available prosthesis are based on Electromyographic (EMG) signals, their use implies unnatural movements for the patient that needs a special training to develop the control capabilities over the mechanical limb. The proposed approach offers a number of advantages compared to the traditional prosthesis, first because the signals used are the same used to control the biologic limb, allowing a more comfortable solution for the patient that will be closer to feel the robotic hand as a natural extension of his/her body. Secondly, placing temperature and pressure sensors on the limb surface, it is possible to trasduce such information in an electrical current that, injected into the PNS, can restore the sensory feedback in amputees. The weakness of the neural signals (neural spike amplitudes can span from few microvolts to hundreds of microvolts) makes their recording a critical operation and requires special care in terms of low noise and low power design. Neural spike bandwidth lies in the frequencies from $500Hz$ to $10kHz$ with a peak around $2kHz$ and it partially overlaps with that of EMG signals which have amplitudes several order of magnitude higher than that of neural signals.

EMG signals are, for this reason, the most serious interference to cope with. Fortunately the spectral signature of EMG decreases with frequency and, at 800Hz has an energy lower than that of neural signals. Using a proper filter stage in the front-end circuit, it is then possible to isolate the neural signals and to prevent the EMG to mask them completely. On the other hand, the stimulation circuitry must provide current pulses whose amplitude, duration and frequency evoke the programmed stimulus without damaging the tissues. In this contest, our final goal is the development of a fully implantable device able to perform a bidirectional communication between the robotic hand and the patient. Due to small area, low noise and low power constraints, the only possible way to reach this aim is the design of a full custom Integrated Circuit (IC). However a preliminary evaluation of the key design features, such as neural signal amplitudes and frequencies as well as stimulation shape parameters, is necessary in order to define clearly and precisely the design specifications. A low-cost and short implementation time device is then needed for this aim, the Components Off The Shelf (COTS) approach seems to be the best solution for this purpose. A Printed Circuit Board (PCB) with discrete components has been designed, developed and tested, the information extracted by the test results have been used to guide the IC design.

In the first chapter an overview on the main characteristics of the neural cells and on the electrochemical processes involved in the neural spikes generation is presented. A brief description of the project in which this research is part is also provided, finally an analysis on the state of art concerning the neural-machine interfaces is presented.

The second chapter is aimed to the developing of a PCB system for neural recording and stimulation. The proposed neural interface allows the bidirectional communication between an electrode inserted in the PNS and a host computer. The designed system is composed by three main blocks: the recording circuit, the stimulation unit and the digital system controller. The extracellular signals are extracted from a 8 channel electrode then they are acquired and filtered by a recording circuitry in order to remove noise and other biological interferences. The stimulation circuitry delivers trains of electrical charge pulses to excitable tissue, via the electrode. The system receives stimulus patterns from the digital controller and converts them into a stimulation current to be injected into the PNS. The digital system controller has two main tasks. First, it provides power from a rechargeable battery to ensure the isolation of the patient from the electric grid (both for safety reasons and to reduce the interferences injected by the grid). Main task of the module, however, is managing the configuration of the whole system with the generation of timing signals, programmable gain and stimulation patterns.

For a high-speed real time data transmission a Universal Serial Bus (USB) controller has been integrated in the system. A Graphical User Interface, that allows the user to have a real time control on the acquisition and on the stimulation and to modify the programmable parameters, has also been developed. The system has been successfully tested with in-vivo experiments on rats performed at the "Universitat Autònoma de Barcelona" thanks to Prof. Xavier Navarro. The results confirmed the capability of the system to record neural signals of few microvolts and to provide stimulation patterns capable to elicitate the PNS of the rat. The design, implementation and testing of all the COTS system has been developed in close collaboration with Ing. Daniela Loi at the Department of Electrical and Electronic Engineering at University of Cagliari.

The third chapter presents an IC system for neural recording composed by the cascade of a preamplifier/ prefiltering block and a sigma delta modulator. The signal acquisition chain has been designed using two parallel models: a high level simulation model in Simulink environment has been used for a first rapid evaluation of the system properties and to define the needed specifications for each sub-module. Consequently, a transistor level simulation model, developed in cadence environment, describes precisely the circuit components and gives more reliable information on the specification meeting. The task of the preamplifier/prefiltering block is first to amplify the signal in order to avoid its corruption due to noise and secondly to attenuate the huge EMG interferences avoiding the amplifier saturation. The signal is then digitalized by a 10 bit resolution, third order, single loop, delta sigma modulator. The resulting 1 bit data stream is finally sent to the decimator and stored in the pc for further processing. First simulation results show a good agreement between the two models, and the capability of the system to record without corruption signals in the order of magnitude of few microvolts.

The system level implementation of a Read out circuit for ion channel current detection is discussed in the fourth chapter. This part of the work has been carried on during my permanence at the "Institut fuer Mikrosystemtechnik" of the "Albert Ludwigs Universitaet " in Freiburg im Breisgau, under the supervision of Prof. Yannis Manoli and Dr. Matthias Keller. The generation of electrical signals in biological cells, such as neural spikes, is possible thanks to ions that move across the cell membrane. In many applications it is important, not only to record the spikes, but also to measure these small currents (their range varies from pA to μA) in order to understand which electro-chemical processes are involved in the signal generation and to have a direct measurement of the ion channels involved in the reaction. Ion currents, in fact, play a key role in several physiological processes, in neural signal generation, but also in the maintenance of heartbeat and in

muscle contraction. The traditional method used to measure these currents is called patch clamp and consists in fixing the external membrane potential to a control voltage and in recording the current that flows across the membrane using proper electronic devices. For this purpose, a current feedback delta sigma modulator has been developed in a high level behavioral model (verilogAMS in cadence environment).

Chapter 1

Neural-machine interfaces

At a first glance the biological world seems to be far away by the modern electronic equipments that surround our lives. A more detailed analysis can reveal how this impression is false and that the signals used by the cells to communicate with each other are electrical currents and voltages, exactly how it happens in electronics. This fact makes it possible, on one side, to read the biological signals flowing into the body and, on the other side, to apply electrical signals to the cells from the external in order to stimulate them restoring lost functionalities. It should be clear that the implementation of such interfaces has an enormous potential in the field of biomedicine and on the fight against a wide range of diseases. That is the reason why nowadays bioelectronics and human-machine interfaces are widely propelled and are subjected to a great deal of attention by scientists.

In this chapter a brief summary on biological cells and on the characteristics of electrical signals generated inside them is presented. A special attention is payed to neural cells and to the way in which neural signals are generated. The state of art concerning low noise electronic devices used to read such signals is finally discussed.

1.1 Motivation and Project Description

The work described in this thesis is part of two wider projects, called Safe-Hand ad OpenHand, funded within the PRIN initiative of Italian Ministry of Education, University and Research (MIUR), aimed at realizing a neurally-controlled prosthetic hand able to provide appropriate, graded and distally referred tactile and proprioceptive sensations to the wearer. In this way, the artificial hand would be intuitively controlled and felt by the amputee as the natural one.

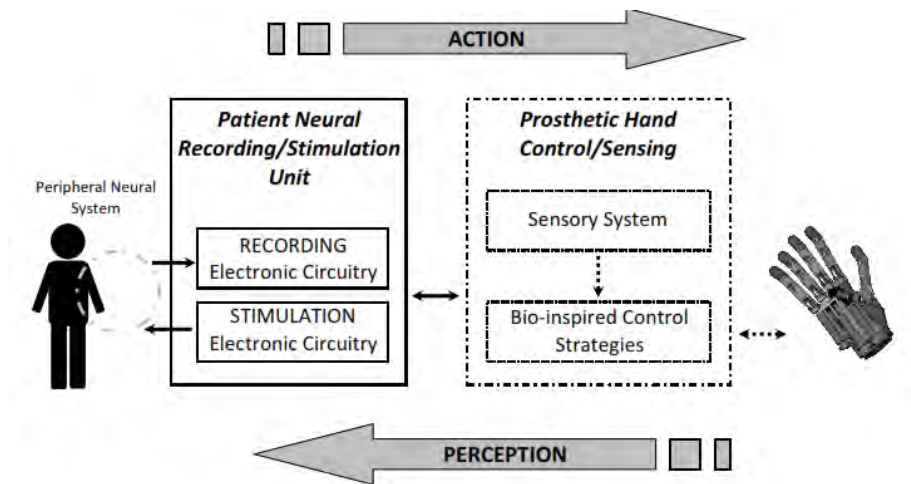


Figure 1.1: Safehand - Openhand project

To reach this aim, the platform shown in Fig. 1.1 was conceived. It consists of a recording and stimulation electronic system, a bio-mechatronic prosthetic hand and a bio-inspired control system (developed at ARTS Lab, Scuola Superiore Sant'Anna, Pisa, Italy and at Università Campus Biomedico, Rome, Italy). In such framework, special attention has been paid to the implementation of the electronic unit for conditioning the efferent bio-signals and generating the afferent signals in order to reach the final goal of the clinical evaluation of the platform on selected patients. This approach has several advantages with respect to commercially available solutions based on EMG signals, because the possibility to control the prosthesis with the thought clearly allows the patient to feel more conformable with the artificial limb. Nevertheless, also in the neural prosthetics there are several possible approaches, the one pursued in these projects takes advantage by signals acquired by means of intraneural electrodes, thus allowing a stronger signal detection compared with extraneural recordings and a better selectivity, since the electrode insertion inside the nerve permits to discriminate among the single nerve fascicles within the nerve.

1.2 Neural system

The neural system can be described as the infrastructure that allows the communication among the different parts of the body. It is divided into two main parts: the *Central Neural System (CNS)*, composed by the brain and the spinal cord, and the *Peripheral Neural System (PNS)* whose function is

to bring the signals elaborated in the CNS towards the rest of the body and viceversa. Due to the final aim of this thesis, the focus will be put overall on the PNS. It is composed by nerves fascicles, depending on the direction of the signal, the nerves are called motor nerves (the signal flows from the brain to the periphery), or sensor nerves (the signals acquired by the environment and transduced into electrical signals are forwarded to the brain). Afferent and efferent signals can also be transmitted on the same nerve, but in different cells.

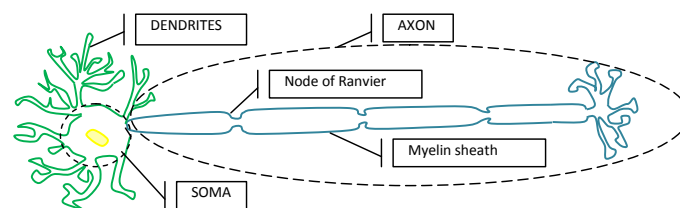


Figure 1.2: Neuron parts: Soma, Dendrites and Axon

1.2.1 Neural cells

The cells that make up the neural system are divided in two classes: the neurons and the glial cells that give them structural support. A typical neuron of a peripheral nerve is shown in Fig. 1.2, it is composed by three main parts:

- *soma*: is the body cell and contains the nucleus.
- *dendrites*: are very thin branches that carry the signal from a connection with another neuron (synapsis) to the soma.
- *axon*: is the part that transports the signal from the soma to the next cell.

A neuron can have a lot of dendrites but only one axon that, in humans can reach lengths up to $1m$. Axons play a key role in nerve signal propagation, the conduction is facilitated by the *Myelin sheath*, a special sheath that surrounds the neuron and shields the signal preventing its scattering outside the nerve. Moreover special interruptions of the sheath *Nodes of Ranvier* in which there is a concentration of Sodium-Potassium channels (see next paragraph) allow for a faster propagation called saltatory conduction.

1.2.2 Neural signal generation in biological cells

In Fig. 1.3 the shape of a classical neural spike is depicted, the changes of the voltage potential can be explained looking at the membrane cell configuration. In fact, the signal propagation across the nerve is possible thanks to the ion currents that flow across the cell membrane.

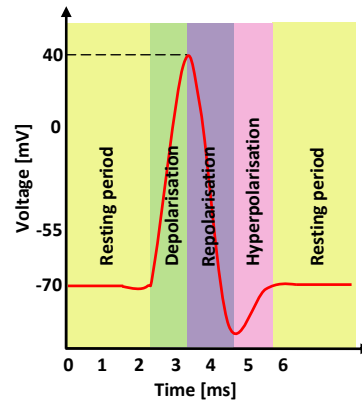


Figure 1.3: Action potential voltage spike

Inside the cell there is a major concentration of potassium ions (K^+) while outside the Sodium (Na^+) concentration is prevalent. In resting conditions the internal side of the membrane is more negative than the external creating a resting potential of $-70mV$ (Fig. 1.4). When an over-threshold voltage stimulus (the threshold is around $-55mV$) is applied to the membrane the Sodium channels open, allowing the Sodium ions to enter inside the cell (Fig. 1.5), this causes the inside to become more positive than the outside increasing the membrane voltage up to $40mV$ (depolarisation phase), due to this change of polarity the potassium channels open and ions flow out of the cell (Fig. 1.6), by this way a negative potential is restored inside the cell (repolarisation phase). The Potassium channels are slower than the Sodium ones, for this reason the number of Potassium ions flowing from the inner to the outside is higher than that of Sodium ions flowing in the opposite direction, as a result a hyperpolarization phase occurs. To restore the resting potential the Sodium-Potassium pump is needed, by this way potassium ions are brought back to the inside and Sodium ions pushed out of the cell (Fig. 1.7). During this time interval, called refractory period, the action potential propagation is blocked. Note that the Sodium-Potassium pump is an active process because it moves ions against their gradients, so it requires energy to work that is provided by a coenzyme called *Adenosine triphosphate (ATP)*.

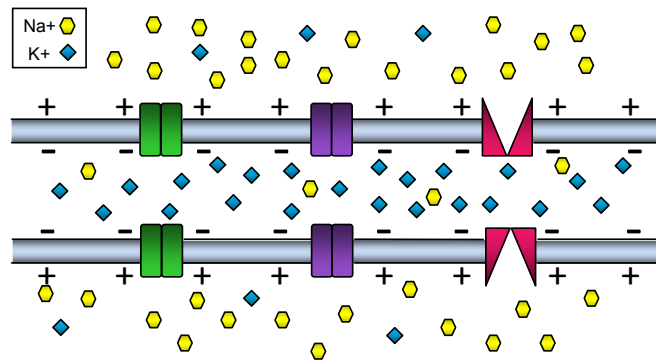


Figure 1.4: Ion cells concentration in resting conditions

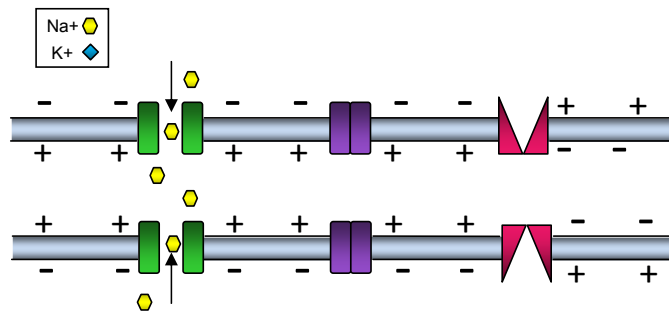


Figure 1.5: Cell membrane during depolarisation phase

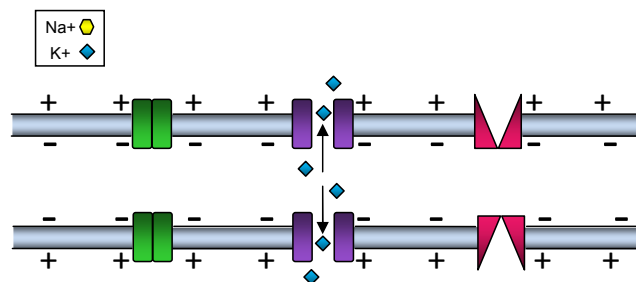


Figure 1.6: Cell membrane during repolarisation phase

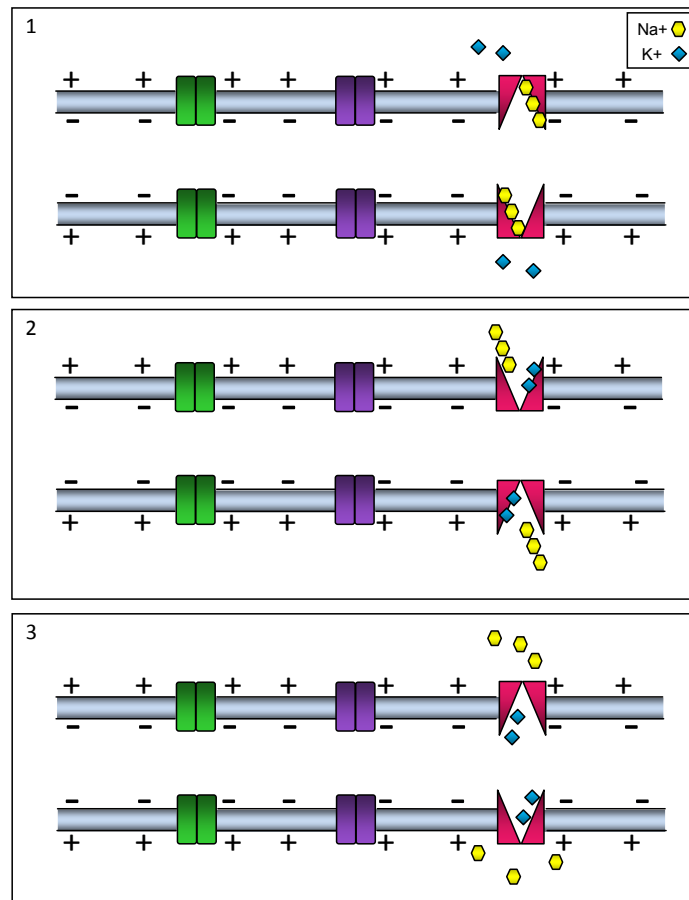


Figure 1.7: Cell membrane during hyperpolarisation phase

1.2.3 Nerve structure

Peripheral nerves consist of bundles of nerve fibers. Each group is surrounded and protected by a thick layer of dense connective tissue, called epineurium, which endures most of the mechanical tension applied to the nerve. The connective tissue layer wrapping the individual bundles, called perineurium, bears the elongation load. While the space between individual nerves fibers is filled by a delicate layer of loose connective tissue, the endoneurium. A schematic sketch of the nerve structure is shown in Fig. 1.8.

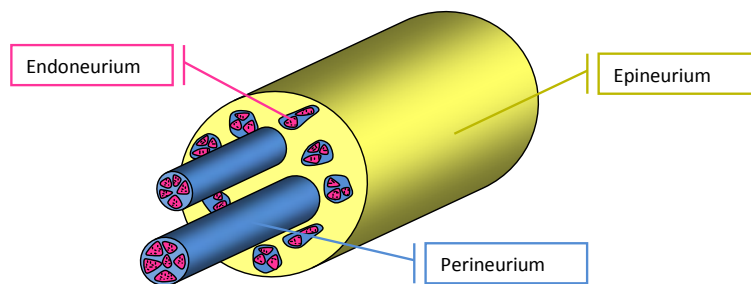


Figure 1.8: Peripheral nerve structure

1.3 Implantable nerve electrodes

In amputees and in patients with neural diseases, the biological structure described in 1.2 needs some help to communicate with the external. The electrodes represent the link between the biological tissues and sensing electronics. It is desirable to develop the communication in both directions. On one hand the device must allow to record neural signals, on the other hand to send stimulating signals from the external to the nervous system. Major properties for electrodes are selectivity and non-invasivity.

Selectivity plays a key role because of the nerve bundle structure. In the inner part of the nerve, there are several fascicles and each fascicle contains different axons, therefore the electrode must be able to isolate a single neural signal from the other electrical activities around it. In this way, with electrodes placed close to neural fibers, it becomes possible to record a stronger signal, improving Signal to Noise Ratio (SNR). From the patient point of view, it is suitable to minimize invasivity. These two requirements are clearly in contrast. In fact, if the aim is to have a high selectivity, than it is necessary to increase invasivity inserting the electrode into the body (non superficial electrode) or even within the nerve (intranural electrode). In these years several categories of electrodes have been developed, they can be divided in

two categories: extraneural (i.e cuffs) which are less selective but also less invasive, and intraneural (longitudinal, penetrative and regenerative) which are preferred for their better selectivity but imply a higher invasivity. A brief summary on the main electrode types is presented in the following.

1.3.1 Cuff electrodes

Among extra-neural electrodes the more used are cuff electrodes. As depicted in Fig. 1.9, they are a cylindrical wrapping that envelops the nerve from the outside.

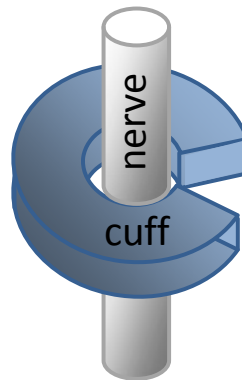


Figure 1.9: Cuff electrode

Electrical contacts are placed in the inside, in this way the recorded signal is as strong as possible. There are two main sorts of cuffs: split-cylinder and spiral cuff. The first ones have the shape of a semi-open cylinder and must be closed around the nerve with suture, this makes them uneasy to implant. It would be also suitable to have an electrode with an adaptable diameter; a too large section will produce a neural signal too weak whereas a device too tight may cause nerve diseases. In order to overcome these problems spiral cuffs have been introduced. They are fabricated with a stretch sheet that allows the electrodes to follow the nerve shape [1]. The advantage of cuffs compared to the others extraneural electrodes is the precision with which they can be placed around the nerve. The placement of the contact in the inside of the cylinder means that stimulation can occur with lower current than those used in other extraneural electrodes. The main drawback of extraneural electrodes is their low selectivity. In fact, being wrapped around the nerve, they record the whole electrical activity of the nerve which is the sum of all axonal signals. Moreover, in order to reach afferent axons from outside, they must provide

high stimulation currents with respect to the intraneural ones. For these reasons electrodes able to penetrate the nerve have been introduced.

1.3.2 Longitudinal electrodes

Longitudinal electrodes get the name from their insertion way and are often indicated as LIFE (Longitudinal Intra-Fascicular Electrodes). In fact they are implanted throughout perinervium and placed, parallel to the axe of nerve, inside the nervous fascicles. They host multi-active sites composed of a thin conductor wire made of Platinum-Iridium or fabricated with metalized Kevlar fibers, covered with an insulating sheath. Multi-channel structures allow understanding better the signal propagation along the nerve. LIFE's drawbacks regard their radial symmetry [2], since the fixed distance between electrode and nerve limits selectivity. Moreover the electrode stiffness causes micro-movements that, in the long term, may damage the nerve.

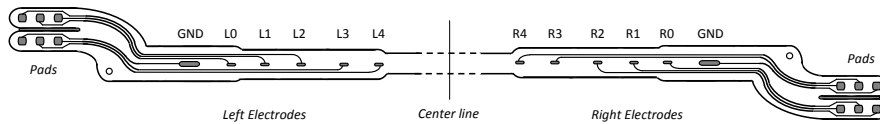


Figure 1.10: tfLIFE electrode

The thin film Longitudinal Intra-Fascicular Electrode is an evolution of LIFE that overcomes these problems. It is composed of a double sided structure with contacts dislocated in different parts of the electrode. Its flexible structure allows a better adaptation to the nerve shape preventing all damages due to an excessive stiffness. The need for electrodes able to move within the nerve, approximating the electrical contacts to nervous fibers, have brought to a new generation of tfLIFE's based on Shape Memory Alloy (SMA) materials. A serpentine shape can be memorized in the SMA, placing electrical contacts in the crests of serpentine. In this way, when the electrode reaches a determined temperature, its shape can be modified and active sites moved closer to the axon [3]. An interesting application of tfLIFE's is in neural prosthesis development.

1.3.3 Penetrative electrodes

Penetrative electrodes are constituted of an array of needles attached to a rigid support (Fig. 1.11). In their simplest configuration they are called shaft

electrodes and they are composed of only one needle. Structures with many electrodes are called MEA (Multi Electrode Array), a widely used version of MEAs has been developed at Utah University and it is called UEA (Utah Electrode Array) [4].

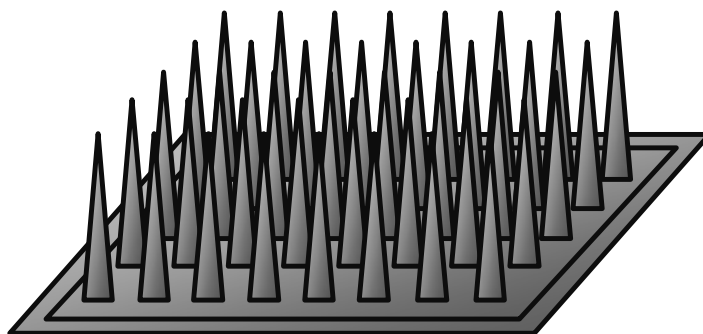


Figure 1.11: MEA electrode

Penetrative electrodes were used primarily in the CNS, but there are also applications related to PNS although their stiffness and their difficult implantation does not make them particularly suitable for this purpose. When the electrode is used in CNS, needle can penetrate through the skin in the skull reaching cerebral neurons. In the PNS, needles penetrate within nervous fascicles, implantation is facilitated by pneumatic insertion techniques that, increasing insertion velocity, allow preserving nerve integrity [5]. Recent studies show that a valid alternative, that can guarantee a better mechanical stability and a high biocompatibility, is in implementing MEAs with carbon nanotubes. Tests demonstrate that impedance in this electrode is one to two orders of magnitude smaller than that measured using traditional MEAs, thus significantly improving the performance of neural electrode [6]. Electrodes array have been used in numerous applications, implanted within acoustic nerve for auditory function restoring [7] and in the skull for recording brain signals in animals and also implanted in humans for robotic limb control [8].

1.3.4 Regenerative electrodes

The last electrode that will be analyzed is regenerative electrode or sieve electrode. These electrodes are inserted in the nerve transversally and are shaped as a grid that can be either circular or square, a schematic example is shown in Fig. 1.12.

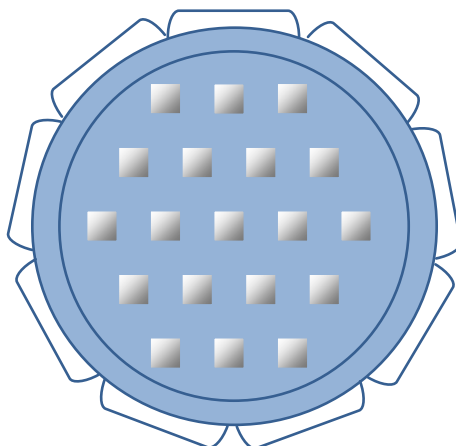


Figure 1.12: Sieve electrode

Neural fibers may regenerate through the holes of the grid hence the name of regenerative electrode. Active sites are situated around the holes, thus they can reach single axons, making them the more selective among all electrodes presented. A crucial issue in sieve electrodes fabrication is the number and the dimension of vias. Different studies demonstrate that too small vias can inhibit neural tissue regeneration. On the other hand increasing diameter, the distance between vias increases leading to an excessive deflection of neural fibers with a consequently difficulty in neural tissue regeneration. A good compromise seems to be the fabrication of electrodes with a diameter range from $45\mu m$ to $60\mu m$ [9]. In the case of prosthesis control, it is useful to divide electrode in reference areas contacting different vias with the same electrical contact, to record specific neural patterns [10]. The implementation of multi-via electrodes (some sieves contain 800 vias) is facilitated by the introduction of polyamide electrodes. This material is more flexible than silicon and allows to reduce risk of nerve diseases during implantation. Moreover the high biocompatibility degree of polyamide permits longer time implantation than that of silicon [11]. The main advantages of sieve electrodes are their high selectivity and the stability of the electrode-tissue interface once that the neural tissue regeneration has occurred. Drawbacks are their high invasivity and the fact that neural signal cannot be recorded until regeneration is completed and this process takes at least 12 weeks. The high invasivity of sieves has not yet allowed their implantation on humans, however encouraging experiments have been carried out on frogs, rats and fishes [9].

1.4 Implementation issues

The neural signals weakness makes their recording a critical operation and requires special care in terms of low noise and low power design. On the other hand, the stimulation circuitry must provide current pulses whose amplitude, duration and frequency evoke the programmed stimulus without damaging the tissues (in muscles, for instance, a heating corresponding to only $80mW/cm^2$ can cause necrosis [12]). As it can be easily understood, there are several issues to take into consideration during the design, in this section a brief discussion on the main problems related to neural-machine interfaces is presented.

1.4.1 Neural recording issues

As displayed in Fig. 1.3, the neural spikes measured in the cell membrane have an amplitude of $70mV$, the surrounding layers shield the signal, and this causes a radial drop of its amplitude. Nevertheless, the signal can still be detected, but its weakness makes it necessary to introduce in the read-out circuit special techniques for low noise design. Amplitudes outside the epineurium can be lowered down to $1\mu V$ [13], while typical amplitudes for intraneural signals range from tens to hundreds of microvolts [14, 15]. Neural spikes bandwidth lies in the frequencies from $500Hz$ to $10kHz$ with a peak around $2kHz$ and it partially overlaps with the *Electromyographic signals (EMG)* which have amplitudes several order of magnitude higher than that of neural signals. EMG interferences are, for this reason, the most serious interferences to cope with. Fortunately the spectral signature of EMG decreases with frequency and, at $800Hz$ has an energy lower than that of neural signals [13, 16]. Using a proper filter stage in the front-end circuit, it is then possible to isolate the neural signals and to prevent the EMG to mask them completely.

In addition to the biological interferences, also the noise due to the electronic devices must be considered. The main noise contributions are flicker noise and thermal noise. Flicker noise is inversely proportional to the frequency (it is also called $1/f$ noise), and plays a key role in low frequency applications. In a MOS transistor it can be modeled as a voltage source in series with the MOS gate given by 1.1, where K_f is a constant depending on process parameters:

$$\overline{V_{n,flicker}^2} = \frac{k_f}{WLC_{ox}} \cdot \frac{1}{f} \quad (1.1)$$

Equation 1.1 shows that flicker noise is reduced if wide area transistors are

used. Physical causes of Flicker noise are not well known, the phenomena has been explained with charge fluctuation at oxide-semiconductor interface due to presence of traps. As the p-conduction occurs in depth while n-conduction is superficial, very close to the interface with the oxide, PMOS devices exhibit less flicker noise than NMOS ones. The thermal noise expression is given by equation 1.2, where γ represents the channel length modulation effect.

$$\overline{V_{n,th}^2} = \frac{4KT\gamma}{g_m} \Delta f \quad (1.2)$$

The noise is reduced when g_m increases [17]. In terms of MOS size, this means that a large and short channel MOS minimizes thermal noise. A useful parameter for the evaluation of flicker noise incidence with respect to thermal noise is the corner frequency. It is the frequency at which flicker noise and thermal noise give the same contribute to the circuit. It can be calculated equating 1.1 and 1.2, obtaining 1.3.

$$f_{corner} = \frac{K_f}{WLC_{ox}} \frac{3}{8KT} g_m \quad (1.3)$$

Input Referred Noise (IRN) is the most widely used parameter to estimate the effect of noise in a circuit. It resumes all noise sources into a single voltage noise source, placed at the input of the amplifier. By this way it is immediate to understand how much noise is degrading the input signal. A key role in neural signal acquisition is also played by low powering. Since the tendency is to acquire more signals simultaneously, the use of more amplifiers is required, causing the power reduction available for each of them. Unfortunately low-noise and low-power designs are in contrast since power scales as $1/(\overline{V_{noise}})^2$ [18]. For this reason, the major effort of researchers is to find a good compromise between these two crucial issues. Noise Efficiency Factor (NEF) is an indicator used to compare the power-noise performances of different amplifiers. It has been introduced in [19] and describes how many times the noise of a system, with the same current drain and bandwidth, is higher compared to the ideal case. Its value is given by 1.4.

$$NEF = V_{rms,in} \sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot U_t \cdot 4kT \cdot BW}} \quad (1.4)$$

The minimum value for NEF is reached by an amplifier with a single bipolar transistor, in this case without considering flicker noise, $NEF = 1$. Basically all practical circuits have higher values [14]. Amplifiers with lower NEF can achieve the same IRN with lower power dissipation [20].

1.4.2 Neural stimulation issues

The ability to supervise the effects of stimulating neural tissue is essential in neuroscience research since it allows to study the function of the nervous system. In particular, the ability to provide a controlled application of electrical signal to specific afferent nerves (Functional Electrical Stimulation or FES), enables to restore and to enhance neural functions in people with nervous system dysfunctions. Examples of useful stimulation applications include clinical treatment of epilepsy, tremors associated with Parkinson's disease, retinal and cochlear implants and multiple sclerosis [21–24]. The stimulation system must be capable of generating a wide range of electrical signals for nerve stimulation via implantable nerve electrodes. From an electrochemical point of view when the stimulation signal is provided, a charge transfer between the electrons in the metal electrode and the ions in the biological tissue is created. The ionic flow can be induced by two primary mechanisms, the capacitive and the Faradaic reaction. In the first one no electron transfer occurs, just a redistribution of charged chemical species in the tissue. While during the second mechanism, an exchange of electrons across the electrode-tissue interface is involved, resulting in reduction or oxidation of some chemical species. A Faradaic process can be classified as reversible or irreversible depending on the rate of electrons transfer at the interface. A reversible Faradaic reaction is characterized by fast kinetics, this allows to achieve large currents with small potential excursions away from equilibrium. Moreover, since the reaction takes place near the electrode surface, by passing a current in the opposite direction it can be reversed back into its initial form. Instead in a irreversible reaction, slow electron transfer kinetics produce the diffusion to the surface of new chemical species, that can alter the chemical composition of the tissue, generating the beginning of corrosion or oxidation. Then, in order to prevent toxic reaction and tissue or electrode damages, in a neural stimulation system only reversible Faradaic processes can be used for charge injection. Regarding safety during electrical stimulation, several analysis and models have been presented in literature. Some studies focus on electrode material and geometric area [25, 26], using as selection criteria the reversible charge injection limit of the material. Such quantity depends on the reversible processes that are available over the duration of the stimulus, as well as the stimulus waveform shape and frequency [27, 28]. Considering the methods of controlling charge injection, two categories are available: current-controlled and voltage-controlled. Several works consider the current-controlled method the most effective because the effects of such stimulation take place near the electrode and can be directly calculated and easily understood [26, 29]. Current pulses allow to eliminate variations in the stimulation

threshold even with changes in the electrode-tissue impedance and are commonly used for functional electrical stimulation of excitable tissue. However many researchers prefer voltage stimulation in terms of electrode safety. In fact, current pulses can cause high electrode voltages with a following electrochemical damage of the electrode [30]. Choice of stimulus parameters is then very important in the design of neural stimulation circuitry and depends on the type of stimuli to generate. Charge-injection for neural stimulation is usually applied in the form of rectangular pulses but in the recent years different waveform types have been explored. The results obtained in [31] and [32], suggest that Gaussian waveforms, compared to rectangular stimulus, reduce the non-uniformity of the current density distributions on the electrode surface while maintaining stimulation efficacy and requiring the smallest electrode surface area.

1.5 State of art

Neural signals can be considered both in terms of voltages and currents. In fact, as explained in Section 1.2.2, voltage spikes are generated by means of ion channel currents. According to what reported in literature, in this thesis the main focus is on the neural voltage recording. Nevertheless an analysis and a high implementation of a front-end circuit for ion channel current detection is also presented. For these reasons in this section the state of art related to both type of measures is presented, the voltage signal acquisition and the ion current readout circuits. An overview on literature related to neural stimulation is also provided.

1.5.1 Neural recording and stimulation systems

In last decades great advancements have been reached in biomedicine, in particular as described in Section 1.3 the introduction of intraneural electrodes has made it possible to work with stronger signals. Nevertheless, amplitudes remain in the order of magnitude of tens of microvolts, therefore the noise is still the major concern. A low noise front-end stage is then mandatory to prevent the signal destruction. Many researchers are currently working on low noise neural interfaces, aimed to different applications. This kind of devices indeed can be very useful for many purposes: to find a solution against neural-degenerative diseases like Parkinson and Alzheimer for instance, as well as for injured patients with permanent damages to the spinal cord and, as in the work presented in this thesis, to restore lost functionalities in amputees thanks to neuroprosthesis. According to the pursued goal, different

specifications drive the neural interface design. In the recording systems related to CNS, for example, also neural signals different from action potentials can be useful (*Local Field Potential (LFP)* for instance). Their amplitudes are in the order of magnitude of mV and their frequency overlaps with EMG interferences [33–35]. The recording is still possible because EMG, in CNS recordings, are not of a such importance, due to the fact that there are no muscles moving into the brain. For this kind of applications the bandwidth includes also very low frequencies (in the $mHz - 100Hz$ range) [7, 14, 36, 37]. The neural signal weakness together with the strong interferences drive the designers to develop solutions capable to filter and amplify the signal as close as possible to the electrode, the miniaturization and optimization of electronics for neural activity stimulation and registration seems to be then, the new challenge. Attempts to solve this issue are based on two different approaches: the use COTS electronics or the realization of a custom IC. The first approach is utterly useful for a preliminary analysis because it is a low-cost solution and has a rapid implementation time so it is suitable for short-term experiments, especially on animals. Moreover, since neural signal characteristics in terms of bandwidth and stimulation pulse amplitudes are patient and electrode dependent, the possibility to easily modify the electronic configuration represents a great advantage in the first stages of research. The IC approach, on the contrary, allows the realization of low noise and compact devices, combining low power consumption and small sizes [14, 38, 39] and is, therefore, more suitable for long-term implantation. Nevertheless, design time and prototyping costs are large and the custom device usually lacks flexibility and adaptability. To sum up all the typical approach is to start with a COTS device and, only once that the terms of the problem are better known, a custom integrated circuit can be developed on a solid ground.

Several works aimed at the realization of neural interfaces with discrete components have been presented, but many of them include only the recording module [40–43]. On the other hand, papers including the stimulation circuitry use a simple recording unit with low order filters and single-ended signal paths [34, 37, 44–46]. Moreover, such discrete component systems are focused on the study of the Central Nervous System (CNS). For what concerns the integrated circuit approach, many papers have been presented but the majority is still aimed to process cortical neural signals [14, 33, 35, 39, 47–51]. Several integrated circuits for PNS have also been developed [13, 38, 52–54], but in most cases they do not include the stimulation unit and are focused on cuff electrodes. The IC circuits have the great advantage on their discrete system counterpart, to allow the designer to have the complete control on all the system parameters, by this way it is possible to find a better fitting between the specifications and the prototype. The drawback is obviously a

major project complexity due to the enormous degree of freedom that must be handled by the designer. In the following a survey on literature regarding the amplifier, the filter, the Analog to Digital Converters (ADC) and the stimulator used in neural signal interfaces is presented.

Amplifiers

One of the key points concerning the recording module is to realize a low noise amplifier. Different choices have been made in this direction but the most pursued one has been to use a Symmetrical OTA topology of Fig.1.13. Thanks to its simple circuitry, in fact, it guarantees the minimum IRN comparing with other topologies as Folded Cascade and Miller OTA. Many papers present such solution for neural implementation in its single ended [7, 14, 55, 56] or fully differential versions [36].

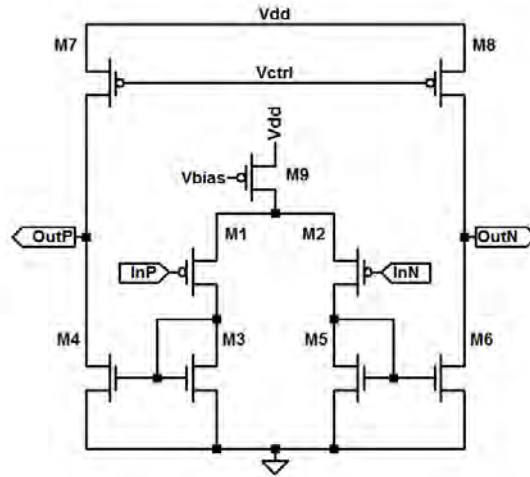


Figure 1.13: Simmetrical OTA in Fully differential configuration

Using Symmetrical OTA architecture, thermal noise is given by equation 1.5.

$$\overline{V_{n,th}^2} = \left[\frac{16kT}{3g_{m1}} \left(1 + 2\frac{g_{m5}}{g_{m1}} + \frac{g_{m8}}{g_{m1}} \right) \right] \quad (1.5)$$

Where g_{m1} is the transconductance of the input differential pair, while g_{m5} and g_{m8} are the transconductances of the transistors in the output branch. In order to reduce noise, a designer must have special care in MOS sizing.

Equation 1.5 shows that thermal noise minimization requires $g_{m1} \gg g_{m5}, g_{m8}$. Since the g_m expression for a MOS in saturation region is given by

equation 1.6, a low noise amplifier can be achieved by using large and short differential pair and narrow and long mirror transistors.

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L}} \quad (1.6)$$

The consequence in choosing large transistor for input differential pair is that the device enters in weak inversion region. In such region g_m is maximized and becomes independent from MOS size, depending only upon drain current. Thus, once that the differential pair MOS is in weak inversion, the only way to further increase the transconductance is to increase the current with a consequent increase of power. Taking everything into account, the majority of papers choose to maximize g_{m1} by using a large input differential pair in weak inversion without increasing current, and to minimize g_{m5} and g_{m8} by putting M5 and M8 in strong inversion [57–60]. This approach is not used only in Symmetrical OTA configuration but also in Folded Cascade [18, 61] and Miller OTA [52]. Such choice has advantages in terms of flicker noise reduction. As already shown in equation 1.1, this noise is in fact reduced when MOS dimensions are increased. Almost all researchers prefer a PMOS differential pair to NMOS for its lower sensitivity to flicker noise. Nevertheless, analysis carried out in [62] shows as such assumption is true only comparing NMOS and PMOS with the same g_m . The noise reduction, in this case, derives from a larger implementation area of PMOS transistors. Considering the same biasing and area it is demonstrated that a NMOS amplifier presents higher g_m than a PMOS one and then a better figure noise. Another approach that has positive effects on noise is the use of a fully differential topology. Having two branches, in which the signal is mirrored and propagated, is an advantage in terms of common mode noise. Such noise spreads in the same way along the two differential paths of the circuit and is canceled taking the difference of the two output voltages. These benefits are paid with a large occupation area due to the duplication of feedback networks of the filters and to the introduction of common-mode feedback (CMFB) blocks. Although the use of fully differential architectures would be desirable, only few papers adopt this strategy [53, 60, 61, 63]. Even if symmetrical OTA is the most widely used configuration, other topologies have been exploited. The modified folded cascade proposed in [18] allows to obtain a NEF of 2.67 which is one of the lower values reported today. This result is achieved reducing power by means of current reduction in folded branches (1/16 with respect to input branches) that may imply worse noise performance. This drawback is avoided using degenerating resistors in series with M5 and M6. An appropriate choice of these resistances may significantly reduce the contributions to total noise. First because thermal noise in resistors can be

significantly lower than in MOS and second because the resistance gives no contribution to flicker noise. A folded cascade topology has been used by [64] that, taking advantage by the current-splitting technique, reaches a NEF of 3.09 with an $IRN = 3.07\mu V_{rms}$. Among the other topologies exploited in neural amplifiers, Wang et al., in [52], propose a preamplifier stage based on Miller OTA configuration. The circuit gives a gain of 20 dB and it is followed by an instrumentation amplifier that brings the gain to 80 dB. Sacristan and Osés [65] present instead a multi-stage architecture. In the design of the first stage, represented by a simple preamplifier, authors have paid particular attention in noise reduction and CMRR, using large area transistors and high biases current. The second stage takes advantage by a DDA (Difference Differential Amplifiers), composed by two pairs of differential inputs. Inputs are applied to the first pair while in the second two, feedback loops are implemented. One feedback loop imposes the gain, while the other introduces zero and poles for filter implementation. The third stage consists of a simple RC high pass filter followed by a fixed gain amplifier, needed to adjust the gain to the level required by the ADC. This circuit solution allows to achieve particularly low noise levels ($0.35\mu V$ in the bandwidth of $100Hz - 5kHz$), at the cost of a high power consumption ($2mW$). In [53], a different solution employing an instrumentation amplifier has been proposed. In order to reduce the noise, a fully differential approach is used and the input stage is constituted by a PMOS differential pair with large area. Despite that, the noise at $1kHz$ is about $0.73\mu V/\sqrt{Hz}$. Integrated in the neural useful band ($250Hz - 5kHz$) an IRN value of $50\mu V$ is obtained, still too high if compared with the weak amplitude of neural signals.

Filters

Several approaches in neural filter design have been implemented. The major degree of freedom in filter design is the choice of the filter type. In integrated systems, filter strategies can be classified in Continuous Time Filters (R-C or MOSFET-C and Gm-C) and Discrete Time Filters (Switched-Capacitor) [66, 67]. The most used are MOSFET-C filters for their ability to reach very low cut-off frequencies useful for LFP recording [14, 18] as well as for *Fast Ripples (FR)* detection in epileptic patients [64]. Since the cut-off frequency is given by the inverse of the product of the MOSFET equivalent resistance and the capacitance, a very low value can be obtained using a high capacitor or a high resistance. But as both solutions imply large area implementation, a widely used approach is to employ a MOSFET biased in triode region that emulates a resistive behavior. By this way, the relationship between drain current and the drain-source voltage is linear, as expected

from a resistor. This particular application requires large values of resistance (to achieve a mHz cut-off frequency with a capacitor in the pF range, it is necessary an equivalent resistance in the order of hundreds of $G\Omega$). For this reason, bipolar transistors compatible with CMOS process are used [68]. This technique allows achieving resistances of several hundreds of $G\Omega$. The discrete time approach is rarely used but it presents several advantages with respect to continuous time filters. In this case, cut-off frequency is set by the ratio of two capacitors. The ratio of parameters of the same kind of device is more precise than the ratio of a transconductance and a capacitor (Gm-C filters) since it is affected by statistical fluctuations of the same manufacturing process. Moreover, Switched Capacitor filters allow an effective use of silicon area, making possible to realize low cut-off frequencies with small areas. A great advantage is also given by the flexibility due to the dependence of the filter parameters on the clock frequency. In [53] a six order band-pass filter is proposed. The architecture consists in three fully differential biquad stages, in which the filter signal flow is based on ladder-type implementation. Gusmeroli et al., in [69] use a first order switched capacitor high pass cell, changing the high pass cut-off frequency in order to reduce the recovery time during stimulation. Through switching capacitor technique, it is sufficient to increase the clock frequency to achieve a time recovery reduction. In the solution proposed in [70] the switching capacitor stages are preceded by a continuous time filter in order to avoid aliasing and to prevent input corruption due to switching noise. Regarding the heavy incidence of flicker noise in neural signal acquisition, some researchers [57, 71] have overcome this problem introducing a chopper stabilization technique. The working principle is to modulate input signal in order to translate it into high frequency where the flicker noise effect becomes irrelevant. The modulated signal is band-pass filtered and then demodulated in the baseband. Uranga et al. in [61] propose a signal chain composed by a modulator followed by a pre-amplifier stage and by a band-pass filter centered at chopping frequency. The pass-band removes the undesirable spikes introduced in chopping process due to non-idealities of switches. A post amplifier stage has been introduced after the band-pass, then a demodulator folds the signal into base band and finally a low pass filter isolates the neural signal from noise. Both band-pass and low-pass continuous time filters have been designed using the Gm-C technique. The advantage of this approach is that the noise can be reduced simply increasing the chopper frequency. On the other hand, this implies an increase of the amplifier cut-off frequency that must be higher than the clock frequency, in order to avoid any harmonic distortion of the modulated signal. Gosselin et al. [63] present a multi-channel structure composed by a front-end stage and a mixed-signal compression module that uses an analog wavelet transform

process followed by an ADC. The front-end stage is present for each acquisition channel while the wavelet signal processing block is shared among all channels. The front-end stage is based on Chopper Stabilization technique. After modulation, the signal is amplified with a rail-to-rail CMOS amplifier and filtered with a second order Gm-C stage. The signal is then demodulated into the baseband while the equivalent noise is added to the amplifier input after that the modulation process has occurred. Thus, noise is subject only to one modulation process (the same used for signal demodulation) that translates the noise out of the band of interest. Another technique, called autozeroing, has been exploited in order to reduce low-frequency noise and offset at the amplifier input. Between Chopper Stabilization and autozeroing there is a clear distinction: while the first is a modulation technique, the latter is a sampling technique. The basic idea of autozeroing is to sample the offset voltage value and the noise and to hold them in a capacitor. Once that these values have been stored, the input is put into the amplifier and the unwanted quantities can be subtracted from the instantaneous input. With the offset voltage this process works well since offset is constant, the problem is a bit more complex considering time-varying and random flicker noise. The efficiency of autozeroing strongly depends on the correlation between the noise sampled and held in the capacitor and the instantaneous noise value from which such sample is subtracted. It can be stated that this process reduces also the flicker noise because the autocorrelation between two consecutive samples of flicker noise decreases slowly enough to allow the cancellation when the subtraction occurs. The main drawback of this approach is the aliasing. Since this is a sampling technique, the aliasing noise is folded into the base band [72]. Chan et al. [60] propose a neural amplifier based on autozeroing technique: the design consists of three stages. The first one is a variable gain amplifier composed by two differential pair, one for input recording and the other for offset-noise adjustment. The second stage is a low Gm-C high-pass filter and the third is a low-pass Gm-C amplifier. From the point of view of power consumption, autozeroing seems to give better performances than chopper. The modulation implies a wider amplifier bandwidth and to this aim, it is necessary to increase current and then power consumption. A summary on the main features of the neural recording system presented in literature has been reported in Tables 1.1 and 1.2. It should be clear that each system has his own characteristics, thus a mere comparison of the parameters can be unfair. For this reason in the last column the number of channel to which the parameters are referred has been reported.

Analog-to-digital conversion and spike sorting

Once the signal has been properly amplified and filtered, the last operation is digitalization. At this regard, two main approaches have been proposed. The first consists in a traditional digital conversion, where the neural signal morphology is held and transmitted to external for processing and classification. The second approach consists in spike detection; in this case the signal morphology is lost and the only information kept is about spike occurrences. The A/D conversion is exploited in several works. In [7, 53, 65], an 8 bit successive-approximation register (SAR) ADC has been used. This solution involves low power consumption and small layout area. Watkins et al. in [73] make use of a 10 bit SAR ADC but, since the signal is acquired from 100 different channels, it would be too onerous to convert all signals. The proposed solution converts only one channel, while for the others there is a spike detection block that recognizes if a spike has occurred or not. In this way there is a considerable reduction in bandwidth requirement for the external communication link. Horiuchi et al. [56] use the spike detection approach, but their circuit is more elaborate than a simple comparator and it is able to discern between peaks and troughs of spikes and gives also information about spikes amplitude. Another approach proposed is based on oversampling converters. Due to the low frequencies of the neural signals in fact, large OverSampling Ratio (OSR) can be achieved, without using high sampling frequencies. In [74] a first order sigma delta converter has been designed, reaching a 8 bit resolution with a 40 oversampling ratio over a $6.25kHz$ frequency. A second order sigma delta modulator that exploits a new superinverter amplifier has been proposed in [75] and allows to reach a 11 bit resolution considering a $8kHz$ bandwidth.

Stimulation circuitry

Stimulation circuit is present only in a few of the neural conditioning systems mentioned above. Basically, the stimuli are generated through a Digital to Analog Converter (DAC) while the stimulation parameters as frequency, duration and intensity are controlled by a digital unit or an external microcontroller (μC). In [53], a current-mode microstimulator for cuff electrodes has been implemented. It is made up of a thermometer DAC, which generates an output current from 0 to $1mA$ with 8 bits of resolution. The maximum value for the stimulation current has been chosen estimating a load resistance of $1k\Omega$. In [65] a 6 bit binary weighted DAC with a full-scale current of $128\mu A$ is used to generate stimulating currents. The architecture of such device assures a high flexibility and programmability, making it useful for dif-

ferent types of electrodes (as sieve, cuff, LIFE or microneedle) and for several stimuli shapes. A novel modification to the binary-weighted DAC has been presented in [76]. It is based on distributed multiple bias potential in transistors of same size. Relative currents are controlled by gate bias rather than by geometry, this significantly reduces the circuit area which scales linearly versus number of bits. Since the major disadvantage of DACs for implantable stimulators is the implementation area which grows exponentially with resolution, the multi-bias approach offers important benefits.

Ref.	Tech.	Band [Hz]	Gain [dB]	V_{DD} [V]	Area	Power	IRN	NEF	Ch.
[7]	CMOS 0.5 μ	5 – 7.2k	36	3	2.25mm ²	99 μ W	9 μ V	<i>n.a.</i>	64
[14]	CMOS 1.5 μ	25m – 7.2k	39.5	± 2.5	0.16mm ²	80 μ W	2.2 μ V	4	6
[18]	CMOS 0.5 μ	45 – 5.32k	40.8	2.8	0.16mm ²	7.56 μ W	3.06 μ V	2.67	1
[35]	CMOS 0.18 μ	16 – 5.3k	40	1.8	2.7mm ²	89 μ W	18.9 μ V	<i>n.a.</i>	8
[36]	SOI 0.18 μ	0.6m – 7.1k	39.5	1.5	0.004mm ²	6 μ W	3.07 μ V	2.8	1
[38]	CMOS 0.8 μ	310 – 3.3k	80	± 2.5	12mm ²	24mW	291nV	<i>n.a.</i>	10
[39]	BiCMOS 0.6 μ	<i>n.a.</i> – 5k	60	3.3	25.38mm ²	8mW	4.8 μ V	<i>n.a.</i>	100
[41]	COTS	445 – 6.6k	70 – 94	± 2	80.19cm ²	130mW	1 μ V	<i>n.a.</i>	16
[47]	CMOS 0.35 μ	(0.5 \div 50) – (500 \div 10k)	54 – 73	3	8.5mm ²	9.3mW	6.08 μ V	5.6	128
[48]	CMOS 0.35 μ	(30 \div 925) – (970 \div 18k)	54	± 1.5	6.25mm ²	<i>n.a.</i>	32 μ V	<i>n.a.</i>	16
[49]	CMOS 0.6 μ	0.5 – 15k	30 – 80	5	45.75mm ²	135m	2.4 μ V	<i>n.a.</i>	126
[53]	CMOS 0.35 μ	250 – 5k	80	3 – 4	4mm ²	2.25mW	0.73 μ V/ \sqrt{Hz}	<i>n.a.</i>	1
[54]	CMOS 1.5 μ	300 – 6k	40 – 60	± 1.5	41.84mm ²	1m	1.95 μ V	<i>n.a.</i>	1
[55]	CMOS 0.35 μ	10 – 10k	46 – 74	3.3	13.5mm ²	6mW	13 μ V	<i>n.a.</i>	256

Table 1.1: Main characteristics of neural recording system presented in literature

Ref.	Tech.	Band [Hz]	Gain [dB]	V_{DD} [V]	Area	Power	IRN	NEF	Ch.	
[56]	CMOS	1.5 μ	22 – 1.7k	42.5	1.5	81 μ m ²	0.8 μ W	20.6 μ V	n.a.	1
[57]	CMOS	1.5 μ	100 – 5k	38	5	1mm ²	28mW	1.13nV/ \sqrt{Hz}	n.a.	1
[59]	CMOS	0.5 μ	73 – 2.18k	70	\pm 2.5	0.33mm ²	180 μ W	2.76 μ V	n.a.	1
[60]	CMOS	0.18 μ	200 – 2k	55	1.8	0.245mm ²	26 μ W	4.24 μ V	14	1
[61]	CMOS	0.7 μ	n.a. – 3k	74	5	2.7mm ²	1.3mW	0.453 μ V	5.3	1
[63]	CMOS	0.18 μ	100 – 6k	80	1.8	0.064mm ²	20 μ W	30nV/ \sqrt{Hz}	n.a.	100
[64]	CMOS	0.6 μ	250 – 486	38.5	2.8	0.45mm ²	4.5 μ W	2.46 μ V	7.6	1
			106 – 5.1k							
[65]	CMOS	0.7 μ	119 – 5.1k	76 – 102	\pm 2.5	1.13mm ²	4mW	0.35 μ V	3.6	1
			201 – 5.1k							
			352 – 5.1k							
[68]	CMOS	0.35 μ	2 – 20k	64	\pm 1.65	8.96mm ²	33mW	2.9 μ V	n.a.	64
[69]	CMOS	0.35 μ	100 – 10k	20	\pm 1.65	5mm ²	n.a.	10 μ V	n.a.	1
[70]	CMOS	0.5 μ	530 – 5.3k	61 – 73	\pm 2.5	15.96mm ²	n.a.	27.7nV/ \sqrt{Hz}	n.a.	17
[73]	CMOS	0.5 μ	1.1k – 5k	60.1	3.3	27.3mm ²	13.5mW	5.1 μ V	n.a.	100

Table 1.2: Main characteristics of neural recording system presented in literature

1.5.2 Patch clamp circuits for Ion channel current detection

As explained in Section 1.2.2, the generation of electrical signals in biological cells is possible thanks to ions that move across the cell membrane. In many applications it is important to record these currents in order to understand which electro-chemical processes are involved in the signal generation and to have a direct measurement of the ion channels involved in the reaction. Ion currents, in fact, play a key role in several physiological processes, in neural signal generation, as already discussed, but also in the maintenance of heartbeat and in muscle contraction [77]. The signal is recorded by means of a pipette, depending on the way the pipette is attached to the membrane. It is possible to record the electrical activity of the whole cell or of a small patch of channels (even a single channel current can be measured) [77–79]. The recording of a small cluster of channels is possible because the contact between the pipette and the membrane cell forms a Gigaohm seal [77, 80], allowing to isolate the electrical activity of a small area of the membrane. The patch clamp working principle consists in fixing the external membrane potential to a control voltage and in recording the current that flows across the membrane using proper electronic devices. These devices can be implemented, as in a wide number of paper presented in literature [77, 79, 81], as the cascade of an integrator and a differentiator (Fig. 1.14) or, as also proposed in this thesis, as a current feedback delta sigma modulator (Fig. 1.15) [82–87]. In Fig. 1.14, it is also shown the equivalent electrical circuit

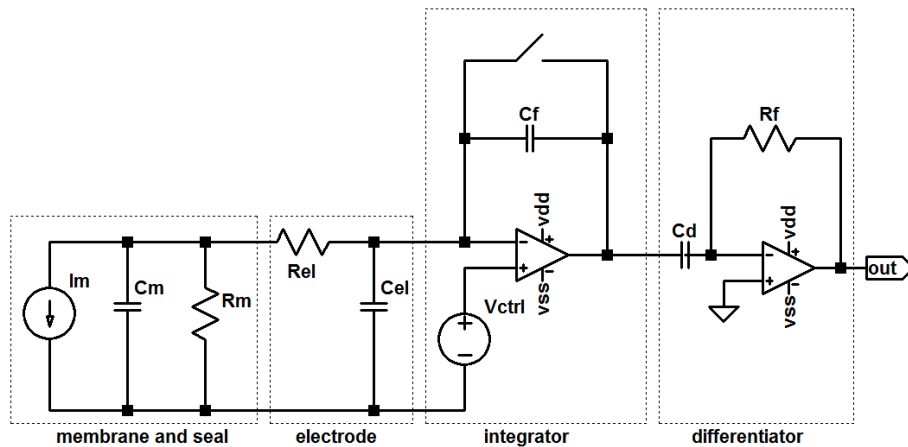


Figure 1.14: Patch Clamp circuit based on integrator-differentiator approach

for the membrane-seal connection and for the electrode. Typical values for these equivalent components are given in Table 1.3

C_m	C_{el}	R_m	R_{el}
$300fF$	$500fF$	$20G\Omega - 40G\Omega$	$10M\Omega - 140M\Omega$

Table 1.3: Equivalent electrical parameters for membrane and electrode

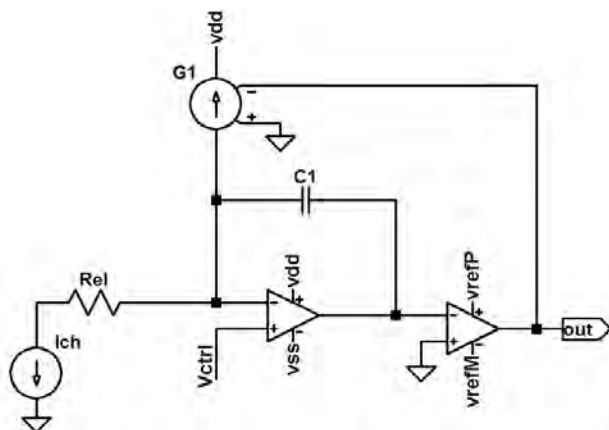


Figure 1.15: Patch Clamp circuit based on a sigma-delta approach

The circuits traditionally used to detect ion channel currents, are very similar to potentiostats used to record redox current in electrochemical sensing devices [88–90]. In fact in both cases the aim is to detect a current in a range from hundreds of fA to few μA . The control voltage in the case of ion channel detection is used to set the membrane potential while in potentiostat it sets the redox voltage. The advantages of the delta-sigma approach are that the current is directly recorded as a digital pattern without need of differentiator, and the reset switch of Fig. 1.14 can be avoided considering that the current, at the input node, is supplied or sinked according to the feedback bit, avoiding the amplifier saturation.

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Chapter 2

Neural recording and stimulation: a COTS device

The realization of a neural electrical interface is a particularly critical task and requires to have a clear and complete control on all the parameters involved in such design. Prior to proceeding with a fully implantable device, that, due to dimensions and power consumption, is the only possible way for a long term solution, it is necessary to carefully evaluate the characteristics of the neural signals, in terms of amplitudes, bandwidth, as well as regarding the neural stimulation parameters. The use of COTS is a low cost and short implementation time solution, widely used to assess preliminarily all these specifications. In this Chapter, the system architecture of the COTS neural interface is presented, the available operating modes are described and finally the results obtained by means of electrical and in-vivo tests are discussed.

2.1 Design specifications

As widely discussed in the first Chapter, neural spikes are characterized by low amplitudes, that can vary in a range from few microvolts to hundreds of microvolts, and they are drowned in a noisy environment due to EMG interferences. The recording module should then provide a gain and a resolution capable to describe a microvolt level signal and should be able to filter the unwanted components. A first amplification-filtering stage is thus mandatory to amplify the weak signal for a proper ADC conversion and to eliminate the EMG interferences. The gain needed for the amplifier can be determined considering the converter resolution. In order to find a good compromise between resolution and data transmission speed, a 16 resolution ADC has been chosen. Using a 3V voltage supply, the resulting Least Significant Bit

(LSB) is $45.7\mu V$, to achieve a proper conversion it is then suitable to bring at the ADC input a signal of about $500\mu V$. Considering a worst case condition, with an input signal of $1\mu V$, a gain of at least $54dB$ is needed. A higher gain can be useful to have a better signal representation in the case of weak signals, but could be detrimental for strong signals because it could cause amplifier saturation. The solution seems to be then a programmable gain amplifier (PGA). The total input referred noise of the system should be lower than the minimum detectable signal. A high selective bandpass filter is necessary to reject the huge low frequency interferences; since the neural spectral signature is in the interval $800Hz - 3kHz$, the filter operates in this range. in Table 2.1 the resulting system specifications are reported.

Fixed Gain	$54dB$
Variable Gain	$40dB$
HPF order	8^{th}
HPF frequency	$800Hz$
LPF order	4^{th}
LPF frequency	$3kHz$
ADC resolution	16 bit
IRN	$< 2\mu V$

Table 2.1: Recording module specifications

From the stimulation point of view, the generation of biphasic train pulses is needed, the parameters are shown in Fig. 2.1 and should vary in the ranges indicated in Table 2.2. In Fig. 2.1, a stimulation pulse in which the anodic phase precedes the cathodic is depicted, but also the cathodic-anodic shape can be useful and must be provided by the stimulation unit.

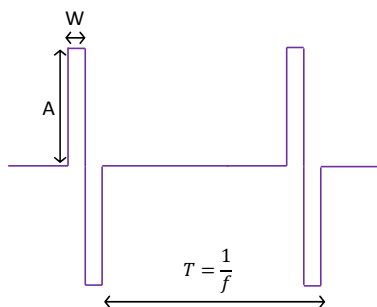


Figure 2.1: Stimulation pulse train

Pulse Width [W]	$10\mu s \div 300\mu s$
Pulse Amplitude [A]	$10\mu A \div 300\mu A$
Pulse Frequency [1/T]	$10Hz \div 400Hz$

Table 2.2: Stimulation module specifications

2.2 System Architecture

The neural recording-stimulation unit is described in its basic blocks in Fig. 2.2 and consists of four main parts: electrode, neural recording circuitry, stimulus generation circuitry and digital system controller.

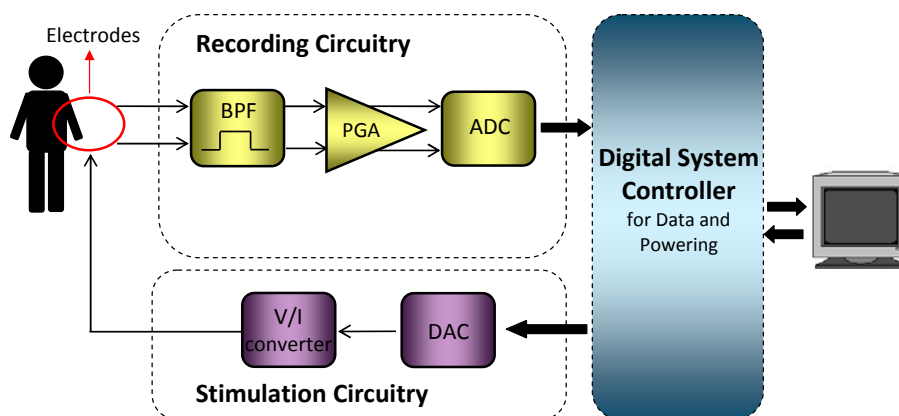


Figure 2.2: Block diagram of the neural recording and stimulation system

The extracellular signals are extracted from a tf-LIFE electrode then they are acquired and filtered by a recording circuitry in order to remove unwanted low frequency components. Once that the neural signal has been cleaned, it can be digitally converted before being transmitted to the digital control unit. A programmable amplification stage has been added in order to exploit the full dynamic range of the ADC. The stimulation circuitry delivers trains of electrical charge pulses to excitable tissue, via the tf-LIFE electrode. The system receives stimulus patterns from the digital controller and converts them first into an analog voltage through a DAC then into a stimulation current signal by means of a V/I converter. The digital system controller has two main tasks. First, it provides power from a rechargeable battery to ensure the isolation of the patient from the electric grid (both for safety reasons and to reduce the interferences injected by the grid). Main task of the module, however, is managing the configuration of the whole system with the

generation of timing signals (for multiplexers, ADC, DAC), programmable gain and stimulation patterns. For a high-speed real time data transmission a Universal Serial Bus (USB) controller has been integrated in the system. The user can easily control the system by means of a Graphical User Interface (GUI) customized for this application and shown in Fig. 2.3.

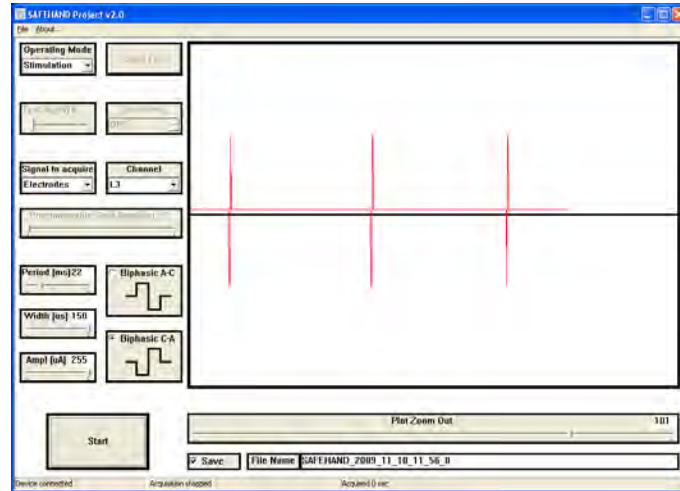


Figure 2.3: Graphical User Interface

2.2.1 Recording unit

The implemented filtering circuitry is shown in Fig. 2.4: it is made up of a 8th order high-pass filter cascaded with a 4th order low-pass filter. All the basic blocks are second order cells and have been implemented with a Multiple Feedback topology. Fully differential input/output amplifiers (Linear Technology, LT1994) with a very low noise density ($3nV/\sqrt{Hz}$) have been employed.

The filter design specifications required a gain of $54dB$ and a frequency bandwidth between $800Hz$ and $3kHz$. The gain has been equally subdivided among the blocks, therefore every cell provides a gain of $9.3dB$. Since the major concern is due to low frequency huge interferences, the HPF blocks have been collocated as first stages. In this way it has been possible, to filter out such interferences preventing the amplifier saturation. Reduction of IRN is achieved allocating some gain ($9.3dB$) at the very first stage of amplification; by distributing the overall gain along the signal chain it has been possible to filter out interference components before fully amplifying them [1–3]. In Table 2.3 and in Table 2.4 the values of the resistive and

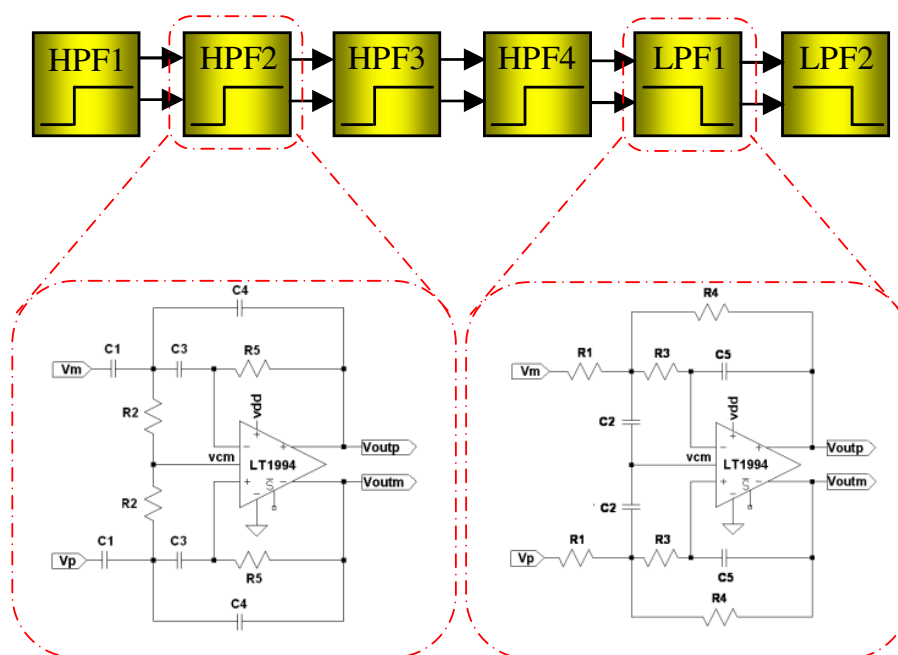


Figure 2.4: Circuit diagram of the band-pass filter

capacitive components, referring respectively, to the high-pass filter and to the low-pass filter, are reported.

Component	HPF1	HPF2	HPF3	HPF4
R_2	150Ω	56Ω	150Ω	56Ω
R_5	820Ω	3520Ω	820Ω	3520Ω
C_1	$1.13\mu F$	$1.13\mu F$	$1.13\mu F$	$1.13\mu F$
C_3	$1.13\mu F$	$1.13\mu F$	$1.13\mu F$	$1.13\mu F$
C_4	$330nF$	$330nF$	$330nF$	$330nF$

Table 2.3: Resistors and Capacitors values for the HP filter

In Fig. 2.5 the chosen amplification circuitry is shown: the digitally controlled potentiometers $R7$ (Intersil, ISL90727, ISL90728), in pair with resistors of 100Ω ($R6$), allow obtaining a gain factor that can vary from $1V/V$ to $100V/V$ with 127 different values. The gain is set by the user through the GUI, however the software can be easily modified in order to implement automatic control. The chosen differential analog-digital converter (Analog Devices, AD7687) provides the processed signal with a resolution of 16 bit, an Effective Number of Bits (ENOB) of about 15.3 and a sampling frequency

Component	LPF1	LPF2
R_1	150Ω	390Ω
R_3	150Ω	390Ω
R_4	390Ω	1500Ω
C_2	$330nF$	$330nF$
C_5	$10nF$	$10nF$

Table 2.4: Resistors and Capacitors values for the LP filter

of $10kHz$ to the digital control unit. The attenuator used in test mode has the same architecture proposed for the amplifier but fixed resistances have been used ($R6 = 10k\Omega$, $R7 = 100\Omega$).

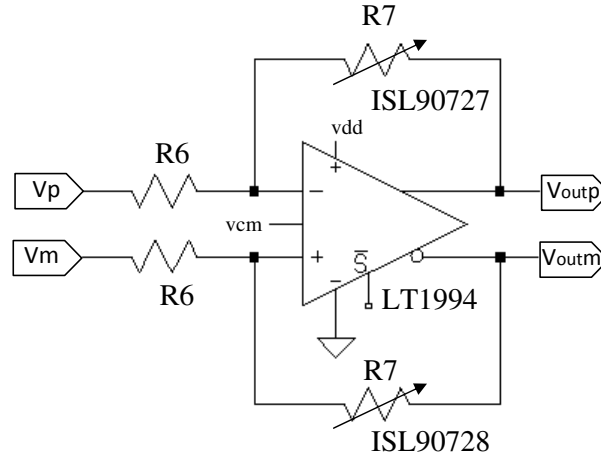


Figure 2.5: Amplification circuitry

2.2.2 Stimulation unit

The bi-directionality of the neural electronic interface implies the integration of a stimulation unit. Neural stimulation consists typically in the injection of current pulses into the implanted electrode. As shown in Fig. 2.6, this is possible using two main blocks: a D/A converter (Linear Technology LTC2641) and a V/I converter realized using a simple operational amplifier (Texas Instruments, OPA343) in a non-inverting configuration, where the feedback resistor is the electrode impedance. The basic idea is to convert a programmable voltage, generated by the DAC, into a stimulation current that will flow through the tf-LIFE. Note that R_{electr} in the circuit represents

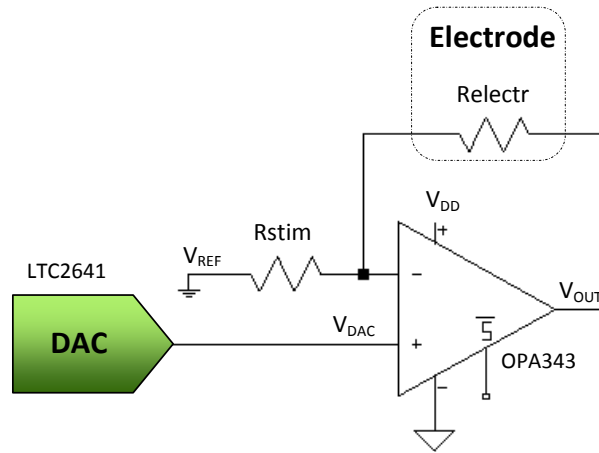


Figure 2.6: Neural stimulator

the tf-LIFE impedance. According to datasheets, the exact range of the electrode impedance is controversial and its values at $1kHz$ span from $10k\Omega$ to $1M\Omega$; in literatures similar values have been reported [4, 5]

2.2.3 Digital control unit

The analog part of the board contains, as reported in previous sections, many devices whose behavior must be digitally controlled. For this reason, a digital unit is mandatory for the proper operation of the system. As main Digital Signal Controller (DSC), the high-performance Microchip *dsPIC33Fj256GP506* has been used. The DSC employs a powerful 16 bit architecture that integrates the control features of a Microcontroller (MCU) with the computational capabilities of a Digital Signal Processor (DSP). Among all the available communication modules the 3-wire Serial Peripheral Interface (SPI) and the Inter-Integrated Circuit (I^2C) have been employed in this system.

As show in Fig. 2.7, in the analog recording and stimulation management, two SPI modules are used for the communication between dsPIC/ADC and dsPIC/DAC while an I^2C bus is employed to control the value of the digital potentiometers of the amplification circuit. The transmission module consists of an USB controller (Microchip *PIC18LF4550*) that interfaces the DSC (exploiting an I^2C interface) with the host PC. The digital unit is also responsible of the system configuration (electrode selection, stimulation shape parameters, switches selection). Moreover the controller unit contains all the circuitry for power management namely: a rechargeable battery (3.7 V) to ensure the isolation of the patient from the electrical grid, the recharg-

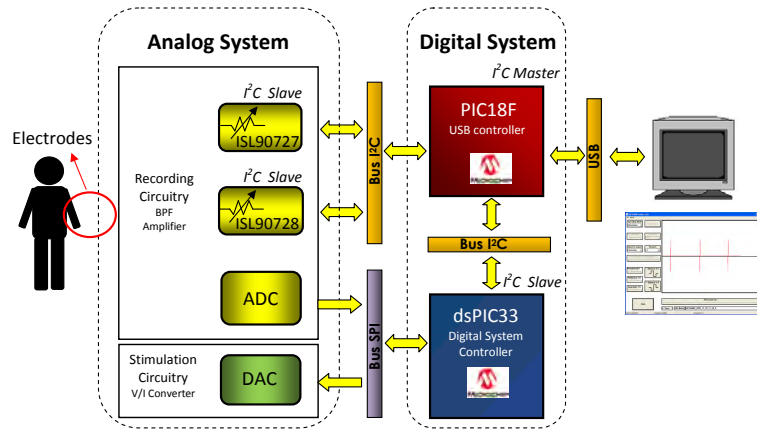


Figure 2.7: Microcontrollers management of the system modules

ing circuit, and two voltage regulators (Maxim, MAX1589 and MAX1792) of 3V and 1.5V, needed to power the digital board itself.

2.3 Operating modes

The proposed device is characterized by a high degree of reconfigurability and can switch among several different operating modes. There are four main tasks performed by the board: signal recording, neural stimulation, electrode impedance measurement and self-testing. This high flexibility is guaranteed by the network of switches shown in Fig. 2.8. Table 2.5 describes how the signals *Rec*, *Stim*, *Test* and *Imp_meas* must be digitally set to choose the operating mode.

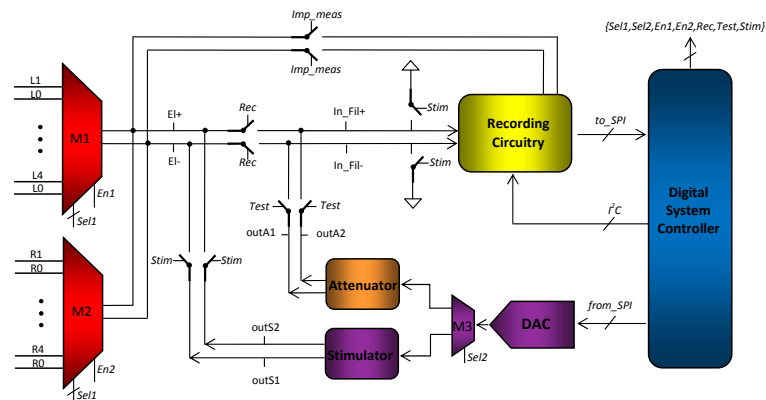


Figure 2.8: Switch network for system reconfigurability

Working mode	<i>Rec</i>	<i>Stim</i>	<i>Test</i>	<i>Imp_meas</i>
<i>Recording</i>	1	0	0	0
<i>Stimulation</i>	0	1	0	0
<i>Test</i>	0	0	1	0
<i>Imp. Measurement</i>	0	1	0	1

Table 2.5: Switches configuration for different operating modes

These four different physical paths, actually, are handled by the micro-controllers firmware as if they were seven different operating modes. Indeed, there are two different testing modes, two different approaches for impedance measurement and one additional mode that combines together stimulation and recording. The digital control module, in order to acquire and generate signals, must manage the communication between three different processors: the PC, the USB controller (PIC18F) and the main DSC (dsPIC). Fig. 2.9 shows how this communication is performed.

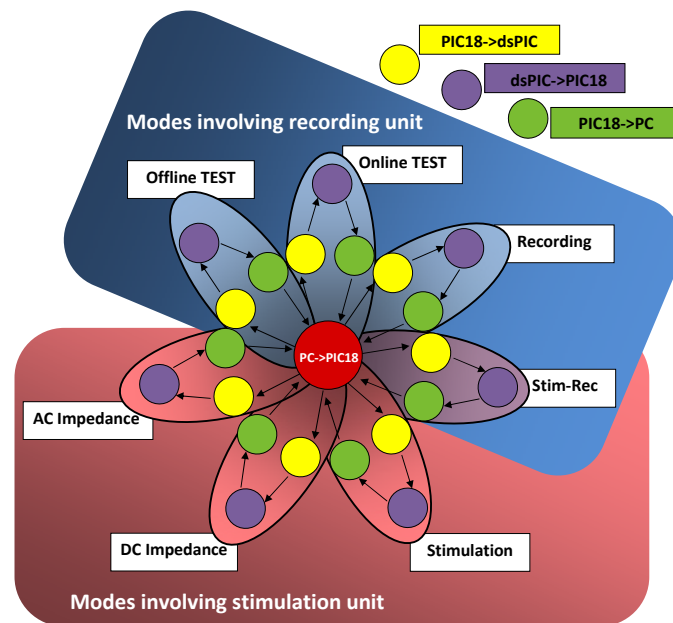


Figure 2.9: State diagram of processor communication in different operating modes

All the modalities share the same initial state, in which the communication $PC \Rightarrow PIC18F$ is managed. Then, for the working mode selected by the user, there are three further states that handle respectively the communications $PIC18F \Rightarrow dsPIC33$, $dsPIC33 \Rightarrow PIC18F$ and $PIC18F \Rightarrow PC$.

The four states are in a closed loop and come one after the other until the user stops the process from the GUI. Once that the signal has been processed and transferred to the PC, it can be saved in a data file for further elaborations and, at the same time, displayed in the GUI. In the following, each function is described in details referring to Fig. 2.8.

2.3.1 Recording mode

During this working mode, in vivo-signal recording can be performed. The neural signal is captured from the tf-LIFE electrode and sent to the recording unit by short-circuiting nodes $El+$ and $El-$ with the input terminals of the filter (In_Fil+ , In_Fil-), using the switches driven by Rec signal. The signal is then filtered, amplified, converted into digital samples and sent to the PC to be stored in a data file. Since the system has a single signal path, the eight tf-LIFE channels can not be acquired simultaneously. Two multiplexers ($M1$ and $M2$) select which input pair must be acquired and forwarded to the recording unit. The enable signals $En1$ and $En2$ activate only one multiplexer at a time. The developed GUI allows the user to change the recording channel (among the 8 available in a tf-LIFE) and to modify the amplification gain during the experiments. A trigger signal can be activated to keep track of the occurrence of external stimuli thus simplifying the off-line analysis or recorded data. The captured physiological data can be viewed in the GUI in real time and can also be sent to the loudspeakers of the PC. This latter function is particularly useful during in-vivo experiments as a run-time feedback and could be exploited during implantation to guide final adjustment of the electrode position inside the nerve.

2.3.2 Stimulation mode

When this operating mode is selected, the system is enabled to inject a stimulation current in a selected tf-LIFE channel. Different digital patterns, generated by the system controller, are converted into an analog voltage by the DAC. Activating the selection signal $Sel2$ of $M3$, the resulting analog signal can be sent to the stimulator, a V/I converter, that generates the stimulation current. The switches driven by the signal $Stim$ allow to connect the stimulator outputs to $El+$, $El-$ nodes. At the same time, to avoid drift voltage phenomena and to prevent amplifier saturation (thus reducing the recovery time after the stimulation artifact), the input terminal of the filter is connected to a reference voltage, thus temporarily blanking the recording circuitry. The typical stimulus shape is a train pulse composed of biphasic pulses; the GUI allows to select a wave in which the anodic phase precedes the

cathodic or viceversa. Stimuli parameters such as amplitude, pulse duration, frequency of the pulses and number of pulses are fully programmable by the user. The system allows also to acquire the signals sent to the PNS, selecting the electrodes as an ADC input. In this way, the stimulation form can be displayed in the GUI and stored in a data file allowing to verify if the current in the electrode is that expected.

2.3.3 Stimulation-Recording mode

This mode combines together the feature provided in stimulation mode and in recording mode. Once that a stimulation pattern has been sent to the tf-LIFE, the system switches automatically its configuration into the recording mode to acquire the neural response. During the stimulation phase, the recording unit is disconnected from the electrodes and is connected to the reference voltage. This avoids the filter saturation that would result in a recovery time too long from the slew rate condition. The possibility to stimulate in a channel and to record the results in a different one is also provided.

2.3.4 Impedance measurement mode

The electrode impedance can be measured exploiting the stimulation and the recording circuits. A known current signal is provided by the stimulator and injected into the electrode closing the switches driven by *Stim*. Contemporarily, the *Imp_meas* signal allows to connect the electrode terminals with the ADC of the recording unit. By this way the voltage drop across the electrode is sent to the digital system controller and the impedance value can be assessed. The frequency and the amplitude of the injected current can be set through the GUI. Such a feature has a particular importance for stimulation, in fact from the Fig. 2.6 it can be observed that, with an electrode impedance too high, the gain of the amplifier increases and the current that flows through the electrode saturates at a value that is as much lower as higher the electrode impedance is.

DC impedance measurement

A series of constant steps of different amplitudes covering all the output dynamic range of the DAC is generated and sent to the V/I converter. The voltage drop across the electrode is recorded by the ADC and this allows to extract the value of the impedance (its real part only).

AC impedance measurement

In the AC impedance measurement, the signal injected into the electrode is a sine with frequency and amplitude programmable from the GUI. The program acquires ten periods of the signal taken across the resistance, extracts the sine peaks and uses the average of these values to calculate the impedance at the given frequency.

2.3.5 Test mode

The test working mode allows to evaluate and verify the recording circuitry functionalities in terms of bandwidth and gain, before in-vivo laboratory trials on animals. Since the converter output voltage swings from 0V to 3V, with a resolution of $45.7\mu V$, the generation of signals in the range of few microvolts has required the introduction of an attenuation factor of 0.01. The DAC output signal is propagated to the attenuator by means of *M3*, deactivating *Sel2* signal. Once that the signal has been significantly reduced, it is redirected to the recording circuitry (closing the switch driven by *Test* signal) in order to be processed.

Online TEST

This working mode allows to test the performance of the system in a context similar to that expected in an in-vivo recording case. This means that the signal sent to the recording unit is filtered, amplified and re-acquired in real time. The sinusoidal signal is generated inside the dsPIC33 according to the command set by the user in the GUI. The frequency and the amplitude of the wave can be changed in real time, by this way it has been possible to verify the specifications of the filter bandwidth.

Offline TEST

A further test mode has been used in order to test the filter with pre-recorded neural signals. In this case the input signal is stored in a text file that can be selected by the user as input for the system. Due to the limited memory of the dsPIC33 (16 kByte) the whole file can not be loaded into the microcontroller, for this reason it is transferred in blocks of 7200 samples of 16 bits each. The blocks are sent to the recording unit, acquired by the ADC and stored in the dsPIC33 memory (overwriting the input values). Once that this operation has been completed, the blocks are sent back to the PC and stored in a output data file.

2.4 Experimental results

The fabricated prototype housed in a protective enclosure is shown in Fig. 2.10. Special attention has been paid on how to isolate the analog module from the interferences (especially on supplies) generated by the digital unit. For this reason the system has been divided into analog and digital parts and implemented in two separate, sandwich-detachable, printed circuit boards (PCB) sizing respectively, $7\text{cm} \times 6.1\text{cm}$ and $7.5\text{cm} \times 5.8\text{cm}$.



Figure 2.10: Photograph of the implemented PCB system

The proper operation of the whole neural embedded system has been validated at two different levels. First, the electronic behavior has been confirmed by configuring the system in test working mode. Later, the recording and stimulation capabilities have been assessed through in-vivo measurements on animals.

2.4.1 Electrical tests

Recording capabilities

The first phase of experiments was aimed at validating the band-pass filter selectivity. Sinusoidal signals, generated by the DAC, have been acquired by the recording unit at 20 different frequencies, covering values from 400Hz to 9kHz . The filter presents a maximum gain value of 56dB in a bandwidth between 800Hz and 3kHz , a high-pass roll-off of 160dB/dec and a low-pass roll-off of 80dB/dec . The filter frequency response is shown in Fig. 2.11.

Moreover, the high selectivity of the BPF has been tested using as input of the recording circuitry the signal reported in Fig. 2.12(a). It is composed

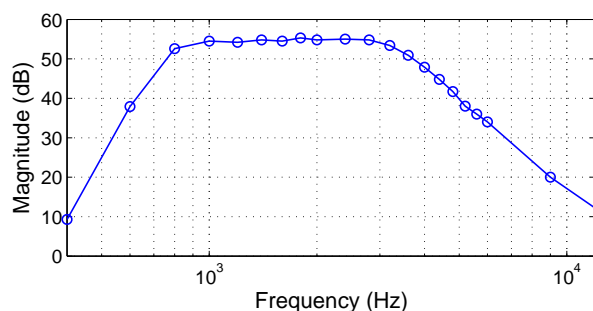


Figure 2.11: Bode diagram for the recording module filter

by the sum of three sines at the frequencies of 400Hz , 1.2kHz and 8.4kHz , whose spectrum is displayed in Fig. 2.12(b).

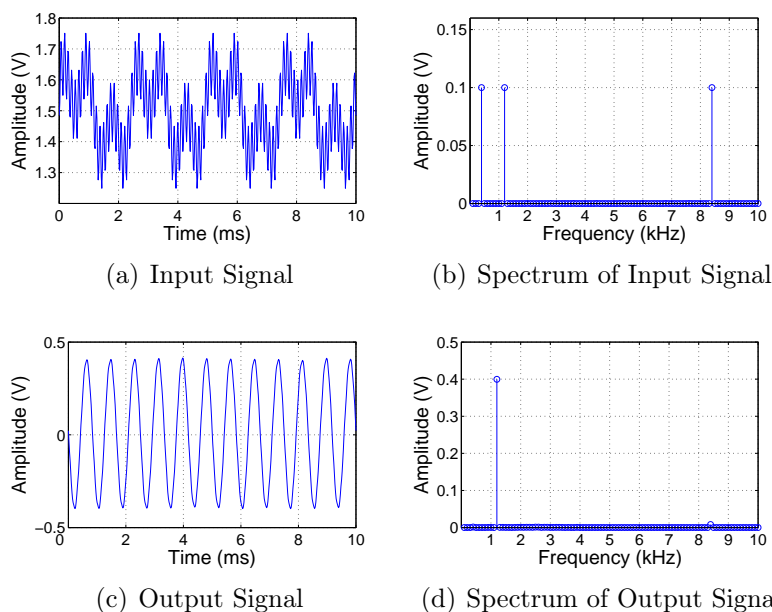


Figure 2.12: BPF response to an input obtained as the sum of three sines at different frequencies (400Hz , 1.2kHz , 8.4kHz)

The effects of the bandpass filtering are shown in Fig. 2.12(c) where, as expected, only the component at 1.2kHz has been allowed to pass. The output spectrum shown in Fig. 2.12(d) proves how out-band frequencies have been strongly attenuated while the component in bandwidth has been amplified. The filter linearity has also been verified; the output differential voltage, at

800Hz, can swing between $[-2.84V \div 2.83V]$. For an input signal with amplitude of $1.1mV_{pp}$ and frequency 800Hz the total harmonic distortion, with a programmed gain of 56dB, is 0.076%. All front-end (filter, amplifier and A/D converter) functionalities have been tested using, as input, pre-recorded neural patterns supplied by the Scuola Superiore Sant'Anna in Pisa (SSSA), on the basis of recordings made in clinical trials with rabbits. The input pattern, represented in Fig. 2.13(a), corresponds to 10 seconds of recording during which the rabbit was subjected to vibrations at 50Hz and 100Hz in cutaneous afferents.

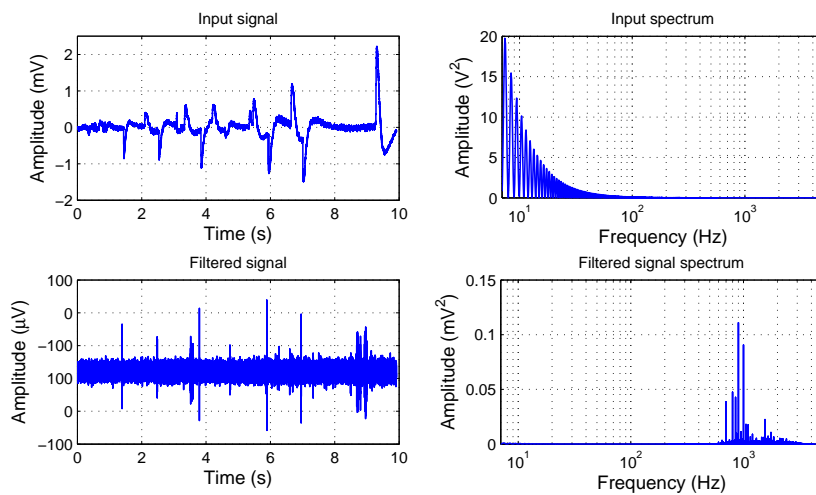


Figure 2.13: Self-test with pre-recorded data: (a) input signal, (b) input power spectral density, (c) output signal (input-referred), (d) output spectral density

The input signal is affected by EMG (and probably ECG) interferences with a very large amplitude (in the millivolts range) and a spectrum (Fig. 2.13(b)) concentrated below 300Hz. Such interferences completely mask the underlying neural signal. Fig. 2.13(c) displays the measured, input-referred, output of the device and Fig. 2.13(d) its power spectral density: the low-frequency interferences are completely removed and the weak neural signal (in the microvolts range) is now visible, as well as its frequency signature. The test was carried out in a noisy environment without any special electrostatic shielding.

Stimulation capabilities

The capability of the system to generate the programmed stimulation pulses has also been proved. For this purpose in the electrical tests, the tf-LIFE

electrode has been replaced by a $50k\Omega$ resistor whose value is within a reasonable range according to literature [5, 6].

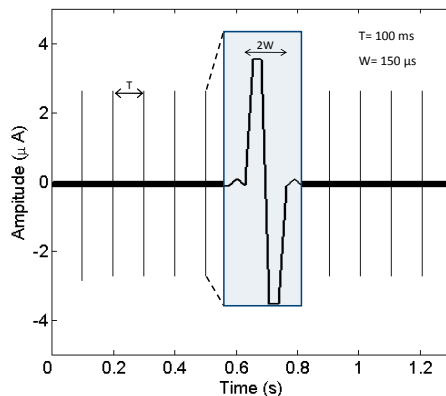


Figure 2.14: Stimulation pulse train

In Fig. 2.14 a stimulation pattern composed by 12 bi-phasic pulses with $10Hz$ frequency, $150\mu s$ pulse width and $26\mu A$ amplitude has been generated.

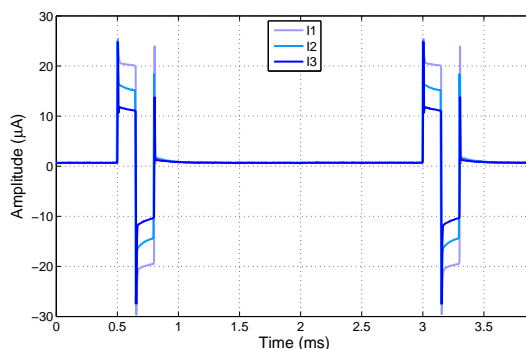


Figure 2.15: Current stimulus with different amplitudes

Amplitude programmability of stimulation pulses is evident in Fig. 2.15, where three different current values of $10\mu A$, $15\mu A$ and $20\mu A$ have been obtained. It must be noted that with a lower impedance, higher current values can be obtained up to a maximum of $255\mu A$.

Fig. 2.16(a) and Fig. 2.16(b) display different voltage pulses applied to the V/I converter that generate current pulses widths (represented in Fig. 2.16(c) and Fig. 2.16(d)) covering values within the interval $5\mu s$ to $150\mu s$. The pulse frequency can also be programmed and can vary in the range $[10Hz \div 400Hz]$ while the number of pulses within a single train can reach

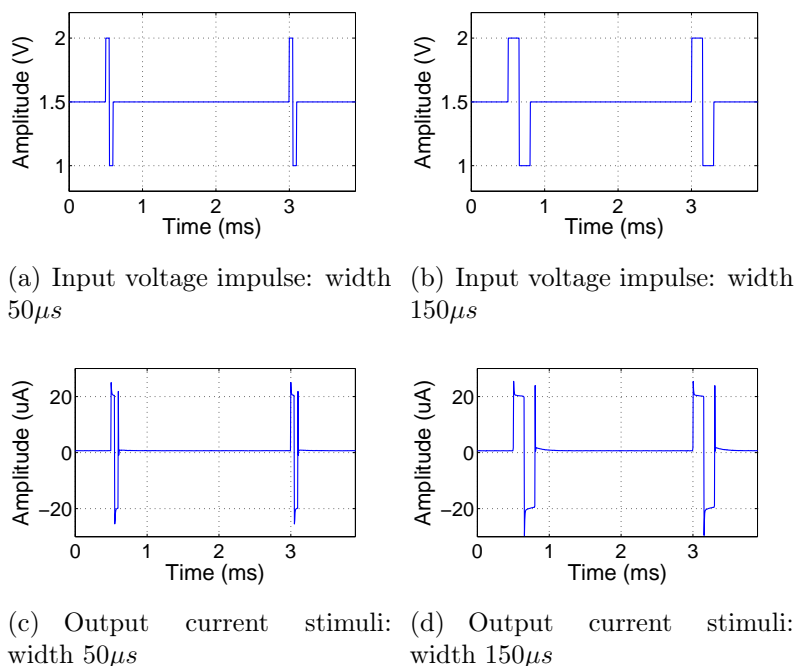


Figure 2.16: Neural stimulation: pulse width programmability

up to 50. Moreover it is possible to select a pulse shape in which the anodic phase precedes the cathodic or viceversa.

Impedance measurements capabilities

Looking at the stimulator schematic of Fig. 2.6 it can be explained that, although the stimulation current flowing into the electrode is independent by the electrode impedance value, it saturates to a maximum value that depends on the electrode impedance. Thus the assessment of the impedance value has a primary importance to determine the current injected into the electrode. For this reason the impedance measurement mode has been introduced in the system. From Equation (2.1) it can be stated that between the voltage drop across the electrode and the input voltage there is a linear relation.

$$V_{OUT} - V_{DAC} = \frac{R_{electr}}{R_{stim}} V_{DAC} - \frac{R_{electr}}{R_{stim}} V_{ref} \quad (2.1)$$

In Fig. 2.17 the linear fitting of the curve $(V_{out} - V_{DAC}; V_{DAC})$ has been extracted (only the linear range of the curve has been considered while the saturated samples have been eliminated). Comparing the resulting coefficients of

Fig. 2.17 and the Equation (2.1), the resulting impedance is $R_{electr} \simeq 50k\Omega$ as expected (a $R_{stim} = 5.6k\Omega$ has been used).

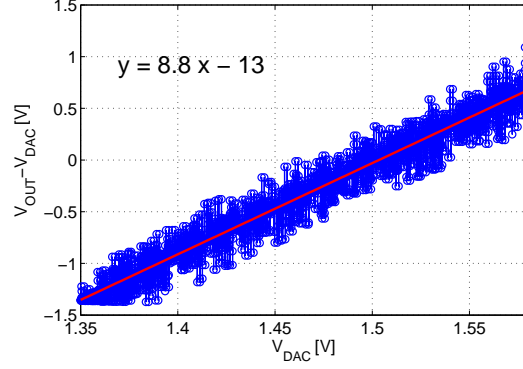


Figure 2.17: DC impedance measurement results: linear fitting

The system is also able to measure the AC impedance injecting a sinusoidal signal into the electrode. The input frequency can vary in the range $[10Hz \div 1kHz]$ while its amplitude can cover values from $1mV$ to $255mV$.

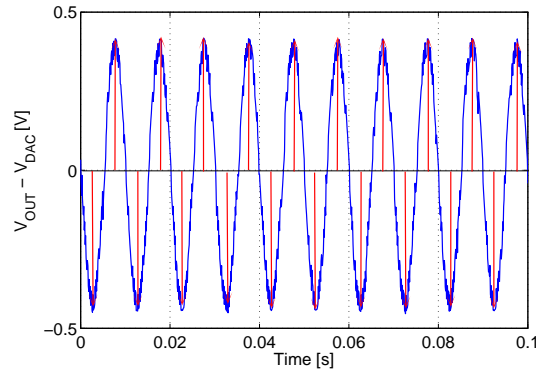


Figure 2.18: AC impedance measurement results: peaks extraction

In Fig. 2.18 the voltage drop across the electrode resistance is shown when a $100Hz$ sine with an amplitude of $50mV$ is applied as input signal.

$$R_{electr} = R_{stim} \frac{(V_{OUT} - V_{DAC})_{av}}{V_{DAC} - V_{ref}} \quad (2.2)$$

The electrode impedance can be obtained with the Equation (2.2), where

the output value $V_{OUT} - V_{DAC}$ has been achieved by averaging ten sine peaks. The result confirmed again an electrode impedance $R_{electr} \simeq 50k\Omega$

2.4.2 In-vivo tests

The in-vivo measurements have been performed on anaesthetized animals at the School of Medicine of the Universitat Autònoma de Barcelona (Spain) under the supervision of Prof. Xavier Navarro. A tf-LIFE electrode was implanted in the sciatic nerve of an adult 3-month-old Sprague-Dawley rat weighting $300g \div 350g$, using aseptic microsurgery procedures as shown in Fig. 2.19. All processes were performed under ketamine/xilacynce anaesthesia ($90/10$ mg/kg i.p.) and using a protocol approved by the local Ethical Committee. Various sensory stimuli were applied to the hind limb of anaesthetized animal and the elicited ENG signals were recorded using the developed embedded system (Fig. 2.20). In Fig. 2.21, the real time acquisition on the pc of the signal coming from the PNS of the rat can be observed.

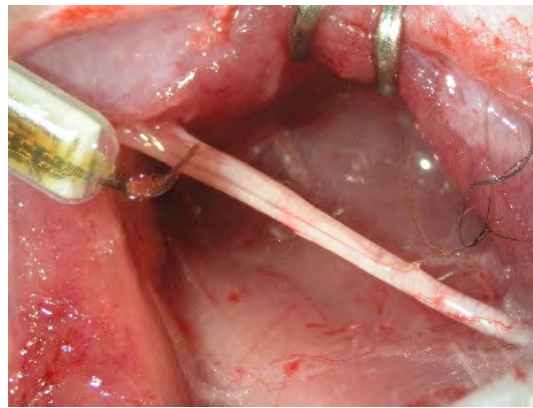


Figure 2.19: Photograph of the rat sciatic nerve with a tf-LIFE implanted

Various sensory stimuli were applied to the hind limb of anaesthetized animal and the elicited ENG signals were recorded using the developed embedded system (Fig. 2.20). In Fig. 2.21, the real time acquisition on the pc of the signal coming from the PNS of the rat can be observed.

In Fig. 2.22 it is shown the big difference, in terms of dimensions, between the typical laboratory instrumentation and the proposed PCB.

Recording capabilities

The neural activity was recorded from each electrode's active site, both in response to mechanical stimuli applied on the animals hindpaw and distal

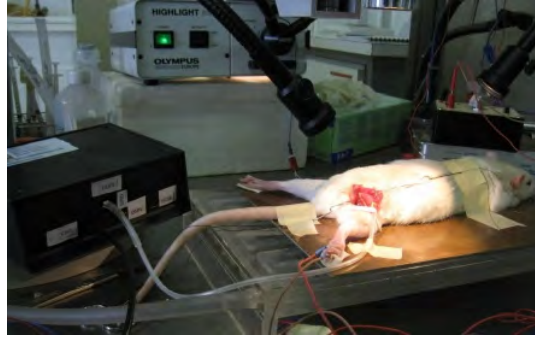


Figure 2.20: Photograph of the rat connected to our board

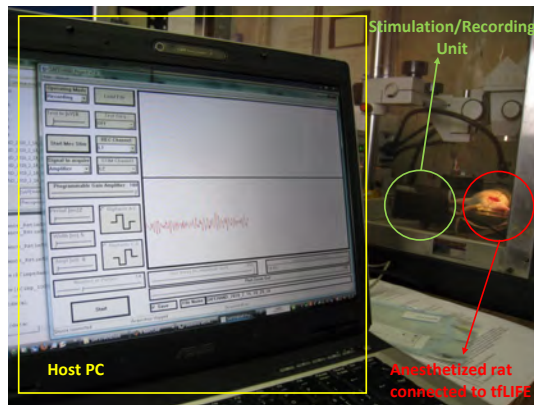


Figure 2.21: Photograph of the PC while acquiring the signal from the rat PNS

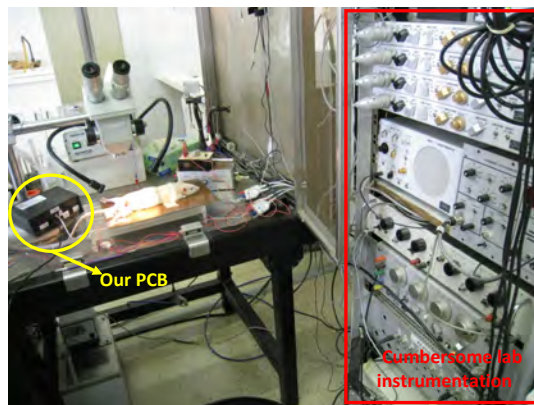


Figure 2.22: Experimental setup: the proposed board and the cumbersome laboratory equipment

electrical stimulation. A good sensitivity to the application of tactile stimuli

on the rat's hindpaw by touching the plantar skin with a special instrument used to produce a controllable sensation of touch (the Von Frey filament) has been observed for R4 channel as depicted in Fig. 2.23.

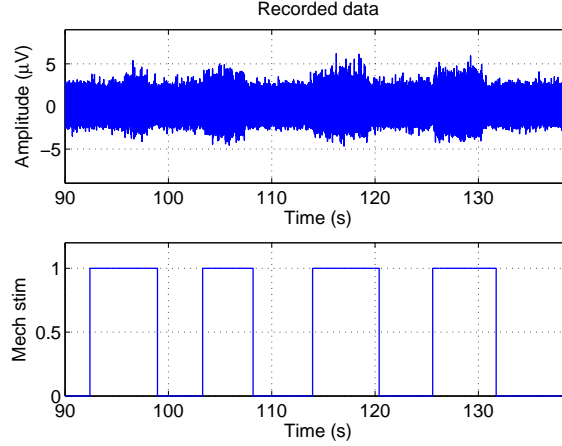


Figure 2.23: Input-referred response recorded from a tf-LIFE during mechanical stimulation of rats hindpaw by means of Von Fray filaments

It can be observed as the noise floor is $5.6\mu V_{pp}$, corresponding to a root mean square (rms) value of $0.83\mu V$, the recording unit is therefore capable to detect microvolt-level neural signals. The rms value has been calculated according to Equation (2.3), where $N = 77200$ noise samples have been extracted from the data displayed in Fig. 2.23.

$$x_{rms} = \sqrt{\frac{x_1^2 + x_2^2 + \dots + x_n^2}{N}} \quad (2.3)$$

The neural patterns show amplitudes around $10\mu V_{pp}$; such low values, even if not common, have been detected by other authors [7]. In Fig. 2.24 the spectrum of the signals displayed in Fig. 2.23 is reported, it can be observed that the most significant contributes are close to $1kHz$.

To further test the acquisition circuitry, electrical stimulation of afferent peripheral nerves has been performed by means of a micrographic stimulation needle inserted in the rat hind paw and connected to Grass stimulation unit. The recording site was $5cm$ distal to the stimulating needle which generated graded electrical potentials (from $0V$ to $10V$), assuring current values lower than $10mA$. The total duration of the stimulus was $100\mu s$ with a pulse repetition frequency of $1Hz$. The afferent response recorded by means of the tf-LIFE electrode and elaborated by the presented circuit is shown in Fig. 2.25.

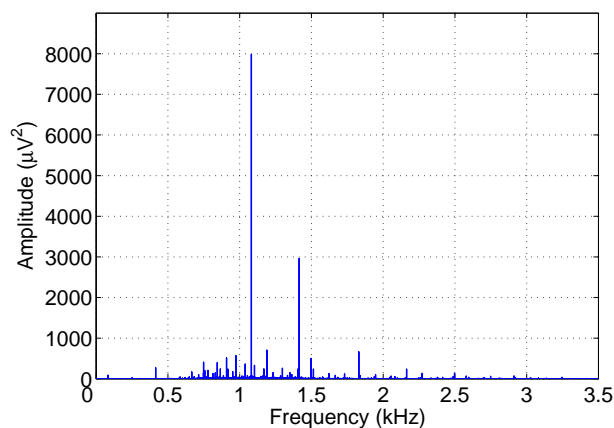


Figure 2.24: Power spectral density of the recorded pattern of Fig. 2.23

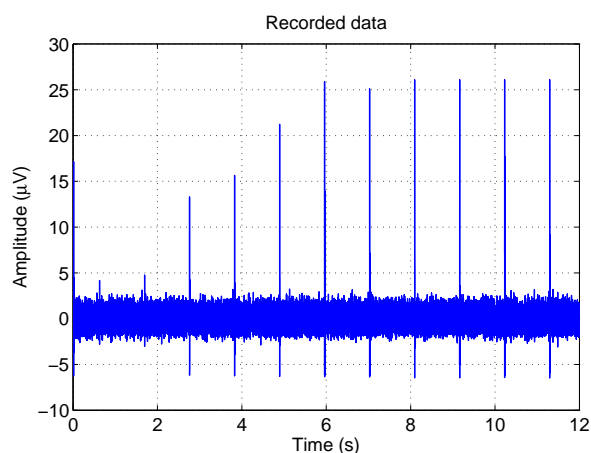


Figure 2.25: Neural response recorded from tf-LIFE during graded afferent electrical stimulation

Fig. 2.26 highlights the response evoked by a single stimulation impulse. The first peak of the waveform is the stimulation artifact while the second peak should correspond to the Compound Action Potential (CAP). For an estimated propagation speed of $42m/s$ (it may vary depending on many factors) the $5cm$ distance should produce a delay of around $1.2ms$ between the two peaks. Such delay is about 10 times larger than the sampling period, thus it is detectable by the system. The curve of Fig. 2.26 is coherent with such theoretical value.

The results of this experiment, anyhow, should be analyzed more in detail since the peaks in Fig. 2.25 may also have a different origin. Actually, when passing through the high-order band-pass filter, the stimulation arti-

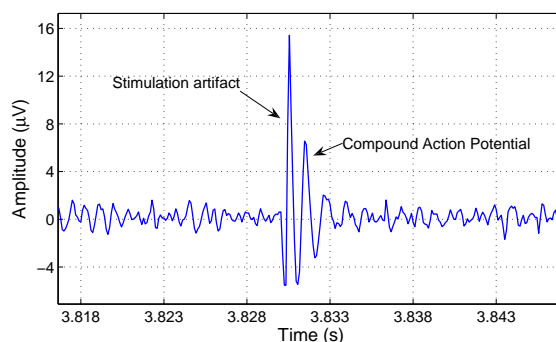


Figure 2.26: Recorded compound nerve action potential response to afferent electrical stimulation

fact may generate an impulse response with a ringing effect similar to that shown in Fig. 2.26. In order to be sure to distinguish a CAP signal from the natural ringing of the filter, we measured the impulse response of the device directly applying an external stimulation of the same amplitude and width of that applied during the in-vivo experiments. An example of such impulse response is shown in Fig. 2.27, where it is compared with the corresponding in-vivo experimental recordings. The figure shows that the two waveforms have different shapes and ringing frequencies. We must conclude that the measured waveform is the superposition of the actual CAP signal and the natural ringing of the filter. The actual CAP signal, anyway, can be reconstructed simply subtracting the measured impulse responses from the experimental recordings (the result is shown in Fig. 2.27).

We repeated this operation for a number of different recordings, changing the stimulus amplitude and the recording electrode. Measuring the delay between the stimulation artifact and the first peak we estimated, considering a nerve propagation speed of 42m/s , the distance between the stimulation needle and the tf-LIFE electrode. In Table 2.6, we report the estimated distances for each electrode, averaged over measures repeated for different stimulus amplitudes. In all the trials, the signal obtained calculating the difference between the in-vivo results and the ringing leads to a calculated distance more consistent with the expected results of about 5cm , confirming that the ringing is partially masking a CAP.

The reason of the graded nerve response of Fig. 2.25 is quite simple. The nerve is composed of many fibres of different diameters and conduction velocity. At lowest stimulus strengths, the fibres closest to the recording site with largest diameter start responding. Then, as the stimulus intensity is gradually increased, more fibres are recruited giving rise to a higher response.

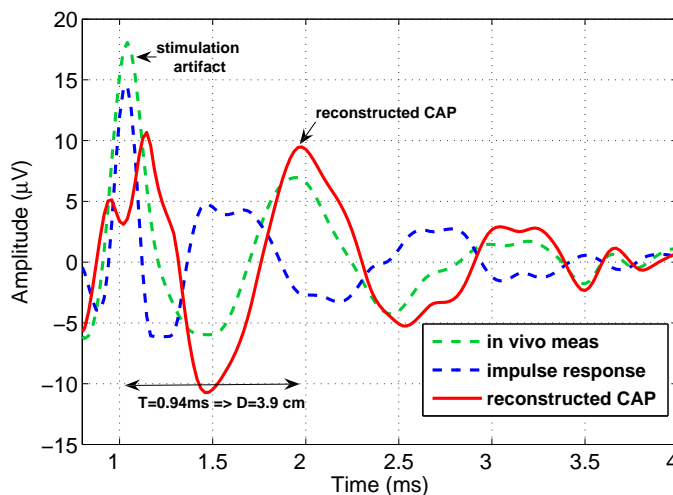


Figure 2.27: In vivo recorded data vs. amplifier ringing

Channel	D1 [cm]	D2 [cm]	D3 [cm]
L1	3.7	2.5	4
L2	4.1	2.4	4.2
L3	3.2	2.5	3.7
L4	2.6	2.3	3
R1	3.3	2.8	3.4
R2	3.9	2.4	4.1
R3	2.9	2.4	3.9
R4	2.4	2.1	3.2
AVERAGE	3.2	2.4	3.7

Table 2.6: Estimated distances between the recording and the stimulation site. D1: distance calculated directly from in-vivo measurements. D2: distance calculated from the filter impulse response. D3: distance calculated from the reconstructed CAP obtained as the difference between the in-vivo measurement and the impulse response

Finally, at maximal stimulus strength, every axon in the nerve is involved and no further increase in the response can be achieved. This phenomenon is confirmed by the saturation in the curve, showing the maximum value of each CAP peak (Fig. 2.28).

As a further confirmation that what is observed in Fig. 2.25 is the CAP response, this saturation phenomenon does not happen for the measured

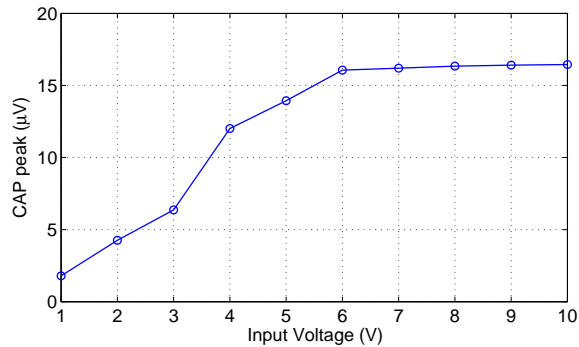


Figure 2.28: Maximum value of each CAP peak

impulse response of the filter, at least until the dynamic range of the amplifier is reached.

Stimulation capabilities

The stimulation capabilities of the embedded system have been validated by means of selective stimulation of efferent fibres. The evoked muscle response was recorded in the plantar muscle of the rat using a PowerLab system by ADInstruments for data acquisition. The stimulus was delivered individually selecting the electrode sites of the implanted tf-LIFE. In Fig. 2.29, the EMG response evoked by 2 bi-phasic pulses of amplitude $200\mu A$ and width $10\mu s$ is shown. Muscular activity appears approximately $2.5ms$ after the stimulus artifact.

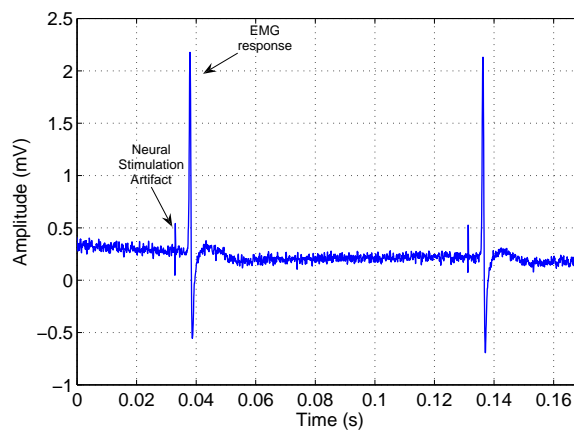


Figure 2.29: EMG recording from the plantar muscle evoked by the developed stimulation circuitry

Amplitude programmability of stimulation pulses is evident in Fig. 2.30, where EMG response to graded neural efferent stimulus is reported. Slight muscle twitches in the hind paw of the rat have also been observed during the experiments.

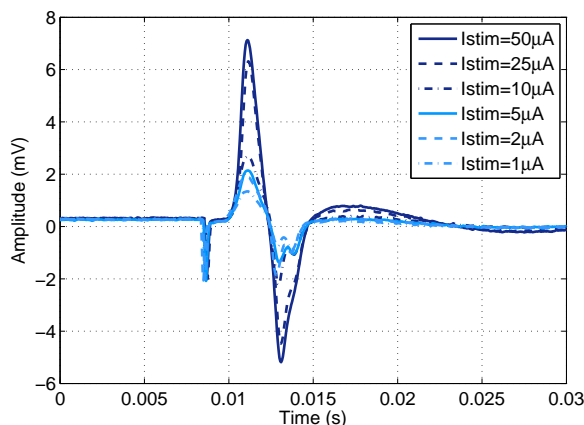


Figure 2.30: EMG response evoked by graded stimulation currents

Due to time reasons it has not been possible to perform a complete and clear in vivo tests using the electrode impedance measurements. The few trials done exhibit a saturated signal, evidence of an impedance higher than expected. In any case, we reserve to do more tests and a deeper analysis regarding the impedance evaluation in future experiments.

2.5 Results discussion

In all the applications in which the signals to be acquired are weak biological voltages or currents, the use of special techniques for low noise and low power design is mandatory. Therefore, the choices made during the design phase have been addressed to reduce these problems. The whole system has been implemented in two distinct PCBs, one for the analog part and one for the digital part in order to preserve the critical analog paths from digital interferences and from power supply noise. The fully differential configuration helps to eliminate all the common mode noise sources. Moreover, it allows doubling the output dynamic range making possible voltage supply reduction. The thermal noise has been reduced minimizing the resistor value in the filter feedback network, obtaining a simulated IRN of $268nV_{rms}$ in the bandwidth ($600Hz - 3.6kHz$). Environmental noise has been minimized paying a careful attention in the PCB layout, making the connection lengths among

different modules as short as possible, especially tracks carrying the neural signals directly coming from the electrodes. Since the EMG interferences are the most worrying noise contributors, in order to avoid the neural signal corruption, an 8th order high pass filter with a $160\text{dB}/\text{dec}$ roll off factor has been chosen. A blanking technique has also been adopted, by this way it is possible to switch from the stimulation mode to the recording mode avoiding the recovery time of the filter. The power consumption has been reduced as possible (given the use of a COTS approach) but the main aim remained minimization of total noise so not all power reduction techniques could be used. A single supply architecture was adopted extracting a 3V supply voltage with a linear regulation (MAX1589) of a 3.7V battery supply. A signal ground of 1.5V (with respect to battery ground) was obtained from another linear regulator (MAX1792). The signal ground obtained in this way proved to be very clean since no current is drawn from the wire. This approach allowed to avoid the use of step-up converters that would be needed in a dual supply architecture, thus avoiding the related high-frequency noise.

The total power consumption was evaluated during electrical tests by measuring the current drawn from the battery. Static power, including both the analog and the digital part, is lower than 1W . About 35% of total power is dissipated by the analog module. The 86% of the analog board power consumption is due to the recording module which contains 7 low-noise operational amplifiers not specifically addressed at low-power operations.

The device could be used for several hours and the battery was recharged only during the breaks of the experimental session. This is compatible with the use in clinical trials that cannot last, not to fatigue the patient, more than a few consecutive hours.

The electrical and in-vivo tests confirm that the level of noise and interferences in the circuit is low enough to detect neural spontaneous signals in the order of magnitude of a few microvolts. The IRN is one of the lowest for a COTS device. The overall gain of the front-end signal path is suitable and allows adapting the output signal level to the dynamic range of the ADC without saturation effects. The absence of EMG interferences has been confirmed by tests with pre-recorded neural signals (Fig. 2.13).

From the stimulation point of view, we demonstrated the capability of generating muscular twitches and the related electromyographic signals by injecting bi-phasic current pulses. Even if many other stimulation shapes have been investigated [8], the bi-phasic waveforms seem to be the best ones. As a matter of fact, monophasic stimulation leads to charge accumulation at the electrode-tissue interface and can cause tissue damages whereas bi-phasic stimulation ensures charge balancing thus preventing such problems [9]. Anyhow, the stimulation parameters are fully programmable and easily

reconfigurable by the user to meet changing requirements in real-time by means of a GUI. If needed, the firmware can be simply modified allowing generation of other kinds of stimuli.

A possible improvement is the implementation of parallel acquisition of all the 8 channels of the tf-LIFE. This requires replication of the analog front-end module made-up by the filter and the programmable amplifier. The estimated area for a board containing 8 parallel channels is around $15\text{cm} \times 15\text{cm}$ which corresponds to an increase of 161% of the present area. The increase is so small (around 2.5x) since the A/D conversion, the stimulation unit and the digital board would stay the same while replication of the input channels would allow to remove the bulky analog multiplexers. The drawback, of course, is an increase of power consumption which we estimate would reach 2.7W . Another useful improvement is further miniaturization of the system, that would be possible removing the self-test structures and the multiplexers required to implement the different operating modes. For what concerns the recording unit, the selectivity of the filter is important to reduce interferences but has the drawback of generating an impulse response with a large ringing effect, thus a proper trade-off should be envisaged. Looking at the spectral fingerprint of the acquired signals, it seems reasonable that the order of the high-pass filter could be reduced without affecting too much the recording capabilities and without picking up too many interferences. The effective resolution of 15 bits is enough to distinguish the neural signals from the noise floor. On the stimulation side, we proved that it is possible to evoke muscle responses even with stimuli of tens of microamperes; with animal experiments, what remains unanswered is the possibility of evoking sensorial feedback with such levels of currents. Finally, in view of the realization of a portable neuroprosthetic device, given the power consumption and size of the present board, the natural evolution seems to be the integration of recording and stimulation circuitry on a single integrated circuit. The results presented in this chapter have also been published in [10–13]

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Chapter 3

An Integrated Circuit for neural signal acquisition

In this chapter the design of an IC circuit for the recording module is described. After the design specification definition, the system design is presented. It has been developed on two different levels: a high level behavioral model for a rapid evaluation of the specification meeting and a transistor model for a slower but more accurate analysis. Finally the simulation results are presented and discussed.

3.1 Design Specifications

In the specification definition of the IC design we have taken into consideration the results of the developed COTS system. In particular, the problems with the filter ringing described in previous Chapter, have driven us toward an implementation characterized by a lower selective filter in the analog domain. This fact implies a worse rejection of the EMG noise, the huge interferences will be however completely eliminated after the digital conversion, by filtering the signal in the digital domain. In this implementation we propose, in fact, to keep the analog part as simple as possible and to move all the complexity on the digital domain. It is then necessary to decrease the gain of the analog filter in order to avoid the amplifier saturation; reasonable values for the gain are in a range from a minimum of $46dB$ to a maximum of $66dB$. The converter resolution requirements have also been changed, a 10 bit ADC, with a $V_{ref} = 1V$ is enough to obtain an $LSB=1.95mV$ which considering the maximum filter gain of $2000V/V$ results in a $977nV$ resolution referred to the input, which is lower than the noise floor of about $2\mu V$. Moreover, the filter bandwidth has been widened in order to investigate whether there is or

not neural content even at frequencies higher than $3kHz$. The specifications for recording module of the IC design are summarized in Table 3.1.

Fixed Gain	$46dB$
Variable Gain	$20dB$
HPF order	1^{th}
HPF frequency	$800Hz$
LPF order	1^{th}
LPF frequency	$8kHz$
ADC resolution	10 bit
IRN	$< 2\mu V$

Table 3.1: Recording module specifications

3.2 System architecture

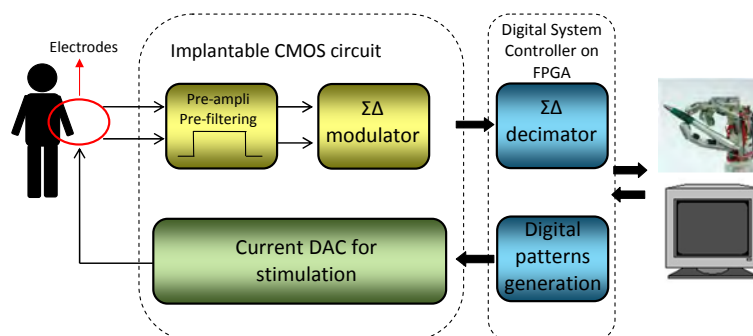


Figure 3.1: Block diagram of the recording and stimulation system

The block diagram in Fig. 3.1 shows the system architecture which is composed by two main blocks: the analog front-end and the digital processing unit. The front-end module works in a bidirectional way, it implements basic signal conditioning on the incoming neural signal (in recording mode) and provides current pulses on the feedback path (in stimulation mode). The signal is, thus, filtered and amplified by the pre-filtering/pre-amplifier block as close as possible to the recording site. In this way, the noise due to long cables and connection paths can be avoided. The conditioned signal is then converted into a 1-bit digital stream by the delta-sigma modulator and sent to the digital module for decimation and further processing. One of such

signal streams is needed for each input channel if the device is connected to a multichannel electrode. The digital module is hosted on an external board; it implements the decimation block of the sigma-delta converter altogether with the highly selective bandpass filter. The digital module is also responsible for the generation of digital programmable stimulation waveforms and for the management of the communication between the artificial limb and the electrodes. The digital unit will be implemented on programmable logic (FPGA), hosted on the robotic limb. A further advantage of such approach, is the possibility of changing the selectivity of the filter on the fly by adjusting the digital parameters. Considering the stimulation direction, digitally programmed current pulses will be created by the FPGA and sent to the Current DAC in the analog board to generate current patterns to be injected into the electrode.

The work presented in this Chapter is a part of the whole architecture design and concerns only the development of the analog recording unit, namely the band pass filter and the delta sigma modulator. The recording module design has been carried out parallel on two different levels: a behavioral model developed in Simulink and a circuitual design in cadence environment. The first model is needed to provide a first rapid check on the system behavior and to translate the specification of the whole system in the requirement that each single block must have, while for the physical realization of the device the transistor level simulation is mandatory. All the amplification chain has been designed using a fully differential topology, this approach in fact is the more suitable in a low noise design because helps in reducing the effect of the common mode noise sources in the circuit. Filter and modulator have been designed using a discrete time approach with switched capacitor circuits. This choice allows to reach a better precision in the filter cut-off frequency realization compared to the continuous time approach.

3.3 Behavioral model design

The introduction of a behavioral model is particularly useful in systems, like the proposed one, including sigma delta modulators and discrete time circuits. At a transistor level in fact, it is still possible to evaluate the frequency response for switched capacitor circuits using periodic analysis, but sigma delta modulators exhibit a non linear and non-periodic behavior and this makes it impossible to perform any analysis in the frequency domain (i.e. AC, noise etc). Transient simulations are then the only possible way to evaluate the sigma delta performances. The results are excellent but they are really time consuming, especially if, as in this case, also transient noise

analysis is required. The behavioral model allows to overcome these difficulties because describes reliably the circuit behavior using lower simulation time.

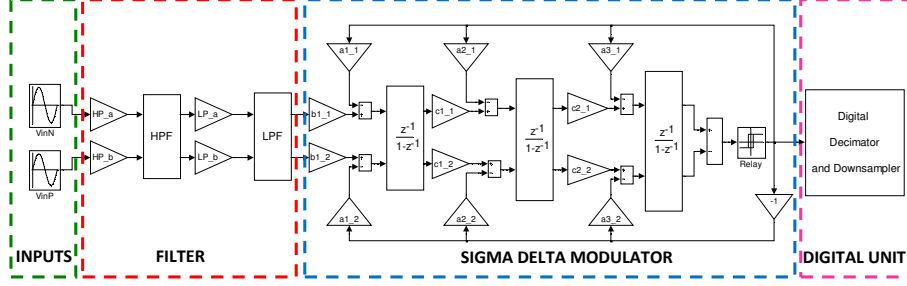


Figure 3.2: The Simulink schematic for the ideal behavioral model

The core of the behavioral model is composed by the high pass and low pass transfer function for the filter and by the integrators with weighted digital feedback for the sigma delta modulator. As it is shown in Fig. 3.2, the signal chain has been modeled using a fully differential approach. Even though the signal transfer function remains unchanged with respect to the single ended version, the double path is useful in view of non-ideal effect inclusion. In this way indeed it is possible to take into account the effect of capacitance mismatch generating mismatched coefficients for the two branches.

3.3.1 Filter behavioral model

The high pass and low pass filter transfer functions in the frequency domain (Equation (3.1) and Equation (3.2)) can be easily determined once that cut-off frequencies have been defined.

$$TF_{hp}(s) = \frac{\tau_{hp}s}{\tau_{hp}s + 1} \quad (3.1)$$

$$TF_{lp}(s) = \frac{1}{\tau_{lp}s + 1} \quad (3.2)$$

where $\tau_{hp} = 1/2\pi f_{hp}$ and $\tau_{lp} = 1/2\pi f_{lp}$ are respectively the high pass and the low pass time constants. The equivalent expressions for the discrete time domain can be obtained using the bilinear transform (or AKA Tustin's Method) based on the equivalence of Equation (3.3)

$$s \approx \frac{2}{T} \times \frac{z - 1}{z + 1} \quad (3.3)$$

the resulting transfer function are reported in Equation (3.4) and Equation (3.5).

$$TF_{hp}(z) = \frac{2\tau_{hp} - 2\tau_{hp}z^{-1}}{(2\tau_{hp} + T) - (2\tau_{hp} - T)z^{-1}} \quad (3.4)$$

$$TF_{lp}(z) = \frac{T + Tz^{-1}}{(2\tau_{lp} + T) - (2\tau_{lp} - T)z^{-1}} \quad (3.5)$$

Where T is the sample period (in our case $T = 488.28125ns$) and $\tau_{hp} = 1/2\pi 800$, $\tau_{lp} = 1/2\pi 8000$ are the filter time constants.

To this ideal model, several non-idealities sources have been added in order to make the simulation results as similar as possible to the real circuit behavior. First the transfer function has been inserted in a closed loop in order to take into account of finite gain, slew rate and saturation limitations (Fig. 3.3).

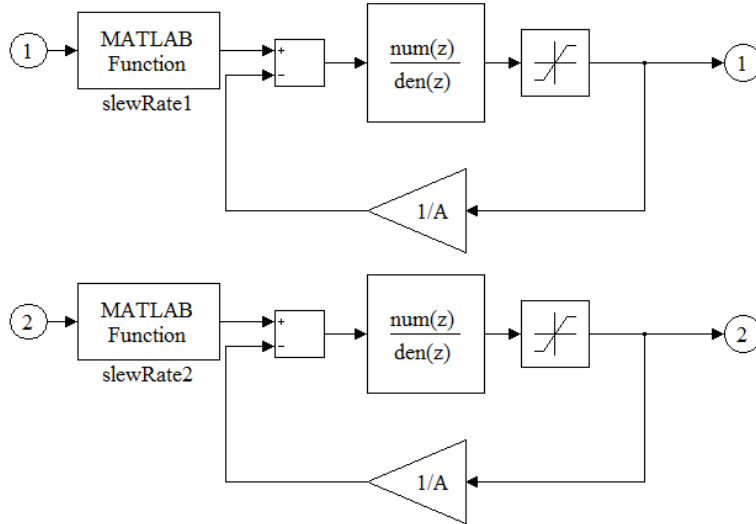


Figure 3.3: The Simulink schematic for the filter transfer functions including saturation, finite gain and slew rate effects

The closed loop transfer function is then expressed by Equation (3.6), where $TF(z)$ is the filter transfer function of Equations (3.1) and (3.2) and A is the finite gain of the open loop amplifier.

$$TF_{CL}(z) = \frac{TF(z)}{1 + \frac{TF(z)}{A}} \quad (3.6)$$

The slew rate limitation has been introduced exploiting a Matlab function taken from the "SD Matlab toolbox", available online (www.mathworks.com) [1]. The filter gain has also been introduced in the differential paths with the parameters LP_a , LP_b and HP_a , HP_b .

3.3.2 Delta Sigma modulator behavioral model

The delta sigma model is a modification of what presented in [1] and [2] which take into consideration saturation, slew rate, finite gain and bandwidth limitations. The coefficients of Fig. 3.2 are summarized in Table 3.2 and were chosen using the Schreier Toolbox [3] for a third order single loop with a 18-bits target resolution. The oversampling ratio that allows to reach the target resolution is $OSR = 128$ that, considering a signal band of $8kHz$ results in a sampling frequency $f_s = 2.048MHz$.

Coefficient	Value	Coefficient	Value
a_1	0.05	b_1	0.05
a_2	0.3	c_1	1
a_3	0.8	c_2	1

Table 3.2: Sigma delta modulator: coefficients

The single integrator schematic is represented in Fig. 3.4, and, with respect to the original model, was transformed in a fully differential architecture in order to make it more similar to the actual transistor implementation. The slew rate and the saturation blocks are the same used for the filter description, while the *alfa* parameter is given by $alfa = (A - 1)/(A)$ where A is the finite opamp gain.

3.3.3 Noise sources behavioral models

Several noise sources have been modeled in order to make the system as similar as possible to the transistor level system implementation. KT/C noise, thermal noise of the amplifier, switches non-idealities and clock jitter effects have been included, part of them are the same proposed in [1, 2], others as clock jitter and switch non idealities have been modified considering the fully differential approach. The mismatch effects were also taken into consideration: the coefficients in fact have been generated as ratios of capacitances, whose values have been obtained summing N base capacitance according to the final layout realization. Each value is extracted randomly from a normal distribution within a 6σ range around the nominal value. In each branch, independent random values have been used, granting the inclusion of mismatch effects in the model.

In the following a brief explanation of each non-ideality model is presented:

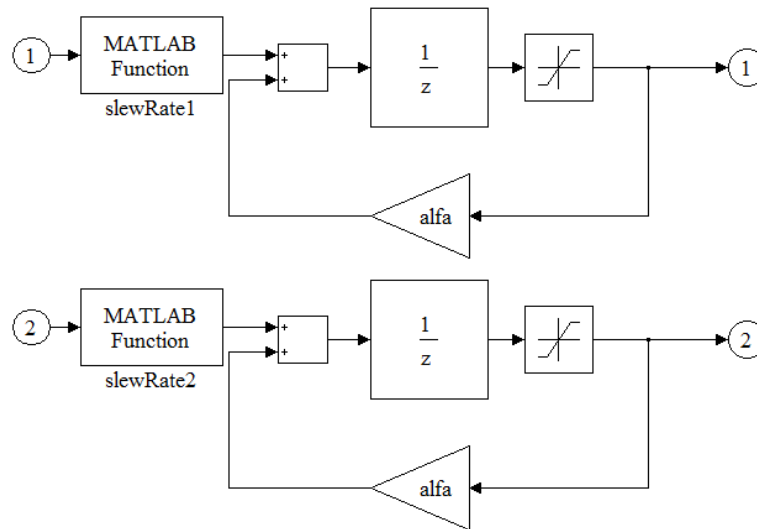


Figure 3.4: The Simulink schematic for the integrator including saturation, finite gain and slew rate effects

- **Opamp thermal noise.** The thermal noise of the amplifier has been modeled as a simulink block in which a normalized random signal is multiplied by the thermal IRN of the amplifier. From Fig. 3.5 it can be observed that a constant (equal to the integrator gain) multiplies the result; in this way we take into account that the input noise is subjected to the same amplification factor of the input signal.

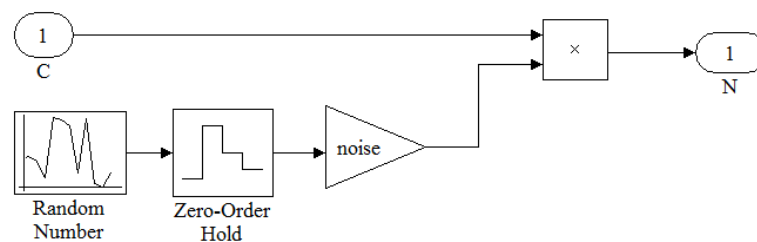


Figure 3.5: The Simulink schematic for the thermal noise block

- KT/C . This noise source is particularly important in switched capacitor circuits. The switches are typically implemented with MOS transistor and KT/C noise is due to the integration of the thermal noise of the switch. It is generated every time that a MOS is connected in series with a capacitance [4]. As shown in Fig. 3.6, it has been modeled as a random value multiplied by the noise expression calculated in eq. 3.7.

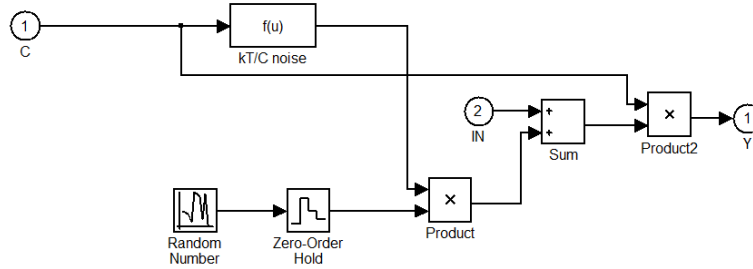


Figure 3.6: The Simulink schematic for the KT/C block

$$\overline{V_{n,rms}} = \sqrt{\frac{kT}{C_f \cdot G}} \quad (3.7)$$

Where k is the Boltzmann's constant, T is the absolute temperature, C_f is the feedback capacitor of the integrator and G is integrator gain.

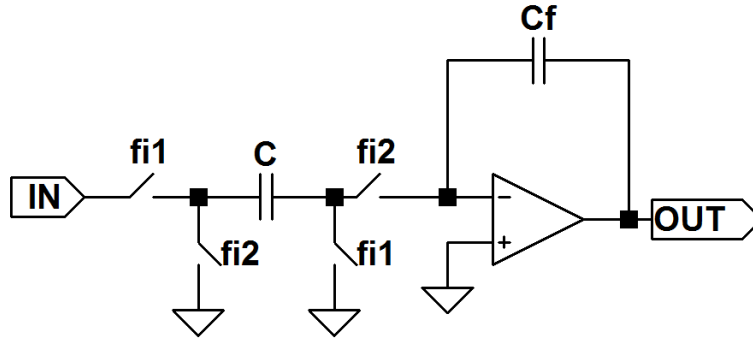


Figure 3.7: Integrator schematic for the KT/C noise calculation

Looking at Fig. 3.7 and considering that the gain is $G = C/C_f$, the expression of Equation (3.7) can be reduced to the classical KT/C form. The resulting noise is summed to the input signal and boosted to the output value with the multiplication by the integrator gain.

- **Switch noise.** The switch contribution to noise is mainly due to two different phenomena called charge injection and clockfeedthrough [5]. The charge injection is caused by the charge of the transistor channel. In fact, when the switch turns off this charge is partially moved into the capacitance connected to the switch, the presence of this extra-charge causes an error in the coefficient generation. The amount of charge in a triode NMOS switch is given by Equation (3.8) [5].

$$Q_{ch} = -WLC_{ox}V_{eff} \quad (3.8)$$

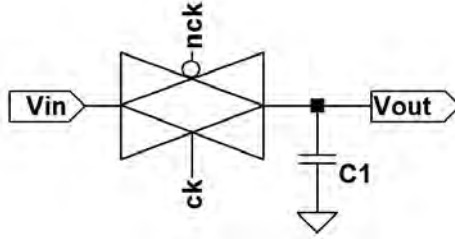


Figure 3.8: Charge injection due to switch

Thus, considering the simple circuit in Fig. 3.8, when the transmission gate switch is turned off, roughly half of the channel charge is injected into C (Equation (3.9))

$$\Delta Q = -\frac{1}{2}W_nL_nC_{ox}(V_{DD} - V_{in} - V_{tn}) + \frac{1}{2}W_pL_pC_{ox}(V_{in} - V_{SS} - |V_{tp}|) \quad (3.9)$$

resulting in an error on V_{out} given by Equation (3.10)

$$\Delta V = -\frac{1}{2C}[W_nL_n(V_{DD} - V_{tn}) + W_pL_p(V_{SS} + |V_{tp}|)] + \frac{1}{2} \frac{C_{ox}}{C} [W_nL_n + W_pL_p]V_{in} \quad (3.10)$$

The clock feedthrough is a phenomena due to the parasitic overlap capacitance between gate and source. This capacitance in fact is coupled to the main capacitor and causes an error on the output voltage calculated by Equation (3.11).

$$\Delta V = -(C_{ovn} - C_{ovp})V_{DD} \quad (3.11)$$

In Fig. 3.9, the Simulink model for switch non idealities is reported. It should be noted that the most worrying contribution is given by the input dependent term of charge injection that causes signal distortion.

- **Clock Jitter:** The error introduced by clock jitter is due to the finite slope of the clock edges. As shown in Fig. 3.10, where a simple sample and hold circuit is depicted, the source of the NMOS is connected to the input voltage while at the gate is applied the clock signal. The NMOS

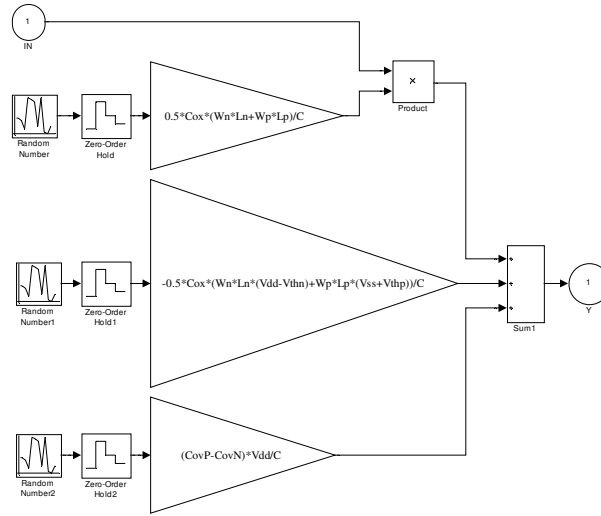


Figure 3.9: Simulink model for the switches non-idealities

is ON when the condition $V_{gs} > V_{th}$ is verified, which, in our case can be rewritten as $V_{ck} > V_{in} + V_{th}$. From Fig. 3.11 it is evident that the time instants (t_+ and t_-) in which $V_g > V_{inP} + V_{th}$ and $V_g > V_{inM} + V_{th}$ is different from the ideal sampling time (t_0) and this causes the ΔV_+ and ΔV_- errors in the sampled signals (actual samples are marked in green in the picture). The graphic shows a fully differential signal, as it can be observed, the error sign is the same in both cases, and, if the clock slope is high enough compared to the signal frequency, also the two amplitudes are quite similar, thus the error can be seen as a common mode noise and can be rejected taking the differential output [6, 7].

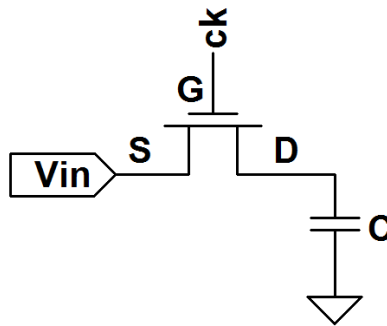


Figure 3.10: Sample and hold circuit

According to what reported in [1], considering a single ended system, the error in a sinusoidal signal $x(t)$ due to the time error δ can be modeled as:

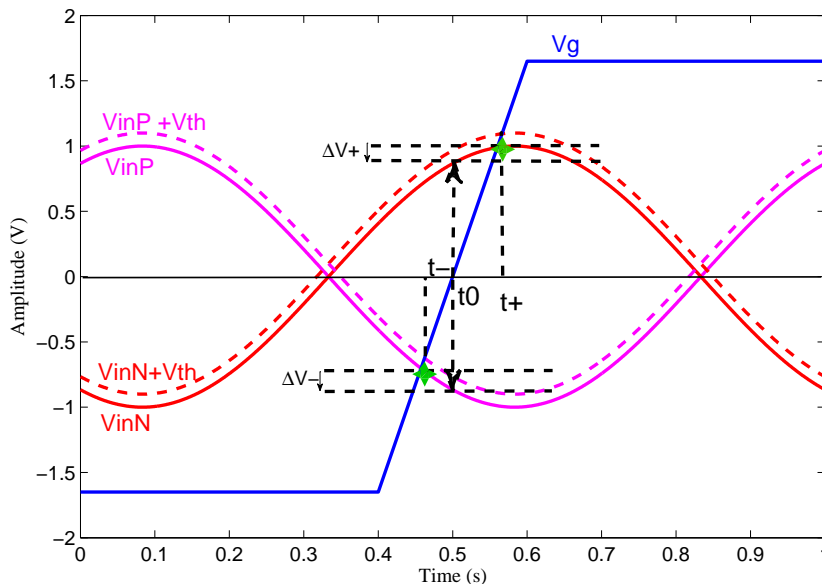


Figure 3.11: Error in signal sampling due to clock jitter

$$x(t + \delta) - x(t) = \delta \frac{d}{dt} x(t) \quad (3.12)$$

As explained, in a fully differential configuration it is particularly important to consider the correct error sign for a proper common mode noise rejection. Since this sign depends both on the rise direction (i.e. on the signal derivative) and on the jitter time sign, in the simulink model of Fig. 3.12 we added to the model proposed by Malcovati et al. [1] a part that takes into account whether the actual sample is taken before or after the ideal sample (i.e if the instantaneous value of $V_{in} + V_{th}$ is positive or negative).

In Fig. 3.13 the complete block diagram including all noise sources is reported, note that non-idealities blocks are concentrated mainly on first stages. The gain introduced in fact makes less critical the noise influence on the following stages and its effect can be neglected.

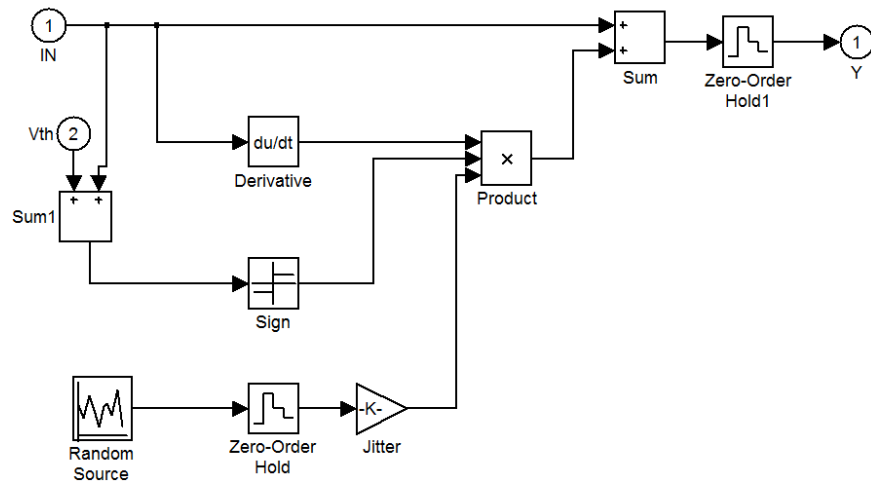


Figure 3.12: Simulink model for the clock jitter effect

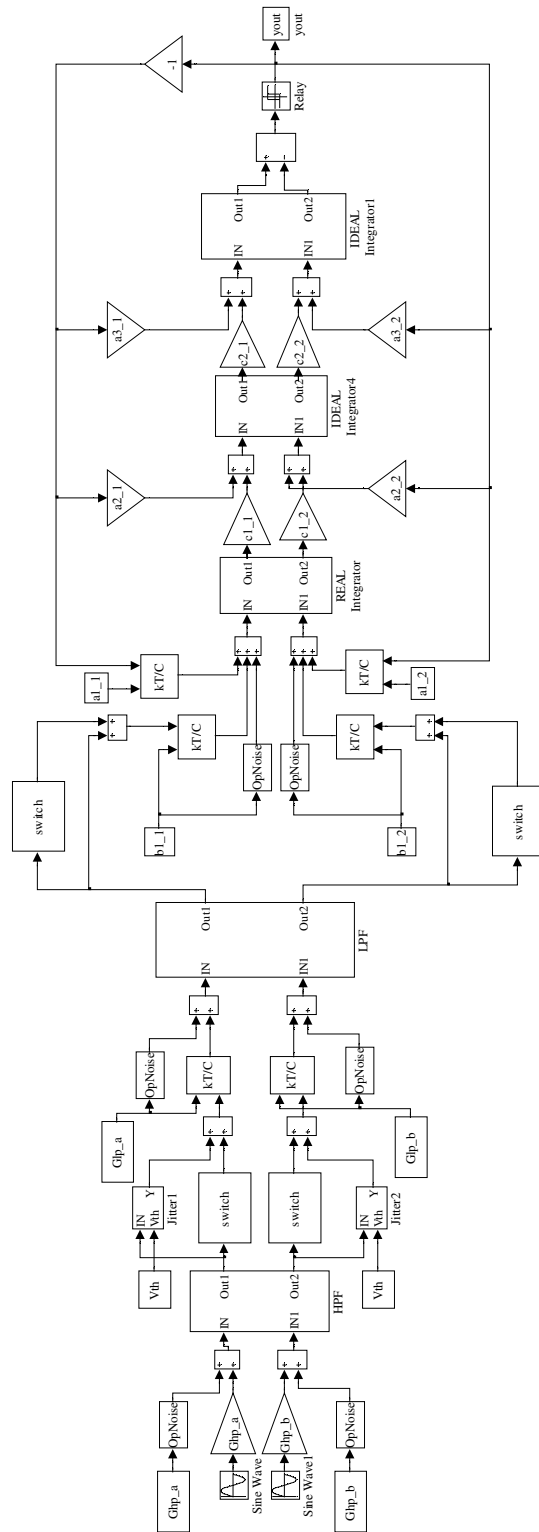


Figure 3.13: Simulink model of filter and modulator with noise sources

3.4 Transistor level circuitry design

The transistor level circuit was designed in a $0.35\mu\text{m}$ CMOS process from AMS (Austriamicrosystems) with double-poly capacitors, 3.3V power supply and 4 metal layers. Area, power and noise constraints are particularly compelling since the chip must be integrated with the electrode and implanted in the patient stump, our main aim is then to find a good compromise among these requirements.

3.4.1 Bandpass Filter design

Fig. 3.14 shows the pre-amplifier/pre-filtering block that was implemented with a first order Switched Capacitor (SC) filter. The bandpass filter was realized cascading a highpass filter with a lowpass filter; the highpass is used as first stage in order to start rejecting the EMG interferences as close as possible to the electrode, before any amplification.

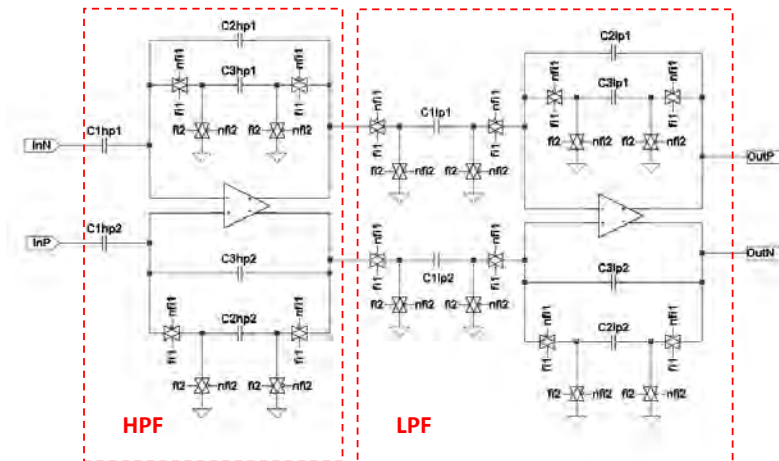


Figure 3.14: Bandpass filter

The filter specifications required a bandwidth between 800Hz and 8kHz and a minimum gain of 200V/V . These parameters can be achieved choosing proper values for capacitances and clock frequency according to the expressions of Table 3.3.

The gain value has been determined in order to maximize the amplification at neural frequencies avoiding the risk of amplifier saturation due to the high amplitude of EMG interferences. According to what reported in literature in fact, the EMG amplitude can reach, at 100Hz up to 50mV [8], since the maximum signal swing allowed is 2V (due to sigma delta reference

	HPF	LPF
Gain	$\frac{C1}{C3}$	$\frac{C1}{C2}$
cut off freq.	$\frac{f_s C3}{2\pi C2}$	$\frac{f_s C3}{2\pi C2}$

Table 3.3: Equations for filter gain and cut-off frequency

voltage), the maximum acceptable gain at $100Hz$ is $100V/V$, resulting in a $200V/V$ gain in the neural bandwidth.

C	Value [pF]	C	Value [pF]
$C_{1hp1,2}$	70	$C_{1lp1,2}$	3.3
$C_{2hp1,2}$	17	$C_{2lp1,2}$	2.7
$C_{3hp1,2}$	0.06	$C_{3lp1,2}$	0.05

Table 3.4: Filter Capacitance values

In Table 3.4 the capacitance values used in the minimum gain configuration are summarized. Since the reported value for the *EMG* interference is assessed in worst case conditions, a higher gain can be useful in order to increase further the neural signal level and to achieve a better resolution in normal case conditions. Hence, a programmable gain has been introduced, it is possible to modify the gain with 256 different levels reaching a maximum of $66dB$. For this purpose a switch network connects a rank of capacitors to the main components C_{1hp} and C_{1lp} , *8bit* are used to configure this network, 2 bits for the HPF, bringing the maximum C_{1hp} value to $140pF$ and 6 bits for the LPF are used to increase the C_{1lp} capacitance value up to $34.8pF$. In Fig.3.15, the part of schematic regarding the filter programmability is reported, C_{1hp} and C_{1lp} values are respectively $70pF$ and $3.3pF$ (as indicated in Tables 3.4) while $C_{var_{hp}} = 17.5pF$ and $C_{var_{lp}} = 500fF$. All reported values have been realized using multiples of the minimum capacitance used in the stage (i.e. $60fF$ for the *HPF* and $50fF$ for the *LPF*)

A simple cascade symmetrical OTA (Fig. 3.16) was chosen for the operational amplifier implementation and it was carefully dimensioned in order to minimize the input referred noise. Flicker noise is one of the major concerns, given the low frequencies of the neural signal, thus a p-type differential pair with large area was adopted to minimize this contribute [4]. Thermal noise was addressed using a large g_m for the differential pair and reducing

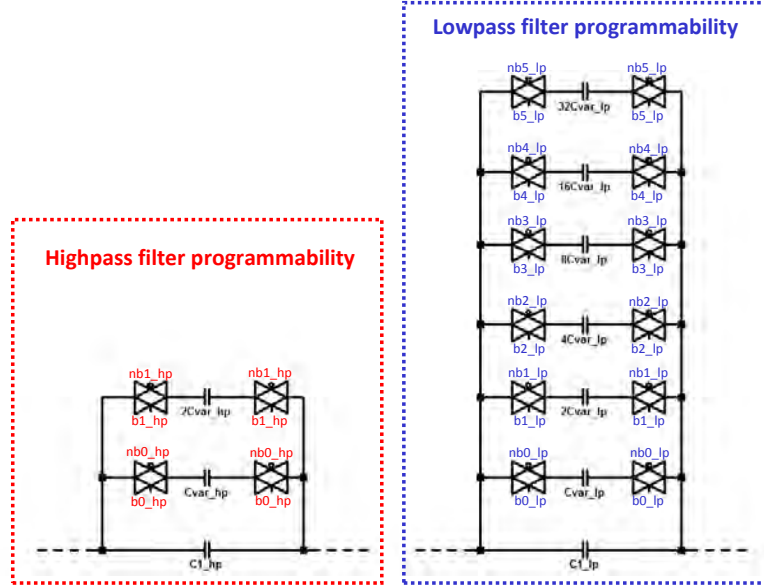


Figure 3.15: Circuitry design of filter programmability

the g_m of the output branch transistor [9] according to the formula 3.13. As explained in Chapter 1, this result has been achieved by putting the differential pair in the weak inversion region and the current mirror transistors in strong inversion.

$$v_{n,th} = \frac{16kT}{3g_{m1}} \left(1 + \frac{g_{m6}}{g_{m1}} + \frac{g_{m8}}{g_{m1}} \right) \quad (3.13)$$

where k is the Boltzmann constant, T the absolute temperature and g_{mx} the transconductance of transistor x . In Table 3.5, all sizes are reported, all transistors were biased with a $12.5\mu A$ current using the lower gain configuration, when the gain rises also the current can be increased proportionally in order to meet the GBW requirements. A passive SC common mode feedback block was used for power saving (Fig. 3.17), $4pF$ capacitance have been chosen in order to have a refresh time sufficiently long, this value also helps to have better performances in terms of stability.

3.4.2 Modulator circuitry design

The block diagram described in Section 3.3 was mapped into a transistor level design using a SC circuit. The main components are the discrete time integrators shown in Fig. 3.18 (first stage) and Fig. 3.19 (second and third stages). It can be observed that all the feedback paths have been realized driving a switch with the quantizer output and connecting the corresponding

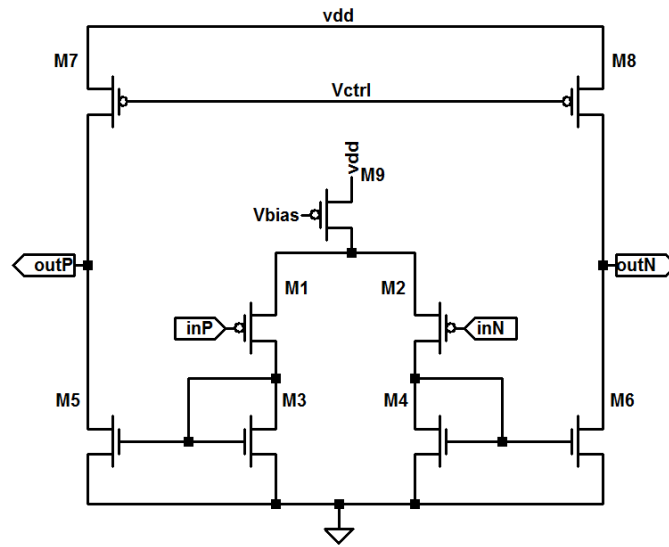


Figure 3.16: Symmetrical OTA

	$\frac{W}{L} \left[\frac{\mu\text{m}}{\mu\text{m}} \right]$		$\frac{W}{L} \left[\frac{\mu\text{m}}{\mu\text{m}} \right]$
$M_{1,2}$	$\frac{400}{2}$	$M_{7,8}$	$\frac{64}{21}$
$M_{3,4,5,6}$	$\frac{4}{8}$	M_9	$\frac{128}{21}$

Table 3.5: Dimensions of the OTA used in the filter

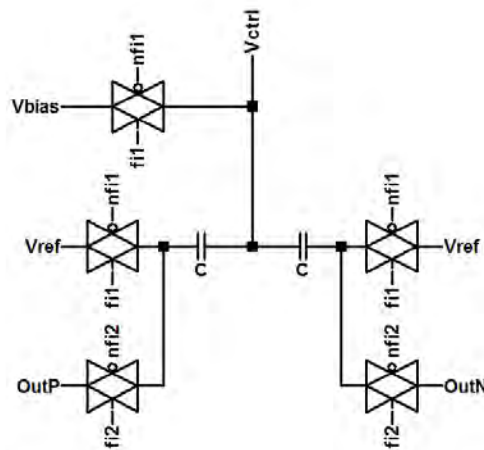


Figure 3.17: Common Mode Feedback schematic

capacitor to the reference voltages $V_{ref-} = V_{dd}/2 - 1$ and $V_{ref+} = V_{dd}/2 + 1$. Since the a and b coefficients are equals, in the first stage the same capacitor was shared for the two paths while in the second and third stage two different capacitors were used in order to implement coefficients a and c .

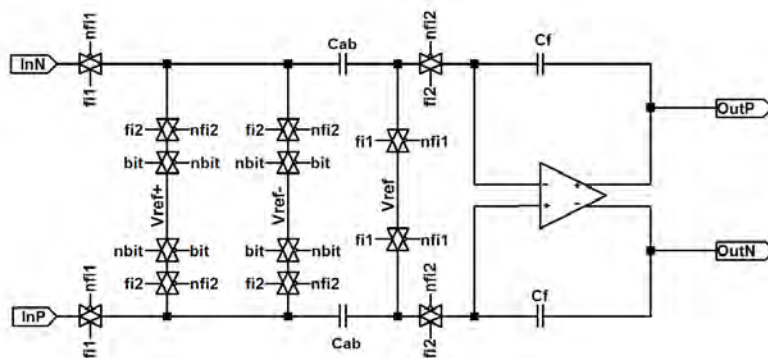


Figure 3.18: Sigma-delta modulator: first integrator schematic

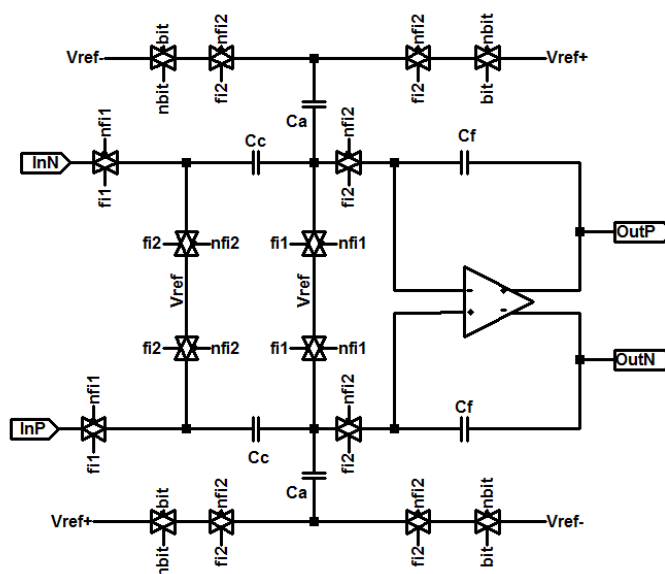


Figure 3.19: Sigma-delta modulator: second and third integrator schematic

In Table 3.6, all the values used for the capacitors are reported, each coefficient of Table 3.2 can be obtained by capacitance ratios using the relationship $x = C_x/C_f$. A simple symmetrical OTA was used to realize the operational amplifier (the same topology reported in Fig. 3.16 for the filter OTA has been used), it has been sized in order to meet the specifications

determined with the behavioral simulation (in terms of DC gain, GBW, dynamic range and slew rate) the transistor sizes are reported in Table 3.7. The single bit quantizer has been designed with the track and latch circuit shown in Fig. 3.20.

C	Value [pF]	C	Value [pF]
$C_{ab,1st}$	0.4	$C_{f,2st}$	8
$C_{f,1st}$	8	$C_{a,3st}$	6.4
$C_{a,2st}$	2.4	$C_{c,3st}$	8
$C_{c,2st}$	8	$C_{f,3st}$	8

Table 3.6: Sigma-Delta modulator: capacitance values

	$\frac{W}{L}$ [μm]		$\frac{W}{L}$ [μm]
$M_{1,2}$	$\frac{107}{11}$	$M_{5,6}$	$\frac{10}{1}$
$M_{3,4}$	$\frac{1}{1}$	$M_{7,8}$	$\frac{15}{5}$

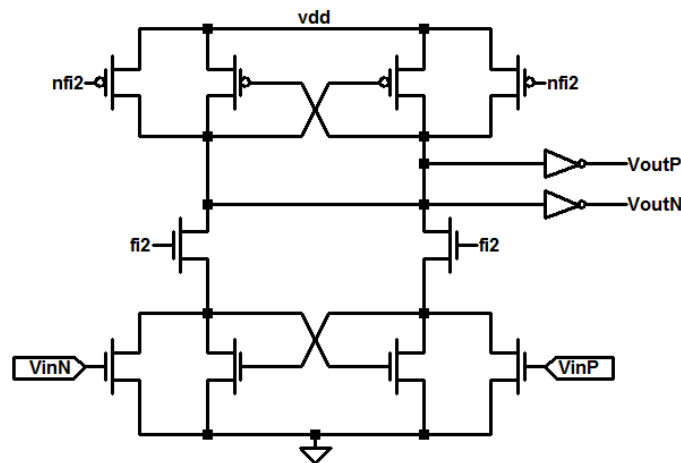


Figure 3.20: 1-bit quantizer circuitual implementation

In Fig. 3.21 a global view of the modulator schematic with the cascade of the three integrators is depicted.

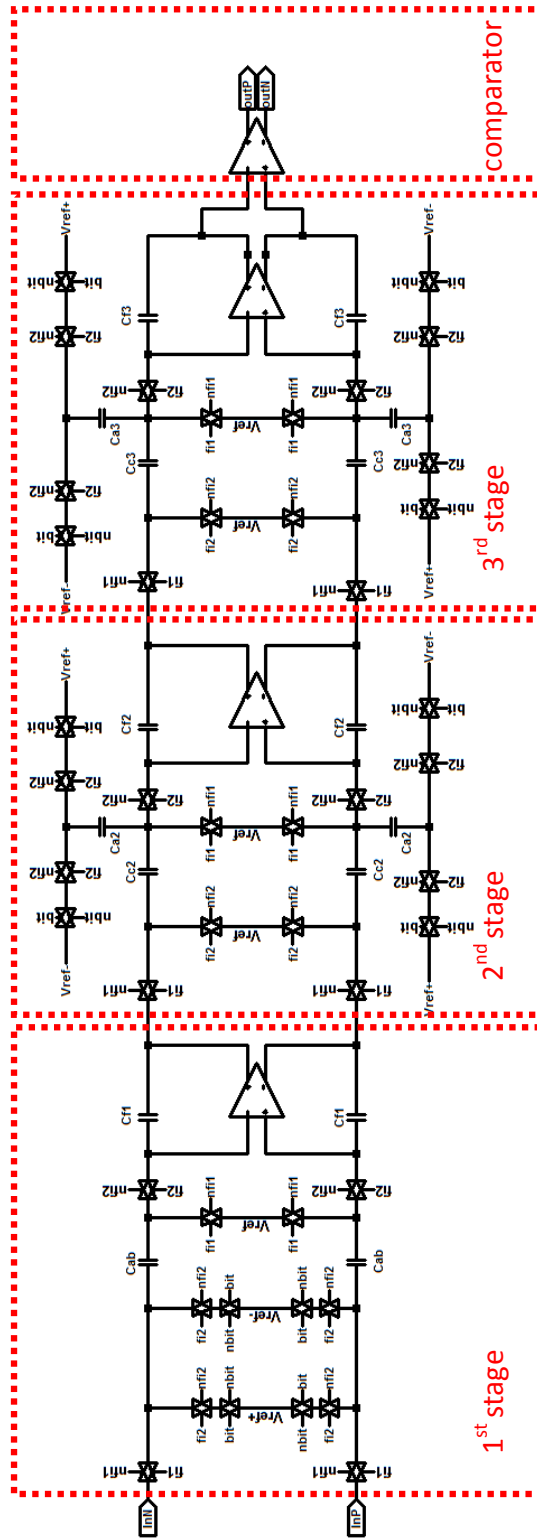


Figure 3.21: Sigma Delta Modulator: circuitual schematic

3.5 Experimental results

In this Section, the simulation results are shown: first the results obtained by means of behavioral simulation are discussed, then those achieved with the transistor model developed are presented.

3.5.1 Behavioral simulation results

The possibility to perform behavioral simulations is particularly useful because, as already stated, allows to avoid the long transistor level simulations in first steps of design and to define the specifications for each base block. High level simulations have been helpful to define the amplifier parameters: DC gain, GBW, IRN, slew rate and also to determine which are the minimum capacitance dimensions that allow to achieve a noise level below the desired threshold. The transistor level design has been guided by the specifications obtained in this design phase which are summarized in Table 3.8. The results presented in this section have all been calculated using these parameters.

Filter OTA		Modulator OTA	
DC gain	67.7dB	DC gain	56dB
GBW	7.8MHz	GBW	11MHz
noise	1.7 μ V _{rms}	noise	15 μ V _{rms}
slew rate	50V/ μ s	slew rate	50V/ μ s

Table 3.8: OTA parameters used in simulink simulations

The bandpass filter has been tested setting as input sinusoidal signals at different frequencies, the frequency response obtained is reported in Fig. 3.22, the gain obtained, 47.5dB, is slightly higher than expected but still acceptable as a good compromise between minimal neural amplification and saturation avoidance. The 3dB cut off frequencies are 800Hz and 8kHz as predicted by the filter transfer functions.

The ideal Power Spectral Density (PSD) of the modulator is shown in Fig. 3.23, the plot has been obtained using only the cascade of the three ideal integrators, without taking into account non-ideality effects. The results show as, with an input at 2.7kHz with a 0.5V amplitude, the modulator grants to achieve a $SNR = 98dB$ corresponding to an ENOB of 16 bit.

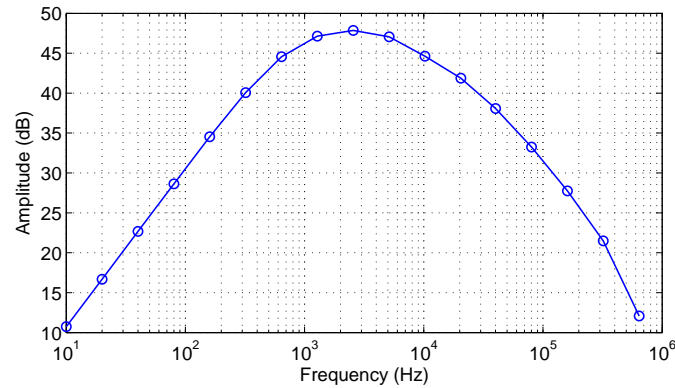


Figure 3.22: Bode diagram obtained with simulink model

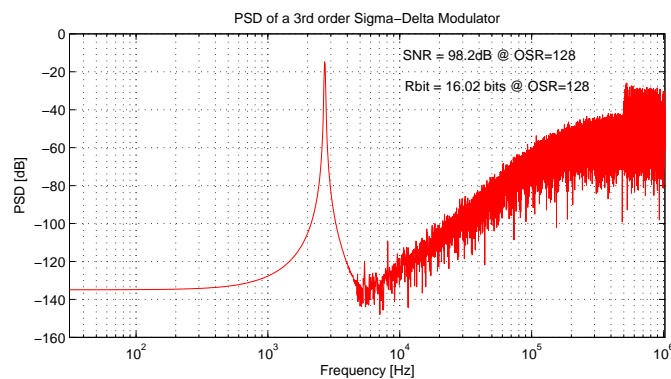


Figure 3.23: Sigma delta modulator: power spectral density of the ideal model

PSD results obtained simulating all the recording chain (filter + modulator) and that include also all the noise sources show a deep degradation in terms of resolution, leading to a $SNR = 56dB$ corresponding to a 9 bit converter resolution. The plot has been obtained using a filter input with an amplitude of $2mV$ at $2.7kHz$. The main contribute is due to the switches non-idealities, it should be clear that in any case this is a worst case estimation (for instance half of the MOS channel charge is supposed to be injected into the capacitance) and that in real implementation we expect to have better noise performances.

Fig. 3.25 represents the system response in terms of SNR to the changes

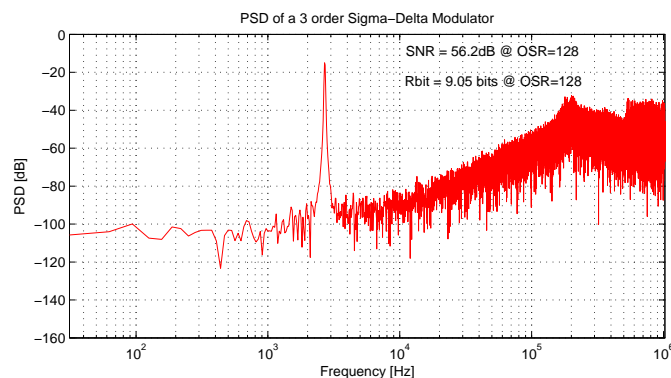


Figure 3.24: Sigma delta modulator: Power spectral density of the complete real model

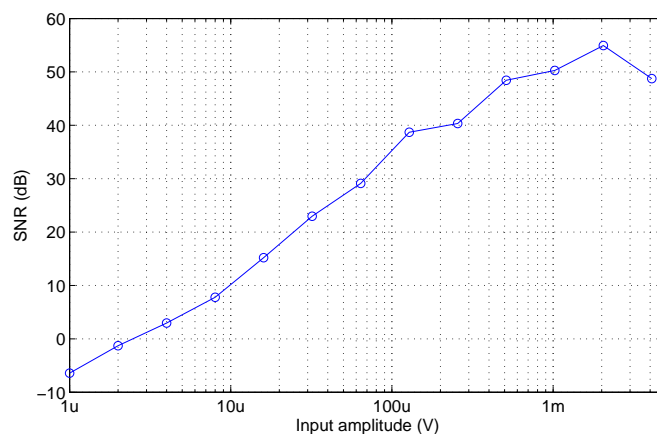


Figure 3.25: Signal to Noise Ration variations with different signal amplitudes

in input signal amplitude, as expected the SNR increases for increasing input amplitudes and starts to degrade when a $2mV$ input amplitude is selected. This value in fact correspond to a modulator input of $0.5V$, i.e. $V_{ref}/2$ and for inputs higher than half V_{ref} , sigma delta modulators performances drop drastically [3]. It can be observed that the minimum detectable signal (corresponding to $SNR = 0dB$) is equal to $2\mu V$ that is the noise level indicated in Section 3.1 as target noise level.

In order to evaluate the system capability to work with real neural signals, the whole system has been tested with a pre-recording neural signal extracted in clinical trials from the PNS of a rabbit subjected to cutaneous afferent stimulation at $50Hz$ and $100Hz$, the resulting stream of bit have

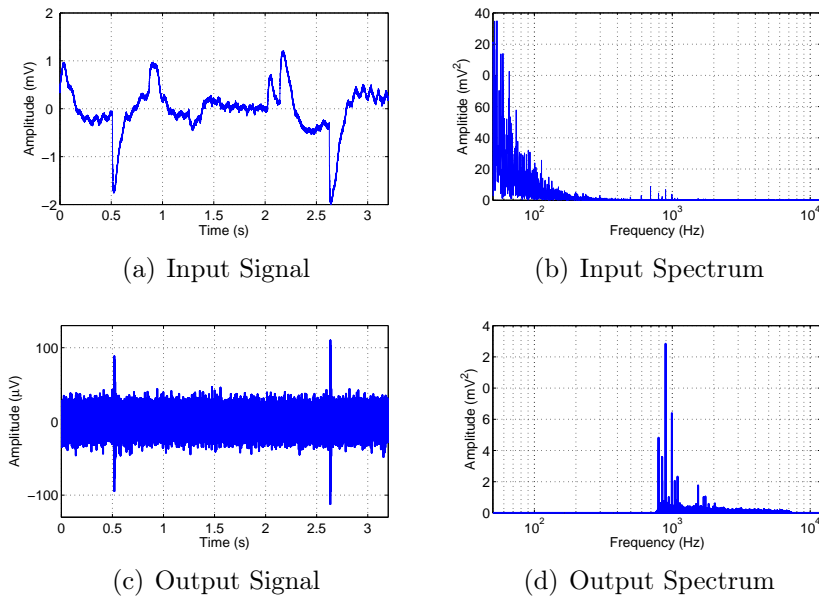


Figure 3.26: Sigma Delta modulator: pre-recorded neural signal processing

been filtered with an ideal matlab filter that decimates the output band-pass filtering the out of band interferences. The input pattern, represented in Fig. 3.26(a), corresponds to 3.2 seconds of recording. The input signal is affected by EMG and ECG interferences with a very large amplitude (in the millivolts range) and a spectrum (Fig. 3.26(b)) concentrated below 300Hz. Such interferences completely mask the underlying neural content. The signal has been processed by the delta-sigma modulator and then decimated and band-pass filtered using a digital filter in simulink environment. Fig. 3.26(c) displays the input-referred output signal and Fig. 3.26(d) its power spectral density: the low-frequency interferences are completely removed and the weak neural signal (in the microvolts range) is now visible, as well as its frequency signature.

3.5.2 Transistor level simulation results

Once that a first "operating point" has been achieved with the coarse behavioral simulations, more accurate analysis can be performed at transistor level. Concerning the filter implementation, first a circuit capable of meeting the target specifications presented in Table 3.8 has been designed. As shown in Fig. 3.27, the specifications have been met. For the sake of completeness, in Table 3.9 both the low pass and high pass parameters are reported, in fact,

having different loads, they exhibit a slightly different behavior in terms of bandwidth and phase margin.

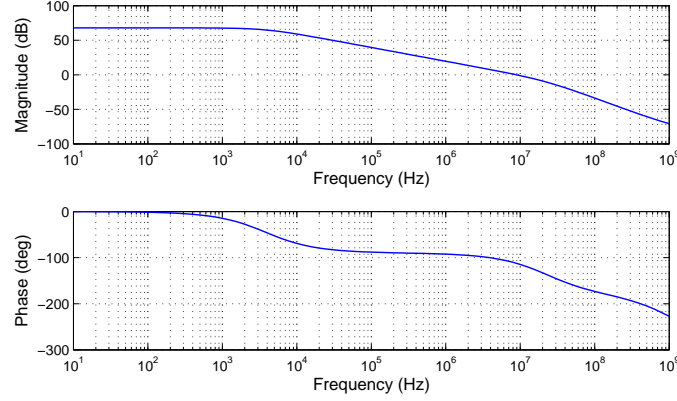


Figure 3.27: Bode diagram of open loop high pass filter amplifier

	LPF OTA		HPF OTA
DC gain	67.7dB	DC gain	67.7dB
GBW	5MHz	GBW	7.8MHz
noise	1.64 μV_{rms}	noise	1.64 μV_{rms}
slew rate	54V/ μs	slew rate	54V/ μs
phase margin	72.8 $^{\circ}$	phase margin	64.1 $^{\circ}$

Table 3.9: OTA parameters resulted from transistor level simulations

The frequency response of the programmable filter is reported in Fig. 3.28, the gain filter can be programmed with 256 possible values covering the range from 45.5 dB (red curve) to 63 dB (blue curve). The filter bandwidth has been optimized for the lower gain configuration, in this case in fact the 3dB bandwidth is in the range 780Hz – 8kHz, the gain increase causes a slight extension on the low cut off frequency that becomes $f_l = 680Hz$. Since we are using a first order filter, the error is small and can be easily eliminated with the high selective filter implemented with the digital decimator,

moreover, if the EMG interferences were high enough to cause amplifier saturation, the gain reduction could fix the problem.

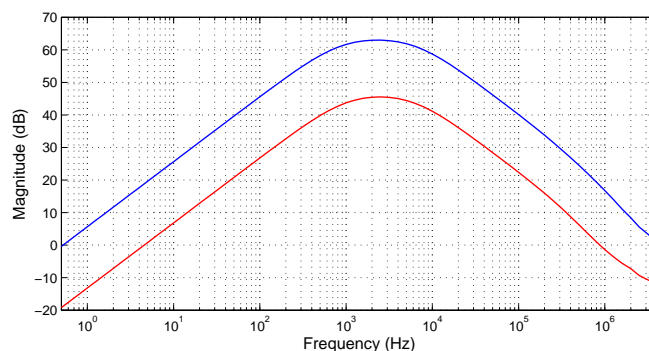


Figure 3.28: Bode diagram of the band pass filter. Red curve, minimum gain. Blue curve, maximum gain

The plot in Fig. 3.29 represents all the possible values for the programmable gain, the four possible ranges correspond to the four possible combinations in the high pass filter (2 bits have been used to control the HPF programmability Fig. 3.15), each interval is composed by 64 different values corresponding to 64 different C_1 values in the low pass filter circuit.

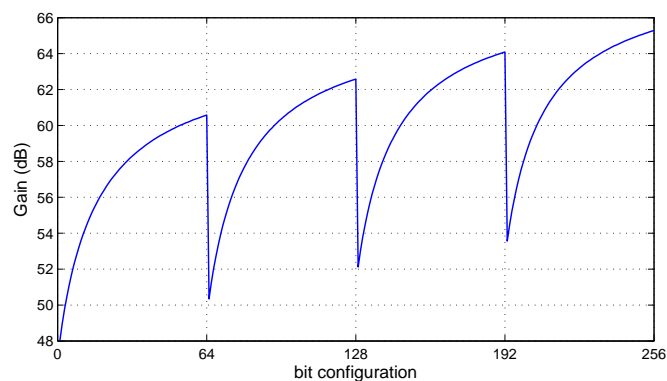


Figure 3.29: Programmable gain values vs bit configuration

The OTA used in the three integrators of the modulator has been designed according to the parameters coming from the behavioral simulation and presented in Table 3.8. In Fig. 3.30, the open loop frequency response of the amplifier is shown, the main parameters are summarized in Table 3.10.

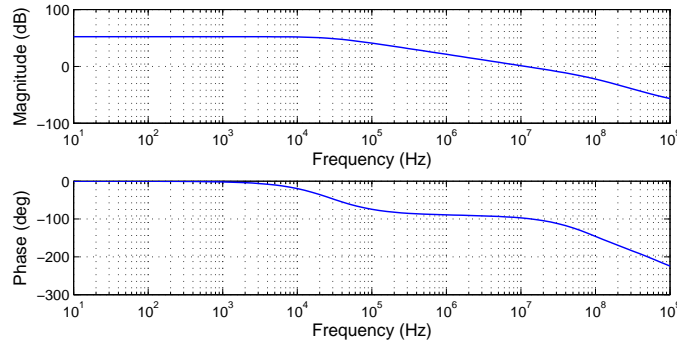


Figure 3.30: Bode diagram of open loop modulator filter amplifier

Modulator OTA	
DC gain	$56dB$
GBW	$11.6MHz$
noise	$14.7\mu V_{rms}$
slew rate	$54V/\mu s$
phase margin	81.7°

Table 3.10: Modulator OTA parameters resulted from transistor level simulations

The modulator resolution has been tested using an input signal with a frequency in the neural bandwidth and with an amplitude equal to half the modulator reference voltage (higher amplitudes cause modulator saturation). The modulator output has been saved on a data file and processed with a Matlab function that plots the PSD and calculates the SNR with the corresponding ENOB. In Fig. 3.31 the result obtained running ideal simulations using spectre simulator in cadence environment is reported: the resolution obtained is 16 bits, in a good agreement with what obtained with the behavioral simulation and displayed in Fig. 3.23.

The performances degrade when noise is taken into account in transient analysis. This leads to a $SNR=71.2dB$, that corresponds to a $ENOB = 11.54bit$ (Fig. 3.32).

In Fig. 3.33, the PSD obtained simulating the complete amplification chain composed by the pre-amplifier/pre-filtering block and by the modulator is reported. The signal set as filter input is $2.3mV$ which, considering a $200V/V$ gain, results in a modulator input of roughly $0.5V$. As expected the resolution is further reduced and the system exhibits a $ENOB=10.22$

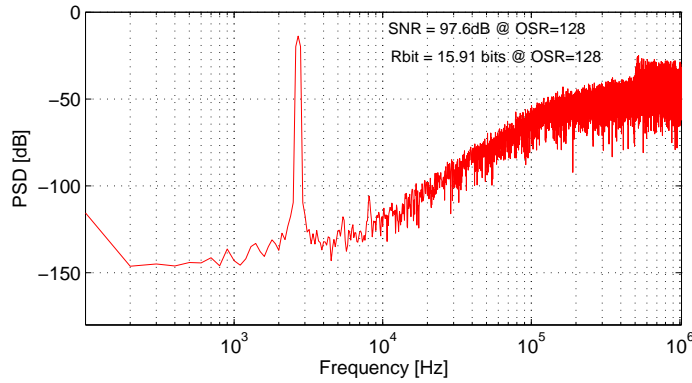


Figure 3.31: Ideal PSD of the modulator with a $0.5V$ amplitude and $2.7kHz$ frequency input signal

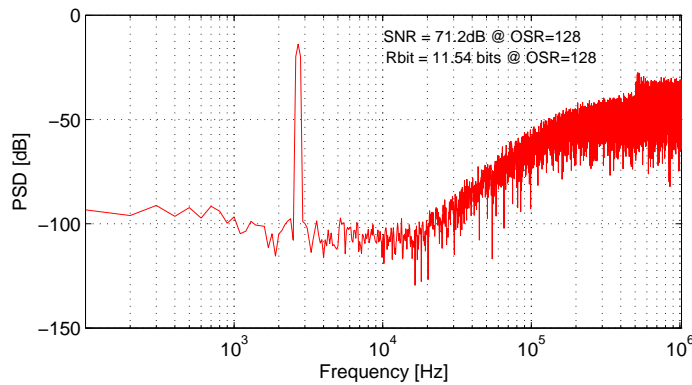


Figure 3.32: PSD of the modulator with a $0.5V$ amplitude and $2.7kHz$ frequency input signal considering the noise effects

bits which is in any case compliant with the specification of 10 bit resolution defined in Section 3.1.

The modulator SNR in response to different amplitudes of input signals is shown in Fig. 3.34, the relation between SNR and input signal is perfectly linear for small signals and starts to saturate for amplitudes higher than $2.3mV$ referred to the filter input (i.e. a modulator input greater than $0.5V$ which corresponds to the half of the reference voltage). The quantization noise floor, corresponding to the $SNR=0dB$ is about $1.5\mu V$ which is under the level of the OTA input referred noise. The whole recording chain has been tested setting as filter input the sum of three sines at three different

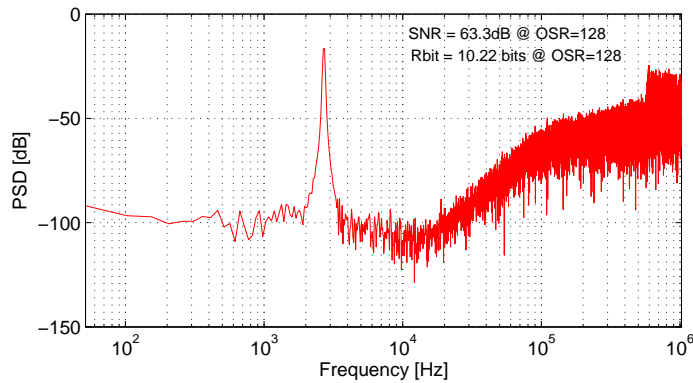


Figure 3.33: PSD of the filter and modulator with a $2.3mV$ amplitude and $2.7kHz$ frequency input signal considering the noise effects

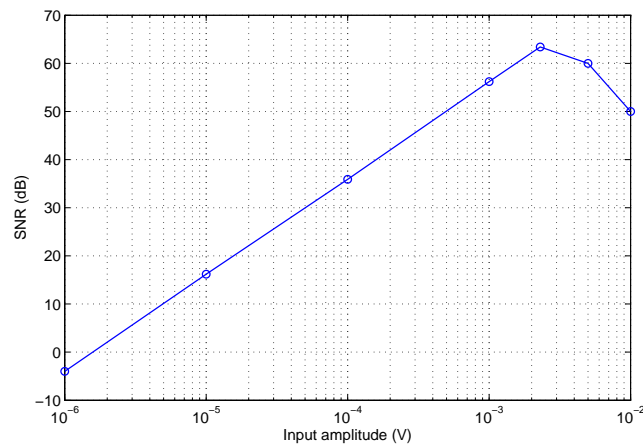


Figure 3.34: SNR calculated for different amplitudes of the filter input signals

frequencies representing the neural signal and the noise sources with realistic amplitudes and frequencies. A $100\mu V$ signal at $2.7kHz$ has been used to emulate the neural signal while two components with an amplitude of $1mV$ at $100Hz$ and $16kHz$ has been used as out of band interferences. The input signal in the time and frequency domain is shown in Fig. 3.35(a) and Fig. 3.35(b). The signal has been pre-filtered and pre-amplified by the analog block before being converted in a 1bit stream by the delta sigma modulator. The resulting signal is shown in Fig. 3.35(c) in the time domain, while the PSD can be observed in Fig. 3.35(d): the three components are still de-

tectable and, as expected, the $2.7kHz$ component has been amplified more than the two out of band signals. The noise shaping effect due to the delta sigma modulator is also evident. In order to remove the unwanted components, the signal has been decimated with a 32^{th} order IIR Butterworth filter implemented in a Xilinx Virtex 5 LX330 FPGA. The results in time and frequency domain are reported in Fig. 3.35(e) and Fig. 3.35(f), it is evident how the unwanted components are completely filtered out and only the in band frequency, amplified by the $45.5dB$ filter gain is allowed to pass.

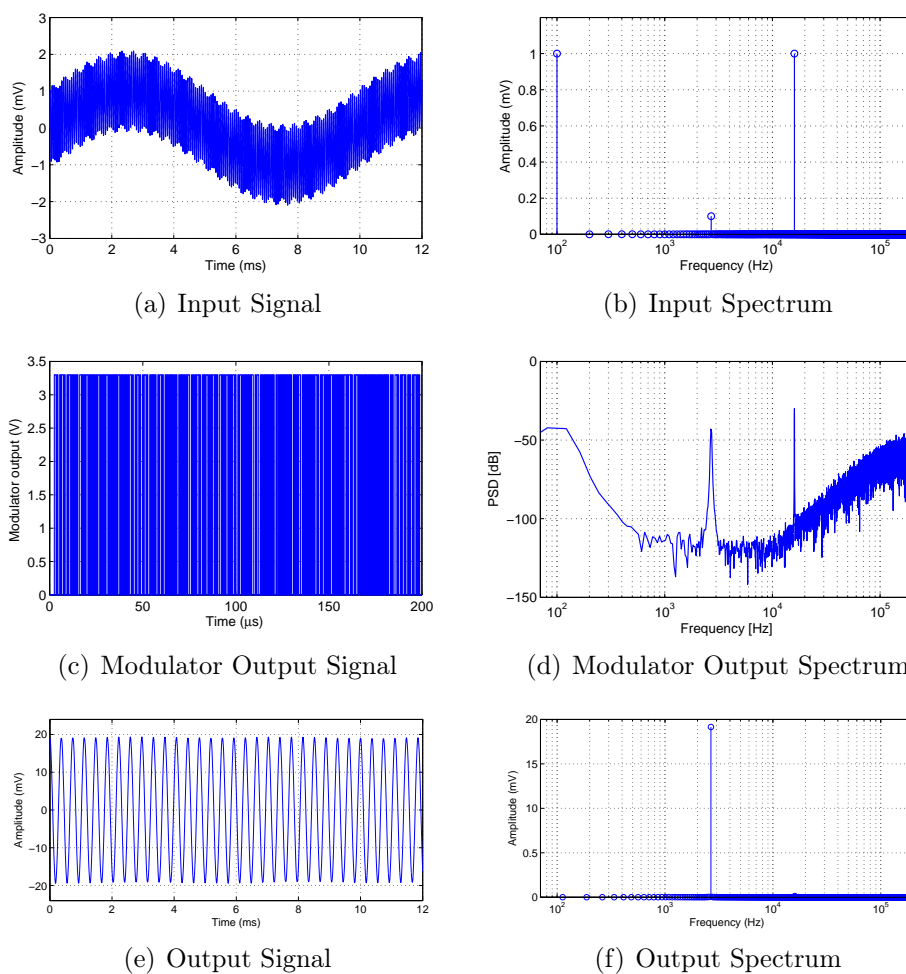


Figure 3.35: Recording chain response to an input composed by the sum of three sines at $100Hz$, $2.7kHz$ and $16kHz$

Finally in Table 3.11, the main characteristics of the IC recording circuit are summarized. The device is able to detect neural signals as low as

Recording module characteristics	
Total Gain	46 – 66dB
Bandwidth	800Hz – 8kHz
IRN	1.67 μ V _{rms}
Power (1 ch.)	2.5 – 3.4mW
Area (1 ch.)	1.6mm ²

Table 3.11: IC recording module: main parameters summary

2 μ V, filtering them in a 800Hz – 8kHz bandwidth and providing a programmable gain able to boost the signals up to millivolts level for a proper 10 bits resolution digital conversion. The simulated input referred noise is 1.64 μ V_{rms} achieved with a maximum 3.4mW power consumption for each recording channel. The power consumption can be reduced, in the lower gain configuration, to 2.5mW. The area occupied by each channel is roughly 0.8mm².

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Chapter 4

Ion channel readout interfaces based on patch-clamp circuits

In previous sections, a deep analysis on methods and circuits for neural signals spikes recording has been presented, the approach proposed in this chapter is slightly different and it is aimed to investigate on elementary electrochemical variations in biological cells that make possible the spikes generation and their propagation along the nerve. As explained in Chapter 1, the electrical spikes in biological cells arise from gradients of concentration of ion species. In the case of neural signals the major role is played by Sodium (Na^+) and Potassium (K^+) ions, their movement from one side to the other of the cell membrane generates ion currents. In the following, the system level design of a circuit capable of detecting such ion channel currents is presented.

4.1 Design specifications

The ion current amplitude strongly varies depending on the number of channels involved in the electro-chemical reaction, the range of interest covers values from 1pA , for a single channel current detection, to the mA order of magnitude for multi-channel current recording. Thus, the recording system must be able to operate over six decades and must be characterized by a 120dB of dynamic range. Different solutions can be implemented to address these problems (see Chapter 1), the one proposed in this work is based on current mode delta sigma converter. The wide 120dB dynamic range results in a 20 bit converter resolution to which 1 – 2 bits of noise margin should be added. A design based on a one range solution is possible but implies high sampling frequency and high power consumption. It has then been chosen a

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double range approach in which a modulator with a $60dB$ dynamic range can be reconfigured in order to operate in the two different ranges $1pA - 1nA$ and $1nA - 1\mu A$ depending on which kind of recording is required. A continuous time sigma delta modulator has been used, for a first coarse evaluation of the modulator order and of the OSR needed to achieve the target resolution, the analytic expression of Equation (4.1) can be used [1].

$$SNR_{peak} = \frac{3\pi}{2}(2^B - 1)^2(0.5)^2(2n + 1)\left(\frac{OSR}{\pi}\right)^{(2n+1)} + 20\log(k_q \prod_i k_{s,i}) \quad (4.1)$$

B is the signal bandwidth ($10kHz$ in this case), n is the modulator order, OSR is the oversampling ratio while k_q and $k_{s,i}$ are respectively the quantizer gain and the continuous time modulator coefficients. Several trials using second and third order modulators have been done in order to determine which OSR must be used to reach a $70dB$ dynamic range (it corresponds to about 11 bit resolution because one bit has been added for noise margin requirements). In Table 4.1, the coefficients used for second and third order sigma delta modulators have been reported [2, 3].

2nd order k		3rd order k	
k_1	$\frac{2}{3}$	k_1	$\frac{1}{4}$
k_2	$\frac{3}{8}$	k_2	$\frac{24}{47}$
		k_3	$\frac{47}{120}$

Table 4.1: Scaling coefficient for second and third order sigma delta modulators

In order to have a major stability safety margin, a gain halving over the whole modulators has been implemented, for that reason the coefficients of Table 4.1 have been further scaled of a $1/\sqrt{2}$ and $1/\sqrt[3]{2}$ factor respectively for the second and third order modulator. In Table 4.2, the SNR results obtained using Equation (4.1) for a second and a third order modulator with different OSR values are reported. The OSR that allows to achieve a $70dB$ target SNR, is then in the $80 \div 90$ range for a second order modulator while a OSR=40 – 50 is needed using the third order modulator. The first solution has the advantage to be a lower area-and-power consumption approach while the third order modulator benefit is the possibility to use a lower sampling frequency. We have then developed simulations for both cases and postponed the decision on the basis of noise analysis results.

Second Order			Third Order		
OSR	f_s [MHz]	SNR [dB]	OSR	f_s [MHz]	SNR [dB]
60	1.2	63.2	30	0.6	55.25
70	1.4	66.6	40	0.8	64
80	1.6	69.5	50	1	70.8
90	1.8	72	60	1.2	76.3
100	2	74.3	70	1.4	81
110	2.2	76.4	80	1.6	85.1

Table 4.2: SNR values at different OSR in second and third order modulators

4.2 Simulink behavioral model

A high level behavioral model in simulink environment has been first developed in order to evaluate the sigma delta performances, the analysis has been done both for second (Fig. 4.1) and third order modulator (Fig. 4.2). The integrator gains have been obtained as the product of the sampling frequency and the scaling coefficients indicated in the previous section.

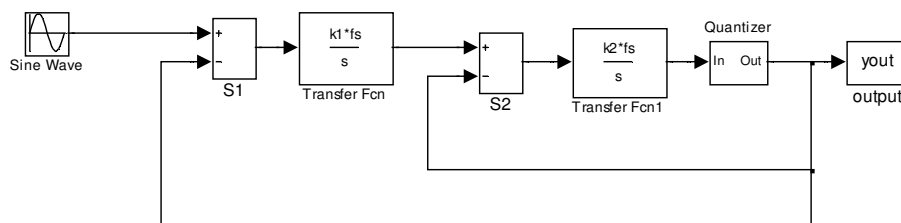


Figure 4.1: Simulink model for a second order modulator in the $\mu A - nA$ range

Each block diagram has been adapted for the two different operating ranges as it can be observed in Fig. 4.3 and Fig. 4.4. The $1/1000$ gain factor that multiplies the input signal, takes into account the reduction of the input of three order of magnitude, to compensate this reduction, granting the same SNR, an equivalent gain must be provided to the modulator loop. The total gain of 1000 has been divided between the two stages (a factor of 32 for each stage), also the feedback paths must be attenuate of the same factor to compensate the amplification provided by the loop gain. In third

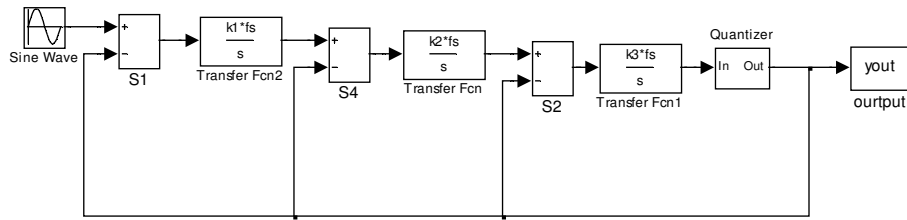


Figure 4.2: Simulink model for a third order modulator in the $\mu A - nA$ range

order modulator, the gain scaling has been distributed leaving more gain to the first stage for noise consideration and a $32 - 5.7 - 5.7$ configuration has been chosen. In fact, a higher gain in the first stage allows to relax the noise requirements on the following stages, because their noise is added to an amplified signal thus its effect becomes less critical and often can be neglected.

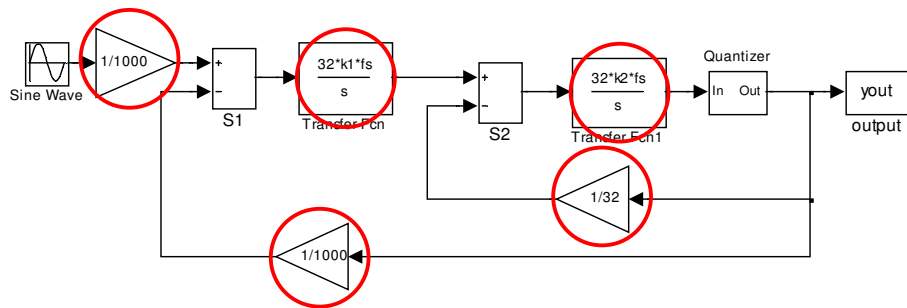


Figure 4.3: Simulink model for a second order modulator in the $nA - pA$ range

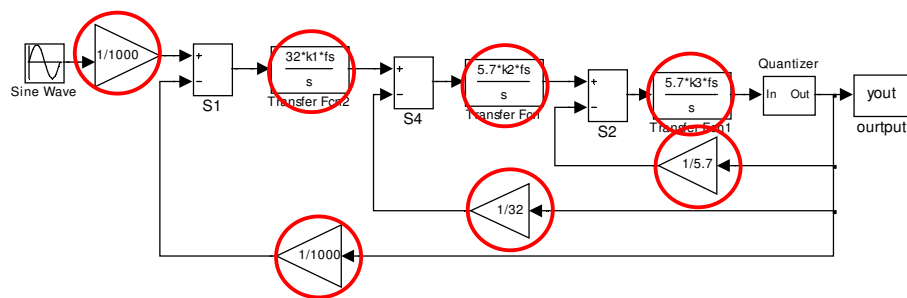


Figure 4.4: Simulink model for a third order modulator in the $nA - pA$ range

The resulting PSDs for the second and third order are reported respectively in Fig. 4.5 and Fig. 4.6 and, as summarized in Table 4.3, confirm the results obtained with hand calculations using Equation (4.1). As expected the results, at this simulation level, are the same for both input ranges.

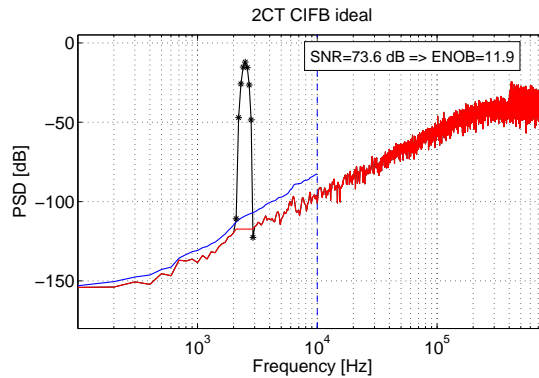


Figure 4.5: PSD calculated with the simulink model of the second order modulator

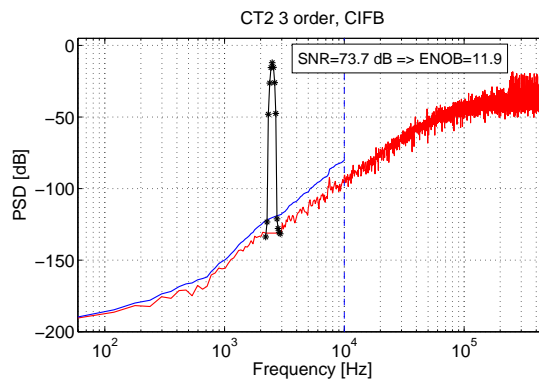


Figure 4.6: PSD calculated with the simulink model of the third order modulator

	2nd order	3rd order
fs	1.64 MHz	0.98 MHz
OSR	82	48.75
SNR	73.6	73.7

Table 4.3: Simulation results in simulink environment

4.3 VerilogA behavioral model

The ideal results obtained with matlab-simulink simulations have been confirmed with a more realistic system description using VerilogA models in cadence environment. This solution in fact allows to insert a wide number of parameters both in terms of operational amplifier non-idealities and of noise sources. The used verilogA library permits to introduce effects due to opamp

Opamp parameters			
Avd	$10^6(V/V)$	cin	$10^{-15}(F)$
Avc	$0(V/V)$	ricp	$10^{12}(\Omega)$
rin	$10^{12}(\Omega)$	ricm	$10^{12}\Omega$
rou	$0.1(\Omega)$	Vos	$0(V)$

Table 4.4: Opamp parameters in veriloga model

finite bandwidth and gain, harmonic distortion, input noise, saturation limits, offset voltage and offset current. The parameters used in first simulations are reported in Table 4.4 and refer to the small signal model of Fig. 4.7, any other non-ideal effect can be easily added to the simulation.

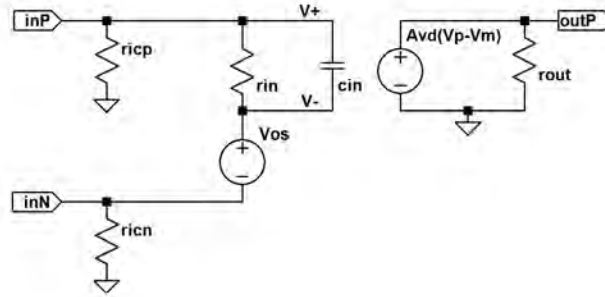


Figure 4.7: Small signal model for the veriloga opamp

4.3.1 From voltage to current mode sigma delta modulator

Typical analysis for delta sigma modulators are referred to voltage input and voltage feedback. In our case the signal to be acquired is a current, thus the practical sigma delta implementation must be adapted for this purpose. The correspondence between the two model is quite simple, the voltage and current models are reported respectively in Fig. 4.8(a) and Fig. 4.8(b).

In voltage mode R_1 is determined on the basis of noise analysis to make sure that its thermal noise is at least one order of magnitude lower than the target LSB. Once that this value has been chosen the integrator capacitance C_1 is fixed by the expression of Equation (4.2), where K_1 is the scaling factor of stage 1 and f_s is the sampling frequency.

$$C_1 = \frac{1}{K_1 f_s R_1} \quad (4.2)$$

The maximum voltage is imposed by the sigma delta reference voltage, hence the maximum input current is consequently fixed by maximum voltage and R_1 considerations. In current mode the situation is slightly different because the minimum value of the maximum input current is imposed by the input current amplitude to be detected (i.e. $1\mu A$ and $1nA$ for the two ranges), and, since the constraint on the maximum input voltage is still true, the equivalent R_1 is fixed by the eq. 4.3

$$R_1 = \frac{V_{in,max}}{I_{in,max}} \quad (4.3)$$

Actually, as shown in Fig. 4.8(b), there is not input resistance in current mode implementation, but this fictitious component is still useful to calculate C_1 and to determine the voltage controlled current source transconductance $G_1 = 1/R_1$ that provides the feedback current.

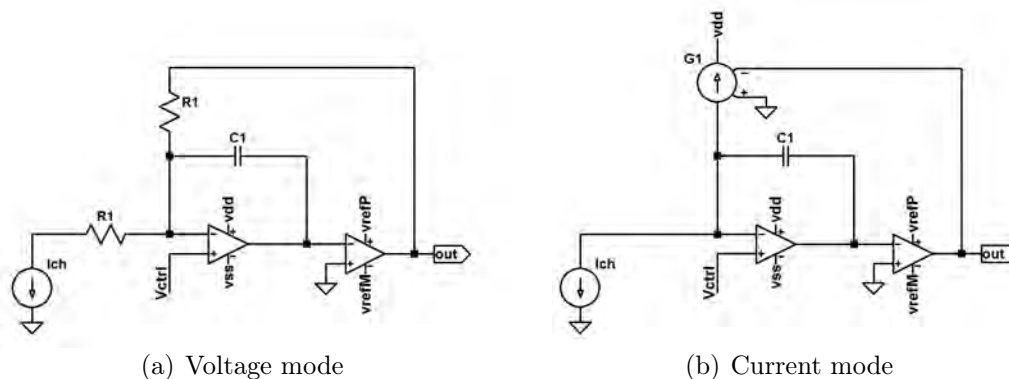


Figure 4.8: Sigma delta circuits for voltage and current mode recordings

With this discussion, carried on in the case of ideal current source, we are not considering the membrane and electrode impedances. In order to evaluate their effect, we added a series resistance to the input current signal to verify if the system performances are still the same. To model the impedance electrode membrane with a simple resistive component is clearly a strong simplification useful for first evaluations, for a more reliable analysis all components described in Chapter 1 should be added. The circuit including also the electrode impedance is shown in Fig. 4.9

The voltage and current models for a second order modulator are reported in Fig. 4.10 and Fig. 4.11, the same approach can be extended to third order modulators. Equations (4.4) and (4.5) show the correspondences between

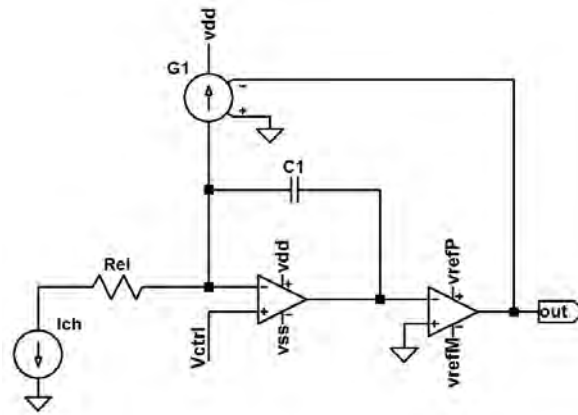


Figure 4.9: Sigma delta circuits for current mode recordings with electrode impedance modeling

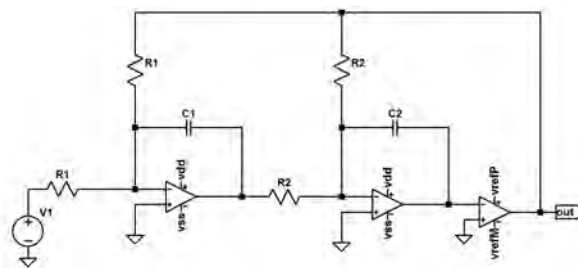


Figure 4.10: Second order sigma delta circuits for voltage mode recordings

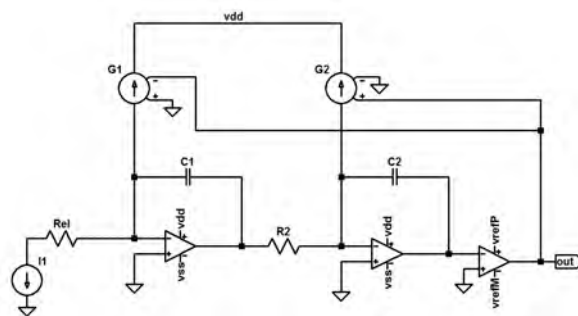


Figure 4.11: Second order sigma delta circuits for current mode recordings with electrode impedance modeling

the two models.

$$I_{ch} = \frac{V_1}{R_1} \quad I_{ref1} = \frac{V_{ref}}{R1} \quad I_{ref2} = \frac{V_{ref}}{R2} \quad (4.4)$$

$$C_1 = \frac{1}{k_1 f_s R_1} \quad C_2 = \frac{1}{k_2 f_s R_2} \quad (4.5)$$

4.3.2 Circuit sizing

According to what has been explained in Section 4.2, the second order and third order delta sigma current modulators have been scaled in order to be adapted to the $1\mu A - 1nA$ and $1nA - 1pA$ ranges. We chose to scale the coefficients modifying only the values of integrator capacitances and feedback current generator. In fact, in view of physical implementation, this solution will allow an easier design based on ranks of capacitance and ranks of output current mirror MOS. These components will be connected in parallel or disconnected by means of a switch network controlled by the external according to the desiderate range.

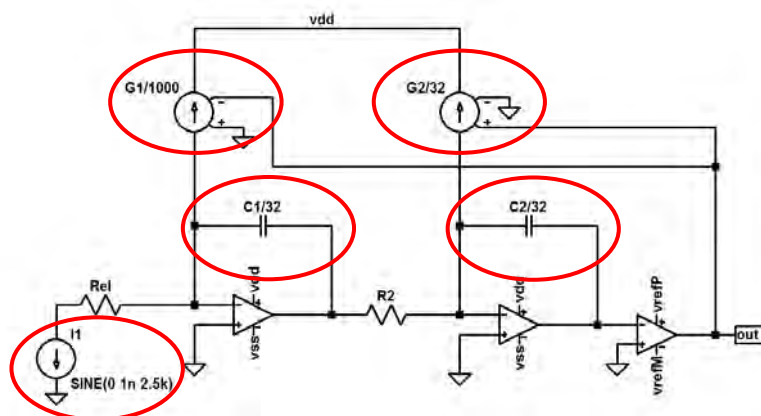


Figure 4.12: Scaled second order sigma delta circuits

In Fig. 4.12 and Fig. 4.13, the sigma delta modulator circuits with scaled components values for the second and third order loop are reported. In Table 4.5 and Table 4.6, the sizes chosen for the relative circuits components are presented. As explained, the resistance values have been kept constant while the scaling have been done using capacitors and currents.

4.4 Experimental results

Experimental results are aimed to confirm the good agreement between the different developed models. We have then set up simulations in order to verify the correspondence between the voltage and the current sigma delta

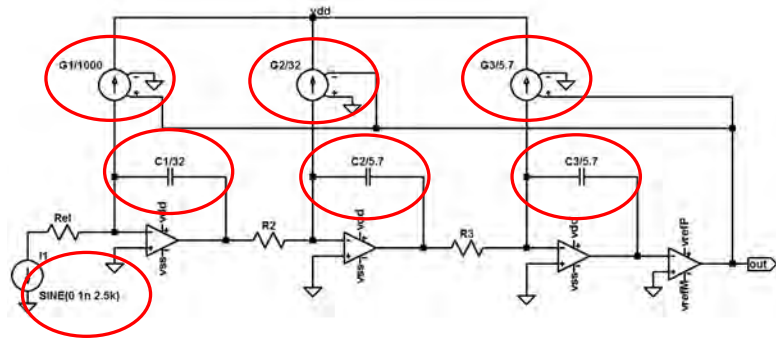


Figure 4.13: Scaled third order sigma delta circuits for current mode recordings with electrode impedance modeling

	2nd order	2nd order scaled
R_1	$500k\Omega$	$500k\Omega$
C_1	$2.6pF$	$82fF$
I_{ref1}	$2\mu A$	$2nA$
R_2	$88.4k\Omega$	88.4Ω
C_2	$26pF$	$820fF$
I_{ref2}	$11.3\mu A$	$350nA$

Table 4.5: Second order modulator sizing

	3rd order	3rd order scaled
R_1	$500k\Omega$	$500k\Omega$
C_1	$10.3pF$	$325fF$
I_{ref1}	$2\mu A$	$2nA$
R_2	$246k\Omega$	246Ω
C_2	$10.3pF$	$1.8pF$
I_{ref2}	$4.06\mu A$	$713nA$
R_3	$320k\Omega$	$320k\Omega$
C_3	$10.3pF$	$1.8pF$
I_{ref}	$6.25\mu A$	$274nA$

Table 4.6: Third order modulator sizing

modulator and to confirm that adding the electrode impedance the achieved results are still valid. Power spectral density for the three cases are reported

in Fig. 4.14, Fig. 4.15 and Fig. 4.16. As it can be inferred from the PSD plot, the agreement among the three different models is excellent, as their signal to noise ratio is 71.8dB for the voltage base model and 71.1dB for both current models (with and without the electrode impedance).

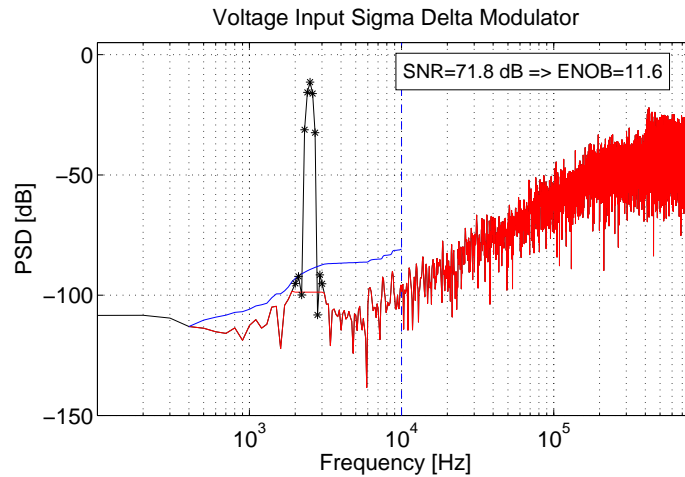


Figure 4.14: PSD for a second order voltage mode sigma delta modulator

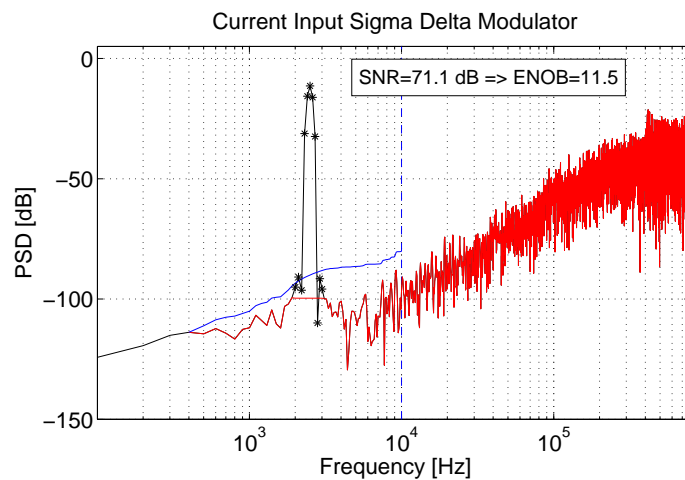


Figure 4.15: PSD for a second order current mode sigma delta modulator

The perfect matching between the voltage and current modulator as well as the agreement with the results predicted by the ideal simulink model has also been verified for different values of the input current, and for both

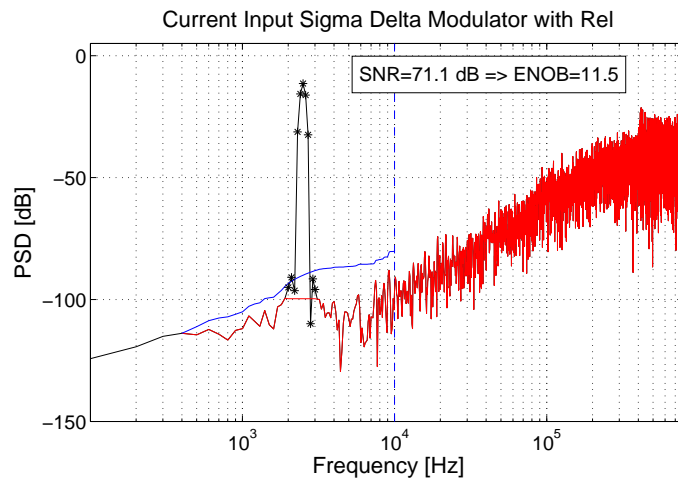


Figure 4.16: PSD for a second order current mode sigma delta modulator with electrode impedance modeling

the operative ranges. As shown in Fig. 4.17 and Fig. 4.18, respectively for second and third order loop modulators, the points calculated using the verilogA models fit very well with the continuous curve representing the simulink results. The red curve with the cyan markers represents results for the $1\mu A - 1nA$ range while the blue curve with black markers is related to the $1nA - 1pA$ range. It is clear how, both for second and third order loop, the two range curves are simply shifted in terms of current amplitudes without any distortion. Clearly this is due to noise effects neglecting; a deep noise analysis is then required in order to evaluate how noise effects can cause the degradation of these curves. The most critical point regards the generation of high precision currents in the nA range, a very high output impedance current mirror is in fact necessary for low current generation. Future developments of this project concern then an accurate noise analysis before to proceed with transistor level implementation.

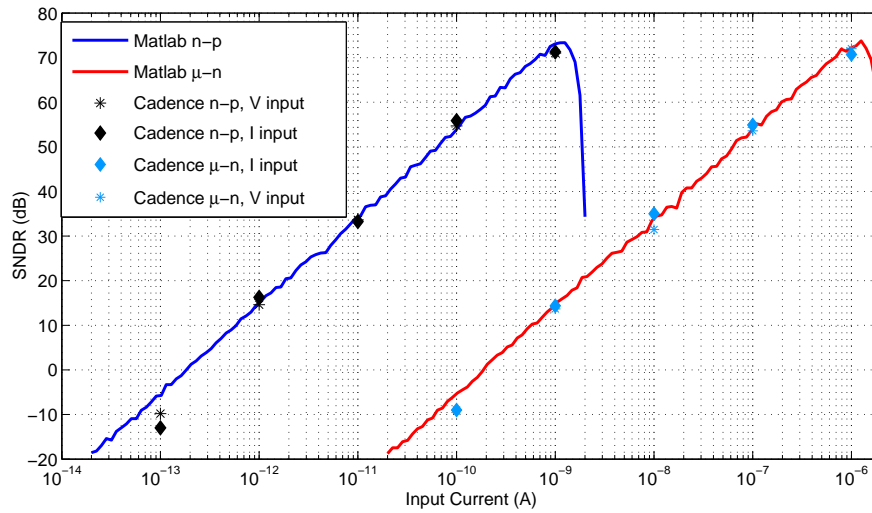


Figure 4.17: Second order modulator: SNR vs input amplitude

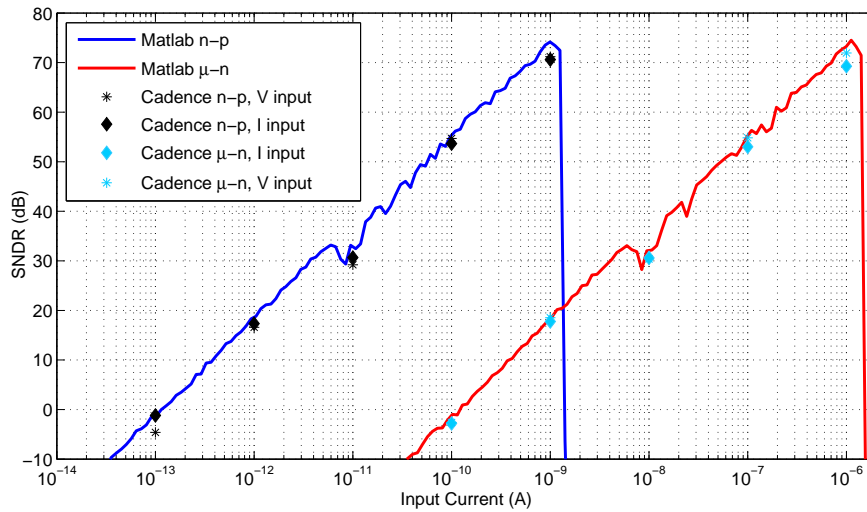


Figure 4.18: Third order modulator: SNR vs input amplitude

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Conclusions

The work presented in this thesis is the result of three years of research during which several advancements, in the long way aimed to realize a fully implantable device for neural recording and PNS stimulation, have been achieved. Three main topics have been dealt with: first a discrete electronic interface for neural recording and stimulation has been implemented, then the possibility to extract the ion channel currents that generate the neural spikes have been investigated and finally an IC circuit for neural recording has been developed.

The bidirectional interface realized with discrete electronics and hosted in a PCB has been designed, implemented and successfully tested with in-vivo experiments performed in clinical trials with rats. The interface is made up of a recording and a stimulation unit, connected to the PC thanks to a digital control system. The device can be easily configured by the user with a custom developed GUI. The main tasks of the recording module are to amplify, filter and digitalize the neural signal coming from one of the eighth-channel tFLIFE electrode. The acquired signal can be visualized in real-time during the acquisition and stored in a data file for offline processing. The stimulation unit permits to deliver current train pulses programmable in terms of duration, width and amplitude. The generated patterns are injected into the electrode and sent to the PNS. Results obtained during in-vivo tests have shown the system capability to record signals in the order of magnitude of ten μV exhibiting a $IRN = 0.83\mu V_{rms}$ with a power consumption lower than $1W$. The possibility to evoke muscles contractions in response to neural stimulations has also been successfully verified.

Since neural spikes are generated by means of ion channel currents, an investigation on electronic devices able to record such currents has also been carried out. A redout circuit based on patch-clamp technique for ion channel current recording has been designed at a system level. A current mode sigma-delta converter has been used to set the voltage on the cell membrane and to detect the ion current flowing through the channels. Due to the wide range of the ion channel currents, a $120dB$ dynamic range converter is re-

quired. The proposed solution splits the range in two parts and solve the problem using a single delta sigma converter, with a $60dB$ dynamic range, whose capacitances and feedback current values can be reconfigured depending on the working range. Simulation results show an excellent agreement between the ideal model and a behavioral design, that also takes into account non-ideal effects, and confirm the possibility to use a single reconfigurable modulator for both ranges. As next step a careful noise analysis must be done in order to verify the possibility to realize physically this device, prior to proceed with a transistor level implementation.

The last project developed in this thesis has been the design of a neural recording chip in a $0.35\mu m$ technology from austriamicrosystems. The COTS system results have been used as a guideline to define the specifications of the neural recording chip. The architecture used for the IC design is based on a delta sigma converter and the approach proposed is to keep the analog part of the system as simple as possible, moving the complexity on the digital side. The analog IC module is composed by a first order analog preamplifier/pre-filtering block and by a third order single loop sigma delta modulator. The bandpass high selective filter is provided by the digital part of the system implemented in a Xilinx Virtex 5 LX330 FPGA. The simulation results confirmed the capability of the system to amplify, filter and correctly digitalize, with a 10 bit resolution, pre-recorded neural signals in the order of magnitude of tens of microvolts. The device exhibits an $IRN = 1.64\mu V_{rms}$ with a $3.2mW$ power consumption (referred to single channel), the total power can be reduced to $2.5mW$ using the device in the lower gain configuration. The chip area occupancy is $0.8mm^2$ for each recording channel. Future developments are aimed, first, to the physical realization of the device and to perform electrical tests to confirm the simulation results by means of real measurements. The stimulation integrated unit must also be designed and realized. Then, in-vivo tests in clinical trials both with animals and human subjects are scheduled within a new project called Nemesis, in which the University of Cagliari is involved, funded by the Italian Ministry of Health and carried on in collaboration with Scuola Superiore Sant'Anna, Pisa and Università Campus biomedico, Rome.

The research leading to this thesis has received funding from MIUR (Italian Ministry of Education, University and Research) through projects Safehand (PRIN 2006) and Openhand (PRIN 2008) and from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement No. 248424, MADNESS Project and under grant agreement No. 231500, ROBOSKIN Project.

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