

Short Report

Optimization of Vertical Double-Diffused Metal-Oxide Semiconductor (VDMOS) Power Transistor Structure for Use in High Frequencies and Medical Devices

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Abstract

Power transistors, such as the vertical, double-diffused, metal-oxide semiconductor (VDMOS), are used extensively in the amplifier circuits of medical devices. The aim of this research was to construct a VDMOS power transistor with an optimized structure to enhance the operation of medical devices. First, boron was implanted in silicon by implanting unclamped inductive switching (UIS) and a Faraday shield. The Faraday shield was implanted in order to replace the gate-field parasitic capacitor on the entry part of the device. Also, implanting the UIS was used in order to decrease the effect of parasitic bipolar junction transistor (BJT) of the VDMOS power transistor. The research tool used in this study was Silvaco software. By decreasing the transistor entry resistance in the optimized VDMOS structure, power losses and noise at the entry of the transistor were decreased, and, by increasing the breakdown voltage, the lifetime of the VDMOS transistor lifetime was increased, which resulted in increasing drain flow and decreasing R_{on} . This consequently resulted in enhancing the operation of high-frequency medical devices that use transistors, such as Radio Frequency (RF) and electrocardiograph machines.

Keywords: VDMOS transistor, UIS implant, electrocardiograph machine, noise, high frequency

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In order to apply the power and high frequency of medical devices amplifier circuits, the VDMOS transistor must have a short channel length and a low doping level in the drain area (1). Having the low level of doping in drain will guarantee that the charge space layer in the drain-channel connection is extended in the drain area instead of the channel area, where it could block the high voltage. Because of having a high breakdown voltage and a low R_{on} , the VDMOS transistor is an important device for use in medical devices and at high frequencies. In order to use this transistor in power applications, at high frequencies, and in the amplifier circuits of medical devices, the R_{on} must be decreased as much as possible, but there is always a trade-off between R_{on} and the breakdown voltage (2). Decreasing the breakdown voltage in power systems, especially DC/DC converters and the

amplifier circuits of medical devices, which use VDMOS extensively, will result in damage to the inner circuits of converters and decelerating devices, thereby increasing losses and decreasing the lifetime of the converters (3). In addition, in high-frequency applications, if R_{on} increases, the operation speed of the amplifiers in the sender and receiver channels will decrease, causing large power losses. However, if R_{on} decreases, the breakdown voltage will also decrease, and, if the decrease in the breakdown voltage is excessive, the VDMOS transistor would be inappropriate for use in power applications.

The starting point of this research included the steps of implanting UIS and the Faraday shield. The latter was done to replace the gate-field parasitic capacitor in the entry part of the device (2-4). Then, the UIS was implanted to decrease the parasitic BJT effect of the VDMOS power transistor. Implementing the suggested structure also eliminated the need of using an extra mask in every step of implanting the devices, maintained the self-aligned structure to the gate mass, and eliminated the overlay error potential in the photolithography step. As a result, in comparison to other transistors, the switching speed was increased and noise was decreased. The gate contact junctional pad and all of the metal oxide layers were connected, which had drainage on intrinsic substrate-pad capacitors. Hence, infiltration low-contamination (p) could sit under the pad. The infiltration layer was connected to the source area, and it acted as a conductor between the gate pad and the drain substrate and decreased the gate-drain capacitor (C_{gd}) effect. In this way, the boron implant was referred to as the implanted Faraday shield, which was used in the VDMOS to replace the gate-field parasitic capacitor in the entry part of the device.

In this research, the process of constructing the VDMOS transistor was completed successfully, including the extension of the implant and infiltration processes and the integration process, which was done by the total self-aligning structure of the gate, the source, and the body. In addition, the R_{on} was decreased as much as possible by adding the boron implant step and adjusting the energy implant of the boron. The V_t also was decreased in such a way that no changes were made in the device's breakdown voltage. The breakdown voltage was increased from 82 to 86 volts, and, as a result of increasing the breakdown voltage, the VDMOS transistor became Stronger in different applications, such as in high-frequency devices. In addition, since the C_{iss} must be charged to threshold voltage, before the device is turned on and discharged to a specified voltage before the device is turned off. It had a direct effect on the time of device turning on and off. In this research the V_t was reached from 3.2 volts to 2.75 volts. By decreasing the V_t , the C_{iss} capacitor was charged faster and consequently discharged faster, and the F_{max} frequency was also increased. In addition, the R_{on} was decreased as much as possible by adding the boron implant step and adjusting the energy required by the boron implant, and the V_t also was decreased.

In the new, optimized VDMOS structure, there were small increases in noise and switching speed in medical applications. By decreasing the R_{on} , the maximum rate of drain flow when the gate-source voltage was 6.5 V was reached between 40 and 50 microamperes. This increasing drain flow will result in decreasing the amount of the R_{on} , which can help enhance the operation of medical devices that use transistors, such as the RF and electrocardiograph machines, and it also can increase their operational speed (5). The important technical achievement of this research was determining the relationships between the physical and electrical functions of the VDMOS transistor structure by using diagrams and process parameters. The problem that existed with this method was the need to adjust the impurity rate carefully. However, since the breakdown voltage was increased and the R_{on} was decreased, it was possible to ignore the impurity rate.

In a study conducted (3), in which they analyzed and simulated the stress-decreasing operation of power VDMOS transistors, the results showed that using VDMOS transistors under stress conditions produced enhanced physical and electrical characteristics, such as R_{on} and breakdown voltage, and the surface charge was negative. Although the VDMOS operation was enhanced to a specified rate by increasing the stress time, the shortcoming of this method was that, after passing the specified stress time, increasing the stress time did not affect the operation of the device, and, as a result, the breakdown voltage could not be optimized.

The advantage of this research compared to a similar project in creating a new method for the gradation of single-event, gate-rupture (SEGR) in a VDMOS was the deletion of the trade-off rate. The defect of this method was that the local oxide of silicon (LOCOS) structure located in the neck area was dependent on the neck area in the VDMOS transistor (6). The results of this research project showed that decreasing the V_t decreased the R_{on} rate in the optimized VDMOS structure, and, as a result, noise was decreased and the switching speed in medical applications was increased (7). In order to attain the optimized VDMOS structure, the decrease in V_t from 3.2 to 2.75 volts and the increase in the device breakdown-voltage from 82 to 86 volts increased the maximum drain flow from 40 to 50 microamperes. This increase in the drain flow decreased the R_{on} , which helped enhance the operation of high-frequency medical devices that use transistors, such as the RF and the electrocardiograph machines, by increasing their operation speed (8).

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Conflict of Interest:

There is no conflict of interest to be declared.

Authors' contributions:

Both of authors contributed to this project and article equally. Both of authors read and approved the final manuscript.

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References:

1. Ghamati M. Low-noise low-power MOSFET only electrocardiogram amplifier. Conference Publications of Electrical Engineering (ICEE). 2013;13767968 (3):1-5
2. Cai WZ, Gogoi BS, Loechel GH. TCad Analysis of a Vertical RF Power Transistor. Conference of San Diego USA. 2009; 978-1-4244-3947-8(5):249-52
3. Zoeter M, Beydoun B, Hajjar M, Debs M, Charles J-P. Analysis and Simulation of Functional Stress Degradation on VDMOS Power Transistors. J of Active and Passive Elec. 2002; 25(8):215–223. DOI: <http://dx.doi.org/10.1080/08827510213500>
4. Ren M, Hong Z. A. Novel planar vertical double-diffused metal-oxide semiconductor field-effect transistor with in homogeneous floating islands Chin. IEEE electron dev lett. 2011;20(12): 7-12
5. Zhaohuan T, Gangyi HU. Novel structure for improving the SEGR of a VDMOS. Journal of Semiconductors. 2012;33(4):982-4. DOI: <http://dx.doi.org/10.1088/1674-4926/33/4/044002>
6. Roig J, Mouhoubi S. New VDMOS Structure with Discontinuous Thick Inter-Body Oxide to Reduce Gate-to-Drain Charge Process Development & Integration. journal of Corporate R&D ON Semiconductor. 2011; 36(4):25-32
7. Ueda D, Takagi H. A new vertical double diffused MOSFET—the self-aligned terraced-gate MOSFET. IEEE Trans On Elec Devices. 1984; 31(4):416–20. DOI: <http://dx.doi.org/10.1109/T-ED.1984.21543>
8. Yih C, Cheng S. A new approach to simulating n-MOSFET gate current degradation by including hot-electron induced oxide damage. IEEE Transaction on Electron Devices. 1998;45(11):2343–8. DOI: <http://dx.doi.org/10.1109/16.726653>

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