Threshold Voltage Compensation Error in Voltage Programmed AMOLED Displays

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***Abstract*—A new accurate voltage-programmed pixel circuit for active matrix organic light-emitting diode (AMOLED) displays is presented. Composed of three TFTs and one storage capacitor, the proposed pixel circuit is implemented both in a-Si and a-IGZO TFT technologies for the same pixel size for fair comparison. The simulation result for the a-Si-based design shows that, during a programming time of 90μs, the pixel circuit was able to compensate for a 3V threshold voltage (V_{th}) shift of the drive TFT with almost no error. In contrast, the a-IGZO-based pixel circuit, has a larger current error (of around 8%), despite its proven three-fold higher speed.**

***Index Terms*—active-matrix organic light-emitting diode (AMOLED), amorphous silicon (a-Si), oxide thin-film transistor (TFT), compensation.**

I. Introduction

OWNING to their competitive advantages over the ubiquitous liquid crystal display (LCD), organic light-emitting diode (OLED) displays, integrated with thin film transistor (TFT) technology, have generated considerable interest in recent years. The process of compensation for the threshold voltage shift as an intrinsic property of the TFT, differentiates the driving scheme of active matrix OLED (AMOLED) display from its LCD counterpart.

Among various technologies to implement TFT backplanes, there is amorphous silicon (a-Si), low-temperature polycrystalline silicon (LTPS) and amorphous indium gallium zinc oxide (a-IGZO). LTPS offers higher mobility and generally lower parasitic capacitance compared to IGZO depending on device structure [1]. However, it suffers from short range mismatch due to grain boundaries. The fabrication process is more costly especially when it comes to large area scaling due to the more complex processing. IGZO technology, which belongs to the general category of metal-oxide semiconductor, offers a carrier mobility of at least 15 times higher compared to the silicon-based technology [2]. This and the low temperature fabrication process[1] (enabling flexible displays) as well as higher stability of threshold voltage shift under positive gate-bias stress [3] have made this new technology very attractive for implementing circuits, including image capture [4], in AMOLED displays.

It is well known that the threshold voltage shift has a direct impact on ciruit performance. For example, consider the simple 2−TFT pixel circuit shown in Fig. 1. The data line provides the required programming voltage for the drive TFT,

[1]Mainly because the deposition method that is used for fabricating a-IGZO TFTs is Physical Vapour Deposition (PVD) rather than Chemical Vapour Deposition (CVD).

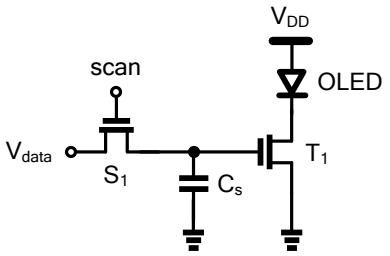

Fig. 1: A simple structure for AMOLED pixel.

while the scan line determines the running state of the switch TFT, i.e. ON or OFF. The voltage stored on C_s is converted to a current by T_1, which passes through the OLED. Due to the voltage shift in V_{th} of T_1, this simple circuit cannot be used as a practical pixel configuration to drive the OLED, because the current and thus the luminance of the OLED degrades for a specific data voltage over time. Since this shifting process of the threshold voltage of a TFT under gate-source stress is not accurately predictable, and circuit designers have been persuaded to propose diverse techniques to compensate for the aforementioned instability of the AMOLED pixel circuits and stabilize the OLED luminance [5].

Among the different methods proposed for V_{th} compensation, the voltage-programming based drive scheme [5-9] has attracted considerable attention in view of its advantages such as faster settling time. In essence, in all voltage-programming schemes, a storage capacitor (C_s) is precharged to a desired voltage, and during the compensation period, it discharges through a diode-connected TFT (drive TFT, T_1) until its voltage reaches the threshold voltage, as illustrated in Fig. 2. At this time, T_1 goes OFF and C_s stops discharging. After that, the data voltage (V_{data}) is added to the voltage across C_s, making the gate-source voltage of T_1 $V_{\text{data}} + V_{\text{th}}$. Supposing T_1 is in the saturation region, the current through T_1 would be independent of V_{th} and is given by

$$\begin{aligned} I_{\text{OLED}} &= \frac{1}{2}K(V_g - V_{\text{th}})^2 \\ &= \frac{1}{2}K(V_{\text{data}} + V_{\text{th}} - V_{\text{th}})^2 \\ &= \frac{1}{2}KV_{\text{data}}^2, \end{aligned} \tag{1}$$

where

$$K = \mu_{\text{FET}} C_i \frac{W}{L}, \tag{2}$$

and μ_{FET}, C_i, W, and L are field effect mobility, gate insulator

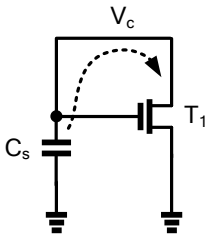

Fig. 2: Compensation phase of a voltage-programmed pixel circuit.

capacitance, channel width, and channel length, respectively. This very simple method is, however, flawed in some respects: First and foremost, the time constant of the circuit is determined by the transconductance (g_m) of the drive TFT, the value of which depends on the voltage of the top plate of the capacitor (which is the voltage of the gate (drain) of the drive TFT). As this voltage degrades, g_m also reduces, making the circuit very slow to reach the desired V_{th}. The final overdrive voltage of the drive TFT can be obtained as [10]

$$V_{\text{ov}} = \frac{V_{C0} - V_{\text{th}}}{(V_{C0} - V_{\text{th}})\frac{K}{2C_s}t_c + 1} \tag{3}$$

where V_{C0} is the initial voltage of the capacitor, and t_c is the compensation time.

Second, even when V_C reaches V_{th}, due to the subthreshold current, it still keeps decreasing, making it impossible to accurately measure the threshold voltage.

A new method of compensation was devised in [11] that yielded a fast, accurate pixel circuit. This was not however at the expense of circuit complexity. In this work, we adopt the same methodology, but with a reduced complexity circuit. The circuit has one less TFT, one less capacitor, and one less control line. An analytical description of the functionality of the compensation approach is also presented.

II. Analysis of the Proposed V_{TH} Compensation Method

Fig. 3 shows the concept of the new driving scheme. The circuit consists of a capacitor (C_1) which is connected to the drain of the drive TFT (T_1) (Fig. 3(a)). If we precharge C_1 to a voltage, say V_{C0}, and apply an arbitrary voltage function to the gate of T_1 (Fig. 3(b)) for a definite time (from $t = 0$ to $t = t_1$), C_1 starts discharging until the gate voltage becomes zero. Now, assume that the threshold voltage of T_1 shifts (to a more positive one). If the gate voltage function remains unchanged, T_1 experiences a smaller gate-source voltage during the discharging interval. Hence, the current which causes C_1 to discharge is now smaller, resulting in a larger final voltage stored on the top plate of C_1 ($V_C(t_1)$).

To summarize, we can state that, *as the threshold voltage of T_1 shifts, the final voltage stored across C_1 increases*. This is the principle of the proposed V_{th} compensation technique.

In the proposed circuit, the applied voltage is a constant equalling V_{g0}. In order to work out the final voltage of C_1 at the end of the discharging interval, we assume the initial

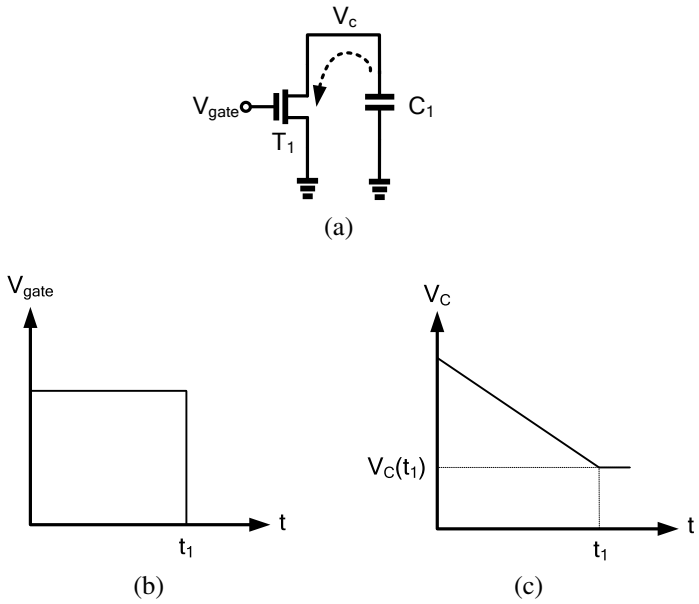

Fig. 3: (a) Circuit core that compensates for V_{th} (b) applied gate voltage (c) voltage across the capacitor.

voltage of the capacitor to be V_{C0}. Now, from the simple square-law characteristic of a field-effect transistor, which is

$$I = \frac{1}{2}K(V_{g0} - V_{\text{th}})^2, \tag{4}$$

and the current-voltage relation for a linear capacitor, which is

$$i = C\frac{\triangle V}{\triangle t}, \tag{5}$$

the final voltage of C_1 is readily derived and is given by

$$V_C(t_1) = V_{C0} - \frac{K}{2C_1}\left(V_{g0} - V_{\text{th}}\right)^2 t_1. \tag{6}$$

If V_{th0} is the initial threshold voltage of T_1, and ΔV_{th0} is the threshold voltage shift, (6) can be rewritten as

$$V_C(t_1) = V_{C0} - \frac{K}{2C_1}\left(V_{g0} - V_{\text{th0}} - \Delta V_{\text{th}}\right)^2 t_1. \tag{7}$$

Expanding the above equation, we have

$$\begin{aligned} V_C(t_1) = &\left[V_{C0} - \frac{K}{2C_1}\left(V_{g0} - V_{\text{th0}}\right)^2 t_1\right] \\ &+ \frac{Kt_1}{2C_1}\left[2\left(V_{g0} - V_{\text{th0}}\right)\Delta V_{\text{th}} - \Delta V_{\text{th}}^2\right]. \end{aligned} \tag{8}$$

The first group of terms in (8) is independent of ΔV_{th}. We name it V_{ind}. Following (8), and by adding the data voltage, V_{data}, to $V_C(t_1)$, the current through the OLED is then given by

$$\begin{aligned} I_{\text{OLED}} &= \frac{1}{2}K(V_{\text{data}} + V_{\text{ind}} \\ &\quad + \frac{Kt_1}{2C_1}\left[2\left(V_{g0} - V_{\text{th0}}\right)\Delta V_{\text{th}} - \Delta V_{\text{th}}^2\right] - V_{\text{th}})^2 \\ &= \frac{1}{2}K(V_{\text{data}} + V_{\text{ind}} - V_{\text{th0}} \\ &\quad + \frac{Kt_1}{2C_1}\left[2\left(V_{g0} - V_{\text{th0}}\right)\Delta V_{\text{th}} - \Delta V_{\text{th}}^2\right] - \Delta V_{\text{th}})^2. \end{aligned} \tag{9}$$

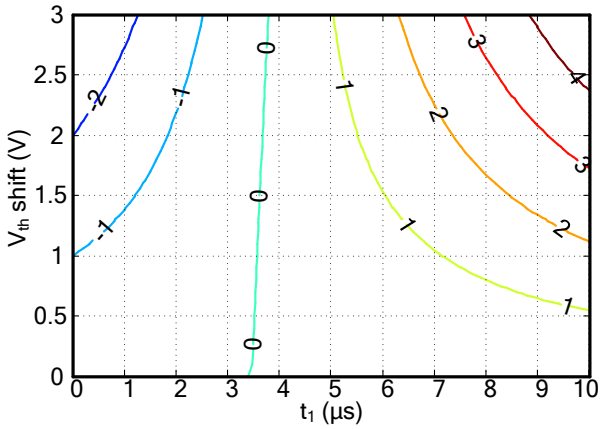

Fig. 4: The profile of the error voltage during OLED compensation in the proposed pixel circuit.

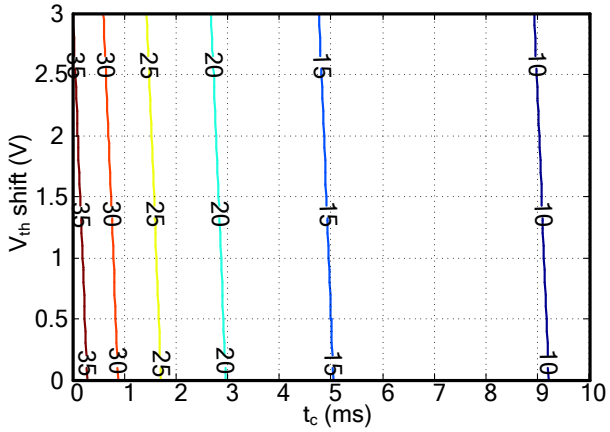

Fig. 5: The profile of the error voltage during OLED compensation in the conventional pixel circuit.

The $V_{\text{th}}-$dependent terms in (9) need to be minimized within a defined range of V_{th} shift to reach an optimum point for the current error of the OLED. Typical values for K and V_{th0} for an a-Si TFT with $W/L = 10\mu m/10\mu m$ (used in the simulations) are close to $16nA/V^2$ and $2V$, respectively. The optimization is conducted for $0 < \Delta V_{\text{th}} < 3V$ and C_1 and V_{g0} are chosen as $1pF$ and $20V$, respectively. The profile of the $V_{\text{th}}-$dependent terms (error voltage), i.e.

$$f\left(t_1, \Delta V_{\text{th}}\right) = \frac{Kt_1}{2C_1}\left[2\left(V_{g0} - V_{\text{th0}}\right)\Delta V_{\text{th}} - \Delta V_{\text{th}}^2\right] - \Delta V_{\text{th}}, \tag{10}$$

is numerically analysed and plotted in Fig. 4. As can be seen, the error voltage is approximately zero around $t_1 = 3.5\mu s$. For sake of comparison, the error voltage in (3), which is the second term, is also plotted in Fig. 5. A similar simulation demonstrates that in order to reach an error comparable with that of the proposed circuit, t_c must be in the order of 1ms, while the maximum programming time budget is around 70μs in QVGA displays and less than 45μs in XVGA ones [10].

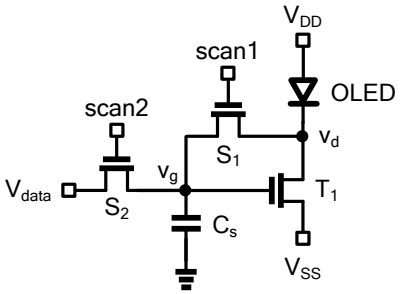

Fig. 6: Proposed pixel circuit for V_{th} compensation.

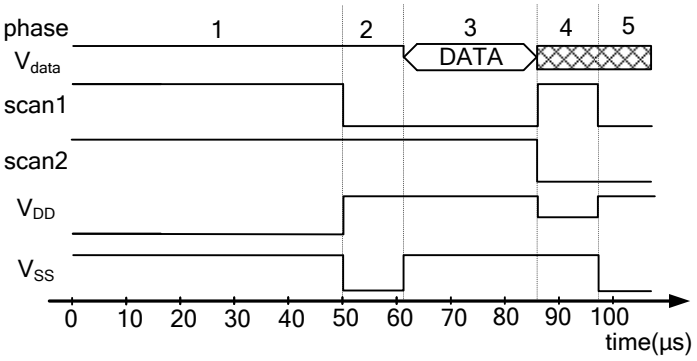

Fig. 7: Timing diagram for the various lines for the a-Si circuit.

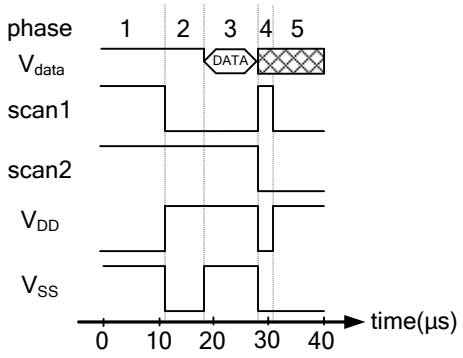

Fig. 8: Timing diagram for the various lines for the a-IGZO circuit.

III. Circuit Implementation in a-Si and a-IGZO Technologies

In this section, the programming process of the proposed pixel circuit is analysed in two thin film technlogies: a-Si TFT and a-IGZO TFT. To have a fair comparison, we should assume the same size of the pixel for both implementations. This in particular means equal sizes of the drive TFT, the switches and the storage as well as the OLED capacitor. Fig. 6 shows the structure of the circuit. As can be seen, it is composed of three TFTs and one capacitor. V_{data} provides the data voltage, and V_{DD}, V_{SS}, scan1, and scan2 are the controlling lines. Fig. 7 and Fig. 8 demonstrate the driving sequence of the pixel using a-Si and a-IGZO TFTs, respectively. The driving sequence divided into five main phases which will be elaborated in the following.

A. Driving Sequence

In the first phase, i.e. the initialization phase, scan1, scan2 and V_{DD} are high, high, and low, respectively. V_{SS} is also high, making T_1 OFF. Since the voltage of the cathode in the OLED is greater than that of the anode, the OLED is reversed-bias and acts as a capacitor C_{OLED}[2], similar to C_1 in Fig. 3. At this time, V_{data} is set to a constant voltage (initializing), precharging v_d and the top plate of C_s through the two switches S_1 and S_2.

In the second phase, i.e. the compensation phase, scan1 and scan2 are low and high respectively. V_{DD} turns back to its maximum, introducing a jump on node v_d via the floating OLED capacitor C_{OLED}. This causes v_d to reach a relatively high voltage. While V_{data} remains unchanged [3], V_{SS} is pulled down, turning the drive TFT T_1 ON. As a result of that, C_{OLED} starts discharging through T_1 with a constant rate for a period of t_{comp}. Here, t_{comp} should be chosen appropriately to reach a minimum error, as will be discussed below.

In the third phase, i.e. the programming phase, scan1, scan2, V_{DD} are low, high, and high, respectively. Pulling V_{SS} up, T_1 turns off and C_{OLED} stops discharging. Assuming a total compensation time of t_{comp} and according to (8), the final voltage of the bottom plate of C_{OLED} (v_d) can be written as

$$V_d = V_{\text{ind}} + \frac{Kt_{\text{comp}}}{2C_{\text{OLED}}}\left[2\left(V_{\text{data2}} - V_{\text{th0}}\right)\Delta V_{\text{th}} - \Delta V_{\text{th}}^2\right], \quad (11)$$

where V_{g0} in (9) is replaced by V_{data2}, and represents the value of V_{data} in the second phase.

Simultaneously, the data voltage (V_{data}) is also applied to the top plate of C_s via S_2.

The fourth phase, i.e. the charge sharing phase, starts with pulling scan1 up and scan2 down. Doing so, the bottom plate of C_{OLED} connects to the top plate of C_s and a charge sharing occurs. The final voltage of the top plates after settling depends on the ratio of the two capacitors. Assuming a ratio of $C_s/C_{\text{OLED}} = \alpha$ and according to (11), this voltage would be

$$\begin{aligned} V_g =& \frac{\alpha}{\alpha+1}V_{\text{data}} \\ &+ \frac{1}{\alpha+1}(V_{\text{ind}} + \frac{Kt_{\text{comp}}}{2C_{\text{OLED}}}\left[2\left(V_{\text{data2}} - V_{\text{th0}}\right)\Delta V_{\text{th}} - \Delta V_{\text{th}}^2\right]). \end{aligned} \quad (12)$$

At this time, since the overall voltage across C_{OLED} decreases (especially for smaller V_{data}s), the OLED may enter the forward-bias regime and it no longer acts as a capacitor. To avoid this to happen, we reduce V_{DD} in the beginning of the phase.

In the final phase, i.e. the driving phase, scan1 and scan2 are low, and V_{DD} returns to its default value, and V_{SS} is pulled down. A current proportional to the voltage of C_s, which is given by (12), passes through the OLED, i.e,

$$\begin{aligned} I_{\text{OLED}} &= \frac{1}{2}K(V_g - V_{\text{th}})^2 \\ &= \frac{1}{2}K(\frac{\alpha}{1+\alpha}V_{\text{data}} + \frac{1}{1+\alpha}(V_{\text{ind}} + \frac{Kt_{\text{comp}}}{2C_{\text{OLED}}} \\ &\left[2\left(V_{\text{data2}} - V_{\text{th0}}\right)\Delta V_{\text{th}} - \Delta V_{\text{th}}^2\right]) - V_{\text{th}})^2 \\ &= \frac{1}{2}K(\frac{\alpha}{1+\alpha}V_{\text{data}} + \frac{1}{1+\alpha}(V_{\text{ind}} + \frac{Kt_{\text{comp}}}{2C_{\text{OLED}}} \\ &\left[2\left(V_{\text{data2}} - V_{\text{th0}}\right)\Delta V_{\text{th}} - \Delta V_{\text{th}}^2\right]) - \Delta V_{\text{th}} - V_{\text{th0}})^2. \end{aligned} \quad (13)$$

As can be seen, there is an undesirable $V_{\text{th}}-$dependent term (the error) in (11), which is

$$\begin{aligned} V_{\text{error}} =& \\ &\frac{1}{1+\alpha}(\frac{Kt_{\text{comp}}}{2C_{\text{OLED}}}\left[2\left(V_{\text{data2}} - V_{\text{th0}}\right)\Delta V_{\text{th}} - \Delta V_{\text{th}}^2\right]) \\ &- \Delta V_{\text{th}}. \end{aligned} \quad (14)$$

This is a parabolic curve with respect to ΔV_{th}. Assuming $0 < \Delta V_{\text{th}} < \Delta V_{\text{th,max}}$, the maximum (absolute) voltage error occurs either at the peak (vertex) of the curve or at the edge of the definition range (where $\Delta V_{\text{th}} = \Delta V_{\text{th,max}}$). To reach a minima for the error, the larger one of the two should be minimized, and this proves to be where the error values at these two points are equal. Based on this, we derive the optimum value for the compensation time as

$$t_{\text{comp,opt}} = \frac{C_s + C_{OLED}}{K\left[V_{\text{data2}} - V_{\text{th0}} - (\sqrt{2}-1)\Delta V_{\text{th,max}}\right]} \quad (15)$$

and the maximum voltage error as

$$V_{\text{error,max}} = \frac{(3-2\sqrt{2})\Delta V_{\text{th,max}}^2}{2\left[V_{\text{data2}} - V_{\text{th0}} - (\sqrt{2}-1)\Delta V_{\text{th,max}}\right]} \quad (16)$$

Therefore, the error is totally determined by the gate voltage during the second phase V_{data2} (or equivalently the overdrive voltage $V_{ov} = V_{\text{data2}} - V_{\text{th}}$) and the maximum V_{th} shift ($\Delta V_{\text{th,max}}$). For $V_{\text{th0}} = 2V$, this maximum error is plotted in Fig. (9) as a function of the overdrive voltage during the compensation phase. As can be seen, for large overdrive voltages, the error is very small and negligible.

We can use (15) to calculate an approximation[4] for t_{comp}. We can alternatively perform the procedure in section II (and related to Fig. 4) to calculate the optimum compensation time. The most accurate method, however, is to use a trial-and-error approach through simulation with the real circuit models. Using the extracted model parameters of an a-Si TFT and for an OLED capacitor of $C_{\text{OLED}} = 1pF$ and α between 0.5 and 1, this optimum time as well as the corresponding current error is obtained and plotted in Fig. 10. The same trend can be followed for an a-IGZO TFT.

B. Driving/Circuit Discrepancies in the Two Technologies

The phases and their driving sequence are exactly the same for both circuits implemented in a-Si and a-IGZO technologies. As such, if we simply get the signaling of the circuit in

[2]From [12] a typical value for this capacitance is $200-400pF/mm^2$. An area of $500\mu m^2$ for the OLED would result to an OLED capacitor of $1pF$.

[3]V_{data} can change here to a different value of that in phase 1, but, for whatever V_{data} in either phases, one should make sure that the drive transistor T_1 always remains in the saturation region, i.e. $V_{D1} > V_{G1} - V_{\text{th1}}$, where V_{D1}, V_{G1} and V_{th1} are the drain voltage, the gate voltage and the threshold voltage of T_1.

[4]This is indeed an apprpximate value because all the secondary effects, e.g. the channel length modulation, as well as the junction and parasitic capacitances of the drive TFT are neglected.

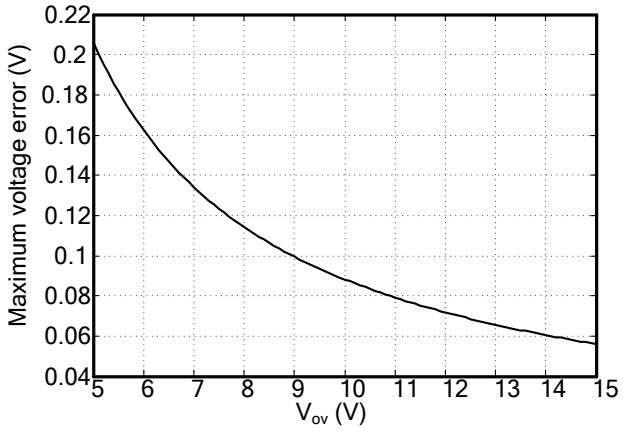

Fig. 9: Maximum voltage error rate as a function of overdrive voltage during the second phase for a threshold voltage shift of 3V.

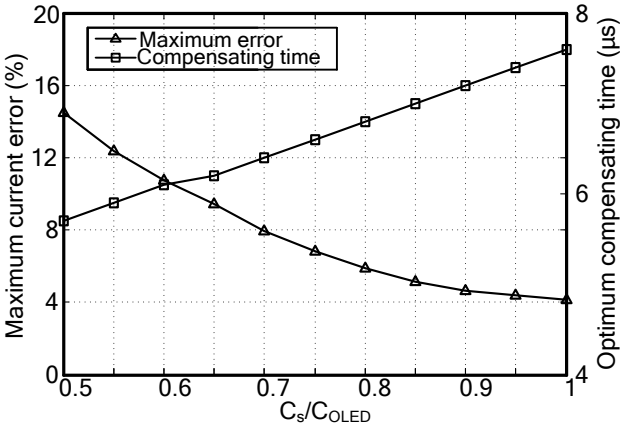

Fig. 10: Profile of the optimum compensation time and maximum current error as a function of $\alpha = C_s/C_{\text{OLED}}$.

one technology (as it is) and apply it to the circuit implemented in the other technology, it will work, probably with a different rate of error. In order to adjust the error to its minimum, we need to make some modifications in both the circuit parameters and the timings of the waveform itself. What we should do first is to choose proper sizes for the TFTs. As already mentioned, we choose the same size for all the constituent components of the two circuit implementations in the two technologies. As for the drive TFT, the aspect ratio is chosen to provide enough driving current for the OLED. This sets the lower limit. The upper size limit, however, is imposed by any inaccuracy in the time setting during the compensation phase. A timing error can occur because of the driving circuits themselves or as a result of different interconnect-associated delays of different pixels over the display area. Assuming a maximum timing error of Δt, the voltage deviation during the compensation phase would be

$$\Delta V_c = \frac{K}{C_s} V_{\text{ov}}^2 \Delta t. \tag{17}$$

Thus, a large K would be followed with a large voltage error. The same conclusion can be drawn with regard to V_{ov} during the compensation phase. This too, puts a limit on choosing

TABLE I: Parameters of the circuit.

	Value	
Parameter	a-Si	a-IGZO
T_1	W/L=10μm/10μm	W/L=10μm/10μm
S_1	W/L=20μm/10μm	W/L=20μm/10μm
S_2	W/L=20μm/10μm	W/L=20μm/10μm
C_s	1pF	1pF
V_{data}	0V$\sim$20V	0V$\sim$13V
scan1	0V/30V	0V/20V
scan2	0V/30V	0V/20V
V_{DD}	0V/10V/20V	0V/20V
V_{SS}	0V/30V	0V/20V

TABLE II: Summery of model parameters.

	Value	
Parameter	a-Si	a-IGZO
Equivalent field effect mobility (μ_{FET})	$1.2cm^2V^{-1}s^{-1}$	$15cm^2V^{-1}s^{-1}$
Sub-threshold slope (S_{f0})	0.5V/dec	0.25V/dec
Reference OFF current (I_{off0})	5pA	1pA
Normalized contact resistance (R_cW)	$1000\Omega - cm$	$100\Omega - cm$
Threshold voltage (V_{th})	2V	2V
Normalized overlap capacitance[5]	8pF/cm	8pF/cm
Normalized gate insulator capacitance	20nF/cm^2	20nF/cm^2

an appropriate value for V_{data2}, which is in trade-off with the maximum voltage error in (16).

For the switches, the limited size of the pixel does not allow us to incorporate large sizes to have better conductivity and higher speed. The pedestal error (clock feedthrough and charge injection) is another factor that needs to be taken into consideration in choosing the switch size. Due to very low ON resistance of the a-Si transistors, a higher driving voltage of 30V is chosen to have a reasonable settling time. Apart from that, since the maximum data voltage for a-Si implementation is 20V (to have the same maximum OLED current as the a-IGZO implementation), the gate voltage of switch S_2 must be sufficiently larger than 20V to allow a low enough switch resistance.

Another discrepancy between the two technologies arises during the forth phase when V_{DD} needs to drop to a lower voltage. As can be seen in Fig. (7), after the third phase, V_{DD} is pulled down to a mid-level and not to the ground. Otherwise, the final voltage stored on C_s, which then provides the overdrive biasing voltage of T_1, would be too small that cannot supply a reasonably large enough current to drive the OLED. Due to almost one order of magnitude higher mobility of an a-IGZO TFT, this need not be done for the other circuit, thus giving us the advantage of employing a two-level supply voltage rather than a three-level one.

IV. Simulation Results

The proposed pixel circuit with parameters listed in Table I has been implemented with both a-Si and a-IGZO TFTs, and simulated with Verilog-AMS extracted model based on real measurement data [13-16]. A list of important parameters used in the models is summarized in Table II.

A sample transient waveform of the drain and gate voltage of the drive a-Si TFT is illustrated in Fig. 11. The waveforms

[5]An overlap of 1μm on drain and source sides for the minimum gate length of 10μm is assumed.

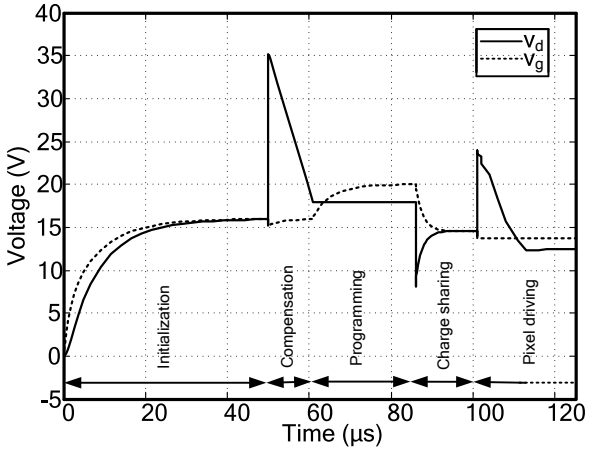

Fig. 11: Transient waveform of gate and drain voltages using a-Si TFTs.

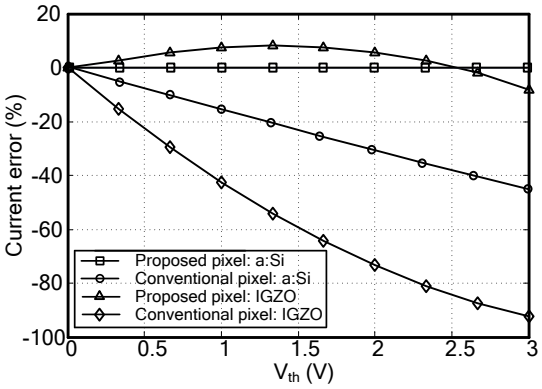

Fig. 12: Measured current error as a function of the threshold voltage shift in the drive TFT.

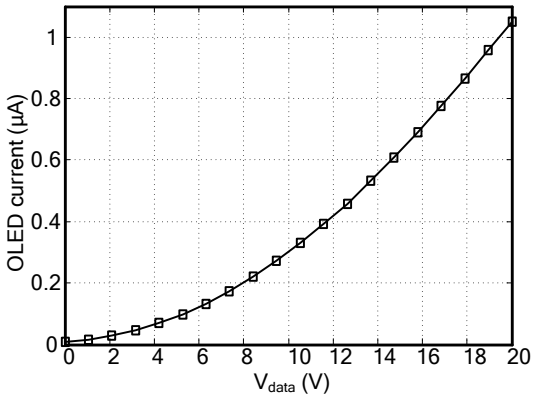

Fig. 13: OLED current as a function of V_{data} (a-Si implementation).

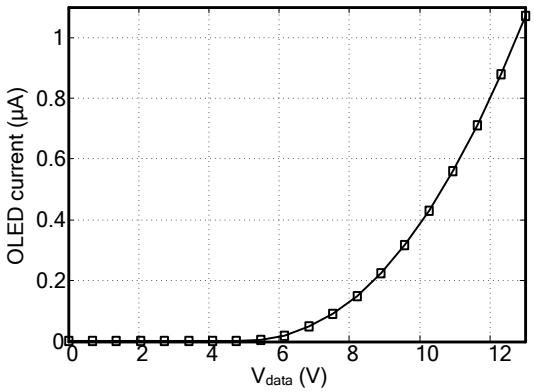

Fig. 14: OLED current as a function of V_{data} (a-IGZO implementation).

are similar for a-IGZO model. The total programming times are $91\mu s$ and $26\mu s$ for the a-Si and the a-IGZO implementation, respectively. Fig. 12 shows the current error for a 3V shift in the threshold voltage of T_1 as well as the relative error in a conventional $2-$TFT pixel (Fig. (1)) with the same size of the drive and the switch TFTs used in the proposed circuit. As can be seen, the maximum error is almost zero for the a-Si circuit, while this is around 8% for the a-IGZO implementation. The larger error of a-IGZO circuit is because of the low value of overdrive voltage during the compensation phase ($V_{\text{ov}} = 5V$). A larger value, as explained in section III(B), would result in high susceptibility to any timing error of the pixel. The overdrive voltage for a-Si circuit during the compensation period is 14V. The profiles of the OLED current versus V_{data} are also depicted in Fig. 13 and Fig. 14.

V. Conclusion

A pixel circuit comprising three TFTs and one capacitor (3T1C), controlled by two scan lines is presented. For maintain fair comparison, identical component sizes is chosen for the two circuits in two different technologies of the same pixel area. The simulation results using established VerilogA models show that the maximum non-uniformity in the OLED current is near zero for the a-Si implementation when experiencing a 3V shif of the threshold voltage. The a-IGZO circuit, however, shows an error of around 8% while being 3.5 times faster than its equivalent a-Si circuit. This demonstrates that the accuracy-speed trade-off of transistor-based circuits holds here as well.

Compared to the 2-TFT pixel, the circuit presented here requires an additional TFT and scan line. As such, the circuit would not impose restrictions on pixel size, although the requirements on driving sequence including switching power lines may require a custom driver. The pixel layout needs to be optimized so as to accommodate the size of the OLED capacitor, which is crucial in determining the compensation time.

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References

[1] G.R. Chaji and A. Nathan, " LTPS vs Oxide Backplanes for AMOLED Displays: System Design Considerations and Compensation Techniques", *SID Symposium Digest of Technical Papers*, Vol. 45, Issue 1, pp. 153-156, 2014.

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", *Nature*, vol. 432, pp. 488-492, 2004.

[3] J. Jang, M. Mativenga and J. Choi, “Stabilities of TFTs under bias-stress”, *ECS Transactions*, vol. 33, pp. 31-39, 2010.

[4] S. Jeon, S. Ahn, I. Song, C. Kim, U. Chung, E. Lee, I. Yoo, A. Nathan, S. Lee, K. Ghaffarzadeh, J. Robertson, and K. Kim, “Gated three-terminal device architecture to eliminate persistent photoconductivity in oxide semiconductor photosensor arrays”, *IEEE Journal of Solid-State. Circuits*, vol. 39, no. 9, pp. 1477-1486, 2004.

[5] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, “Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic”, *IEEE Journal of Solid-State. Circuits*, vol. 39, no. 9, pp. 1477-1486, 2004.

[6] J. Goh, H-J. Chung, and J. Jang, “A new pixel circuit for active matrix organic light emitting diodes”, *IEEE Electron Device. Lett.*, vol. 23, no. 9, pp. 544-546, 2002.

[7] J. Goh, J. Jang, K. Cho, and C. Kim, “A new a-Si:H thin-film transistor pixel circuits for active matrix organic light-emitting diodes”, *IEEE Electron Device. Lett.*, vol. 24, no. 9, pp. 583-585, 2003.

[8] G.R. Chaji, P. Servati, and A. Nathan, “driving scheme for stable operation of the 2-TFT a-Si AMOLED pixel”, *Electron. Lett.*, vol. 41, pp. 499500, Apr. 2005.

[9] B-H. You, J-H. Lee, and M-K. Han, “Polarity Balanced driving scheme to suppress the degradation of Vth in a-Si:H TFT due to the positive gate bias stress for AMOLED”, *IEEE Journal of Display Technology*, vol. 3, no. 2, pp. 40-44, 2007.

[10] A. Nathan, R. Chaji, and S-J. Ashtiani, “Driving Schemes for a-Si and LTPS AMOLED displays”, *IEEE/OSA Journal of Display Technology*, vol. 1, no. 2, pp. 267-277, 2005.

[11] M. Bagheri, S. J. Ashtiani, and A. Nathan, “A Fast Driving Scheme Voltage-Programmed Pixel Structure for AMOLED Displays”, *IEEE Journal of Display Technology*, vol. 6, pp. 191-195, Apr. 2010.

[12] J. Jacobs, D. Hente, E. Waffenschmidt, “Driving for OLEDs”, *IEEE 42nd Industry Applications Conference*. 200. pp. 1147-1152, Sept. 2007.

[13] P. Servati, D. Striakhilev, and A. Nathan, “Above-threshold parameter extraction and modeling for amorphous silicon thin-film transistors”, *IEEE Trans. Electron Devices*, vol. 50, no. 11, pp. 2227-2235, 2003.

[14] S. Lee, A. Nathan et al., “Modeling Sub-Threshold Current-Voltage Characteristics in Thin Film Transistors”, *IEEE Journal of Display Technology*, vol. 9, no.11, Nov. 2013.

[15] S. Lee, A. Nathan et al., “LateNews Paper: Modeling CurrentVoltage Behaviour in Oxide TFTs Combining Traplimited Conduction with Percolation”, *Digest of Technical papers, International Symposium, Display Week 2013*, SID 2013, vol. 44, no. 1, pp. 2225, June 2013.

[16] S. Lee, A. Nathan et al., “Analytical Field-Effect Method for Sub-gap States Extraction in Amorphous Semiconductor Thin Film Transistors”, *IEEE Electron Device Letters*, vol.33, no.7, Jun. 2012.

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