

Construction of Rate-Compatible Low Density Parity Check Codes for Fast Blind Rate Estimation

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Synopsis

Recently, Rate-Compatible LDPC (RC-LDPC) codes are attractive research topics on channel coding. RC-LDPC codes provide various coding rates and users can select suitable code rates according to channel conditions. However, RC-LDPC codes have a disadvantage that transmitter should notify the code rate to the receiver as a side-information. In this paper, we compare rate estimation techniques when the transmitter selects code rates randomly. And we have proposed RC-LDPC codes which could estimate rate more easy than conventional codes. By computer simulation, we obtain that performance of proposed techniques and proposed codes can estimate more higher than performance of conventional those.

KEYWORDS: Low-Density Parity-Check (LDPC) codes, Rate Estimation Technique, Rate-Compatible LDPC codes, Quasi-Cyclic codes, Greedy algorithm

1. Introduction

Low-Density Parity-Check (LDPC) codes were error-correcting codes proposed by Gallager[1] in 1962, and LDPC codes were confirmed that their performances in terms of Bit Error Rate (BER) were close to the Shannon-limit by using the Sum-Product decoding[2, 3, 4]. Recently, Rate-Compatible LDPC (RC-LDPC) codes were proposed that provide various coding rates and would allow the rate of this LDPC codes to be changed. In particular, RC-LDPC codes based on Quasi-Cyclic (QC) codes[5] stand out for their user-friendly design[6]. Still, we have to deal with the fact that the transmitter notifies the coding rate to the receiver as side-information. But in this case, the reliability of side-information becomes a new problem. And in reference [7, 8], the rate estimation technique was proposed that it estimated rates without side-information.

In this paper, we offer a rate estimation technique as a solution when the transmitter selects coding rates randomly without side-information on rate. And, we also offer the composition, which is used initial phase of a greedy algorithm[9] which expand the resolvable burst-erasure length[10], of parity check matrices of RC-LDPC codes when the receiver cannot receive all of the code. We will then make performance comparison with two rate estimation techniques. Proposed technique estimates the rate with the Log-Likelihood Ratio (LLR). As a result, it tries to reduce rate estimation errors by using the rate estimation technique.

2. LDPC codes and Sum-Product decoding

LDPC codes are linear codes defined by a parity check matrix H composed of the elements which are a lot of 0 and a few non 0. In this paper, we consider only binary LDPC codes that the elements of non 0 as 1.

Sum-Product decoding used to decode LDPC codes is a form of iterative decoding; it decodes by handing over the probability information between nodes based on the reception value. The outline of

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the algorithm of the Sum-Product decoding is as follows. Where a parity check matrix is $H = [H_{m,n}]$, sets of the row indexes with 1 in the m line are $\mathcal{N}(m) = \{n : H_{m,n} = 1\}$, sets of the row indexes with 1 in the n line are $\mathcal{M}(n) = \{m : H_{m,n} = 1\}$, $\mathcal{N}(m) \setminus n$: in the set that excludes n from $\mathcal{N}(m)$, and $\mathcal{M}(n) \setminus m$: in the set that excludes m from $\mathcal{M}(n)$. Moreover, F_n is the prior LLR of bit n , $\varepsilon_{m,n}$ is the LLR of bit n sent from check node m to bit node n , $z_{m,n}$ is the LLR of bit n sent from bit node n to check node m , z_n is the posteriori LLR of bit n , $\hat{\mathbf{y}}$ is the decoding sequence, I_{\max} is a maximum iteration count, and i is an iteration count.

[STEP1] Initialization

$i = 0$ and $z_{m,n} = F_n$ for each m, n .

[STEP2] Check nodes process

The following update equation is used for each m, n .

$$\varepsilon_{m,n} = \prod_{n' \in \mathcal{N}(m) \setminus n} \text{sign}(z_{m,n'}) \cdot f \left(\sum_{n' \in \mathcal{N}(m) \setminus n} f(|z_{m,n'}|) \right), \quad (1)$$

where

$$f(x) = \ln \frac{e^x + 1}{e^x - 1}. \quad (2)$$

[STEP3] Bit nodes process

The following update equation is used for each m, n .

$$z_{m,n} = F_n + \sum_{m' \in \mathcal{M}(n) \setminus m} \varepsilon_{m',n}, \quad (3)$$

$$z_n = F_n + \sum_{m \in \mathcal{M}(n)} \varepsilon_{m,n}. \quad (4)$$

[STEP4] Termination judgment

The decoding sequence $\hat{\mathbf{y}}$ is generated by hard decision of z_n . If $\hat{\mathbf{y}}H^T = \mathbf{0}$, output $\hat{\mathbf{y}}$. Also, if $i = I_{\max}$, output $\hat{\mathbf{y}}$. If $\hat{\mathbf{y}}H^T \neq \mathbf{0}$, increase the iteration count like $i = i + 1$ and return to STEP2.

3. Rate-Compatible Low-Density Parity-Check (RC-LDPC) codes

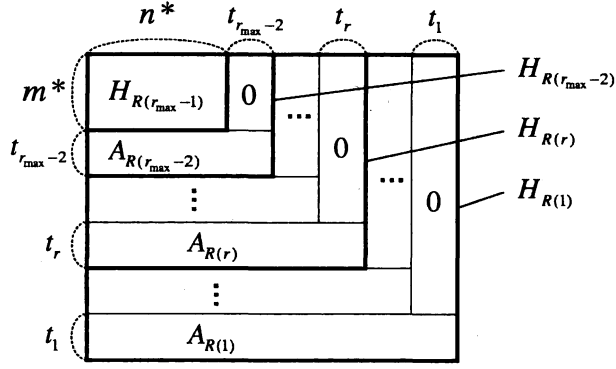
We define $H_{R(r)}$ is a parity check matrix of a RC-LDPC code $C_{R(r)}$ whose rate is $R(r)$, where $0 < R(1) < R(2) < \dots < R(r_{\max}) = 1$, $r = 1, 2, 3, \dots, r_{\max}$. $R(r_{\max})$ is a rate of an uncoded word. As shown in Fig. 1, we define $H_{R(r_{\max}-1)}$ is an $m \times n$ parity check matrix for codeword $C_{R(r_{\max}-1)}$, $H_{R(r_{\max}-2)}$ is an $(m + t_{r_{\max}-2}) \times (n + t_{r_{\max}-2})$ parity check matrix consisting of $H_{R(r_{\max}-1)}$, a $t_{r_{\max}-2} \times (n + t_{r_{\max}-2})$ parity check matrix $A_{R(r_{\max}-2)}$ and an $m \times t_{r_{\max}-2}$ zero matrix $\mathbf{0}$ as follows,

$$H_{R(r_{\max}-2)} = \left[\begin{array}{c|c} H_{R(r_{\max}-1)} & \mathbf{0} \\ \hline A_{R(r_{\max}-2)} & \end{array} \right], \quad (5)$$

$$R(r_{\max} - 1) = (n - m)/n, \quad (6)$$

$$R(r_{\max} - 2) = (n - m)/(n + t_{r_{\max}-2}), \quad (7)$$

where $H_{R(r_{\max}-1)}$ and $H_{R(r_{\max}-2)}$ are of full rank.



* These parameters are for $H_{R(r_{\max}-1)}$

Figure 1 Composition of parity check matrices of RC-LDPC codes.

In the same way, parity check matrices for $R(1)$ are recurrently defined. As a result, $H_{R(r)}$ and $R(r)$ are generally shown as follows,

$$H_{R(r)} = \left[\begin{array}{c|c} H_{R(r+1)} & \mathbf{0} \\ \hline A_{R(r)} & \end{array} \right], \quad (8)$$

$$R(r) = (n - m) / \left(n + \sum_{i=r}^{\max-2} t_i \right), \quad (9)$$

where t_i is the difference in the number of columns between $H_{R(i)}$ and $H_{R(i+1)}$. $H_{R(r)}$ obtained thus is of full rank for all r ($1 \leq r \leq r_{\max} - 1$). And the number of information bits $k = n - m$ is invariable regardless of rates $R(r)$.

4. RC-LDPC codes based on QC codes

In this section, we consider RC-LDPC codes based on the QC codes. A parity check matrix of a (J, L) QC-LDPC code of length $N = pL$ is defined as follow,

$$H_{QC} = \begin{bmatrix} I(p_{0,0}) & I(p_{0,1}) & \cdots & I(p_{0,L-1}) \\ I(p_{1,0}) & I(p_{1,1}) & \cdots & I(p_{1,L-1}) \\ \vdots & \vdots & \ddots & \vdots \\ I(p_{J-1,0}) & I(p_{J-1,1}) & \cdots & I(p_{J-1,L-1}) \end{bmatrix}, \quad (10)$$

where for $0 \leq j \leq J - 1$, $0 \leq l \leq L - 1$, $I(p_{j,l})$ represents the circulant permutation matrix with a 1 at column- $\{(r + p_{j,l}) \bmod p\}$ for row- r , $0 \leq r \leq p - 1$, and 0 elsewhere. p is natural number.

Also, let T_1 be a $pJ \times pJ$ matrix represented as follow,

$$T_1 = \begin{bmatrix} 1 & & & & & \\ 1 & 1 & & & & \mathbf{0} \\ & 1 & 1 & & & \\ & & \ddots & \ddots & & \\ & & & \ddots & \ddots & \\ \mathbf{0} & & & 1 & 1 & \\ & & & & 1 & 1 \end{bmatrix}. \quad (11)$$

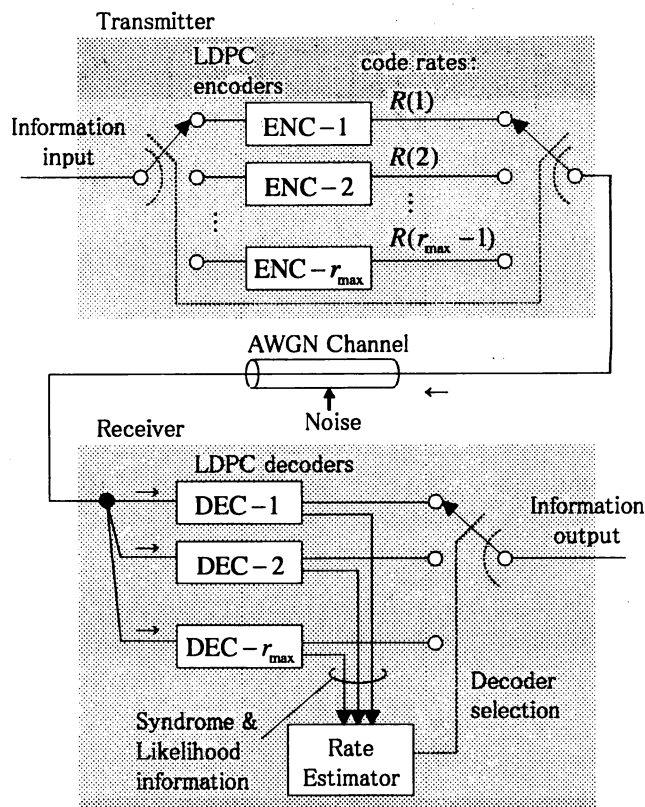


Figure 2 Block composition chart of transmitter and receiver.

At this time, a parity check matrix $H_{R(1)}^{QCT}$ is defined as $H_{R(1)}^{QCT} = [H_{QC}|T_1]$. As a result, $H_{R(2)}^{QCT}$ is a $pJ \times p(J+L)$ matrix, $H_{R(2)}^{QCT}$ is a $(pJ - t_1) \times (p(J+L) - t_1)$ matrix, $H_{R(\max-1)}^{QCT}$ is a $\left(pJ - \sum_{i=1}^{\max-2} t_i\right) \times \left(p(J+L) - \sum_{i=1}^{\max-2} t_i\right)$ matrix. Generally, $H_{R(r)}^{QCT}$ is a $\left(pJ - \sum_{i=1}^{r-1} t_i\right) \times \left(p(J+L) - \sum_{i=1}^{r-1} t_i\right)$ matrix. Also, the number of information bits is always $k = pL$ bits.

5. Proposed techniques

5.1 Rate estimation techniques

Figure 2 shows the composition of the transmitter and receiver that applies RC-LDPC codes. The transmitter selects the rate according to channel conditions, and encodes the information bits with the encoder. Then the transmitter continuously transmits the codes. While, the receiver operates the decoders correspond to each rate of the encoders in parallel as shown in Fig. 3. The rate estimation is done with the rate estimator in the receiver of Fig. 2, and selects the decoder based on the syndrome output and the likelihood of information on each decoder. We explain the rate estimation technique as follows.

[STEP1]

Sum-Product decoding is limited to the amount of iteration in a regulated number (i_{\max}); each rate of the decoders is corresponding to its respective rate of the encoders.

[STEP2]

Rate $\hat{R}(r)$, which can be decoded, only happens when the output $\hat{\mathbf{y}}$ is $\hat{\mathbf{y}}H_{\hat{R}(r)}^T = 0$, and only

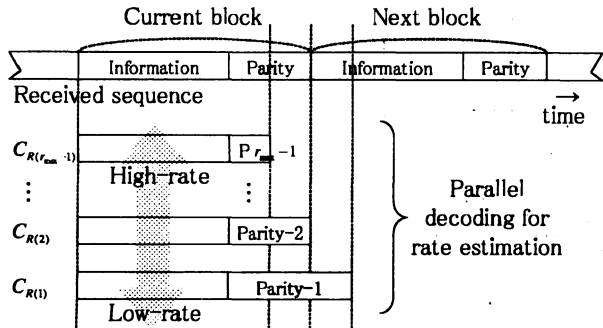


Figure 3 Parallel decoding of unknown coding rate for rate estimation.

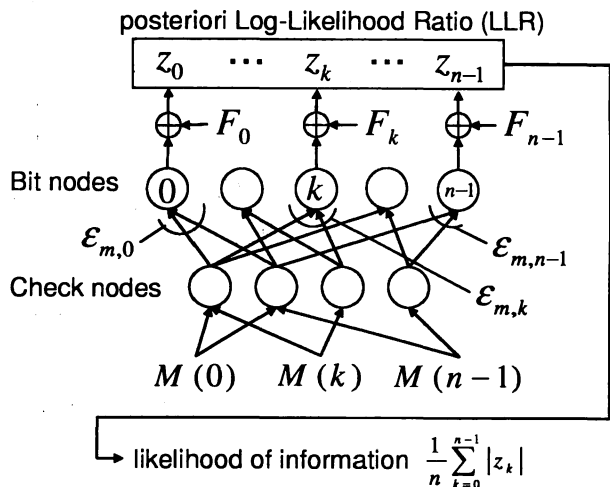


Figure 4 Computational method of the likelihood of information.

when $\hat{y}H_{R(r)}^T = 0$ is in a regulated number. When two or more rates are available to be decoded in a regulated number, the rate estimator selects the decoder which is the lowest rate of those and takes it as an estimation rate.

[STEP3]

If it is not possible to decode in a regulated number, the operations of STEP 1 and 2 are repeated as long as total numbers of iteration do not exceed I_{max} .

[STEP4]

If totals of iteration exceed I_{max} , it bases its estimate on the likelihood of information on each decoder because the code cannot be decoded.

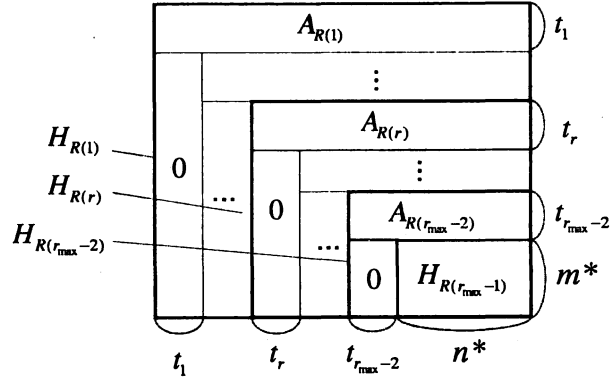
Even at times when it cannot decode the Sum-Product decoding by the maximum iteration count, the rate estimation technique enables the program to approximating the correct rate. The bit error does not become 0 because it has failed in decoding even if the rate can be accurately estimated by using this rate estimation technique. To correct this error, it is necessary to execute the Sum-Product decoding again and again, to add parity bits by using retransmission, and to do decoding over again. In our study, it will be remained as a future work.

Next, we explain method calculating the likelihood of information on the decoder. When iteration of Sum-Product decoding reaches the maximum iteration, the absolute value of the posteriori LLR ($|z_n|$) of each bit output with each decoder is assumed to be reliability of the bit. And, when the mean value of the reliability of each decoder is taken as shown in Fig. 4, the mean value is assumed to be the likelihood of information on the decoder. The rate of the decoder by which the likelihood of information becomes the maximum is assumed to be estimation rate $\hat{R}(r)$. That is, $\hat{R}(r)$ is shown by the next equation.

$$\hat{R}(r) = \arg \max_{R(r)} \left(\frac{1}{N_{R(r)}} \sum_{n=0}^{N_{R(r)}-1} |z_n| \right), \quad (12)$$

where z_n is the posteriori LLR shown by Eq. (4), and $N_{R(r)}$ is given as follow,

$$N_{R(r)} = p(J + L) - \sum_{i=1}^{r-1} t_i. \quad (13)$$



* These parameters are for $H_{R(r_{max}-1)}$

Figure 5 Composition of parity check matrices of RC-LDPC codes.

Conventional technique estimates rates based on syndrome and the likelihood of information. But the proposed technique estimates rates only from the likelihood of information. That is, termination judgment of syndrome process is not used in Sum-Product decoding. So, process from STEP1 to STEP3 is repeated until $i = I$ in section . The likelihood of information is calculated from Eq. (12), and the rate of the decoder by which the likelihood of information becomes the maximum is assumed to be estimation rate $\hat{R}(r)$.

5.2 Composition of a parity check matrix used initial phase of a greedy algorithm

We make parity check matrices shown as Fig. 5 to be able to estimate rate when the receiver cannot receive all of the code. So, we use a parity check matrix $H = [T_2 | H_{QC}]$, where

$$T_2 = \begin{bmatrix} 1 & 1 & & & & \\ & 1 & 1 & & & \mathbf{0} \\ & & 1 & 1 & & \\ & & & \ddots & \ddots & \\ \mathbf{0} & & & & 1 & 1 \\ & & & & & 1 \end{bmatrix}, \quad (14)$$

and H_{QC} is shown as Eq. (10). We call this code conventional code.

When the receiver cannot receive all of the code, the receiver can regard unreceived part of the code as burst erasure. Therefore, we expand the resolvable burst-erasure length from backmost column of the code by using initial phase of a greedy algorithm, which is proposed by Wadayama. The resolvable burst-erasure length is checked by L_{max} -algorithm, which is proposed by Yang and Ryan. Initial phase of a greedy algorithm is the following. Where the sub-matrix $H_{QC}(p, q)$ is defined by

$$H_{QC}(p, q) \triangleq (\mathbf{h}_p, \mathbf{h}_{p+1}, \dots, \mathbf{h}_{q-1}, \mathbf{h}_q). \quad (15)$$

[STEP1]

$$p = n - 1 \text{ and } q = n.$$

[STEP2]

Perform L_{max} -algorithm for $H_{QC}(p, q)$. If $H_{QC}(p, q)$ is not resolvable, swap \mathbf{h}_p and \mathbf{h}_r , where r is chosen randomly from the range $[1, p - 1]$.

Table 1 Parity check matrices for simulation.

Parity check matrix	n	k	m	$R(r)$
$H_{R(1)}^{QCT}$	2688	1536	1152	0.571
$H_{R(2)}^{QCT}$	2496	1536	960	0.615
$H_{R(3)}^{QCT}$	2304	1536	768	0.667
$H_{R(4)}^{QCT}$	2112	1536	576	0.727
$H_{R(5)}^{QCT}$	1920	1536	384	0.800
$H_{R(6)}^{QCT}$	1728	1536	192	0.889

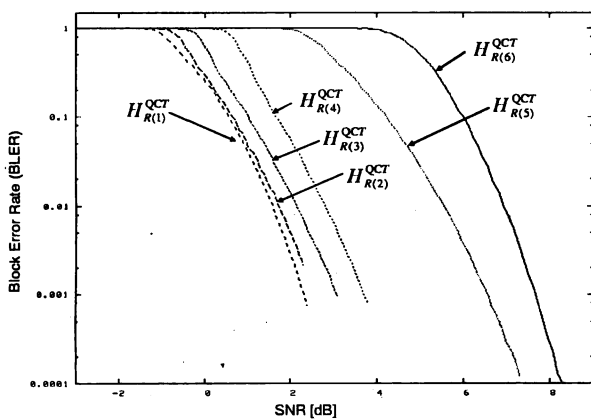


Figure 6 BLER performance of RC-LDPC codes based on QC codes ($I_{\max} = 100$).

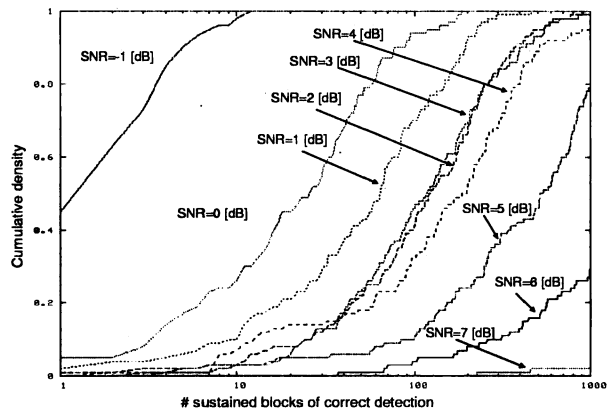


Figure 7 Performance of rate estimation (CDF of number of blocks which succeeded at the rate estimation in conventional technique $I_{\max} = 5$).

[STEP3]

If the retrieval of swap reaches Q times, output $H_{QC}(1, n)$ and end this process, otherwise return to STEP2.

6. Performance evaluation

6.1 Performance evaluation of rate estimation techniques

By the computer simulation, we evaluate the performance of the rate estimation techniques. We consider the worst condition that the transmitter selects coding rates randomly without side-information. As well, the receiver do not know coding rates which transmitter selects, but codeword synchronous in first condition.

First of all, we evaluate basic performance of RC-LDPC codes based on QC codes used in computer simulation of rate estimation. Figure 6 shows results of simulation of Block Error Rate (BLER) performance in each rate of RC-LDPC codes based on (J, L) QC codes. Where, parity check matrices are $p = 192$, $J = 8$, $L = 6$, $r_{\max} = 7$, $t_1 = t_2 = \dots = t_6 = 192$. So, we obtain parity check matrices as shown Table 1. n is code length, k is the number of information bits. m is the number of parity bits, and $R(r)$ is coding rates. Maximum iteration count of Sum-Product decoding is $I_{\max} = 100$. We assume that BPSK modulation over AWGN channel is used. As shown in Fig. 6, RC-LDPC codes of

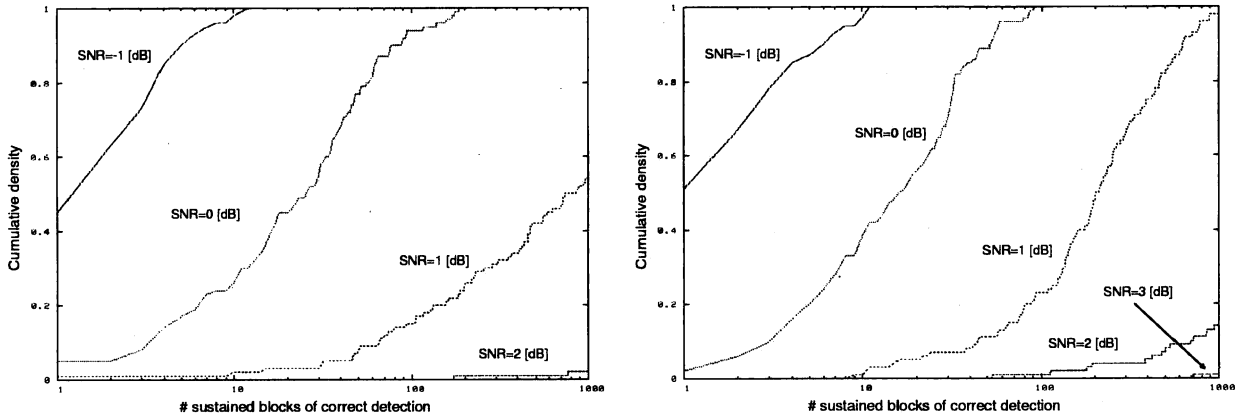


Figure 8 Performance of rate estimation (CDF of number of blocks which succeed at the rate estimation in proposed technique $I = 5$). Figure 9 Performance of rate estimation (CDF of number of blocks which succeed at the rate estimation in proposed technique $I = 20$).

high rates cannot decode in low SNR. In particular, BLER of $H_{R(6)}^{QCT}$ in SNR= 6[dB] is 1.00×10^{-1} , and in SNR= 5[dB] is 5.1×10^{-1} . So, we cannot hope that codes are decoded less than these SNR.

Figure 7 shows results of conventional technique, the receiver estimates rates of RC-LDPC codes, that the transmitter selects coding rates randomly and transmits 1000 blocks continuously. Horizontal axis is the number of sustained blocks of correct detection, and vertical axis is cumulative density function (CDF). Parity check matrices are the same as matrices used in computer simulation of Fig. 6. Maximum iteration of Sum-Product decoding is $I_{\max} = 5$. Figure 7 shows that conventional technique in high SNR like SNR= 7[dB] can estimate the correct rate in high probability, but it fails in the rate estimation in area more than 200 sustained blocks. And conventional technique in low SNR like SNR= 3[dB] estimate the correct rate only 50% in 100 sustained blocks.

Figure 8 shows results of proposed technique whose iteration is $I = 5$, and other parameters are the same as parameters used in computer simulation of Fig. 7. When we compare Fig. 7 with Fig. 8, it turns out that proposed technique could estimate more than conventional technique. Proposed technique from SNR= 3[dB] to SNR= 7[dB] could estimate rates of all blocks. So, it means that syndrome of Sum-Product decoding cannot be trusted for rate estimation. Performance of Fig. 8 SNR= -1[dB] and SNR= 0[dB] is same as performance of Fig. 7. The reason is that Sum-Product decoding of conventional technique cannot become $\hat{\mathbf{y}}H_{R(r)}^T = 0$.

Figure 9 shows results of proposed technique whose iteration is $I = 20$, and other parameters are the same as parameters used in computer simulation of Fig. 8. When we compare Fig. 8 with Fig. 9, it turns out that performance of Fig. 9 is worse than that of Fig. 8. In particular, CDF of $I = 5$, SNR= 1[dB] in 1000 sustained blocks is about half, and CDF of $I = 5$, SNR= 2[dB] in 1000 sustained blocks is about seventh part of $I = 20$.

Figure 10 shows CDF of each sustained blocks of correct detection in SNR= 1[dB] when I is changed. Horizontal axis is the number of I , and vertical axis is CDF. All of them are minimized by $I = 3$, and the more I increases, the worse CDF become. The analysis of this is remained as a future work.

From the above-mentioned simulation result, it turns out that the proposed technique, which estimates the rate only from the likelihood of information to estimate rates of RC-LDPC codes when the transmitter selects randomly, achieves performance that is superior to conventional technique, which estimates rates based on syndrome and the likelihood of information. It also turns out that

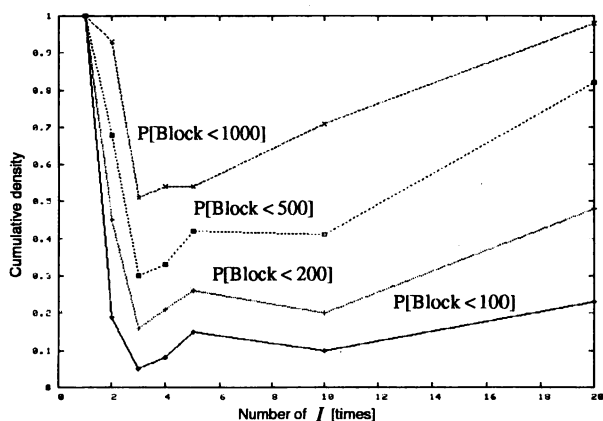


Figure 10 Effect of number of iterations (SNR=1[dB]).

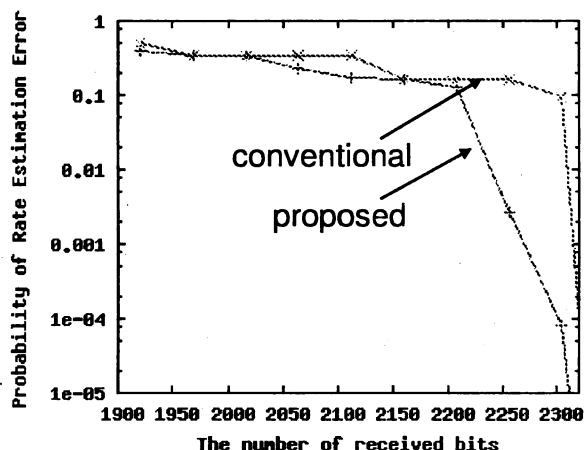


Figure 11 Performance of comparison of proposed and conventional codes (SNR=3[dB]).

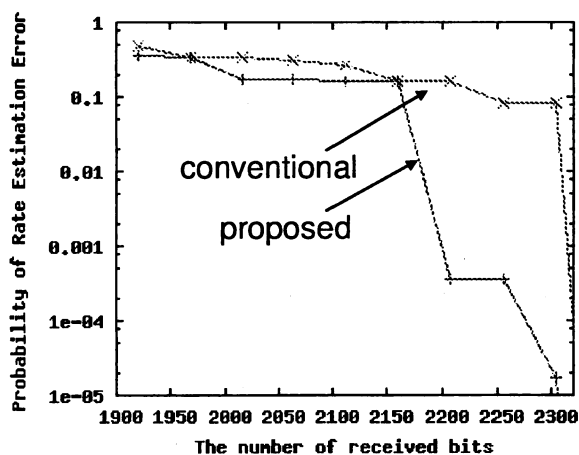


Figure 12 Performance of comparison of proposed and conventional codes (SNR=5[dB]).

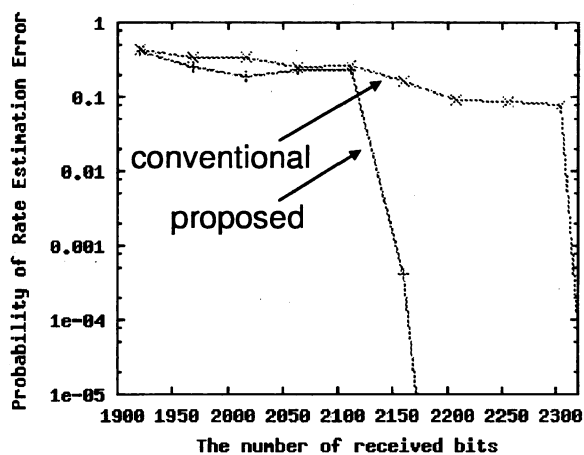


Figure 13 Performance of comparison of proposed and conventional codes (SNR=9[dB]).

performance of rate estimation is optimum when iteration of Sum-Product decoding of proposed technique is three times.

6.2 Performance evaluation of a parity check matrix used initial phase of a greedy algorithm

By the computer simulation, we evaluate the performance of a parity check matrix used initial phase of a greedy algorithm in the worst condition that the transmitter selects coding rates randomly without side-information on rate. As well as the section 6.1, the receiver do not know coding rates which transmitter selects, but perfect codeword synchronization is assumed.

The resolvable burst-erasure length from backmost column of conventional code is 384, and the resolvable burst-erasure length from backmost column of proposed code is 785 by using initial phase of a greedy algorithm. The code length of RC-LDPC codes which have the lowest rate is 2688 bits, and the number of iterations is 20.

Figures 11, 12 and 13 show performance comparisons of proposed and conventional codes. Horizontal axis is the number of received bits, and vertical axis is probability of rate estimation error. When the number of received bits is increased, probability of rate estimation error is decreased. On most of the results, performance of proposed codes is better than that of conventional codes. In order

to satisfy probability of rate estimation error of 10^{-5} at SNR= 9[dB], the proposed code requires only 2160 received bits compared to 2350 bits with the conventional code.

7. Conclusion

In this paper, we offered the rate estimation technique as a solution when the transmitter selected coding rates randomly without side-information on rate. We then compared rate estimation techniques. Proposed technique estimated the rate with LLR only. As a result, we showed that the proposed technique reduce rate estimation errors compared with conventional technique. And we also showed that performance of rate estimation of proposed code was higher than that of conventional code. The analysis of performance of rate estimation worsens as iteration of Sum-Product decoding increases is remained as a future work.

References

- [1] R. G. Gallager, "Low-density parity-check codes," in Research Monograph series. Cambridge, MIT Press, 1963.
- [2] F. R. Kschischang, "Factor graphs and the sum-product algorithm," *IEEE Trans. Inform. Theory*, vol. 47, no. 2, pp. 498–519, Feb. 2001.
- [3] D. J. C. MacKay, "Good error-correcting codes based on very sparse matrices," *IEEE Trans. Inform. Theory*, vol. 45, pp. 399–431, March 1999.
- [4] D. J. C. MacKay, R. M. Neal, "Near Shannon limit performance of low-density parity-check codes," *Electronics Letters*, vol. 32, pp. 1645–1646, Aug. 1996.
- [5] M. Fossorier, "Quasi-cyclic low density parity check codes," *Proc. ISIT2003*, p. 150, Yokohama, Japan, June 28–July 4 2003.
- [6] W. Matsumoto, H. Imai, "A study on rate-compatible LDPC codes," *Proc. ISITA2004*, pp. 529–534, Parma, Italy, Oct. 10–13 2004.
- [7] T. Yoshikawa, T. Tsujioka, H. Sugiyama, M. Murata, "A study on rate estimation technique of rate-compatible LDPC codes," *Tech. Rep. IEICE*, vol. 104, no. 721, CS2004-236, pp. 19–24, March 2005.
- [8] T. Yoshikawa, T. Tsujioka, H. Sugiyama, M. Murata, "Comparison of rate estimation techniques for rate-compatible LDPC codes," *Tech. Rep. IEICE*, vol. 105, no. 83, IT2005-4, pp. 18–23, May 2005.
- [9] T. Wadayama, "Greedy construction of LDPC codes for burst erasure channel," *Tech. Rep. IEICE*, vol. 104, no. 302, IT2004-44, pp. 35–40, Sept. 2004.
- [10] M. Yang, W. E. Ryan, "Performance of efficiently encodable LDPC codes in noise bursts on the EPR4 channel," *IEEE Trans. Magnetics*, Vol. 40, No. 2, pp. 507–512, March 2004.