Low leakage ZrO$_2$ based capacitors for sub 20 nm DRAM technology nodes

Milan Pešić, 1 Steve Knebel, 1 Maximilian Geyer, 1 Sebastian Schmelzer, 2 Ulrich Böttger, 2 Nadiia Kolomiiets, 3 Valeri V. Afanas’ev, 3 Kyuho Cho, 4 Changhwa Jung, 4 Jaewan Chang, 4 Hanjin Lim, 4 Thomas Mikolajick, 1,5 and Uwe Schroeder 1

1 NaMLab gGmbH, Noethnitzer Strasse 64, 01187 Dresden, Germany
2 RWTH Aachen, IWE2, Sommerfeld Strasse 24, 52074 Aachen, Germany
3 Laboratory of Semiconductor Physics, Katholieke Universiteit Leuven, B-3001 Leuven, Belgium
4 Samsung Electronics, Semiconductor Research Center, 1, Samsungeonja-ro, Gyeonggi-do, 445-701, Korea
5 Chair of Nanoelectronic Devices, Technische Universität Dresden, Noethnitzer Strasse 64, 01187, Dresden, Germany

During DRAM capacitor scaling a lot of effort was spent searching for new material stacks to overcome the scaling limitations of the current material stack, such as leakage and sufficient capacitance. In this study, very promising results for a SrTiO$_3$ based capacitor with a record low capacitance equivalent thickness value of 0.2 nm at target leakage current are presented. Due to the material properties of SrTiO$_3$ films (high vacancy concentration and low band gap), which are leading to an increased leakage current, a physical thickness of at least 8 nm is required at target leakage specifications. However, this physical thickness would not fit into an 18 nm DRAM structure. Therefore, two different new approaches to develop a new ZrO$_2$ based DRAM capacitor stack by changing the inter-layer material from Al$_2$O$_3$ to SrO, and the exchange of the top electrode material from TiN to Pt are presented. A combination of these two approaches leads to a capacitance equivalent thickness value of 0.47 nm. Most importantly, the physical thickness of < 5 nm for the dielectric stack is in accordance with the target specifications. Detailed evaluations of the leakage current characteristics lead to a capacitor model which allows the prediction of the electrical behavior with thickness scaling.

I. INTRODUCTION

For many decades, dynamic random access memory (DRAM) capacitors have been successfully scaled down to smaller nodes, but technology barriers which would limit further scaling became visible [1]. A reduction of capacitance equivalent thickness (CET) and the physical thickness of the ZrO$_2$ based stacks are challenging due to the exponentially enhanced leakage current for thinner dielectric layers. The thickness of the dielectric and the electrode materials needs to be scaled down as much as possible while maintaining the basic physical properties of the material. According to the international road map for semiconductors (ITRS) scaling should lead to a reduction in CET values down to 0.45 nm for a 20 nm and 0.4 nm for an 18 nm technology node [2]. Different schemes will be discussed to find a feasible pathway to an optimized capacitor dielectric for 18 nm DRAM nodes. In the first part of the study, new SrTiO$_3$ (STO) based devices are examined as a
prospective and promising successor of the ZrO$_2$ based DRAM nodes. Besides the introduction of the new dielectric two electrode options are considered. This is followed by two new approaches to re-develop the current ZrO$_2$-based workhorse. Firstly, a replacement of the Al$_2$O$_3$ with SrO interlayer material, which should lead to satisfying projected technology nodes and decrease of the leakage current, is evaluated [3]. Leakage current transport mechanisms are determined by the trap level depth, trap density in ZrO$_2$ and the conduction band offset (CBO). Therefore, a second pathway is the increase of the CBO between electrode and dielectric by usage of a high workfunction, inert, noble metal electrode. By increasing the CBO, the probability of an electron being injected to the first trap state decreases. Moreover, the low reactivity of the noble electrode material with the dielectric decreases the number of defects within the dielectric layer and increases the distance between the traps, accordingly. This results in a lower tunneling probability for electrons and lower leakage currents. In this work, the CBO for two different electrode materials titan-nitride and platinum (TiN, Pt) on atomic layer deposited ZrO$_2$/Al$_2$O$_3$/ZrO$_2$ (ZAZ, 6 nm) was examined by internal photoemission spectroscopy (IPE) and correlated to leakage current measurements. In addition, the scaling potential for a ZAZ dielectric by increasing the CBO was discussed based on leakage current simulation results of a ZAZ capacitor.

II. EXPERIMENTAL PROCEDURE

Overall three different types of capacitor structures were fabricated. In order to examine high k DRAM materials, a first set of STO based metal insulator metal (MIM) capacitors stacks was processed by physical vapor deposition (PVD) using SRO or Pt electrodes as described elsewhere [4]. The SRO based structures were deposited in-situ on oxidized silicon substrates by low-rate rf sputtering from pressed powder SRO and sintered STO targets. Pt electrode deposition was performed ex-situ. Growth conditions were a substrate temperature of 550 °C and a chamber pressure of 8·10$^{-3}$ mbar Ar for both the SRO and STO deposition. The initial partial pressure of other gases, for instance oxygen, is several orders of magnitude lower and settles in the range of 10$^{-7}$ mbar.

To investigate different interlayer materials in a ZrO$_2$ based capacitor, complete MIM stacks were prepared by an in-situ PVD process in a Bestec ultra high vacuum (UHV) cluster tool as reported by Knebel et al. [3]. ZrO$_2$/X/ZrO$_2$ stack (where X represents Al$_2$O$_3$ or SrO interlayer, respectively) was deposited on room temperature and sandwiched between TiN top and bottom electrodes deposited on 300 °C. Afterwards, ZrO$_2$ was crystallized by a 450 °C anneal for 10 min in a nitrogen atmosphere. Annealing at this temperature allows reaching a fully crystallized ZrO$_2$ layers with a k-value of ~40. The total dielectric stack thickness of all evaluated layers was 5-10 nm, whereas the thickness of the interlayer was preserved at about one monolayer (~0.3 nm).
For the purpose of characterization of the electrode influence on the capacitor performance production type ZAZ layers were deposited by atomic layer deposition (ALD) on chemical vapor deposition (CVD) based TiN bottom electrodes. The TiN bottom electrode was prepared by using TiCl₄ and NH₃ precursor. Afterwards, the dielectric stack was processed using trimethyl aluminum (TMA), a Zr based Cp organic precursor and O₃ as reactants. ZrO₂ was crystallized by a 550 °C anneal in a nitrogen atmosphere. Top electrodes (TE) were deposited in a BESTEC UHV sputtering tool (TiN) or a BESTEC e-beam evaporation tool (Pt), respectively. To form the individual TiN top electrode structures, platinum dots were evaporated onto the top TiN layer as a hard mask. Thus, the top TiN layer was removed outside the pads with a diluted standard clean 1 (SC-1) solution. For Pt top electrode characterization, the material was directly evaporated on the dielectric. The total dielectric stack thickness of evaluated layers was 5-6.5 nm.

In order to measure the workfunction of the different electrodes terraced oxide structures were prepared as described elsewhere [5]. Thermally grown SiO₂ on a Si sample was etched in diluted hydrofluoric acid (HF) to form terraces of different thickness. Thermal oxidation was followed by 10 minute long forming gas processing step in H₂ atmosphere at 400°C. Afterwards, the ZrO₂ high-k material and TiN electrode were deposited. Structuring and creation of the discrete Si/SiO₂/ZrO₂/TiN MOS structures were performed as described before using a SC1 clean. Electrical characterization of the capacitors was done in a semiautomatic probe station from Cascade Microtech and an Agilent B1500A semiconductor device parameter analyzer, equipped with a capacitance measurement unit. Capacitance voltage (CV) measurements were performed at frequency of 1 kHz whereas the leakage current was measured with the delay of 20 s in order to out-rule all dielectric relaxation processes. The total thickness of top electrode plus hard mask was maintained at less than 20 nm for IPE measurements. CBO for electrons and the oxide band gap were measured in the spectral range 2-6.5 eV [6]. Moreover, thickness and the surface roughness of each film of the examined structures were determined by x-ray reflectometry (XRR).

IPE represents a process where electrons from the occupied states near the Fermi level (E_F) of the metal are optically excited to surmount the interface barrier and to be injected into the oxide conduction band (E_C). By analyzing the spectral dependence of the IPE quantum yield (Y) (the photocurrent normalized to the incident photon flux), the electron barrier height (Φ_e) can be found by Fowler et al.[7].

III. RESULTS AND DISCUSSION

In a first set of experiments, STO based MIM capacitors were deposited on SrRuO₃ (SRO) or Pt electrodes by physical vapor deposition. The according leakage current versus CET plots are shown in Figure 1. For a Pt electrode a minimum CET
value of ~0.45 nm can be reached at DRAM leakage specifications of $1 \times 10^{-7}$ A/cm². The values are similar to recent Ru/STO/Ru ALD based results [8]. By replacing the Pt electrode with SrRuO₃ the CET value can be reduced by more than a factor of 2 to the so far lowest reported value of 0.2 nm. This value would be even lower than the one specified for a 16 nm node target in the ITRS roadmap. However, this result opposes the proposal of Stengel et al. [9] who recommended Pt electrode due to its shorter electronics screening length. The main reason for the CET improvement in this capacitor stack is the low misfit of the lattice constants of SRO and STO leading to a minimum dead layer effect as reported by Schmelzer et al [4]. In contrast to the SRO/STO system, the mismatch and roughness of the Pt/STO surface and interface were higher [10] which is increasing the passive layer effect. Even though this deposition study minimized the issues of the dead layer effect which is the major drawback of the application of this layer in the DRAM capacitor deposition, overall processing issues still remain. Unfortunately, due to a missing 3D-capable SRO ALD process this material stack cannot be transferred in a high aspect ratio DRAM capacitor configuration. Furthermore, the physical thickness of the STO film of ~10 nm is by a factor of 2 too high for an introduction into an 18 nm DRAM node. Accordingly, two new approaches to improve the current ZAZ dielectric are discussed.

![Graph](image.png)

**FIG. 1.** Leakage current density vs. CET: Comparison of PVD deposited STO based MIM capacitors with SRO vs. Pt electrode.

In a second set of experiments, as already described by Knebel at al.[3], in complete in-situ PVD study SrO was evaluated as a new interlayer material to replace the currently used Al₂O₃. Again, the complete capacitor stack was deposited by PVD.
SrO was selected due to the higher dielectric constant of 16 (compared to 9 for Al₂O₃) and an expected band gap ~5.4 eV similar to ZrO₂[11]. Later, lower values of ~4.4 eV were reported [12]. Typically, a ~1 nm Al₂O₃ interlayer reduced the overall dielectric constant of the ZAZ stack from ~40 for pure ZrO₂ to 35. This value can be enhanced by a SrO introduction and a CET improvement of ~10 % is visible compared to the ZAZ stack (Fig. 2a). This higher k-value of the ZSrZ layer reduces the field over the stack which is resulting in a lower field dependent transport mechanism. In addition, an enhanced crystallinity of these thin layers was confirmed by TEM with respect to the ZAZ stacks [3]. Besides, introduction of the SrO improves the reliability behavior which is of significant importance for the production introduction [3].

After the basic material studies in PVD based capacitor stacks, further ZrO₂ based capacitor process improvements were performed to optimize the ZAZ dielectric and the CET value at target leakage current. Primarily, an ALD in-situ processing of the electrode and dielectric stack enhanced the capacitor properties due to less interfacial contamination.

The additional enhancement of the current state of the art stack is an introduction of a noble metal electrode. A replacement of the top electrode was chosen for characterization of the influence of the barrier height engineering. The CBO of a Pt noble metal electrode on atomic layer deposited ZAZ was evaluated and compared to a TiN electrode. Leakage current vs. CET graphs of TiN/ZAZ stacks with TiN and Pt top electrode are shown in Figure 2b. It is important to emphasize that during the deposition of the ZrO₂ dielectric on the TiN bottom electrode a TiOₓNᵧ interface is formed, which pulls oxygen out of the ZrO₂ and nitrogen diffuses into the dielectric. This determines the conduction characteristics and increases the trap density in
ZrO$_2$. Moreover, an additional growth of the bottom interface layer was reported during the top electrode deposition [5, 13]. Accordingly, for both discussed top electrodes (TiN and Pt) an asymmetric stack is formed resulting in a different charge injection for both polarities and different leakage current density levels. In contrast to TiN, the reaction of a Pt top electrode with the dielectric is minimal and therefore maintains almost unchanged concentration of the oxygen vacancies. This results also in a lower leakage current for positive polarities as shown in Figure 2b. CBO offset engineering has significant impact on the transport through the dielectric as reported by Pešić et al. [5]. The slight decrease in CET with Pt electrode compared to TiN observed in Figure 2b originates from the formation of the interfacial layer between the TiN top electrode and the ZrO$_2$ film as described above. The increase of the thickness influences the reduction of the capacitance and corresponding CET.

IPE and photoconductivity (PC) measurement were used to estimate and compare the CBO and the band gap between the two electrodes as reported before [5]. IPE represents a process where electrons from the occupied states near the Fermi level ($E_F$) of the metal are optically excited to surmount the interface barrier and to be injected into the oxide conduction band ($E_C$). Irrespective of the top electrode the band gap of dielectric layer is 5.7 eV, which is close to the previously reported value for ALD ZrO$_2$ of 5.5 eV [6]. The CBO of the TiN/ZAZ interface is 2.5 eV, which correlates well with an electron affinity of ZrO$_2$ (2.2-2.5 eV [6]) and TiN effective work function (EWF) measurement results of 4.9 eV [14]. The CBO of the Pt/ZAZ interface is determined as 3.1 eV, which is 0.6 eV higher than the one of TiN. In order to confirm the workfunction value, measurements on the terraced oxide structures are performed. Structures as described in Wen et al. [15] resulted in a constant fixed charge value at the interface between the Si substrate and the dielectric. The influence of high-k bulk charges is limited to a thickness of ZrO$_2$ based dielectric. The EWFs for terraced oxide stacks is extracted using the method described elsewhere [5] which is a simplified form of the general model given by Wen et al. [15]. Extracted workfunction values of 5.6 and 4.9 eV for Pt and TiN TE (see Fig. 3) are well matched with the IPE measurements.
FIG. 3. Suggested band model showing charge transport mechanisms and hopping probability. An increased CBO decreases the probability of hopping to the first state which results in a decrease of the leakage current resulting in a decreased injection probability.

Furthermore, it is important to define the limits of the intrinsic leakage and to understand the correlation of all the determining parameters. Based on Monte Carlo simulations Jegert et al. suggested that the leakage current of the TiN/ZAZ/TiN stack depends on the CBO [16]. Modeling of the MIM structure was performed by applying a compact model approach described by Pešić et al [5] where the leakage transport mechanism was examined and simulated in detail for the different electrodes. In that study, it was shown that a capacitor with Pt top electrode showed a similar transport characteristic to TiN but leakage current values shifted to higher fields resulting in a leakage reduction by about two orders of magnitude. This shift is related to the decrease in trap concentration and decrease of the probability for tunneling due to the low reactivity of the noble metal Pt electrode and the increased workfunction value of the material, respectively. In addition, the asymmetric workfunction stack results in a field change and a built-in field. This also influences the electrons injected from the bottom electrode, causing a reduction of the leakage on this side as well.

In order to observe the scaling influence on the capacitor characteristics, ALD based capacitors with three different ZAZ thicknesses (5, 5.5 and 6 nm) were prepared as described above. Comparing the shape of the overall IV characteristic in addition to the separated leakage current components (trap assisted tunneling (TAT) [17] and Poole-Frenkel (PF)) [18], leads to conclusion that two main leakage mechanisms define the curve (see Fig.4). In case of an injection from the top side, devices with a Pt top electrode exhibited trap assisted tunneling occurring for low fields followed by a Poole-Frenkel mechanism for higher fields. All devices showed a similar behavior with a field shift towards lower fields with decreasing film thickness. In addition, it can be seen that the top electrode impacted the behavior of the leakage current traces of the
bottom electrode (positive side), as well. As discussed before, the reaction of the Pt top electrode with the dielectric is minimal and could be neglected. Therefore, the concentration of the oxygen vacancies stayed constant whereas the workfunction value is increased. This results in lower leakage current for both polarities. Furthermore, the most important result is that devices with Pt top electrode fulfill leakage current criterion, even for the thinnest (5 nm) ZAZ layers.

![Graph showing simulated influence of the scaling of the dielectric thickness. An electrode limited transport was observed.](image)

**FIG. 4.** Simulated influence of the scaling of the dielectric thickness. An electrode limited transport was observed.

In order to estimate the influence of the dielectric scaling, a simulation of the 5 nm thick ZAZ stack was performed and compared with a simulation of 6 nm thick dielectric (see Fig. 4). The modeling approach described by Pešić et al [5] was extended and applied on the TiN/ZrO$_2$/Al$_2$O$_3$/ZrO$_2$/Pt stacks with different thicknesses. Due to the same annealing condition for both thicknesses, the resulting level of crystallization differs (see Fig.5). Namely, thinner films are more difficult to crystalize due to the increased crystallization temperature. Therefore, due to the same annealing temperature and time thinner dielectric shows a lower crystallinity and a lower k value [19]. As a result, thinner high-k material possesses a lower amount of defects that behave as electron traps and contribute to the conduction. These two effects oppose each other. Lower k-value increases the field over the stack enhancing the field driven leakage current mechanisms, whereas the lower defect concentration decreases the magnitude of the leakage current. Therefore, as a consequence, on the top side (Pt TE), electrode limited transport was observed (Figure 5). Moreover, due to the different ratio of interlayer to overall ZAZ stack thickness, a slightly lower optical dielectric constant was assumed. Using the extracted parameters a good model was obtained that corresponded well with the electrical measurement (see Fig. 4).
FIG. 5. Dielectric constant scaling with the decrease of the dielectric thickness.

TABLE I: Summary results of scaled ZrO$_2$ and STO based capacitor results in comparison to 4 nm ZrO$_2$ MIM capacitor model with Pt electrode. CET value at target leakage current density of $10^{-7}$ A/cm$^2$ characterized at 1 V.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ITRS</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>18 nm</td>
<td>STO</td>
</tr>
<tr>
<td>k-value</td>
<td>60</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SRO</td>
</tr>
<tr>
<td>CET</td>
<td>0.4</td>
<td>0.45</td>
</tr>
<tr>
<td>Thickness</td>
<td>10 nm</td>
<td>5 nm</td>
</tr>
</tbody>
</table>

Additionally, in Fig. 4 a simulated estimation of the further scaling of the ZAZ dielectric down to 4 nm is shown. Simulated results fulfill the leakage current criteria of $1 \times 10^{-7}$ A/cm$^2$ for both top and bottom side injection. Parameters used for the simulation of the leakage current are given in the Table I. Besides the extrapolation of the measured capacitance, a simulation of the scaled capacitance was performed. These two values were averaged and used for estimation of the CET value of the future scaled DRAM nodes. Therefore, it can be seen that application of the noble metal electrodes enables further scaling of the dielectric and DRAM nodes down to the dielectric thicknesses of 4 nm.
Using the extracted band diagram parameters, a CET of 0.53 nm at target leakage current was extrapolated from the model (Fig. 6). An additional replacement of the interlayer material with SrO would lead to an overall CET value of 0.47 nm (Fig. 6), resulting in CET values almost comparable to those reported for STO with RuO$_2$/TiN (0.43 nm) [20] or two Ru electrodes [21] and Al doped TiO$_2$ (ATO) dielectrics with RuO$_2$/Pt electrodes (0.46 nm) [22,23,24] but a lower physical thickness could be reached. Besides the decrease of the CET value, introduction of the SrO within the ZrO$_2$ based reduces the leakage current significantly. The main reason for such behavior is the higher dielectric constant of the stack, which reduces the field drop over the stack and therefore decreases the field driven transport mechanism.

IV. CONCLUSION

It can be concluded that this study paved the way for future DRAM nodes. By replacing the Al$_2$O$_3$ interlayer with SrO in a production type ZrO$_2$ dielectric the CET value was reduced by 10 %. Additionally, the introduction of Pt instead of the current TiN top electrode increased the barrier height for electron trapping to a defect state resulting in a leakage current reduction and decreased the oxygen vacancy concentration. Both improvements lead to a CET value of 0.47 nm. It was shown that besides slight dielectric engineering, the increase of the CBO by introduction of an inert metal electrode represents one of the most effective ways to scale down the ZrO$_2$ dielectric for future DRAM capacitors (Fig. 4, Table I).
REFERENCES


24 Jeon et al., ACS Appl Mater. Interfaces 6, 21632 (2014).
Current density $[\text{A/cm}^2]$ @ 1 V

$\varepsilon_r_{\text{STO}} = 200$
$t_{\text{STO}} = 10 \text{ nm}$

DRAM target
Current density [A/cm²] @ 1 V
Current density [A/cm²] @ -1 V

ZSrZ
ZAZ

~ 10 %
$\text{CBO} = 2.5 \text{ eV}$

$E_g = 5.7 \text{ eV}$

$\text{WF} = 4.9 \text{ eV}$

$WF = 5.6 \text{ eV}$

$WF = 4.9 \text{ eV}$

$\text{Pt}$

$\text{TiN}$

$\chi = 2.2-2.5 \text{ eV}$

Injection probability $P_2$

Injection probability $P_1$
Current density $[\text{A/cm}^2]$

Electric field $[\text{MV/cm}]$

- Measured Pt 5 nm
- Measured Pt 6 nm
- TAT
- PF
- Simulated Pt 6 nm
- Simulated Pt 5 nm
- Estimated Pt 4 nm ZAZ

Bottom Electrode
Injection

Top Electrode injection

Bottom Electrode Injection
Current density [A/cm²] @ I1I V