Flexible AMOLED Display and Gate-driver with Self-aligned IGZO TFT on Plastic Foil

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ABSTRACT

We present a QQVGA (160x120 with 3 sub-pixel) top-emitting AMOLED display with 85ppi resolution using a self-aligned (SA) IGZO TFT backplane on polyimide-foil. The backplane process flow is based on a 5 layer photolithography process. The aperture ratio of the top-emitting OLEDs is approx. 25%. For operation at 6 V supply voltage ($V_{DD}$), the brightness of the display exceeds 150cd/m\textsuperscript{2}. On the same substrate a 160-stage gate-driver was measured at FHD rate.

Keywords: flexible displays; AMOLED; metal-oxide semiconductors; self-aligned TFT

1. INTRODUCTION

The development of AMOLED displays has made rapid progress in the last few years. There are two application fields in which AMOLED displays compete: On the one side small mobile displays where the key differentiator are resolution, daylight readability and power consumption. On the other side medium and large sized displays where only medium resolution is required but cost is the dominating issue. There are several domains where cost needs to be addressed, OLED deposition where we can see a strong push for printed OLEDs for large size displays [1], cost reduction in the backplane by switching to metal-oxide TFT and reducing the number of mask steps [2] and finally integrating the line driver into the backplane process [3]. More value can be added by moving to flexible displays, allowing additional form factor, lighter weight and mechanical robustness.

In this work we integrate SA IGZO TFT on foil and realize an AMOLED backplane with only 5 mask steps. A 160-stage gate-driver is implemented as well on the same substrate.

2. Backplane Fabrication

Compared to the commonly used etch-stop layer (ESL) TFT architecture, we can reduce the number of mask steps from 5 to 4 by switching either to a back-channel etch (BCE) or self-aligned (SA) architecture [4]. The use of a SA architecture allows additionally a strong reduction in parasitic overlap capacitance and therefore RC delay. This is beneficial for larger displays like 4k2k with higher frame rate.

The cross-section of the TFT can be seen in Figure 1. On a temporary glass carrier with a 20um thick polyimide film, a humidity barrier is deposited. Afterwards IGZO (metal ratio = 1:1:1) is sputtered by DC-PVD followed by a wet-etch step to define the active semiconductor area. In a further step we deposit 200nm PECVD SiO\textsubscript{2} as a gate dielectric at a deposition temperature of 250°C. The optimized deposition recipe results in a gate dielectric with a dielectric constant of 4.5, a median breakdown field of 7.5MV/cm and a leakage of 8nA/cm\textsuperscript{2} @ 2MV/cm. Afterwards we deposit 100nm Mo as gate-metal. The gate/dielectric stack is patterned within the same step by dry-etching. Subsequently we deposit 200nm CVD SiN. The CVD SiN fulfills the double purpose of intermetal dielectric and doping the IGZO in the areas not covered by the gate/dielectric stack with hydrogen. The CVD SiN has a dielectric constant of 7.3 , a median breakdown field of 7.5MV/cm and a leakage of 30nA/cm\textsuperscript{2} @ 2MV/cm.

The contact holes for the Source-Drain (SD) contacts are opened up by dry etching and 100nm Mo is deposited and patterned to define the SD-contacts. The last step in the TFT process is a final anneal. All process steps in the backplane process stay below a thermal budget of 300°C.

The resulting TFT characteristic can be seen in Figure 2. For a channel length of 5µm, we achieve a mobility of ~12cm\textsuperscript{2}/Vs. An image of the realized TFT is depicted in Figure 3. All the design rules are compatible with an exposure by using a large GenX scanner.
One of the challenges in a SA TFT, is the required sheet conductivity of the IGZO spacing (SP) between gate and drain contact and between gate and source contact. A value of \(~1k\Omega/sq\) would be the target in our TFT layout to avoid an increased contact resistance. In our case, we rely on the doping of the IGZO by hydrogen. The hydrogen out-diffusion from the SiN recipe needs to be balanced with the time and temperature of the further annealing steps. In Figure 4, we measured the resistivity of the doped IGZO by using separate resistor structures with different channel length. The extracted \(R_{\text{sheet}}\) is 1.5k\(\Omega/sq\).

To verify that the sheet conductivity of the gate-source contact spacing does not limit our TFT performance, we measured TFT with the same W/L but with varying distance of the spacing. In Figure 5, no visible impact of the scaling of SP on the transfer curves can be seen.

In Figure 6, we plotted the transfer curves with varying channel length while the W and SP remained the same. The extracted mobility did not decrease with decreasing channel length, meaning that contact resistance is not a significant issue.

In the next step we summarized the bias stability of our TFT. The results can be seen in Figure 7. for 2000s constant gate-bias at \(+/-20V\), the Von shift remained below 0.5V. This is comparable to previous published results for SA TFT [5].

To verify the speed of our SA TFT, we designed 19-and 41-stage ring-oscillator using diode load-logic in our mask. This allows to measure the oscillation frequency and therefore to extract the stage-delay of inverter gates. This information is required for designing more complex circuits like gate-driver. The stage-delay which we achieved is plotted in Figure 8 with respect to the supply voltage VDD. At VDD=20V, we achieve a stage-delay of \(~19.6ns\). We have plotted other literature data, representing the fastest published ring oscillator using IGZO in the same graph. Here the advantage of the SA TFT with reduced overlap capacitance is obvious. Compared to regular bottom-gate TFT, we gain factor 5-10 in stage delay.
Next, a 160-stage gate-driver has been designed and measured. It comprises only 10 TFT per stage [3], employing in total 1600 TFT. This allows us to achieve a very dense layout, requiring only 125µm width per stage. This would be sufficient for a display resolution up to 200ppi. In Figure 9, the output signal of the stages 2, 3 and 160 is plotted. Added to this graph are the reset signal and the clock signals. The gate-driver starts to work from a $V_{DD}=7V$ and a clock voltage of $V_{CLK}=10V$. The frequency applied corresponds to a frame rate required for FHD. We measured the signals in a regular probe station and effects of the capacitive load of the probes and cables on our signals are already notables. The power consumption of the 160-stage line driver driven with the conditions outlined in Figure 9 is 0.32mW.

A microscopic image of the gate-driver can be seen in Figure 10a. A QQVGA (160x120x3 subpixel) AMOLED display with 85ppi (300µmx300µm) was realized on the same substrate. For high resolution mobile displays, the preferred architecture is a top-emitting display including a third metallization layer as the anode [6]. This allows a very high aperture because the emitting area is on top of the pixel engine. However this approach requires at least 3 additional mask steps. Here we implement a architecture whereby the Source-Drain metallization is used as the anode. This limits the aperture to 25% at 85ppi but requires only one additional mask step to define the edge cover (ECL) layer. An image of the resulting backplane can be seen in Figure 10b and a cross-section in Figure 11.

A conventional 2T1C pixel scheme has been implemented, employing a select TFT of $W/L=15/5µm/µm$ and drive TFT of $W/L$ of $15µm/20µm$. The longer channel length improves the output resistance to $>5M\Omega$ at the operation point (Figure 12).
3. Conclusion
We have demonstrated for the first time self-aligned IGZO-TFT AMOLED and gate-driver on polyimide-foil. The implemented backplane process flow uses only 5 lithographic mask steps resulting in SA TFT with a mobility of 12cm²/Vs for a channel length of L=5µm and a record stage delay <20ns. With this process we have realized a 85ppi QQVGA top-emitting AMOLED display and shown 160-stage gate-driver driven at FHD frame rate.

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4. References
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