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In situ observation of electromigration-induced void migration in dual-damascene Cu interconnect structures
**In-situ** scanning electron microscope observation of electromigration-induced void growth in 30 nm 1/2 pitch Cu interconnect structures

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**In-situ** electromigration tests have been performed inside a scanning electron microscope on 30 nm wide single damascene interconnects without vias, where a good resolution was obtained and drift velocities during void growth could be measured at 300°C. These tests showed direct evidence that the cathode end of the line, where a polycrystalline grain cluster encounters a bigger grain, can act as a flux divergent point of Cu diffusion. Moreover, it was found that a thicker barrier suppresses barrier/interface diffusivity of Cu atoms, thereby slowing down electromigration-induced void growth. It was also demonstrated that Cobalt based metal caps are beneficial to electromigration for advanced interconnects where thinner barriers are required. © 2014 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4866330]

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I. INTRODUCTION

Electromigration (EM) describes the mass transport of metal ions in a conductor due to an electron wind caused by an electrical current. EM is one of the main metal failure mechanisms of back-end-of-line (BEOL) Cu interconnects, particularly with the continuous scaling. The effective Cu diffusivity in a Cu line is very sensitive to and strongly dependent on its microstructure and on the fabrication methods. Cobalt based metal caps have been widely studied for EM enhancement compared to dielectric caps such as SiCN. However, in advanced technology nodes, the Cu/dielectric cap interface would no longer be the dominant Cu diffusion path compared to grain boundaries because of the change in Cu grain structure.1 This implies that for advanced technology nodes, metal caps could potentially be less beneficial to EM reliability. On the other hand, extrinsic factors caused by a wide variability of line width roughness and a poor coverage of Cu seed and barrier metal can deteriorate EM performance because the Cu/metal barrier interface can potentially become more diffusible. Therefore, understanding of Cu diffusivity in scaled dimensions is extremely important for potential reliability improvement.

For the past 40 years, direct observation of EM damage in micron scale or wider metal interconnects has been the key to understand fundamental mechanisms of EM. Scanning Electron Microscopy (SEM) is one of the most commonly used techniques for in-situ studies, since it yields a high lateral resolution without additional specimen preparation.2–5 Besides, also in-situ transmission electron microscopy (TEM) studies6 and in-situ transmission X-ray microscopy (TXM) studies7–9 are reported, among others. However, it becomes more difficult to achieve real-time observation of EM failure mechanisms as the interconnect dimensions scale down to sub-100 nm range. This is because at these dimensions, the change in void size and shape becomes comparable to the lateral resolution of the available in-situ techniques. Additionally, achieving a high temperature stability of the specimen during in-situ EM experiments becomes extremely important, especially when images are recorded at high magnifications. Even the smallest variation in temperature can induce thermal expansion of the sample holder and consequently result in a mechanical sample drift, which in turn may cause image distortions and misinterpretation of the void shape and size. So far, only a few papers have reported EM void growth behavior in sub-100 nm polycrystalline grained Cu lines using an in-situ SEM technique10 or electrical measurements.11 In this paper, we demonstrate, for the first time, the direct observation of EM induced void growth in 30 nm wide Cu single damascene interconnects using an in-situ SEM method.

II. EXPERIMENTAL DETAILS

A schematic top-view of the EM test structure for a single level Cu line used in this work is illustrated in Figure 1(a).16 This so-called local sense structure allows a sensitive resistance measurement at the cathode end of the line using a positive voltage terminal, $V_1^+$, that was placed 10 μm away from the electron injector. Additionally, it can be used to measure the resistance over the full length of the line using a second voltage terminal, $V_2^-$. The 30 nm wide and 100 nm deep Cu lines were fabricated into a chemical vapor deposition (CVD) SiOCH low-k dielectric ($k = 3.2$) with a litho-etch-litho-etch double patterning approach. The metallization was performed by damascene processes of physical vapor deposition (PVD)-Ta/Ta, PVD-Cu seed, Cu electrochemical plating, and chemical mechanical polishing (CMP).17 The Cu lines were capped with 30 nm thick SiCN and subsequently SiO2 and SiN were deposited as passivation layers. Since advanced technology nodes require thinner metal barriers, poor coverage of the barrier metal can result in a more diffusible Cu/metal barrier interface. To

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investigate the contribution of the Cu/barrier interface to Cu diffusivity, 30 nm wide copper interconnects with, respectively, 1.5 nm and 3 nm thick PVD-TaN/Ta barriers and a 30 nm thick SiCN dielectric cap were compared (Figure 1(b)). To investigate the effect of the capping materials, the EM performance was compared for a 1.5 nm PVD-TaN/Ta barrier with and without a Cobalt based metal cap. The impact on EM-induced void growth was studied using the following methodology (Figure 2). First, package level EM tests were performed on a 30 nm wide Cu interconnect until a full void across the line height and width was formed. The applied current density and temperature for the package level EM tests were 8 MA/cm² at 250 °C. Next, the package level EM test was stopped and the passivation layers were removed. After this, in-situ EM tests were performed to further study EM-induced void growth in the Cu line.

In-situ EM tests were achieved by combining a SEM (FEI XL30-FEG SEM) with a proportional-integral-derivative (PID) controlled heating stage with a temperature stability of 0.1 °C to minimize the mechanical sample drift due to temperature fluctuations at the sample position. In addition, a probing system with nanometer precision was integrated. All was controlled by a Keithley 4200 parameter analyzer. An overview of the experimental setup is shown in Figure 3.

The resistance measurements can be performed using standard or local sense probe pads (Figure 1(a)) and is remotely controlled through a GPIB interface. The applied current density for all in-situ EM tests was 2 MA/cm² and the test temperature was 300 °C. During the in-situ EM tests, secondary electron (SE) images at 5 keV were acquired at well-defined moments in time, while in between, the electron beam was blanked to avoid any interference with the EM process. The resulting video sequences provide a good visualization of the growth and motion of voids at the stressed interconnects.
III. RESULTS AND DISCUSSION

The SE image sequences that are acquired during the in-situ EM experiments contain information about the void sizes (two-dimensional projections) as well as their lateral position along the interconnect lines. However, due to the three-dimensional geometry of the EM interconnect structures, the interpretation of these images can be quite challenging. Therefore, some considerations regarding the interaction volume of the incident electrons in the sample are necessary to estimate the minimum detectable void size as well as the maximum information depth of detection. Because the interaction volume of the incident electron beam decreases with decreasing acceleration voltage and since the EM structure contains 100 nm deep Cu interconnects capped with 30 nm SiCN, SE images are typically acquired at 5 keV to minimize the interaction volume. The incident electron beam causes electrons to be emitted from the sample due to elastic and inelastic scattering events within the sample’s surface and near-surface material. Secondary electrons result from inelastic scatterings of electrons with valence electrons of the target atoms, but only those electrons very close to the surface can leave the sample again and be detected due to their limited energy. Typically, this ranges from several nm for metals and tens of nanometers for insulators. Despite their small escape depth, secondary electrons can be generated from different regions underneath the sample surface. The largest contribution to the SE signal is coming from secondary electrons that are generated by the incoming electron beam as it enters the surface. However, a smaller fraction of the secondary electrons are generated by backscattered electrons that have returned to the surface after several inelastic scattering events. This typically occurs at depths up to half of the penetration depth. From the expression of Kanaya and Okayama, the penetration range of the interaction volume can be estimated by

\[
R_e = \left(0.0276A/\rho Z^{0.889}\right)E_b^{1.67},
\]

where \(R_e\) is the penetration range, \(A\) is the atomic weight, \(\rho\) is the density, \(Z\) is the atomic number, and \(E_b\) is the acceleration voltage of the incident electron beam. Applying a 5 keV electron beam on pure Cu, this results in \(R_e \approx 150\) nm, while in the case of a SiCN cap, \(R_e\) is about 3 times larger. From this, we can conclude that the penetration range in 100 nm deep Cu interconnects capped with 30 nm SiCN is mainly restricted by the Cu. Therefore, voids that are present throughout the Cu volume could potentially be visualized by the detected SE signal. However, due to the three-dimensional geometry of the EM structure, it is difficult to assess the theoretical limitations for the minimal detectable void size and depth range, since this depends on the width of the incident electron beam and the size and shape of the interaction volume. Nevertheless, the smallest changes in void size that was experimentally observed during in-situ EM tests was in the order 10 nm, which is at the limit of the SEM equipment that was used. Figure 4(a) shows the initial stages of EM-induced void growth in a 30 nm wide line with a 1.5 nm TaN/Ta barrier with a 30 nm SiCN cap. During the first 15 min (I to IV in Figure 4(a)), the void length along the line (L_void) remains constant despite the stepwise resistance increase. On the other hand, the contrast of the void increases, which suggests void growth towards the line bottom (h_void). Indeed, a larger void size along the line depth results in less available Cu volume that can contribute to the SE signal, therefore increasing the contrast with the surrounding material. Repeated in-situ EM tests on similar structures revealed that this initial stage is not always present. This is because the void nucleation and growth modes during package level EM tests highly depend on the specific grain structure of polycrystalline Cu interconnects. Once the void reaches the line bottom, it starts to grow along the line with the drift velocity of 6 nm/min for a current density of 2 MA/cm² and a test temperature of 300 °C (V to VII in Fig. 4(b)). The drift velocity in a metal line caused by the EM driving force can be expressed by the equation

\[
v_d = \left(D_{eff}/k_B T\right)Z_{eff}^* e\rho j,
\]

where \(D_{eff}\) is the effective diffusivity, \(Z_{eff}^*\) is the effective charge number, \(k_B\) is the Boltzmann constant, \(T\) is the absolute test temperature, \(\rho\) is the resistivity, and \(j\) is the current density. There are several possible diffusion paths in an interconnect line, so the total material transport is determined by the sum of the mass transport taking place along each of these paths. In the case of 30 nm polycrystalline Cu lines with a thin TaN/Ta barrier and a SiCN dielectric cap, \(D_{eff}\) can be expressed as
\[ D_{\text{eff}} = n_{\text{GB}} D_{\text{GB}} + n_{\text{Cap}} D_{\text{Cap}} + n_{\text{Barrier}} D_{\text{Barrier}}, \]  \hfill (3)

where the subscripts GB, Cap, and Barrier refer to grain boundary, Cu-SiCN cap, and Cu-TaN/Ta barrier interface, respectively. \( D_{\text{GB}}, D_{\text{Cap}}, \) and \( D_{\text{Barrier}} \) are the diffusion coefficients for diffusion through grain boundaries, Cu-SiCN interface, and Cu-TaN/Ta interface, while \( n_{\text{GB}}, n_{\text{Cap}}, \) and \( n_{\text{Barrier}} \) denote the corresponding fractions of atoms diffusing along these paths. As expected, the growth direction of the full void is away from the cathode end of the line. This behavior can be explained by the presence of a bigger grain at the connection to the electron injector, as was evidenced by a TEM cross section of the injector (Figure 5). The TEM picture shows that a big grain at the connection to the electron injector acts as a location of flux divergence for the void growth, which stops the void movement towards the injector. Figure 6 shows EM-induced void growth in a 30 nm wide Cu interconnect in the case of a 3 nm thick TaN/Ta barrier. In this particular case, since the void was already fully grown across the line height and width during package level EM, the void immediately started to grow along the line, again away from the injector. In contrast to the thin TaN/Ta barrier case, the void growth happens in a consecutive two-step way. First, the void grows over the cap-interface, which is evidenced by the lower
contrast of the additionally depleted Cu volume compared to the initial void contrast (i and ii in Figure 6). Next, the void continues to grow towards the line bottom, which corresponds to a stepwise increase of the resistance (ii and iii in Figure 6(b)). After this, void growth happens again over the cap-interface, and so on (iv in Figure 6(b)). The calculated drift velocity at 300°C with 2MA/cm² current density was about 10 times smaller compared to the 1.5 nm TaN/Ta case. This difference in drift velocity may be related to the integrity of the TaN/Ta barrier. Insufficient coverage of the barrier material can cause oxidation of the tantalum during the various processing and reliability steps and could potentially lead to EM void nucleation sites. Recently, this was confirmed by Richard et al., who used electron tomography to characterize voids in Cu lines after EM.19 Medium-size voids were found at the sidewalls of 30 nm wide Cu lines with a 1.5 nm TaN/Ta barrier after EM test. Moreover, the TaN/Ta barrier was clearly observed next to the voids, whereas no barrier was present near the voids, suggesting that the formation of voids is related to the integrity of the TaN/Ta barrier. Figure 7 shows the proposed grain depletion void model in the case of a 1.5 nm or 3 nm thick TaN/Ta metal barrier and a 30 nm thick SiCN dielectric cap. Both the reduced drift velocity and the observation of void growth over the cap-interface demonstrate that a thicker barrier suppresses the barrier/interface diffusion of Cu atoms, which in turn improves the effective diffusivity and slows down the EM-induced void growth. Figure 8 shows EM-induced void growth in a 30 nm wide Cu interconnect in the case of a 1.5 nm TaN/Ta barrier and a CoWP metal cap. Only limited void growth was observed at 300°C with 2 MA/cm² current density. The calculated drift velocity was therefore about 30 times smaller compared to the case of 1.5 nm TaN/Ta combined with a SiCN dielectric cap (Figure 9). This can be explained by the fact that Co diffuses into the interface between the barrier metal and Cu and suppresses Cu diffusivity at that interface, as was demonstrated by Kirimura et al.20 Since both Cu diffusivities at the cap and barrier interfaces are suppressed by the presence of Co, a CoWP cap is beneficial to EM for advanced interconnects where thinner barrier metals are required. Figure 9 compares the void growth velocity measured by the in-situ SEM technique at 300°C with 2 MA/cm² current density in case of 30 nm wide copper interconnects with different TaN/Ta barrier thicknesses and different cap materials. It clearly shows that a thicker TaN/Ta barrier suppresses the barrier/interface diffusivity of Cu atoms, while Co suppresses Cu diffusivities at the cap and barrier interfaces. In both cases, the EM-induced void growth is slowed down.

IV. CONCLUDING REMARKS

A direct observation of void growth in 30 nm wide single damascene interconnects was demonstrated using an in-situ EM test method, where a good resolution was obtained at 300°C. These in-situ EM tests showed direct evidence that a grain boundary between a polycrystalline grain cluster and a bigger grain can be a flux divergent point of Cu diffusion. Moreover, it was evidenced that a thicker barrier suppresses barrier/interface diffusivity of Cu atoms, thereby slowing down EM-induced void growth. Also, it was demonstrated that Cobalt based metal caps are beneficial to EM for advanced interconnects.

16O. Richard, J. Geypen, Y. K. Siew, T. Kirimura, K. Croes, P. Van Marcke, and H. Bender, in European Microscopy Congress (EMC) (2012), session PS2.4: 3D/4D Imaging.