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<th><strong>Citation</strong></th>
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A 0.9 V 29.9dBm 22.3% PAE E-Band Power Amplifier with Broadband Parallel-Series Power Combiner in 40nm CMOS

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The 71-to-76GHz and 81-to-86GHz bands (known as E-Band) exhibit low atmospheric attenuation and are allocated to FCC and CEPT for long-haul transmission. They enable multi-Gb/s data links services such as fiber extension/replacement and cellular backhaul. It is beneficial to have a design operating in both 50GHz bands for high data throughput (due to full usage of the 50GHz band) and low interference (due to the 1GHz spacing between the two bands). This requires a PA that delivers uniform gain and output power from 71 to 86GHz. An output power of more than 29dBm is also desired for sufficient link margin to accommodate rain attenuation. These requirements are not satisfied by prior reported 70/80GHz PAs in silicon-based technology [1-4].

This paper reports a fully integrated 40nm CMOS PA that utilizes a broadband parallel-series power combiner to achieve an output power (PO2) of 29.9dBm with more than 150% small-signal 3dB bandwidth (BWps) and 22% PAE at 0.9V supply. The in-band variation of PO2 is only ±2.5dB. This silicon-based PA covers both 71-to-76GHz and 81-to-86GHz bands with uniform gain, output power and PAE.

Transformer-based series combiners are popular in mm-Wave PA design due to their high power transfer efficiency and compact layout. However, two crucial issues limit the efficiency and effectiveness of such structures to combine more than four signal paths (i.e. two differential signal paths) to achieve high output power at mm-Wave. 1) The parasitic interconnecting capacitance between the primary and secondary coils will distort the amplitude and phase of the signals to be combined and reduce the combining efficiency. 2) The input impedance in each path of the series combiner decreases in proportion to the number of the combining paths. Considering that the performance of mm-Wave transistors is constrained by the loss of the peripheral interconnects, the typical value of the transistor width above 66GHz is limited to 150 to 150um, which leads to an optimum load impedance (ZLO) of a common-source (CS) differential amplifier in the range of 30 to 50Ω. Therefore, to accomplish beyond 2-way differential combining, either the transistor size needs to be considerably increased for a much lower ZLO (i.e. causing much higher interconnect loss) or an additional matching circuit is required to perform the impedance transformation. The above two issues will limit the output power, combining efficiency and bandwidth of the whole network.

In this design, a combination of parallel and series combiners is used, which efficiently combines four differential amplifiers with low insertion loss and at the same time minimizes the impedance transformation ratio of the whole passive network to maximize the bandwidth. Figure 14.1.1 shows the E-band PA schematic which incorporates two unit PAs with a slow-wave T-line-based parallel combiner and a transformer-based series combiner. The slow-wave T-line in the parallel combiner has a differential-mode characteristic impedance of 70Ω. It transforms the 50Ω load (100Ω seen by each differential line) and adds parasitics to an equivalent resistance of 52Ω seen by the two unit PAs. The series combiner reduces this impedance by a factor of 2 and provides the ZLO (i.e. 29Ω, close to half of 52Ω) for the output stage. With this parallel-series power combining approach, the transistor size of each PA stays optimal for high power gain and efficiency, while four of these PAs are combined efficiently with low impedance transformation rate as required for broadband operation. Figure 14.1.2 plots the power contours of the output stage at 74 and 83GHz and the input impedance of series combiner (i.e. ZLO seen by the output stage) from 70 to 95GHz. It is shown that optimum power matching is achieved in the entire band. The load impedance remains around 29Ω and the load inductance increases at lower frequency which is desired for broadband matching. The insertion loss of the complete parallel-series combiner is less than 1dB from 85 to 95GHz.

The broadband power matching for the drivers will be constrained by the interstage matching network. Therefore, the driver stage is sized sufficiently large to provide enough linear power for the output stage in the 71-to-86GHz band. In this design, each driver drives two output stages and they have the same transistor size (176um/40um). The transistor layout is optimized to minimize the interconnect loss. Compared to the DPA transistor model, the maximum power gain of the neutralized CS amplifier is reduced by only 0.7dB (C0=43Ω). In addition, the parallel T-line-based power divider at the input also lowers the overall input impedance by a factor of 2, which simplifies the input matching design and preserves the bandwidth.

A compact floor plan is crucial to mm-Wave circuits where the placement of all the interconnects has to be considered carefully. These interconnects should not only route the signals between stages but also be employed as part of the matching circuits to minimize the overall loss. Besides, the input matching lines and coupling that cannot be avoided in a compact design has to be characterized accurately. Figure 14.1.3 illustrates the layout of the output series combiner, the power divider and associated interconnects. The distance between the combiner and divider is only 24μm. There are two ways to connect the power divider to the output stages, referred as interconnects A and B in Figure 14.1.3. Both differential interconnects act as part of matching circuits and are optimized to minimize the impedance and associated loss. The major difference of using these two interconnects is the possibility of coupling between the power combiner and power divider. Simulations predict that the complete PA achieves 1dB higher gain with interconnect A and it even outperforms the case when no coupling exists.

The PA prototype is fabricated in a 40nm bulk CMOS process. The chip micrograph is shown in Figure 14.1.7. Due to the compact floor plan, the chip occupies only 0.19mm2 including the input and output RF pads. Thanks to the parallel combing/aligning structures at the PA output/input, the two unit PAs are perfectly symmetrical against the center dashed line. This facilitates the TX integration as the magnetic couplings of the two unit PAs to the preceding stages will be cancelled and the VCO pulling can be alleviated.

Figure 14.1.4 shows the measured small-signal S-parameters. The PA achieves a peak PO2 of 18.1dB at 78.5GHz and small-signal BWps of 15.2GHz (7.03 to 85.6GHz). The S11, S21, and S22 are lower than -8, -10 and -37dB respectively from 71 to 86GHz. The amplifier is unconditionally stable over the entire measured frequency range (0.1 to 110GHz). Consuming 37.5mW from a 0.9V supply, the PA has a measured PO2 of 17.4dBm, PO1-dB of 20.4dBm with 22% PAE at 80GHz. Figure 14.1.5 shows that the PA achieves a measured PO2 of 17.55±2.25dBm, PO1-dB of 20.5±0.35dBm and PAE of 20.8±1% from 71 to 86GHz. The variation of PO1-dB is even smaller than that of PO2 thanks to the design techniques discussed, which maximize the bandwidth of the output combiners and ensure sufficient power delivered by the drivers. The measured EVM in the 70GHz band (I=47GHz) is also shown in Figure 14.1.5. The input data generated by the AWG and external SSB up-converter limit the performance. The PA achieves 29.6dBm 160AM and 50.6dBc 10PSK at 12.5 and 13.6GHz average P0.1-dB respectively with a measured EVM slightly higher than the one directly measured from the setup. For long-term reliability, we operated the PA with 20dBm P0.1-dB at 0.9V for more than 10 hours. No obvious degradations of output power (±0.1dB) and drain current (±1%) were observed.

Figure 14.1.6 summarizes the comparison with the state-of-the-art 70/80GHz PAs in silicon. This work achieves comparable small-signal BWps to a distributed topology [3] that compromises in efficiency and silicon area. Among the PAs in the comparison table, the proposed 0.19mm2 40nm CMOS PA achieves highest and nearly uniform PO2, PO1-dB and PAE at 71-to-86GHz band at 0.9V supply.

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References:
Figure 14.1.1: Schematic of the complete PA and the unit PA.

Figure 14.1.2: Input impedance of the series combiner and the simulated insertion loss of the parallel-series combiner (including output pads).

Figure 14.1.3: Unwanted magnetic coupling between series combiner and power divider (supply and ground lines not shown for simplicity but included in the simulation) and simulated $S_{11}$ of the complete PA with different coupling effects.

Figure 14.1.4: Measured S-parameters vs. frequency and measured power gain, output power, PAE vs. input power at 800GHz.

Figure 14.1.5: Measured $P_{out}$, $P_{sat}$ and PAE vs. frequency, and measured EVM (w/ & w/o BUT) in 70GHz band (f0=240GHz).

Figure 14.1.6: Comparison of PAs in 70/80GHz bands.