Stability Synthesis of Power Hardware-in-the-Loop (PHIL) Simulation

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Abstract--A virtual power system can be interfaced with a physical system to form a power hardware-in-the-loop (PHIL) simulation. In this scheme, the virtual system can be simulated in a fast parallel processor to provide near real-time outputs, which then can be interfaced to a physical hardware that is called the hardware under test (HuT). Stable operation of the entire system, while maintaining acceptable accuracy, is the main challenge of a PHIL simulation. In this paper, after an extended stability analysis for voltage and current type interfaces, some guidelines are provided to have a stable PHIL simulation. The presented analysis have been evaluated by performing several experimental tests using a Real Time Digital Simulator (RTDS™) and a voltage source converter (VSC). The practical test results are consistent with the proposed analysis.

Index Terms--PHIL, RTDS, Real-Time Simulation, Interface Issues, Stability of PHIL.

I. INTRODUCTION

IN POWER hardware-in-the-loop (PHIL) simulation, a real-time parallel processing computer system, that can simulate a large electric network, is interfaced with a physical system through D/A and A/D converters and a power amplifier. This has the advantage that it can provide an opportunity to investigate the operation of a system under test (HuT) repeatedly in real test conditions. Wide variety of tests and experiments on power systems, which are costly, difficult and risky to be practically examined, can be economically and safely implemented through a PHIL simulation. Moreover, this method has the potential to reveal the full extent of system interactions to be expected in the final design stage [1-3].

A PHIL test can be realized using several simulation tools. Among them Real Time Digital Simulator (RTDS) is one of the prominent platforms to perform complex power system simulations in near real-time [4]. It consists of high speed processors and several I/O cards that can be used to interface RTDS to any real world hardware. RTDS has been used by researchers to implement and test their ideas [5-7].

There should be an appropriate power interface between the virtual network and HuT to manage low power signals from the simulation and the medium or high power absorption or production from the HuT. An ideal interface has unity gain and does not impose any time delay or phase distortion to assure the integrity of the PHIL simulation. However, in practice, an ideal interface is not possible and the closed loop will have time delay associated with signal exchange. Therefore, PHIL simulations will always have some errors due to the imperfection of the interface [8, 9].

There are two different stability aspects that need attention for PHIL simulation. One is the numerical stability associated with the splitting a system into two parts. The other is associated with the practical implementation, such as the power converter bandwidth, sensor noise, time delay, and ripple of the power amplifier [2]. In addition to stability, accuracy of the results is another important issue. Stability and accuracy requirements can be achieved using an appropriate interface between the virtual and hardware side of a test [8].

In this paper, stability and accuracy problems of PHIL simulations are analytically addressed and impacts of employing a low-pass filter (LPF) and changing its parameters are investigated. The presented studies have been tested experimentally using an RTDS.

II. EFFECT OF INTERFACE ALGORITHM ON STABILITY

Consider a hypothetical system which is split into two parts and each part is represented by its Thevenin equivalence. Such a network is shown in Fig. 1. To form a PHIL test, the left part is supposed to be simulated in a real-time simulator and is considered as the virtual part, while the network at the right is assumed to be the HuT. Components of each section are denoted by the relevant subscripts. Stability of such PHIL implementation depends on the interface and equivalent impedance of the two sides. This is discussed below.

A. Voltage Type Interface

Using a voltage type ideal transformer model (ITM) [1, 10] interface algorithm, the system in Fig. 1 can be represented as the network shown in Fig. 2. Here a controlled current source replaces the HuT part, while the voltage of the virtual side is imposed on the HuT by a controlled voltage source.

Let us assume that this controlled current source injects the same amount of current as the HuT network draws in the origi-
inal circuit. Then the voltage across this current source, \( V_{\text{Virtual}} \), is expected to be equal to the voltage across the HuT in the original network. So \( V_{\text{Virtual}} \) can be measured and be used as the reference for a controlled voltage source. The voltage source then must follow this reference voltage and generate \( V_{\text{Virtual}} \) at its terminals. Then the HuT current, \( i_{\text{HuT}} \) can be measured to be given as an input to the controlled current source. System in Fig. 2 can be represented by the block diagram of Fig. 3.

\[
T_V = \frac{V_{\text{HuT}}}{V_{\text{Virtual}}} = e^{-s\tau_d}, \quad T_I = \frac{I_{\text{Virtual}}}{I_{\text{HuT}}} = 1
\]

\[
T_{\text{Virtual}} = \frac{Z_{\text{HuT}}}{Z_{\text{Virtual}}} = \frac{1}{R_{\text{HuT}} + sL_{\text{HuT}}}
\]

\[
T_{\text{Virtual}} = \frac{Z_{\text{HuT}}}{Z_{\text{Virtual}}} = \frac{R_{\text{Virtual}} + sL_{\text{Virtual}}}{R_{\text{Virtual}} + sL_{\text{Virtual}}}
\]

The system open loop transfer function is then equal to

\[
T_{\text{OL}} = T_V T_I T_{\text{HuT}} = \frac{Z_{\text{HuT}}}{Z_{\text{Virtual}}} e^{-s\tau_d}
\]

Values of the parameters used for the first PHIL test are tabulated in Table I. It should be noted that these values are only considered to probe the analysis and do not aim to reflect characteristics of any specific device or system. The Bode plot of the system, shown in Fig. 4, implies on a stable system with positive gain margin and infinite phase margin.

To address the stability issue, let us change the Thevenin equivalent impedance of the virtual side network to a new value with the Laplace transform of \( 25 + 0.016s \), while the HuT side remains unchanged. The Bode plot for the system is shown in Fig. 5 with the solid lines. It can be seen that, the system has a negative gain margin (i.e., the gain is above 0 dB in the phase crossover point of \( -180^\circ \)). Although the original system without the time delay has an infinite gain margin, the inclusion of the time delay makes the system unstable.

<table>
<thead>
<tr>
<th>System Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{S_{\text{Virtual}}} )</td>
<td>( 45 \sin(100\pi t) ), V</td>
</tr>
<tr>
<td>( I_{\text{Virtual}} )</td>
<td>12, mH</td>
</tr>
<tr>
<td>( R_{\text{Virtual}} )</td>
<td>18, ( \Omega )</td>
</tr>
<tr>
<td>( V_{S_{\text{HuT}}} )</td>
<td>( 35 \sin(100\pi t - 25^\circ) ), V</td>
</tr>
<tr>
<td>( I_{\text{HuT}} )</td>
<td>14, mH</td>
</tr>
<tr>
<td>( R_{\text{HuT}} )</td>
<td>21, ( \Omega )</td>
</tr>
<tr>
<td>( \tau_d )</td>
<td>20, ( \mu s )</td>
</tr>
</tbody>
</table>

To counter this problem, a negative pole is added in the open loop path. This is achieved by low-pass filtering \( I_{\text{HuT}} \) to obtain \( I_{\text{Virtual}} \) such that

\[
T_I = \frac{\alpha}{\alpha + s}
\]

where \( \alpha \) is the corner frequency of the LPF in rad/s. Therefore, the open loop transfer function of the system will change to

\[
T_{\text{OL}} = \frac{\alpha Z_{\text{Virtual}}}{Z_{\text{HuT}}(\alpha + s)} e^{-s\tau_d}
\]

The Bode plots for the open loop transfer function of (4) for \( \alpha = 5000 \) and \( \alpha = 50000 \) are shown in Fig. 5. It can be seen that the gains are below 0 dB in the phase crossover points indicating a stable system. It is also evident from the results that larger stability margins can be achieved with smaller value of cut-off frequency. Experimental time domain test results will be presented in the Section IV.

B. Current Type Interface

Now let us consider the current type ITM [1, 10]. The system under study can then be represented as in Fig. 6. A controlled current source injects current to HuT based on the calculated current of the virtual side. The voltage of HuT is then measured and fed back to the virtual side using a controlled voltage source. The block diagram of the system is shown in...
Again, we assume that the interface part is ideal with a unity gain and there is only a time delay associated with it. From Fig. 7, we get the following:

\[ T_i = \frac{I_{\text{HuT}}}{I_{\text{Virtual}}} = e^{-\alpha t_d}, \quad T_v = \frac{V_{\text{Virtual}}}{V_{\text{HuT}}} = 1 \]

\[ T_{\text{HuT}} = Z_{\text{HuT}} = R_{\text{HuT}} + sL_{\text{HuT}} \]

\[ T_{\text{Virtual}} = \frac{1}{Z_{\text{Virtual}}} = \frac{1}{R_{\text{Virtual}} + sL_{\text{Virtual}}} \]

The open loop transfer function of the system is

\[ T_{OL} = T_i T_j T_{\text{HuT}} T_{\text{Virtual}} = \frac{Z_{\text{HuT}}}{Z_{\text{Virtual}}} e^{-\alpha t_d} \]

The Bode plot of (8) is also shown in Fig. 9, in which the dashed lines show the system with \( \alpha = 5000 \) and the dotted lines illustrate the system with \( \alpha = 50000 \). It is seen that the LPFs stabilize the system. Analogous to the voltage type interface, it is evident from the figure that stability margins are larger with the smaller cut-off frequencies of LPF.

In general, given that only a time delay is associated with the interface, it can be concluded that without employing LPF, the stability of PHIL implementation depends on the equivalent impedances of the virtual side and HuT. Irrespective of the interface type, the time delay is a determining factor for the stability of a PHIL simulation. With an ideal interface without noise, ripple, or time delay, the PHIL simulation is stable so long as the original system is stable. However, in practical cases all interface devices are non-ideal and therefore, there will be a potential instability for some test conditions. Practical test results using RTDS and a VSC are presented in the Section IV.

III. EFFECT OF DELAYS ON STABILITY

Several factors may affect accuracy and stability of PHIL simulations. Amongst them, time delays caused by different components in the loop have a crucial impact on these issues. As shown in Fig.10, these delays can be categorized as follows:

- \( t_M \): time delay of voltage and current measuring devices
- \( t_{A/D} \): time required for converting analogue signals to digital
- \( t_{RTS} \): time required by the real-time digital simulator
- \( t_{D/A} \): time delay caused by digital to analogue converter
- \( t_{\text{VSC}} \): time delay of the power amplifier and driver.

Therefore, the total time delay of a PHIL open loop transfer function, \( t_d \) will be

\[ t_d = t_M + t_{A/D} + t_{RTS} + t_{D/A} + t_{\text{VSC}} \]

The main portion of \( t_d \) includes the computation time required by the real-time simulator i.e. \( t_{RTS} \). To probe the effect of total time delay, \( t_d \) on stability of a PHIL test let us consider the unstable current type interface case in the Section II where \( Z_{\text{HuT}} = 21 + 0.014s \) and \( Z_{\text{Virtual}} = 18 + 0.012s \). As demonstrated in that section, an LPF with a cut-off frequency of \( \alpha \) can improve the stability of the system. Nevertheless, stable operation of the system directly relates to the loop delay. Fig. 11 illustrates stability margins of the case while \( t_d \) is
changed from 0 to 150 μs for four different LPF cut-off frequencies. The plot demonstrates the lesser is the time delay, the more are the stability margins.

Taking into account that LPFs impose a phase shift between measured data and the filtered signal, it can be concluded that the stability improvement achieved by employing an LPF always sacrifices some fraction of the results accuracy. A lower value of the cut-off frequency improves the stability more than a higher one, but on the other hand it adversely affects the accuracy. It can also be inferred from Fig. 11 that for the systems with higher computing speeds, i.e. less time delays, higher cut-off frequencies can be chosen. This implies a more accurate simulation while stability margins are still in an acceptable level. So, real-time digital simulators with higher processing speeds can provide more stability margins and more accurate results simultaneously.

IV. EXPERIMENTAL RESULTS

In order to experimentally verify the hypotheses of the previous sections, an RTDS and a SEMIKRON modular IGBT stack are utilized. The SEMIKRON VSC serves as the power amplifier between the virtual network in the RTDS and the HuT. The virtual side of the system is simulated in the RTDS using its Graphical User Interface (GUI), RSCAD with a circuit solution time-step of 12 μs. The RTDS Gigabit-Transceiver Digital Output (GTDO) card is used to import the generated switching signals to the VSC driver board. The required HuT voltages and currents are measured and transferred to the Gigabit-Transceiver Analogue Input (GTAI) card of the RTDS.

The aim of the VSC controller in the voltage type and current type interfaces is to follow \( v_{\text{Virtual}} \) and \( i_{\text{Virtual}} \) as accurate as possible, respectively. Therefore, any type of controller that can serve this purpose can be utilized. In this paper, the control scheme is based on state feedback as has been discussed in [11] (not discussed here due to page limit). A triangle waveform of 10 KHz is used to generate PWM switching signals.

A. Voltage Type Interface

For this type of interface, the hardware side of Fig.1 is connected to the VSC through an LC filter of 10 mH and 650 μF. \( v_{\text{Virtual}} \) and \( v_{\text{HuT}} \) are the same as given in Table 1. Fig. 13 shows the PHIL test results for \( Z_{\text{Virtual}} = 18 + 0.012s \) and \( Z_{\text{HuT}} = 21 + 0.014s \). Based on the discussion given in Section II, the system is stable. In order to have a benchmark to evaluate the results of the experimental tests, the original system of Fig. 1 is simulated in RSCAD as well. So, the current and voltage errors shown in the figure are the difference between the voltage and current of the original circuit and the HuT. Since the hardware model cannot be expected to reflect the exact characteristics of the real one, some portion of the error would be due to inaccurate models and is not associated with the PHIL simulation. More detailed discussions about evaluating accuracy of PHIL simulations can be found in [12]. Note that, the data are collected from RTDS (RSCAD, RunTime) and then are plotted using MATLAB for better clarity. As can be understood from the figure, results confirm the stable operation of the system.

B. Current Type Interface

In order to enable the VSC to track the reference current, an LCL filter is utilized, where the filter’s capacitance and high frequency and low frequency side inductances are 50 μF, 10 mH, and 100 mH respectively. According to the analysis of Section II, the current type interface would be stable for \( Z_{\text{Virtual}} = 25 + 0.016s \) and \( Z_{\text{HuT}} = 21 + 0.014s \). It is clear in plots of Fig. 15 that the results of the experimental implementation of
the PHIL test also verify the stable operation of the system. Here, again the error is defined as the difference between the original circuit and HuT quantities.

For this type of interface, changing Z_{virtual} to 18 + 0.012s makes the closed loop system unstable. LPFs with two different cut off frequencies are used for stabilization. It is clear in plots of Fig. 16 that the system does not show any unstable behavior. Analogous to the voltage type interface, error is smaller when a larger cut-off frequency is chosen for the LPF.

For both the stabilized cases shown in Fig. 14 and 16, a redesign of the controller could lead to better tracking for α = 5000. But on the other hand, for α = 50000 the redesigned controller may lead to an unstable situation since the LPF does not provide sufficient stability margins to change the controller parameters freely without the risk of retrograding stability.

V. CONCLUSIONS

In this paper, stability and accuracy of PHIL simulations are discussed through analytical studies as well as experimental tests. Effects of impedances of HuT and virtual side on stability for the voltage type and current type interfaces are analyzed. It has been concluded that equivalent impedance of the two sides is a determining factor for stability. The voltage type interface is stable when equivalent impedance of the virtual side is smaller than HuT impedance. On the other hand, when HuT impedance is smaller than virtual side equivalent impedance, current type interface is stable. In other words, aside from the type of interface, if the impedance which is connected to the current source is smaller, the system will be stable. Moreover, time delay caused by different components including the real-time computer is another important factor that can limit stability margins. It has been shown that an LPF can improve the stability of PHIL but its parameters must be tuned carefully. Although the smaller corner frequencies imply on more stability margins, increasing the time delay imposed by the filter deteriorates the accuracy of the results. Practical PHIL test results using an RTDS confirm the validity of the proposed analysis.

REFERENCES