# Active Positive Sloped Equalizer for X-Band SiGe BiCMOS Phased Array Applications

Can Çalışkan, Abdurrahman Burak, Esref Turkmen, Melik Yazıcı and Yasar Gurbuz

*Abstract*— **This work presents an active equalizer circuit with positive gain slope at X-Band (8 - 12 GHz). Compared to passive examples, the active equalizer realized better filter and impedance characteristics in frequency of interest with increased functionality for a single amplification stage. It achieved close to 10 dB of peak gain, a + 1.13 dB/GHz gain slope with 2.8 dB NF by utilizing cascode topology. The design reaches a -1.5 dBm input-referred compression point (input-P1dB) while consuming 46 mW of power. To the best of authors' knowledge, the presented work achieves the best on-chip gain, a gain slope and NF performance in the literature as an equalizer that utilizes SiGe BiCMOS technology.**

*Index Terms*— **amplifiers; active filters; noise; BiCMOS integrated circuits; transceivers.**

## I. INTRODUCTION

MODERN phased array systems include thousands of transceiver blocks, which leads transceivers to be the dominant block not only on RF features of the system, but also on total cost, area consumption, power and heat dissipation [1, 2]. In addition to improvements in technology, demand is increasing both commercially [3] and in the aerospace-military industry to broaden the data rate in communication links [4] and to generate multiple beams. The systems that depends on single beam operation also demands wide operation bandwidth to reduce the unnecessary repetition of the blocks.

The new generation transceiver modules require high performance such as low noise, high gain and high phase/amplitude control in addition to compactness, high integration capability, low power dissipation and low cost [5, 6]. Hence, the number of sub-blocks is increased to satisfy the demands of the market, which results with complicated transceiver architectures. As a result, the transfer function characteristics of the transceivers or multifunctional chips have started to be complicated and it is degrading the 3-dB gain bandwidth of the system due to resulting a negative gain slope [7].

Rieger presented a GaN based X-Band T/R module on LTCC substrate [8]. It has around 35 dB of receiver (RX) gain, however its 3-dB gain bandwidth (BW) is relatively low; the gain decreases about 10 dB (-2.5dB/GHz) from 8-to-12 GHz. Masuda demonstrated GaN based LNA that achieves close to 20 dB gain at 10 GHz with around -1.75 dB/GHz of gain slope [9]. Bentini presented a wideband T/R module

C. Çalışkan, A. Burak, E. Türkmen, M. Yazıcı and Prof. Y. Gurbuz are with the Electronics Engineering at Sabanci University, Faculty of Engineering Natural Sciences, Tuzla, 34956, İstanbul, Turkey (email: yasar@sabanciuniv.edu).

core-chip in GaAs technology; its RX gain drops to 18 dB at 14 GHz, which is about 23.5 dB at 9 GHz (-1.1 dB/GHz) [10]. Jeong demonstrated a SiGe BiCMOS X-Band multifunctional chip with 5-bit of phase and amplitude control; its receiver and transmitter gain slopes are -3.33 dB/GHz and -5 dB/GHz, respectively [11]. As can be seen from the examples given above, they might suffer from 3-dB BW due to having negative gain slope, which can be even worse after the system integration. Hence a certain level of gain flatness is desired in recent generation of transceivers [12]. Integration of an external equalizer might contradict with the compactness of the system. Moreover, on-chip passive equalizers can worsen the total gain and noise figure (NF) due to limited quality factor of the components. Therefore, active equalizers become a significant block for the system due to improving the 3-dB gain bandwidth of the new generation transmit/receive (T/R) module core-chips.

Several methodologies have been developed to accomplish expected filter characteristics for the equalizer. Hsiao proposes a transformer-based ring filter by using SiGe BiCMOS technology; however, this work aims at band selection, instead of equalization [13]. Madjar illustrates an active tunable equalizer for 2 – 4 GHz which utilizes an amplifier and a feedback mechanism as an MIC circuit on a duriod substrate [14]. Similarly, Bera demonstrates p-i-n diode based equalization by utilizing lead components [15]. Additionally, an equalization method is presented at X-Band by Camarchia on a GaN MMIC power amplifier which depends on input matching; this design achieved a certain level of gain flatness [16]. Lu demonstrated a transformer based analog equalizer to achieve 18 dB peak gain at 25 GHz [17]. Jeong also presented a wideband GaAs multifunctional chip with 8-bit true time delay and 7-bit amplitude control, which utilize three separate amplifiers to tolerate the negative slope; the amplifier added to the multifunctional chip has 12 dB of gain with 1 dB of positive slope. Its area is 5.2 mm$^2$ and consumes about 500 mW of power [7]. However, the mentioned works have high noise figure (NF), limited positive slope and compactness, without sacrificing the gain and return loss performances.

This paper presents an active equalizer with a positive gain slope for X-Band phased array applications, which is designed by utilizing IHP Microelectronics' 0.25 μm SiGe BiCMOS technology. The priority of this equalizer is to obtain a positive sloped gain with a return loss performance which would not affect the sequential blocks of the transceiver, as presented in Fig. 1. In addition to gain and slope specifications, NF and the linearity of the equalizer are also
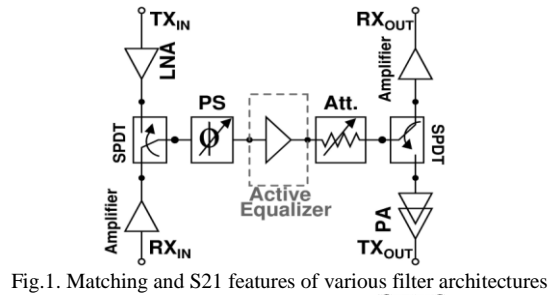
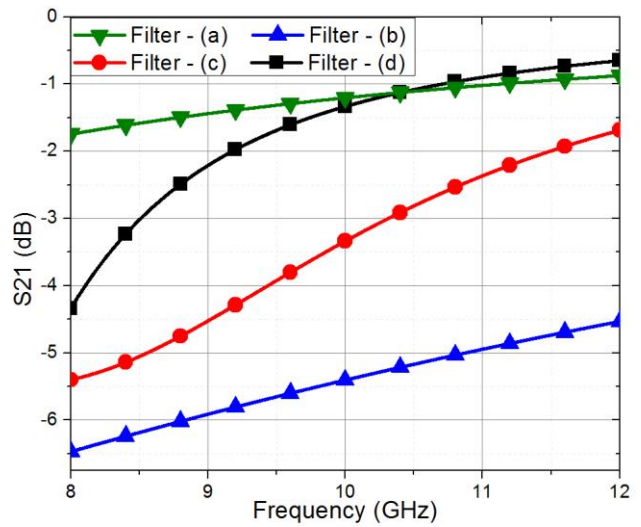Fig.1. Matching and S21 features of various filter architectures
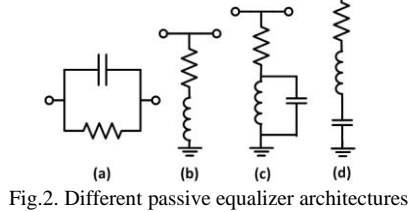


Fig.2. Different passive equalizer architectures

considered. The design procedure of the presented equalizer is described in Section II, while the measurement results are demonstrated in Section III. Section IV summarizes the presented work as the conclusion.

## II. ACTIVE EQUALIZER DESIGN PROCEDURE

The proposed equalizer amplifier consists of an amplification and a filter section; therefore, the design process starts by selecting an appropriate amplifier topology and a filter architecture to conclude with the desired positive gain sloped active equalizer.

### A. Proper Filter Topology Selection

Achieving a high gain slope is one of the prior expectations of the active equalizer amplifier. In this content, several filter architectures have been developed, as represented in Fig.2 [4]; higher order topologies exist however, the total area rises as the order of the filter is increased. The presented passive filters are compared between each other in terms of their loss behavior and impedance matching as in Fig.3 and Fig.4, to decide appropriate filter architecture for the amplifier. The filters are designed by considering same resonant frequency and 50 Ω termination. As can be seen from the results in Fig.3, filter (a) can achieve low loss where it has a moderate level of return loss as shown in Fig.4. However, the low gain slope is the main disadvantage of filter (a). The filter (b) has higher gain slope, but it has poor matching performance. Although the filters (c) and (d) have the expected gain slope, their behavior within the amplifier should be considered.

At resonant frequency, the LC tank circuit of the filter (c) acts like an open circuit, which causes deviation in impedance as frequency varied. The filter (d) adds an additional shunt resistor and lowers the quality factor of the output matching network by short circuiting the resistor at resonant frequency, which is high impedance for the filter (c). Hence, the filter (d) was preferred for the presented work.

### B. The Amplification Stage

The passive equalizers suffer from high loss and NF. Therefore, a proper amplification stage should be chosen for
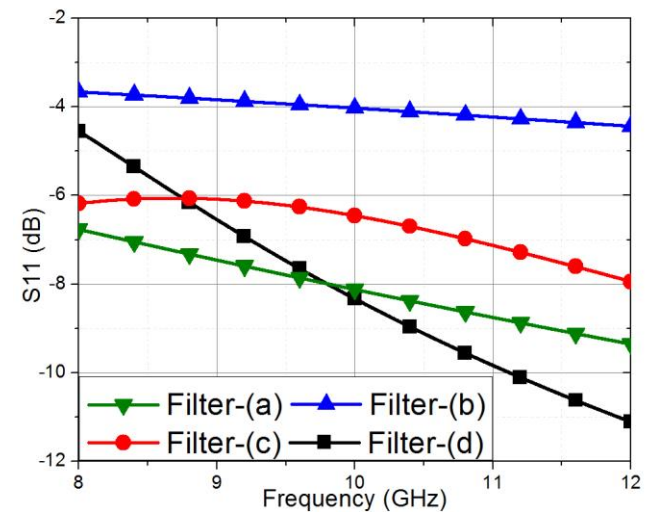


Fig.3. S21 features of given filter architectures



Fig.4. Matching performance of given filter architectures

the proposed active equalizer amplifier to surpass the metrics of the passive counterparts. Common-Emitter (CE) and cascode architectures are the two basic and generally favored amplifier topologies; CE amplifiers can achieve low NF and a moderate level of gain. However, the HBT sizes in CE amplifier is optimized regarding noise match, which is decreasing base-to-collector impedance. This causes lower isolation; therefore, including a filter would challenge the design process of the CE amplifier. Compared to the CE amplifier, cascode topology is capable of cancelling Miller effect, which results in a high output impedance and better input-output isolation [18]. It results with a higher power and noise level; however, it can suppress the noise of the following stages due to having a higher gain level. Hence, the cascode topology was preferred for the amplification stage of the active equalizer.

### C. Design of the Output Terminal

The output matching network of the amplifier and the filter should be designed coherently to succeed the targeted slope level and impedance termination. However, achieving expected slope and matching performance simultaneously is
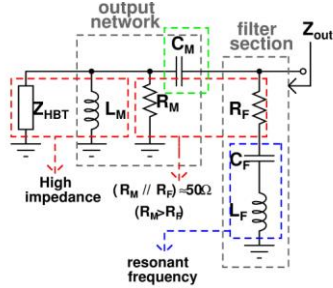
Fig.5. The basic model used for analyzing the output of the active equalizer.

$$Z_{out}(\omega_L) \cong \frac{R_F\left(1 + j\omega_L R_M C_M\right)}{1 + j\omega_L C_M\left(R_F // R_M\right)} \tag{1}$$

$$\Re\{Z_{out}\} = 50\,\Omega \cong R_F // R_M \tag{2}$$

$$|H(\omega)| = \frac{R_F + \dfrac{1}{j\omega C_F} + j\omega L_F}{R_F + \dfrac{1}{j\omega\left(C_F // C_M\right)} + j\omega L_F} \tag{3}$$

$$loss\ of\ the\ filter \cong 20\log\left(\frac{C_F // C_M}{C_F}\right) \tag{4}$$

(LNA). However, the amplifier was optimized for the higher end of the selected frequency band to maximize the gain at the higher end of the band. This assists the amplifier in achieving a positive slope. The procedure continued by following the generally known simultaneous noise and power match technique [18]. The optimum bias current was selected for lowest $NF_{min}$ succeeding of the HBT. The size of the devices were selected regarding the optimum source resistance ($R_{s,opt}$). The proper input termination was achieved by determining adequate emitter inductance, where a series base inductor was used to neutralize the imaginary part of (1). An RF-choke inductor ($L_{RF-CHOKE}$) was preferred to bias the amplifier and to improve the input matching performance at the frequency of interest. It should be noted that the presented work is not designed to replace the LNA of a receiver. It is an amplifier to improve the gain characteristic of the system without sacrificing from the remaining performance metrics.

The output terminal of the active equalizer is the most critical part of the design. Although the filter can achieve expected characteristic, it cannot provide desired impedance termination. Similarly, if the amplifier is optimized to have a positive sloped gain, it can fail from proper in-band terminal matching. The described trade-offs surpassed by following design steps mentioned in section-C; Fig.7 presents the simulated impedance terminations of the amplifier (Amp.), filter and their cascaded version which is the active equalizer amplifier (EQ-Amp). As shown, the amplifier fails to achieve proper 50 Ω output termination of its own. The filter has a better impedance matching due to including a shunt 70 Ω resistance, which limited the slope level. When the amplifier and the filter were designed separately, they gave neither expected slope level nor matching performance. As presented, adequate level of output matching is achieved after cascading the filter and the amplifier stage.
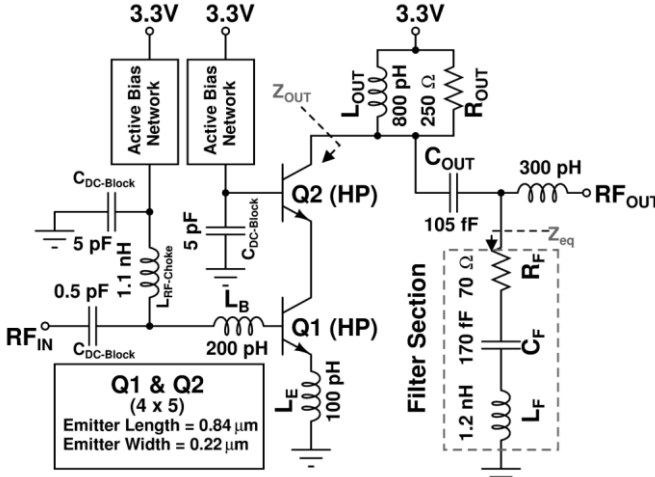


Fig.6. Schematic of EQ-Amp and top view of the fabricated chip

remaining as a trade-off; the filter (d) may achieve positive slope with a poor terminal matching in defined band. Therefore, the amplification stage and filter stage had to be designed coherently to satisfy the expectations.

The model in Fig.5 was used for the output terminal calculations of the active equalizer amplifier. The output impedance of the amplifier ($Z_{HBT}$) is a high value because of the nature of the cascode topology, while a shunt inductor, $L_M$, is utilized to resonate with the imaginary part of $Z_{HBT}$ in frequency of interest. The $C_F$ and $L_F$ are the components that are determining the center frequency of the band-reject filter, $\omega_L$. At $\omega_L$, the output impedance of the amplifier ($Z_{out}$) can be approximated as in (1); if $R_M$ and $C_M$ is chosen to dominate the imaginary parts in (1), the real part of $Z_{out}$ will be determined by $R_M$ and $R_F$ as shown in (2). To validate the calculations $R_M$ should be larger than $R_F$.

The preferred band-reject filter can be converted to a high-pass filter by including the $C_M$, which aids to achieve shaper filter characteristics. The transfer function between $C_M$ terminals can be calculated as in (3). The additional loss that $C_M$ is going to introduce for $\omega < \omega_L$, can be approximated as in (4); $C_M$ will be behaving like a short circuit for $\omega > \omega_L$, which result with a sharp positive slope and desired impedance termination simultaneously.

*D. The Active Equalizer Amplifier Design*

The total schematic of the presented Equalizer Amplifier (EQ-Amp), which is the combination of amplifier and filter section, can be seen from Fig.6. The design steps of the amplifier stage are similar to those of a Low Noise Amplifier

The DC biases were chosen by considering the linearity of the design; high-performance (HP) HBTs were selected for both Q1 and Q2, and they were biased to maximize the voltage swing. The design includes active bias networks to provide required voltage and current level. On-chip inductors were utilized in both EQ-Amp, which were custom designed by using Sonnet: IHP Microelectronics' 0.25 µm SiGe BiCMOS technology offers three thin and two thick metal layers, where thick metals are employed for inductors to achieve a quality factor of 20.
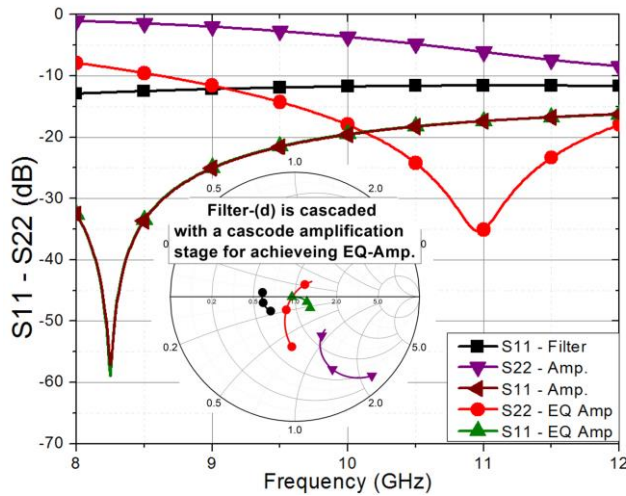
Fig.7. Matching performance of filter, amplifier and EQ-Amp


Fig.8. Top view of EQ – Amp Chip (0.95 x 1.126 = 1.07 mm² area)

## III. Measurement Results

The proposed EQ-Amp has a 1.07 (0.95 x 1.126) mm² area including pads, as shown in Fig. 8. An R&S ZVL Network Analyzer was used to measure the S-Parameters of EQ-Amp, while NF and linearity measurements were done by using Agilent ESA-E E4407B Spectrum Analyzer, 346A noise source, Agilent 8705C Pre-amplifier, and 8267D Vector Signal Generator.

Fig.9 demonstrates the gain performance of the described active equalizer amplifier (EQ-Amp). The design achieved 9.8 dB peak gain at 12 GHz and which is adequate to compensate the NF of remaining blocks in a transceiver. The EQ-Amp achieved +1.13 dB/GHz of positive gain slope. Additionally, it can be adjusted up to 0.8 dB by changing the bias of the Q2 transistor, which updates the gain slope to 0.95 dB/GHz. The measured gain is about 1 dB lower than expected, due to variations in the active bias networks which affected the current density of the HBTs. Fig.10 presents the simulated and measured input-output matching performance of the (EQ-Amp). As shown, the measurements are coherent with the simulations and the desired level of terminal matchings are achieved for X-Band; the deviations are attributed to not including RF Pads in EM simulations.

Fig.11 shows the NF measurements of the EQ-Amp, which is 2.8 dB at 12 GHz. The EQ-Amp has a positive slope gain; therefore, the NF decrease as frequency increase as expected. Moreover, the deviation in gain performance also reflected to the NF measurements, especially at low frequencies due to having low gain. The input-P1dB (IP1dB) of the EQ-Amp should be as high as possible while consuming low power; it should to be able to compete with the passive counterparts and be compatible with the adjacent blocks of the system. The design reaches a - 1.5 dBm of input-P1dB while consuming a 46 mW of power, as shown in Fig.12. The design is unconditionally stable at X-Band as shown in Fig.13.

The slope of the EQ-Amp design can be increased by changing the gain peaking frequency of the amplifier and the resonant frequency of the filter section. That would result with higher gain slope with the expense of higher NF, due to
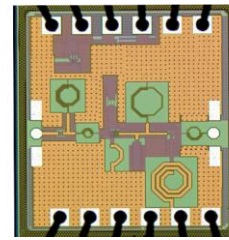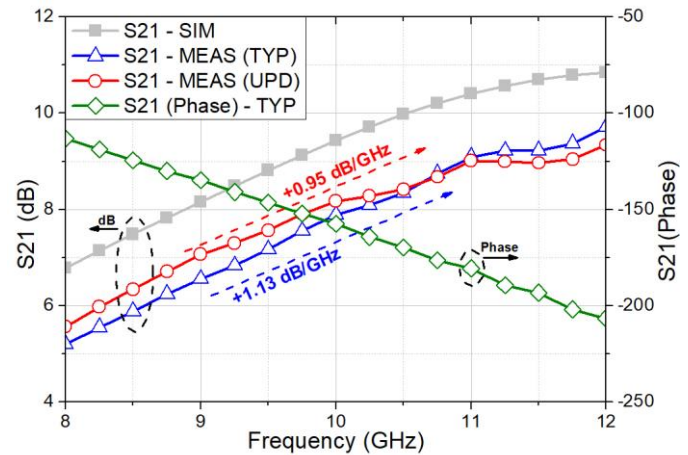

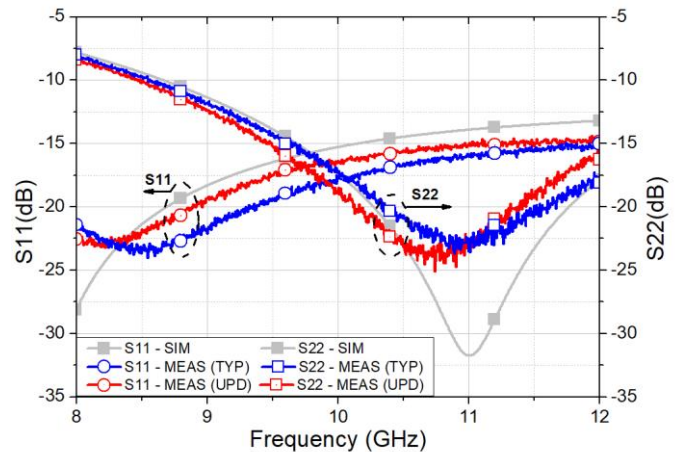Fig.9. Measured and simulated gain of the EQ-Amp


Fig.10. Matching performance of measured EQ Amp

shifting the peak gain of the amplifier to a higher frequency. The area and power dissipation of the design would be approximately same, but the input-and-output matching of the amplifier must be reconsidered.

## IV. Conclusion

In this paper, a new active equalizer amplifier is presented for a positive gain slope to broaden the 3-dB gain bandwidth of a transceiver. We achieved this by using the design method of integrating passive filter and an amplification stage to realize the main features of a filter with adequate level of gain. The measured EQ-Amp achieved more than 9.5 dB gain and 2.8 dB NF at 12 GHz. It has - 1.5 dBm of input-P1dB, while consuming 46 mW power. The presented work has a low NF regarding to its gain slope; the NF might be much larger if the expected performance is achieved by a passive equalizer due to having insertion loss. Additionally, its gain level is high
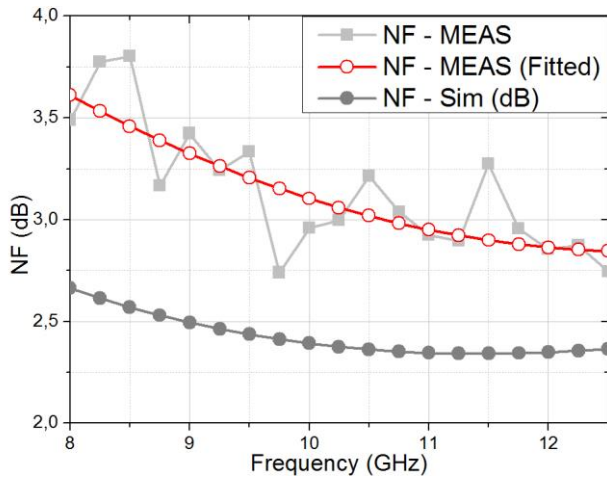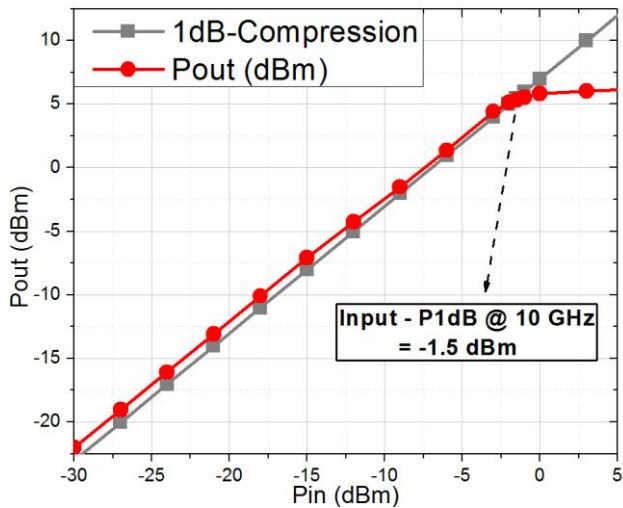
Fig.11. S21 and NF performance of measured EQ Amp



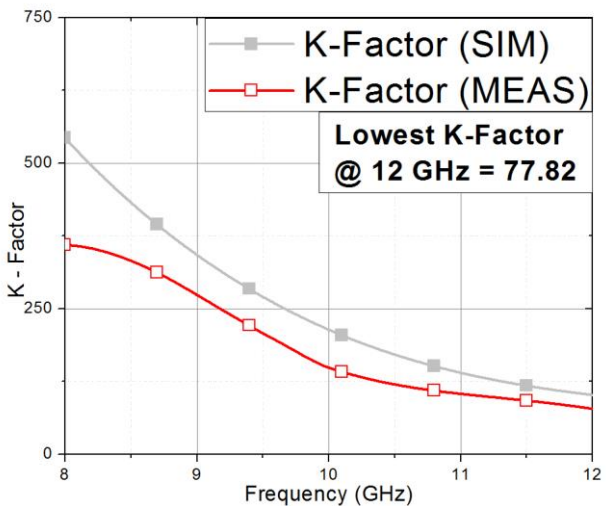Fig.12. Measured input-P1dB and K-factor performance of EQ-Amp



Fig.13. Measured input-P1dB and K-factor performance of EQ-Amp

enough to both suppress the noise of the incoming blocks. Compared to the similar amplifier presented in [13], the presented EQ-Amp achieved higher gain slope with low power consumption in a compact area. To the best of authors' knowledge, the presented work achieves the best positive gain slope and NF performance in SiGe BiCMOS technology.

## REFERENCES

[1] D. N. McQuiddy, R. L. Gassner, P. Hull, J. S. Mason and J. M. Bedinger, "Transmit/receive module technology for X-band active array radar," in *Proceedings of the IEEE*, vol. 79, no. 3, pp. 308-341, Mar 1991.

[2] X. Chen, Y. Shen, Z. Wang, W. Rhee and Z. Wang, "A 17 mW 3-to-5 GHz Duty-Cycled Vital Sign Detection Radar Transceiver With Frequency Hopping and Time-Domain Oversampling," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 4, pp. 969-980, April 2017.

[3] C. Lai, K. Tan, Y. Chen and T. Chu, "A UWB Impulse-Radio Timed-Array Radar with Time-Shifted Direct-Sampling Architecture in 0.18-μm CMOS," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 7, pp. 2074-2087, July 2014.

[4] A. Fejzuli, R. Kaarsberg, and N. Roldan, "Broadband amplifier gain slope equalization with a single passive component," *High Freq. Electron.*, vol. 5, no. 6, pp. 22–26, Jun. 2006.

[5] M. Caruso, M. Bassi, A. Bevilacqua and A. Neviani, "A 2–16 GHz 65 nm CMOS Stepped-Frequency Radar Transmitter with Harmonic Rejection for High-Resolution Medical Imaging Applications," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 2, pp. 413-422, Feb. 2015.

[6] A. Jha, F. Zhang, T. Hsieh, R. Gharpurey and P. R. Kinget, "A Discrete-Time Digital-IF Interference-Robust Ultrawideband Pulse Radio Transceiver Architecture," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 2, pp. 481-494, Feb. 2010.

[7] J. C. Jeong, I. B. Yom, J. D. Kim, W. Y. Lee and C. H. Lee, "A 6–18-GHz GaAs Multifunction Chip With 8-bit True Time Delay and 7-bit Amplitude Control," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 5, pp. 2220-2230, May 2018.

[8] R. Rieger, A. Klaaßen, P. Schuh and M. Oppermann, "GaN based wideband T/R module for multi-function applications," *2015 European Microwave Conference (EuMC)*, Paris, 2015, pp. 514-517.

[9] S. Masuda *et al.*, "GaN single-chip transceiver frontend MMIC for X-band applications," *2012 IEEE/MTT-S International Microwave Symposium Digest*, Montreal, QC, 2012, pp. 1-3.

[10] A. Bentini, M. Ferrari, P. E. Longhi, E. Marzolf, J. Moron and R. Leblanc, "A 6–18 GHz GaAs multifunctional chip for Transmit/Receive Modules," *2014 11th European Radar Conference*, Rome, 2014, pp. 605-608.

[11] J. C. Jeong and I. B. Yom, "X-band high power SiGe BiCMOS multi-function chip for active phased array radars," in *Electronics Letters*, vol. 47, no. 10, pp. 618 -619, 12 May 2011.

[12] A. Meaamar, C. C. Boon, K. S. Yeo and M. A. Do, "A Wideband Low Power Low-Noise Amplifier in CMOS Technology," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 4, pp. 773-782, April 2010.

[13] Y. C. Hsiao, C. Meng and S. T. Yang, "2.4-GHz Q-Enhanced Lumped Ring Filter With Two Transmission Zeros Using 0.18-μm SiGe BiCMOS Process," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 3, pp. 305-307, March 2017.

[14] A. Madjar, B. Even-Or and E. Gertel, "A novel 2-4 GHz multi-passband tunable and gain controlled miniature active equalizer/filter," *IEEE MTT-S International Microwave Symposium Digest*, Boston, MA, USA, 1991, vol.2, pp. 451-454.

[15] S. C. Bera, "Amplitude Tilt Active Equalizer for Frequency and Temperature Compensation," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 7, pp. 344-346, July 2011.

[16] V. Camarchia, J. Fang, G. Ghione, J. M. Rubio, M. Pirola and R. Quaglia, "X-band wideband 5W GaN MMIC power amplifier with large-signal gain equalization," *Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits*, Dublin, September 2012, pp. 1-3.

[17] J. Lu and S. Liu, "A 50-Gb/s 10-mW Analog Equalizer Using Transformer Feedback Technique in 65-nm CMOS Technology," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 10, pp. 783-787, Oct. 2009.

[18] W. M. L. Kuo, Qingqing Liang, J. D. Cressler and M. A. Mitchell, "An X-band SiGe LNA with 1.36 dB mean noise figure for monolithic phased array transmit/receive radar modules," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium,* June 2006.