Fully Depleted MAPS in 110-nm CMOS Process With 100–300-m Active Substrate

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# Fully Depleted MAPS in 110-nm CMOS Process With 100–300-$\mu$m Active Substrate

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***Abstract*— This article presents a fully depleted monolithic active pixel sensor technology compatible with a standard deep submicrometer 110-nm CMOS process. Passive test pixels structures, produced in various flavors, have proved the feasibility of 100- and 300-$\mu$m-thick active substrates. Active pixel sensors with monolithically integrated analog and digital electronics, consisting of a 24 $\times$ 24 array of pixels with 50-$\mu$m pitch, have been shown to be fully functional when operating in the full depletion mode. Characterization results obtained with a proton microbeam and a $^{55}$Fe radiation source are presented and discussed.**

***Index Terms*— CMOS, monolithic active pixel sensor (MAPS), radiation detector, silicon.**

## I. Introduction

MONOLITHIC active pixel sensors (MAPSs) are emerging as a viable alternative to hybrid pixels in charged-particles' detection and high-energy photons imaging, showing advantages in both performance and overall costs per unit area [1]–[3].

The reconstruction with the highest precision of the perigee parameters of charged-particle trajectories in a dense environment calls for pixel pitches of tens of micrometers, low material budget, a high signal-over-noise ratio, and limited diffusion of the charge carriers originated by the impinging particle. These specifications can be obtained with a monolithic design implemented on a fully depleted (FD) high-resistivity substrate. As a consequence, FD-MAPSs are raising a significant interest in the high-energy physics community [4], [5].

FD-MAPSs have also been proposed for X-ray imaging [6], where an active substrate of 300–500 $\mu$m would enable an efficient detection of photon energies up to 15 keV. Other applications, such as medical particle tomography and tracking in space experiments, would benefit from the low material budget, fine pixel pitch, and low power consumption offered by MAPS sensors [7], [8].

As a general trend in the development of pixel sensors, the complexity of on-chip digital functions is increasing, making it easier to integrate and deploy a complete sensor system. Moreover, event-driven readout schemes are frequently adopted to reduce power consumption and, in turn, relax the requirements of the cooling systems, impacting on the overall system material budget. To these purposes, very scaled process nodes should be used to reduce the area and to increase the speed of on-chip digital electronics.

The latest FD-MAPS design efforts in the high-energy physics community are adopting 180- and 150-nm process nodes. Most of the developments, in this respect, have been devoted to the implementation of devices with a depletion region ranging from a few tens of micrometer and hundreds of micrometer [4], [5]. In [4], large depletion regions are obtained by including the electronics inside a deep n-well that is used as a collection node for the electrons generated by the incident charged particles. This approach has demonstrated an excellent radiation hardness and a fast charge collection, but the sensor capacitance is relatively large, and a nonnegligible part of the pixel area cannot be used to accommodate the readout circuits. Scaling to very small pixels is thus very challenging while using such topology.

An alternative approach, arising from an evolution of the pixels designed for the ALICE detector [1], uses small sensing nodes while implanting a low-doped n-type region below the electronics [5]. In this way, most of the generated charges can be collected by drift, while the area and the capacitance of the sensors are maintained small, granting scalability toward

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small pixel sizes. This approach, although excellent for particle tracking, cannot be easily extended to an active thickness in excess of 100 $\mu$m since the space-charge region extends from the top surface of the sensor, thus limiting the applicable voltage at the sensor top side.

The possibility of FD thick substrates in CMOS-integrated sensors has been first explored in [9], demonstrating an FD sensor with p-type substrate and a n-type backside implantation. In the first prototype, the electronics were made entirely of p-type transistors. A similar approach was adopted in [10], using a CMOS process with n-type substrates and implanting a p+ region on the back.

Full depletion can also be obtained using a silicon-on-insulator process. Although the radiation damage of the insulator oxide poses several challenges related to parameter drift in the transistor characteristics, the latest advancements have greatly improved the radiation hardness of the process, and sensors with depletion regions up to 500 $\mu$m thick have been demonstrated [11].

In this article, we present a technology platform for the implementation of FD MAPS based on a modified 110-nm CMOS process. The process node was chosen to enable the in-pixel implementation of complex digital functions while keeping low prototyping and production costs. Backside processing was used to create a junction on the bottom surface that is biased to deplete the whole sensor substrate.

This article is structured as follows. Section II discusses the simulated characteristics with reference to geometry and process parameters. In Section III, the design of pixel test structures and a small array of active pixels with integrated electronics are presented. Section IV presents the results of the characterization of the arrays compared with the expectations according to the simulation. The perspectives for this technology are highlighted in Section V.

## II. Sensor Concept

The process was developed starting from a 110-nm industrial CMOS with 1.2-V transistors and six metal layers. A few add-ons were necessary to allow for full substrate depletion with electron collection at the sensing electrodes. A concept cross section of the pixel array is shown in Fig. 1 [12].

The standard p-type substrate was replaced with an n-type floating zone material. Wafer thinning and backside lithography were necessary to introduce a junction at the bottom surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side. A shallow boron-doped region was implanted on the rear side of the wafer, and the dopants were activated by laser annealing. Since, at large wafer thicknesses, the voltage needed for sensor full depletion exceeds 150 V, a termination structure composed of multiple guard rings was introduced.

A deep p-well scheme was used to prevent the n-wells hosting p-MOSFETs from collecting the charge generated by radiation in the substrate. Care had to be taken to limit the punchthrough current between the back-side junction and the deep p-well at sensor full depletion. A good control of punchthrough could be obtained either by increasing the bias voltage at the pixel sensor nodes or by increasing the n-dopant concentration below the p-wells. Since the sensors had to be directly coupled to the low-voltage electronics, the second solution was adopted, by adding an n-doped epitaxial layer, having a resistivity lower than the substrate, to the process flow.

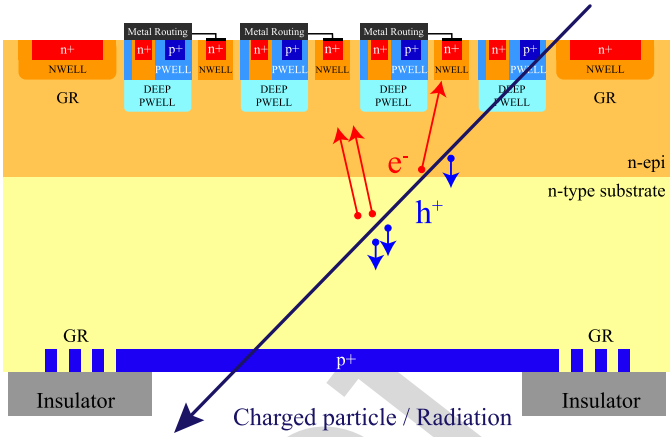


Fig. 1. FD pixel sensor cross section.

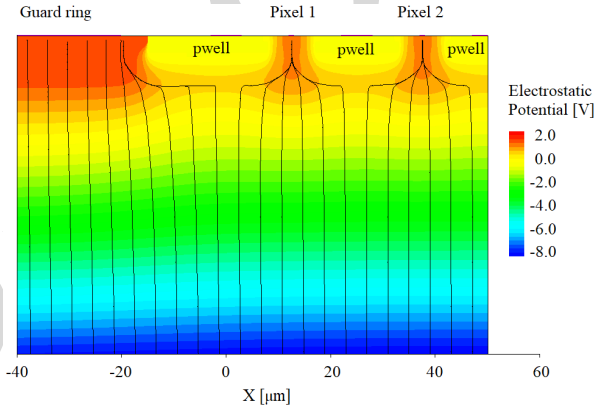


Fig. 2. Simulated 2-D potential profile and electric-field lines at full depletion. The simulation domain includes part of the guard rings and 2 pixels with 25-$\mu$m pitch. Only the sensor surface region is shown.

TCAD simulations were used to tune the process parameters. The simulated potential profile at full depletion for a domain, including 2 pixels and part of the surface guard ring, is shown in Fig. 2. Electric-field lines are orthogonal to the sensor surface up to the bottom of the deep p-wells, and then, they deviate horizontally toward the collection electrodes.

The full depletion and punchthrough voltages were simulated on this domain by introducing a small unbalance (10 mV) between pixel and guard ring bias voltages. The current flowing at the sensing electrodes and at the backside as a function of applied backside bias is shown in Fig. 3. At low reverse voltage, the substrate is not FD, and resistive paths exist between the pixels and the guard ring, leading to a macroscopic current. As the bias voltage is increased, a sharp current drop is observed, indicating the onset of full depletion. The depletion voltage is reduced by increasing the voltage applied at the front side to the sensor nodes. If the backside voltage is further increased, a punchthrough current starts flowing and

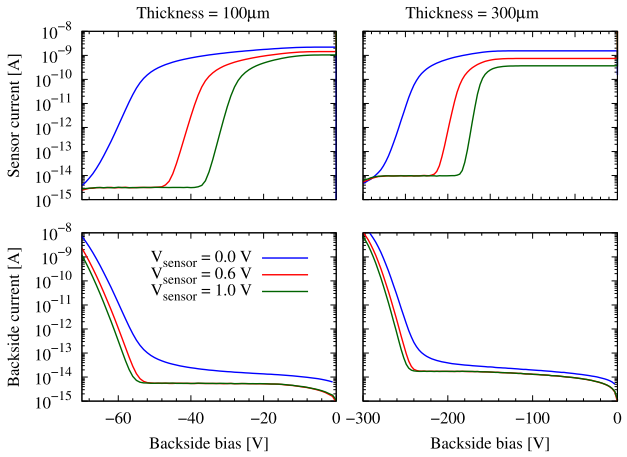


Fig. 3. Simulated sensor and backside current as a function of backside voltage for two values of sensor thickness [100 $\mu$m, (left) and 300 $\mu$m (right)]. Pixel pitch is 25 $\mu$m.

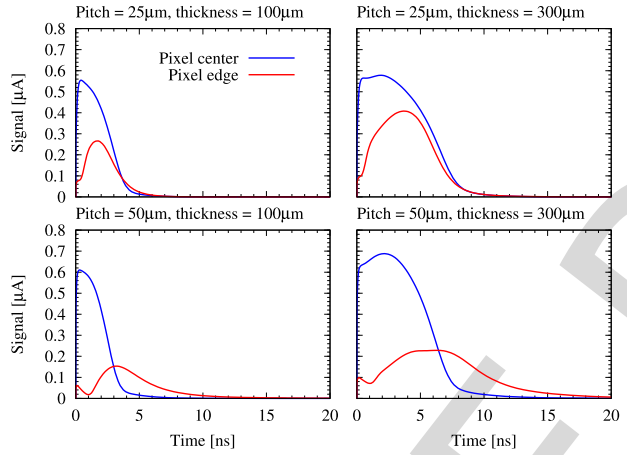


Fig. 4. Simulated transient current signal with an incident MIP for two different values of sensor thickness [100 $\mu$m (left) and 300 $\mu$m (right)] and pixel pitch [25 $\mu$m (top) and 50 $\mu$m (bottom)].

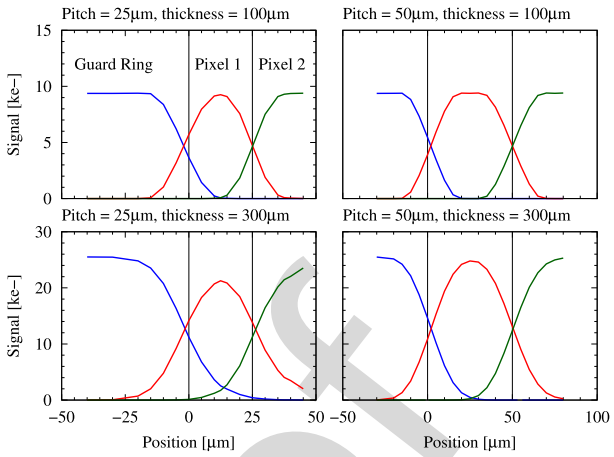


Fig. 5. Simulated collected charge at the sensor periphery as a function of the position of the incident particle for two different values of sensor thickness [100 $\mu$m (top) and 300 $\mu$m (bottom)] and pixel pitch [25 $\mu$m (left) and 50 $\mu$m (right)].

eventually reaches very large values. The voltage difference between breakdown and punchthrough voltages depends on the sensor bias. At a sensor voltage between 0.6 and 1 V that can be applied if the sensor is directly coupled to the electronic readout channels, the difference between full depletion and punchthrough is a fraction of 10%–20% of the applied bias voltage. This value is large enough to reliably accommodate the operation of a pixel array, considered possible doping gradients and nonuniformities between the pixels.

Charge collection dynamics upon the incidence of a minimum ionizing particle (MIP) were also simulated. The MIP was modeled as a continuous charge density of 80 e–h pairs/$\mu$m, orthogonal to the sensor surface and extending throughout the sensor thickness. With reference to the simulation domain shown in Fig. 2, several positions of incidence were considered for the MIP. The current signal generated at the sensor is shown in Fig. 4 for two different MIP incidence positions, two values of pixel pitch (25 and 50 $\mu$m), and two values of sensor thickness (100 and 300 $\mu$m). As expected, complete charge collection is observed in less than 5 and 10 ns, respectively, for 100 and 300 $\mu$m thickness when the MIP is incident in the center of the pixel. If the MIP is incident at the pixel periphery, the collection speed depends on the pixel pitch; at 50-$\mu$m pitch, the collection time approximately doubles since the charge generated in the substrate first reaches the bottom of the deep p-well and then drifts horizontally toward the collection node. Even considering this worst case situation, however, the charge is completely collected within 20 ns. In 25-$\mu$m pixels, on the contrary, the collection time is only slightly degraded, as a result of the smaller horizontal distance traveled by electrons generated at the pixel periphery.

The integrated charge as a function of the MIP incidence position is shown in Fig. 5. Charge sharing between the pixels for two values of thickness and pixel pitch can be observed. As expected, sharing slightly increases by increasing the pixel pitch and sensor thickness, but, in all the cases considered here, the effect is confined to the nearest neighboring pixels.

## III. Active Pixel Array and Test Structures

A 576-active pixel array was designed as a test bench to validate the performance of the proposed technology [13], [14]. The pixels are organized in four sectors, each one consisting of 6 columns of 24 pixels. An end-of-column (EoC) block manages the column logic, handling pixel configuration and controlling data transmission. In this way, each sector works in parallel with the others. To read out the data for a single sector, two clocks are used. The first controls the shift register in the EoC to select the column, whereas the second one is dedicated to the row shift register. In a typical case, they, respectively, work at 5 and 0.2 MHz. Thus, the whole array can be read in less than 30 $\mu$s using a 5-MHz clock.

A single 50-$\mu$m pitch pixel hosts both the electrode and the in-pixel electronics. The sensing electrode, together with a surrounding area clear from electronic circuits, occupies a region of 20 $\mu$m $\times$ 20 $\mu$m, and it is centered in the pixel area. The remaining area is partitioned between the analog front end and the digital logic.

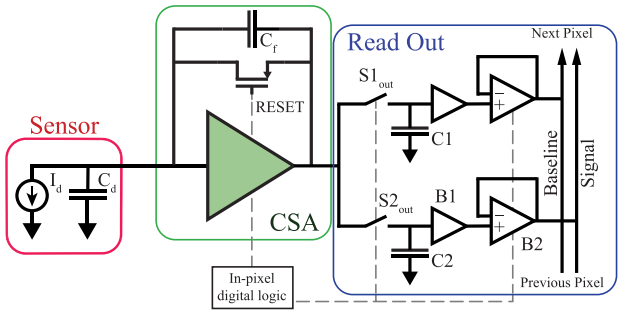


Fig. 6. Pixel readout block scheme.

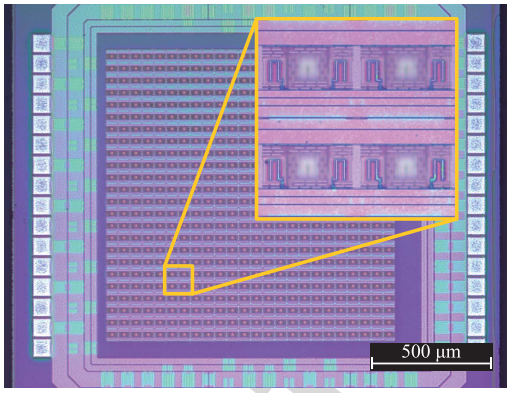


Fig. 7. Micrograph of active pixel array. Inset: close-up of 4 pixels.

The readout chain is shown in Fig. 6. The radiation-generated current signal is amplified by a charge-sensitive amplifier (CSA) circuit. A sample and hold circuitry, designed to perform correlated double sampling (CDS) operation, follows the CSA. Metal–insulator–metal (MIM) capacitors are used to store the signal at this stage. Two analog buffers are included to transmit the analog output signal along the column.

The charge-integrating amplifier, designed to maximize the signal-to-noise ratio (SNR), is based on a telescopic cascode architecture with a feedback capacitor $C_f$ and a minimum-size pMOS reset switch. $C_f$ has been chosen equal to 5.8 fF, giving a postlayout simulation gain of 130 mV/fC. The output dynamic range of the amplifier is defined by considering the expected signal for an MIP in a 300-$\mu$m-thick detector. Thus, for 3.8 fC (corresponding to 80 e–h pairs/ $\mu$m in 300 $\mu$m thickness), the output voltage signal matches the linear output range of the amplifier, which is around 500 mV. This gain also ensures a good SNR for MIPs in substrates with a thickness as low as 50 $\mu$m.

The pixel unit is also equipped with a digital logic to manage data readout and to define the pixel functions. A 3-bit in-pixel register allows to switch OFF defective pixels, enable the injection of a test pulse for the electrical characterization of the readout electronics, and enable the buffer amplifier for data transmission. To study digital noise coupling between the analog and digital sections of the design, each pixel accommodates a digital buffer made by 18 elements, each with a bandwidth of 5 GHz, designed to inject digital noise.

Fig. 7 shows a micrograph of the active pixel array, with a group of 4 pixels in the magnified area. At the center of the pixels, an area free from metal is present to allow the illumination from the top. This feature was included to carry out studies with laser sources.

The pixels were designed for a power consumption around 6 $\mu$W. Providing a power supply of 1.2 V, the power consumption of the pixel array in the static and dynamic conditions is, respectively, 3.84 and 6.4 mW, without considering the contribution of digital and EoC logic.

Small pixel arrays, formed by pixels free from electronic readout circuits, were designed to allow additional flexibility in the experimental evaluation of sensor and process characteristics [12]. In these arrays, these are termed pseudomatrices (PMs) since all the sensing electrodes in the pixels are connected to the same pad, and pixels with both 50- and 25-$\mu$m pitch were included.

TABLE I
PRODUCED SENSOR SAMPLES

| Sensor type | Thickness [µm] | Pixel Pitch [µm$^2$] |
|---|---|---|
| Full Sensor | 300 | $50 \times 50$ |
| PM | 100 | $25 \times 25$, $50 \times 50$ |
| PM | 300 | $25 \times 25$, $50 \times 50$ |
| **PM Pixel pitch [µm]** | **Pseudo-pixels** | **Metal width [µm]** |
| $25 \times 25$ | $16 \times 18$ | 8 |
| $50 \times 50$ | $8 \times 9$ | 15 |

Two fabrication runs, including both pixel arrays and PM test structures, were produced on high-resistivity wafers ($\rho > 2$ k$\Omega \cdot$ cm) that were thinned to 300 and 100 $\mu$m prior to backside processing. A summary of the devices presented in this article is shown in Table I, highlighting their main geometrical characteristics.

## IV. Experimental Results

An extensive experimental test campaign has been carried out on both the test structures and the active pixel arrays in order to assess their functionality. This section summarizes the most meaningful results, discussed with reference to the simulated characteristics presented in Section II.

### A. Electrical Characterization

Static electrical characterizations have been performed at room temperature on PM structures in order to evaluate full depletion and punchthrough voltages for different pixel sizes, thicknesses, and bias conditions. Current–voltage ($I$–$V$) curves have been measured using a four-channel semiconductor parameter analyzer. In the measurements, the same conditions used for the simulations described in Section II have been applied; the p-wells were biased at 0 V, the sensing nodes and the guard ring were biased between 0 and 1 V, and a negative bias sweep was applied to the backside contact. The measured sensor and backside currents are shown in Fig. 8 as a function of the backside bias voltage for PMs with 25-$\mu$m pitch. While the sensor current is plotted for three different values of sensor voltage, only one curve is shown for the backside current since no dependence on sensor voltage was observed.

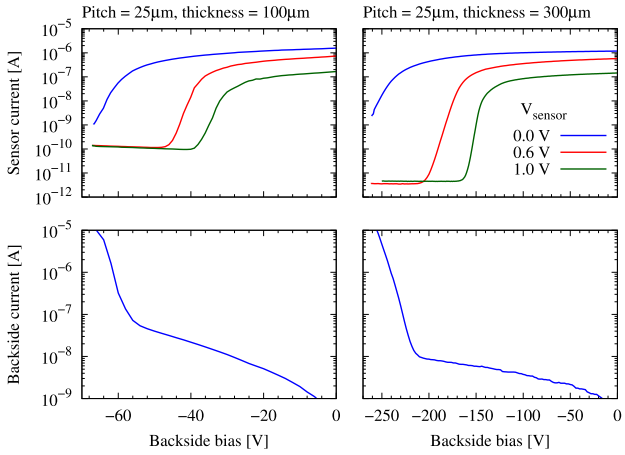


Fig. 8. Measured *I*–*V* curves for 100 $\mu$m (left) and 300 $\mu$m (right) thick PM sensors. Pixel pitch is 25 $\mu$m.

When compared with the simulated curves in Fig. 3, an excellent agreement was found in both the full depletion and the punchthrough voltage for both the device thicknesses and sensor bias voltages. The simulated and measured currents differ by several orders of magnitude due to the different sizes of the simulation domain (single pixel, 25 $\mu$m × 1 $\mu$m in 2-D simulations) and PM sensors (400 $\mu$m × 450 $\mu$m total active area). In the 300-$\mu$m-thick sensors, the measured dark current is more than one order of magnitude smaller than in 100-$\mu$m-thick sensors. Further investigations are going on to understand the origin of this difference, probably due to the different processing conditions. The *I*–*V* curves measured on pixels with 50-$\mu$m pitch are very similar to the ones shown in Fig. 8.

### B. Microbeam Sensor Characterization

The PMs have been tested at the RBI microbeam facility in Zagreb, Croatia [15]. The microbeam has been generated using a 1-MV Tandetron accelerator capable of delivering protons in the 0.5–2.0-MeV range; 2-MeV proton beams with $\sigma_{\text{spot}} \approx 2$ $\mu$m have been focused onto PM structures with different pixel sizes and thickness (see Table I). Protons of this energy have been simulated to have a Bragg peak located at a depth $\lambda \approx 47$ $\mu$m in silicon. As a result, the number of collected carriers and, in turn, the output signal is expected to be independent of the sensor thickness. The proton flux was adjusted to provide a maximum hit rate of 2 kHz.

AQ:4 The DUTs have been wire bonded to a specifically designed PCB equipped with p-i-n connectors to bias the collection electrodes, guard rings, and p-wells. The bias voltages were supplied by a HAMEG HMP2030 power supply, while the high-voltage power supply was an NHQ 202M. As shown in Fig. 9, an ORTEC 142-A bias-T preamplifier with a 20-mV/MeV gain has been connected between the pixel array and the biasing module. An ORTEC 570 voltage amplifier was connected between the preamplifier and a CANBERRA 8075 12-bit 10-V ADC.

Different bidimensional scans were performed by varying the sensor bias voltage to measure the uniformity in the charge collection efficiency (CCE) and characterize the transition at the boundary between the pixels and the guard ring.

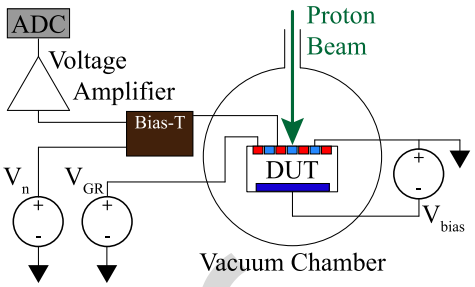


Fig. 9. Schematic of the PM bias and amplification circuits used at the proton microbeam.

The gain of the full readout chain was optimized to maximize the SNR of the output signal. The overall gain, depending on the gain of the different amplification stages, was tuned as follows:

$$G = G_1 \times G_2 = 20\,\frac{\text{mV}}{\text{MeV}} \times 1.5 \times 100\,\frac{\text{mV}}{\text{mV}} = 3\,\frac{\text{V}}{\text{MeV}} \quad (1)$$

where $G_1$ and $G_2$ are, respectively, the gain of the preamplifier and the voltage amplifier.

Considering the beam energy, $E = 2$ MeV, which is fully absorbed within 60 $\mu$m, the following theoretical output voltage is expected:

$$V_{\text{th}} = G \times E \approx 6\ \text{V}. \quad (2)$$

In the measurements, the signal output was acquired as a function of the microbeam position. Maps with 128 × 128 points were acquired in different areas of the sensor, both in the center of the pixel array and near the boundary between the pixels and the guard ring. In the former case, the map can be used to calculate uniformity of the CCE along the array, whereas in the latter case, some information on the spatial resolution of the sensor can be inferred.

The sensor output signal, expressed in ADC counts, is shown in Fig. 10 for two PM structures. To better appreciate the variation of the signal with beam position, the maps have been sliced along and across the sensing electrodes. The results are shown in Fig. 11.

The top plots show the CCE variation between the sensor electrodes and the metal lines. In the uniform regions between two metal lines, the mean value was 6.10 V, in good agreement with the expected one.

In the regions under the metal lines, having a width of 15 and 8 $\mu$m for the PMs with 50- and 25-$\mu$m pitch, respectively, and a thickness of 2.32 $\mu$m, a 2% reduction in the collected charge can be estimated, while simulations predict a reduction of 3.5%. This slight discrepancy is due to the limited width of the metal lines, which does not allow observing a region with uniform response due to the finite spot size.

The bottom plots in Fig. 11, showing the signal along the vertical slices, offer information on charge sharing between the pixels and the guard ring. In the 100-$\mu$m sensor, the signal rises from 10% to 90% in 22 $\mu$m independently of the reverse bias. In the 300-$\mu$m sensor, on the other hand, the width of the

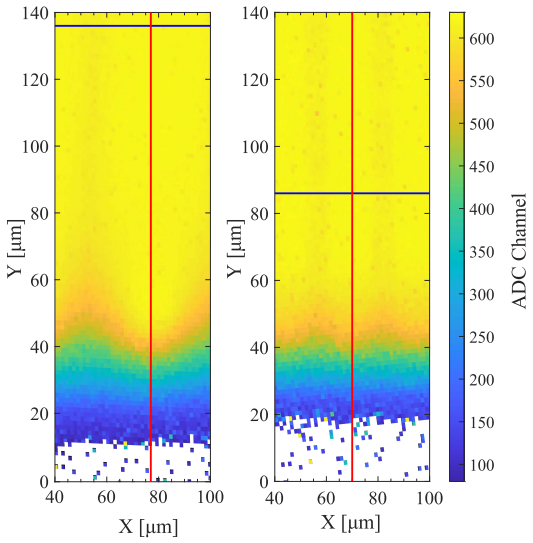


Fig. 10. Microbeam scan of 100 $\mu$m sensor with 50-$\mu$m pixel pitch (left) and 300-$\mu$m sensor with a 25-$\mu$m pixel pitch (right). The microbeam scan step is equal to $\Delta X \approx$ 1.35 $\mu$m. The horizontal cut (blue line) is done across the second electrode from the matrix edge, whereas the vertical cut (red line ) is performed halfway between the metal lines, i.e., along the collecting electrodes.

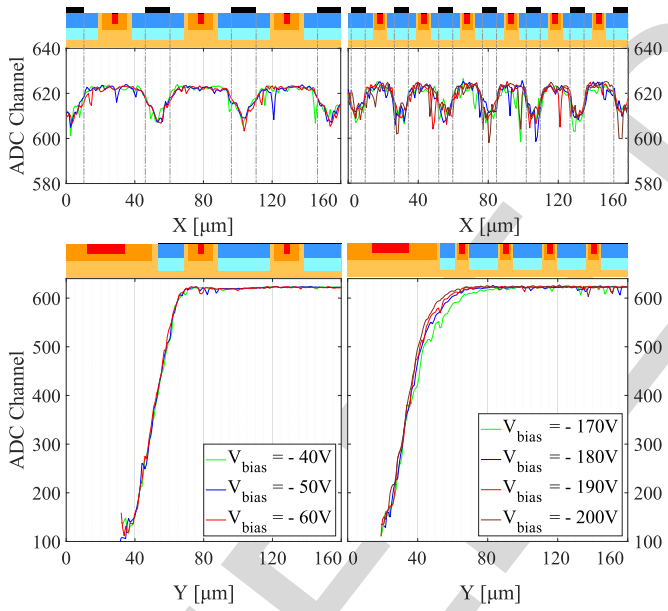


Fig. 11. Signal amplitude profiles at different bias voltages on the 100-$\mu$m (left) and 300-$\mu$m (right) thick sensors. The profiles are shown along (top) and across (bottom) the sensing electrodes in the same location as in Fig. 10.

transition region decreases from 34 to 26 $\mu$m as the reverse bias increases. These results are in good agreement with the simulations in Fig. 5.

### C. Active Pixel Sensor Characterization With $^{55}$Fe Source

A test campaign on the active pixel array with a $^{55}$Fe calibration source was carried out in order to characterize both the sensor and its front-end electronics.

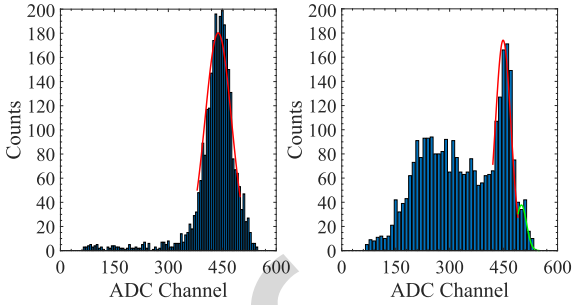


Fig. 12. Reconstructed spectrum of $^{55}$Fe source for all clusters (left) and for seed signals (right) at $V_{\text{bias}} = -200$ V. The fits are superimposed to the distributions.

The reconstructed spectrum of the absorbed photoelectrons was first used to calibrate the pixel response sector by sector. In the following discussion, all data refer to one of the four sectors at $V_{\text{bias}} = -200$ V and for an integration time of 12.8 $\mu$s. This value has been chosen to collect enough statistics in a reasonable amount of time, without increasing the noise contribution, due to the leakage current, too much. Cluster signals were reconstructed by applying a double threshold method on a matrix of $5 \times 5$ pixels selected around a candidate cluster seed. Clusters were requested to have a seed pixel with an SNR, S/N, of at least 6.0 and the neighboring pixels an S/N in excess of 4.0.

In Fig. 12, we show the spectrum of the cluster signals (left) and the one of the seed pixels only (right). The energy peak of the distribution, including all clusters (mean value $\approx$ 439 ADC), was used to calibrate the pixel response. The analog gain of the full readout chain was found to be $\approx$ 124 mV/fC, in good agreement with simulations ($\approx$ 130 mV/fC). The energy resolution [full-width at half-maximum (FWHM)] depends on the cluster multiplicity; it is $\approx$ 1.1 keV when all clusters are included (regardless of their size) and is reduced to $\approx$ 0.7 keV for single-pixel clusters. On the seed value distribution, the peak corresponding to the full charge collection of the 5.9-keV photoelectrons can be recognized at $\approx$ 449 ADC. The charge deficit of $\approx$ 1% with respect to the distribution, including all clusters, puts a lower limit to the CCE of the detector. It is interesting to note that also the peak of the 6.5-keV photons, centered at $\approx$ 500 ADC, can be distinguished. We used the gain information to evaluate the noise performance of the prototype (sensor and electronics). For each pixel, its noise was measured as the rms of the pedestal distribution in dark conditions. The noise distribution for the full matrix is $\approx$ 12 ADC (two ADCs coming from the readout chain: DAQ and readout boards) which, expressed in electrons after the calibration, is shown in Fig. 13. The mean noise value is found to be $\approx$ 40 e$^-$ at room temperature.

In order to study the charge sharing between the pixels in the two configurations, the cluster size and shape were also analyzed, applying both front- and back-side irradiation. The results are shown in Fig. 14, on the left for front illumination and on the right for back illumination. It can be observed, in both cases, how the cluster size is limited to 4 pixels since clusters with a multiplicity larger than 5 are only a small fraction of the total (<1%). This proves how charge

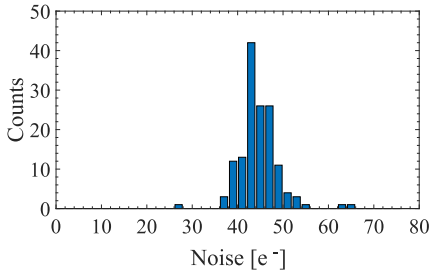


Fig. 13. Noise distribution at room temperature with $V_{bias} = -200$ V and an integration time of 12.8 $\mu$s.

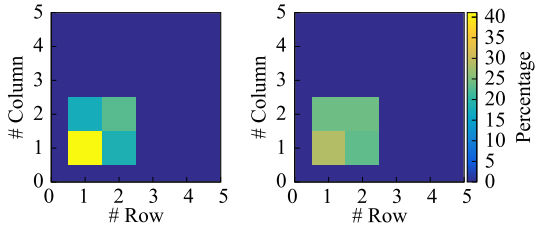


Fig. 14. Cluster size at $V_{bias} = -200$ V in front illumination (left) and in back illumination (right).

sharing is small, and the cluster size is mainly affected by the photon conversion position. In addition, the observation that the cluster size in back illumination is comparable with the one in front illumination confirms that, at the selected voltage, the sensor is FD and charge collection is dominated by the drift mechanism.

## V. Conclusion

In this article, we have demonstrated the feasibility of FD-MAPS in a 110-nm CMOS process. The first experimental results confirm the expected sensor characteristics for a pixel thickness up to 300 $\mu$m and a pixel pitch down to 25 $\mu$m. A large-area active pixel detector is currently under development and will be used to validate the technology in the context of a charged-particle tracking experiment. The interest of the developed process, however, is not limited to charged-particle detection applications. The detection of photons with high penetration depth, i.e., X-ray imaging as well as time-resolved near-infrared imaging, are potentially interesting application scenarios where the proposed technology can be competitive with other state-of-the-art approaches.

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## References

[1] M. Mager, "ALPIDE, the monolithic active pixel sensor for the ALICE ITS upgrade," *Nucl. Instrum. Methods Phys. Res. A, Accel., Spectrometers, Detectors Associated Equip.*, vol. 824, pp. 434–438, Jul. 2016, doi: 10.1016/j.nima.2015.09.057.

[2] C. B. Winderer *et al.*, "The PERCIVAL soft X-ray imager," *J. Instrum.*, vol. 9, no. 3, 2014, Art. no. C03056, doi: 10.1088/1748-0221/9/03/C03056.

[3] I. Perić, "A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology," *Nucl. Instrum. Methods Phys. Res. Sect. A, Accel., Spectrometers, Detectors Associated Equip.*, vol. 582, no. 3, pp. 876–885, Dec. 2007, doi: 10.1016/j.nima.2007.07.115.

[4] T. Wang *et al.*, "Development of a depleted monolithic CMOS sensor in a 150 nm CMOS technology for the ATLAS inner tracker upgrade," *J. Instrum.*, vol. 12, no. 1, 2017, Art. no. C01039, doi: 10.1088/1748-0221/12/01/C01039.

[5] H. Pernegger *et al.*, "First tests of a novel radiation hard CMOS sensor process for depleted monolithic active pixel sensors," *J. Instrum.*, vol. 12, no. 6, 2017, Art. no. P06008, doi: 10.1088/1748-0221/12/06/P06008.

[6] T. Hatsui *et al.*, "A direct-detection X-ray CMOS image sensor with 500 $\mu$m thick high resistivity silicon," in *Proc. Int. Image Sensor Workshop*, Snowbird Resort, UT, USA, Jun. 2013, p. 4.

[7] S. Mattiazzo *et al.*, "IMPACT: An innovative tracker and calorimeter for proton computed tomography," *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 2, no. 4, pp. 345–352, Jul. 2018, doi: 10.1109/TRPMS.2018.2825499.

[8] V. Scotti *et al.*, "The high energy particle detector onboard CSES-02 satellite," in *Proc. 36th Int. Cosmic Ray Conf. (ICRC)*, Madison, WI, USA, Jul./Aug. 2019. AQ:5

[9] W. Snoeys, J. D. Plummer, S. Parker, and C. Kenney, "PIN detector arrays and integrated readout circuitry on high-resistivity float-zone silicon," *IEEE Trans. Electron Devices*, vol. 41, no. 6, pp. 903–912, Jun. 1994, doi: 10.1109/16.293300.

[10] S. Lauxtermann, J. Fisher, and M. McDougal, "A monolithic 640 × 512 CMOS imager with high-NIR sensitivity," *Proc. SPIE*, vol. 9070, Jun. 2014, Art. no. 907002, doi: 10.1117/12.2053449.

[11] M. Asano *et al.*, "Characteristics of non-irradiated and irradiated double SOI integration type pixel sensor," *Nucl. Instrum. Methods Phys. Res. Sect. A, Accel., Spectrometers, Detectors Associated Equip.*, vol. 831, pp. 315–321, Sep. 2016, doi: 10.1016/j.nima.2016.03.095.

[12] L. Pancheri *et al.*, "A 110 nm CMOS process for fully-depleted pixel sensors," *J. Instrum.*, vol. 14, no. 6, 2019, Art. no. C06016, doi: 10.1088/1748-0221/14/06/C06016.

[13] E. J. Olave *et al.*, "MATISSE: A low power front-end electronics for MAPS characterization," in *Proc. Topical Workshop Electron. Part. Phys. PoS(TWEPP)*, Santa Cruz, CA, USA, Mar. 2018, pp. 11–14, doi: 10.22323/1.313.0016.

[14] S. Panati *et al.*, "MATISSE: A versatile readout electronics for monolithic active pixel sensors characterization," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Atlanta, GA, USA, Oct. 2017, pp. 1–4, doi: 10.1109/NSSMIC.2017.8532806.

[15] M. Jakšić *et al.*, "New capabilities of the Zagreb ion microbeam system," *Nucl. Instrum. Methods Phys. Res. Sect. B, Beam Interact. Mater. At.*, vol. 260, no. 1, pp. 114–118, Jul. 2007, doi: 10.1016/j.nimb.2007.01.252.

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# Fully Depleted MAPS in 110-nm CMOS Process With 100–300-$\mu$m Active Substrate

Lucio Pancheri, *Member, IEEE*, Raffaele A. Giampaolo, Andrea Di Salvo, Serena Mattiazzo, Thomas Corradino, Piero Giubilato, Romualdo Santoro, Massimo Caccia, Giovanni Margutti, Jonhatan E. Olave, Manuel Rolo, and Angelo Rivetti

***Abstract*— This article presents a fully depleted monolithic active pixel sensor technology compatible with a standard deep submicrometer 110-nm CMOS process. Passive test pixels structures, produced in various flavors, have proved the feasibility of 100- and 300-$\mu$m-thick active substrates. Active pixel sensors with monolithically integrated analog and digital electronics, consisting of a 24 $\times$ 24 array of pixels with 50-$\mu$m pitch, have been shown to be fully functional when operating in the full depletion mode. Characterization results obtained with a proton microbeam and a $^{55}$Fe radiation source are presented and discussed.**

***Index Terms*— CMOS, monolithic active pixel sensor (MAPS), radiation detector, silicon.**

## I. Introduction

MONOLITHIC active pixel sensors (MAPSs) are emerging as a viable alternative to hybrid pixels in charged-particles' detection and high-energy photons imaging, showing advantages in both performance and overall costs per unit area [1]–[3].

The reconstruction with the highest precision of the perigee parameters of charged-particle trajectories in a dense environment calls for pixel pitches of tens of micrometers, low material budget, a high signal-over-noise ratio, and limited diffusion of the charge carriers originated by the impinging particle. These specifications can be obtained with a monolithic design implemented on a fully depleted (FD) high-resistivity substrate. As a consequence, FD-MAPSs are raising a significant interest in the high-energy physics community [4], [5].

FD-MAPSs have also been proposed for X-ray imaging [6], where an active substrate of 300–500 $\mu$m would enable an efficient detection of photon energies up to 15 keV. Other applications, such as medical particle tomography and tracking in space experiments, would benefit from the low material budget, fine pixel pitch, and low power consumption offered by MAPS sensors [7], [8].

As a general trend in the development of pixel sensors, the complexity of on-chip digital functions is increasing, making it easier to integrate and deploy a complete sensor system. Moreover, event-driven readout schemes are frequently adopted to reduce power consumption and, in turn, relax the requirements of the cooling systems, impacting on the overall system material budget. To these purposes, very scaled process nodes should be used to reduce the area and to increase the speed of on-chip digital electronics.

The latest FD-MAPS design efforts in the high-energy physics community are adopting 180- and 150-nm process nodes. Most of the developments, in this respect, have been devoted to the implementation of devices with a depletion region ranging from a few tens of micrometer and hundreds of micrometer [4], [5]. In [4], large depletion regions are obtained by including the electronics inside a deep n-well that is used as a collection node for the electrons generated by the incident charged particles. This approach has demonstrated an excellent radiation hardness and a fast charge collection, but the sensor capacitance is relatively large, and a nonnegligible part of the pixel area cannot be used to accommodate the readout circuits. Scaling to very small pixels is thus very challenging while using such topology.

An alternative approach, arising from an evolution of the pixels designed for the ALICE detector [1], uses small sensing nodes while implanting a low-doped n-type region below the electronics [5]. In this way, most of the generated charges can be collected by drift, while the area and the capacitance of the sensors are maintained small, granting scalability toward

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small pixel sizes. This approach, although excellent for particle tracking, cannot be easily extended to an active thickness in excess of 100 $\mu$m since the space-charge region extends from the top surface of the sensor, thus limiting the applicable voltage at the sensor top side.

The possibility of FD thick substrates in CMOS-integrated sensors has been first explored in [9], demonstrating an FD sensor with p-type substrate and a n-type backside implantation. In the first prototype, the electronics were made entirely of p-type transistors. A similar approach was adopted in [10], using a CMOS process with n-type substrates and implanting a p+ region on the back.

Full depletion can also be obtained using a silicon-on-insulator process. Although the radiation damage of the insulator oxide poses several challenges related to parameter drift in the transistor characteristics, the latest advancements have greatly improved the radiation hardness of the process, and sensors with depletion regions up to 500 $\mu$m thick have been demonstrated [11].

In this article, we present a technology platform for the implementation of FD MAPS based on a modified 110-nm CMOS process. The process node was chosen to enable the in-pixel implementation of complex digital functions while keeping low prototyping and production costs. Backside processing was used to create a junction on the bottom surface that is biased to deplete the whole sensor substrate.

This article is structured as follows. Section II discusses the simulated characteristics with reference to geometry and process parameters. In Section III, the design of pixel test structures and a small array of active pixels with integrated electronics are presented. Section IV presents the results of the characterization of the arrays compared with the expectations according to the simulation. The perspectives for this technology are highlighted in Section V.

## II. Sensor Concept

The process was developed starting from a 110-nm industrial CMOS with 1.2-V transistors and six metal layers. A few add-ons were necessary to allow for full substrate depletion with electron collection at the sensing electrodes. A concept cross section of the pixel array is shown in Fig. 1 [12].

The standard p-type substrate was replaced with an n-type floating zone material. Wafer thinning and backside lithography were necessary to introduce a junction at the bottom surface, used to bias the substrate to full depletion while maintaining a low voltage at the front side. A shallow boron-doped region was implanted on the rear side of the wafer, and the dopants were activated by laser annealing. Since, at large wafer thicknesses, the voltage needed for sensor full depletion exceeds 150 V, a termination structure composed of multiple guard rings was introduced.

A deep p-well scheme was used to prevent the n-wells hosting p-MOSFETs from collecting the charge generated by radiation in the substrate. Care had to be taken to limit the punchthrough current between the back-side junction and the deep p-well at sensor full depletion. A good control of punchthrough could be obtained either by increasing the bias

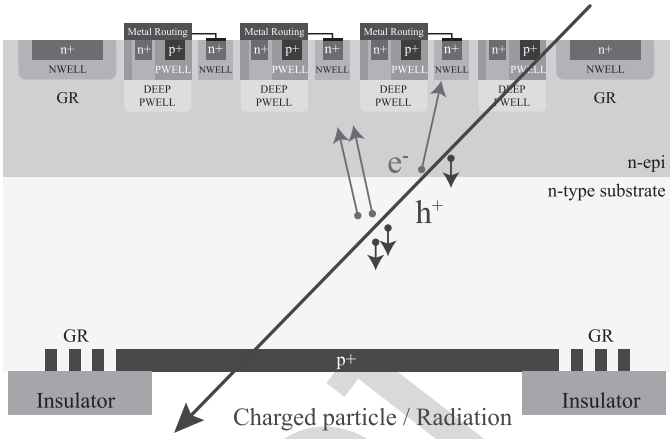


Fig. 1. FD pixel sensor cross section.

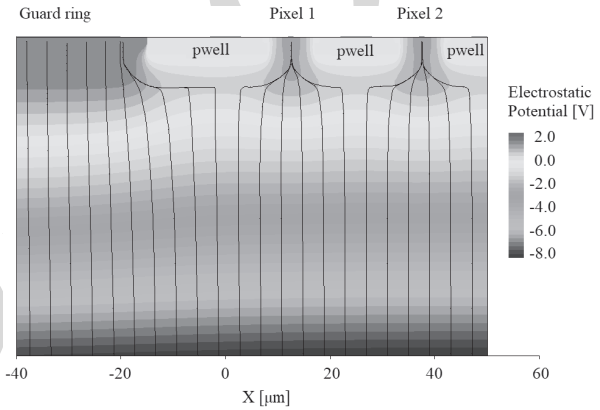


Fig. 2. Simulated 2-D potential profile and electric-field lines at full depletion. The simulation domain includes part of the guard rings and 2 pixels with 25-$\mu$m pitch. Only the sensor surface region is shown.

voltage at the pixel sensor nodes or by increasing the n-dopant concentration below the p-wells. Since the sensors had to be directly coupled to the low-voltage electronics, the second solution was adopted, by adding an n-doped epitaxial layer, having a resistivity lower than the substrate, to the process flow.

TCAD simulations were used to tune the process parameters. The simulated potential profile at full depletion for a domain, including 2 pixels and part of the surface guard ring, is shown in Fig. 2. Electric-field lines are orthogonal to the sensor surface up to the bottom of the deep p-wells, and then, they deviate horizontally toward the collection electrodes.

The full depletion and punchthrough voltages were simulated on this domain by introducing a small unbalance (10 mV) between pixel and guard ring bias voltages. The current flowing at the sensing electrodes and at the backside as a function of applied backside bias is shown in Fig. 3. At low reverse voltage, the substrate is not FD, and resistive paths exist between the pixels and the guard ring, leading to a macroscopic current. As the bias voltage is increased, a sharp current drop is observed, indicating the onset of full depletion. The depletion voltage is reduced by increasing the voltage applied at the front side to the sensor nodes. If the backside voltage is further increased, a punchthrough current starts flowing and

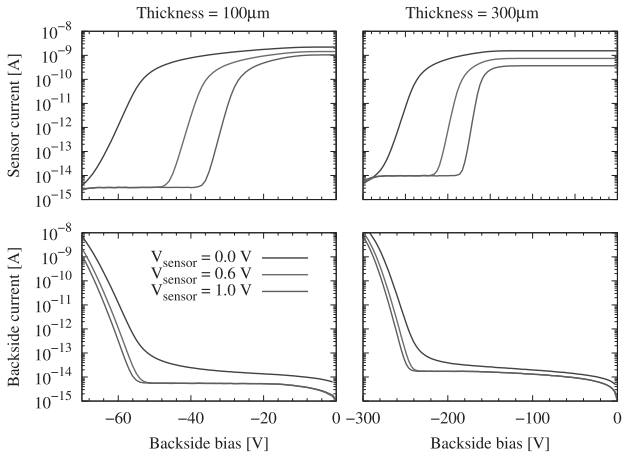


Fig. 3. Simulated sensor and backside current as a function of backside voltage for two values of sensor thickness [100 $\mu$m, (left) and 300 $\mu$m (right)]. Pixel pitch is 25 $\mu$m.

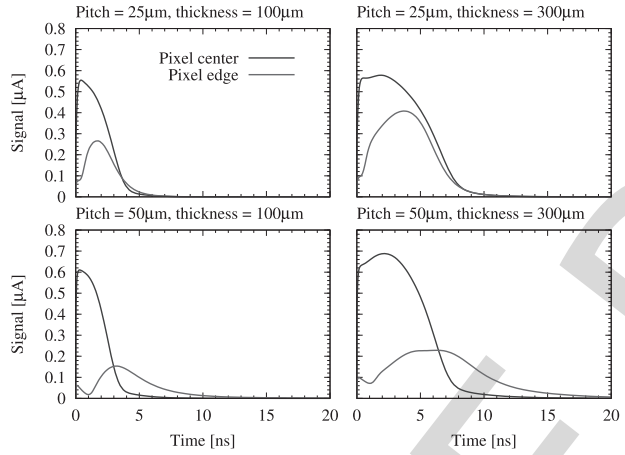


Fig. 4. Simulated transient current signal with an incident MIP for two different values of sensor thickness [100 $\mu$m (left) and 300 $\mu$m (right)] and pixel pitch [25 $\mu$m (top) and 50 $\mu$m (bottom)].

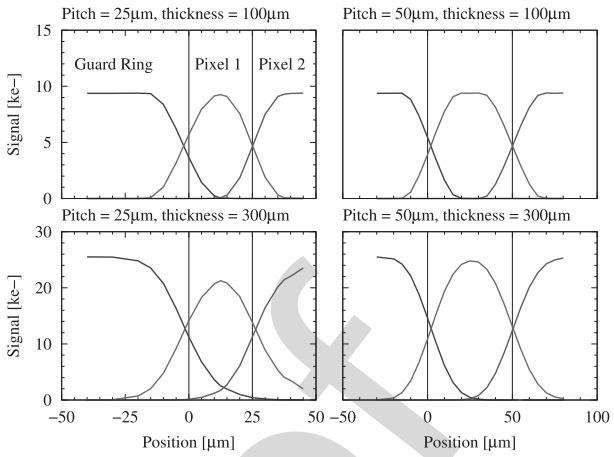


Fig. 5. Simulated collected charge at the sensor periphery as a function of the position of the incident particle for two different values of sensor thickness [100 $\mu$m (top) and 300 $\mu$m (bottom)] and pixel pitch [25 $\mu$m (left) and 50 $\mu$m (right)].

eventually reaches very large values. The voltage difference between breakdown and punchthrough voltages depends on the sensor bias. At a sensor voltage between 0.6 and 1 V that can be applied if the sensor is directly coupled to the electronic readout channels, the difference between full depletion and punchthrough is a fraction of 10%–20% of the applied bias voltage. This value is large enough to reliably accommodate the operation of a pixel array, considered possible doping gradients and nonuniformities between the pixels.

Charge collection dynamics upon the incidence of a minimum ionizing particle (MIP) were also simulated. The MIP was modeled as a continuous charge density of 80 e–h pairs/$\mu$m, orthogonal to the sensor surface and extending throughout the sensor thickness. With reference to the simulation domain shown in Fig. 2, several positions of incidence were considered for the MIP. The current signal generated at the sensor is shown in Fig. 4 for two different MIP incidence positions, two values of pixel pitch (25 and 50 $\mu$m), and two values of sensor thickness (100 and 300 $\mu$m). As expected, complete charge collection is observed in less than 5 and 10 ns, respectively, for 100 and 300 $\mu$m thickness when the MIP is incident in the center of the pixel. If the MIP is incident at the pixel periphery, the collection speed depends on the pixel pitch; at 50-$\mu$m pitch, the collection time approximately doubles since the charge generated in the substrate first reaches the bottom of the deep p-well and then drifts horizontally toward the collection node. Even considering this worst case situation, however, the charge is completely collected within 20 ns. In 25-$\mu$m pixels, on the contrary, the collection time is only slightly degraded, as a result of the smaller horizontal distance traveled by electrons generated at the pixel periphery.

The integrated charge as a function of the MIP incidence position is shown in Fig. 5. Charge sharing between the pixels for two values of thickness and pixel pitch can be observed. As expected, sharing slightly increases by increasing the pixel pitch and sensor thickness, but, in all the cases considered here, the effect is confined to the nearest neighboring pixels.

## III. Active Pixel Array and Test Structures

A 576-active pixel array was designed as a test bench to validate the performance of the proposed technology [13], [14]. The pixels are organized in four sectors, each one consisting of 6 columns of 24 pixels. An end-of-column (EoC) block manages the column logic, handling pixel configuration and controlling data transmission. In this way, each sector works in parallel with the others. To read out the data for a single sector, two clocks are used. The first controls the shift register in the EoC to select the column, whereas the second one is dedicated to the row shift register. In a typical case, they, respectively, work at 5 and 0.2 MHz. Thus, the whole array can be read in less than 30 $\mu$s using a 5-MHz clock.

A single 50-$\mu$m pitch pixel hosts both the electrode and the in-pixel electronics. The sensing electrode, together with a surrounding area clear from electronic circuits, occupies a region of 20 $\mu$m $\times$ 20 $\mu$m, and it is centered in the pixel area. The remaining area is partitioned between the analog front end and the digital logic.

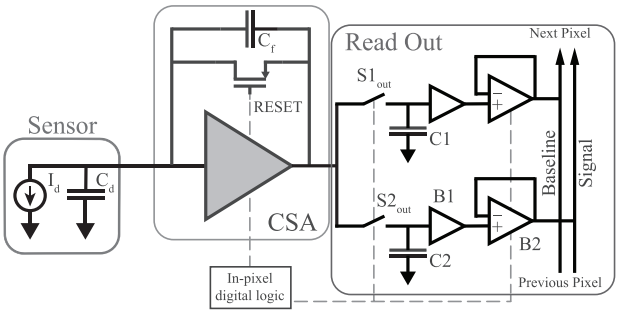


Fig. 6. Pixel readout block scheme.

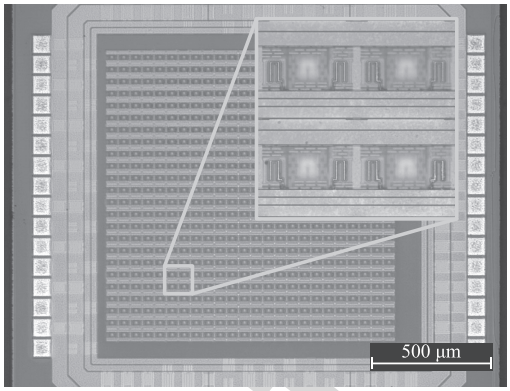


Fig. 7. Micrograph of active pixel array. Inset: close-up of 4 pixels.

The readout chain is shown in Fig. 6. The radiation-generated current signal is amplified by a charge-sensitive amplifier (CSA) circuit. A sample and hold circuitry, designed to perform correlated double sampling (CDS) operation, follows the CSA. Metal–insulator–metal (MIM) capacitors are used to store the signal at this stage. Two analog buffers are included to transmit the analog output signal along the column.

The charge-integrating amplifier, designed to maximize the signal-to-noise ratio (SNR), is based on a telescopic cascode architecture with a feedback capacitor $C_f$ and a minimum-size pMOS reset switch. $C_f$ has been chosen equal to 5.8 fF, giving a postlayout simulation gain of 130 mV/fC. The output dynamic range of the amplifier is defined by considering the expected signal for an MIP in a 300-$\mu$m-thick detector. Thus, for 3.8 fC (corresponding to 80 e–h pairs/ $\mu$m in 300 $\mu$m thickness), the output voltage signal matches the linear output range of the amplifier, which is around 500 mV. This gain also ensures a good SNR for MIPs in substrates with a thickness as low as 50 $\mu$m.

The pixel unit is also equipped with a digital logic to manage data readout and to define the pixel functions. A 3-bit in-pixel register allows to switch OFF defective pixels, enable the injection of a test pulse for the electrical characterization of the readout electronics, and enable the buffer amplifier for data transmission. To study digital noise coupling between the analog and digital sections of the design, each pixel accommodates a digital buffer made by 18 elements, each with a bandwidth of 5 GHz, designed to inject digital noise.

Fig. 7 shows a micrograph of the active pixel array, with a group of 4 pixels in the magnified area. At the center of the pixels, an area free from metal is present to allow the illumination from the top. This feature was included to carry out studies with laser sources.

The pixels were designed for a power consumption around 6 $\mu$W. Providing a power supply of 1.2 V, the power consumption of the pixel array in the static and dynamic conditions is, respectively, 3.84 and 6.4 mW, without considering the contribution of digital and EoC logic.

Small pixel arrays, formed by pixels free from electronic readout circuits, were designed to allow additional flexibility in the experimental evaluation of sensor and process characteristics [12]. In these arrays, these are termed pseudomatrices (PMs) since all the sensing electrodes in the pixels are connected to the same pad, and pixels with both 50- and 25-$\mu$m pitch were included.

TABLE I
PRODUCED SENSOR SAMPLES

| **Sensor type** | **Thickness** [$\mu$m] | **Pixel Pitch** [$\mu$m$^2$] |
|---|---|---|
| Full Sensor | 300 | $50 \times 50$ |
| PM | 100 | $25 \times 25$, $50 \times 50$ |
| PM | 300 | $25 \times 25$, $50 \times 50$ |
| **PM Pixel pitch** [$\mu$m] | **Pseudo-pixels** | **Metal width** [$\mu$m] |
| $25 \times 25$ | $16 \times 18$ | 8 |
| $50 \times 50$ | $8 \times 9$ | 15 |

Two fabrication runs, including both pixel arrays and PM test structures, were produced on high-resistivity wafers ($\rho > 2$ k$\Omega \cdot$ cm) that were thinned to 300 and 100 $\mu$m prior to backside processing. A summary of the devices presented in this article is shown in Table I, highlighting their main geometrical characteristics.

## IV. Experimental Results

An extensive experimental test campaign has been carried out on both the test structures and the active pixel arrays in order to assess their functionality. This section summarizes the most meaningful results, discussed with reference to the simulated characteristics presented in Section II.

### A. Electrical Characterization

Static electrical characterizations have been performed at room temperature on PM structures in order to evaluate full depletion and punchthrough voltages for different pixel sizes, thicknesses, and bias conditions. Current–voltage ($I$–$V$) curves have been measured using a four-channel semiconductor parameter analyzer. In the measurements, the same conditions used for the simulations described in Section II have been applied; the p-wells were biased at 0 V, the sensing nodes and the guard ring were biased between 0 and 1 V, and a negative bias sweep was applied to the backside contact. The measured sensor and backside currents are shown in Fig. 8 as a function of the backside bias voltage for PMs with 25-$\mu$m pitch. While the sensor current is plotted for three different values of sensor voltage, only one curve is shown for the backside current since no dependence on sensor voltage was observed.

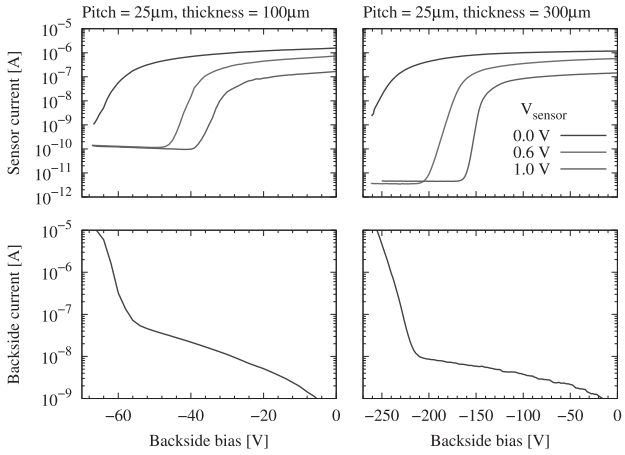


Fig. 8. Measured *I–V* curves for 100 $\mu$m (left) and 300 $\mu$m (right) thick PM sensors. Pixel pitch is 25 $\mu$m.

When compared with the simulated curves in Fig. 3, an excellent agreement was found in both the full depletion and the punchthrough voltage for both the device thicknesses and sensor bias voltages. The simulated and measured currents differ by several orders of magnitude due to the different sizes of the simulation domain (single pixel, 25 $\mu$m $\times$ 1 $\mu$m in 2-D simulations) and PM sensors (400 $\mu$m $\times$ 450 $\mu$m total active area). In the 300-$\mu$m-thick sensors, the measured dark current is more than one order of magnitude smaller than in 100-$\mu$m-thick sensors. Further investigations are going on to understand the origin of this difference, probably due to the different processing conditions. The *I–V* curves measured on pixels with 50-$\mu$m pitch are very similar to the ones shown in Fig. 8.

### *B. Microbeam Sensor Characterization*

The PMs have been tested at the RBI microbeam facility in Zagreb, Croatia [15]. The microbeam has been generated using a 1-MV Tandetron accelerator capable of delivering protons in the 0.5–2.0-MeV range; 2-MeV proton beams with $\sigma_{\text{spot}} \approx 2$ $\mu$m have been focused onto PM structures with different pixel sizes and thickness (see Table I). Protons of this energy have been simulated to have a Bragg peak located at a depth $\lambda \approx 47$ $\mu$m in silicon. As a result, the number of collected carriers and, in turn, the output signal is expected to be independent of the sensor thickness. The proton flux was adjusted to provide a maximum hit rate of 2 kHz.

The DUTs have been wire bonded to a specifically designed PCB equipped with p-i-n connectors to bias the collection electrodes, guard rings, and p-wells. The bias voltages were supplied by a HAMEG HMP2030 power supply, while the high-voltage power supply was an NHQ 202M. As shown in Fig. 9, an ORTEC 142-A bias-T preamplifier with a 20-mV/MeV gain has been connected between the pixel array and the biasing module. An ORTEC 570 voltage amplifier was connected between the preamplifier and a CANBERRA 8075 12-bit 10-V ADC.

Different bidimensional scans were performed by varying the sensor bias voltage to measure the uniformity in the charge

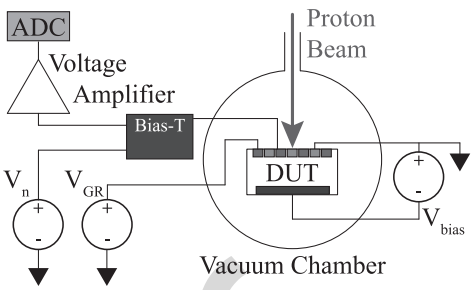


Fig. 9. Schematic of the PM bias and amplification circuits used at the proton microbeam.

collection efficiency (CCE) and characterize the transition at the boundary between the pixels and the guard ring.

The gain of the full readout chain was optimized to maximize the SNR of the output signal. The overall gain, depending on the gain of the different amplification stages, was tuned as follows:

$$G = G_1 \times G_2 = 20\,\frac{\text{mV}}{\text{MeV}} \times 1.5 \times 100\,\frac{\text{mV}}{\text{mV}} = 3\,\frac{\text{V}}{\text{MeV}} \quad (1)$$

where $G_1$ and $G_2$ are, respectively, the gain of the preamplifier and the voltage amplifier.

Considering the beam energy, $E = 2$ MeV, which is fully absorbed within 60 $\mu$m, the following theoretical output voltage is expected:

$$V_{\text{th}} = G \times E \approx 6 \text{ V}. \quad (2)$$

In the measurements, the signal output was acquired as a function of the microbeam position. Maps with 128 $\times$ 128 points were acquired in different areas of the sensor, both in the center of the pixel array and near the boundary between the pixels and the guard ring. In the former case, the map can be used to calculate uniformity of the CCE along the array, whereas in the latter case, some information on the spatial resolution of the sensor can be inferred.

The sensor output signal, expressed in ADC counts, is shown in Fig. 10 for two PM structures. To better appreciate the variation of the signal with beam position, the maps have been sliced along and across the sensing electrodes. The results are shown in Fig. 11.

The top plots show the CCE variation between the sensor electrodes and the metal lines. In the uniform regions between two metal lines, the mean value was 6.10 V, in good agreement with the expected one.

In the regions under the metal lines, having a width of 15 and 8 $\mu$m for the PMs with 50- and 25-$\mu$m pitch, respectively, and a thickness of 2.32 $\mu$m, a 2% reduction in the collected charge can be estimated, while simulations predict a reduction of 3.5%. This slight discrepancy is due to the limited width of the metal lines, which does not allow observing a region with uniform response due to the finite spot size.

The bottom plots in Fig. 11, showing the signal along the vertical slices, offer information on charge sharing between the pixels and the guard ring. In the 100-$\mu$m sensor, the signal rises from 10% to 90% in 22 $\mu$m independently of the reverse bias. In the 300-$\mu$m sensor, on the other hand, the width of the

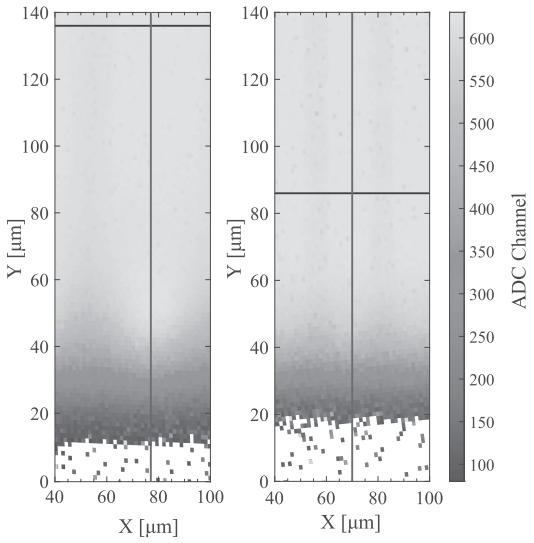


Fig. 10. Microbeam scan of 100 $\mu$m sensor with 50-$\mu$m pixel pitch (left) and 300-$\mu$m sensor with a 25-$\mu$m pixel pitch (right). The microbeam scan step is equal to $\Delta X \approx$ 1.35 $\mu$m. The horizontal cut (blue line) is done across the second electrode from the matrix edge, whereas the vertical cut (red line ) is performed halfway between the metal lines, i.e., along the collecting electrodes.

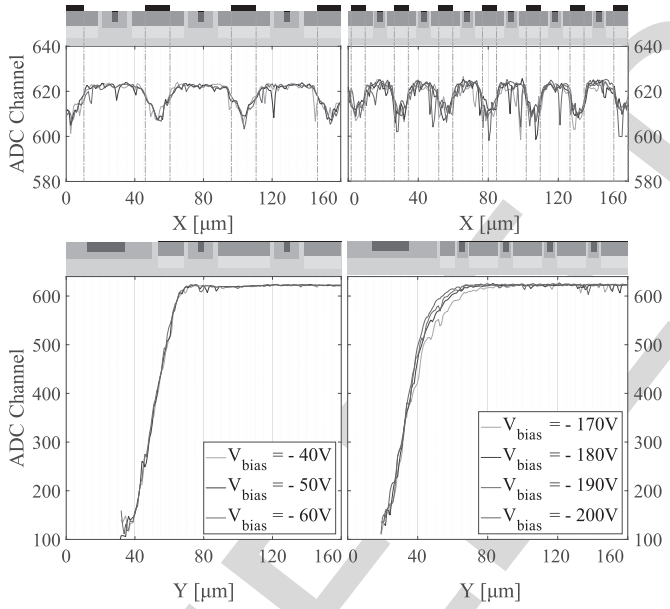


Fig. 11. Signal amplitude profiles at different bias voltages on the 100-$\mu$m (left) and 300-$\mu$m (right) thick sensors. The profiles are shown along (top) and across (bottom) the sensing electrodes in the same location as in Fig. 10.

transition region decreases from 34 to 26 $\mu$m as the reverse bias increases. These results are in good agreement with the simulations in Fig. 5.

### C. Active Pixel Sensor Characterization With $^{55}$Fe Source

A test campaign on the active pixel array with a $^{55}$Fe calibration source was carried out in order to characterize both the sensor and its front-end electronics.

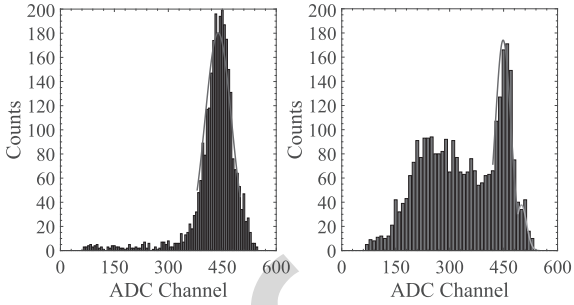


Fig. 12. Reconstructed spectrum of $^{55}$Fe source for all clusters (left) and for seed signals (right) at $V_{\text{bias}} = -200$ V. The fits are superimposed to the distributions.

The reconstructed spectrum of the absorbed photoelectrons was first used to calibrate the pixel response sector by sector. In the following discussion, all data refer to one of the four sectors at $V_{\text{bias}} = -200$ V and for an integration time of 12.8 $\mu$s. This value has been chosen to collect enough statistics in a reasonable amount of time, without increasing the noise contribution, due to the leakage current, too much. Cluster signals were reconstructed by applying a double threshold method on a matrix of $5 \times 5$ pixels selected around a candidate cluster seed. Clusters were requested to have a seed pixel with an SNR, S/N, of at least 6.0 and the neighboring pixels an S/N in excess of 4.0.

In Fig. 12, we show the spectrum of the cluster signals (left) and the one of the seed pixels only (right). The energy peak of the distribution, including all clusters (mean value $\approx$ 439 ADC), was used to calibrate the pixel response. The analog gain of the full readout chain was found to be $\approx$ 124 mV/fC, in good agreement with simulations ($\approx$ 130 mV/fC). The energy resolution [full-width at half-maximum (FWHM)] depends on the cluster multiplicity; it is $\approx$ 1.1 keV when all clusters are included (regardless of their size) and is reduced to $\approx$ 0.7 keV for single-pixel clusters. On the seed value distribution, the peak corresponding to the full charge collection of the 5.9-keV photoelectrons can be recognized at $\approx$ 449 ADC. The charge deficit of $\approx$ 1% with respect to the distribution, including all clusters, puts a lower limit to the CCE of the detector. It is interesting to note that also the peak of the 6.5-keV photons, centered at $\approx$ 500 ADC, can be distinguished. We used the gain information to evaluate the noise performance of the prototype (sensor and electronics). For each pixel, its noise was measured as the rms of the pedestal distribution in dark conditions. The noise distribution for the full matrix is $\approx$ 12 ADC (two ADCs coming from the readout chain: DAQ and readout boards) which, expressed in electrons after the calibration, is shown in Fig. 13. The mean noise value is found to be $\approx$ 40 e$^-$ at room temperature.

In order to study the charge sharing between the pixels in the two configurations, the cluster size and shape were also analyzed, applying both front- and back-side irradiation. The results are shown in Fig. 14, on the left for front illumination and on the right for back illumination. It can be observed, in both cases, how the cluster size is limited to 4 pixels since clusters with a multiplicity larger than 5 are only a small fraction of the total (<1%). This proves how charge

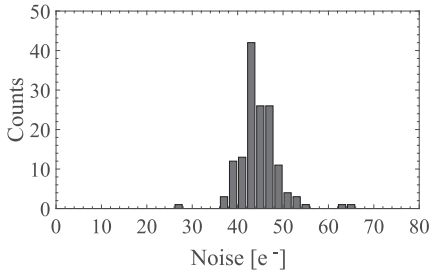


Fig. 13. Noise distribution at room temperature with $V_{bias} = -200$ V and an integration time of 12.8 $\mu$s.

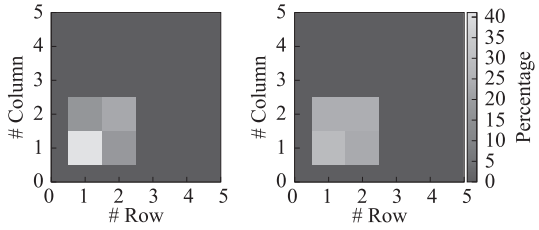


Fig. 14. Cluster size at $V_{bias} = -200$ V in front illumination (left) and in back illumination (right).

sharing is small, and the cluster size is mainly affected by the photon conversion position. In addition, the observation that the cluster size in back illumination is comparable with the one in front illumination confirms that, at the selected voltage, the sensor is FD and charge collection is dominated by the drift mechanism.

## V. Conclusion

In this article, we have demonstrated the feasibility of FD-MAPS in a 110-nm CMOS process. The first experimental results confirm the expected sensor characteristics for a pixel thickness up to 300 $\mu$m and a pixel pitch down to 25 $\mu$m. A large-area active pixel detector is currently under development and will be used to validate the technology in the context of a charged-particle tracking experiment. The interest of the developed process, however, is not limited to charged-particle detection applications. The detection of photons with high penetration depth, i.e., X-ray imaging as well as time-resolved near-infrared imaging, are potentially interesting application scenarios where the proposed technology can be competitive with other state-of-the-art approaches.

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## References

[1] M. Mager, "ALPIDE, the monolithic active pixel sensor for the ALICE ITS upgrade," *Nucl. Instrum. Methods Phys. Res. A, Accel., Spectrometers, Detectors Associated Equip.*, vol. 824, pp. 434–438, Jul. 2016, doi: 10.1016/j.nima.2015.09.057.

[2] C. B. Winderer *et al.*, "The PERCIVAL soft X-ray imager," *J. Instrum.*, vol. 9, no. 3, 2014, Art. no. C03056, doi: 10.1088/1748-0221/9/03/C03056.

[3] I. Perić, "A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology," *Nucl. Instrum. Methods Phys. Res. Sect. A, Accel., Spectrometers, Detectors Associated Equip.*, vol. 582, no. 3, pp. 876–885, Dec. 2007, doi: 10.1016/j.nima.2007.07.115.

[4] T. Wang *et al.*, "Development of a depleted monolithic CMOS sensor in a 150 nm CMOS technology for the ATLAS inner tracker upgrade," *J. Instrum.*, vol. 12, no. 1, 2017, Art. no. C01039, doi: 10.1088/1748-0221/12/01/C01039.

[5] H. Pernegger *et al.*, "First tests of a novel radiation hard CMOS sensor process for depleted monolithic active pixel sensors," *J. Instrum.*, vol. 12, no. 6, 2017, Art. no. P06008, doi: 10.1088/1748-0221/12/06/P06008.

[6] T. Hatsui *et al.*, "A direct-detection X-ray CMOS image sensor with 500 $\mu$m thick high resistivity silicon," in *Proc. Int. Image Sensor Workshop*, Snowbird Resort, UT, USA, Jun. 2013, p. 4.

[7] S. Mattiazzo *et al.*, "IMPACT: An innovative tracker and calorimeter for proton computed tomography," *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 2, no. 4, pp. 345–352, Jul. 2018, doi: 10.1109/TRPMS.2018.2825499.

[8] V. Scotti *et al.*, "The high energy particle detector onboard CSES-02 satellite," in *Proc. 36th Int. Cosmic Ray Conf. (ICRC)*, Madison, WI, USA, Jul./Aug. 2019. AQ:5

[9] W. Snoeys, J. D. Plummer, S. Parker, and C. Kenney, "PIN detector arrays and integrated readout circuitry on high-resistivity float-zone silicon," *IEEE Trans. Electron Devices*, vol. 41, no. 6, pp. 903–912, Jun. 1994, doi: 10.1109/16.293300.

[10] S. Lauxtermann, J. Fisher, and M. McDougal, "A monolithic 640 × 512 CMOS imager with high-NIR sensitivity," *Proc. SPIE*, vol. 9070, Jun. 2014, Art. no. 907002, doi: 10.1117/12.2053449.

[11] M. Asano *et al.*, "Characteristics of non-irradiated and irradiated double SOI integration type pixel sensor," *Nucl. Instrum. Methods Phys. Res. Sect. A, Accel., Spectrometers, Detectors Associated Equip.*, vol. 831, pp. 315–321, Sep. 2016, doi: 10.1016/j.nima.2016.03.095.

[12] L. Pancheri *et al.*, "A 110 nm CMOS process for fully-depleted pixel sensors," *J. Instrum.*, vol. 14, no. 6, 2019, Art. no. C06016, doi: 10.1088/1748-0221/14/06/C06016.

[13] E. J. Olave *et al.*, "MATISSE: A low power front-end electronics for MAPS characterization," in *Proc. Topical Workshop Electron. Part. Phys. PoS(TWEPP)*, Santa Cruz, CA, USA, Mar. 2018, pp. 11–14, doi: 10.22323/1.313.0016.

[14] S. Panati *et al.*, "MATISSE: A versatile readout electronics for monolithic active pixel sensors characterization," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Atlanta, GA, USA, Oct. 2017, pp. 1–4, doi: 10.1109/NSSMIC.2017.8532806.

[15] M. Jakšić *et al.*, "New capabilities of the Zagreb ion microbeam system," *Nucl. Instrum. Methods Phys. Res. Sect. B, Beam Interact. Mater. At.*, vol. 260, no. 1, pp. 114–118, Jul. 2007, doi: 10.1016/j.nimb.2007.01.252.