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Study of High-k Dielectrics and their Interfaces on Semiconductors for Device Applications

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Abstract

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This thesis has focused on two emerging applications of high-*k* dielectrics in Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) and in Metal-Insulator-Semiconductor High Electron Mobility Transistors (MIS-HEMTs). The key aim has been to propose the best routes for passivation of semiconductor/high-*k* oxide interfaces by investigating the band alignments and interface properties of several oxides, such as Tm_2O_3, Ta_2O_5, ZrO_2, Al_2O_3 and MgO, deposited on different semiconductors: Si, Ge, GaN, InGaAs and InGaSb. The electrical characterisation of fabricated MIS capacitor and (MIS)-HEMT devices have also been performed.

Thulium silicate (TmSiO) has been identified as a promising candidate for integration as interfacial layer (IL) in HfO_2/TiN MOSFETs. The physical properties of Tm_2O_3/IL/Si interface have been elucidated, where IL (TmSiO) has been formed using different post-deposition annealing (PDA) temperatures, from 550 to 750 °C. It has been found that the best-scaled stack (sub-nm IL) is formed at 550 °C PDA with a graded interface layer and a strong SiO_x (Si 3+) component. A large valence band offset (VBO) of 2.8 eV and a large conduction band offset (CBO) of 1.9 eV have been derived for Tm_2O_3/Si by X-ray photoelectron spectroscopy (XPS) and variable angle spectroscopic ellipsometry.

Further increase of device performance can be achieved by replacing Si with GaN for high frequency, high power and high-temperature operation. In this thesis, several GaN cleaning procedures have been considered: 30% NH_4OH, 20% $(NH_4)_2S$, and 37% HCl. It has been found that the HCl treatment shows the lowest oxygen contamination and Ga-rich surface, and hence has been used prior sputtering of Ta_2O_5, Al_2O_3, ZrO_2 and MgO on GaN. The large VBOs of 1.1 eV and 1.2 eV have been derived for Al_2O_3 and MgO on GaN respectively, using XPS and Kraut's method; the corresponding CBOs are 2.0 eV and 2.8 eV respectively, taking into account the band gaps of Al_2O_3 (6.5 eV) and MgO (7.4 eV) determined from XPS O 1s electron energy spectra. The lowest leakage currents were obtained for devices with Al_2O_3 and MgO, i.e. 5.3×10^{-6} A/cm^2 and 3.2×10^{-6} A/cm^2 at 1 V, respectively in agreement with high band offsets (> 1 eV). Furthermore, the effect of different surface treatments (HCl, O_2 plasma and 1-Octadecanethiol (ODT)) prior to atomic layer deposition of Al_2O_3 on the GaN/AlGaN/GaN heterostructure has been investigated. The MIS-HEMTs fabricated using the low-cost ODT GaN surface treatment have been found to exhibit superior performance for power switching applications such as a low threshold voltage, V_T of -12.3 V, hysteresis of 0.12 V, a small subthreshold voltage slope (*SS)* of 73 mV/dec, and a low density of interface states, D_{it} of 3.0×10^{12} cm^{-2}eV^{-1}.

A comprehensive novel study of HfO_2/InGaAs and Al_2O_3/InGaSb interfaces have also been conducted for use in III-V based MOSFETs. The addition of the plasma H_2/TMA/H_2 pre-cleaning has been found to be very effective in recovering etch damage on InGaAs, especially for (110) orientation, and led to the improvement of electrical characteristics. Furthermore, the combination of H_2 plasma exposure and forming gas anneal yielded significantly improved metrics for Al_2O_3/InGaSb over the control HCl-treated sample, with the 150 W plasma treatment giving both the highest capacitance and the lowest stretch out.

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Contribution from this work

Journals and conferences proceeding

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Abbreviations

AFM – Atomic force microscopy

Al – Aluminium

AlGaN – Aluminium gallium nitride

AlN – Aluminium nitride

Al_2O_3 – Aluminium oxide

AlO_x – aluminium oxide

ALD – Atomic layer deposition

Ar – Argon

BB – Band bending

BE – Binding energy

C – Capacitance

CB – Conduction band

CBO – Conduction band offset

CeO_2 – Cerium oxide

CET – Capacitance equivalent thickness

CL – Core level

CMOS – Complementary metal oxide semiconductor

CV – Capacitance-voltage

DC – Direct current

D-mode – Depletion-mode

E-mode – Enhancement-mode

DI – Deionised

DT – Direct tunnelling

EELs – Electron energy-loss spectroscopy

EOT – Equivalent oxide thickness

EWF – effective workfunction

FGA – forming gas anneal

FN – Fowler-Nordheim

FWHM – Full width at half maximum

GaAs – Gallium arsenide

GaN – Gallium nitride

GaSb – Gallium antimonide

Gd_2O_3 – Gadolinium oxide

Ge – Germanium

GeO_2 – Germanium dioxide

GeO_x – Germanium oxide

HCl – Hydrochloric acid

HF – Hydrofluoric acid

HfO_2 – Hafnium oxide

H_2O_2 – Hydrogen peroxide

HRTEM – High-resolution transmission electron microscopy

H_2SO_4 – Sulfuric acid

I – Current

IC – Integrated circuits

InGaAs – Indium gallium arsenide

IL – Interfacial layer

ITRS – International technology roadmap for semiconductors

InGaSb – Indium gallium arsenide

IV – Current-voltage

JV – Current density-voltage

KE – Kinetic energy

KK – Kramers-Kronig

La_2O_3 – Lanthanum oxide

MBE – Molecular beam epitaxy

MgO – Magnesium oxide

MISFET – Metal-insulator-semiconductor field effect transistor

MOSFET – Metal-oxide-semiconductor field effect transistor

MSE – Mean standard error

N – Nitrogen

NH_3 – Ammonia

ODT – 1-octadecanethiol

PDA – Post deposition annealing

PF – Poole-Frenkel

R – Resistance

RE – Rare-earth

RF – Radio frequency

RMS – Root mean square

RT – Room temperature

SAM – self-assembled monolayer

SCE – Short-channel effect

SCLC – Space-charge limited current

Si – Silicon

SiC – Silicon carbide

Si_3N_4 – Silicon nitride

SiON – Silicon oxynitride

Ta – Tantalum

Ta_2O_5 – Tantalum oxide

TiO_2 – Titanium oxide

TMA – Try-methyl-aluminium

Tm – Thulium

Tm_2O_3 – Thulium oxide

TmSiO – Thulium silicate

UV – Ultraviolet

VASE – Variable angle spectroscopic Ellipsometry

VB – Valence band

VBM – Valence band maximum

VBO – Valence band offset

WBG – Wide band gap

XPS – X-ray photoelectron spectroscopy

XRD – X-ray diffraction

Y_2O_3 – Yttrium oxide

ZrO_2 – Zirconium oxide

CHAPTER 1

Introduction

1.1 CMOS technology

The complementary metal-oxide-semiconductor (CMOS) field-effect transistor (FET) made from silicon is the important electronic device among other devices such as resistor and capacitor devices, diodes, and bipolar junction transistors. Si has been the dominant semiconductor material since the middle 1960s. One of the reasons is due to the excellent properties of silicon dioxide which can be formed easily on Si by thermal oxidation. Moreover, SiO_2 has the large band gap of ~9 eV and provides large conduction and valence band offsets with Si. In addition, SiO_2 has an amorphous structure with very few electronic defects and forms an excellent, abrupt interface with Si. Besides, Si-based metal-oxide-semiconductor field effect transistor (MOSFET) technology has arisen because of its low power consumption and its continuing performance improvement over 50 years following Moore's Law of scaling. Moore's law first stated by Gordon Moore in 1965 predicts that the number of devices on an integrated circuit increases exponentially, doubling every 2–3 years [1] as illustrated in Figure 1.1. The basic idea of device scaling is to reduce the dimensions of electronic devices to allow the integration of a greater number of transistors on a chip and enable higher speed of integrated circuits with decreasing the cost and power consumption per unit function.

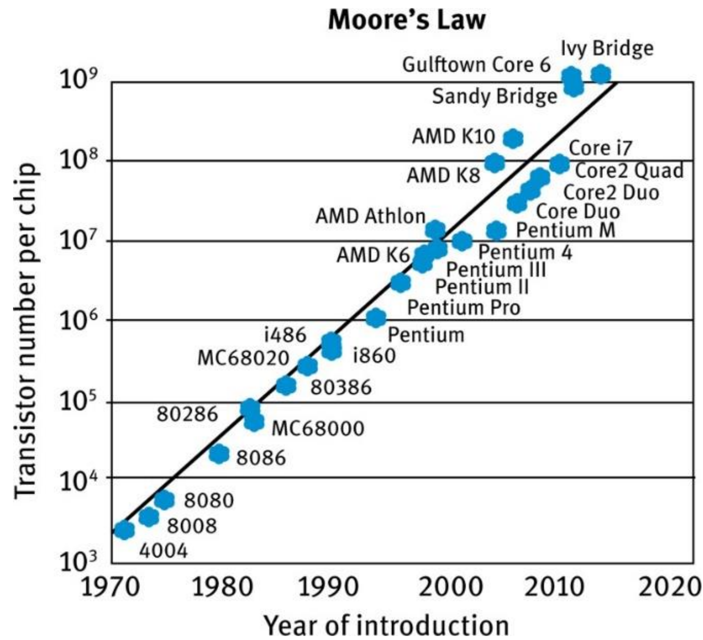

Figure 1.1: The number of transistors per chip increases exponentially as predicted by Moore's law [2].

However, besides all mentioned advantages, the aggressive scaling of the gate oxide thickness of MOSFETs became increasingly difficult as the conventional SiO_2 approached its fundamental limit. Reducing the gate dielectric thickness of SiO_2 below 2 nm exhibits an unacceptable large leakage current due to direct tunnelling of electrons through the SiO_2 layer leading to excessive power dissipation and limits the device performance and reliability [3], [4]. The problem of leakage current can be mitigated with the introduction of high dielectric constant (high-*k*) materials to replace SiO_2. Theoretically, tunnelling currents decrease exponentially with increasing distance. Hence, the solution to the tunnelling problem is to replace SiO_2 with a physically thicker layer of new material of higher *k*, which will keep the same capacitance and can reduce the leakage current as illustrated in Figure 1.2. A FET is a capacitance-operated device, where the FET source-drain current depends on the gate capacitance, which can be expressed as Equation (1.1):

$$C = \frac{\varepsilon_0 k A}{t} , \tag{1.1}$$

where ε_0 is the permittivity of free space, k is the relative dielectric constant, A is the area, and t is the oxide thickness.

It is good to define an electrical thickness of new oxide in terms of its equivalent oxide thickness (EOT) which can be defined as the equivalent SiO_2 thickness which would provide the same gate capacitance as the actual high-k dielectric. The relation between EOT and the thickness of the high-k layer is expressed in Equation (1.2):

$$EOT = \frac{k_{SiO_2}}{k_{high-k}} \; t_{high-k}, \tag{1.2}$$

where k_{SiO_2} and k_{high-k} are the dielectric constants of SiO_2 and high-k dielectric, respectively. t_{high-k} is the physical thickness of the high-k dielectric. The static dielectric constant of SiO_2, k_{SiO_2} is equal to 3.9. Usually, the gate dielectric consists of several layers, e.g. a lower-k interfacial layer and a higher-k layer. In terms of EOT, the series capacitance can be written as:

$$EOT_{total} = EOT_{high-k} + \sum EOT_{low-k}, \tag{1.3}$$

Any low-k interfacial layer contributes to the overall EOT value and thus should be minimised to achieve as low an EOT as required.

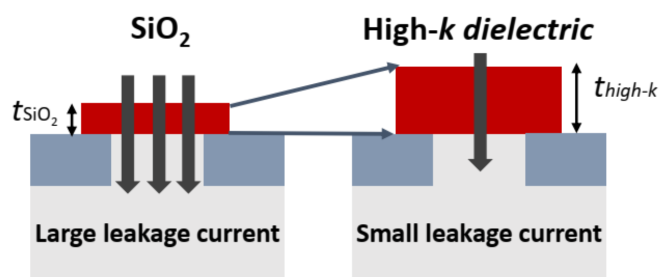

Figure 1.2: Reduction of the tunnel leakage current by replacing SiO_2 with a high-k gate dielectric.

1.1.1 High-*k* dielectric material

Generally, the high-*k* dielectric can be defined as those with a relative dielectric constant greater than about 9 and refer to a class of simple binary and ternary metal oxide insulators, including transition metals from groups III–V, the lanthanides and aluminium [5]. The selection of high-*k* materials primarily needs to meet a few key requirements of the International Technology Roadmap for Semiconductors (ITRS) to be identified as a potential candidate to replace SiO_2 as a gate dielectric [6]. The requirements of a new oxide are six-fold [4], [7], [8] as mentioned below.

One of the key requirements is a dielectric constant, *k* value which must be sufficiently large enough (should be over 12, or preferably 25-35) to be used economically for a reasonable number of scaling nodes. However, there is a trade-off between *k* value and band gap as shown in Figure 1.3, where an oxide's *k* value tends to vary inversely with its band gap. In this case, a relatively low *k* value should be accepted because a very large *k* value will provide a large electric field along the channel edges and hence will damage short-channel performance [9]. In detail, if the *k* value is too high, the physical thickness of the gate dielectric becomes comparable to the channel length. Then, the percentage of field lines originating from bottom of the gate electrode and terminating on the source/drain regions increases compared to the field lines terminating on the channel. These field lines finally induce an electric field from source to channel thereby reducing the source to channel barrier height. Also, a weaker coupling between gate and channel due to fringing, increases the control of drain on the source to channel barrier height. This phenomenon is generally known as fringing induced barrier lowering (FIBL). The reduction of channel length further increases the physical dielectric thickness to the channel length ratio leading to poor short channel performance.

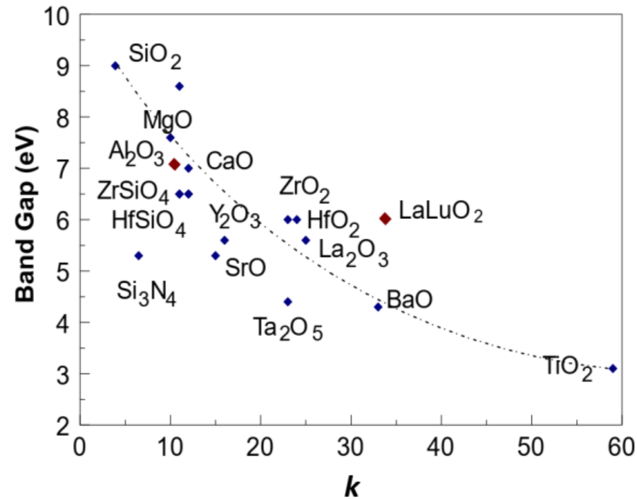

Figure 1.3: The trade-off between the dielectric constant and band gap, which limits the choice of gate oxides [8].

The second requirement is also crucial to ensure that the chosen oxide is thermodynamically stable as it is in direct contact with the semiconductor, i.e. the oxide must not react with Si to form either SiO_2 or a silicide, where SiO_2 layer increases the EOT while silicides are metallic which could short circuit the channel [10], [11].

The third requirement is that the oxide must act as an insulator, by having sufficiently large band offsets, conduction band offset (CBO) and valence band offset (VBO) of at least 1 eV. Robertson *et al*. [10], [12], [13] reported that a band offset of over about 1 eV is needed to minimise the injection by the Schottky emission of the carriers into the oxide bands that cause unacceptably high leakage currents. For example, the band gap of SiO_2 is 9 eV, so it has high barriers for both electrons and holes where the conduction and valence band offsets with Si are 3.1 eV and 4.8 eV, respectively. However, if the oxide has a narrower band gap like $SrTiO_3$ which is only 3.3 eV, its bands must be aligned almost symmetrically with respect to those of Si for both barriers to be over 1 eV. The oxides with a band gap larger than 5 eV that satisfy

this requirement are Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3, and various lanthanides, and their silicates and aluminates [12].

The fourth requirement is kinetic stability, meaning that the oxide must be processed at the dopant activation anneal of 1000 ^{o}C for at least 5 seconds in the gate-first process [10]. In practice, most of the amorphous oxides such as HfO_2, ZrO_2, TiO_2, and rare-earth (RE) oxides crystallise at lower temperatures, unlike SiO_2 and Al_2O_3. It is preferable that the gate dielectrics remain amorphous after annealing because grain boundaries may serve as the paths of dopant diffusion and result in a variation of the electrical properties [14]. Therefore, it is important to mitigate this problem by alloying the high-*k* oxide with either SiO_2, Al_2O_3, a silicate, or an aluminate [15], [16] or introducing nitrogen as it lowers diffusion rates and raises crystallisation temperatures [17].

The fifth condition refers to an alternative gate dielectric to form a good quality interface with Si in terms of low roughness and absence of defects in order to prevent scattering of carriers. The interface between Si and the high-*k* oxide always has a SiO_2-rich interfacial layer; it is not an abrupt interface. This allows for lower interfacial defect densities to exist in practice.

Finally, the dielectric must have few electrically active defects. Electrically active defects relate to the atomic configurations which give electronic states in the oxide band gap which can then trap carriers. Typically, these are sites of excess or deficit of oxygen or impurities. These unwanted defects will result into several major problems [10]: 1) the trapped charges in defects shift the gate threshold voltage, V_T of the transistor; 2) the trapped charge changes with time so V_T shifts with time, leading to instability of operating characteristics; 3) trapped charge scatters carriers in the

channel and lowers the carrier mobility; and 4) defects cause unreliability; they are the starting point for electrical failure and oxide breakdown.

Therefore, it is important to meet all mentioned criteria for selecting a high-k gate dielectric material as a potentially promising candidate for CMOS technology applications.

1.1.2 MOSFET operation

The MOSFET has become the most important device for advanced integrated circuits, particularly microprocessors and semiconductor memories. The heart of the MOSFET is a metal-oxide-semiconductor structure known as a MOS capacitor as shown in Figure 1.4 (a). The energy bands in the semiconductor interface bend as a voltage is applied across the MOS capacitor. The position of the conduction band (E_c) and valence band (E_v) relative to the Fermi level (E_F) at the oxide-semiconductor interface is a function of the MOS capacitor voltage so that the characteristics of the semiconductor surface can be inverted from p-type to n-type, or from n-type to p-type, by applying the proper voltage.

There are three different modes of operation: accumulation, depletion and inversion. In the case of the p-type substrate, the accumulation region (Figure 1.4 (b)) occurs when the negative voltage ($V_G < 0$ V) is applied to the metal electrode and attracts positively charged holes from the substrate to the oxide-semiconductor interface to satisfy the need for charge neutrality. However, by applying a small positive voltage ($V_G > 0$ V) will force holes away from the surface leaving a depletion region shown in Figure 1.4 (c), where the semiconductor provides the necessary negative charge, with negative acceptor ions. The voltage is dropped across the semiconductor and the potential at the oxide-semiconductor interface is referred to as

the surface potential, $\emptyset_s$, where for depletion: $0 < \emptyset_s < 2\,\emptyset_F$. If a sufficiently large positive voltage ($V_G > 0$ V) is applied, the energy bands are bent sufficiently to approach the Fermi level, and this predicts that the electron concentration is increasing which form a so-called inversion region (Figure 1.4 (d)), where the negative charge on that plate of the capacitor is made up of two components: inversion (electrons) and depletion (acceptors) charge. Further increase of voltage, will be satisfied by an increase in the inversion component and the depletion width remains about the constant in width. This condition provides the surface potential equal to twice the Fermi potential ($\emptyset_s = 2\,\emptyset_F$), where the minority carrier (electron) concentration at the surface is equal to the majority carrier (hole) concentration in the semiconductor bulk. The operation and characteristics of the MOSFET are dependent on this inversion and the creation of an inversion charge density at the semiconductor surface. The threshold voltage is defined as the applied gate voltage required to create the inversion charge and is one of the important parameters of the MOSFET.

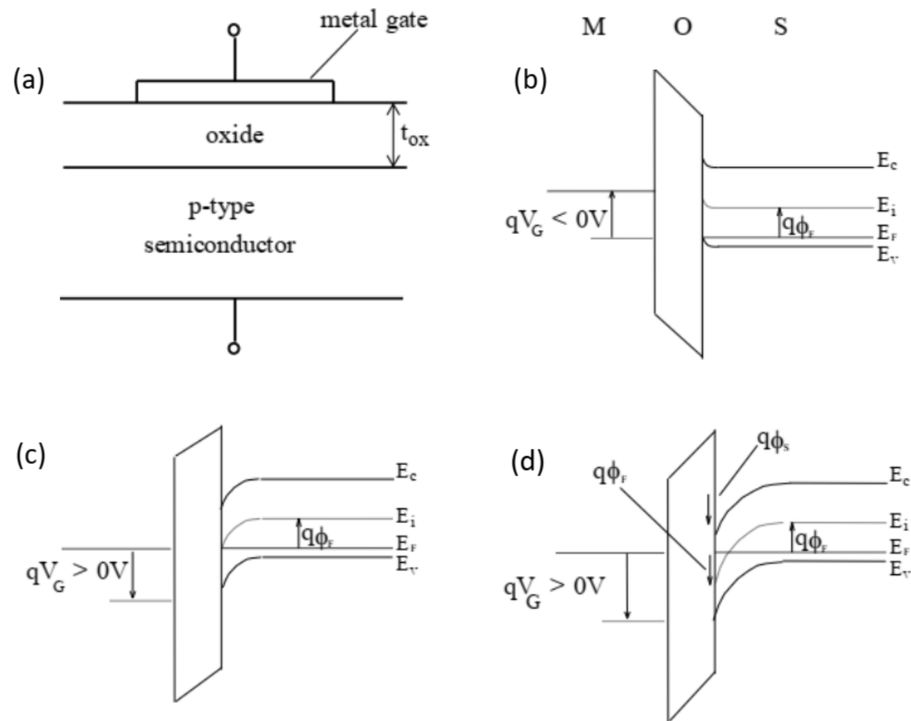

Figure 1.4: (a) p-type MOS-capacitor, (b) accumulation condition, (c) depletion condition and (d) depletion and inversion condition (electron channel forming) [18].

The basic structure of MOSFET consists of four terminals: source, gate, drain, and body terminals, as illustrated in Figure 1.5. The body (or substrate) of the MOSFET often is connected to the source terminal, making it three terminal devices like other FETs. The charge carriers of the conducting channel constitute an inversion charge, that is electrons in the case of a *p*-type substrate (*n*-channel MOSFET) or holes in the case of an *n*-type substrate (*p*-channel MOSFET), induced in the semiconductor at the semiconductor-oxide interface by the voltage applied to the gate electrode. The electrons enter and exit the channel at the *n*+ source and drain contacts in the case of an *n*-channel MOSFET, at *p*+ contacts in the case of a *p*-channel MOSFET. Each of these devices can be either depletion mode in which the device is normally 'on' and is turned off by applying a gate voltage or enhancement mode in which the device is normally 'off' and is turned on by applying a gate voltage.

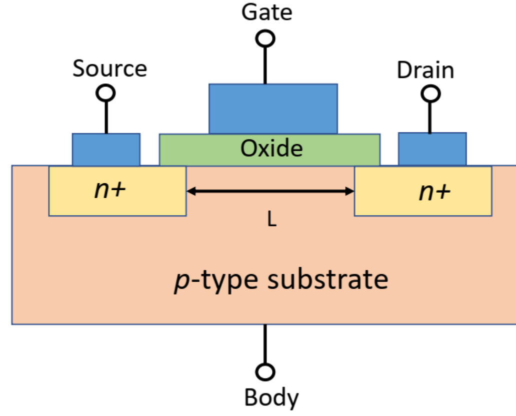

Figure 1.5: A schematic of an n-MOSFET structure. The current in the MOSFET is due to the flow of charge from the source terminal to drain terminal through the inversion-layer-induced (or referred to the channel region with a channel length L) adjacent to the metal-oxide-semiconductor interface.

1.1.2.1 *Current-Voltage characteristics*

The output characteristics of a long-channel MOSFET is shown in Figure 1.6, where each line in the family of characteristics corresponds to a different input gate-source voltage V_{GS}. For small values of drain-source voltage V_{DS} where $V_{DS} \leq V_{DS(sat)}$, the current is proportional to the voltage. This region is known as a linear or ohmic region, and a MOSFET operates like a resistor with the resistance being determined by the input voltage V_{GS}. The ideal *IV* relationship of the n-channel MOSFET in the linear region for $V_{GS} \geq V_T$ and for $0 \leq V_{DS} \leq V_{DS(sat)}$ is given by Equation (1.4).

$$I_D = \frac{\mathrm{W}\mu_n C_{ox}}{L}(V_{GS} - V_T - V_{DS}/2)V_{DS}, \tag{1.4}$$

where I_D is drain current, W and L are the channel width and channel length of the device, μ_n is the electron mobility, C_{ox} is the oxide capacitance, V_{GS} is the gate-source voltage, V_T is the threshold voltage, and V_{DS} is the drain-source voltage.

Moreover, in a long-channel device, the saturation current has a quadratic dependence with the V_{GS}. For a given V_{GS}, I_D will increase with V_{DS} until it reaches certain point.

After this point, the I_D will stop increasing even though V_{DS} increases. This is because of the inversion channel connecting the drain and source "pinches off" due to the electric field between the gate and source. When the electrons reach the pinch-off point they are injected in the depleted region and travels to the drain. This region is referred to saturation or beyond the pinch-off region where $V_{DS} \geq V_{DS\,(sat)}$. The Equation (1.5) is the ideal *IV* for n-channel MOSFET in the saturation region.

$$I_{D(sat)} = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2, \tag{1.5}$$

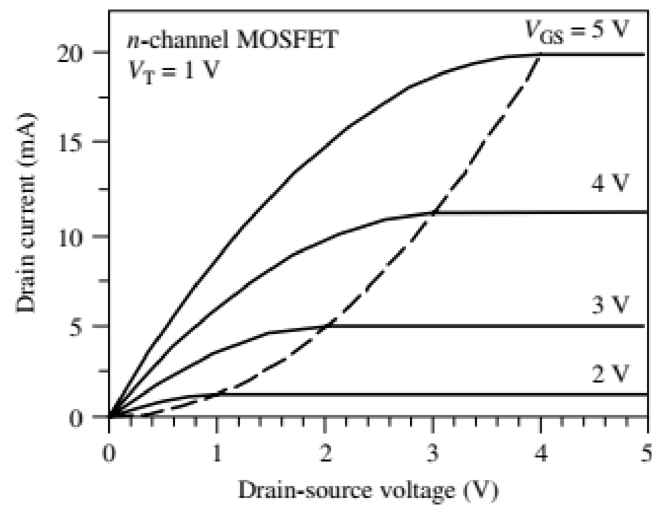

Figure 1.6: The current-voltage output characteristics of an *n*-channel MOSFET (long-channel device) with current saturation caused by pinch-off. The intersections with the dotted line indicate the onset of saturation for each characteristic. The threshold voltage is assumed to be $V_T = 1$ V [19].

However, a MOSFET will behave differently to a long-channel device as the channel length of the device is reduced due to scalling. The MOSFET is considered as a short-channel device if the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. Velocity saturation of the charge carriers when travelling along the channel is the most common short channel

effect as shown in Figure 1.7. Therefore, in a very short-channel MOSFET, I_D is in linear region when $V_{DS} \leq V_{GS} - V_T$, the I_D is given by the Equation (1.6).

$$I_D = \kappa(V_{DS})\frac{W\mu_n C_{ox}}{L}[(V_{GS} - V_T - V_{DS}/2)V_{DS}], \tag{1.6}$$

where $\kappa(V) = 1/(1 + (V\xi_c L))$ is a measure of the degree of velocity of saturation, whereas ξ_c is the electric field in the channel. For large L or small V_{DS}, κ approaches 1.

Moreover, in a short-channel device the saturation current has a linear dependence with V_{GS}. This is because the I_D saturates prematurely mainly due to velocity saturation. This is happens because the velocity of the carriers (and therefore the current) tends to saturate due to scattering effects (collisions suffered by the carriers). I_D saturates when $V_{DS} = V_{DS\,(sat)} \geq V_{GS} - V_T$. Therefore, the I_D is given by the Equation (1.7).

$$I_{D(sat)} = \kappa(V_{D(sat)})\frac{W\mu_n C_{ox}}{L}[\left(V_{GS} - V_T - V_{D(sat)}/2\right)V_{D(sat)}], \tag{1.7}$$

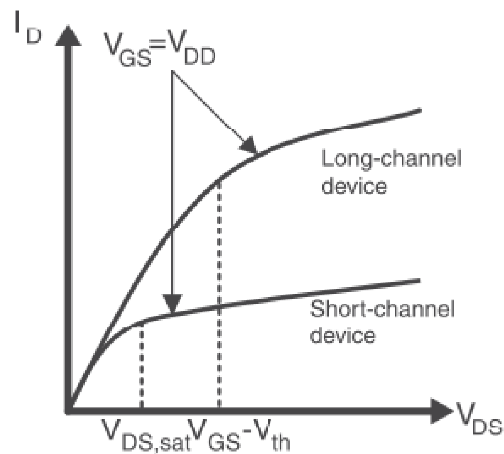

Figure 1.7: Short channel device expected behaviour due to velocity saturation [20].

1.1.2.2 *MOSFET device metrices*

Several of the device metrics can be determined from the current-voltage characteristics as shown in Figure 1.8 (a) and (b). The on-current (I_{ON}) is the maximum drain current which occurs at where I_D ($V_{GS} = V_{DS} = V_{DD}$), where V_{DD} is the power supply voltage. The on-resistance (R_{ON}) is the minimum channel resistance, which is one over dI_{DS}/dV_{DS} in the linear region for ($V_{GS} = V_{DD}$), whereas the output-resistance (r_d) is one over dI_{DS}/dV_{DS} in the saturation region for ($V_{GS} = V_{DD}$). Moreover, the MOSFET transconductance (g_m) is defined as the change in drain current with respect to the corresponding change in gate-source voltage. The transconductance is sometimes known as the transistor gain in unit µS/µm which is can be expressed in Equation (1.8) [21].

$$g_m = \frac{\partial I_{D\ to}}{\partial V_{GS}}, \tag{1.8}$$

For an n-channel MOSFET operating in the non-saturation region, the transconductance increases linearly with V_{DS} but is independent of V_{GS} as in Equation (1.9).

$$g_{mL} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{W \mu_n C_{ox}}{L} . V_{DS}, \tag{1.9}$$

Meanwhile, the transconductance is a linear function of V_{GS} and is independent of V_{DS} in the saturation region as in Equation (1.10).

$$g_{ms} = \frac{\Delta I_{D\,(sat)}}{\Delta V_{GS}} = \frac{W \mu_n C_{ox}}{L} . V_{GS} - V_T, \tag{1.10}$$

The transconductance is a function of the geometry of the device as well as of carrier mobility and threshold voltage. The transconductance increases as the width of the

device and the oxide capacitance increases, and it also increases as the channel length and the oxide thickness decrease [21].

The subthreshold swing (SS) with typically in unit mV/decade is the change in gate voltage required to change the drain current by a factor of 10. The SS can be extracted from the slope of log I_D versus V_{GS} curve as shown in Figure 1.8 (b). The smaller the SS, the lower the gate voltage needed to switch the transistor from off to on. The subthreshold characteristics increase exponentially with V_{GS} and can be given by Equation (1.11).

$$SS = \frac{k_B T}{q}\left[\frac{d(log_{10} I_D)}{dV_{GS}}\right], \tag{1.11}$$

The shift of subthreshold IV characteristics with increasing drain voltage is attributed to drain-induced barrier lowering (DIBL) effect which can be defined as the horizontal shift in the low and high V_{DS} subthreshold characteristics divided by the difference in the drain voltage, typically $V_{DD} - 0.05\ V$ as shown in Figure 1.8 (b).

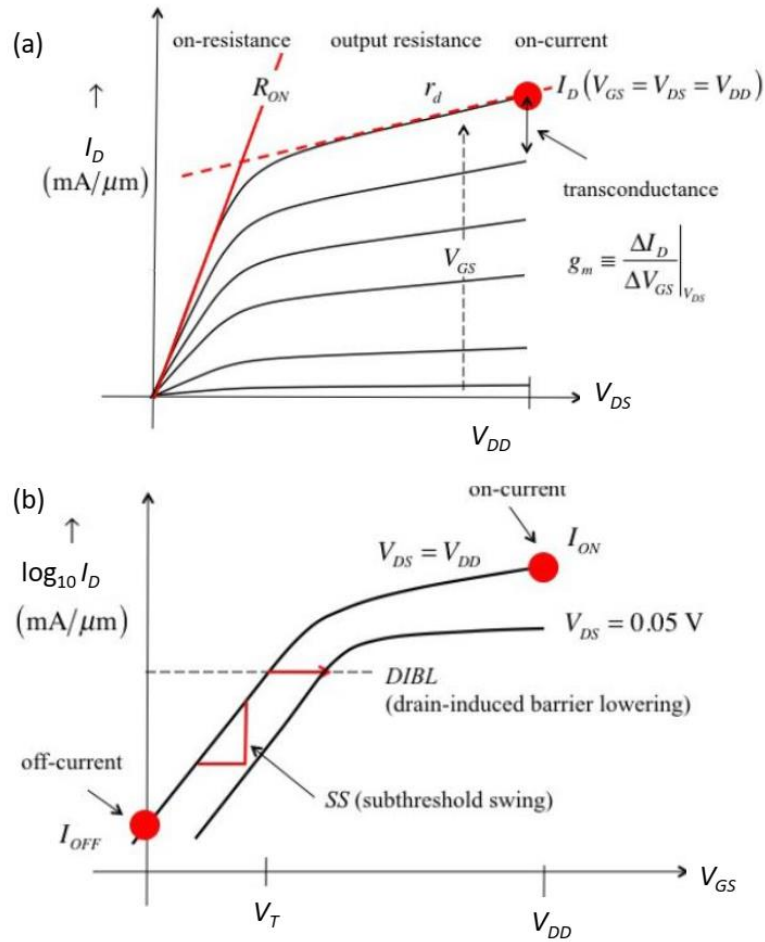

Figure 1.8: The common source output characteristics of an n-channel MOSFET (a) with four device metrics: on-current, on-resistance, output resistance, and transconductance; and (b) with two additional device metrics: subthreshold swing and drain-induced barrier lowering [22].

1.1.3 State of the art Si CMOS technology

State of the art CMOS technology employs HfO_2 as the most promising material for alternative gate dielectric applications due to its relatively high dielectric constant (20–25) [23], wide band gap (5.68 eV) [24] , high heat of formation (271 kcal/mol) [25], [26], high density (9.68 /cm^3) [24] and thermodynamic stability in contact with Si [7], [27] as well as it can achieve appropriate threshold voltages [28], [29]. The introduction of high-*k*/metal gate technology has a profound effect on many critical device properties including EOT, channel mobility, threshold voltage and reliability. The gate dielectric typically consists of multilayer stacks where each layer

performs different function [30]. The interfacial layer (IL) which is usually formed between the main high-k oxide and the underlying semiconductor has the purpose of achieving a high electrical quality of the interface with the channel while the main layer is bulk high-*k* responsible for EOT scaling and leakage current control. In current Hf-based technology, a bulk high-*k* layer of Hf-based dielectric (e.g. HfO_2, HfSiON) is deposited on top of chemically grown silicon oxide (SiO_x) or oxynitride (SiON) IL, whose thickness can be controlled using different oxidation methods and carefully designed scavenging steps [29]. The reduction of IL thickness has been observed to have a significant effect on the degradation of the channel mobility and device reliability [31], [32] and even worse for the case without the IL [33].

As discussed above, the integration of high-*k* ILs is a possible solution to extend the scalability of Hf-based gate stacks. Rare-earth oxides became the promising high-*k* candidates because of their relatively high dielectric constants [34], wide band gap and good thermodynamic stability [35]. RE oxides have been previously studied including Y_2O_3 [36], [37], Pr_2O_3 [38], Gd_2O_3 [39], Lu_2O_3 [40], [41], La_2O_3 [42]–[46], Er_2O_3 [47], [48] and Tm_2O_3 [49]–[55]. There is a lot of research reported that a direct contact approach of RE oxides of La_2O_3 with the Si substrate has successfully achieved the formation of La-silicate IL [42]–[44], [56], [57]. This system achieved low EOT of 0.5 nm [56] with high transistor mobility of 155 cm^2/Vs [57] and low interface state density of 1.6×10^{11} $cm^{-2}eV^{-1}$ [57]. The main problem with La_2O_3 is the excess growth of the silicate layer after annealing which is found to increase EOT [58]. In addition, the drawback of La_2O_3 is its hygroscopic nature as well as high reactivity with Si. Recently, several studies have been done on the integration of Tm-silicate (TmSiO) as an IL [28], [59]–[62]. Tm_2O_3 has interesting properties of a high dielectric constant of k ~16 [63], an energy band gap of E_g ~5.77 eV [64], high effective barriers for holes

(CBO=2.3 eV) and electrons (VBO=3.1 eV) [52], and a low reactivity with the Si substrate [53]. The formation of TmSiO IL provides a relatively high dielectric constant (k = 10–12) [53] which is similar to LaSiO [43]. It has been demonstrated recently that TmSiO is a contender for integration as a high-k IL, achieving EOT of the IL of ~ 0.2 nm with interface state density <2×10^{11} $cm^{-2}eV^{-1}$ [59]. An optimised annealing condition has been reported leading to gate leakage current density comparable with state-of-the-art SiO_x/HfO_2 *n*FETs (0.7 A/cm^2 at a gate bias of 1 V) at 0.6 nm EOT [62].

1.1.4 Ge-based MOSFETs

Using semiconductors with high channel mobility can also improve the performance of MOSFETs by enabling faster speed and lower power dissipation. In recent years, germanium has attracted much interest as an alternative channel material to replace Si for the next generation of CMOS technology due to its high carrier mobilities for both electrons (3900 cm^2/Vs) and holes (1900 cm^2/Vs) than those of Si [65]. This permits more efficient source injection and shorter CMOS gate delay and is due to the low effective electron and hole masses. Moreover, Ge also has a smaller band gap (0.67 eV) for lower contact resistances which are suitable for voltage scaling [66]. Another advantage of Ge is its low-temperature activation of source/drain implants that it is possible to fabricate self-aligned metal-gate MOSFETs by applying a conventional Si process [67]. It also has process compatibility with Si-based MOS technologies.

Interestingly, in semiconductor history, Ge was the material used in the first transistor invented by John Bardeen, William B. Shockley and Walter H. Brattain in 1947. This became the most important invention of the 20th century. Unfortunately,

the semiconductor industry shift from germanium to silicon in the 1960s has been due to the requirement of high purity of Ge crystal. In addition, Ge lacks a high-quality native oxide, where GeO_2 is less stable due to its hygroscopic and water-soluble nature [68]. It was reported that GeO_2 is thermodynamically unstable at a temperature of about 400-450 °C [69]. In order to establish the Ge MOS technology, one of the most critical challenges is the formation of gate stacks with superior interface properties, that is a low defect interface layer and a dielectric layer. High-*k* gate dielectrics deposited on Ge have been extensively studied including HfO_2 [70]–[74], ZrO_2 [74], [75], Al_2O_3 [73], [76]–[78], $LaAlO_3$[79], CeO_2 [80], [81], Gd_2O_3 [82], La_2O_3 [83], and Y_2O_3 [83], [84]. Recently, rare-earth thulium oxide (Tm_2O_3) has also been studied for use as a passivation layer on Ge [64], [85].

There is still a difficulty in producing Ge-based CMOS, where direct deposition of high-*k* gate dielectric on Ge has exhibited poor electrical characteristics [70], [75], [76], [79], [85]. To overcome this problem, an interfacial layer is introduced between the high-*k* layer and the Ge substrate to provide effective electrical passivation of the Ge surface. Among a variety of ILs, high-quality GeO_2 has been reconsidered as an alternative passivation layer due to exhibiting lower interface trap density (D_{it}) values and also for its use in high-performance Ge n-channel MOSFETs [86], [87]. GeO_2/Ge is one of the most fundamental interfaces in Ge CMOS, similar to the SiO_2/Si interface in the Si CMOS technology. However, because GeO_2 has much lower *k* value (~6), means that the gate stacks containing thick interfacial GeO_2 layers are difficult to scale below 1 nm EOT. Therefore, a high-*k*/GeO_2 IL/Ge gate stack with high quality and ultrathin GeO_2 interfacial layer is needed to achieve sub-nanometer overall EOT in high-performance Ge MOSFETs. The integration of high-*k* *g*ate dielectric in high-quality GeO_2 IL/GeO_2 may exhibit better electrical characteristics than the GeO_2 as a

gate dielectric layer. The most promising route is to use a well-controlled oxidation method to fabricate the GeO_2 IL of very good quality. It has been reported that high-quality GeO_2/Ge interfaces have been fabricated by thermal oxidation [85], [87], [88], ozone oxidation [89] and plasma oxidation [90]. Recently, it has been reported that the D_{it} of the gate stack can be improved to below 5×10^{11} $cm^{-2}eV^{-1}$ for Tm_2O_3/GeO_2/Ge with an O_2 rapid thermal anneal at 500 °C for 1 min [85].

1.1.5 Other III-V MOSFETs

Besides Ge, III-V compound semiconductors have been recently considered as promising candidates to replace Si for future CMOS technology nodes [91]–[93]. These III-V materials attracted great interest due to their several advantages in terms of band engineering, high mobility/offsets and low effective mass for both electrons and holes used for high-speed, high-frequency and low-power electronic devices [92]. These III-V devices can be used in great volumes for applications such as data processing, communications, imaging, and sensing, particularly in portable equipment such as hand-held devices and satellites [92]. On the other hand, unlike Si that can form SiO_2 native oxide layer, no native oxides exist for III-V compounds. The exposure of an III-V surface to oxygen results in Fermi-level pinning, which is an inability to modulate the electrostatic potential inside the semiconductor [94]. Moreover, the oxidation produces a rich layer of Ga and As oxides and sub-oxides, elemental As, As-As dimers and Ga dangling bonds and other defects [95]. The surface oxidation was the main issue for MOSFET devices during early research of III-V materials. Hence, deposited gate insulators required for III-V semiconductors need to achieve device performance superior to that of Si devices. The integration of high-*k* material on III-V compounds has been extensively investigated including HfO_2/GaAs

[96], HfO_2/InSb [97], HfO_2/GaSb [98], Al_2O_3/InSb [99], [100], Al_2O_3/GaSb [101][102], HfO_2/InGaAs [103], Al_2O_3/InGaAs [104]–[109], Al_2O_3/InGaSb [110]–[112] and Al_2O_3/InGaSb/GaSb/GaAs [113].

$In_xGa_{1-x}As$ ternary compound is a very promising candidate for future use in high-performance CMOS technology particularly in *n*-FETs because it allows for a very good trade-off between the excellent transport properties of InAs and the low leakage of GaAs [114], [115]. InGaAs has surpassed GaAs as a potential compound semiconductor for future MOSFETs due to its superior electrical performance. Stable InGaAs exists in a variety of In concentrations allowing for control of both physical properties and therefore electrical properties such as mobility and band gap. One of the challenges in realising a high mobility channel is to understand the surface passivation techniques. In InGaAs systems, numerous approaches including sulfur-based chemical cleans [105], [109], As_2 capping and decapping [104], trimethylaluminum (TMA) pre-dosing [108], cyclic plasma (H_2 or N_2) and TMA exposures [103] as well as AlN interface control layer [116] have been explored to passivate InGaAs (100) surfaces prior to atomic layer deposition (ALD) of high-*k* gate dielectrics.

On the other hand, antimony (Sb)-based compound semiconductors have also attracted extensive interest due to their superior transport properties for both electrons and holes, with InSb and GaSb having bulk electron and hole mobilities of 77000 $cm^2V^{-1}s^{-1}$ and 1000 $cm^2V^{-1}s^{-1}$ respectively. $In_xGa_{1-x}Sb$ ternary compounds offer the combined optimal performance for electrons and holes in the same material. The incorporation of In maintains excellent electron transport [103], while hole mobilities as high as 1500 $cm^2V^{-1}s^{-1}$ have been demonstrated in strained *p*-$In_{0.4}Ga_{0.6}Sb$ quantum wells [117]. Moreover, Sb-based materials are suitable for low-temperature processing

due to low melting points, which allow for simpler process flow. Many studies have been reported on InGaSb devices [110]–[112] to improve the electrical properties of the dielectric interface to antimonides, particularly on GaSb and InSb only. For the former, ex-situ HCl acid and $(NH_4)_2S$ surface treatments as well as in-situ H_2 plasma have shown promising results. Recently, surface treatments comprising a combination of ex-situ HCl treatment and in-situ H_2 plasma exposure prior to the ALD of Al_2O_3 gate dielectric yielded significant improvements to the electrical properties of the $In_{0.3}Ga_{0.7}Sb$-Al_2O_3 interface [111], [112].

1.2 GaN MIS-HEMTs

Gallium nitride (GaN)-based power devices, especially the high electron mobility transistors (HEMTs), have been demonstrating the potential to satisfy the ever-growing demand for improved performance in terms of speed, power and efficiency over the past few decades. The HEMT has the advantages of offering simple circuit design and fail-safe operation [118]–[121]. GaN belongs to the III-Nitrides family of III-V semiconductors and exhibits excellent properties due to its wide band gap (3.4 eV) being larger than that of Si (1.1 eV) and SiC (3.2 eV) [122]–[125]. This wide band gap offers a higher breakdown voltage because of the ultimate breakdown field required for band-to-band impact ionisation [126]. In detail, under high electric field, high-energy electrons and holes generate electron-hole pairs by collisions with the atoms in the lattice exciting electron from the valence band to conduction band. This process for the generation of electron-hole pairs is called impact ionisation. GaN also has high electron mobility of 2000 cm^2/Vs for two-dimensional electron gas (2DEG) [124], high saturation velocity of 3×10^7 cm/s, and high critical breakdown electric field of 4.2 MV/cm [125] as compared to Si and SiC which allows for higher

frequency operation [127]. The combination of high carrier concentration and high electron mobility results in a high current density and a low channel resistance, which are especially important for high-frequency operation and power switching applications. Moreover, the ability of GaN to form heterojunctions makes it superior compared to SiC [128], [129]. Nowadays the GaN-based Metal-Insulator-Semiconductor (MIS)-HEMT device is demonstrating superior performance in power electronics applications over the Schottky gate counterpart, due to its ability to suppress gate leakage current [130], and provide larger forward gate voltage swing by engineering the threshold voltage between the depletion and enhancement mode operations [131] and to improve gate-drain breakdown voltage as well [132]. These attractive properties of GaN over other wide band gap materials make it a very promising candidate for next-generation semiconductor devices, which are intended for high temperature and high-frequency operation. Table 1.1 shows the important GaN material parameters in comparison to other common semiconductor materials such as Si, Ge, GaAs, InP, SiC and diamond, InAs, GaSb, and GaSb. Other ternary III-V compound semiconductor such as $In_{0.47}Ga_{0.53}As$ has a band gap of 0.75 eV with electron mobility of 14000 cm^2/Vs and hole mobility of 300 cm^2/Vs as well as the dielectric constant of 13.9 [133], whereas $In_{0.4}Ga_{0.6}Sb$ provides electron mobility of 1500 cm^2/Vs [117].

Table 1.1: GaN properties as compared to other semiconductor materials [122]–[125], [133]–[136].

Semiconductors / Properties	Si	Ge	GaAs	InP	SiC	diamond	GaN	InAs	GaSb	InSb
Band gap, E_g (eV)	1.12	0.66	1.42	1.35	3.2	5.5	3.4	0.36	0.72	0.18
Electron mobility at 300 K, μ_n (cm^2/Vs)	1500	3900	8500	5400	700	1900	1000–2000	30000	5000	80000
Electron saturation velocity, V_{sat} ($\times 10^7$ cm/s)	1.0	0.6	1.0	1.3	2.0	2.7	3.0	4.0	–	5.5
Critical breakdown field, E_c (MV/cm)	0.3	0.08	0.4	0.5	3.0	5.6	4.2	0.04	0.05	0.001
Thermal conductivity at 300 K, λ (W/cm.K)	1.5	0.59	0.5	0.7	4.5	20	> 1.5	0.27	0.4	0.15
Relative dielectric constant, ε_r or k	11.8	16	12.8	12.5	10	5.5	9	15.1	15.7	17.9

1.2.1 Basic structure of HEMT

The basic structure of a HEMT consists of a wide band gap semiconductor (AlGaN) grown on top of another material with narrower band gap (GaN). This is known as a heterojunction where a junction forms between two materials with different band gaps. Figure 1.9 (a) shows the basic structure of AlGaN/GaN HEMT. The principle of operation in a HEMT is very similar to MOSFET (Figure 1.9 (b)). However, instead of carrying current in a thick channel like MOSFET, a HEMT relies on the formation of a 2DEG at the heterojunction interface. In AlGaN/GaN HEMTs, the formation of the 2DEG is due to the charge carriers appearing at the interface of the heterojunction caused by inherent electric field [137]. This electric field forms two components of polarisation namely spontaneous and piezoelectric polarisation. The

polar nature of GaN and AlGaN crystals is related to the high electron negativity of nitrogen, which produces a negative sheet charge density on one face of the crystal and a positive sheet charge density at the opposite face. The presence of polarisation charges causes a built-in polarisation along the layer thickness (Figure 1.10 (a)) known as spontaneous polarisation [137]. The different lattice constants of AlGaN and GaN crystal cause tensile stress on the AlGaN layer near the interface of the heterojunction. The tensile stress from growing lattice-mismatched AlGaN on GaN induces a static charge and a built-in polarisation field in the barrier layer due to piezoelectric properties of nitrides. The piezoelectric polarisation has the same direction as the spontaneous polarisation (Figure 1.10 (b)) [137]. This spontaneous and piezoelectric polarisation produces a net positive charge at the AlGaN/GaN interface and a net negative charge at the top of the barrier forming a polarisation dipole (Figure 1.10 (c)) [137]. This dipole is complemented by an opposing one, which is formed by the 2DEG at the interface and a hole gas at the top of the AlGaN surface (Figure 1.10 (d)).

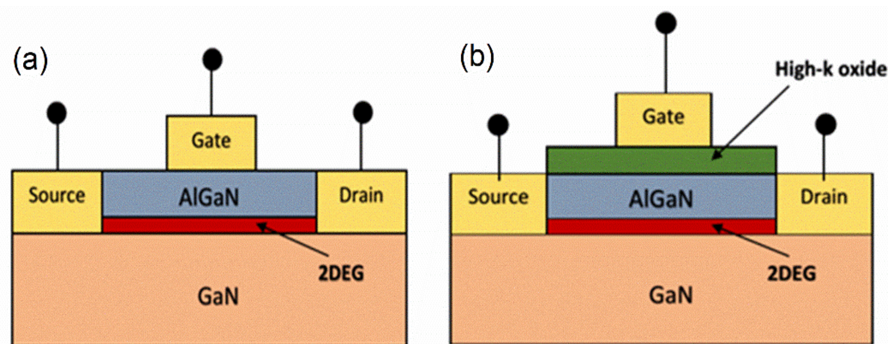

Figure 1.9: Structure of (a) AlGaN/GaN HEMT, (b) AlGaN/GaN MIS-HEMT.

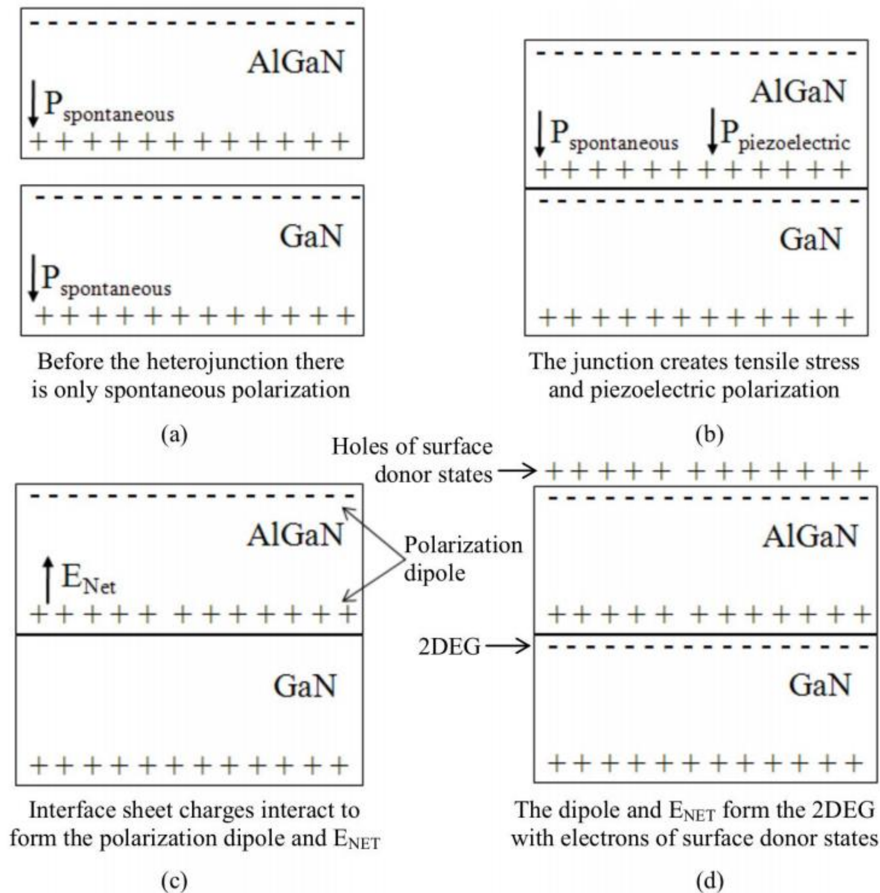

Figure 1.10: The 2DEG formation (a) before heterojunction, (b) the formed heterojunction produces tensile stress, (c) the polarization dipole occurs, (d) the 2DEG is formed [137], [138].

1.2.2 GaN issues

There are significant challenges that must be addressed related to GaN HEMTs such as high gate leakage refers to current lost through the gate by electron tunnelling, degrading power efficiency, and noise performance. This can be minimised by the insertion of a thin insulator layer between the gate metal and the semiconductor, which behaves as a barrier to reduce the gate leakage current [139], [140] resulting in MIS-HEMT shown in Figure 1.9 (b).

Another issue is related to the surface defects (e.g. vacancies and interstitials) in GaN which result in the degradation of the device performance [6], [141], [142].

One of the most common defects that have been reported is nitrogen vacancies which can be easily formed due to the thermal decomposition and evaporation of nitrogen from the GaN surface during the high-temperature process [142]. It was reported that the N-passivation technique improves the surface and interface quality of GaN film by filling the nitrogen vacancies, reducing the dangling bonds, and removing the surface impurities [142].

1.2.3 Several oxides on GaN

High-k dielectric metal oxide films have attracted considerable research attention due to their promising features as gate insulators including Al_2O_3 [123], [128], [129], [143]–[145], HfO_2 [123], [146], MgO [147], [148] and $LaLuO_3$ [149]. Al_2O_3 is the most commonly used gate dielectric. This system offers a large band offset with III-nitride material, high dielectric constant (k ~8.6–10), high breakdown electric field (~10–30 MV/cm) and good interface quality with average D_{it} of ~7 $\times 10^{10}$ $cm^{-2}eV^{-1}$ and a corresponding hysteresis voltage of 100 mV [143]. Table 1-2 shows the band offsets for various dielectric/GaN interfaces [10], [150], [151]. Recently, ZrO_2 is reported to exhibit maximum transconductance (g_m) of 138 mS/mm with low interface state density ($< 4 \times 10^{11}$ $cm^{-2}eV^{-1}$) [152] due to the favourable band alignment to GaN [153]. Besides, Ta_2O_5 also shows good interface quality with GaN because it has a high-k of 22–25 [10], [154] which could improve transconductance. 2DEG carrier concentration of AlGaN/GaN structures passivated with a thin Ta_2O_5 film (2–4 nm) also has been reported [155]. A previous study incorporating Ta_2O_5 compared to HfO_2-based HEMTs showed a larger g_m of 315 mS/mm and a higher current density of 1.37 A/mm with comparable gate leakage currents [156]. Recently, it has been reported that the complementary characteristics of high-k Ta_2O_5 and wide

band gap Al_2O_3 could be combined by fabricating $Ta_2O_{5x}(Al_2O_3)_{1-X}$ as a gate dielectric to achieve a high-*k* and sufficient CBO to the GaN for low leakage current in HEMT device configurations [157].

Table 1.2: The physical properties of several dielectric materials suitable with GaN-based devices [10], [150], [151].

Material	Relative permittivity [10]	Band gap [151]	VBO [150]	CBO [150]
SiO_2	3.9	9	3.1	2.6
Si_3N_4	7	5.3	0.8	1.3
AlN	8.5	6.2	0.4	2.4
Al_2O_3	9	8.8	3.0	2.4
Y_2O_3	15	5.7	0.8	1.9
La_2O_3	30	6	0.7	2.0
HfO_2	25	6	1.6	1.1
Ta_2O_5	22	4.4	1.1	0.1
ZrO_2	25	5.8	1.6	1.1

1.3 Research aims and objectives

This research project has the aim to study high-*k* dielectrics and their interfaces on Si, Ge, GaN, InGaAs and InGaSb for device applications. The key objective includes the investigation of the band alignment and interface properties of several oxides (Tm_2O_3, Ta_2O_5, ZrO_2, Al_2O_3 and MgO), deposited on different semiconductors: Si, Ge, GaN, InGaAs and InGaSb in order to propose the best routes for passivation of semiconductor/high-*k* oxide interfaces for semiconductor devices. Besides, the work also focuses on the understanding of electrical characteristics of fabricated GaN-based MIS capacitor and MIS-HEMT devices.

1.4 Thesis outlines

A detailed overview of the structure of this thesis is as follows:

Chapter 1: This chapter has highlighted the significance of device scaling and the requirement of high-*k* dielectrics for the next generation of CMOS technology and industry. The chapter began with a review of the previous and current research work on Si, Ge, and other III-V (InGaAs and InGaSb) semiconductors for CMOS technology with the integration of high-*k* gate dielectrics. This chapter also discusses related issues and overview of GaN MIS-HEMTs and the research objectives.

Chapter 2: The fabrication and characterisation techniques in this work is explained in detail in this chapter. Several GaN surface treatment techniques were discussed in detail in the beginning and followed by the deposition method used to deposit several oxides such as sputtering and atomic layer deposition methods. This chapter also includes an overview of physical characterisation techniques such as X-ray photoelectron spectroscopy (XPS) and variable angle spectroscopic ellipsometry (VASE) as well as the electrical measurement techniques (current-voltage (*IV*) and capacitance-voltage (*CV*)).

Chapter 3: The chapter discusses the physical properties of rare earth Tm_2O_3/Si gate stacks grown by ALD mainly using XPS technique. The band alignment of Tm_2O_3 on Si has also been investigated using Kraut's method. The atomic structure and elemental analysis were also performed using high-resolution transmission electron microscopy (HRTEM) and electron energy-loss spectroscopy (EELS). Furthermore, the physical properties of ALD-deposited GeO_2/Ge and Tm_2O_3/Ge gate stacks with different annealing treatments are also studied.

Chapter 4: The chapter began with a discussion of different GaN surface treatments. The band alignments of sputtered Ta_2O_5, ZrO_2, Al_2O_3 and MgO on GaN have also been studied using XPS and VASE. Comparative studies on band offset values for several oxide/GaN systems in relation to published data are discussed in detail in this chapter.

Chapter 5: This chapter focuses on the electrical characterisation of GaN-based devices including the GaN MOS capacitors with different gate dielectric layers (Ta_2O_5, ZrO_2, Al_2O_3 and MgO) and the depletion (D)-mode and enhancement (E)-mode MIS-HEMTs with gate dielectric ZrO_2 and Al_2O_3 (with and without O_2 plasma treatment). The *IV* and *CV* measurements have been performed to investigate the electrical performance of GaN devices in term of their leakage current density, threshold voltage and interface trap density.

Chapter 6: This chapter studies other III-V compound semiconductors as a replacement of Si for future CMOS technologies. This chapter aims to investigate the effect of forming gas anneal (FGA) and H_2/TMA/H_2 plasma treatment on HfO_2/(100) InGaAs and HfO_2/(110) InGaAs interfaces. Besides, this chapter has also discussed the effect of InGaSb surface treatments with HCl acid only, both ex-situ HCl acid and in-situ H_2 plasma exposure (HCl+H_2) on the electrical properties of the $In_{0.3}Ga_{0.7}Sb$-Al_2O_3 interface. XPS measurements were performed to understand the chemical composition of the HfO_2/InGaAs and Al_2O_3/InGaSb interfaces.

Chapter 7: This final chapter reviews the general findings and presents conclusions from the research presented in the thesis. It also provides directions for further research of interest for future CMOS and MIS-HEMT device applications.

CHAPTER 2

Experimental Techniques

2.1 Material deposition methods

A wide range of techniques has been employed for depositing high-*k* dielectric material films such as molecular beam epitaxy (MBE) [149], [158], chemical vapour deposition (CVD) [159], [160] and atomic layer deposition (ALD) [63], [64], [123], [144], [161]. In our work, the samples have been deposited by sputter and ALD deposition method.

2.1.1 Sputtering

Sputtering is one of the promising techniques in physical vapour deposition (PVD) technology and was first developed in the late 1970s. It has already been widely used to modify various materials in diverse industries including semiconductor processing [162]. Sputter deposition has many advantages as it produces high-energy flux which has high surface mobility and thus can condense into smooth, dense, conformal, and continuous films more easily than evaporation or CVD. Moreover, sputtering preserves the stoichiometry of the target source since the physical bombardment mechanism of particle ejection results in a consistent stoichiometry on the sample surface. Generally, it allows a good film adhesion to the substrate, and high control of the thickness, uniformity and composition of the deposited material [162].

Sputtering techniques can generally be grouped into categories depending on their functions. The techniques include direct current (DC) sputtering, radio frequency (RF) sputtering, reactive sputtering and magnetron sputtering. DC sputtering is usually

used for metal targets. RF sputtering has to be used to avoid charge build-up when an insulating target is used. Magnetron sputtering utilises strong electric and magnetic fields to trap electrons close to the surface of the target. Argon, an inert gas, is often used as the bombardment gas in a sputtering process. In reactive sputtering, the deposited film is formed by chemical reaction between the target material and a reactive gas that is introduced into the sputtering chamber.

RF sputtering is used mainly due to the problem of insulators target type that cannot be sputtered through conventional DC techniques because the accelerating potential cannot be directly applied to the insulator surface [163]. This prevents neutralising of the positive charge which would accumulate on the surface during ion bombardment. This problem can be overcome by applying a high frequency potential to a metal electrode behind the insulator. Power can be fed into the plasma via the displacement current through the dielectric material, and sputtering can occur because the insulator will now be alternately ion and electron bombarded. The positive charge which accumulates on the surface during the negative or sputter portion of each cycle will now be neutralised by electrons during the positive part of the cycle.

Figure 2.1 shows the schematic illustration of a sputtering system, where the substrate (or sample) is placed at sample holder in a vacuum chamber with the source material (target) while an inert gas (typically argon) is introduced at low pressure (or high vacuum). A gas plasma is struck using a radio frequency (RF) power source, causing the gas to become ionised. The ions are accelerated towards the surface of the target, causing atoms of the source material to break off from the target in vapour form and condense on all surfaces including the substrate. In details, ions can be generated by the collision of neutral atoms with high energy electrons. The interaction of the ions and the target are determined by the velocity and energy of the ions. Since ions are

charged particles, electric and magnetic fields can control these parameters. The process begins with a stray electron near the cathode is accelerated towards the anode and collides with a neutral gas atom converting it to a positively charged ion. The process results in two electrons which can then collide with other gas atoms and ionise them creating a cascading process until the gas breaks down. The breakdown voltage depends on the pressure in the chamber and the distance between the anode and the cathode. At too low pressures, there aren't enough collisions between atoms and electrons to sustain a plasma. At too high pressures, there are so many collisions that electrons do not have enough time to gather energy between collisions to be able to ionise the atoms.

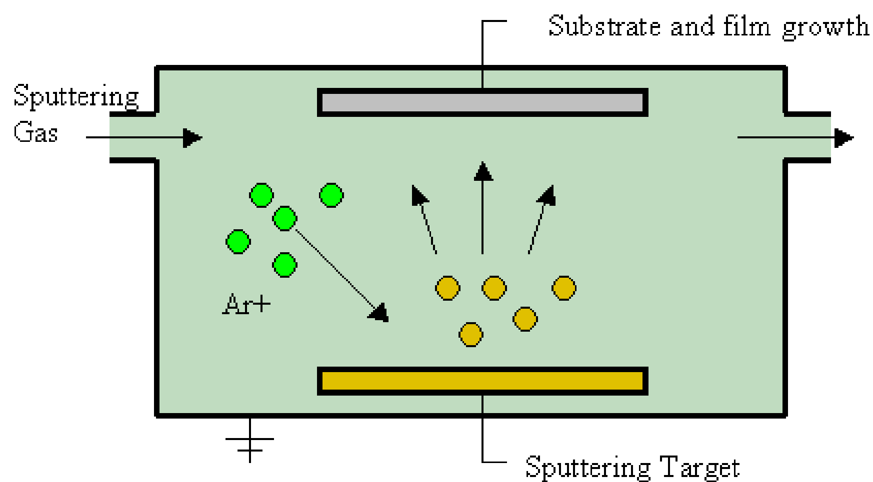

Figure 2.1: The schematic illustration of the sputtering system [164].

The rate at which the coating material leaves the target depends on the number of bombarding ions hitting the target. It is therefore desirable to increase the plasma density in front of the sputtering source, to obtain a high deposition rate. Sputtering without any plasma confinement has the disadvantages of low deposition rates and low ionisation efficiencies of the plasma. These limitations have led to the development of magnetron sputtering. Magnetron sputtering was developed to solve the electron

problem by placing magnets parallel to the target surface, which can constrain the motion of secondary electrons ejected by the bombarding ions to the close vicinity of the target surface. The ion current is also increased by order of magnitude over conventional diode sputtering systems, resulting in faster deposition rates at lower pressure.

In this work, several oxides including Ta_2O_5, ZrO_2, Al_2O_3 and MgO were deposited using NanoPVD (150 W, 13.56 Hz) RF magnetron sputter system developed by Moorfield Nanotechnology as shown in Figure 2.2.

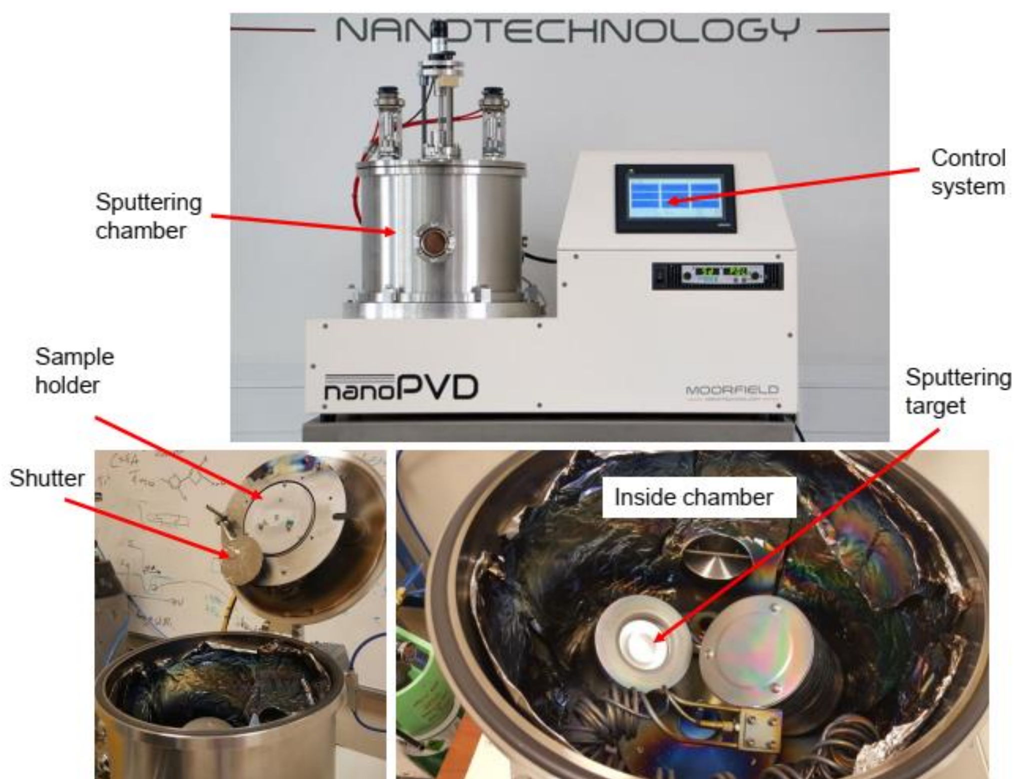

Figure 2.2: The RF magnetron sputtering system used in this work at the University of Liverpool, UK.

2.1.2 Atomic layer deposition

Atomic layer deposition has emerged as a very promising method, which relies on sequential, self-limiting and surface controlled gas phase chemical reactions to

obtain atomic layer control of deposition. ALD has several advantages including lower deposition temperature, precise thickness control, excellent step coverage and greater conformality [165], [166]. Figure 2.3 illustrates one ALD cycle process which consists typically of four steps [167]. These four steps are repeated as many cycles to grow a film of the required thickness as mentioned below:

i. Step 1a: first gas-solid reaction (chemisorption reaction) of the first metal reactant (Reactant A)
ii. Step 1b: purge or evacuation to remove the unreacted precursor and gaseous by-products
iii. Step 2a: the second gas-solid reaction of the second non-metal reactant (Reactant B)
iv. Step 2b: another purge or evacuation to remove the unreacted precursor and gaseous by-products

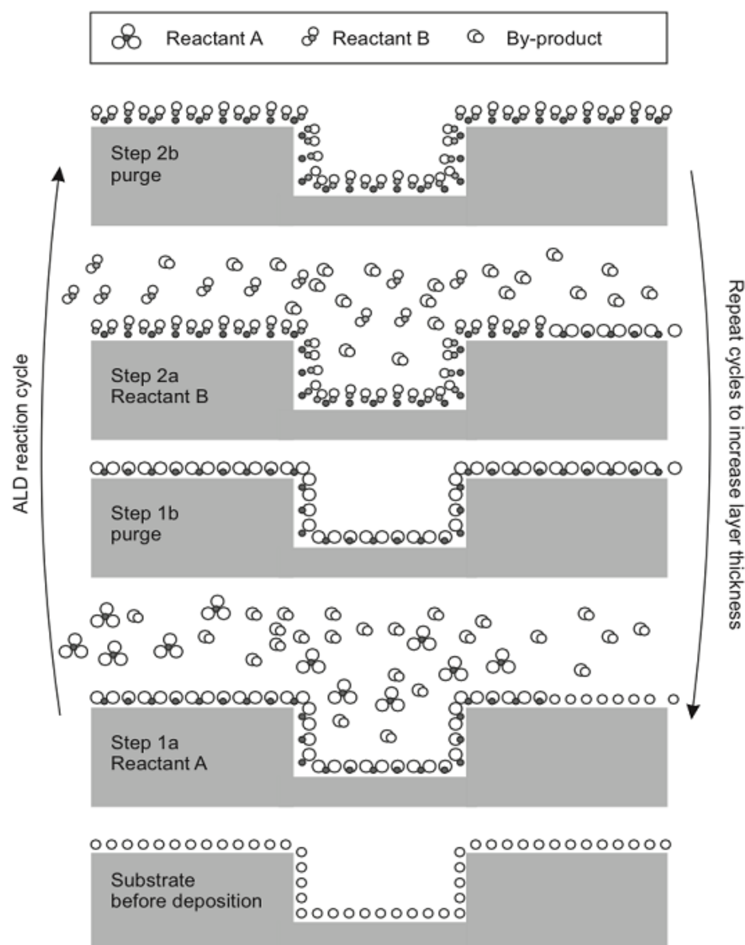

Figure 2.3: The schematic diagram of one ALD cycle [167].

In this work, the commercially available Beneq TFS 200 ALD system was used to deposit Tm_2O_3 as shown in Figure 2.4. The tool employs a crossflow-type 200 mm hot-wall reactor enclosed in a cold-wall chamber, with the possibility to perform both thermal and plasma-enhanced ALD from room temperature to 500 °C. The system supports 4 liquid sources and 2 solid sources, which can be heated up to 300 °C. An external BMT 802N ozone generator allows the use of O_3 as an oxidising agent. Ar is used as carrier and purge gas, at a base pressure of 1 mbar.

Figure 2.4: Beneq TFS 200 ALD system located at the KTH Royal Institute of Technology, Sweden.

2.2 X-ray photoelectron spectroscopy (XPS)

2.2.1 Basic principles of XPS

XPS is a surface analysis characterisation technique that measures the elemental composition, chemical state and electronic state of the elements within a material [45], [50], [51], [168], [169]. XPS or previously known as the term "electron spectroscopy for chemical analysis" (ESCA) was developed in the mid-1960s by Kai Siegbahn and his research group at the University of Uppsala, Sweden.

The XPS system includes an ultra-high vacuum (UHV)-based stainless steel chamber containing the sample stage, electron energy analyser and detection system, an X-ray source (with or without monochromator) as illustrated in Figure 2.5 [170]. This XPS system is usually attached to ion gun for sample cleaning and depth profiling as well. X-ray sources typically used are Mg Kα ($h\nu$ =1253.6 eV), Al Kα ($h\nu$ =1486.6 eV), or monochromatic Al Kα (hν =1486.7 eV). The analyser is usually hemispherical type operated as an energy window which filters and then collects only photoelectrons having correct pass energy. The detector records the defined energy and results in

energy spectra. Outside the UHV system are consoles with electronics supply systems and the computer with the data acquisition and processing software. The XPS components are discussed in more detail in this chapter.

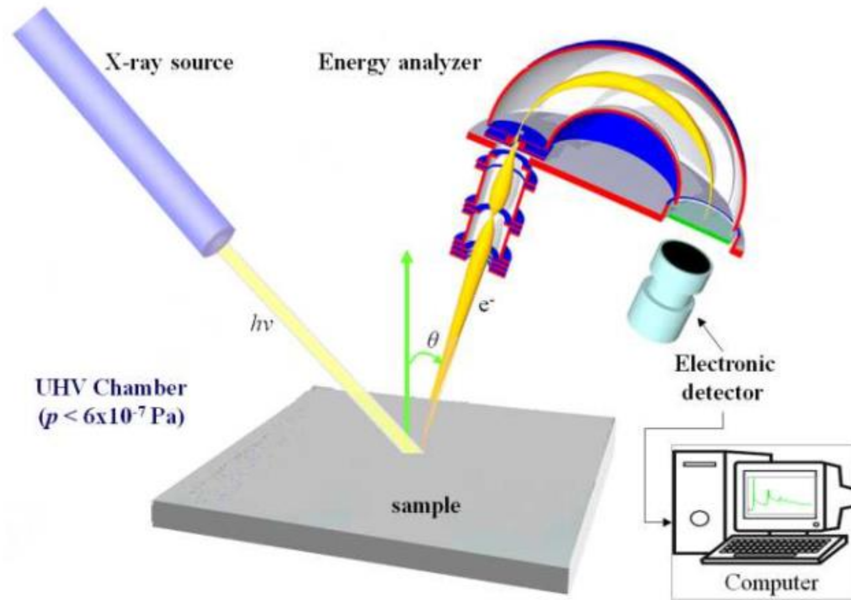

Figure 2.5: The schematic of a typical XPS system consists of the sample stage, UHV chamber, X-ray source, energy analyser and detector [170].

The basic principle of the XPS technique involves the photoemission process where electrons in the atomic core levels are ejected from the material when irradiated with a beam of X-rays as shown in Figure 2.6 [171]. These ejected electrons are called photoelectrons, and all detected photoelectrons are analysed by measuring their kinetic energy as described in Equation (2.1):

$$E_k = hv - E_B - \emptyset_0 \tag{2.1}$$

where E_k is the kinetic energy of the photoelectron, hv is the incident photon energy, E_B is the binding energy of the electron and $\emptyset_0$ is the work function of spectrometer. For each and every element, there will be a characteristic binding energy (BE) associated with each core atomic orbital, i.e. each element will give rise to a

characteristic set of peaks in the photoelectron spectrum at kinetic energies determined by the photon energy and the respective BEs.

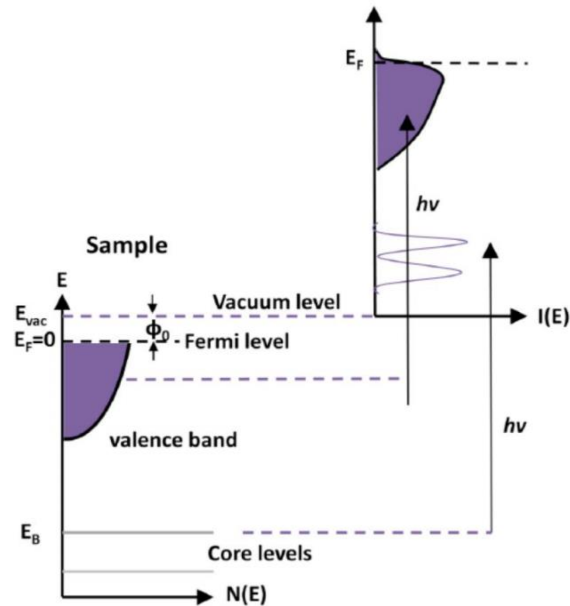

Figure 2.6: An illustration of the photoemission process showing the energy levels within the material [171].

2.2.2 Ultra-high vacuum

There are two basic conditions for the need of vacuum in electron spectroscopy: 1) To avoid electron scattering on gas molecules in the path from sample to an analyser and 2) To avoid attenuation and distortion of the spectra by surface contamination [172]. Therefore, it is critical for XPS system chamber to be kept at UHV condition with the pressure of 10^{-9} mbar or lower for operation so that the photoelectron scattering, and any surface contamination can be avoided for improving the analysis accuracy. Table 2.1 shows the variation of vacuum parameters which are the pressure, mean free path and maximum contamination for nitrogen molecule [172]. The SI unit of the pressure is Pascal, Pa (N/m^2), defined in the metric system. However, mbar and Torr are the units mostly found, where the relations between these units are 1 Pa = 1×10^{-2} mbar = 0.75×10^{-2} Torr; 1 Torr = 133.3 Pa = 1.333 mbar. According to

the kinetic theory of gases, the pressure defines the mean free path, L_{coll} between the two molecular collisions and can be expressed as:

$$L_{coll} = \frac{kT}{1.414\, P\sigma_{coll}}, \tag{2.2}$$

where k = 1.38 $\times 10^{-23}$ JK^{-1} is the Boltzmann constant, T (K) is the absolute temperature, P (Pa) is the pressure, and σ_{coll} (m^2) is the cross section for collision. Note that for hydrogen, the mean free path is about 1.5 times higher, and for argon, about 0.6 times lower than for nitrogen.

Condition (2) as stated above, however, requires that adsorption from the residual gas atmosphere does not produce an intolerable amount of contamination on the surface. The key to that requirement is the monolayer formation time, t_m. When every molecule striking a surface will remain there (sticking coefficient = 1), then the time to build up a monolayer (about 10^{15} atoms=cm^2) is given by:

$$t_m = \frac{4}{Nvd_m^2}, \tag{2.3}$$

where N is the density of the gas (molecules/cm^3), v is the molecular velocity, and d_m is the molecular diameter. Through the gas density, the monolayer formation time is inversely proportional to the pressure. For a highly reactive gas with a sticking coefficient = 1, the monolayer formation time t_m (s) = 1.7 $\times 10^{-6}$ / P(Torr). In the pressure range of 10^{-6} Torr (high vacuum), one monolayer contamination monolayer reduces the signal of the underlying surface, depending on its energy, by typically 10–50%. Furthermore, a species reacting with the surface will influence the peak shape by chemical bonding. For pressures in the lower 10^{-9} Torr range (UHV), the monolayer formation time increases to 20 min, a typical spectrum measurement time. To keep the

contamination below 10% of a monolayer, partial pressures of highly reactive gases (i.e., CO, O_2; H_2O) should be kept at least one or two orders of magnitude lower (i.e., less than 10^{-10} Torr) to ensure negligible contamination within the measurement time. The monolayer formation time increases inversely with the sticking coefficient, which varies, according to the specific reactivity of gas and surface.

The special materials and pumping procedure are required in order to achieve and maintain UHV conditions of XPS chamber. Vacuum chambers manufactured from high quality stainless steel with metal lining on it are widely used in UHV system. However, there are other construction materials that may also have advantages including aluminium, titanium, copper and specialised metals. The choice of this material is based on various factors such as lower corrosion rate (which can be further reduced in UHV condition), low outgassing rate, low vapour pressure (stainless-steel is characterised with a high melting point), cost effectiveness, easy fabrication techniques such as machining and magnetic shielding. Moreover, the seals and gaskets used between components in a UHV system must prevent even trace leakage. Therefore, nearly all such seals are all metal, with knife-edges on both sides cutting into a soft gasket, typically copper. These type of metal seals can maintain integrity to UHV ranges. Besides, the procedure to pump-down the vacuum chamber to UHV need to be well performed. A mechanical (roughing) pump is used to initially evacuate a vacuum system, as a first stage towards achieving high vacuum (HV) or UHV, where it allows pumping down the pressure for about 10^{-3} Torr, and then the turbomolecular pumps were used to achieve UHV regime. UHV conditions were then maintained using a combination of ion pumps, titanium sublimation pumps (TSP) and hydrogen getters. UHV pressures are measured via ion gauges, either a hot filament or an inverted magnetron type.

However, outgassing (from either internal surfaces or materials of construction) is a significant problem for UHV systems. Outgassing from internal materials is minimised by careful selection of those with low vapour pressures (e.g. glass, stainless steel, ceramics). Outgassing from surfaces is a subtler problem. At extremely low pressures, more gas molecules are adsorbed onto the walls that are floating in the chamber, so the total surface area inside a chamber becomes more important than its volume. Water vapour is a significant source of outgassing, especially whenever the chamber is opened to air since any water vapour present absorbs other contaminates and evaporates from surfaces too slowly to be fully removed while pumping at room temperature, but just fast enough to present a continuous level of background contamination. Removal of water and similar gases generally requires baking at 180 °C to 400 °C while vacuum pumps are running. During use, the walls of the chamber may be chilled using liquid nitrogen to further reduce outgassing. Hydrogen and carbon monoxide are the most common background gases present after baking from sources such as stainless steels. The typical vacuum parameters, including those used in XPS chamber are listed in Table 2.1.

Table 2.1: Vacuum parameters: pressure, mean free path and maximum contamination for nitrogen molecule [172].

Degree of vacuum	Pressure, P (Torr)	Mean free path, L_{coll} (m)	Maximum contamination, t_m (s/ML)
Atmsopheric	760	1×10^{-7}	1×10^{-9}
Low (rough or coarse)	1	1×10^{-4}	1×10^{-6}
Medium (fine)	1×10^{-3}	0.1	1×10^{-3}
High	1×10^{-6}	100	1
Ultra-high	1×10^{-10}	1×10^{6}	1×10^{4}

2.2.3 X-ray source

X-rays are generated by accelerating electrons emitted from a heated filament onto a metal anode with an applied voltage of 10–15 keV. These electrons, if attain sufficient energy, remove core electrons from the atom. Creating vacancies which are then filled by the higher energy electron, thus releasing energy in the form of X-rays.

The most common X-ray sources used in non-monochromatic XPS are equipped with Mg or Al anodes, often as a dual anode for alternative use. The characteristic Mg Kα radiation at 1253.6 eV and the Al Kα radiation at 1486.6 eV possess sufficiently high energies for core level excitation as well as a sufficiently low line width (< 1 eV) to yield XPS spectra with a fairly good resolution [172], [173]. The non-monochromatic X-ray source produces a main emission line together with minor lines at higher BE as shown in Figure 2.7 (a). The pattern of such satellites for Mg and Al is shown in Table 2.2. These satellites together with the Bremsstrahlung background, distort the spectra, the resolution of which is limited to the $K\alpha_{1,2}$ line width of Mg or Al (0.7 and 0.85 eV, respectively).

However, a better energy resolution and removal of the Bremsstrahlung background and the satellite peaks is achieved using a monochromator which selects a narrow line from the natural emission as shown in Figure 2.7 (b).

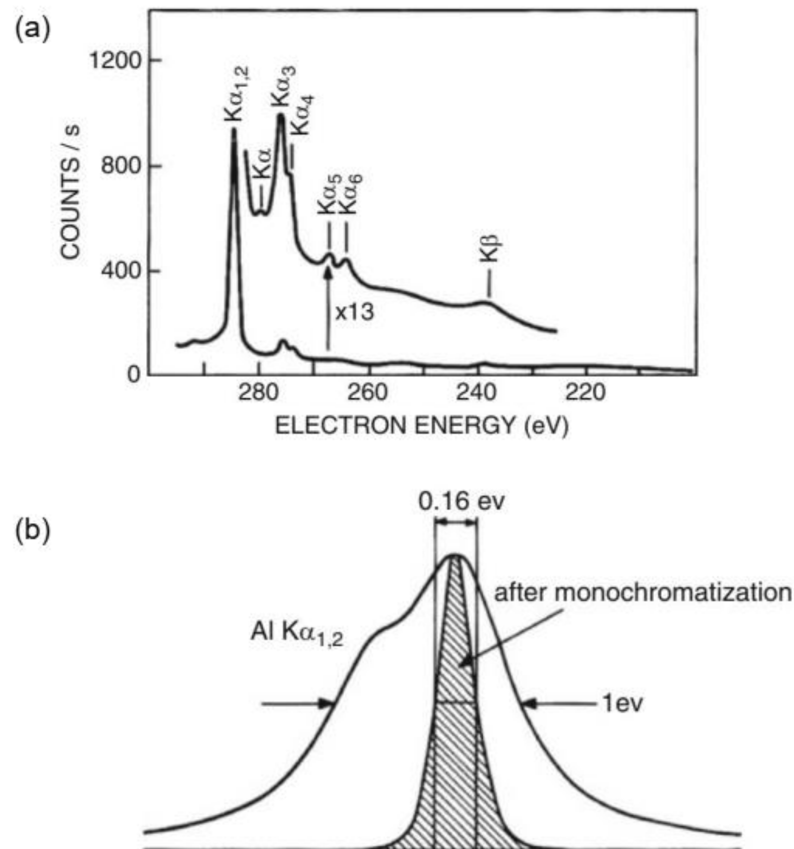

Figure 2.7: (a) Al X-ray satellites of the low binding energy side of a C 1s spectrum (without monochromator); (b) Action of a monochromator crystal on the Al $K\alpha_{1,2}$ radiation. The shadowed region is the excitation line shape with a full width at half maximum FWHM = 0.16 eV which puts a limit to the experimental resolution [172].

Table 2.2: X-ray satellite energies and intensities for Mg and Al sources [172], [173]

K lines		$\alpha_{1,2}$	α_3	α_4	α_5	α_6	β
Mg	Rel. intensity (%)	100	8.0	4.1	0.55	0.45	0.5
	Energy displacement (eV)	0	8.4	10.2	17.5	20.0	48.5
Al	Rel. intensity (%)	100	6.4	3.2	0.4	0.3	0.55
	Energy displacement (eV)	0	9.8	11.8	20.1	23.4	69.7

Figure 2.8 shows the diagram of monochromatic X-ray source where the source, monochromator crystal, and sample are placed on the circumference of a Rowland sphere of typically 0.5 m diameter. A bent quartz crystal (or several pieces) in combination with an Al anode is used for convenient Bragg law dispersion and for focusing the X-rays to the sample surface.

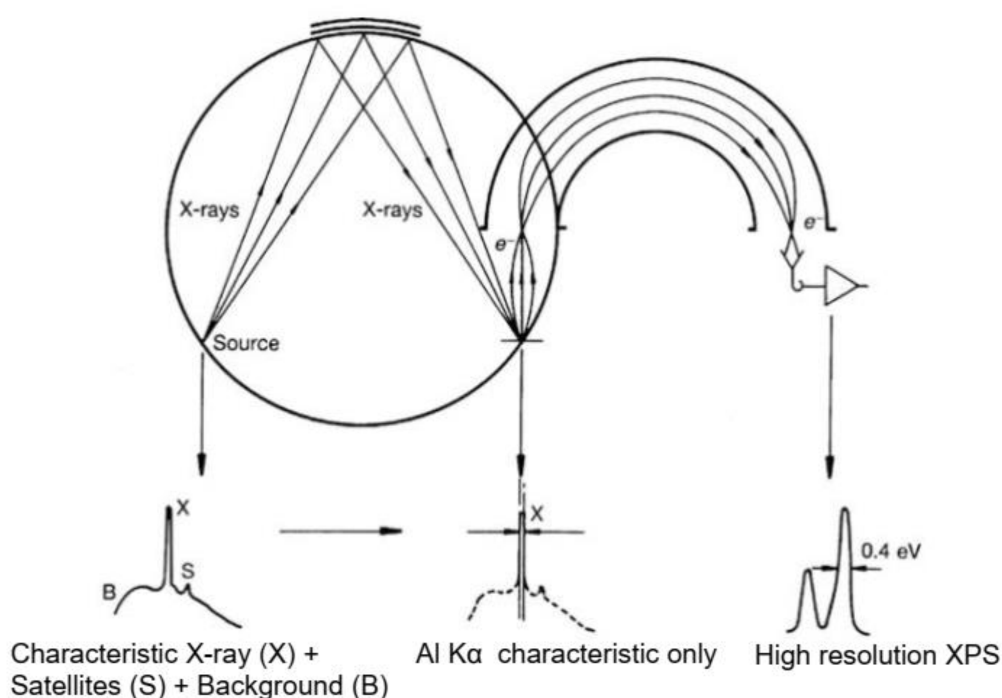

Figure 2.8: Monochromatic X-ray source provide high resolution XPS spectrum [172], [174].

2.2.4 Electron energy analyser

The spectrometer used in XPS can be divided into two parts, the analyser, which only allows electrons of a certain energy to pass through, and the detector, which counts the number of electrons that were allowed to pass through the analyser. Then, by sweeping across the possible kinetic energies, and counting at each point, a spectrum can be generated.

There are two types of electron energy analyser for XPS: the cylindrical mirror analyser (CMA) and the hemispherical sector analyser (HSA). The CMA is used when it is not important that the highest resolution is achieved. Meanwhile, spectral resolution plays an important role in XPS, and this led to the development of the HSA as a design of analyser with adequately good resolution. The addition of a transfer lens to the HSA and multichannel detection increase its sensitivity to the point where both high transmission and high resolution are possible. The CMA consists of two concentric cylinders, where inner is held at earth potential, whereas outer is ramped at a negative potential. An electron gun is often mounted coaxially within the analyser. On the other hand, the HSA, also known as a concentric hemispherical analyser (CHA), uses an electric field between two hemispherical surfaces to disperse the electrons according to their kinetic energy.

The HSA has the main advantage over other designs that it has 180° geometry which permits accurate focusing of the electrons without any distortion which in turn allows a well-defined angular and energy dispersion. The analyser's function can be divided into three parts which are (i) focusing by lens, (ii) dispersion and (iii) counting of the electrons. A lens or a series of lenses are in between the sample and the analyser. The desirable electrons to be counted are collected and focused on the entrance slit of

the analyser. In the process, the lens operates to accelerate or retard the electrons. At the entrance slit, they have the energy set by the potentials on the lens. The lens also allows the sample to be placed at a working distance from the entrance. The schematic diagram of Figure 2.9 shows a typical HSA configuration for XPS. The hemispheres with radii R_1 (inner) and R_2 (outer) are positioned concentrically, and potentials of V_1 and V_2 are applied to these spheres, respectively, with V_2 greater than V_1. Electrons injected tangentially at the input to the analyser will only reach the detector if their energy is given by:

$$E_k = kq\Delta V \tag{2.4}$$

$$\Delta V = \frac{V_1 R_1 + V_2 R_2}{2R_0}, \tag{2.5}$$

where the kinetic energy of the electrons is given by E_k, q is the charge of the electron, ΔV is the potential difference between outer and inner hemispherical plate potential difference between the outer and inner hemispherical plate and k is known as the spectrometer constant and depends upon the design of the analyser.

The CHA is typically operated in two different modes: constant analyser energy (CAE), also known as fixed analyser transmission, and constant retard ratio (CRR), also known as fixed retard ratio. In the CAE mode, electrons are accelerated or retarded according to user-defined pass energy. In the CRR mode, electrons are retarded to some user-defined fraction of their original kinetic energy as they pass through the analyser. In practice, in the CRR mode, the pass energy is proportional to kinetic energy, and so the relative resolution is constant throughout the energy range. In the CAE mode of operation, the absolute resolution remains constant throughout

the energy range of the scan, ensuring that XPS quantification is more reliable and emphasises the XPS peaks at the low kinetic energy (high BE) end of the spectrum.

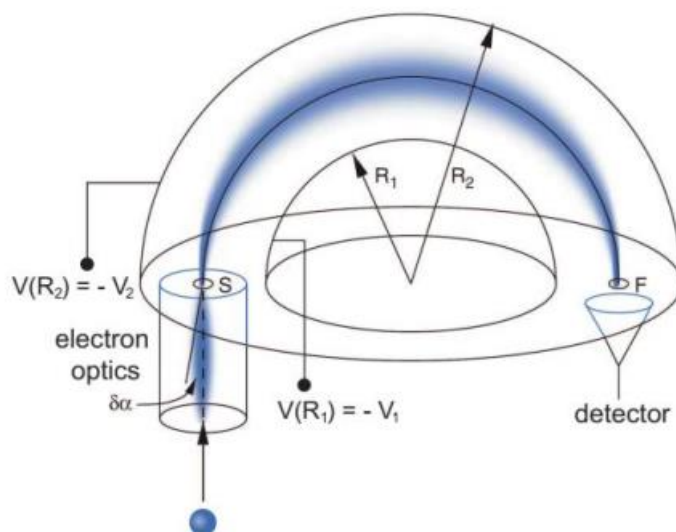

Figure 2.9: Schematic of a concentric hemispherical analyser. Both hemispheres are at a negative potential, with $V(R_2) < V(R_1)$, where $V_2 > V_1$ [175].

2.2.5 Detector

In most electron spectrometers, it is necessary to count the individual electrons arriving at the detector. To achieve this, electron multipliers are used in the XPS system. There are two types of electron multipliers commonly used: channel electron multipliers (CEMs, or channeltrons) and channel plates. A CEM is an electron detector which consists of a spiral-shaped glass tube with a conical collector at one end and a metal anode at the other. The internal walls of the detector are coated with a material which, when struck by an electron having more than some threshold kinetic energy, will emit many secondary electrons. Channeltrons can be capable of detecting up to about 3 x 10^6 counts/s. A channel plate consists of a disc having an array of small holes. Each of these holes behave as a small channeltron. The gain of an individual channel is much lower than that of channeltron; thus, it is common to use a pair of channel

plates in tandem. Chanel plates are used when it is necessary to detect data in two dimensions.

In the current work, XPS spectra were measured with both types of detectors; one containing an array of five CEMs and in another UHV system, an analyser containing a pair of channel plates mounted in front of a phosphor screen. The images of the main XPS systems used in this work are shown in Figure 2.10.

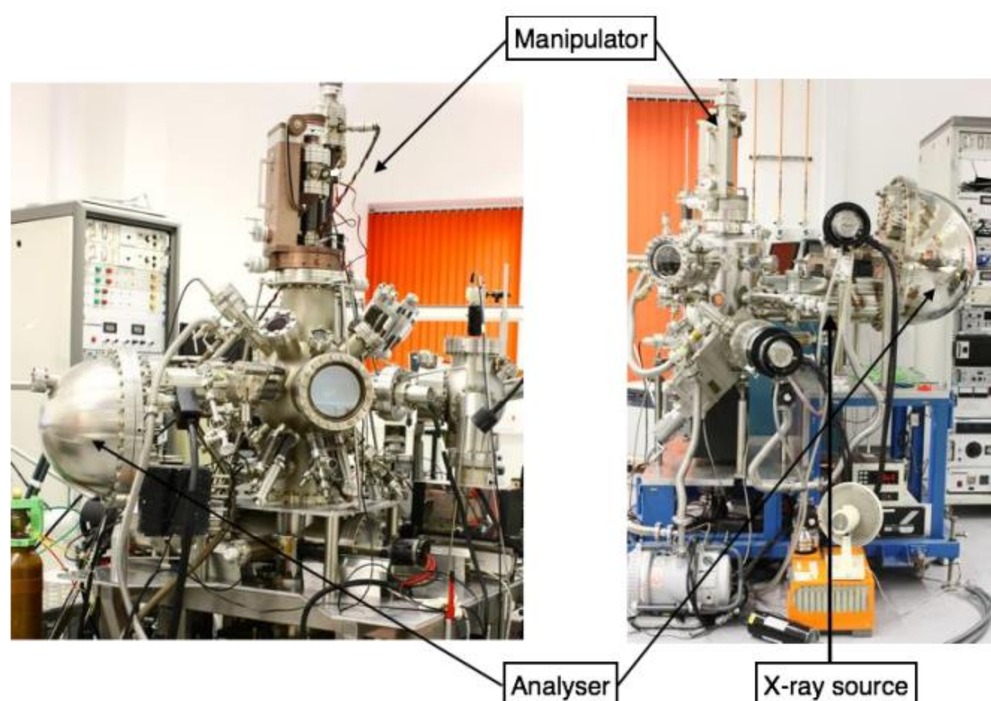

Figure 2.10: XPS system used in this work at the University of Liverpool, UK [176].

2.2.6 XPS resolution

Resolution in XPS is affected by three factors such as source width, sample's inherent linewidth and analyser's resolution. The contribution of intrinsic and instrumental effects to the experimentally observed linewidth can be expressed as [176]:

$$w_T^2 = w_S^2 + w_X^2 + w_A^2 , \tag{2.6}$$

where, w_T represents the measured FWHM of the XPS core line, w_S represents the FWHM (intrinsic or natural linewidth) of the sample's core level, w_X is the FWHM due to X-ray's source, and w_A is the FWHM due to analyser energy resolution. The w_S term is a physical property of the sample and represents the core electron hole lifetime, and as such is a constant. The lifetime varies depending on the core level. For example, for shallow core levels and valence levels, the hole lifetime is short, resulting in broad FWHM, while for deeper core levels, the hole lifetime is long, leading to sharp narrow FWHM. Another physical constant of the X-ray source is the incoming X-ray's natural line width. For a given experiment, different characteristic X-rays are generated by different materials so as to select a good anode, which in turn will improve the resolution. A monochromator can also be used to improve the line width. As compared to a non-monochromatic X-ray, various features such as small X-ray line widths, X-ray satellite lines removal and Bremsstrahlung's reduction are generally offered by the monochromatic X-ray system which results in the reduced incident X-ray's line width and hence improvement in the energy resolution. On the other hand, UV radiation which is produced by He excitation in a discharge tube has a source linewidth of 10 meV or less. In accordance with the following expression in Equation (2.7), the resolution for a hemispherical sphere, ΔE_A which is the FWHM contribution from w_A (see Equation (2.6)) generally depends both on the incoming photoelectrons angular divergence and the geometrical parameters [174]:

$$\Delta E_A = E_P \left(\frac{w}{4R_A} + \frac{\alpha^2}{2} \right), \tag{2.7}$$

where E_P is the pass energy of the HSA and relates to the central potential between the two concentric hemispheres, w is the average width of two slits used in the analyser, R_A represents the average radius of the analyser which consists of inner and

outer hemispheres, and α is the acceptance angle of the analyser. During the XPS measurements, the analyser is operated at constant pass energy to yield a constant absolute energy resolution ΔE_A.

2.2.7 Inelastic mean free path (IMFP)

Any spectroscopic technique based on the detection of photoelectrons is usually surface sensitive. The average distance an electron can travel before scattering inelastically (losing energy) is referred to the inelastic mean free path. The IMFP of escaping photoelectrons determines the depth sensitivity of the technique being used, and it is only on the order of a nanometer for most UV photoemission experiments. In XPS, the photoelectrons have kinetic energies up to approximately 1000 eV. The IMFP is controlled mainly by electron-electron interactions, which is described by the dielectric loss function but the dependency of the IMFP on kinetic energy shows a broad minimum in the range of energies accessible by XPS [177]. Figure 2.11 shows the so- called "universal curve" of the IMFP of electrons in a solid as a function of kinetic energy [177].

The emitted electron intensity (*I*) gets affected by material depth through which an electron possibly travels (*d*) and the mean free path (λ) according to the Beer-Lambert law:

$$I \propto e^{-\frac{d}{\lambda}}. \tag{2.8}$$

The Beer-Lambert law provides a clear correspondence between the intensity 1 to 0 of an electron being attenuated at a depth below the surface with its mean free path and its intensity when it reaches the surface: showing that the 95% of the collected signal

(i.e., the intensity of those photoemitted electrons reaching surface) comes from a depth within 3 λ of the surface.

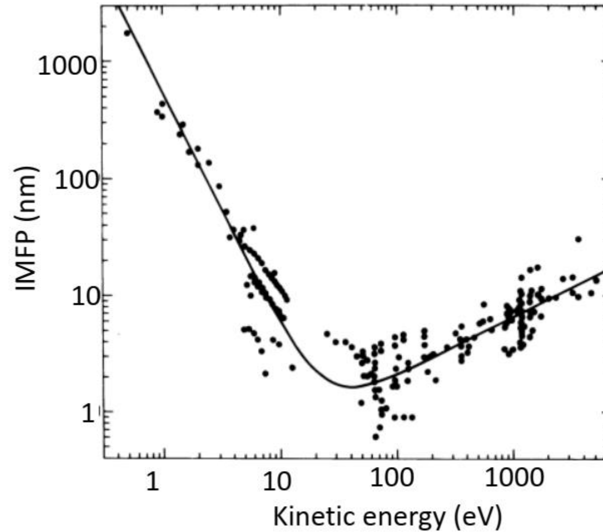

Figure 2.11: The "universal curve" of inelastic mean free path of electrons in a solid as a function of kinetic energy [177].

2.3 Variable angle spectroscopic ellipsometry (VASE)

2.3.1 Basic principle of VASE

Ellipsometry has been used typically to determine the thin film thickness and optical constants. Figure 2.12 shows the electric field vector of linearly polarised light which can be expressed with two basic orthogonal vectors, *p* and *s*. When the incidence polarised light beam hits on the surface of the sample, the resultant light beam is elliptically polarised. Then, it will be detected by an analyser to measure the wave function and the phase of the reflected beam comparing with the incidence beam. The ellipsometry measurement is related to the ratio of complex Fresnel reflection coefficients, ρ using Equation (2.9). There are two parameters used for each wavelength-angle combination Ψ (Psi) and Δ (Delta):

$$\rho = \frac{R_p}{R_s} = \tan(\Psi)\, e^{i\Delta}, \qquad (2.9)$$

where R_p and R_s are the complex reflection coefficients of light polarised parallel (p) and perpendicular (s) to the plane of incidence [178].

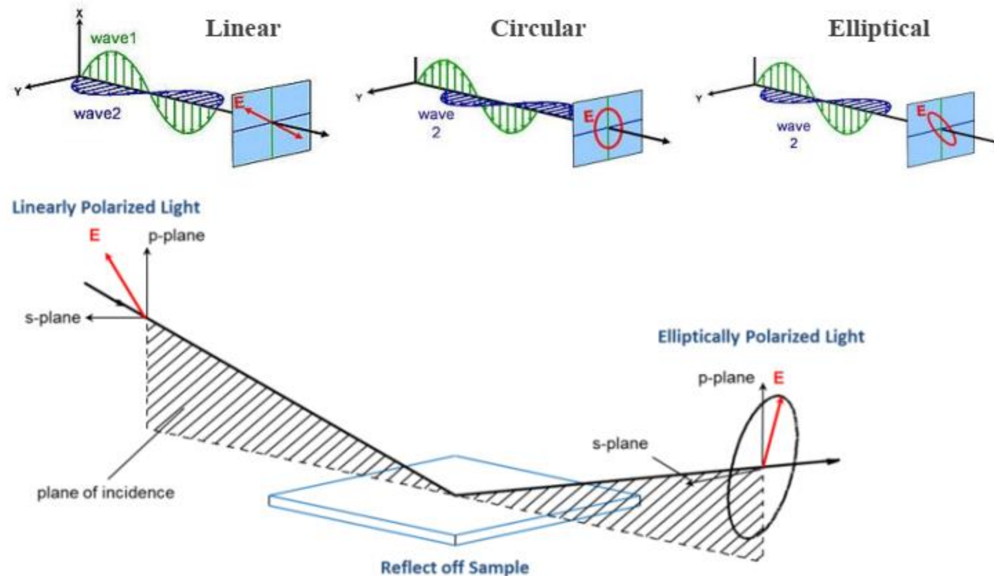

Figure 2.12: A simplified schematic showing the change from linearly polarised light to elliptically polarized light [178].

2.3.2 Data analysis

The full ellipsometry measurement results consist of a large quantity of raw data associated with the intensity and polarisation states of the reflected light over the range of wavelengths selected. These data allow the calculation of the values for ψ and Δ. These values can be used to obtain the properties of interest such as film thickness and the relative dielectric constants of the material. Therefore, data analysis is a very important part of spectroscopic ellipsometry (SE). The model-based analysis approach is summarised by the flowchart shown in Figure 2.13 [178]. The basic steps of this approach include:

i. SE data is measured on the sample.

ii. A layered optical model is built which represents the nominal structure of the sample. This model is used to “generate” SE data.

iii. Model fit parameters are defined, and then automatically adjusted by the software to improve the agreement between the measured and model-generated SE data. This is known as “fitting” the data.

iv. The results of the fit are evaluated. If the results are not acceptable, the optical model and/or defined fit parameters are modified and the data is fitted again.

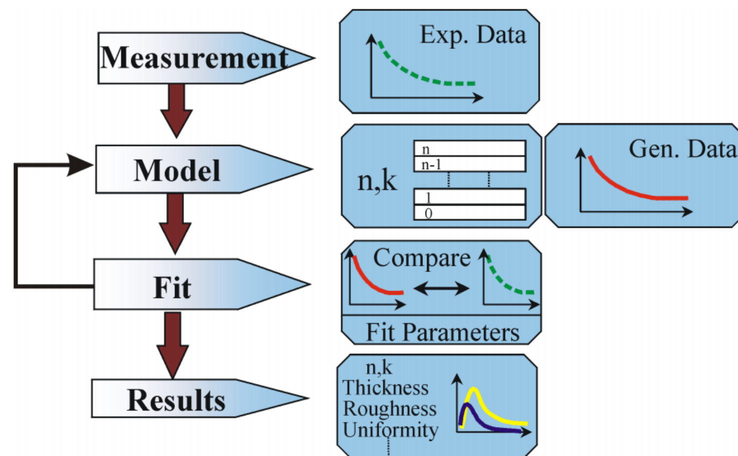

Figure 2.13: The SE data analysis flowchart [178].

The mean standard error (MSE) is a figure of merit, which is used to quantify the difference between the experimental and model generated data (Δ and ψ). The MSE is given by the following formula:

$$MSE = \frac{1}{2N-M}\sum_{i=1}^{N}\left[\left(\frac{\psi_i^{mod}-\psi_i^{exp}}{\sigma_{\psi,i}^{exp}}\right)^2+\left(\frac{\Delta_i^{mod}-\Delta_i^{exp}}{\sigma_{\Delta,i}^{exp}}\right)^2\right], \tag{2.10}$$

where N is the number of measured Δ and ψ pairs, M is the total number of valued fit parameters, $\sigma_{\psi,i}^{exp}$ and $\sigma_{\Delta,i}^{exp}$ are the standard deviations of ψ and Δ. It is always best to achieve the smallest MSE. However, a value below 10 signifies a good fit.

The instrument used in this work was a J. A. Woollam M2000UI VASE kit which uses a combination of deuterium & QTH lamps as the light source to achieve the wavelength region of 241-1700 nm. The data analysis was performed using the Woolam CompleteEASE software.

2.4 Atomic force microscopy (AFM)

An AFM is a type of high-resolution scanning probe microscope which provides powerful surface analytical to generate very high-resolution topographic images of surface down to molecular/atomic resolution. It can record topographic images as well as providing some information on nanoscale chemical, mechanical, electrical and magnetic properties. The AFM principle is based on the cantilever with a sharp probe (< 10 nm) that scans the surface of the sample at a very short distance (0.2-10 nm probe-sample separation) [179]. This flexible cantilever provides a force sensor and a force actuator. When the tip of the probe travels near to a surface, the forces between the tip and sample deflect the cantilever according to Hooke's law. The amount of force (F) between the probe and sample is dependent on the spring constant (k) or known as the stiffness of the cantilever and the distance between the probe and the sample surface or the cantilever deflection (x) as stated in Equation 2.11.

$$F = -kx. \tag{2.11}$$

If the cantilever spring constant is smaller than the stiffness of the surface (typically 0.1-1 N/m), causing the cantilever to bend and this deflection can be

monitored by an optical detection technique which consists of laser and position sensitive photodetector. The laser beam is focused on the back of the AFM cantilever so that the reflected beam can be detected by the position sensitive photodetector. The cantilever deflections are precisely monitored while a scan is performed on a non-uniform surface. The motion across the sample surface is controlled by a feedback loop and a piezoelectric scanner [179].

The dominant interactions at short probe-sample distances in the AFM are Van der Waals interactions. The probe usually experiences repulsive Van der Waals during contact with the sample (contact mode) or attractive Van der Waals as the tip moves further away from the surface (non-contact mode). There are three primary imaging modes in an AFM [179]:

1) Contact mode AFM (< 0.5 nm probe-surface separation)

   The contact mode where the tip scans the sample in close contact with the surface is the common mode used in the force microscope. The force on the tip is repulsive. By maintaining a constant cantilever deflection (using the feedback loops) the force between the probe and the sample remains constant, and an image of the surface is obtained. The advantages of using contact mode AFM are fast scanning, appropriate for rough samples, and in friction analysis. However, few problems with contact mode are caused by excessive tracking forces applied by the probe to the sample. The effects can be reduced by minimising tracking force of the probe on the sample, but there are practical limits to the magnitude of the force that can be controlled by the user during operation in ambient environments.

2) Non-contact mode AFM (0.1-10 nm probe-surface separation)

The probe does not contact the sample surface but oscillates above the adsorbed fluid layer on the surface during scanning. Using a feedback loop to monitor changes in the amplitude due to attractive Van der Waals forces, the surface topography can be measured. The advantages of non-contact mode include a very low force exerted on the sample (10^{-12} N) and extended probe lifetime. However, it generally has lower resolution, contaminant layer on the surface can interfere with oscillation, and need an ultra-high vacuum to have the best imaging.

3) Intermittent contact or tapping mode AFM (0.5-2 nm probe-surface separation) This mode of imaging is similar to contact mode AFM, but the cantilever oscillates at its resonant frequency. The probe gently taps on the sample surface during scanning, contacting the surface at the bottom of its swing. It is possible to obtain an image on the surface by maintaining constant oscillation amplitude and a tip-sample interaction. This technique overcomes most of the limitations caused by both contact mode and the non-contact mode such as high resolution and less damage to the sample surface.

In this experimental work, the AFM is operated in contact mode using a Veeco di Innova instrument.

2.5 High-resolution transmission electron microscopy (HR-TEM)

The HRTEM is one of the most powerful tools used for characterising nanomaterials, and it is indispensable for nanotechnology. With the assistance of energy dispersive X-ray Spectroscopy (EDS) and Electron Energy-Loss Spectroscopy (EELS), the TEM is a versatile and comprehensive analysis tool for characterising the chemical and electronic structure at nano-scale [180]. The main advantage of a TEM

over other microscope is that it can simultaneously provide information in real space (in the imaging mode) and reciprocal space (in the diffraction mode).

The basic principle of TEM is quite similar to their optical counterparts, the optical microscope. The major difference is that in TEM, a focused beam of electrons instead of light is used to image and achieve information about the structure and composition of the specimen. The TEM works by passing electrons through the sample of interest. Electrons from a high-energy electron source are accelerated to an energy range of 0 eV to a few hundred keV. The electrons then are collimated through a condensing electromagnetic lens. The beam of electrons passes through another condensing lens and aperture to narrow down and straighten the electron beam. The beam passes through the sample, and the electrons that are transmitted through are passed through an objective lens and aperture and projected onto a fluorescent screen, where light is generated, allowing the user to see the image. Figure 2.14 illustrates a typical TEM.

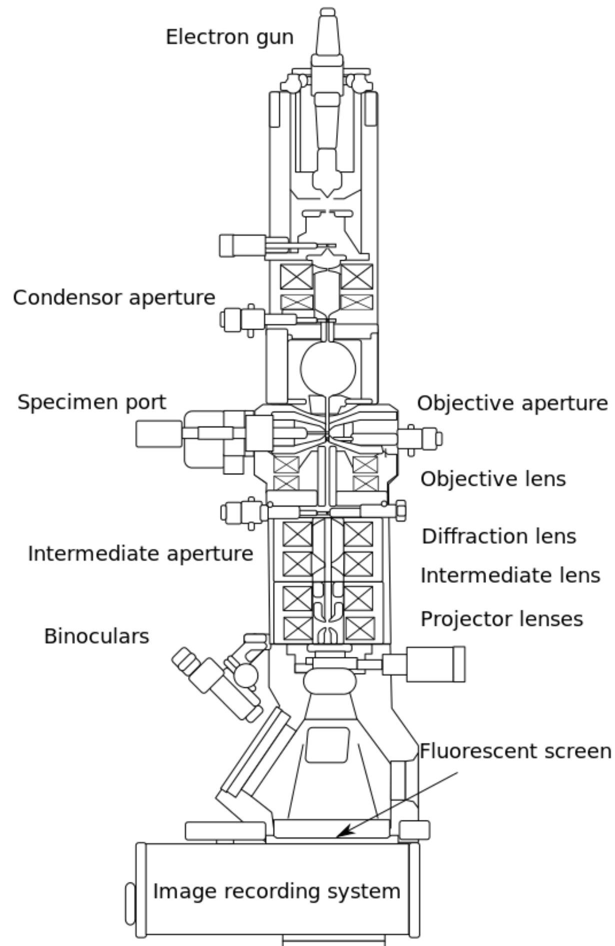

Figure 2.14: A schematic of a typical transmission electron microscope [181].

2.6 Electrical measurement

2.6.1 Current-Voltage measurements

The current-voltage (IV) measurement represents the relationship between the voltage applied across an electrical device and the current flowing through it. It is one of the most common methods of determining how an electrical device functions in a circuit. Key properties of electronic devices can also be extracted from the shape and details of the curve, enabling greater insight into their operation.

The conduction mechanisms in dielectric films can be classified into two types: (i) electrode-limited and (ii) bulk-limited. The electrode-limited conduction

mechanisms include Schottky (SE) or thermionic emission (TE), Fowler-Nordheim (FN) tunnelling, direct tunnelling (DT), and thermionic-field emission (TFE) which depend on the electrical properties at the electrode-dielectric contact. On the other side, the bulk-limited conduction mechanisms depend on the properties of the dielectric itself such as Poole-Frenkel (PF) emission, hopping conduction, ohmic conduction, space-charge-limited current (SCLC), ionic conduction, and grain-boundary-limited conduction. Most common conduction mechanisms are shown in Figures 2.15 and 2.16.

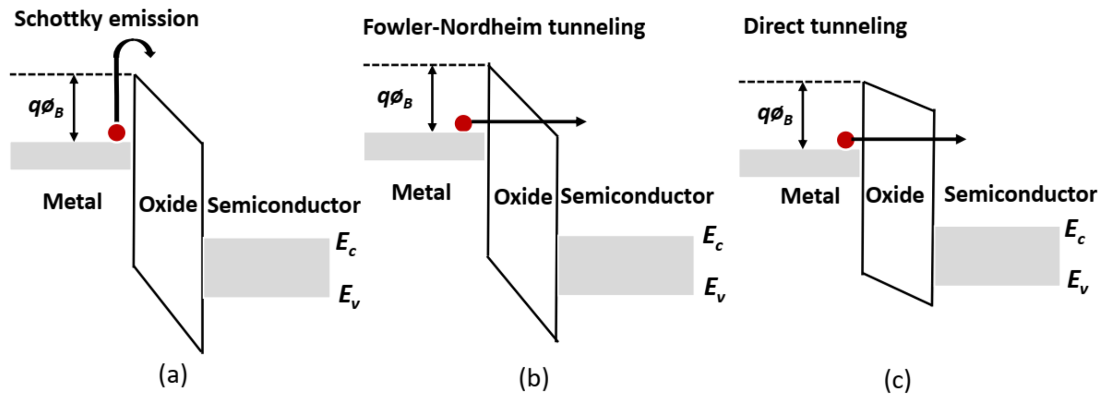

Figure 2.15: MOS band diagrams showing several electrode-limited conduction mechanisms (a) Schottky emission, (b) Fowler-Nordheim tunnelling and (c) direct tunnelling.

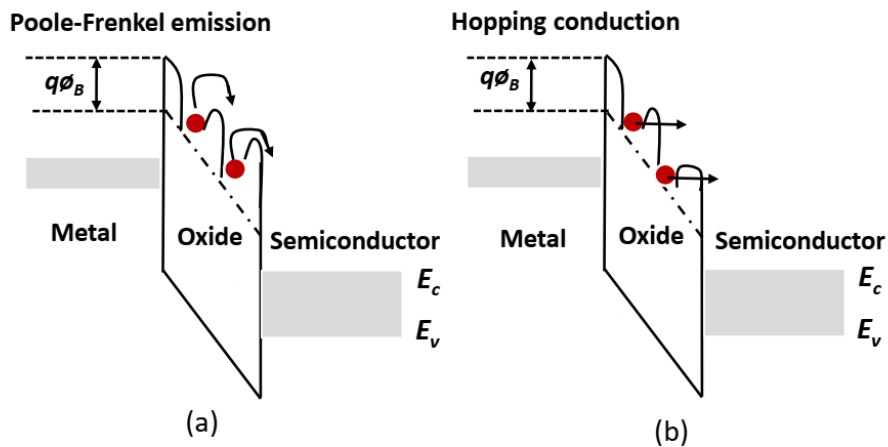

Figure 2.16: MOS band diagrams showing several bulk-limited conduction mechanisms: (a) Poole-Frenkel emission and (b) hopping conduction.

Several conduction mechanisms are explained below:

i) Schottky or thermionic emission

This SE conduction mechanism happens when the electrons in the metal electrode can overcome the energy barrier at the metal-oxide interface to go to the oxide if they can obtain enough energy provided by thermal activation [182]. This phenomenon is illustrated in Figure 2.15 (a). The current due to thermionic emission is highly dependent on the temperature. The energy barrier at the metal-dielectric interface will be lowered for charge emission in the presence of an electric field due to the Schottky effect or Schottky barrier lowering. The Schottky Emission can be expressed as in Equations (2.12) and (2.13).

$$J_{SE} = A^{*} T^{2} \exp\left[\frac{-q\left(\emptyset_{B} - \sqrt{qE/4\pi\varepsilon_{r}\varepsilon_{0}}\right)}{kT}\right] \tag{2.12}$$

$$A^{*} = \frac{4\pi q k^{2} m^{*}}{h^{3}} = \frac{120 m^{*}}{m_{0}} \tag{2.13}$$

where J is the current density, A^{*} is the effective Richardson constant, m_0 is the free electron mass, m^{*} is the effective electron mass in dielectric, T is the absolute temperature, q is the electronic charge, $q\emptyset_B$ is the Schottky barrier height, E is the electric field across the dielectric, k is the Boltzmann's constant, h is the Planck's constant, ε_0 is the permittivity of vacuum, and ε_r is the optical (or the dynamic) dielectric constant.

ii) Fowler-Nordheim tunnelling

The FN tunnelling occurs when the applied electric field is large enough so that electrons penetrate through a triangular potential barrier into the conduction band of oxide [182] as illustrated in Figure 2.15 (b). Quantum mechanics predicts that the

electron wave function will penetrate through the potential barrier when the barrier is thin enough (<10 nm). This mechanism was first proposed by Fowler and Nordheim [183] and then named after them. The leakage current mechanism is related to the quality of oxide where FN tunnelling can be observed in good quality oxide. Moreover, both band gap and the permittivity of the dielectrics influence the quality of oxides Generally, the larger the band gap, the smaller the permittivity, better the oxide; e.g. Al_2O_3 and SiO_2 are very good oxides. The expression of FN tunnelling current is as stated in Equation (2.14) [177].

$$J_{FN} = \frac{q^3 E^2}{8\pi h q \emptyset_B} \exp\left[\frac{-8\pi(2qm^*)^{1/2}}{3hE} \emptyset_B^{3/2}\right], \tag{2.14}$$

where m^* is the electron effective mass in the dielectric, and the other notations are the same as defined above. To extract the tunnelling current, the IV characteristics of the device is measured at very low temperature, where the thermionic emission is suppressed, and the tunnelling current is dominant. For FN tunnelling, a plot (J/E^2) versus $1/E$ should be linear. The slope (V/cm) of the FN plot can be expressed as in Equation (2.15) and is also a function of electron effective mass (m^*) and barrier height (ϕ_B).

$$\text{slope} = -6.83 \times 10^7 \sqrt{\left(\frac{m^*}{m_0}\right)} \emptyset_B^{\frac{3}{2}} \tag{2.15}$$

iii) Direct tunnelling

Direct tunnelling occurs when electrons penetrate through a triangular potential barrier (very ultra-thin oxide layer <3.5 nm) when the small voltage is applied [182] as illustrated in Figure 2.15 (c). The expression of direct tunnelling current density is stated in Equation (2.16).

$$J_{DT} = \frac{q^3 E^2}{8\pi hq\emptyset_B} \exp\left[\frac{-8\pi(2qm^*)^{1/2}}{3hE} \emptyset_B^{3/2}\right] \tag{2.16}$$

iv) Poole-Frenkel emission

The PF emission involves a mechanism due to field-enhanced thermal excitation of trapped electrons into the conduction band of the oxide [182] as shown in Figure 2.16 (a). PF tunnelling can be observed in poor quality oxide which contains a high concentration of defects and impurities which cause additional energy states close to the band edge called traps. These traps restrict the current flow because of a capture and emission process. The current density for PF can be obtained by,

$$J_{PE} = q\mu N_c E \exp\left[\frac{-q\left(\emptyset_T - \sqrt{qE/\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right] \tag{2.17}$$

where μ is the electron drift mobility, N_c is the density of states in the conduction band, $q\emptyset_T$ is the trap energy level, and the other notations are the same as defined above. This PF conduction mechanism is often observed at high temperatures and high electric field since it is owing to the thermal activation under an electric field. For PF emission, a plot In(J/E) versus $E^{1/2}$ should be linear, where the trap barrier height can be extracted from the intercept of the PF plot and the ε_r can be determined from the slope of PF plot.

$$\text{slope} = \frac{q}{kT}\sqrt{\left(\frac{q}{\pi\varepsilon_r\varepsilon_0}\right)}\ . \tag{2.18}$$

v) Hoping conduction

Hopping conduction is due to the tunnelling effect of trapped electrons, i.e. “hopping” from one trap site to another in dielectric films, where it usually occurs at very low voltage and high temperatures [182]. The schematic energy band diagram of

hopping conduction is shown in Figure 2-16 (b). The current density for hoping conduction can be expressed as

$$J = qanv \exp\left[\frac{qaE}{kT} - \frac{E_a}{kT}\right] \tag{2.19}$$

where a is the mean hopping distance, n is the electron concentration in the conduction band of the dielectric, v is the frequency of the thermal vibration of electrons at trap sites, and E_a is the activation energy; the other terms are as defined above.

vi) Space-charge-limited current

The SCLC mechanism results from carrier injection into the insulator, where no compensating charge is present [184]. For structures where carriers can readily enter the insulator and freely flow through the insulator, one finds that the resulting current and carrier densities are much higher. The density of free carriers causes a field gradient, which limits the current density. This situation occurs in lowly doped semiconductors and vacuum tubes. A typical JV characteristic plotted in the log-log scale for SCLC is bounded by three limited curves, namely Ohm's law ($J_{Ohm} \propto V$), traps-filled limit (TFL) current ($J_{TFL} \propto V^2$), and Child's law ($J_{Child} \propto V^2$) as in following equations:

$$J_{Ohm} = qn_0\mu\frac{V}{d} \tag{2.20}$$

$$J_{TFL} = \frac{9}{8}\mu\varepsilon\theta\frac{V^2}{d^3} \tag{2.21}$$

$$J_{Child} = \frac{9}{8}\mu\varepsilon\theta\frac{V^2}{d^3} \tag{2.22}$$

where n_0 is the concentration of the free charge carriers in thermal equilibrium, V is the applied voltage, d is the thickness of thin films, ε is the static dielectric constant, θ is the ratio of the free carrier density to total carrier (free and trapped) density.

In this work, the *IV* measurements were performed on semiconductor devices with MOS-capacitor and MOSFET structures using the B1500A semiconductor parameter analyser. The current mechanisms such as FN tunnelling, FP emission and SCLC were analysed for GaN MOS capacitors with different gate dielectric layers (Ta_2O_5, ZrO_2, Al_2O_3 and MgO). The performance of GaN MOSFET can be obtained in term of its leakage current, threshold voltage and subthreshold voltage swing.

2.6.2 Capacitance-Voltage measurements

The capacitance-voltage (*CV*) measurements are the most frequently used electrical technique in studying gate-oxide quality in detail. The device parameters can be extracted from the *CV* measurement such as oxide thickness, flatband voltage, threshold voltage, fixed oxide charge, interface trap charge density. *CV* measurements are performed using two simultaneous voltage sources: an applied AC voltage signal and a DC voltage. The AC voltage bias is necessary for capacitance measurement as it provides a small signal bias, while DC voltage bias performs sampling of the material at different depths in the device. Figure 2.17 shows an ideal *CV* characteristic of a *p*-type MOS capacitor, which consists of three modes of operation, accumulation, depletion and inversion as discussed in Chapter 1 of the thesis. For *p*-type semiconductor, when a negative voltage is applied between the metal gate and the semiconductor, the majority carriers (holes) in the substrate are attracted towards the gate and accumulate at the interface between the semiconductor and the oxide. Therefore, the oxide capacitance can be measured in the strong accumulation region.

When a positive voltage is applied between the gate and the semiconductor, the majority carriers are repelled away from the oxide-substrate interface and form a depletion layer under the oxide until the maximum depth of the depletion layer is obtained. Thus, the measured capacitance is regarded as the sum of the oxide capacitance and the depletion capacitance in series. As the gate voltage increases beyond the threshold voltage, the positive gate voltage generates electron-hole pairs and attract the minority carriers (electrons) towards the gate which form the inversion layer. The *CV* curve for an *n*-type MOS capacitor is analogous to a *p*-type curve but has accumulation capacitance for positive bias and inversion capacitance for negative bias.

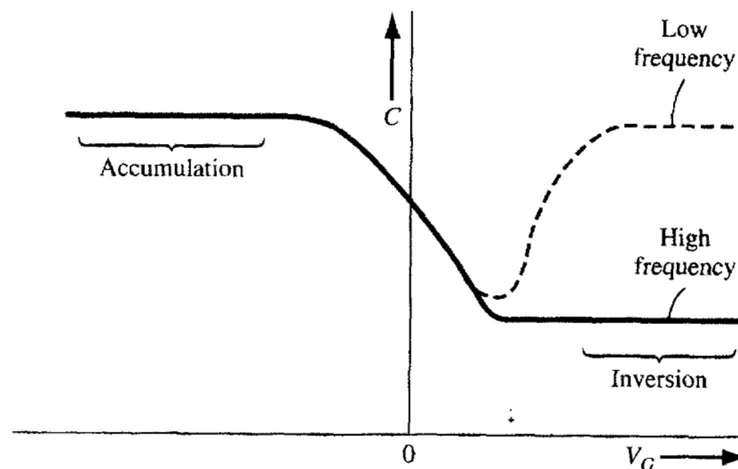

Figure 2.17: Idealized low-frequency and high-frequency CV plots of a MOS capacitor (p-type substrate) [21].

The MOS structure is also affected by the existence of charges in the insulator, and at the interface between the oxide and the semiconductor. There are four possible types of oxide charges, Q_{ox} associated with thermally oxidised silicon system as illustrated in Figure 2.18 [185].

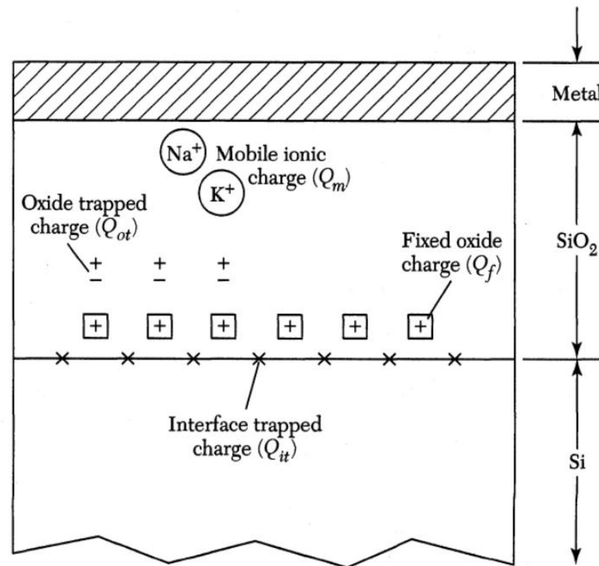

Figure 2.18: Terminology for charges associated with thermally oxidised silicon [185].

1) Fixed oxide charge, Q_f – positive charge, primarily due to structural defects. These can be introduced as a result of incomplete oxidation process depending on oxidation ambient and temperature, cooling conditions, and Si orientation. This charge is fixed and cannot be charged or discharged over a wide variation of surface potential. The number of charges is usually denoted N_f in a unit of cm^{-2} (per unit area).
2) Mobile ionic charge, Q_m – primarily due to ionic impurities such as lithium (Li^+), sodium (Na^+), potassium (K^+), and possibly hydrogen (H^+). They give rise to voltage-dependent shifts in threshold voltage exacerbated by temperature rises.
3) Interface trapped charges, Q_{it} – positive or negative charges, due to (i) structural, oxidation-induced defects, (ii) metal impurities, (iii) other defects caused by radiation or similar bond-breaking processes. They are located at Si/oxide interface. Unlike fixed charge or trapped charge, the interface trapped charges are electrically active defects with an energy distribution throughout the Si band gap. They act as generation/recombination centres and contribute to leakage current,

low-frequency noise, reduced mobility, drain current, and transconductance. This charge type is also known as surface states, fast states or interface states.

4) Oxide trapped charge, Q_{ot} – positive or negative due to holes or electrons trapped in the bulk of oxide. Trapping can be caused by ionising radiation, avalanche injection or other similar processes.

2.7 Conclusion

This chapter outlines key material deposition methods used to fabricate thin dielectric films and MIS and HEMT devices investigated in this work: sputtering and atomic layer deposition. The basic principles of X-ray photoelectron spectroscopy and variable angle spectroscopic ellipsometry have been presented, including different elements of the XPS system and VASE modelling by Complete EASE software. Furthermore, the atomic force microscopy and transmission electron microscopy techniques were described. The electrical characterisation techniques, such as current-voltage and capacitance-voltage have been presented detailing electrode- and bulk-limited conduction mechanisms studied in detail in Chapter 5 of the thesis. The various charges present in the oxide and at oxide/semiconductor interface are listed and discussed following explanation of capacitance-voltage characteristics. This chapter gives foundation for understanding the data and analysis presented in Chapters 3-6.

CHAPTER 3

High-k Dielectrics on Si and Ge

3.1 Introduction

The aggressive scaling in the gate oxide thickness of metal-oxide-semiconductor field effect transistors (MOSFETs) became increasingly difficult as the conventional SiO_2 approached its fundamental limit. Decreasing gate dielectric thickness of SiO_2 produced unacceptable leakage current due to direct tunnelling of electrons through the layer, which limited the device performance and reliability [3]. The problem of leakage current can be mitigated with the introduction of high dielectric constant (high-*k*) materials, where the requirement of thicker high-*k* materials could reduce electron tunnelling, as well as a higher permittivity could provide very low equivalent oxide thickness (EOT). Therefore, the replacement of SiO_2 gate oxide with high-*k* materials which are compatible with complementary metal-oxide-semiconductor (CMOS) process requirement has attracted much attention and became a subject of interest for many researchers in the past decade.

Rare earth (RE) oxides have emerged as the promising high-*k* candidates due to their relatively high dielectric constants, large energy band gaps, and good thermodynamic stability [35]. RE oxides have been previously studied including Y_2O_3 [36], [37], Pr_2O_3 [38], Gd_2O_3 [39], Lu_2O_3 [40], [41], La_2O_3 [42]–[46], Er_2O_3 [47], [48] and Tm_2O_3 [49]–[55]. Among them, Tm_2O_3 has interesting properties of a high dielectric constant of k ~16 [63], an energy band gap of E_g ~5.77 eV [64], high effective barriers for electrons (CBO=2.3 eV) and holes (VBO=3.1 eV) [52], and a low reactivity with the Si substrate [53]. As previously mentioned, band offset relative to

Si and band gap are the most important parameters for a gate dielectric in determining the level of the gate leakage current and assessing high-*k* gate dielectric in future CMOS device technology. The gate leakage current mechanisms for insulator films typically are direct tunnelling (DT) and Fowler-Nordheim (FN) tunnelling [186]. The leakage current is usually dominated by FN tunnelling which depends exponentially on the barrier height (this usually occurs when the gate dielectric thickness is >4 nm) [186]. Therefore, it is very crucial to select a high-*k* material with large band gap as well as a sufficiently large offsets for conduction and valence bands to have a sufficiently high barrier height for both electrons and holes and hence a low leakage current.

In addition, high-*k*/metal gate stacks have been implemented in MOSFETs instead of the conventional SiO_2/poly-Si gate stacks for scaling the EOT in order to supress not only the gate leakage current but also the short-channel effect (SCE) and the threshold voltage variability. As previously mentioned in Chapter 1, the excess gate leakage currents due to direct tunnelling through ultra-thin gate oxides can be reduced by using the high-*k* materials as a gate dielectric while maintaining a small EOT. Since SCE is proportional to the oxide thickness, therefore it can be suppressed by EOT scaling with high-*k*/metal gate. It has been reported that *n*FETs with high-*k*/metal gate stacks show more than 25% improvement in drive current compared with the conventional SiO(N)/poly-Si baseline. In addition, since the EOT has been scaled to <1.1 nm, it enables better SCE [187]. Moreover, the random threshold voltage variation is also proportional to the oxide thickness. Hence, the EOT scaling also directly leads to suppression of random threshold voltage variation.

Hf-based high-*k* dielectrics have been first introduced at the 45 nm node to replace the silicon oxynitride (SiON). In state-of-the-art high-*k*/metal gate CMOS

technology, the gate dielectric usually consists of a bilayer or trilayer dielectric stack, where each layer is personalised to achieve one or more design goals of the gate stack [29], [30], [188], [189]. An interfacial layer (IL) is integrated at the bottom of the gate stack, in direct contact with the underlying Si, with the purpose of ensuring high electrical quality of the interface with the channel. Figure 3.1 illustrates the Hf-based high-*k*/metal gate technology consisting of a multilayer stack where each layer performs different function. The IL consists of a sub-nm SiO_x layer which is grown by chemical oxidation. The main layer in the dielectric stack also known as bulk high-*k* layer to differentiate it from the thinner IL is composed of the high-k oxide (e.g. HfO_2) which is mainly responsible for EOT scaling and gate current control. In gate-first integration schemes, a thin capping layer which is often integrated between the main high-*k* layer and the metal electrode with the purpose of modulating the effective workfunction (EWF) and obtaining symmetric *n*FET and *p*FET threshold voltages, which is necessary for CMOS logic circuit operation. The most developed approach to threshold voltage control involves the integration of dielectric capping layers on top of the SiO_x/HfO_2 stack, where *n*FET and *p*FET gate stacks employ two different capping layers and one common gate metal, typically TiN. The high-temperature dopant activation annealing is used to drive diffusion of the metal atoms from the capping layer to the interfacial layer, where the formation of interfacial dipoles results in a shift of the EWF in the positive or negative direction, depending on the choice of material for the capping layer [190]. Suitable materials for nFETs include reactive oxides such as La_2O_3 and MgO, while for *p*FETs, materials such as Al_2O_3, which are much less reactive are preferred. In gate-last process flows, instead, capping layers are not employed, and threshold voltage control is obtained via integration of different gate metals for *n*FETs and *p*FETs.

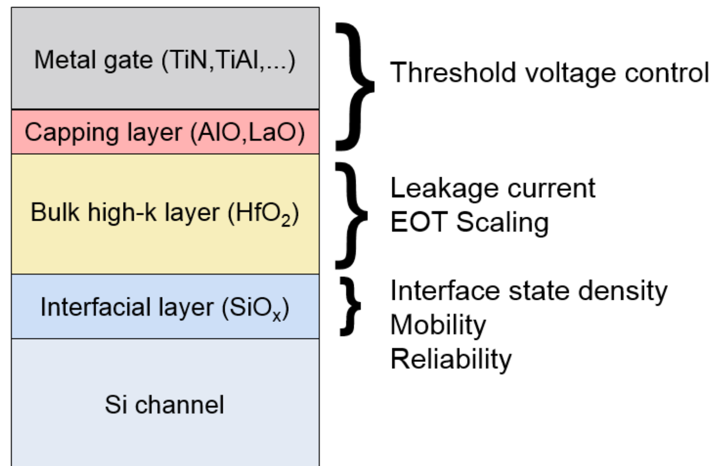

Figure 3.1: The schematic diagram of Hf-based/metal gate stack that has been integrated in CMOS technology since 2007 [191].

Further EOT scaling in Hf-based gate stack which is achieved via reduction of the SiO_x IL thickness remains challenging due to strong degradations in channel mobility [31], [190], threshold voltage control [192] and device reliability [32]. Therefore, the introduction of high-*k* ILs is a possible solution to extend the scalability of Hf-based gate stacks. Kakushima *et al*. [43] reported that the interfacial layer of La-silicates can be obtained at La_2O_3/Si interface with lower EOT and interface state density, D_{it} of 0.48 nm and 10^{11} cm^{-2}eV^{-1}, respectively. Kawanago *et al*. [193] have also investigated the impact of oxygen incorporation in La-silicate at La_2O_3/Si interface, where the effective mobility, μ_{eff} in MOSFET has been improved by oxygen annealing (340 °C for 30 min) and subsequent forming gas anneal (FGA) at 800 °C and 420 °C for 30 min without increase in EOT. Moreover, other study obtained a lower EOT of 0.62 nm and an μ_{eff} of 155 cm^2/V with a direct contact La-silicate/Si interface structure [194]. The lower EOT of 0.73 nm with fairly good electrical characteristics have been demonstrated by controlling the oxygen partial pressure precisely [195]. The main problem with La_2O_3 is the excess growth of the silicate layer after annealing which is found to increase EOT [58]. In addition, the drawback of La_2O_3 is its hygroscopic nature as well as high reactivity with Si. Recently, several

studies have been done on the integration of Tm-silicate (TmSiO) as an IL [28], [59]–[62], [191], [196]. The formation of TmSiO IL provides a relatively high dielectric constant (k = 10–12) [53] which is similar to LaSiO [43]. It has been demonstrated recently that TmSiO IL formation at post deposition annealing (PDA) at 550 °C provided the optimal electrical properties in terms of EOT, interface state density, and channel mobility [61]. Both MOS capacitors and MOSFETs employing TmSiO/Tm_2O_3 gate stack have been found to outperform SiO_x/HfO_2 devices, achieving EOT of the IL of 0.25 ± 0.15 nm while preserving excellent electrical quality at the interface with Si, an interface state density of 0.7–2×10^{11} $cm^{-2}eV^{-1}$ at flat-band condition, the *n*FET and *p*FET subthreshold slopes of 70 mV/dec and the inversion layer mobility 20% higher than reference SiO_x/HfO_2 devices: 230 cm^2/Vs for *n*FET and 60 cm^2/Vs for *p*FET devices, at inversion charge density of 10^{13} cm^{-2} and total capacitance equivalent thickness (CET) of 1.6 nm [61]. Further study on the MOS capacitors integrating a TmSiO IL formed at varying PDA temperatures between 500–900 °C also confirmed that the temperature at 500–550 °C provided the lowest EOT of 0.1–0.3 nm and interface state density at flatband condition lower than 2×10^{11} $cm^{-2}eV^{-1}$ as compared to devices employing LaSiO IL [59]. It has also been reported that the TmSiO/HfO_2 dielectric stack is compatible with common threshold voltage control techniques employed in gate-first and gate-last processes demonstrating that the flatband voltage can be set from -1 V to +0.5 V by proper choice of gate metal, while a shift of 150-400 mV in both the positive and negative direction is achievable by means of integration of Al_2O_3 or La_2O_3 capping layers [196]. It has been shown that TmSiO/HfO_2/TiN MOSFETs can achieve ~20% higher channel mobility compared with the conventional SiO_x/HfO_2 dielectric stack [191]. Furthermore, an optimised annealing condition at 550 °C has been reported leading to gate leakage

current density comparable with state-of-the-art SiO_x/HfO_2 *n*FETs (0.7 A/cm^2 at a gate bias of 1 V) at sub-nm EOT (as low as 0.6 nm), low subthreshold slopes (65-70 mV/decade before FGA), and near-symmetric threshold voltages (0.5 V for *n*FETs and -0.4 V for *p*FETs) [62]. However, there is no current understanding of the physical properties of this interface which can lead to the best-scaled gate stack. This work addresses the latter and provides evidence of a graded IL with strong Si 3+ sub-oxide component.

Furthermore, Ge has also attracted much interest as an alternative channel material for future MOSFETs due to its high carrier mobilities for both electrons (3900 cm^2/Vs) and holes (1900 cm^2/Vs) than those of Si [65] as well as due to its process compatibility with Si-based MOS technologies. Ge also has a smaller band gap (0.67 eV) for lower contact resistance, which is suitable for voltage scaling [66]. The native oxide, GeO_2 has become the subject of intense research interest as a potential passivation layer due to its excellent electrical properties [68]. Although improvements have been made, there is still challenging work in obtaining device quality interfaces on germanium due to the formation of an unstable interfacial GeO_x, $x < 2$ layer [197]. Despite intense investigation, a solution to resolve the stability of the Ge 2+ species and the volatility of molecular GeO by the diffusion of oxygen across any GeO_2 or oxide layer is still elusive. Therefore, for aggressive oxide scaling with equivalent oxide thickness well below 1 nm, the combination of higher-*k* rare-earth oxide and an ultra-thin GeO_2 is required [198]. RE oxides on Ge have been extensively studied including CeO_2 [80], [199], Gd_2O_3 [82] La_2O_3 [83], and Y_2O_3 [83]. Previous work on the band line-up and optical properties of Tm_2O_3/Ge gate stacks deposited by atomic layer deposition (ALD) also has been reported [200]. A dielectric constant of 14 to 15, and the band gap of 5.3 ±0.1 eV have been determined from capacitance-voltage and

ellipsometric (Tauc-method) measurements respectively, whereas a larger band gap value of 5.8 eV has been found using the absorption coefficient method [200]. This work [200] also observed the presence of sub-oxides GeO_x formation and GeO_2 at the Tm_2O_3/Ge interface. A large valence band offset of Tm_2O_3/Ge has been found to be 2.95 ± 0.08 eV with a conduction band offset of ~1.7 eV which can provide a sufficient barrier to holes and electrons for improved Ge MOSFET performance [200]. A recent study reported that thulium oxide (Tm_2O_3) could be potentially used for passivation layer on germanium [64]. Tm_2O_3 shows higher band gap energy (5.77 eV), high effective barriers for holes (~3 eV) and electrons (~2 eV) as well as low reactivity with Ge [64]. Recently, it has been reported that the density of interface states (D_{it}) of the gate stack can be improved to below 5×10^{11} $cm^{-2}eV^{-1}$ for Tm_2O_3/GeO_2/Ge with an O_2 rapid thermal anneal at 500 °C for 1 min [85]. These superior properties of Tm_2O_3 make it a suitable high-k material for future Ge-based technology.

3.2 Band alignment of Tm_2O_3/Si

In this work, the valence band offset (VBO) of Tm_2O_3/Si has been measured experimentally using X-ray photoelectron spectroscopy (XPS) and Kraut's method. Moreover, a detailed XPS analysis of the Tm_2O_3/Si interface when subjected to three different PDA temperatures in the range of 550−750°C has been performed. The atomic structure, thickness and elemental composition were also elucidated using high-resolution transmission electron microscopy (HRTEM) and electron energy-loss spectroscopy (EELS).

3.2.1 Experimental

The Si surface was cleaned using H_2SO_4:H_2O_2 and 5% HF before depositing Tm_2O_3 via atomic layer deposition using a Beneq TFS 200 system. ALD is a surface-controlled growth technique which performs sequential, self-limiting and surface controlled gas phase chemical reactions. ALD has several advantages including lower deposition temperature, precise thickness control, excellent step coverage and greater conformality [165], [166]. The deposition process of Tm_2O_3 occurred at the temperature of 225 °C with precursors of Tris(cyclopentadienyl) thulium (III) ($TmCp_3$) and H_2O. After that, a silicate formation anneal was performed in N_2 at three different post deposition annealing temperatures of 550 °C, 650 °C and 750 °C for 60 s, leading to the formation of a TmSiO/Tm_2O_3 dielectric stacks with a nominal physical thickness of the TmSiO layer of 0.9 nm, 1.3 nm and 2.1 nm respectively. Subsequently, the unreacted Tm_2O_3 was removed selectively in H_2SO_4 (> 23:1 selectivity toward TmSiO). HfO_2 was then deposited by ALD at 350 °C, using $Hf[C_5H_4(CH_3)]_2(OCH_3)CH_3$ and H_2O as precursors, to a target physical thickness of 3 nm. The process flow of the formation of TmSiO/HfO_2 gate dielectric stack is shown in Figure 3.2. All Tm_2O_3/Si samples were fabricated by Eugenio Dentoni Litta under the supervision of Prof. Per-Erik Hellström from KTH Royal Institute of Technology, Sweden. The process conditions are well studied and have been published by Dentoni Litta *et al.* [59].

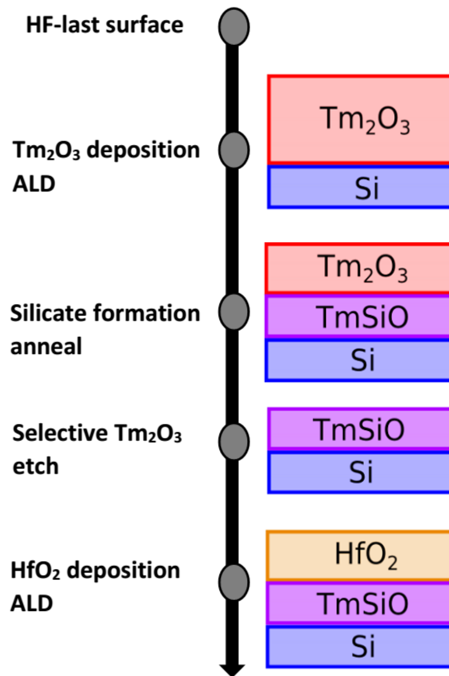

Figure 3.2: The process flow of TmSiO/HfO_2 gate dielectric stack [59].

For band alignment study, three samples (bulk Tm_2O_3, interfacial Tm_2O_3/Si and Si substrate) have been prepared to measure the valence band offset of Tm_2O_3/Si using Kraut's method [201]. The core level (CL) structure and the occupied density of states in the valence band (VB) were probed by XPS using a SPECS monochromatic AlKα X-ray source (hν = 1486.6 eV) and a PSP Vacuum Technology electron energy analyser. In this work, the XPS instrument was operated at power of 250 W with 20 mA emission current and 12.5 kV accelerating voltage. The probe area during the XPS measurements was 1 mm^2. Survey scan was carried out at a pass energy of 50 eV with a step size of 0.5 eV. Survey scans usually were recorded in the 0 −1250 eV energy range to determine the elements present in the samples and to check for surface contamination. The duration of a broad survey scan usually 20 −30 minutes that measures the amount of all detectable elements. Then, the detailed scan for individual CL regions were recorded at a pass energy of 10 eV with step size of 0.031 eV. The individual CL regions for Tm_2O_3 on Si sample including Si 2p, O 1s, C 1s, Tm 4d and VB were scanned for multiple times at a duration of at least an hour for each CL region.

All the spectra were fitted with Gaussian-Lorentzian line shapes for deconvolution of the spectra after a Shirley-type background subtraction [202], which introduces an error of ± 0.05 eV to the determination of VBO typically. The error bar (± 0.25 eV) defined in this work is due to valence band maximum (VBM) determination through the linear interpolation method [203]. For Si 2p CL, the branching ratio and the spin-orbit splitting values of 1:2 and 0.6 eV for the Si doublet (3/2 and 1/2) are considered for the fit [204]. The XPS Si 2p spectrum is used in this study to resolve different oxidation states of Si atoms in the IL via its chemical shift. The spectrum is decomposed into the Si $2p_{1/2}$ and Si $2p_{3/2}$ spin-orbit partner lines where the BE were referenced to the bulk Si $2p_{3/2}$ CL at 98.6 eV. The atomic structure and elemental composition were investigated on TiN capped samples using high-resolution transmission electron microscopy and electron energy-loss spectroscopy performed on a field emission image-corrected FEI Tecnai^{TM} F20 microscope operating at 200 kV.

3.2.2 Estimation of VBO for Tm_2O_3/Si gate stacks using Kraut's method

The VBO was estimated using Kraut's method [201], where δ_{SUB} and δ_{OXIDE} are the energy differences between chosen reference core levels (CLs) in substrate and bulk oxide samples and their respective valence band maxima (VBMs), while δ_{INT} refers to the BE difference for the former two core levels for the interfacial sample as shown in Equation (3.1)

$$VBO = \delta_{SUB} + \delta_{INT} - \delta_{OXIDE} \tag{3.1}$$

In this work, Si 2p and Tm 4d were selected as reference CLs. The energy difference $\delta_{SUB} = \left(E_{Si2p} - E_V{}^{Si}\right)$ is between Si 2p CL and VB edge ($E_V{}^{Si}$) of Si, the energy difference $\delta_{INT} = (E_{Tm4d} - E_{Si2p})$ is between Tm 4d and Si 2p CLs, and the energy

difference $\delta_{OXIDE} = \left(E_{Tm4d} - E_V{}^{Tm_2O_3}\right)$ is between the Tm 4d peak and VB edge of Tm_2O_3. They were determined in order to obtain the VBO, as shown in Equation (3.2).

$$VBO = \left(E_{Si2p} - E_V{}^{Si}\right) + \left(E_{Tm4d} - E_{Si2p}\right) - \left(E_{Tm4d} - E_V{}^{Tm_2O_3}\right) \tag{3.2}$$

The CBO can be obtained using the following Equation (3.3):

$$CBO = E_g{}^{Tm_2O_3} - (E_g{}^{Si} + VBO) \tag{3.3}$$

Table 3.1 shows the binding energy values of E_{Tm4d} , E_{Si2p} and E_V for bulk Si, interfacial Tm_2O_3/Si and bulk Tm_2O_3. Figure 3.3 shows the XPS spectra for a high-resolution Tm 4d, valence band and Si 2p CLs referring to Si substrate (Figures 3.3 (a) and (b)), interface (Figures 3.3 (c) and (d)) and bulk Tm_2O_3 (Figures 3.3 (e) and (f)). The position of the VBM is determined using the linear method [203] and shown in Figures 3.3 (b) and (f). Si 2p CL for sputtered Si substrate can be fitted with two components corresponding to the Si substrate peak (labelled as Si^0) and a sub-oxide component of Si^{1+}. For Si substrate, the value of $\left(E_{Si2p} - E_V{}^{Si}\right)$ is the difference of Si $2p_{3/2}$ peak and the VBM and it was found to be 98.84 eV which is in good agreement with the values reported in the literature [205]–[209]. Moreover, Si 2p CL for the Tm_2O_3/Si interface can be fitted by Si substrate peak, Si^{1+}, Si^{4+} (related to SiO_2), and the IL component related to silicate. The difference between Si $2p_{3/2}$ and Tm 4d peak, $(E_{Tm4d} - E_{Si2p})$ is reported to be 77.52 eV. For the bulk Tm_2O_3, the value of $\left(E_{Tm4d} - E_V{}^{Tm_2O_3}\right)$ is 173.58 eV, ~ 0.2 eV lower than the value previously reported [52]. Therefore, the calculated value for VBO using Equation (3.2) for Tm_2O_3/Si interface is 2.8 eV. From the literature, the band gap of Si is 1.12 eV at room temperature [186], and the band gap value of Tm_2O_3 is reported to be 5.77 eV [64].

Therefore, the measured CBO value using Equation (3.3) is found to be 1.9 eV. Table 3.2 shows the values of δ_{SUB}, δ_{INT}, and δ_{OXIDE} from our work compared to values from previous studies [52], [64], [200], [205]–[209]. Previous work determined a large VBO of Tm_2O_3 on Si of 3.1 ± 0.1 eV and CBO of 2.3 ± 0.3 eV [52]. The most recent work [210] found a CBO of 1.68 ± 0.2 eV from electrical current-voltage measurements using Fowler-Nordheim (FN) tunnelling analysis. Table 3.3 shows the band offset values for Tm_2O_3 and other RE oxides as reported in the literature [46], [52], [64], [200], [209], [211]. The energy band diagram of Tm_2O_3/Si stack with type I band alignment in this work is illustrated schematically in Figure 3.4. The angle-resolved XPS Si 2p and Tm 4d CL spectra taken from an interfacial Tm_2O_3/Si sample at two grazing angles 30 ° (surface sensitive) and 60 ° (bulk sensitive) are shown in Figure 3.5. Figure 3.6 shows that the CL variation is < 0.1 eV, where the BE variation for Si 2p is 98.41 ± 0.05 eV and for Tm 4d is 176.04 ± 0.07 eV. This BE variation is within the experimental error value of the XPS and Kraut's method (± 0.2 eV), so band bending at the interface has been found to be negligible.

Table 3.1: The binding energy values of E_{Tm4d}, E_{Si2p} and E_V for bulk Si, interfacial Tm_2O_3/Si and bulk Tm_2O_3/Si samples determined in this experimental work.

Sample	E_{Tm4d} (eV)	E_{Si2p} (eV)	E_V (eV)
Bulk Si		99.22	0.38
Interfacial Tm_2O_3/Si	175.97	98.45	−
Bulk Tm_2O_3	175.49	−	1.91

Table 3.2: The values of δ_{SUB}, δ_{INT}, and δ_{OXIDE} from this work compared to literature values [52], [64], [200], [205]–[209].

Material system	δ_{SUB} (eV) $\left(E_{Si2p} - E_V{}^{Si}\right)$	δ_{INT} (eV) $(E_{Tm4d} - E_{Si2p})$	δ_{OXIDE} (eV) $\left(E_{Tm4d} - E_V{}^{Tm_2O_3}\right)$
Tm_2O_3/Si (this work)	98.84	77.52	173.58
$SrTiO_3$/Si [205]	98.9 ± 0.05 (n-type Si) 98.98 ± 0.05 (p- type Si)	−	−
HfO_2 /Si [206]	98.80 ± 0.06	−	−
Si/Ge [207]	98.95	−	−
TiO_2/Si [208]	98.76 ± 0.06	−	−
$LaAlO_3$/Si [209]	98.9	−	−
Tm_2O_3/Si [52]	−	77.9	173.8
Tm_2O_3/Ge [200]	−	−	173.49
Tm_2O_3/Ge [64]	−	−	173.32

Table 3.3: Band offsets for Tm_2O_3 and other oxides as reported in the previous studies [46], [52], [64], [200], [209], [211].

Material system	VBO (eV)	CBO (eV)	E_g (eV)
Tm_2O_3/Si (this work)	2.8	1.9	5.77 [64]
Tm_2O_3/Si [52]	3.1 ± 0.1	2.3 ± 0.3	6.5 ± 0.3
Tm_2O_3/Ge [200]	2.95 ± 0.08	1.7	5.3 ± 0.3
Tm_2O_3/Ge [64]	3.05 ± 0.2	2.05	5.77
La_2O_3/Si [46]	2.4 ± 0.1	1.66 ± 0.3	5.18
$LaAlO_3$/Si [209]	2.70 ± 0.1	2.31 ± 0.2	6.13
GdSiO/SiO_2/Si [211]	2.3	2.9	6.3

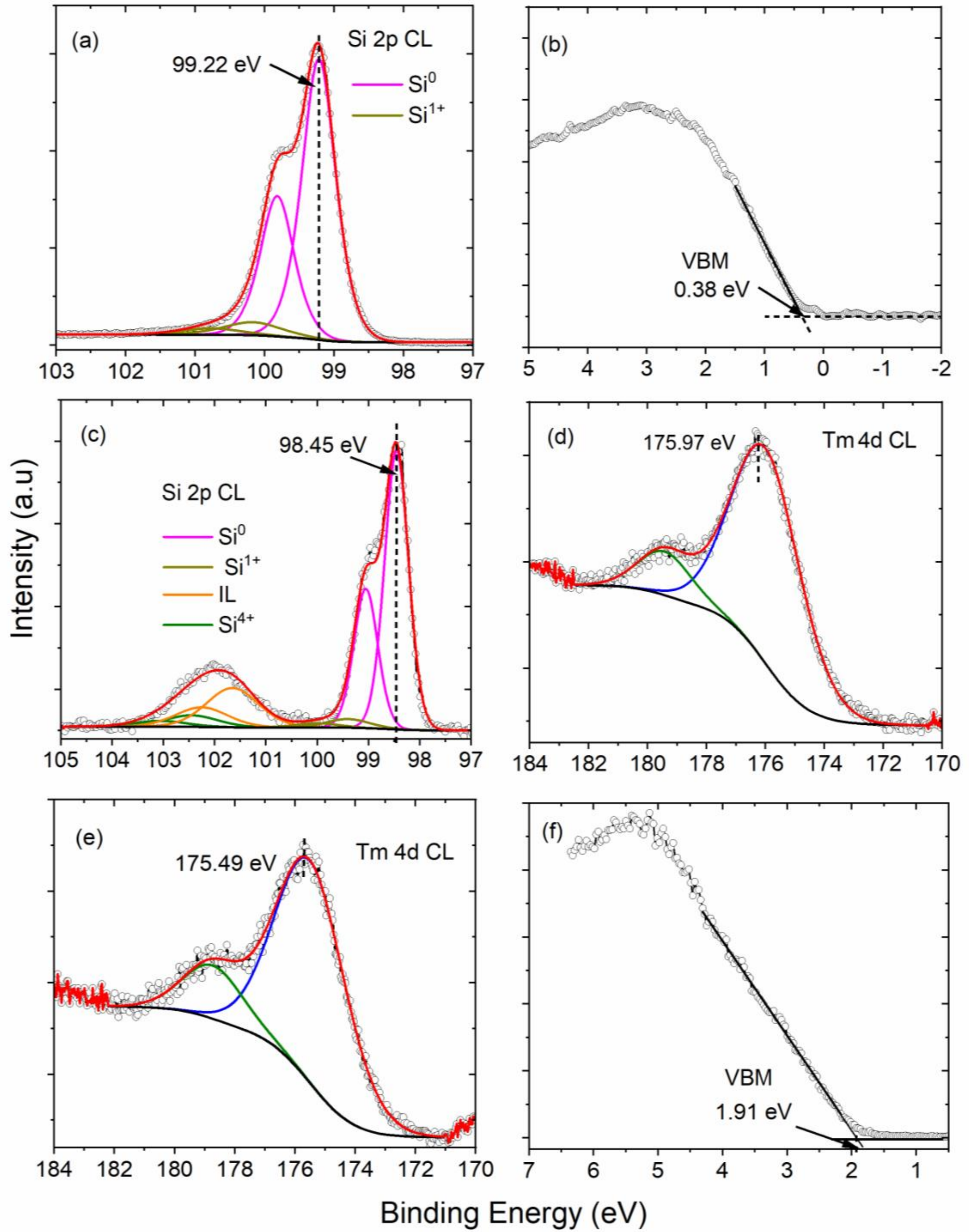

Figure 3.3: (a) Si 2p CL and (b) VB spectrum for Si substrate; (c) Si 2p and (d) Tm 4d CLs for interfacial Tm_2O_3/Si sample; (e) Tm 4d and (f) VB spectrum for bulk Tm_2O_3 sample.

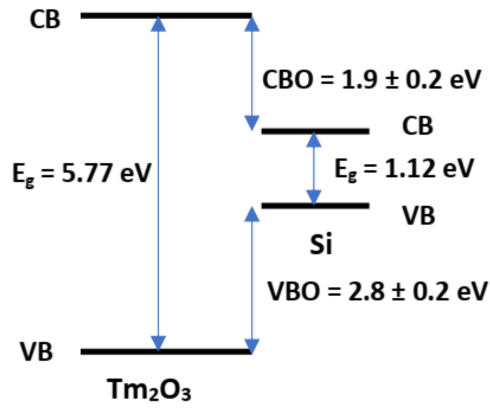

Figure 3.4: Schematic energy band diagram of Tm_2O_3/Si gate stack derived from XPS and VASE measurements in this study.

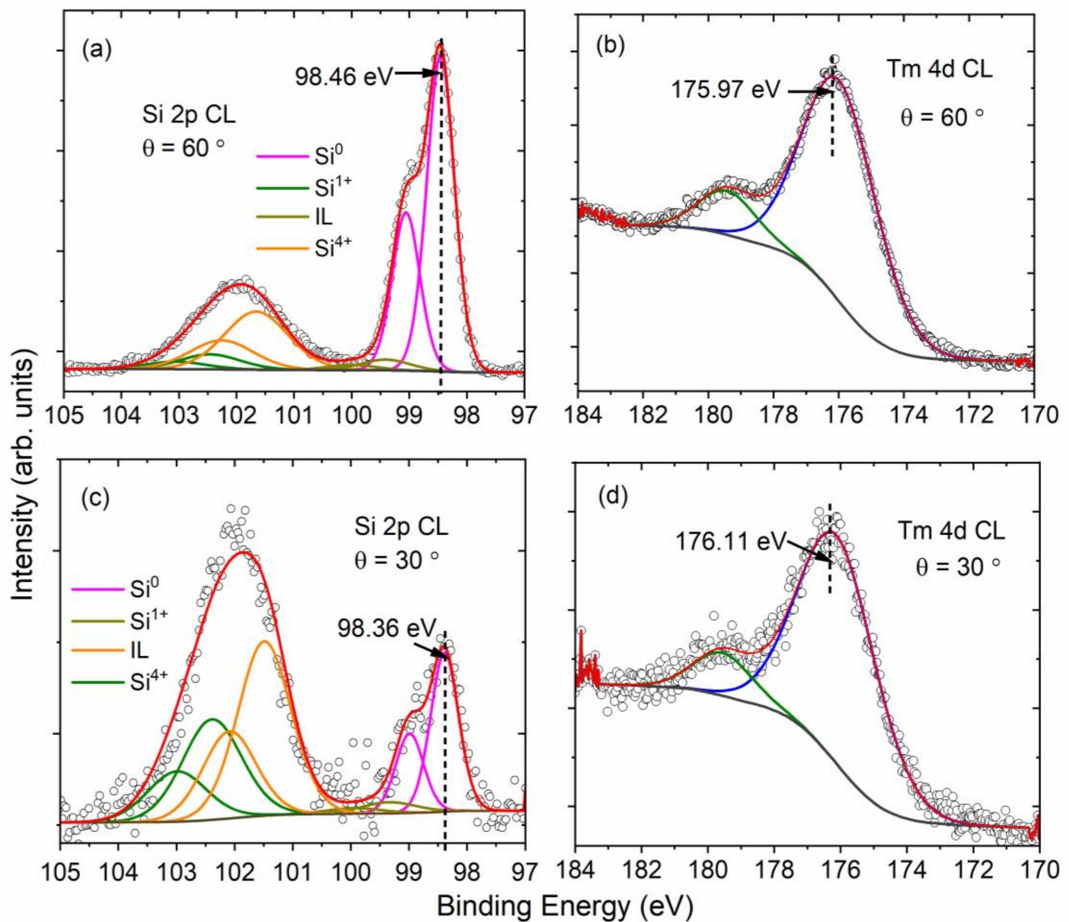

Figure 3.5: The angle-resolved XPS of Si 2p and Tm 4d CLs spectra for the interfacial Tm_2O_3/Si sample.

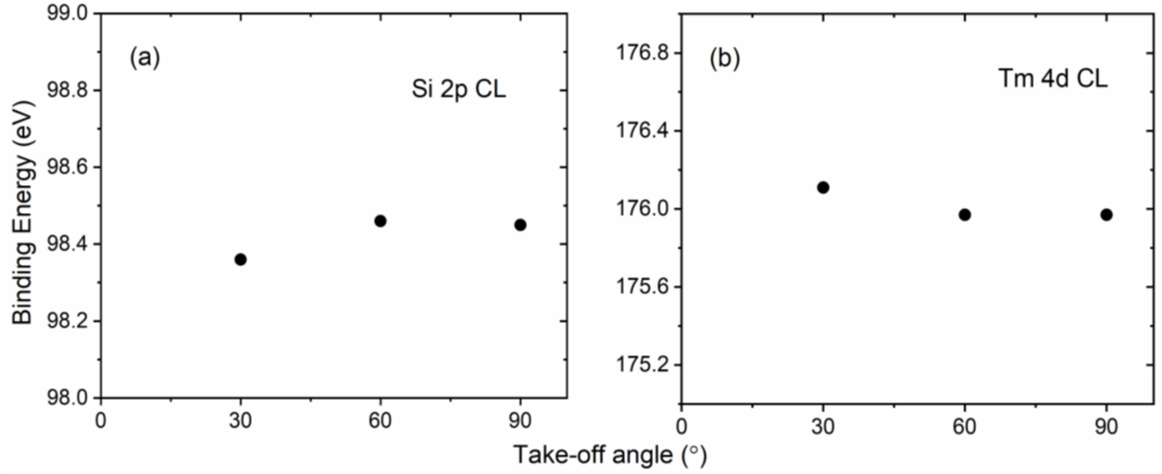

Figure 3.6: Dependence of measured binding energies on take-off angles for Si 2p and Tm 4d XPS CL spectra for the interfacial Tm_2O_3/Si sample.

The measured VBO and CBO values from our work are smaller as compared to previous work on Tm_2O_3 deposited on Si by molecular beam epitaxy (MBE) [52] (see Table 3.3), The difference in CL value of δ_{SUB} in our work is comparable with the value used in Wang *et al*. (see Table 3.2), which is obtained from ref. [64], but the discrepancy is mainly due to the difference in CL values of δ_{INT} and δ_{OXIDE} with a difference values of 0.38 eV and 0.22 eV, respectively. Moreover, a large difference in E_g value of 0.73 eV determined from O 1s energy-loss spectrum based on XPS measurement [52] (see Table 3.3), while the E_g used in our work is determined by vacuum ultra-violet variable angle spectroscopic ellipsometry (VUV-VASE) technique from ref. [64]. However, for different systems where Tm_2O_3 deposited on Ge [64], [200] provide a band offsets values within our measurement error (see Table 3.3). In the case for different oxides such as La_2O_3 deposited on Si [46] and GdSiO on Si [211] (see Table 3.3), both VBO and CBO values were found to be much smaller as compared to our measured results.

3.2.3 Properties of TmSiO interfacial layer fabricated using different PDAs of Tm_2O_3/Si

Figures 3.7 and 3.8 show the Si 2p photoelectron spectra from annealed Tm_2O_3 on Si samples. A signature of the IL of TmSiO can be observed at around 3.1 eV chemical shift from the main Si substrate peak (marked as Si^0), which is located at the BE of 101.7 eV. Previous study on Tm_2O_3/Si stack has identified that a thin silicate layer has been formed at a chemical shift of 3.6 eV from main Si 1s XPS CL [53]. As can be seen in close-up in Figure 3.8, the interfacial layer can be fitted using three components (each with spin-orbit splitting): Tm-Si-O bond at BE of 101.7 eV, 3+ Si at BE of 101.08 eV and 1+ Si at BE of 99.5 eV. Table 3.4 shows the intensity ratio of sub-peak components (representing the IL) to the main Si substrate peak for Tm_2O_3/Si samples with increasing PDA temperatures. It can be seen in Figures 3.7 and 3.8 that the area of IL increases with annealing temperature. This is in agreement with a recent study of TmSiO thin films where it has been found that the physical thickness of IL measured using spectroscopic ellipsometry (SE) is increased with the annealing temperature, and the sub-nm silicate thickness can be achieved for annealing temperatures in the region of 500–550 °C [59].

Figures 3.7 and 3.8 show the formation of an intense Si^{3+} peak at a chemical shift of 2.48 eV [204] from Si^0 peak with corresponding BE of 101.08 eV for annealed Tm_2O_3/Si at a PDA temperature of 550 °C. Previous studies have reported sub-oxide Si^{3+} peak at chemical shifts of 2.5 eV [212], 2.53 eV [213], and 2.6 eV [214], [215] from Si^0 peak, being in agreement with results from this work (2.48 eV). The Si^{1+} peak can also be resolved in the fitting, but has a small intensity with a chemical shift of around 0.95 eV from the main Si^0 peak, in agreement with Refs. [204], [212]. The Si^{1+} peak shows a similar pattern as Si^{3+} peak where the intensity ratio to Si substrate peak

decreases with increasing PDA temperatures from 550 °C to 750 °C. The sub-peak resolved at around 0.3 eV towards higher BE from main Si^0 peak in Figure 3.7 is related to the effect of surface charges in the atomic layers closer to the surface (labelled as SSi) as explained in Reference [216].

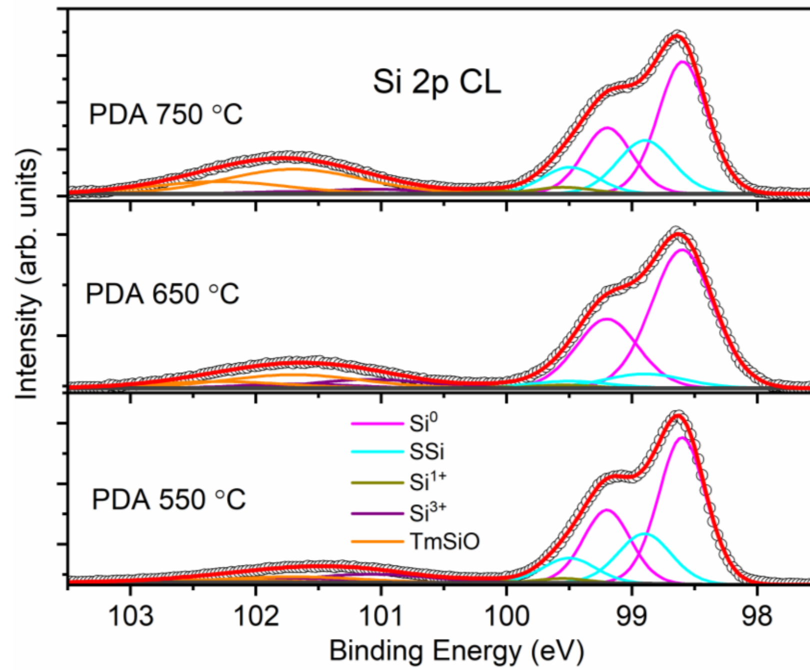

Figure 3.7: Fitted Si 2p XPS CL spectra for Tm_2O_3/Si samples annealed at three different temperatures: 550 °C, 650 °C and 750 °C. Both spin-orbit $2p_{3/2}$ and $2p_{1/2}$ components are included in each spectrum. The sub-peak towards higher binding energy refers to the interfacial layer; it is apparent that the area of the sub-peak is enhanced for higher PDA temperatures. SSi refers to the effect of surface charges in the atomic layers closer to the surface.

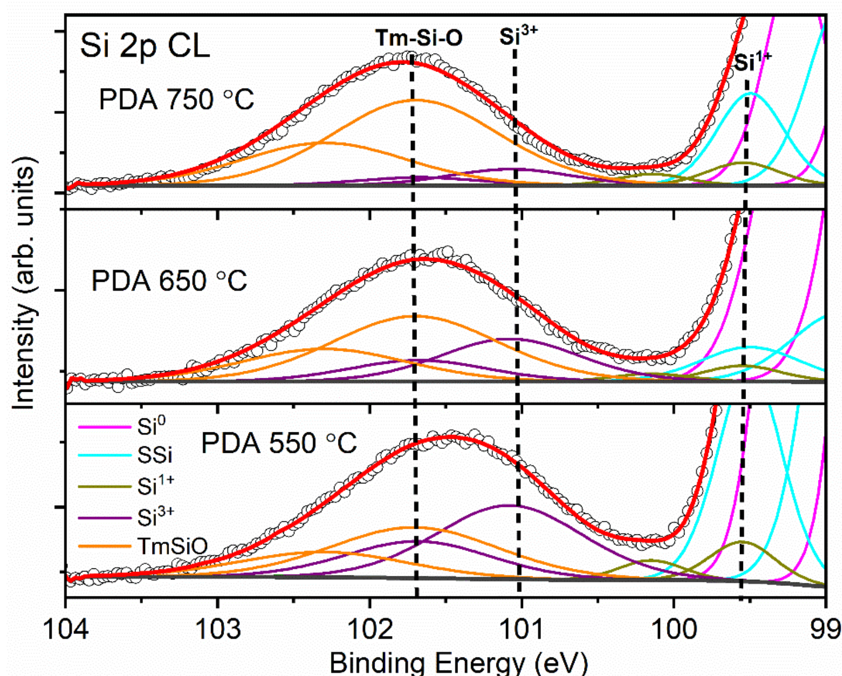

Figure 3.8: A close-up image of the sub-peak of Si 2p XPS CL for annealed Tm_2O_3/Si samples. Both spin-orbit doublet 3/2 and 1/2 components are included for each fitted core level referring to Tm-Si-O, Si^{3+} and Si^{1+}.

It can be concluded from Table 3.4 a very strong presence of SiO_x at the interface, with Si in 3+ oxidation state, for the PDA temperature of 550 °C. Once the PDA temperature increases beyond 550 °C, the area of TmSiO sub-peak increases and dominates over silicon sub-oxide (SiO_x).

Table 3.4: The intensity ratio of sub-peak fitted components (TmSiO, Si^{3+} and Si^{1+}) to main substrate peak referred to as Si^0 for Tm_2O_3/Si samples which underwent different PDA temperatures.

PDA (°C)	Intensity ratio (TmSiO:Si^0) $2p_{3/2}$	Intensity ratio (Si^{3+}:Si^0) $2p_{3/2}$	Intensity ratio (Si^{1+}:Si^0) $2p_{3/2}$
550	0.12	0.15	0.04
650	0.22	0.12	0.02
750	0.52	0.08	0.03

Figure 3.9 shows Tm 4d CL for all annealed Tm_2O_3/Si samples. It can be seen that an increase of annealing temperature from 550 °C to 750 °C, results in the centroid peak of Tm 4d to increase slightly towards higher BE from 175.6 eV to 176.4 eV. This shift substantiates the formation of TmSiO IL for annealed Tm_2O_3/Si samples, which is in line with the fitting of Si 2p CL spectra shown in Figure 3.8. Previous work reported that Tm 4d peak of the Tm_2O_3 is shifted towards higher BE by about 1 eV relative to the Tm_2O_3 reference (located at BE of 175.6 eV) at annealed temperature of 600 °C and 700 °C, whereas the shifting of the Tm 4d peak to a higher BE of the film annealed at 800 °C is 1.4 eV. There was a sudden change in the Tm bonding status at 800 °C due to a thicker Tm-silicate layer [50].

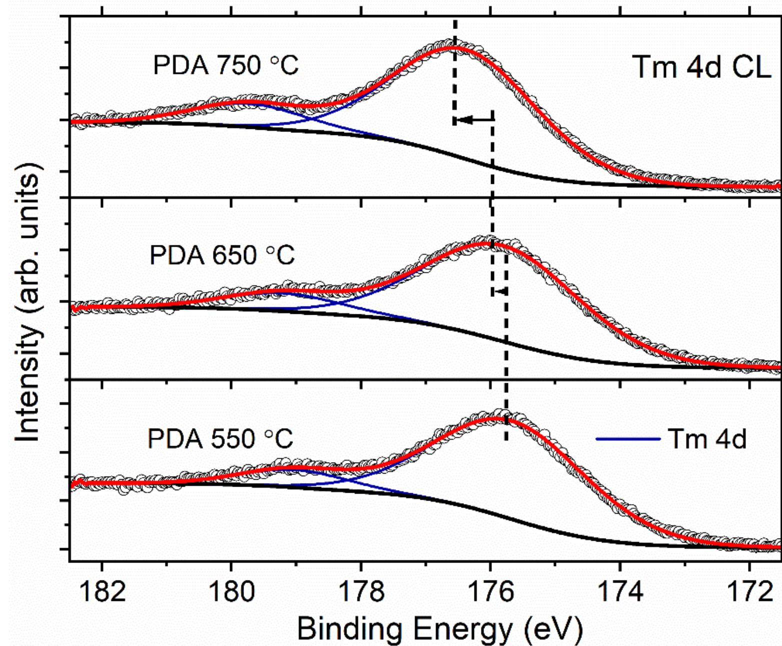

Figure 3.9: Tm 4d XPS CL spectra for Tm_2O_3/Si samples annealed at different PDA temperatures (550 °C – 750 °C).

In Figure 3.10, no TmSiO bond has been detected after the top Tm_2O_3 layer has been etched on Tm_2O_3/TmSiO/Si stack, which means that no Tm-Si-O bond is present within the detection limit. Moreover, the Si^{4+} state can be observed at BE of

102.6 eV with a chemical shift of 4 eV from Si substrate, being indicative of a formation of SiO_2 layer after etching of Tm_2O_3 on the surface. Furthermore, an additional component can be fitted and appears at the chemical shift of 3.4 eV relative to the bulk Si^0 peak, after deposition of HfO_2 on top of the TmSiO/Si which is related to the formation of Hf-Si-O. Previous study on HfO_2/Si interface reported that the chemical shift to the higher BE by 3.7 eV relative to the Si substrate can be assigned to Si-O-Hf bonds [168]. Moreover, Renault *et al.* observed that the Hf-Si-O appears between Si^{4+} and Si^{3+}, shifted by 0.7 eV to lower BE relative to Si^{4+} [168]. The origin of the shift to lower BE compared to SiO_2 can arise from the Si second-nearest-neighbour from Si to Hf [168]. In details, Figure 3.11 shows the HfO_2-capped samples with ILs formed at varying PDA temperatures. The arising peak at a binding energy of 102 eV could be related to Hf-Si-O bond. An intense peak of SiO_2 can be seen at high PDA temperature of 750 °C.

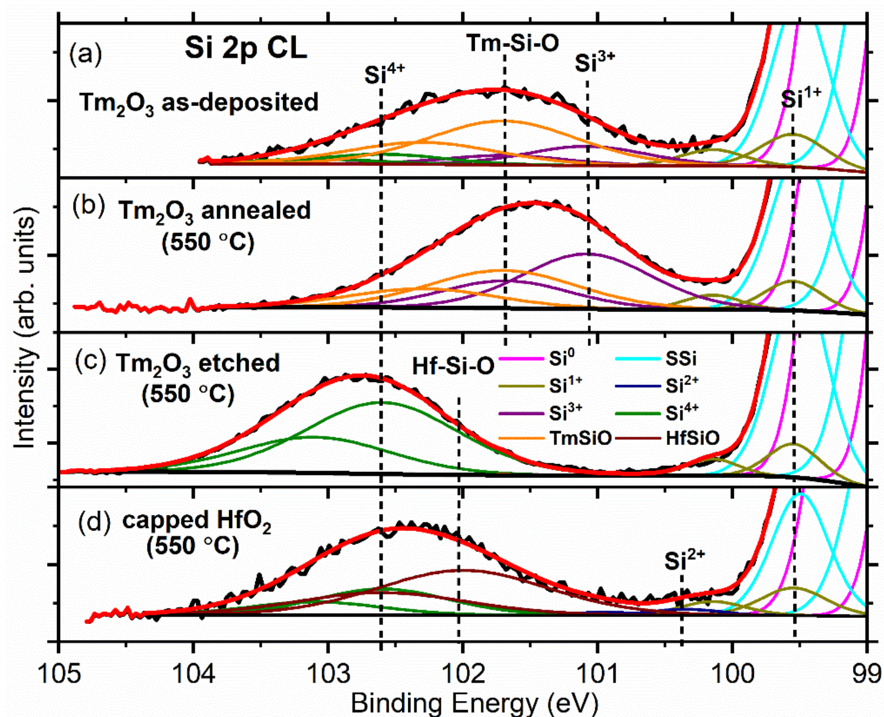

Figure 3.10: The comparison spectra of Si 2p XPS core levels for (a) as-deposited Tm_2O_3, (b) Tm_2O_3 annealed at a temperature of 550 °C, (c) Tm_2O_3 on top etched after PDA of 550 °C, and (d) HfO_2-capped sample with IL formed at 550 °C.

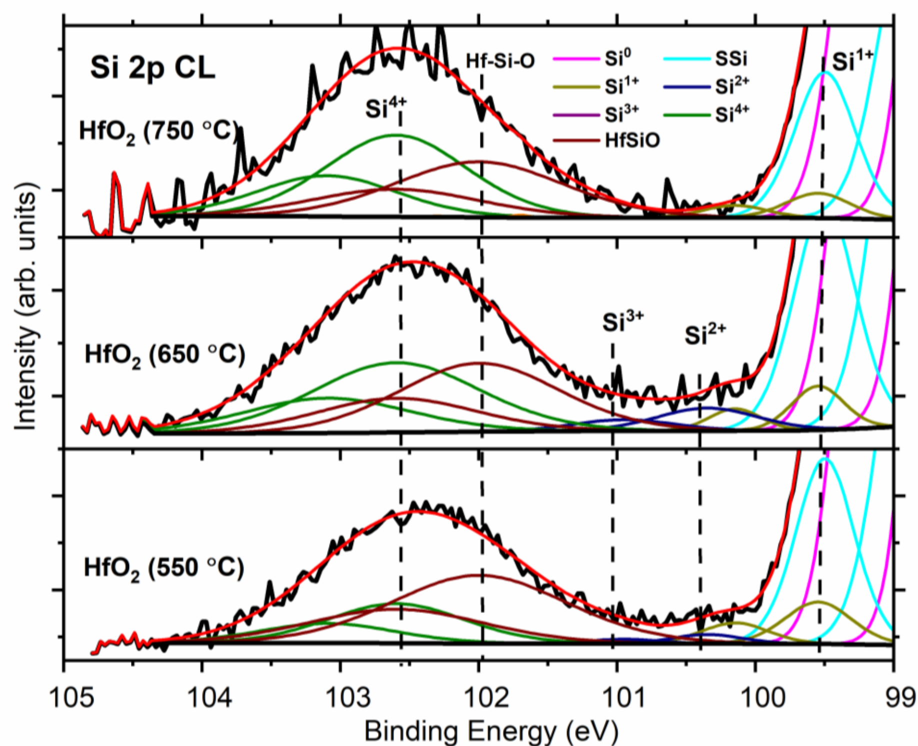

Figure 3.11: Si 2p XPS core level for HfO_2-capped samples with ILs formed at varying PDA temperatures.

The chemical shift from the Si substrate peak (Si^0) referring to the following Si oxidation states of Si^{1+}, Si^{2+}, Si^{3+}, and Si^{4+} are 0.95 eV, 1.75 eV, 2.48 eV, and 4 eV, respectively. These values are found to be consistent with the work done by Himpsel *et al*. [204] except for Si^{4+}. Table 3.5 compares the chemical shifts observed for each oxidation state (Si^{x+}, x = 1, 2, 3, and 4) from the main Si 2p core level in this work and reported in the literature [63,71-73,77-78].

Table 3.5: The chemical shift of Si oxidation states (+1, +2, +3 and +4) fitted from Si 2p XPS core level peak on Tm_2O_3/TmSiO/Si samples in this work and compared to several previous studies [63,71-73,77-78].

	Chemical Shift for Si Oxidation State (eV)			
Ref.	Si^{1+}	Si^{2+}	Si^{3+}	Si^{4+}
This work	0.9	1.75	2.48	4
Himpsel *et al.* [204]	0.95	1.75	2.48	3.9
Thogesen *et al.* [217]	1	2	3.1	4.2
Logofatu *et al.* [213]	0.88	1.36	2.53	4.18
Lu *et al.* [214]	0.97	1.8	2.6	3.82
Rochet *et al.* [212]	0.95	1.72	2.5	3.57
Jolly *et al.* [218]	1.05	1.94	2.72	3.58

3.2.4 High-resolution transmission electron microscopy and electron energy loss spectroscopy studies of HfO_2/TmSiO/Si

Dr Schamm-Chardon from CEMES-CNRS, Toulouse, France is acknowledged for her contribution in the HRTEM measurements. Figure 3.12 shows HRTEM images of Tm_2O_3/TmSiO/Si samples, where IL (i.e. TmSiO) is formed using different PDA temperatures: (a) 550 °C, (b) 650 °C, and (c) 750 °C. It can be seen that the white region above Si substrate, referring to TmSiO, increases in thickness as PDA temperature increased from 0.9 nm for 550 °C, to 1.3 nm for 650 °C and then to 2.1 nm for 750 °C. Furthermore, as there is evidence of Tm-Si-O bond in Fig. 3.10, it seems from Figure 3.12 that the Tm has diffused from the oxide layer and formed TmSiO at the interface. Figure 3.13 shows HRTEM images of Tm_2O_3/TmSiO/Si

stacks, when top Tm_2O_3 layer is etched off, revealing only IL formed by different PDA temperatures (a) 550 °C, (b) 650 °C, and (c) 750 °C. It can be seen from these images that the IL above the Si substrate increases in thickness as the annealing temperature increases, in the same way as seen in Figure 3.12. Further confirmation that the thicknesses of ILs stay within the range of 0.9 nm to 2.1 nm can be seen from images in Figure 3.14, where the TmSiO/Si stacks processed at different PDA temperatures are capped with 3 nm (nominal) HfO_2. An apparent increase of the total thickness from 4 nm (Figure 3.14(a)) to 4.9 nm (Figure 3.14(c)) here could be the artefact, likely to be due to the error done in the measurement as the roughness of the top HfO_2 layer increases for the sample with higher annealing temperature (see “wavy” top surface for the 750°C PDA sample, Figure 3.14(c)). On the other hand, the contrast of the bright layer in Figure 3.14 is rather not changing as the annealing temperature increases and remains bright, which could be a signature of a SiO_2-rich interfacial layer.

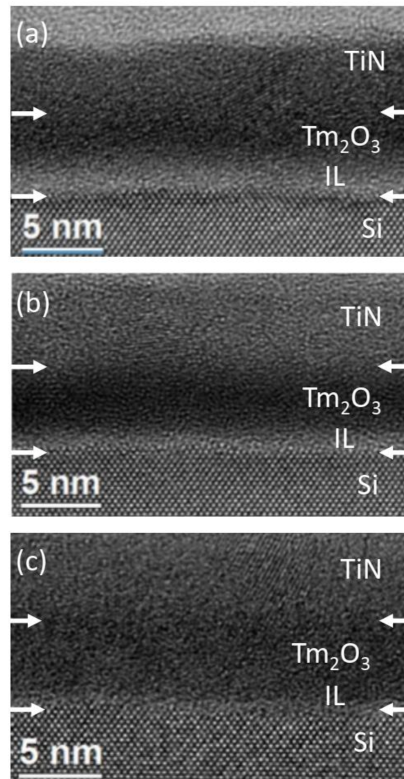

Figure 3.12: HRTEM images of (a) 3 nm Tm_2O_3/0.9 nm TmSiO IL formed at 550 °C, (b) 3 nm Tm_2O_3/1.3 nm TmSiO IL formed at 650 °C and (c) 3 nm Tm_2O_3/2.1 nm TmSiO IL formed at 750 °C PDA. The overall thickness of the stack increases with annealing temperature (courtesy of Dr Schamm-Chardon, CEMES-CNRS, Toulouse, France.)

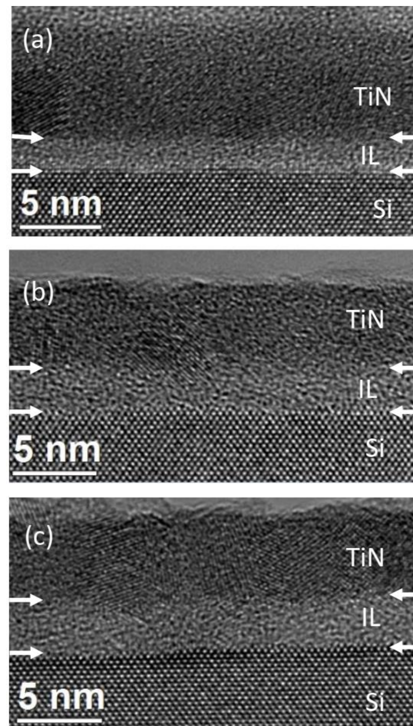

Figure 3.13: HRTEM image of Tm_2O_3/TmSiO/Si stacks when top Tm_2O_3 layer is etched off, revealing only IL TmSiO: (a) 0.9 nm TmSiO IL formed at 550 °C; (b) 1.3 nm TmSiO IL formed at 650 °C; and (c) 2.1 nm TmSiO IL formed at 750 °C. The layers were capped with TiN for protection (courtesy of Dr Schamm-Chardon, CEMES-CNRS, Toulouse France.)

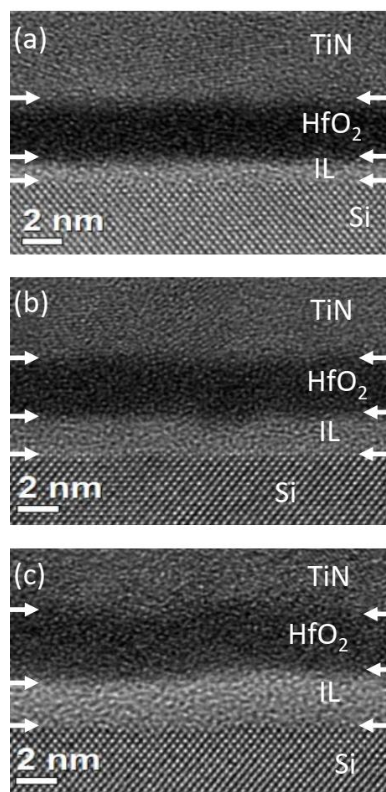

Figure 3.14: HRTEM images of 3 nm HfO_2/TmSiO IL/Si stacks, where IL is formed by PDA temperature of (a) 550 °C, (b) 650 °C, and (c) 750 °C. (courtesy of Dr Schamm-Chardon, CEMES-CNRS, Toulouse France.)

The elemental profiles of Si, Tm, O and Hf versus depth have been derived from electron energy loss (EEL) spectra shown in Figure 3.15 for Tm_2O_3/TmSiO/Si stacks and in Figure 3.16 for HfO_2/TmSiO/Si stacks, where IL (TmSiO) was formed using different PDA temperatures from 550 – 750 °C. The EEL spectra of each element were acquired at several points on the sample (from 3 to 6) in order to have a statistical representation since the spatial resolution is around 1-1.5 nm. The profiles were extracted from elemental quantification (O, Hf) or were deduced from the simulation of the elemental distribution in order to separate signatures being in the same energy domain (for example, Si and SiO_2). The red profiles in Figure 3.15, between the Si and the Tm, represent the SiO_2 character of the Si L edge, where the Tm is also present fully present. This indicates the existence of a silicate layer at the Tm_2O_3/Si interface, in agreement with XPS CL spectra shown in Figures 3.8 and 3.10. As the temperature

increased, there is more Tm at the place of the red profile, indicating more silicate in the films, which agrees with the XPS results (see Figure 3.8). In the case of HfO_2/TmSiO/Si stacks, the EELS profiles shown in Figure 3.16 indicate no Tm present at the interface and the dominance of SiO_2. The latter coincides with the brighter IL regions seen in Figure 3.14 likely to be a SiO_2-rich layer, as well as correlate with XPS CL spectra in Figure 3.11, where SiO_2 sub-peak dominates over potential Hf-Si-O bonds. The EELS in Figure 3.16 also indicate that there is no or nearly no Hf in the interfacial layer.

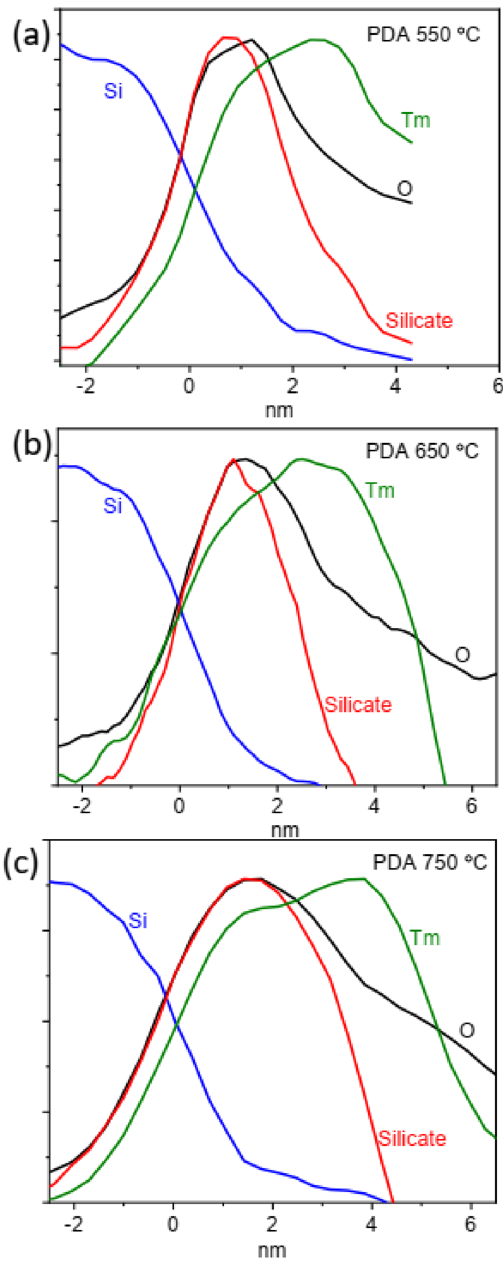

Figure 3.15: The EELS profiles for Tm_2O_3/TmSiO/Si stacks with TmSiO formed at different PDA temperatures: (a) 550 °C, (b) 650 °C, and (c) 750 °C. (courtesy of Dr Schamm-Chardon, CEMES-CNRS, Toulouse France.)

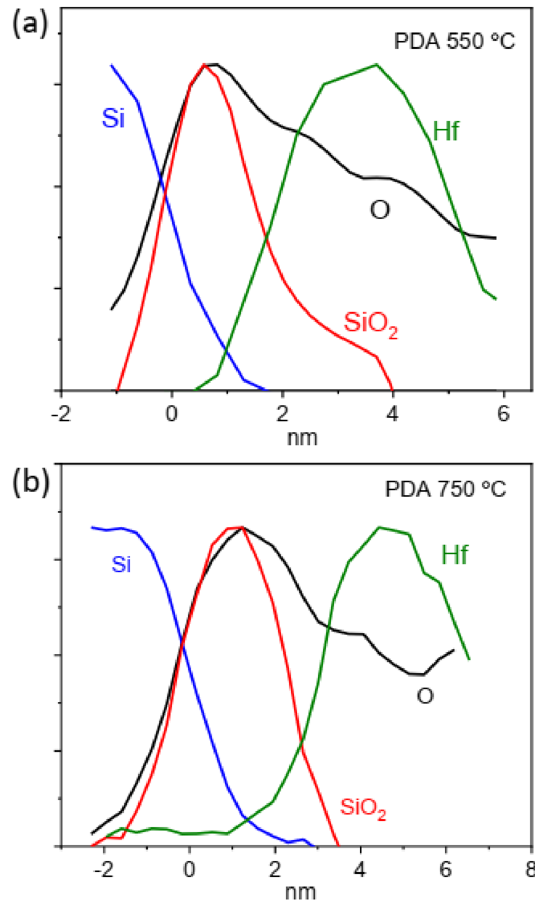

Figure 3.16: The EELS profiles of HfO_2/TmSiO/Si stacks, with TmSiO formed at different PDA temperatures: (a) 550 °C, and (b) 750 °C. (courtesy of Dr Schamm-Chardon, CEMES-CNRS, Toulouse France.)

3.3 XPS study of Tm_2O_3/Ge interfaces

In this work, the objectives were to investigate the interface properties of 3 and 7 ALD cycles of Tm_2O_3 deposited on Ge (as-deposited samples), and after two different annealing conditions: in O_3 at 350 °C and in N_2 at 550 °C using X-ray photoelectron spectroscopy.

3.3.1 Experimental work

All Tm_2O_3/Ge samples for this work were fabricated by Laura Žurauskaitė under the supervision of Prof. Per-Erik Hellström from KTH Royal Institute of Technology, Sweden. These Tm_2O_3 films were prepared by ALD on a Ge epitaxial

layer grown on Si. Our contribution in this work is to characterise ALD deposited samples mainly using XPS technique. The XPS spectra for Tm_2O_3/Ge stacks were recorded at the University of Liverpool facility using a UHV system consisting of an Al Kα X-ray (hυ = 1486.6 eV) source operating at 250 W, and a PSP Vacuum Technology electron analyser. The probe area during the XPS measurements was 1 mm^2. Survey scan was carried out at a pass energy of 50 eV with a step size of 0.5 eV in the 0 −1250 eV energy range. Then, the detailed scan for individual core level (CL) regions were recorded at a pass energy of 10 eV with step size of 0.031 eV. The individual CL regions for Tm_2O_3 on Ge sample including Ge 3d, O 1s, C 1s, Tm 4d and VB were scanned for a duration of at least an hour for each CL region. The electron BEs were then corrected by setting the C 1s peak in the spectra (due to stray carbon impurities) at 284.6 eV for all samples [219]. A Shirley-type background is used during the fitting of all spectra [202]. For Ge 3d core level spectra, the data were fitted using a doublet of Voigt functions corresponding to Ge $3d_{5/2}$ and Ge $3d_{3/2}$ components with spin-orbit splitting of 0.6 eV and area ratio of 2:3 [83], [220]. For Ge 3p core level spectra, the data were fitted using a doublet of Voigt functions corresponding to Ge $3p_{3/2}$ and Ge $3p_{1/2}$ components with spin-orbit splitting of 4.1 eV and area ratio of 1:2.

3.3.2 Results and Discussion

Figures 3.17 and 3.18 show the Ge 3d photoelectron spectra from 3 cycles ALD as-deposited and annealed Tm_2O_3/Ge in N_2 at 550 °C and in O_3 at 350 °C as compared to previous work [200]. The binding energy for Ge substrate peak corresponds to Ge $3d_{5/2}$ and Ge $3d_{3/2}$ components appearing at 29.0 eV and 29.6 eV, in agreement with reported values [83]. It can be seen clearly from Figure 3.18 that a strong formation of

Ge^{3+} and a small Ge^{2+} with BE chemical shifts of around 2.8 eV and 1.4 eV respectively from Ge main peak. The binding energies of Ge^{3+} and Ge^{2+} peaks for Ge $3d_{5/2}$ component are situated at 30.4 eV and 31.8 eV for as-deposited sample. The BE chemical shift for Ge^{2+} of ~1.4 eV can be associated with GeO, which is consistent with previous work [68]; while the BE chemical shift of about 2.8 eV could be related to Ge_2O_3 (Ge^{3+}) [221]. The Ge +2 and Ge +3 oxidation states also have been reported to occur between 1.8 eV and 2.6 eV [199], [222]–[224]. Moreover, the presence of a small peak of Ge^{4+} at the chemical shift of around 3.5 eV from Ge substrate peak can be seen at the interface of Tm_2O_3/Ge annealed in O_3 at 350 °C (Fig. 3.18, middle). The chemical shift of Ge^{4+} around 3.5 eV from our work is similar to previously reported, and it can be related to GeO_2 [200], [221]. In the literature, Ge +4 oxidation state has been reported at chemical shifts of 3.0 eV [225], 3.2 eV [68], [226], 3.4 eV [64], [199], [222], [224] and 3.65 eV [223]. In the case of Tm_2O_3/Ge sample annealed in N_2 at a 550 °C (Fig. 3.18, top), there is no presence of GeO_2. As compared to previous work on Tm_2O_3/Ge [200], we can see clearly from Figures 3.17 and 3.18 that the Ge 3d main peak is intense, but there is no presence of neighbouring O 2s and Tm 5p peaks. This indicates a possible very thin non-stoichiometric TmO_x film on Ge for all three samples, as-deposited and annealed.

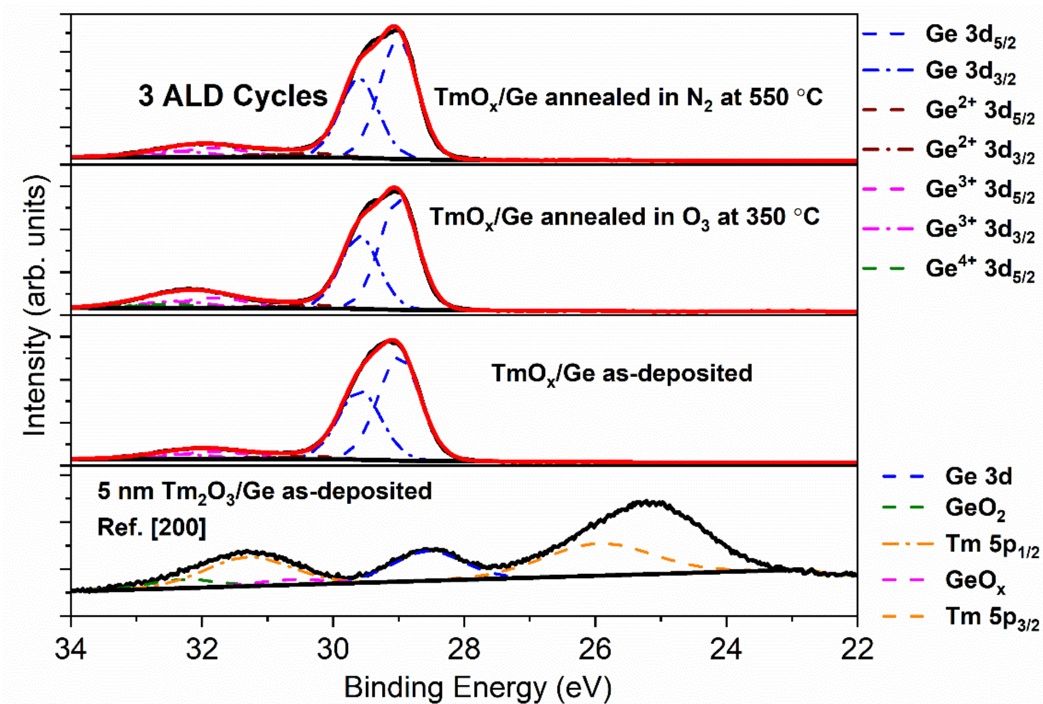

Figure 3.17: Ge 3d XPS core level for 3 ALD cycles of Tm_2O_3 on Ge: for as-deposited and annealed Tm_2O_3/Ge samples compared to previous work in Ref. [200].

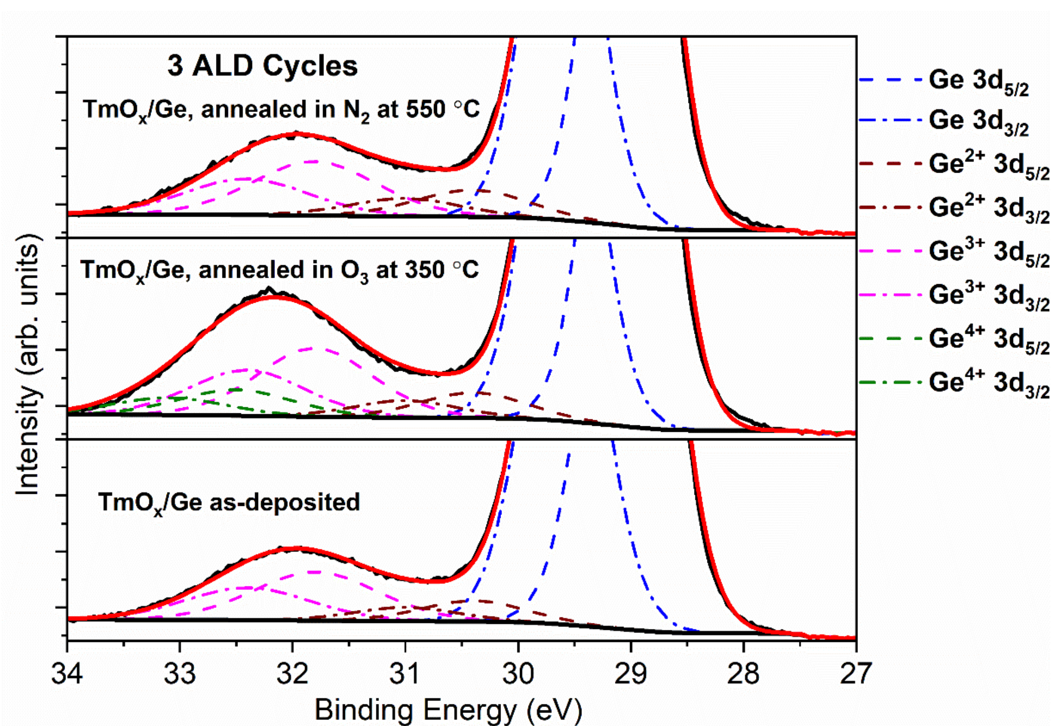

Figure 3.18: Enlarged area of high BE side of Ge 3d XPS CL peak shown in Fig. 3.16. The results relate to 3 ALD cycles of Tm_2O_3 deposited on Ge: for as-deposited and annealed samples.

Figures 3.19 and 3.20 show the Ge 3d photoelectron spectra from 7 ALD cycles of Tm_2O_3 on Ge, as-deposited and annealed samples in O_3 at 350 °C and in N_2 at 550 °C, and compared to similar spectrum in Ref. [200]. The spectra show almost similar pattern as for 3 ALD cycles TmO_x/Ge samples. The formation of Ge^{3+} is the highest for O_3 annealed sample (Fig. 3.20, middle) and there is a very low peak of Ge^{4+} for this sample showing a possible GeO_2 at the interface. Similarly to the case of 3 ALD cycles TmO_x/Ge samples, the main Ge 3d peak is intense, but there is no signal of O 2s and Tm 5p peaks that have been observed in previous work [200]. The latter suggests that by increasing number of ALD cycles to 7, does not lead to the formation of stoichiometric Tm_2O_3 on Ge; the films appear to be TmO_x/Ge.

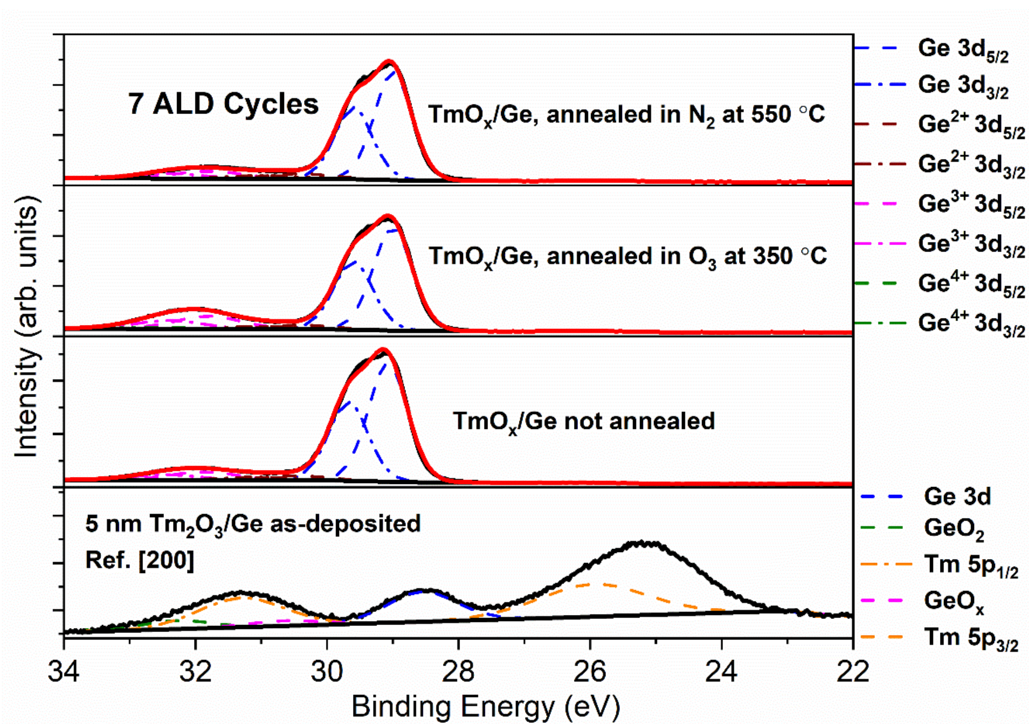

Figure 3.19: Ge 3d XPS core level for 7 ALD cycles of Tm_2O_3 on Ge for as-deposited and annealed samples compared to previous work [200].

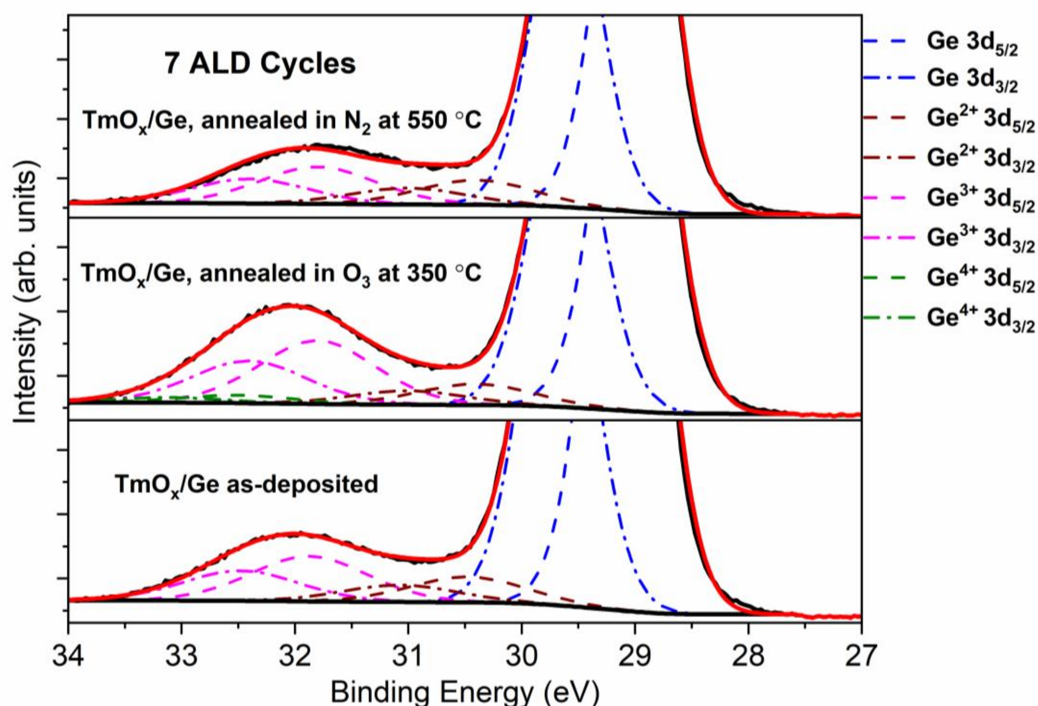

Figure 3.20: Enlarged high BE side of the main Ge 3d XPS core level for 7 ALD cycles of Tm_2O_3 on Ge for as-deposited and annealed TmOx/Ge samples.

Figures 3.21 and 3.22 show the comparison of Ge 3d XPS CL for 3 and 7 ALD cycles TmO_x/Ge samples, together with a similar spectrum from previous work [200]. It can be seen that the binding energy of Ge 3d peak for 7 ALD cycles TmOx/Ge sample is slightly shifted for about 0.08 eV towards higher BEs in comparison to 3 ALD cycles TmO_x/Ge as-deposited sample. Furthermore, the Ge +2 oxidation state is increased in intensity, while Ge +3 oxidation state is decreased slightly when the ALD cycle is increased from 3 to 7. We can also observe very strong intensity of Ge 3d peaks for TmOx/Ge samples in this work, and also their shift towards higher binding energy in comparison to spectrum in reference [200], which relates to 5 nm Tm_2O_3/Ge. Also, there is no Tm 5p peak for samples deposited using 3 and 7 ALD cycles. Table 3.6 summarises the binding energies of fitted Ge $3d_{5/2}$ with their area percentage for TmO_x/Ge samples, whereas Table 3.7 compares the chemical shifts observed for different Ge oxidation states from our work with values from the literature [64], [68], [199], [200], [221]–[226].

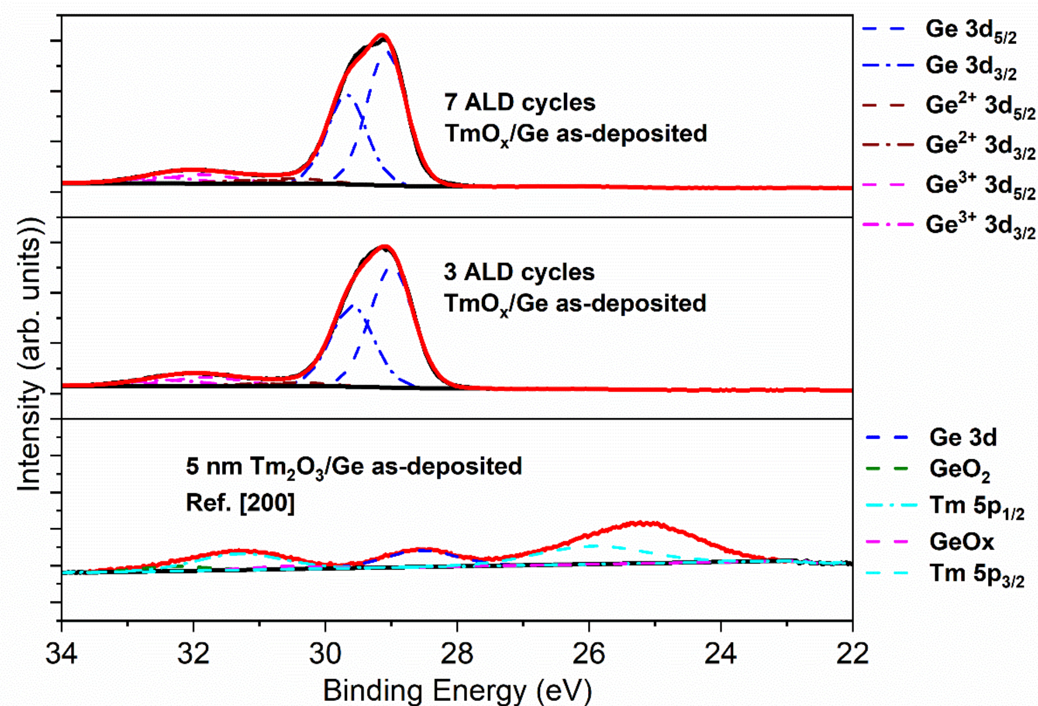

Figure 3.21: Ge 3d XPS CL fitted spectra for 3 and 7 ALD cycles TmO_x/Ge as-deposited samples compared to the similar spectrum from previous work [200].

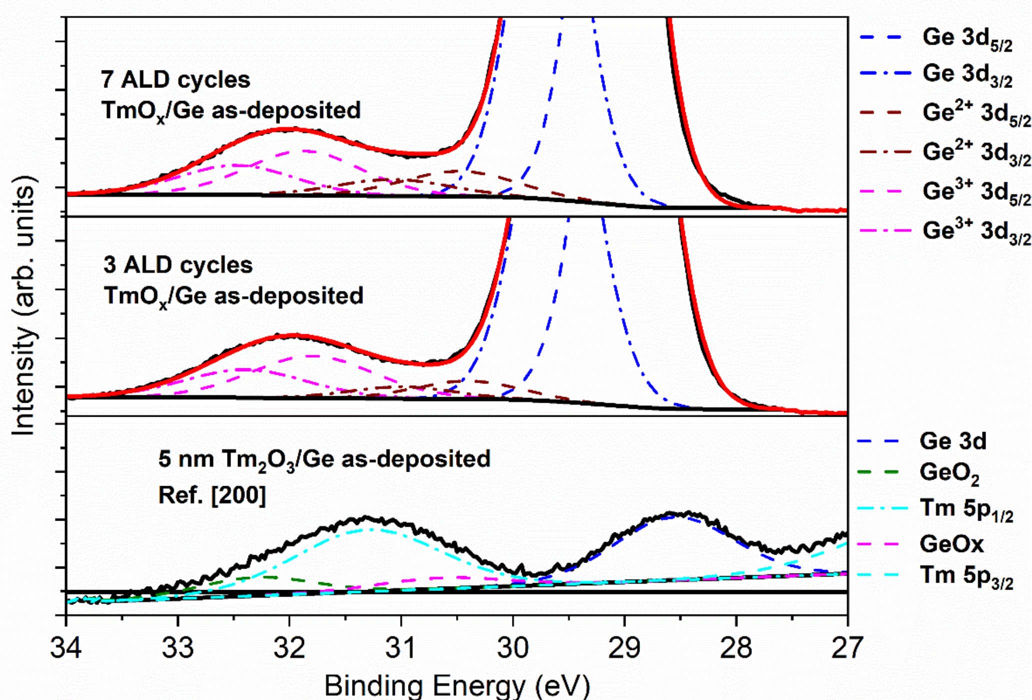

Figure 3.22: Enlarged Ge 3d XPS core level for as-deposited TmO_x/Ge samples formed using 3 and 7 ALD cycles and compared to the similar spectrum from previous work [200]. Note that there is no Tm $5p_{3/2}$ component for TmO_x/Ge samples.

Table 3.6: The binding energy of fitted components of Ge $3d_{5/2}$ peak with their area percentage for TmO_x/Ge samples fabricated using 3 and 7 ALD cycles.

Ge $3d_{5/2}$	Binding Energy (eV), Area (%)				
	Ge^0	Ge^{1+}	Ge^{2+}	Ge^{3+}	Ge^{4+}
3 ALD cycles, TmO_x/Ge, as-deposited	29.00, 51.44	-	30.40, 2.27	31.80, 6.28	-
3 ALD cycles, TmO_x/Ge, annealed in O_3 at 350 °C	29.00, 46.70	-	30.40, 2.64	31.80, 7.74	32.50, 2.91
3 ALD cycles, TmO_x/Ge, annealed in N_2 at 550 °C	29.01, 49.67	-	30.41, 3.19	31.81, 7.13	-
7 ALD cycles, TmO_x/Ge as-deposited	29.08, 50.62	-	30.48, 3.36	31.88, 6.00	-
7 ALD cycles, TmO_x/Ge, annealed in O_3 at 350 °C	29.01, 45.68	-	30.41, 3.25	31.81, 9.83	32.51, 1.23
7 ALD cycles, TmO_x/Ge, annealed in N_2 at 550 °C	29.00, 49.60	-	30.40, 4.13	31.80, 6.26	-

Table 3.7: A summary of the chemical shift values for different Ge oxidation states (1+, 2+, 3+ and 4+) in this work and from the literature.

Ge 3d CL	Core level shifts (eV)			
	Ge^{1+} (Ge_2O)	Ge^{2+} (GeO)	Ge^{3+} (Ge_2O_3)	Ge^{4+} (GeO_2)
This work	-	1.4	2.8	3.5
Schmeisser *et al.* [222]	0.8	1.8	2.6	3.4
Zhang *et al.* [223]	0.8	1.8	2.6	3.65
Mitrovic *et al.* [200]	-	2.0-2.2	-	~ 3.5
Mitrovic *et al.* [64]	-	-	-	3.4
Prabhakaran *et al.* [68]	-	1.4	-	3.2
Wada *et al.* [224]	0.8	1.8	2.6	3.4
Brunco *et al.* [199]	0.8	1.8	2.6	3.4
Dimoulas *et al.* [225]	-	-	-	3.0
Baldovino *et al.* [226]	-	-	-	3.2
Molle *et al.* [221]	0.7 ± 0.5	1.7 ± 0.1	2.81 ± 0.06	3.5 ± 0.1

Figures 3.23 and 3.24 show the Tm 4d XPS core level spectra for TmO_x/Ge samples fabricated using 3 and 7 ALD cycles, as-deposited and annealed. It can be seen that the Tm 4d peak in this work at ~176.3 eV has a very small intensity and is shifted towards higher BEs compared to Tm 4d peak reported previously at ~175.3 eV for Tm_2O_3/Ge [200], where a strong presence of Tm 4d has been observed with no Ge 3s component at ~180.8 eV. Therefore, it can be concluded that the films deposited using 3 and 7 ALD cycles on Ge, are Ge-rich at the interface and comprise of non-stoichiometric TmO_x. In order to produce stoichiometric Tm_2O_3 films on Ge, the parameters influence the deposition of Tm_2O_3 on Ge such as the annealing temperature at different ambient conditions and the ALD cycles should be comprehensively studied. Since these 3 and 7 cycles ALD are not sufficient to produce Tm_2O_3 layer,

then it is suggested that the ALD cycles should be added. Recent work reported that 40 ALD cycles is sufficient to form 7 nm of Tm_2O_3 layer deposited on GeO_2/Ge [85].

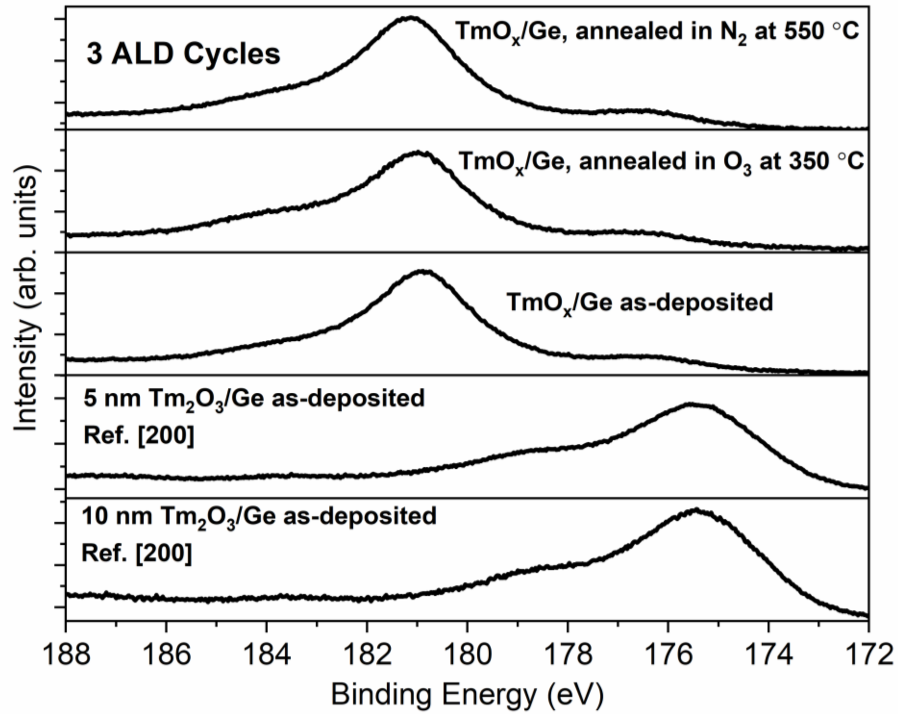

Figure 3.23: Tm 4d XPS core level spectra for TmO_x/Ge samples deposited using 3 ALD cycles, as-deposited and annealed samples compared to similar spectra from previous work of 5 and 10 nm Tm_2O_3/Ge [200].

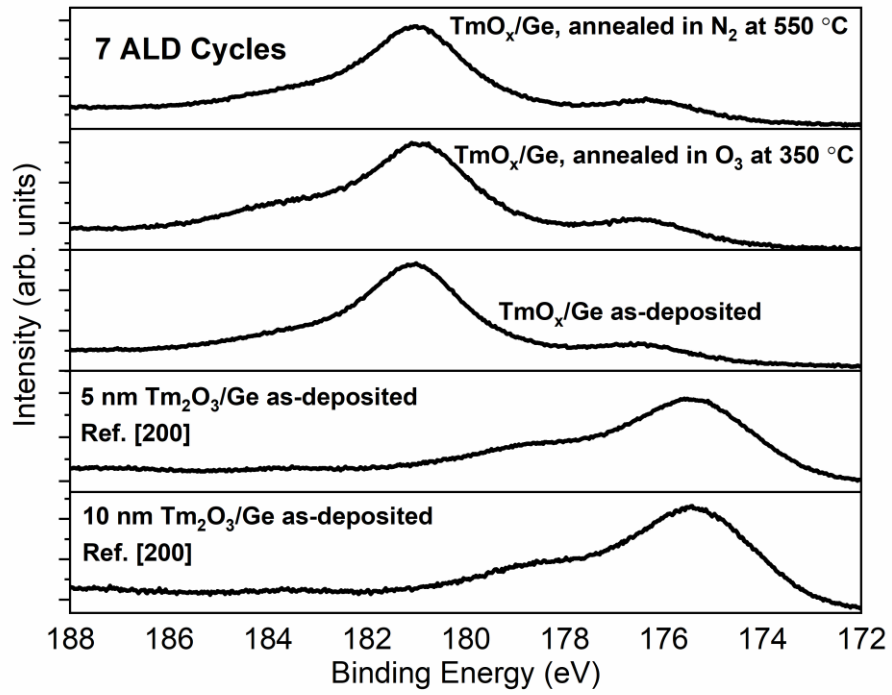

Figure 3.24: Tm 4d XPS core level spectra for TmO_x/Ge deposited using 7 ALD cycles for as-deposited and annealed samples compared to similar spectra from previous work of 5 and 10 nm Tm_2O_3/Ge [200].

3.4 Conclusion

The TmSiO has been considered to be a contender for interfacial layer in HfO_2/TiN MOSFETs, since it has been shown that it can achieve ~20% higher channel mobility compared to the conventional SiO_x/HfO_2 dielectric stack [191]. Furthermore, an optimised annealing condition of 550 °C for Tm_2O_3/Si has been reported to give TmSiO/HfO_2 gate leakage current density comparable with state-of-the-art SiO_x/HfO_2 *n*FETs (0.7 A/cm^2 at a gate bias of 1 V) at sub-nm EOT (as low as 0.6 nm), low subthreshold slopes (65-70 mV/decade before FGA), and near-symmetric threshold voltages (0.5 V for *n*FETs and -0.4 V for *p*FETs). The purpose of this chapter was to elucidate physical properties of Tm_2O_3/IL/Si interface, where IL (TmSiO) has been formed using different PDA temperatures, from 550 to 750 °C. It has been found that the best-scaled stack (sub-nm IL) is formed at 550 °C PDA and that it has a graded interface layer with a strong SiO_x component, with the dominance of Si^{3+} oxidation state. The HRTEM images as well as elemental EELS depth profiles confirm the formation of TmSiO after PDA, in agreement with fitted Si 2p and Tm 4d XPS CL spectra. Furthermore, the valence band offset of Tm_2O_3/Si has been measured experimentally using XPS and Kraut's method. A large valence band offset (± 0.2 eV) of 2.8 eV and a large conduction band offset (± 0.2 eV) of 1.9 eV have been derived for Tm_2O_3/Si, in close agreement with the most recent study of CBO (1.68 ± 0.2 eV) determined from electrical current-voltage measurements and Fowler-Nordheim plots. These large band offsets are important in providing sufficiently high barriers for both electrons and holes in order to suppress high leakage currents.

Furthermore, a small number of ALD cycles (3 and 7) has been used to deposit thin TmO_x films on Ge, to determine if sub-nm films of stoichiometric Tm_2O_3 can be

grown on Ge. The XPS studies of these samples, as-deposited and annealed in O_3 and N_2, show very strong Ge 3d and Ge 3s peaks. Furthermore, the higher binding energy side of the main Ge 3d peak reveals the formation of GeO_x sub-oxides such as both Ge +2 and Ge +3 oxidation states associated with GeO and Ge_2O_3. A small Ge^{4+} peak referring to GeO_2 layer appears only to be present for TmO_x/Ge samples annealed in O_3, but is negligible for as-deposited and N_2 annealed samples. Ge +2 oxidation state has been found to increase in intensity, while Ge +3 oxidation state decreases slightly when the ALD cycle is increased from 3 to 7. Moreover, Tm 4d XPS CL spectra have shown very small intensity indicating non-stoichiometric TmO_x, while very pronounced Ge 3s CLs. The results indicate that 3 and 7 ALD cycles are insufficient to produce stoichiometric Tm_2O_3 films on Ge. Therefore, the parameters influence the deposition of Tm_2O_3 on Ge such as the annealing temperature at different ambient conditions and the ALD cycles should be critically studied in order to produce stoichiomentric layer of Tm_2O_3 on Ge.

CHAPTER 4

Band Alignment of Sputtered Dielectrics on GaN

4.1 Introduction

One of the important parameters which have a significant impact on the properties of GaN-based metal-insulator-semiconductor (MIS) structures is the band alignment between the gate dielectric layer and GaN layer. As mentioned earlier in Chapter 1, the dielectric materials should provide the potential barrier at each band of over 1 eV between the oxide and GaN layer in order to inhibit conduction by the Schottky emission of electrons or holes into the oxide bands [10], [12], [13] as illustrated in Figure 4.1. This requirement is needed to maintain low gate leakage current as well as small equivalent oxide thickness (EOT) [10].

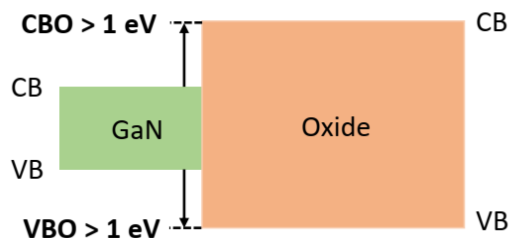

Figure 4.1: The requirement of large band offsets of over 1 eV at oxide/GaN interface.

The band alignment between the oxide and semiconductor interfaces can be determined using various experimental methods such as external photoemission spectroscopy [227], [228], internal photoemission spectroscopy [229], [230] and X-ray photoemission spectroscopy (XPS) core level (CL) based method [201], [231] as well as by theoretical calculations using charge neutrality level (CNL) [12], [150]. The method of Kraut *et al.* [201], [231] using XPS has been established as a reliable way to determine band offsets at the heterojunction interface. This method has also been

successfully used to provide insights into interfacial properties between different materials [231], [232]. It is based on using an appropriate shallow CL position as a reference. Generally, this approach is based on the assumption that the binding energy (BE) difference between a CL position and valence band maximum (VBM) is fixed in the bulk of semiconductor or oxide material. Figure 4.2 illustrates the basic principle of XPS band offsets measurement for two different materials (denoted as material 1 and material 2) which represent semiconductor and oxide. The BE difference between a CL and the VBM for both the single layer dielectric and semiconductor of interest are measured first. Then, the BE difference between the two reference CLs in the heterojunction is also measured. Therefore, the valence band discontinuity/offset (ΔE_V) or known as valence band offset (VBO) can be determined by combining these three quantities corresponding to the bulk semiconductor, oxide/semiconductor interface and bulk oxide.

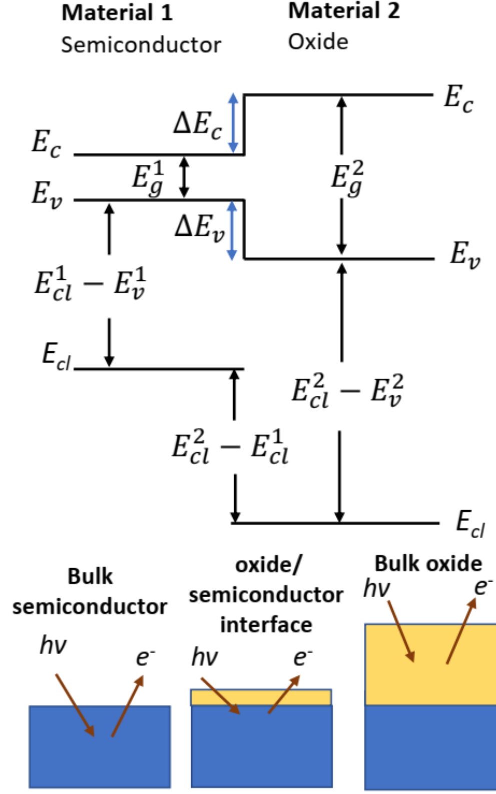

Figure 4.2: A schematic energy band diagram illustrating the basic principle of XPS band offset measurements based on Kraut's method [201], [231].

In this work, the VBO between the oxide and GaN is labelled as ΔE_V and can be extracted using Kraut's method [201], [231] as shown in this equation:

$$\Delta E_V = [E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)] - [E_{CL}^{oxide}(bulk) - E_{VBM}^{oxide}(bulk)] + \Delta E_{CL} \tag{4.1}$$

$$\Delta E_{CL} = E_{CL}^{GaN}(interface) - E_{CL}^{oxide}(interface) \tag{4.2}$$

where $[E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)]$ and $[E_{CL}^{oxide}(bulk) - E_{VBM}^{oxide}(bulk)]$ are the BE differences between the chosen reference CLs and their respective valence band maxima for GaN and bulk oxide samples respectively, while ΔE_{CL} is the BE difference of the two chosen CLs for the interfacial sample. Moreover, the conduction band offset

(CBO) or labelled as the conduction band discontinuity (ΔE_c) can be calculated using Equation 4.3.

$$\Delta E_C = E_g^{oxide} - E_g^{GaN} - \Delta E_V \quad (4.3)$$

where E_g^{oxide} and E_g^{GaN} are the band gaps of oxide and GaN substrate, respectively.

4.2 Band alignment of Ta_2O_5/GaN

The inclusion of a Ta_2O_5 layer has been found to result in good interface quality with GaN and its high dielectric constant with reported values of 22–25 [10], [154], leads to improved transconductance. Ta_2O_5 is a key high-*k* material for next generation MOS due to its high breakdown electric field of 4.5 MV, a low leakage current of < 10^{-8} A/cm^2 at 1 MV/cm as well as good step coverage [233]–[235]. Moreover, Ta_2O_5 used as a gate dielectric in capacitors fabricated on GaN has shown low fixed oxide charge density and low midgap interface trap density of 2.18×10^{11} cm^{-2} and 2.60×10^{11} cm^{-2} eV^{-1}, respectively [236]. So far only a theoretical value of the CBO has been reported for Ta_2O_5/GaN using the method of CNL [12], [150]. In this work, the experimentally derived band alignment of the Ta_2O_5/GaN material system using X-ray Photoelectron Spectroscopy and Variable Angle Spectroscopic Ellipsometry (VASE) were investigated. Different wet chemical cleaning procedures for the GaN surface were investigated prior to oxide deposition. The Ta_2O_5 thin films (up to 10 nm) were deposited by RF (radio frequency) magnetron sputtering.

4.2.1 Experimental

Sawangsri Kriangkamon from the Department of Electrical Engineering and Electronics, University of Liverpool, UK is acknowledged for his contribution in the

experimental work including the deposition of Ta_2O_5 on GaN as well as an XPS and VASE measurements. The Ta_2O_5 films were deposited by RF magnetron sputtering on a wafer of 2 μm GaN (0001) film grown on Si (111) substrate by metal organic chemical vapour deposition. Prior to Ta_2O_5 deposition, surface cleaning of GaN was carried out to minimise C and O contaminants [237], [238]. Both acetone [239] and methanol [240] have been reported to be used for GaN surface cleaning. Trichloroethylene (TCE) has also been used to remove grease [240], [241]. Diale *et al*. have reported $(NH_4)_2S$ as the best etchant compared to HCl and KOH in aqueous solution [241]. The cleaning of GaN started with a rinse in acetone with ultrasonic agitation for 10 min followed by methanol for further 10 min. Then the samples were dipped in three different etchants separately: 30% NH_4OH, 20% $(NH_4)_2S$, and 37% HCl solution followed by a rinse in deionised (DI) water. Ta_2O_5 films were then sputter-coated onto HCl pre-treated GaN by non-reactive RF magnetron sputtering at room temperature with argon pressure of 5 mTorr and a sputtering power of 100 W. The target was 3-inch Ta_2O_5 with purity of 99.99%; the sample-to-target distance was 11 cm. The sputtering was done with durations of 3 and 15 min for the interfacial (nominal 3 nm) and bulk (nominal 10 nm) Ta_2O_5/ GaN samples respectively, using AJA International apparatus. The average surface roughness, R_a of the GaN and Ta_2O_5 bulk samples was found to be 0.99 nm and 0.42 nm with root-mean-square (RMS) of 1.28 nm and 0.57 nm (± 0.1 nm) respectively over 10 μm×10 μm area by Veeco di Innova atomic force microscope, operated in contact mode as shown in Figure 4.3. It can be seen that the roughness of sputtered Ta_2O_5 deposited on GaN is slightly reduced after the deposition process. However, since the effect of sputtering deposition and its process conditions are not well investigated, these results are not to confirm the quality of sputtered Ta_2O_5 layer. The thickness of 10 nm for the bulk Ta_2O_5 sample is well

above the inelastic mean free path (up to 2 nm, [242]) of the photoelectrons at the kinetic energies used in the XPS experiment, to ensure a bulk-like response, that is, all detected photoelectrons originate from the Ta_2O_5 layer.

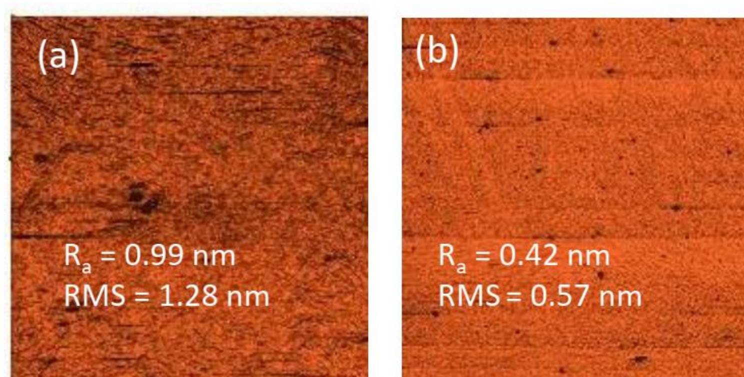

Figure 4.3: Atomic force microscopy (AFM) images of (a) GaN and (b) 10 nm Ta_2O_5 with the scanned area of 10 μm × 10 μm.

The XPS was performed in a standard ultra-high vacuum (UHV) system consisting of a PSP Vacuum Technology dual anode (Mg/Al) X-ray source and a hemispherical electron energy analyser equipped with five channeltrons. For non-monochromatic XPS with AlKα X-ray source (hν = 1486.6 eV) was operated at power of 144 W with 12 mA emission current and 12 kV accelerating voltage. From the XPS point of view, there are two aspects of sources of errors. The data acquisition procedure and background subtraction. In order to record CL spectra, it is necessary to minimise potential instability in the signal, either due to the instrument or the sample. This is done by repeated scan of a CL over several hours, usually 50–100 repeats. When multiple regions were scanned, all regions of interest were scanned sequentially, ensuring that any potential instability would have a similar effect on all the regions. Prolonged scanning also ensured that the detection limit, which is proportional to the square root of the number of scans, was much less than 1 %. The choice of background function can have an effect on peak areas and hence the a full width at half maximum

(FWHM). In this work, the choice was the Shirley background, for which the background intensity at the peak binding energy is proportional to the total area in the energy defined between the peak and an end point on the low binding energy side. Generally, the end points were selected such that a reasonable fit of peak components was achieved. Having followed this procedure throughout and using Ag $3d_{5/2}$ peak as a reference, and which was acquired under similar instrumental conditions, the reference peak (FWHM) could be fitted using 6 points, giving an uncertainty of ± 0.2 eV. This is the precision with which parameters such as FWHM and CL binding energy were determined. It should be noted that physically, the energy resolution of the instrument is a convolution of the X-ray source size in terms of energy, the analyser energy resolution which is determined why the pass energy absolutely, and the inherent line width of the CL. In the instrument used in the current work, the X-ray source contribution was the dominant contribution.

The probe area during the XPS measurements was 1 mm^2. The survey scan was carried out at a pass energy of 100 eV in the 0–1250 eV energy range to determine the elements present in the samples and to check for surface contamination. Then, the detailed scan for individual CL regions were recorded at a pass energy of 50 eV. Then the individual CL regions, such as Ga 2p, O 1s, N 1s, C 1s, Cl 2p, Ta 4f, Ga 3d and valence photoelectron lines were recorded. During the XPS measurements, the X-ray beam exposure was across the whole sample [243], [244] to diminish the effect of differential charging when evaluating the VBO. The individual CL scans were performed for a duration of at least an hour until the point that they attained constant binding energies, and the samples could be considered as charge saturated. The electron BEs were then corrected by setting the Ga 2p CL peak in the spectra to 1117.7 eV for all samples. Note that C 1s correction at 284.6 eV is widely used [219], however

for the spectra measured in this work, the former peak is found to be broad and of low intensity leading to erroneous calibration. A Shirley-type background [202] is used during the fitting of all spectra. The CL positions are defined as the FWHM by fitting a Lorentzian– Gaussian curve to the measured peaks, which introduces typically an error of ± 0.08 eV to the determination of VBO. The error bar (± 0.25 eV) defined in this work is due to VBM estimation through the linear interpolation method [203]. Room temperature VASE measurements were performed using a J.A.Woollam M2000 ellipsometer with a wavelength range of 241.1 nm–1686.7 nm which corresponds to an energy range of 0.7 eV – 5.2 eV at three incident angles 65°, 70° and 75° to maximize the accuracy in extracting thickness, optical properties and band gap of the GaN and Ta_2O_5 layers. Figure 4.4 (a) shows XPS background subtracted O 1s CL for GaN surface treated using the three different etchants: NH_4OH, $(NH_4)_2S$ and HCl. It is evident that the HCl treatment shows the lowest oxygen contamination. There is an indication of Cl on the surface for HCl treated GaN as can be seen from Figure 4.4 (b). From the deconvoluted Cl 2p peak, the Cl $2p_{3/2}$ component is at 199 eV. It is known that Cl $2p_{3/2}$ for metallic chloride is in the range of BEs of 198.5–199 eV, while that of organic chlorine is at the BE of 200 eV and above [242]. Hence, it can be deduced that the chlorine present in this sample is in the form of gallium chloride likely to be due to Ga-rich surface [245].

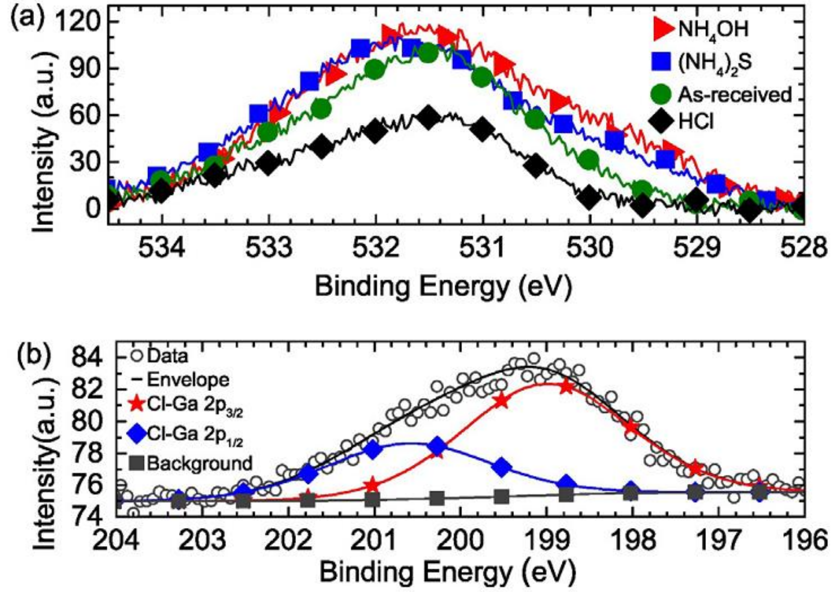

Figure 4.4: (a) Background subtracted O 1s core level after different cleaning treatments (NH_4OH, $(NH_4)_2S$, and HCl) of GaN surface as compared to as-received GaN substrate reference sample. (b) Background subtracted Cl 2p core level of the GaN surface after HCl cleaning treatment.

4.2.2 Thickness and band gap estimation using VASE

The VASE fitting for the GaN substrate was started in the transparent region using the Cauchy model:

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \tag{4.4}$$

where n is the refractive index, λ is the wavelength, and A, B and C are parameters initially set to the values from Kim *et al*. [246]. Then these parameters were varied with the thickness of the GaN layer to fit the experimental data. The VASE fitting for the full wavelength region (241.1 – 1686.7 nm) was done using a parametric model [247], and the thickness of the GaN layer was found to be 2008 ± 2 nm, in close agreement with the nominal value of 2 μm. The VASE experimental and fitted data of psi (Ψ) and delta (Δ) for three incident angles (60°, 65°, and 70°) for the GaN substrate are shown in Figure 4.5. The modelling of interfacial and bulk Ta_2O_5/GaN samples

was done using the Tauc-Lorentz oscillator model for a Ta_2O_5 layer on top of the GaN layer and fitted to extract the thickness and the band gap. Figure 4.6 shows Ψ and Δ experimental and fitted ellipsometry angles for bulk Ta_2O_5/GaN sample in the transparent region. The mean squared error (MSE) between the experimental and theoretical (fitted) curves was in all cases below 5, consistent with a good quality fit of the data. The thickness of the interfacial and bulk Ta_2O_5 was found to be 2.8 ± 0.2 nm and 10.6 ± 0.2 nm, respectively, consistent with the nominal values. The resulting dielectric function spectra, ε_1 and ε_2, for GaN and Ta_2O_5, are shown in Figure 4.7 (a) and (b) respectively. The band gap is obtained by linear extrapolation of the leading edge of the ε_2 spectra to the baseline from VASE measurement. Therefore, the band gap of GaN was found to be 3.34 ± 0.15 eV (Figure 4.7 (a)) which is in close agreement to the previously reported values of 3.4 eV [147], [148], [246], [248], [249] and 3.44 eV [250]. The obtained band gap value for Ta_2O_5 is 4.4 eV in agreement with the same literature value [25,26].

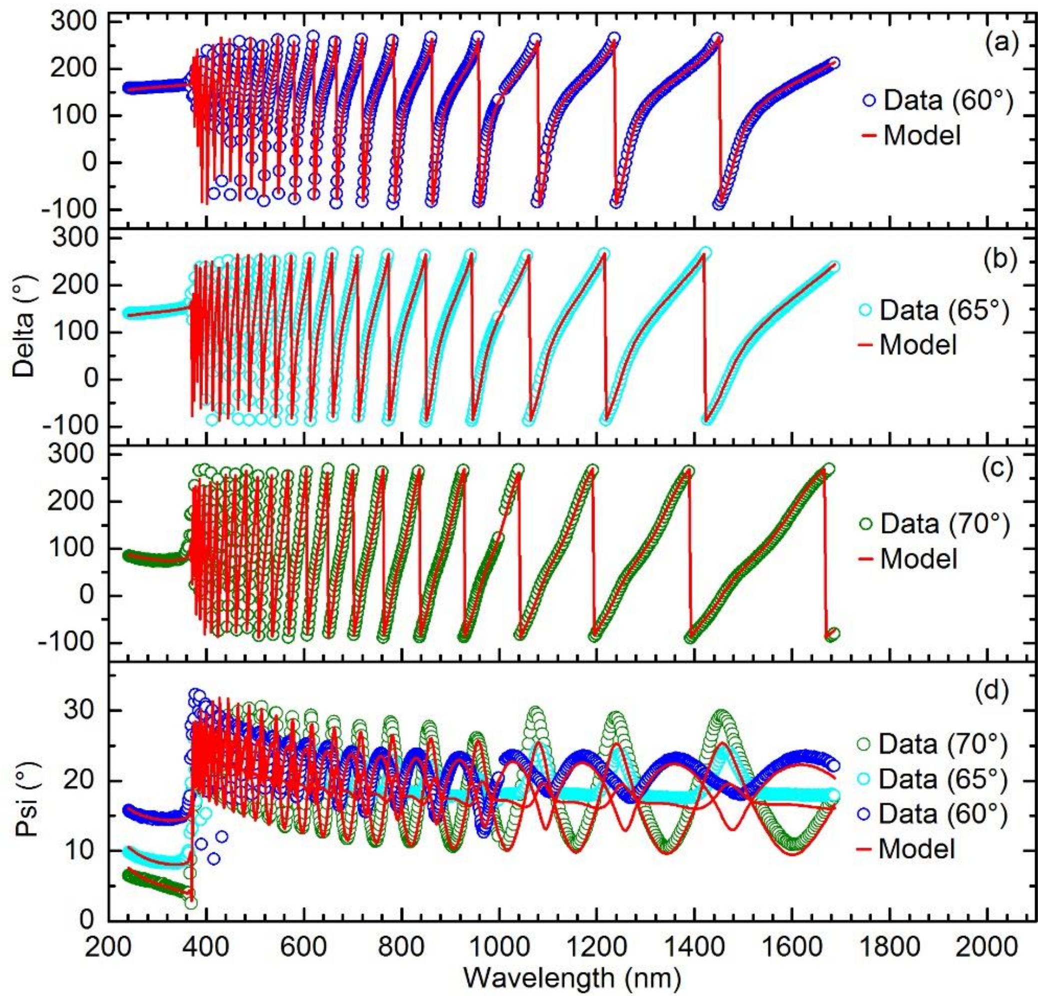

Figure 4.5: VASE data for the GaN sample (circle) and the best multiple-layer model fit (full line) in the wavelength range of 240–1700 nm: Δ for incident angles (a) 60°, (b) 65°, (c) 70°, and (d) Ψ for three incident angles (60–75°).

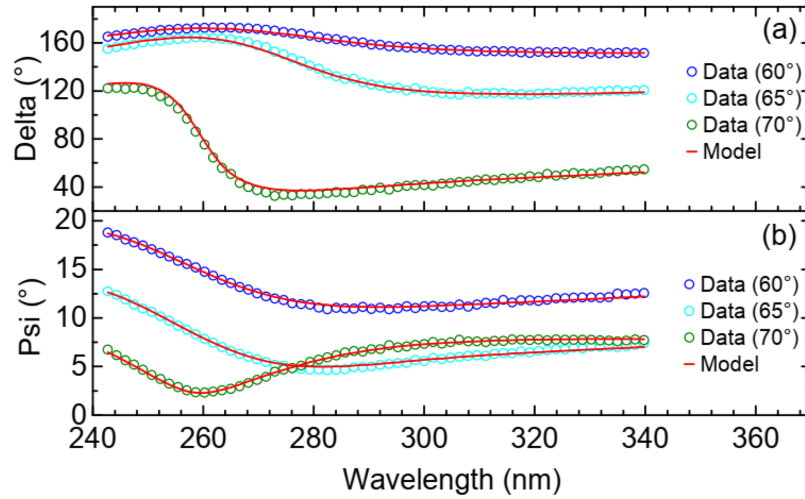

Figure 4.6: VASE data for the bulk Ta_2O_5/GaN sample (circle) and the best model fit (full line) in the transparent wavelength region (240–340 nm): (a) Δ and (b) Ψ for three incident angles (60 – 75°). The thickness of Ta_2O_5 is estimated to be 10.6 ± 0.2 eV.

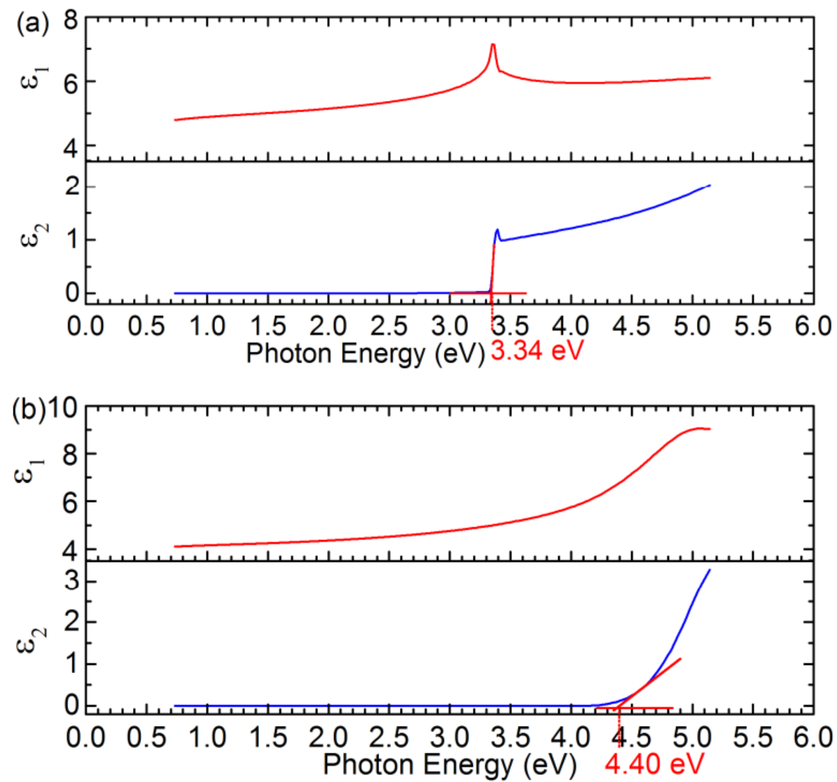

Figure 4.7: Photon energy dependence of parametric dielectric function, ε_1 and ε_2, for (a) as-received GaN substrate, and (b) 10 nm (nominal) Ta_2O_5/GaN.

4.2.3 Band offsets estimation

In our work, the VBO value was calculated using Kraut's method using Equations 4.1 and 4.2. The $E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)$ refers to the BE difference of Ga 3d CL and VBM for GaN substrate (Figure 4.8 (a)), $E_{CL}^{oxide}(bulk) - E_{VBM}^{oxide}(bulk)$ of Ta 4f CL and VBM for Ta_2O_5 bulk sample (Figure 4.8 (b)), and ΔE_{CL} of Ga 3d and Ta 4f CLs for interfacial Ta_2O_5 sample (Figure 4.8 (c)). It can be seen from Figure 4.8 (a) that the Ga 3d peak for GaN substrate can be deconvoluted into seven components, related to Ga-N, Ga-O, Ga-O bonds (each with its spin-orbit splitting sub-peaks) and N 2s in the lower BE side of the main peak (~16.7 eV). For the Kraut's method, the Ga-N component has a BE of 19.94 eV and fitted with the spin-orbit splitting of 0.45 eV and the peak intensity ratio (Ga $3d_{3/2}$:Ga $3d_{5/2}$) of 0.67. For the Ta_2O_5 bulk sample, as shown in Figure 4.8 (b), Ta 4f CL is fitted with two pairs of sub-peaks referring to Ta-O bonds with spin-orbit splitting corresponding to the main (stoichiometric) oxide and sub-oxide. The spin-orbit splitting for the dominant Ta 4f oxide component, centred at 25.89 eV, was 1.91 eV with the intensity ratio (Ta $4f_{5/2}$:Ta$4f_{7/2}$) of 0.75. The VBM was determined by linearly extrapolating the Fermi edge to the base line in the valence band spectra [203] and found to be 2.22 eV for GaN substrate and 2.42 eV for Ta_2O_5 bulk sample as shown in the insets of Figure 4.8 (a) and (b). Hence, the calculated values of $E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)$ and $E_{CL}^{oxide}(bulk) - E_{VBM}^{oxide}(bulk)$ are 17.72 eV and 23.47 eV, respectively. The value of $E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)$ is in agreement with literature values, where the VBO is found to be 17.7 eV [232] in SiO_2/GaN and 17.76 $\pm$ 0.03 eV in AlN/GaN [251]. It is worth mentioning that calculations of both $E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)$ and $E_{CL}^{oxide}(bulk) - E_{VBM}^{oxide}(bulk)$ from the measured XPS CL peaks are independent of band bending (BB) at the interface. The amount of BB, as predicted from Poisson's equation, is caused by the

spatially varying electrostatic potential and is dependent on the distance from the surface [252]. Using the same spin-orbit splitting and intensity ratios deconvolution for Ga 3d and Ta 4f CLs for interfacial Ta_2O_5 sample shown in Figure 4.8 (c), ΔE_{CL} is found to be 6.45 eV. Comparing the Ga 3d CL of the GaN substrate (19.94 eV, see Figure 4.8 (a)) and the same peak from GaN with Ta_2O_5 on top (19.89 eV, Figure 4.8 (c)), a 0.05 eV energy shift towards lower BEs is observed. The latter is a signature of a small upward BB [253], likely to be due to spontaneous polarisation in GaN that can lead to a negative bound polarisation charge at the GaN surface and ionised donors to compensate these defects [254]. The angle-resolved XPS Ga 3d and Ta 4f CL spectra taken from interfacial Ta_2O_5/ GaN sample at three grazing angles 30°, 50° and 70° as shown in Figure 4.9 confirm the CL variation of < 0.05 eV and substantiate a negligible band bending at the interface [153], [255], [256]. The value of VBO from the above data and using Equations 4.1 and 4.2 was calculated to be 0.70 ± 0.25 eV, which with the band gap extracted by VASE gives CBO =0.36 ± 0.25 eV using Equation 4.3.

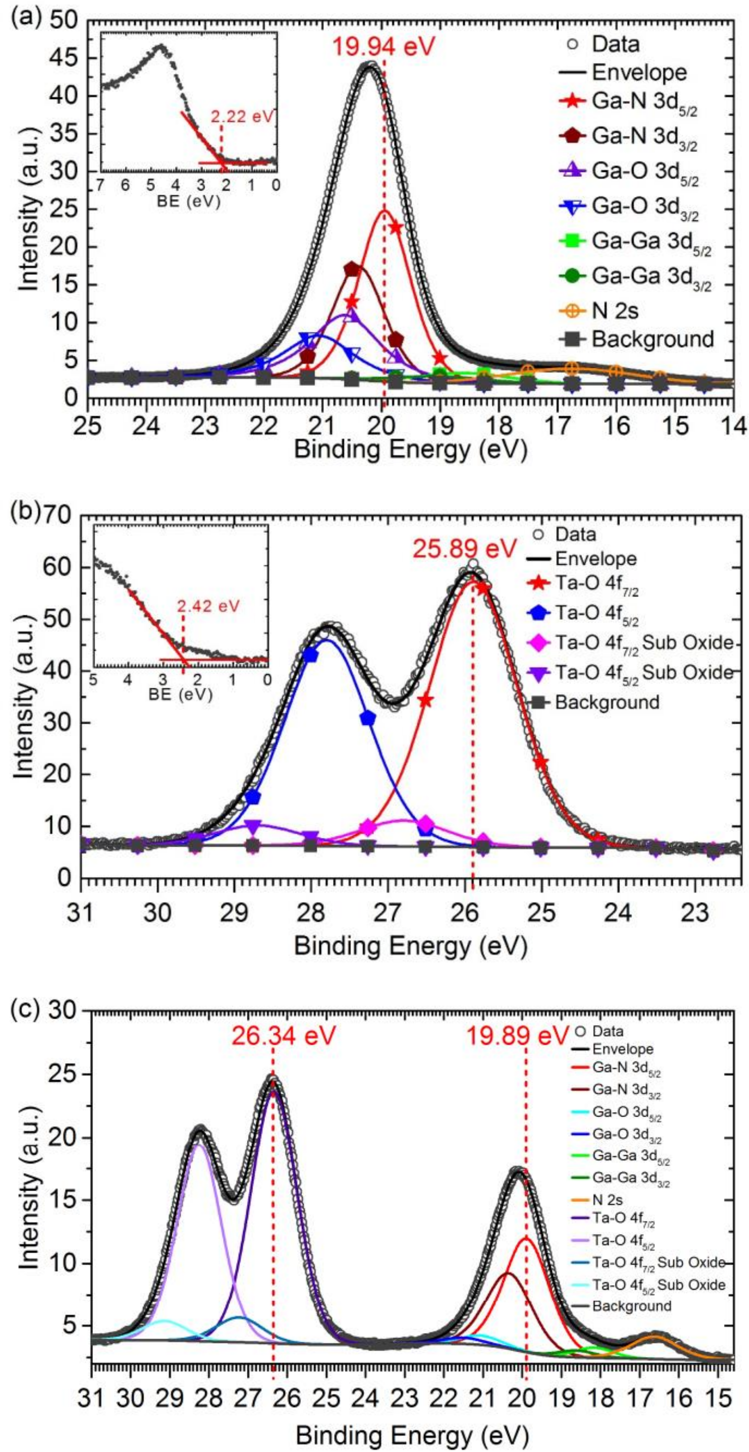

Figure 4.8: The XPS spectra of (a) Ga 3d CL for GaN substrate; (b) Ta 4f CL for bulk Ta_2O_5/GaN sample; (c) Ga 3d and Ta 4f CLs for interfacial Ta_2O_5/GaN sample showing the difference between the CLs. The insets in (a)–(b) show the VBM estimation from valence band leading edge linear fitting. The envelope refers to the fitted curve to experimental data.

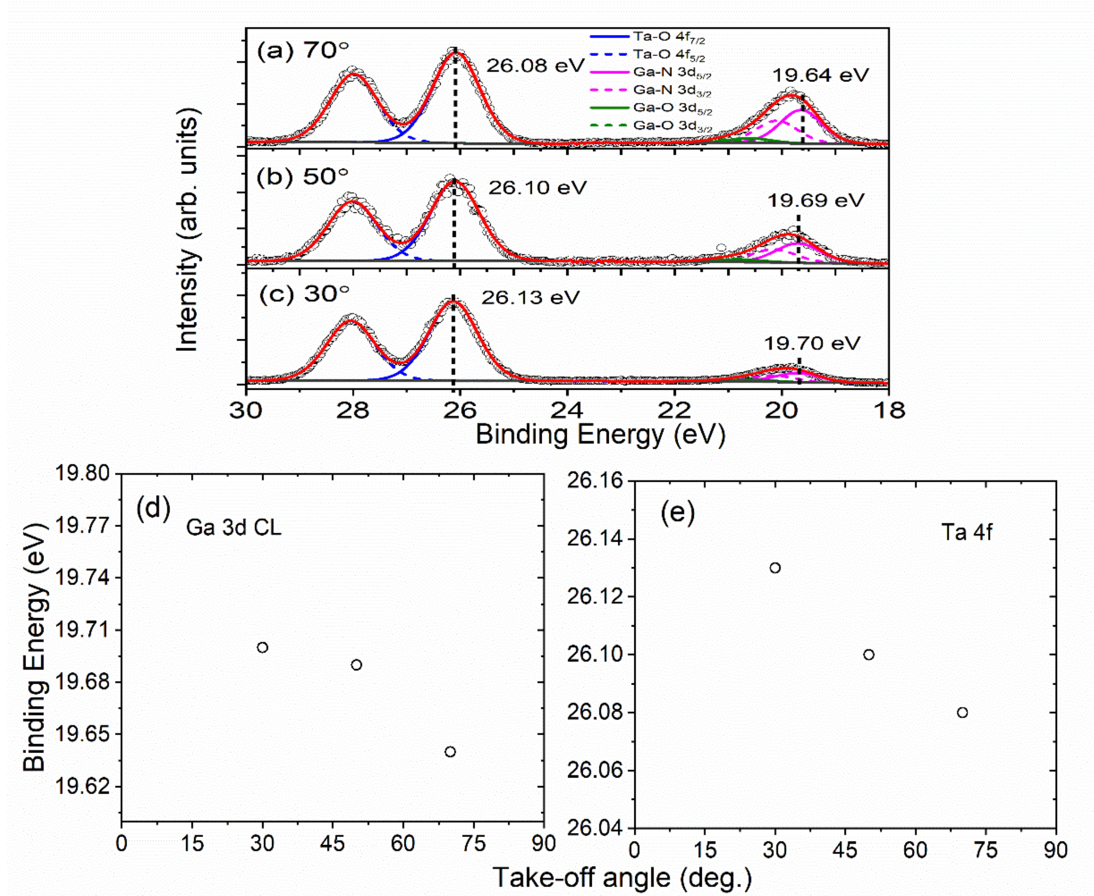

Figure 4.9: Ta 4f and Ga 3d CLs at three different angles (a)-(c) and the dependence of measured binding energies on take-off angles (TOA) ((d) and (e)) for 3 nm Ta_2O_5/GaN

The derivation of the energy band diagram using XPS for Ta_2O_5/GaN in this work is illustrated schematically in Figure 4.10. The obtained VBO value of 0.7 eV from this work compares to the theoretically predicted value of 1.1 eV [150]. It is worth mentioning that the value of band gap for GaN used in Ref. [150] is 3.2 eV; assuming a more widely cited value of 3.4 eV [125], [237], [246], [249], [257] for GaN band gap and the theoretically calculated CBO value of 0.1 eV [150] would imply a VBO of ~0.9 eV, this being consistent with the value obtained in this work within the experimental error of the XPS method. It is evident from the results that both CB and VB offsets of Ta_2O_5 on GaN are smaller than 1 eV. A possible approach to utilise Ta_2O_5 advantages of higher *k* and good interface properties in GaN-based MIS-

HEMTs could be to mix it with other oxides with larger band gap such as Al_2O_3. It has been shown recently that the complementary characteristics of Ta_2O_5 and Al_2O_3 could be combined by fabricating $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ as a gate dielectric to achieve both a high dielectric constant (high-*k*) and a sufficient CBO to the GaN HEMT for low leakage currents [157].

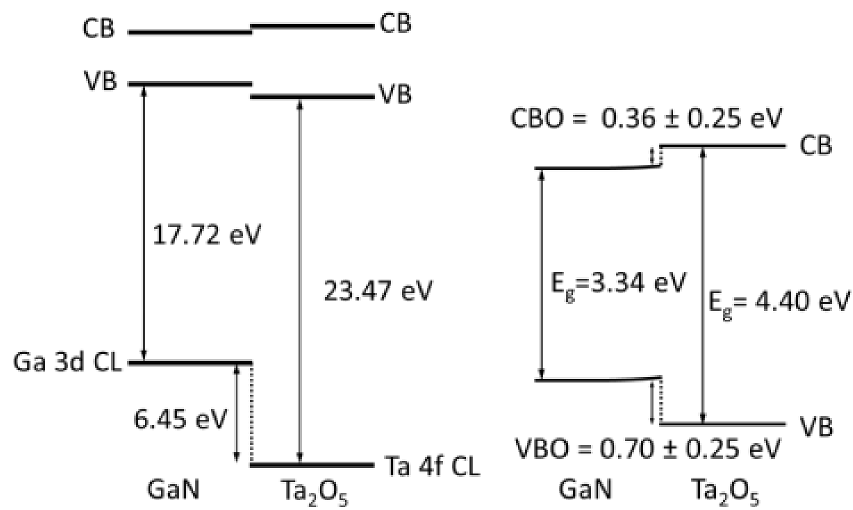

Figure 4.10: Band diagrams of experimentally derived band alignment for the Ta_2O_5/GaN interface: (left) Kraut's method for VBO measurement, and (right) CBO derived using band gap energies measured by VASE.

4.3 Band alignment of ZrO_2/GaN, Al_2O_3/GaN and MgO/GaN

The introduction of the high-*k* gate dielectric layer may also affect the device performance such as leakage current, lower channel mobility and threshold voltage instability. High band gap gate dielectric materials are preferable as they can provide higher tunnelling barriers for electrons and holes, which result in lower gate leakage current. On the other hand, high dielectric constant (high-*k*) material is also necessary for improved electrostatic control over the channel and improved on-current, which in-turn results in higher transconductance. The quality of the gate dielectric and the

dielectric/GaN interface also plays a central role in device performance due to potential problems arising from fixed oxide charge, border and interface traps (fast and slow states). The origin of interface traps may be due to structural damage, oxidation induced defects or dangling bonds [258]. The dynamic charging and discharging of the trap states leads to threshold voltage instability, large hysteresis and significant current collapse [259], which affect the switching performance. Proper selection of high-*k* dielectric materials based on the aforementioned criteria is mandatory. Materials such as SiN [260]–[262] and Al_2O_3 [261], [263] have been used in an attempt to passivate the interface, however high interface state densities (D_{it}) of ~3 $\times 10^{12}$ cm^{-2}eV^{-1} [260] and 3.4 $\times 10^{12}$ cm^{-2}eV^{-1} [261], respectively have been reported. Atomic layer deposition (ALD) of Al_2O_3 [123], [264], [265] is the most commonly used gate dielectric deposition process. Alumina offers a large band offset with GaN material, high dielectric constant (k ~ 8.6 – 10), high breakdown electric field (~ 10 – 30 MV/cm) and good interface quality with an average D_{it} of ~7 $\times 10^{10}$ cm^{-2}eV^{-1} and a corresponding hysteresis voltage of 100 mV [143]. In 2012, Yang *et al.* [123] reported a large VBO of 1.8 eV for plasma-enhanced (PE)-ALD deposited Al_2O_3 on HCl-treated n-type GaN. In this work, the theoretical value of 17.8 eV was used as the BE of Ga 3d XPS CL below the VBM for the calculation of VBO by Kraut's method [231]. The combination of XPS and ultraviolet photoemission spectroscopy (UPS) data in [123] gave an indication of a strong upward band bending at 1 nm Al_2O_3/*n*-GaN. It has been shown that spontaneous polarization in GaN results in a surface bound charge, which has been found to be negative in the case of the Ga-face GaN [266]. Thus, a compensating space charge region comprising positive donors forms near the surface, depleting the *n*-type GaN [232], and resulting in a strong upward BB of ~0.9 eV for as-deposited Al_2O_3/GaN [123]. It is evident from the derived

Al_2O_3/GaN band diagram in Ref. [123] that the difference between valence band maxima away from the interface results in a smaller VBO value of 1.2 eV, closer to the values of 0.9 eV [264] and 1 eV [265] reported in the later XPS studies. Duan *et al.* [264] reported that the VBO between Ga-face *n*-type GaN and ALD Al_2O_3 varies with the thickness of the deposited oxide from 0.9 eV for 4 nm Al_2O_3/GaN to 0.7 eV for 1.3 nm Al_2O_3/GaN. The latter has been explained by an upward energy BB at the GaN surface. Furthermore, Jia *et al*. [265] reported VBO (± 0.2 eV) of 1 eV for ALD Al_2O_3 on non-polar m-plane GaN using angle-resolved (AR)-XPS, where the BEs of Ga 2p and Al 2p CLs at 45° take-off angle (TOA) were used in deriving VBO from Kraut's method.

An AR-XPS experimental study of band alignment of ALD ZrO_2 on undoped GaN on sapphire treated with buffered oxide etchant solution, showed a strong upward band bending at the GaN surface as well as a potential gradient of 400 meV in the 2 nm ZrO_2 film; the AR-XPS data at 15°, 45° and 75° TOAs have been used with numerical calculations [267] to extract the BE of Ga 3d CL at 0° for the interfacial 2 nm ZrO_2 film on GaN. The VBO value found from Kraut's method is 0.59 eV; with the addition of the potential gradient in the oxide film, the VBO shifts to ~1 eV [153]. The theoretically predicted value by Robertson *et al.* [150] is even higher, 1.6 eV.

In the case of MgO grown by molecular beam epitaxy (MBE) on hydrofluoric acid (HF)-treated n-type GaN, the Ga 3d and Mg 2p XPS CLs were used, and Kraut's method applied; the VBO was found to be 1.2 ± 0.2 eV, calculated as an average value measured from three samples with thicknesses of 4 nm, 7 nm and 10 nm MgO on GaN [147]. A similar value of 1.06 ± 0.15 eV has been reported by Chen *et al.* [250] for RF plasma-assisted MBE MgO on GaN, using the same reference CLs measured at 45° TOA. The more recent XPS study of MBE deposited MgO on GaN [148] revealed a

higher VBO of 1.65 eV, the value determined from the three measurements on bulk and interfacial samples using Ga 3s and Mg 2p, as well as Ga 3p and Mg 2p CLs [250]. It is worth noting that neither band bending nor the potential drop across the interfacial oxide layer were discussed in aforementioned studies, which may dramatically alter the band offset values as discussed in Refs. [252], [256], [267].

In this work, we report band alignment studies of sputtered ZrO_2, Al_2O_3 and MgO on GaN and make comprehensive comparison with the results published in the literature, particularly focusing on band diagrams derived from XPS and Kraut's method. The sputtering technique has been used to deposit the high-*k* oxides, due to its advantages of low temperature process, low-cost and the availability of a wider range of materials compared to its ALD counterpart. Sputtered films tend to be amorphous whereas ALD are nanocrystalline. ALD deposited high-*k* oxides can experience leakage via grain boundaries. Further, our intention was to compare the characteristics of the sputtered films with those in the literature where ALD and MBE growth techniques have been used. To account for the effect of differential charging [268] and a potential drop across the oxide film, we have used the method of Iwata *et al.* [206], [269] which is based on the extrapolation of the measured BEs to zero oxide thickness and ideally to zero charge. This approach requires that the oxide composition is independent of thickness; hence, a set of thin oxide samples (up to 7 nm) on GaN has been processed under identical conditions. Furthermore, AR-XPS was employed to look into the effect of BB at the interface for all samples.

4.3.1 Experimental

4.3.1.1 *Sputtering procedure*

In this work, NanoPVD (the maximum power of 150 W and the frequency of 13.56 Hz) RF magnetron sputter system developed by Moorfield Nanotechnology is used to deposit oxides such as Ta_2O_5, ZrO_2, Al_2O_3 and MgO. As discussed previously in Chapter 2, this technique involves a gaseous plasma which is generated by ionizing a sputtering gas (generally a chemically inert, heavy gas like Argon) and confined to a space containing the material to be deposited (the target). The surface of the target is eroded by high-energy ions (Ar^+ ions) within the plama, and the ejected atoms/molecules travel through the vacuum environment and deposit onto a substrate to form a thin film. In sputtering, the target material and the substrate is placed in a vacuum chamber. A voltage is applied between them so that the target is the cathode and the substrate is attached to the anode. A detailed description of the sputtering deposition process used for this work is explained below.

1) Venting the chamber (if the chamber already pumped down)
   - The nanoPVD system is turned on and the chiller is set to 18 °C. Then, the service gas (80 psi) , vent gas (50 psi) and process gas (Argon gas) valves are opened. The 'Vent' on main control panel is pressed and wait until the chamber is fully vented. Once the chamber is fully vented, the vent gas valve is closed and the chamber lid can be opened.
2) Placing target, crystal and sample
   - After the chamber lid is opened, then the clean target can be placed correctly on top of the magnetron. It is important to test connections via a multi-meter, i.e. between the target surface and the clamping; between

the outer shield and the inner chamber. In our work, various insulated targets have been used including Ta_2O_5, ZrO_2, Al_2O_3 and MgO with the purity of 99.99 % to deposit different oxides with different thickness.

- The crystal life time is checked using Q-pod and if needed place a new crystal in its holder
- The substrate (or sample) is placed on the substrate holder as shown in Figure 2.2. This chamber can allocate up to four pieces of substrate at the same time of deposition process. For example, several small pieces of GaN substrates (1 cm × 1 cm dimension size) are cleaned first using GaN cleaning steps as mentioned previously. Si substrate is used for reference to estimate the thickness of deposited layer using ellipsometry measurement and it should be placed as well on the substrate holder). Once the samples are placed correctly, the shutter is checked to make sure it is working correctly. The rotation speed of the sample is checked as well (insert manually the rotation speed of 15 on the 'Process' control system menu which allow it to run for 10 seconds)

3) Pumping the chamber
   - The chamber lid is closed before starting to pump the chamber. The vent gas is turned off, while the service gas is kept turned on. Then, the 'Pump' on main control panel is pressed and wait until the pressure inside the chamber drops below 3×10^{-6} mbar. The service gas is turned off after the door pressure indicator has turned green on the display.
4) Sputtering

- The process gas either Ar as mass flow controller (MFC 1) or O_2 (MFC 2) and the service gas are turned on. For deposition, always run the system using the 'Process' control (the source presets have been defined first).
- The following source presets setting can be defined include:
    i. Max. power supply unit (PSU) (%) - maximum PSU output that can be applied.
    ii. Ramp rate (%/s) - the % increase in power per second. Not used for manual control and only used in process control.
    iii. Soak time (s) - the time, for which the source is held under strike conditions before being ramped to deposition conditions. Only used in process control.
    iv. Strike PSU (%) - The output level of the PSU that should be used for first striking/stabilising the plasma. Only used in process control.
    v. Strike MFC (sccm) - flow rate that should be used when striking/stabilising the plasma. Only used in process control.
- There are 2 main operations; Manual control and Process control. In manual control, the user operates all hardware directly. But process control is used when a specific recipe has been defined and calibrated. The following options need to be defined in both operations.
    i) MFC (sccm rate) – defines the flow rate for the MFC line used into the chamber to ensure the plasma can be struck. The Ar (MFC 1) line is set to 10 sccm.

ii) RF source (target number) – the target has been selected (target 1 or 2). This is based on the position of the target that has been inserted (1=left, 2=right).

iii) RF PSU % – defines the power applied directly to the target as a % of the maximum power where the maximum power of the system is 150 W.

- The process recipe used for each oxides as following:

  i) Ta_2O_5: RF PSU = 40 %, MFC1 = 0.5 sccm, Source preset (Max. PSU = 50 %, Soak time = 50 s, Strike PSU = 40 %, Strike MFC1 = 10 sccm)

  ii) ZrO_2: RF PSU = 40 %, MFC1 = 0.5 sccm, Source preset (Max. PSU = 50 %, Soak time = 50 s, Strike PSU = 40 %, Strike MFC1 = 10 sccm)

  iii) Al_2O_3: RF PSU = 30 %, MFC1 = 0.5 sccm, Source preset (Max. PSU = 50 %, Soak time = 50 s, Strike PSU = 30 %, Strike MFC1 = 10 sccm)

  iv) MgO: RF PSU = 40 %, MFC1 = 0.5 sccm, Source preset (Max. PSU = 50 %, Soak time = 50 s, Strike PSU = 40 %, Strike MFC1 = 10 sccm)

- The thickness and rate of sputtered layer can be monitored using Q-pod system.

4.3.1.2 *GaN samples*

The ZrO_2 and Al_2O_3 films were deposited on 5 µm un-doped GaN on sapphire, while MgO films were deposited on 2 µm un-doped GaN on silicon, using pulsed

reactive sputtering (ZrO_2) and RF magnetron sputtering (Al_2O_3, MgO). Prior to oxide deposition, the GaN surface was cleaned using the following sequence: acetone for 10 minutes in an ultrasonic bath, 10 minutes in methanol, 20 minutes in 37% HCl solution and finally a deionised water rinse. Our previous work shows that the HCl treatment is effective in removing oxygen and carbon contaminant on the GaN surface [270] and the organic solvents serve to degrease the surface. For ZrO_2 deposition, the plasma power used was 25 W with oxygen and argon flow rates of 0.6 sccm and 1.4 sccm, respectively. The chamber pressure was typically $\sim 1\times 10^{-3}$ mbar at room temperature. The sputtering was done with a deposition rate of 0.5 Å/s to deposit the interfacial (3 nm) and bulk (20 nm) ZrO_2/GaN samples respectively. The sputtering power used for Al_2O_3 deposition was 45 W with the rate of 0.06 Å/s to deposit the interfacial (3 nm) and bulk (20 nm) Al_2O_3/GaN samples. For MgO deposition, the sputtering power was 150 W with a chamber pressure of 5 mTorr at room temperature and a rate of 0.04 Å/s to deposit the interfacial (3 nm) and bulk (20 nm) samples. The average surface roughness of the ZrO_2, Al_2O_3 and MgO bulk layers was found to be 0.33 nm, 0.52 nm and 0.58 nm with root-mean-square (RMS) of 0.42 nm, 0.62 nm and 0.78 nm (± 0.1 nm) respectively measured by Veeco di Innova atomic force microscope, operated in contact mode as shown in Figure 4.11. It can be seen that the sputtered ZrO_2 layer on GaN is quite uniform with smooth surface as compared to those Al_2O_3 and MgO layers as its roughness is lower. However, since these AFM results have not been critically evaluated in terms of the efficiency of GaN cleaning and its performance with different sputtered oxides. Therefore, these results cannot be necessarily used for comparison with band alignment results.

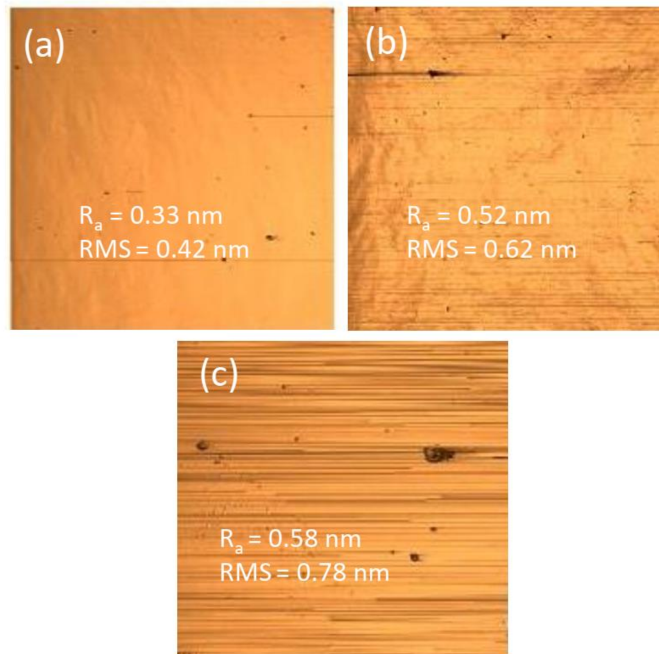

Figure 4.11: AFM images of bulk samples (a) ZrO_2 with a scanned area of 100 μm × 100 μm, (b) Al_2O_3 with a scanned area of 90 μm × 90 μm and (c) MgO with a scanned area of 100 μm × 100 μm.

To account for the effect of differential charging [64], [206], [244], different batches of interfacial samples were prepared using RF magnetron sputtering. In the case of the oxide/semiconductor heterojunction, the positive charge generated during X-ray bombardment accumulate in the dielectrics forming the heterojunction and induce a strong modification of the kinetic energy of the emitted photoelectron. According to the model in Ref. [268], photoelectrons emitted from the semiconductor are easily compensated by electrons provided through the grounded sample holder. Those originated from the oxide cannot be fully compensated either by electrons tunnelling from the substrate or stray electrons in the analysis chamber. This phenomenon results in a bending of the VB and CL signals in the oxide and affects the accurate evaluation of the VBO. A thickness dependent analysis is needed for the correction of the binding energy of the metallic CL for the interfacial sample to obtain

the accurate value of VBO. The plasma power used for ZrO_2 and MgO films deposition was 60 W, while for Al_2O_3 film it was 45 W with the chamber pressure of 1×10^{-3} mbar at room temperature. The sputtering deposition rate was 0.07 Å/s for the interfacial ZrO_2 and Al_2O_3 samples with thicknesses of 1.9 nm, 3.8 nm and 4.0 nm for the former and 2.5 nm, 4.4 nm and 6.9 nm for the latter oxide measured by VASE using a Cauchy model [270]. For MgO, the deposition rate of 0.16 Å/s was used to fabricate interfacial samples with thicknesses of 3.4 nm, 5.8 nm and 6.8 nm as measured by VASE. Note that the two sets of samples were sputtered simultaneously in the chamber, one on GaN and a reference one on Si substrate, where the latter was used for VASE measurements to confirm the thickness of deposited films. Room temperature VASE measurements were performed using a J.A. Woollam M2000 ellipsometer with a wavelength range of 241.1–1686.7 nm, which corresponds to an energy range of 0.7–5.2 eV. The measurements were performed at three incident angles of 60°, 65° and 70°, in order to increase the accuracy of the measurements for extracting thickness of the oxide films. The experimental data extracted in the form of two angles (ψ, Δ) vs photon energy (E) were analysed using Complete EASE software program by developing a theoretical Cauchy model to match the experimental results. The mean squared error (MSE) between the experimental and theoretical (fitted) (ψ, Δ) vs E curves was in all cases below 5, consistent with a good quality fit of the data.

The band alignments of the oxide/GaN interfaces were measured by XPS using non-monochromatic XPS system with Al Kα X-ray source (hν = 1486.6 eV) and a PSP Vacuum Technology electron energy analyser. The spectrometer was calibrated using the Ag $3d_{5/2}$ photoelectron line and the Fermi edge from a clean silver foil. The overall resolution of the spectrometer was 0.8 eV, and peak positions were determined with a precision of ± 0.05 eV. This XPS instrument was operated at power of 144 W with 12

mA emission current and 12 kV accelerating voltage. The probe area during the XPS measurements was 1 mm^2. Survey and detailed scans was carried out at a pass energy of 100 eV and 50 eV, respectively. During all XPS measurements, the X-ray beam exposure was across the whole sample [243], [244] to diminish the effect of differential charging when evaluating the VBO. The electron binding energies were corrected using the C 1s peak at 284.6 eV from adventitious surface carbon present in the sputtered films. A Shirley-type background was used for the fitting of all spectra [202]. The measured CL line-shapes were fitted using a Voigt function to determine the BE position and FWHM of the peaks. The error bar (± 0.2 eV) in evaluating VBO is due to valence band maximum determination through the linear interpolation method.

4.3.2 Band gap estimation of oxides using XPS O 1s energy loss spectra

The band gap energy values for the dielectric materials were determined using the asymmetry of the O 1s XPS peak, that is the difference between the onsets of energy loss and the O 1s CL [271]. The extracted band gap of ZrO_2 was found to be 5.09 ± 0.2 eV, as shown in Figure 4.12 (a). The latter compares with previously reported values of 5.25 eV from spectroscopic ellipsometry (SE) [272], 5.5 eV from UPS combined with inverse photoemission spectroscopy (IPS) [273], and 5.6 eV from XPS [274]. Moreover, from Figures 4.15 (b) and (c) the band gaps of Al_2O_3 and MgO were also extracted using the same method and were found to be 6.48 ± 0.2 eV and 7.36 ± 0.2 eV respectively. These values are comparable with previously reported values of 6.4 eV [83], [275] from SE; 6.6 eV [265], 6.7 eV [274], 6.8 eV [276], [277] from XPS for Al_2O_3 and 7.8 eV [147], [148], [250] from XPS for MgO. The XPS analysis of the core levels (core level position is slightly less than the fully stoichiometric oxide's core levels) indicates that the sputter deposited oxide samples

(ZrO_2, Al_2O_3 and MgO) are not fully stoichiometric. Quantification from survey spectrum also showed nonstoichiometric oxide growth. Also, XPS is a surface sensitive technique, and the measurements reflect the topmost few nanometers of the material, which could have defects and contamination. The reported band gaps may therefore differ from the bulk band gaps reported in the literature.

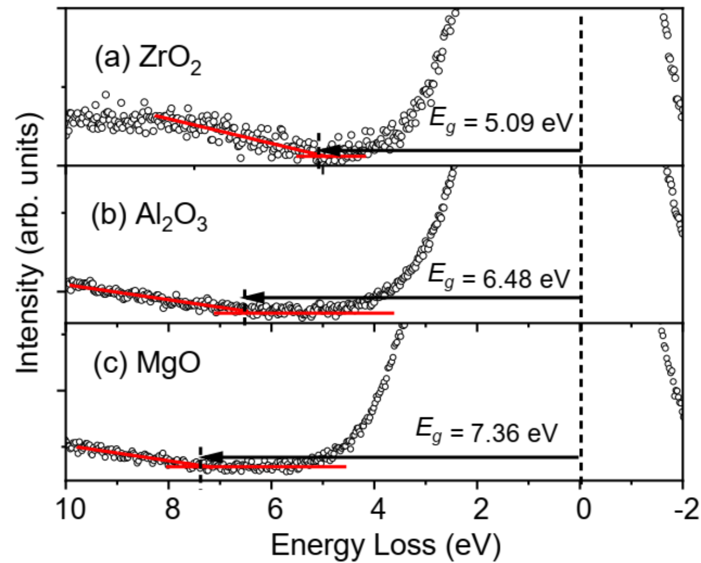

Figure 4.12: The XPS O 1s energy loss spectra for (a) ZrO_2, (b) Al_2O_3 and (c) MgO depicting extraction of the band gap.

4.3.3 Band offsets of ZrO_2, Al_2O_3 and MgO on GaN

The VBO is extracted using Kraut's method [231] by Equations (4.1) and (4.2), whereas the CBO using Equation (4.3). The band gap of the GaN substrate, that has also been used for sputtered oxides (ZrO_2, Al_2O_3) in this study, is 3.34 ± 0.15 eV obtained from VASE measurements by linear extrapolation of the leading edge of the imaginary part of the dielectric function, ε_2 vs photon energy spectra to the baseline as shown in Figure 4.7(a) [270]. This band gap value is used in this study, being in close agreement to the previously reported values of 3.4 eV [147], [148], [246], [248], [249] and 3.44 eV [250].

Figure 4.13 depicts measured XPS spectra for the ZrO_2/GaN system, including the Ga 3d CL and VB spectrum for the GaN substrate (Figures 4.13 (a)-(b)), the Ga 3d and Zr 3d CLs for the interfacial ZrO_2/GaN sample (Figures 4.13 (c)-(d)), and the Zr 3d CL and VB spectrum for bulk ZrO_2 (Figures 4.13 (e)-(f)). In the case of the Al_2O_3/GaN and MgO/GaN systems, Al 2p and Mg 2p CLs were measured in combination with Ga 3d from the GaN substrate for estimation of VBO using Kraut's method; the referring XPS spectra for interfacial and bulk oxide samples are shown in Figures 4.14 (a)-(b) and (e) for Al_2O_3/GaN, and in Figures 4.14 (c)-(d) and (f) for MgO/GaN.

For GaN sample shown in Figure 4.13 (a), the Ga 3d CL was fitted using two sets of doublet Voigt functions corresponding to Ga-N and Ga-O bonds with spin orbit splitting of 0.45 eV and an area ratio of 0.67 for each doublet [278]. The lower BE side of the main peak at 16.8 eV is attributed to the N 2s component. The most intense peak corresponds to Ga-N $3d_{5/2}$ component at 19.88 eV (Figure 4.13 (a)) and is chosen as the reference CL for 5 μm GaN on sapphire sample with its respective VBM value of 2.53 ± 0.2 eV (Figure 4.13 (b)). This gives the $[E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)]$ value of 17.35 eV. This value is in close agreement with the value of 17.34 eV [153] reported for undoped GaN. Partida-Manzanera *et al.* [157] found a $[E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)]$ value of 17.2 eV, slightly smaller as compared to Ye *et al.* [153] and our work, which they attributed to the presence of growth-induced in-plane stress in the nitride epilayer. On the other hand, the $[E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)]$ value of 17.56 eV was obtained for the 2 μm GaN on silicon substrate sample used for sputtering MgO (not shown). This value is in close agreement with experimentally measured values of 17.6 eV [147], [264], 17.69 eV [250], 17.7 eV [279] and 17.72 eV [270]. It is worth mentioning that the theoretical value obtained from electronic-state studies of

bulk GaN has been found to be in the range of 17.7–17.8 eV [232], [251]. It can be noted that the $[E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)]$ values differ in the two GaN samples used in this study. While the values are within the range reported in the literature, the discrepancy could be attributed to differences in the surface conditions of two samples. Note that the VBM for the two GaN samples is found to be 2.5 ± 0.2 eV. Since the BEs in XPS are measured with respect to the Fermi level of the spectrometer that corresponds to the position of the Fermi level within the band gap of the semiconductor, the extrapolated value of the VBM indicates that the Fermi level is closer to the CB edge. It has been shown that undoped GaN can exhibit unintentional *n*-type conductivity [280]. Furthermore, this could also indicate downward BB and an accumulated GaN surface for both substrate samples used in this work. In a recent study, a downward BB has been reported for GaN samples degreased for 5 minutes in acetone, followed by immersion in isopropyl alcohol and a rinse in flowing DI water, without using HF [281].

In our work, GaN samples were also cleaned without HF. The observation of an accumulated GaN surface has been explained by a significant positive charge density residing within the native oxide [281], [282]. It has been suggested that the positive charges on GaN surface compensate the polarization-induced negative surface charge and form an electron accumulation layer. With an accumulated surface, the Fermi level is situated close to the GaN conduction band edge and thus the positive charges cannot be attributed to donor-like gap states [282]. A possible source for the positive charge may be (i) interfacial fixed charge with energy states between the conduction band minima of the native oxide and GaN [282]; or (ii) a possible polarity inversion of the GaN surface, that is a change in the spontaneous polarization charge from negative to positive due to the formation of Ga-O bonds. It can be seen from

Figures 4.13 (a), 4.13 (c), 4.14 (a) and 4.14 (c) that there are Ga-O bonds on the higher BE side of Ga 3d CL peak, which could underpin the existence of a thin GaO_x layer, and a presence of positive charges on the GaN surface.

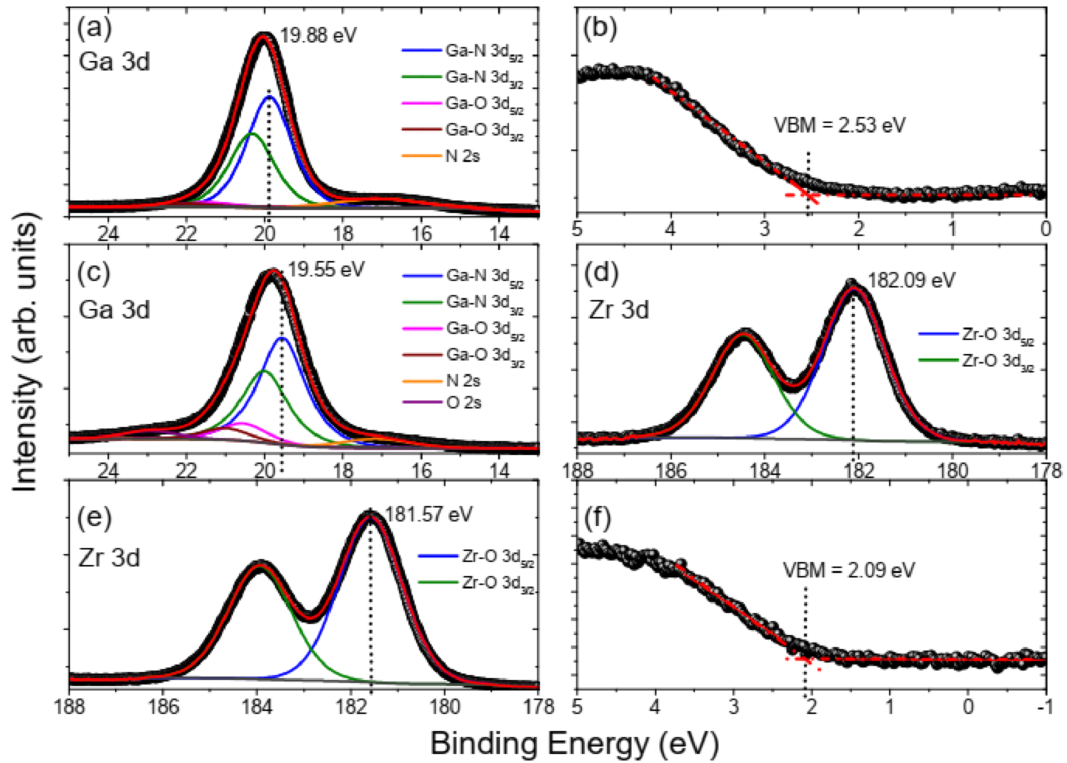

Figure 4.13: The XPS spectra of (a) Ga 3d CL and (b) valence band spectrum for 5 µm GaN on sapphire; (c) Ga 3d and (d) Zr 3d CLs for interfacial ZrO_2/GaN sample; (e) the Zr 3d CL and (f) valence band spectrum showing VBM extraction for bulk ZrO_2/GaN sample.

Figures 4.13 (c) and (d) show XPS spectra for the interfacial ZrO_2/GaN sample, where the Ga 3d CL was fitted using two doublet Voigt function related to Ga-N and Ga-O bonds, N 2s, and O 2s components, whereas the Zr 3d CL was fitted with a single doublet Voigt function related to Zr-O bond. The peak positions at BEs of 19.55 eV (Figure 4.13 (c)) and 182.09 eV (Figure 4.13 (d)) corresponding to Ga-N $3d_{5/2}$ and Zr-O $3d_{5/2}$ respectively were selected as reference CLs. For the bulk ZrO_2 sample, the peak position of Zr-O $3d_{5/2}$ at 181.57 eV (Figure 4.13 (e)) is chosen as the reference CL with its respective VBM value of 2.09 eV (Figure 4.13 (e)), giving

$[E_{CL}^{oxide}(bulk) - E_{VBM}^{oxide}(bulk)]$ = 179.48 eV. In a similar way, Ga 3d and Al 2p XPS CLs were designated and fitted in Figures 4.14 (a)-(b) for Al_2O_3/GaN, as well as Ga 3d and Mg 2p for MgO/GaN as shown in Figures 4.14 (c)-(d). The high resolution spectra of the VB region for bulk Al_2O_3 and MgO are shown in the insets of Figures 4.14 (e) and (f) respectively, with extrapolated values of the VBM of 2.80 eV for Al_2O_3 and 4.38 eV for MgO. The resultant $[E_{CL}^{oxide}(bulk) - E_{VBM}^{oxide}(bulk)]$ values are 70.98 eV and 46.45 eV for Al_2O_3 and MgO, respectively. Table 4.1 shows the XPS CL and VBM data for bulk and interfacial samples (ZrO_2/GaN, Al_2O_3/GaN, and MgO/GaN).

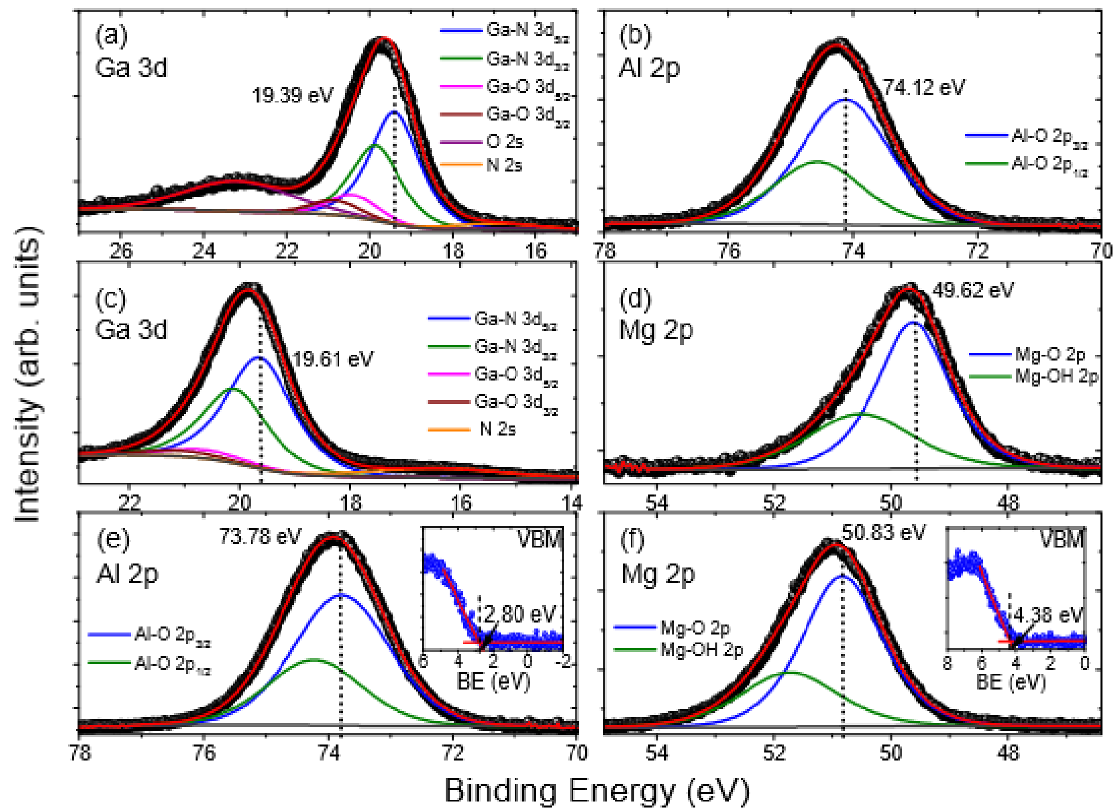

Figure 4.14: The XPS spectra for (a) Ga 3d, (b) Al 2p CLs for interfacial Al_2O_3/GaN; (c) Ga 3d and (d) Mg 2p CLs for interfacial MgO/GaN; (e) Al 2p and Mg 2p CLs for bulk Al_2O_3 and MgO films. The insets in both (e) and (f) refer to VB spectra and extraction of VBM for both bulk oxide films.

Table 4.1: XPS CL and VBM data for the bulk and interfacial samples (ZrO_2/GaN, Al_2O_3/GaN, and MgO/GaN)

		Ga $3d_{5/2}$		Zr $3d_{5/2}$ or Al $2p_{3/2}$ or Mg 2p		O 1s	VBM
Sample	Thickness (nm)	BE (eV)	FWHM (eV)	BE (eV)	FWHM (eV)	BE (eV)	(eV)
ZrO_2/GaN	3.7	19.55	1.40	182.09	1.56	530.10	–
	1.9	19.66	1.20	182.08	1.38	530.18	–
	3.8	19.55	1.20	182.01	1.36	530.06	–
	4.0	19.25	1.20	181.50	1.29	529.73	–
	26.8	–	–	181.57	1.59	529.65	2.09
Al_2O_3/GaN	3.5	19.39	1.40	74.12	1.70	531.18	–
	2.5	19.88	1.30	74.56	1.70	531.40	–
	4.4	19.69	1.30	74.53	1.65	531.38	–
	6.9	19.70	1.22	74.64	1.67	531.45	–
	21.8	–	–	73.78	1.76	530.80	2.80
MgO/GaN	3.5	20.73	1.40	50.72	1.45	532.58	–
	3.4	19.62	1.20	49.74	1.44	531.50	–
	5.8	19.61	1.23	49.56	1.45	531.42	–
	6.8	19.63	1.20	49.79	1.49	531.46	–
	20.2	–	–	50.83	1.50	532.50	4.38

4.3.3.1 *The effect of differential charging*

The effect of differential charging can be seen in Figures 4.15 (a)-(c) and Table 4.2. The constant value of the BE of Zr 3d CL of 182.1 ± 0.1 eV in ZrO_2/GaN heterostructures with all thicknesses in Figure 4.15 (a) can be interpreted as evidence that no charge accumulation occurs in the oxide films during the X-ray irradiation. The

ΔE_{CL} values from thin ZrO_2/GaN samples are listed in Table 4.2, and inserting them into Equation (4.1), the VBO is calculated to vary between 0.29 eV to 0.41 eV, giving an average value of 0.35 ± 0.1 eV. In the Al_2O_3/GaN (Figure 4.15 (b)) and MgO/GaN (Figure 4.15 (c)) heterojunctions, the Al 2p and Mg 2p CLs exhibit a very small increasing shift towards higher BEs when increasing Al_2O_3 and MgO film thicknesses, thus providing clear fingerprints of a small charging phenomenon.

In all cases, a constant energy difference between the metallic (M) Zr 3d, Al 2p and Mg 2p CL and O 1s was observed (± 0.2 eV) regardless of the thickness of the oxide films (see Table 4.2). This suggests that no chemical modification of the oxide matrix occurred when increasing the thickness of the deposited oxide. From the linear fit of the experimental data in Figures 4.15 (b) and (c), the BEs of the Al 2p and Mg 2p CLs in the interfacial Al_2O_3/GaN and MgO/GaN are extrapolated to zero oxide thickness, and found to be 74.48 eV and 49.70 eV, respectively. The referring ΔE_{CL} values for Al_2O_3/GaN and MgO/GaN are listed in Table 4.2, and by inserting them in Equation (4.1), the average VBOs are found to be 1.07 ± 0.1 eV for Al_2O_3/GaN and 1.19 ± 0.1 eV for MgO/GaN.

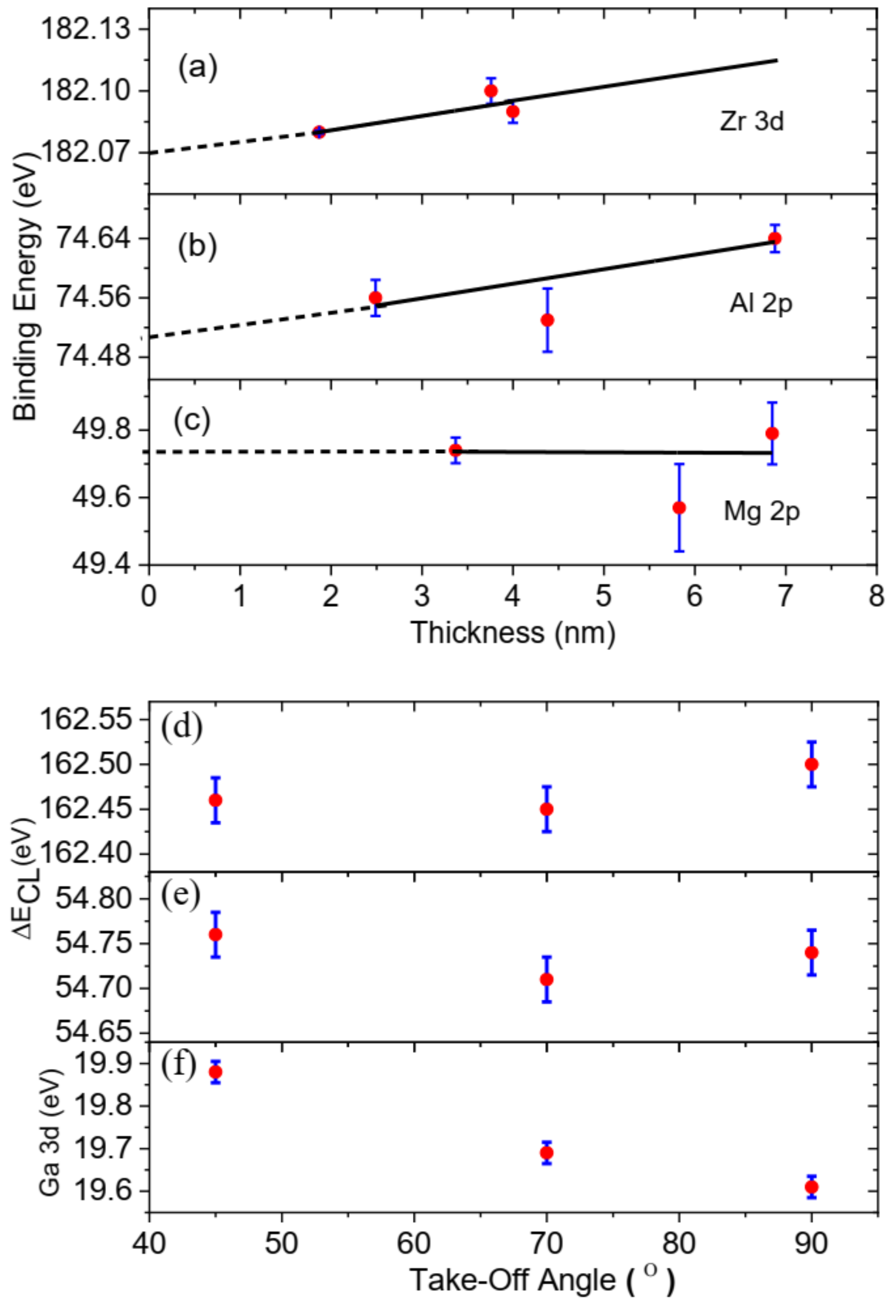

Figure 4.15: The binding energy of (a) Zr 3d, (b) Al 2p, (c) Mg 2p measured for a range of thin (up to 7 nm) oxide/GaN samples. A small differential charging effect can be seen in (b) and (c) for Al_2O_3 and MgO respectively. The CL difference, ΔE_{CL} (eV) between (d) Zr 3d and Ga 3d and (e) Al 2p and Ga 3d for thin (3 nm nominal) ZrO_2/GaN and Al_2O_3/GaN samples as a function of XPS take-off angle. (f) The variation of Ga 3d CL for thin (3 nm nominal) MgO/GaN sample vs XPS take-off angle.

Table 4.2: A summary of VBO results obtained from a set of interfacial oxide/GaN samples with thickness of the oxides measured by VASE; ΔE_{CL} is the difference in binding energies between metallic (M) and Ga 3d XPS CLs, and ΔM-O 1s is the BE difference between the metallic and O 1s XPS CLs. M refers to Zr 3d, Al 2p and Mg 2p for respective ZrO_2, Al_2O_3 and MgO on GaN. The average VBO value across the three films is given on the right-hand side of VBO column.

	Thickness (nm)	ΔE_{CL} (eV)	ΔM-O 1s (eV)	VBO (eV)	
ZrO_2/GaN	1.9	162.42	348.10	0.29	
	3.8	162.46	348.05	0.33	0.35 ± 0.1
	4.0	162.54	348.01	0.41	
Al_2O_3/GaN	2.5	54.60	456.84	0.97	
	4.4	54.79	456.85	1.16	1.07 ± 0.1
	6.9	54.78	456.81	1.15	
MgO/GaN	3.4	30.08	481.76	1.19	
	5.8	30.09	481.86	1.20	1.19 ± 0.1
	6.8	30.07	481.67	1.18	

4.3.3.2 *The effect of band bending*

Furthermore, we looked into the effect of band bending at the oxide/GaN interface by monitoring the difference in BEs of Ga 3d and metallic CLs by AR-XPS as shown in Figures 4.15 (d)-(e). It can be seen that ΔE_{CL} is within 0.1 eV for both ZrO_2/GaN and Al_2O_3/GaN, indicating negligible BB for TOAs up to 45°. Using the Equation (4.1) and the values of ΔE_{CL} from Figures 4.15 (d)-(e), the VBO was found to be 0.37 eV, 0.32 eV to 0.33 eV for ZrO_2/GaN; and 1.11 eV, 1.08 eV and 1.13 eV for Al_2O_3/GaN when TOA varies from 90°, 70° to 45° respectively. Since, the Ga 3d CLs for all three interfacial ZrO_2/GaN (Figure 4.13 (c)), Al_2O_3/GaN (Figure 4.14 (a)) and MgO/GaN (Figure 4.14 (c)) shift towards lower binding energies in comparison to the GaN, this means that there is an upward bend bending after oxide deposition; since the GaN surface is accumulated (see Figure 4.16 (a)), this results in less downward BB at the oxide/GaN interface. The latter can be underpinned by smaller

values of the VB edge from the Fermi level at the interface, that is deduced from the measured Ga 3d CL binding energy and measured $[E_{CL}^{GaN}(bulk) - E_{VBM}^{GaN}(bulk)]$ i.e. for ZrO_2 this is 19.55 eV – 17.35 eV = 2.2 eV; for Al_2O_3 (Figure 4.14 (a)) 19.39 eV - 17.35 eV = 2.04 eV; for MgO (Figure 4.14 (c)) 19.61 eV – 17.56 eV = 2.05 eV (Figure 4.16 (b)). Note that due to the very small photoionisation cross-section of Mg 2p (0.005), the angle-resolved data could not be recorded; instead only Ga 3d CL is measured by AR-XPS.

In Figure 4.15 (f), the BE of Ga $3d_{5/2}$ CL for MgO/GaN sample is seen to increase from 19.61 eV at 90° TOA to 19.88 eV at 45° TOA. The latter is in agreement with a small downward band bending of up to 0.3 eV for MgO/GaN, as found observing the VB edge position from the Fermi level at the interface. Table 4.3 shows AR-XPS CL data for the interfacial samples: ZrO_2/GaN, Al_2O_3/GaN, and MgO/GaN.

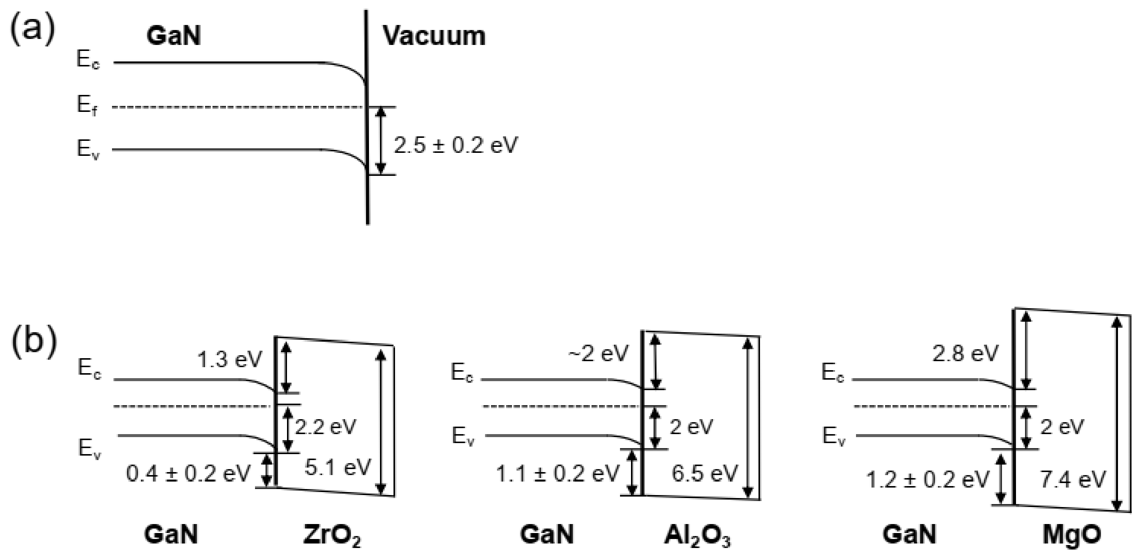

Figure 4.16: The schematics of XPS experimentally derived band alignments: (a) at GaN surface; (b) for ZrO_2/GaN, Al_2O_3/GaN and MgO/GaN fabricated in this work by sputtering. (The diagrams are not to scale.)

Table 4.3: AR-XPS CL data for the interfacial samples: ZrO_2/GaN, Al_2O_3/GaN, and MgO/GaN.

	Ga $3d_{5/2}$		Zr $3d_{5/2}$ or Al $2p_{3/2}$ or Mg 1s		O 1s
Sample	BE (eV)	FWHM (eV)	BE (eV)	FWHM (eV)	BE (eV)
ZrO_2/GaN (90 ^{o})	19.81	1.4	182.31	1.27	530.68
ZrO_2/GaN (70 ^{o})	19.84	1.4	182.29	1.29	530.68
ZrO_2/GaN (45 ^{o})	19.82	1.4	182.28	1.26	530.64
Al_2O_3/GaN (90 ^{o})	19.33	1.4	74.07	1.6	531.16
Al_2O_3/GaN (70 ^{o})	19.52	1.4	74.23	1.6	531.33
Al_2O_3/GaN (45 ^{o})	19.57	1.4	74.33	1.6	531.48
MgO/GaN (90 ^{o})	19.61	1.35	1304.39	2.06	531.56
MgO/GaN (70 ^{o})	19.69	1.3	1304.33	2.03	531.67
MgO/GaN (45 ^{o})	19.88	1.39	1304.4	2.06	531.78

A summary of all measured XPS CL differences, band gap, VBO and CBO extracted in this work and their comparison with literature values is given in Table 4.4. The calculated VBOs (± 0.2 eV) using Equations (4.1) and (4.2) for ZrO_2, Al_2O_3 and MgO on GaN are found to be 0.4 eV, 1.1 eV and 1.2 eV with corresponding CBOs (± 0.2 eV) calculated from Equation (4.3) of 1.3 eV, 2.0 eV and 2.8 eV respectively. The band offset values based on the charge-corrected ΔE_{CL} are summarized in Table 4.4. The derived band diagrams for the ZrO_2, Al_2O_3 and MgO on GaN are shown in Figure 4.16 (b).

In terms of band gap values, we can infer smaller band gap values of 5.1 eV for ZrO_2 and 7.4 eV for MgO than those reported in the literature measured by XPS as listed in Table 4.4. The smaller band gap values measured in this work could be due to the non-stoichiometric surface of sputtered ZrO_2 and MgO films. For Al_2O_3, our XPS derived band gap value of 6.48 eV is in close agreement with our previously

reported value of 6.43 eV by vacuum ultra violet (VUV)-VASE [64] on MBE-deposited Al_2O_3, as well as the most recent theoretically predicted value of 6.36 eV [283]. A variation of reported band gap values for Al_2O_3 can be seen in Table II, from 6.4 eV to 6.9 eV.

The VBO results indicate a smaller value of 0.4 ± 0.2 eV for sputtered ZrO_2 on GaN than the previously reported value of 1 eV for ALD deposited ZrO_2 on GaN [153], while the CBO of 1.3 ± 0.2 eV is within the measurement error to the values of 1.2 eV [153] and the theoretically predicted value of 1.1 eV [150]. The difference in CL values in our work is comparable with Ye *et al*. [153] (see Table 4.4), but the discrepancy is mainly due to a potential gradient in the ZrO_2 layer and a strong upward BB at the GaN surface. The value of VBO of 1.1 eV ± 0.2 eV for Al_2O_3/GaN from our work is in agreement with the experimentally derived values of 0.9 eV [264] and 1.0 eV [265] for conventional ALD Al_2O_3 on HF-treated GaN. Furthermore, it shows excellent agreement with the most recent published theoretical VBO and CBO values of 1.17 eV and 1.79 eV respectively [283]. It is worth mentioning that earlier theoretical work by the same group [150] predicted much higher VBO values for both ZrO_2/GaN and Al_2O_3/GaN. The discrepancy of up to 1 eV of VBO compared to the work of Yang *et al*. [123], [284] is due to a BE difference in the Al 2p CL with respect to Ga 3d CL and between Ga 3d CL and VBM. These discrepancies could be the result of different cleaning and deposition processes, namely PE-ALD deposited Al_2O_3 on HCl and H_2/N_2 plasma-treated GaN [123] or NH_4OH and NH_3 plasma-treated GaN [284]. Both these processes could result in a strong upward band bending at the oxide/GaN interface and higher VBOs of 1.8 eV [123] and 2.0 eV [284] (Table 4.4). Furthermore, Toyoda *et al*. [279] have measured a VBO of 1.5 eV for chemical vapour deposited Al_2O_3/n-GaN using VB spectra of Al_2O_3 films on GaN normalised by that of a bare

GaN layer. In the case of MgO/GaN, our measured VBO of 1.2 ± 0.2 eV is in agreement with the experimentally derived values of 1.2 eV [34] and 1.06 eV [250] for MgO grown by MBE and RF plasma-assisted MBE on untreated GaN respectively. Note that a larger VBO of 1.65 eV has been reported using Kraut's method; however no charge-correction in the oxide film nor BB at the GaN surface have been taken into account [148]. The CBO of MgO/GaN of 2.8 ± 0.2 eV is within measurement error with the experimental value of 2.75 eV [148] and theoretically predicted value of 2.6 eV [150] as shown in Table 4.4.

Table 4.4: The measured values of difference in CLs, E_g, corrected VBO and CBO from this work (± 0.2 eV) compared to literature values.

Material System	$E_{CL}^{GaN} - E_{VBM}^{GaN}$ (eV)	$E_{CL}^{oxide} - E_{VBM}^{oxide}$ (eV)	$\Delta \boldsymbol{E_{CL}}$ (eV)	E_g (eV)	VBO (eV)	CBO (eV)
ZrO_2/GaN	17.35 17.34 [153]	179.48 179.43 [153]	162.54 162.68 [153]	5.09 5.25 [272] 5.5 [273] 5.6 [274]	0.4 1 [153] 1.6 [150]	1.3 1.2 [153] 1.1 [150]
Al_2O_3/GaN	17.35 17.8 [123], [284] 17.6 [147], [264] 17.7 [279]	70.98 70.4 [123] 71.8 [264] 70.6 [284]	54.74 54.4 [123] 55.1 [264] 54.9 [284]	6.48 6.4 [64], [275], [283] 6.6 [265] 6.7 [274] 6.77 [276] 6.88 [277] 7.6 [279]	1.1 1.8 [123] 0.9 [264] 1.0 [265] 2.1 [150] 1.5 [279] 2.0 [284] 1.17 [283]	2.2 1.3 [123], [284] 2.2 [265] 3.4 [150] 2.7 [279] 1.79 [283]
MgO/GaN	17.56 17.6 [147], [264] 17.69 [250] 17.72 [270]	46.45 46.79 [147] 46.94 [250]	30.09 30.32 [147] 30.31 [250]	7.36 7.8 [147], [148], [250]	1.2 1.2 [147] 1.65 [148] 1.06 [250]	2.8 3.2 [147] 2.75 [148] 2.6 [150] 3.3 [250]

[123], [147], [277], [284], [148], [153], [250], [264], [265], [270], [274], [276] XPS
[279] photoemission spectroscopy and XAS
[273] UPS and IPS
[272], [275] SE
[64], [250] photoluminescence
[150], [283] theoretical CNL method

4.4 Conclusion

In this chapter, several high-k dielectrics films (Ta_2O_5, ZrO_2, Al_2O_3 and MgO) were processed by sputtering on GaN, with the aim of determining their suitability for MIS-HEMT applications in terms of their band alignments on GaN. The GaN surface has been cleaned using different treatments; HCl treatment has been compared to NH_4OH and $(NH_4)_2S$ cleaning procedures and has shown to exhibit the lowest oxygen contaminant level on the GaN surface. Variable angle spectroscopic ellipsometry was performed to measure the thickness, optical constants and band gap of GaN and Ta_2O_5/GaN samples. The VBOs of sputtered Ta_2O_5, ZrO_2, Al_2O_3 and MgO on GaN have been measured experimentally using XPS and Kraut's method. The effect of differential charging as well as band bending at oxide/semiconductor interface has been considered and accounted for all samples. The former has been found negligible for Ta_2O_5/GaN and ZrO_2/GaN, while present in case of Al_2O_3/GaN and MgO/GaN and corrected using thickness dependent XPS CL method. The thickness dependent analysis has been used for the correction of the binding energy of the metallic CL for the interfacial samples to obtain the accurate value of VBO. Furthermore, band bending has been evaluated from angle resolved XPS data and found to be small upward (0.05 eV) for Ta_2O_5/GaN, while downward (up to 0.3 eV) for ZrO_2, Al_2O_3 and MgO on GaN. The apparent downward band bending suggests an accumulated GaN surface for these samples and could be explained by a significant presence of positive charge density residing within the native oxide on the GaN surface. The native oxide Ga-O bonds have been found from Ga 3d CL spectra for referring samples. The corrected VBO values (± 0.2-0.25 eV) for Ta_2O_5, ZrO_2, Al_2O_3 and MgO on GaN using Kraut's method were found to be 0.7 eV, 0.4 eV, 1.1 eV and 1.2 eV with corresponding CBOs of 0.4 eV, 1.3 eV, 2.2 eV and 2.8 eV respectively. The band gaps of GaN (3.34

eV) and Ta_2O_5 (4.4 eV) were extracted using VASE, whereas the band gaps of ZrO_2 (5.1 eV), Al_2O_3 (6.5 eV) and MgO (7.4 eV) were determined from XPS O 1s loss spectroscopy. The band offset results from this study have been critically compared with the literature and indicate intrinsic limitations of using XPS and Kraut's method in evaluating valence band offset in addition to discrepancies induced by various surface cleaning treatments of GaN and different deposition methods used for fabricating oxide materials. These results are consistent with the theoretical and experimental results from the literature. The sputtering technique used in this work offers several advantages of low temperature processing, low-cost and the availability of a wider range of materials compared to other techniques such as ALD and MBE. Moreover, no band alignment study for sputtered ZrO_2, Al_2O_3 and MgO on GaN has been previously reported. Therefore, the presented band offset measurements have importance for developing and designing future GaN-based MIS-HEMTs.

CHAPTER 5

GaN-Based Devices

5.1 Introduction

Achieving high power conversion efficiency requires low-loss power semiconductor switches. Silicon power semiconductor devices have several important limitations including high losses due to its relatively low band gap and low critical electric field, low switching frequency and poor high-temperature performance. As a result, new opportunities for higher efficiency have emerged with the development of wide band gap (WBG) power semiconductor devices, driven by the fundamental differences in material properties of Si and semiconductors such as silicon carbide (SiC) and gallium nitride (GaN). The advantages of the low ON-resistance, high critical electrical field, narrow width of the drift region allow GaN-based devices to outperform Si-based for power electronics applications.

Aluminium gallium nitride (AlGaN)-GaN high electron mobility transistors (HEMTs) are emerging as promising contenders for high-temperature, high-power (power electronics) and radio-frequency (RF) electronics due to their unique capabilities of achieving higher electron mobility, higher breakdown voltage, higher operating temperatures and higher cut-off frequencies compared to silicon (Si). Conventional GaN HEMTs with an AlGaN barrier are of depletion-mode (D-mode) or normally-on which require a large negative polarity power supply to turn it off. D-mode is the most reported type of AlGaN/GaN HEMTs due to the nature of two-dimensional electron gas (2DEG) at the AlGaN/GaN hetero-interface. On the other hand, enhancement-mode (E-mode) or normally-off AlGaN/GaN HEMTs are attracting increasing interest

in recent years because no negative gate voltage is necessary to turn off the devices, providing such positive threshold voltage (V_T) along with high drain current density (I_{Dmax}) and improved breakdown voltage (V_{BD}). Unlike conventional device structures which use approximately 20 nm thick AlGaN barrier layers, there is no inherent 2DEG channel at the AlGaN/GaN interface in this structure as the AlGaN barrier thickness is below that required for 2DEG formation (4 nm). This leads to the advantage of simple circuit design and low stand-by power dissipation. For power electronics applications, power switches which incorporate E-mode devices provide the highly desirable essential fail-safe operation with high current/voltage capability and minimum cooling. Figure 5.1 shows the structure of D-mode and E-mode HEMTs. The E-mode HEMTs (recessed gate, implanted gate and p-GaN gate) will only be turned on when a positive voltage is applied to the gate where 2DEG gas will be restored underneath. However, Schottky AlGaN/GaN HEMTs suffer from large gate leakage currents as well as current collapse due to the Schottky-gate contact [285]. The leakage current in Schottky gates degrades the reliability and the performance of AlGaN/GaN HEMTs including power efficiency and noise performances. The electrical degradation mechanism for AlGaN/GaN HEMTs is associated with the strong piezoelectric nature of GaN and AlGaN. Basically, under high voltage conditions, the high electric field that is produced introduces strong tensile stress in the AlGaN barrier layer that peaks in regions which are typically below the gate edge on the drain side. The stress increases stored elastic energy inside the AlGaN, which leads to the formation of crystallographic defects that are electrically active if the elastic energy has reached a limit [286]. Thus, it can provide a path for excess gate leakage current, and result in electron trapping that depletes the sheet charge in the channel resulting in current degradation. The inverse piezoelectric can also cause

increases in resistance and a positive shift in threshold voltage. In order to mitigate this degradation mechanism, one needs to minimize the initial strain in the AlGaN barrier layer, by managing the electric field distribution and especially reducing its peak value under the gate. The AlGaN surface under the drain side corner of the gate is the location where peak stress values are induced.

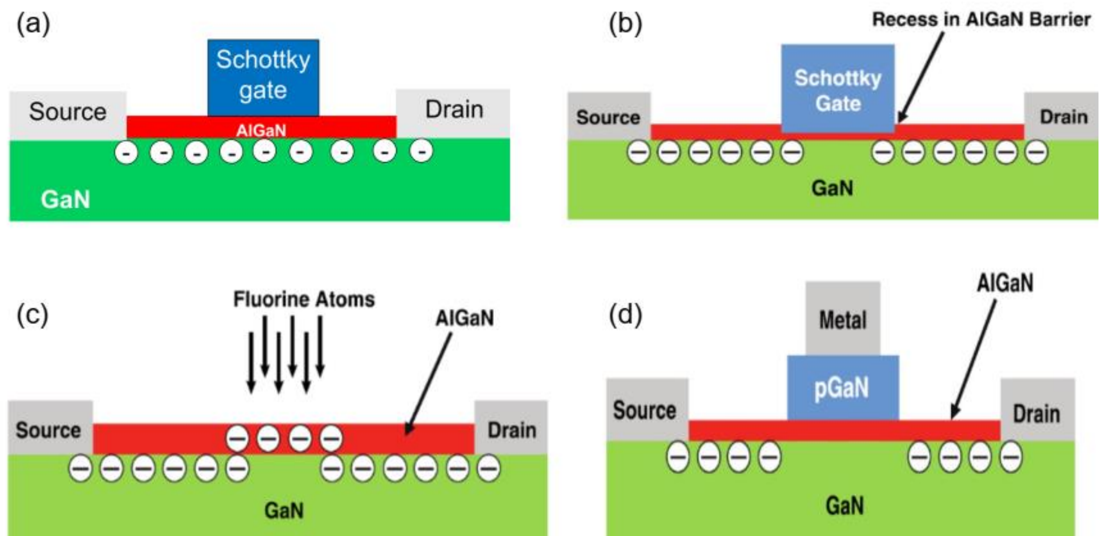

Figure 5.1: The structure of (a) D-mode HEMT – where the channel is formed with 0 V on the gate (normally-on) and there need to be large negative voltage on the gate to turn the transistor off, (b) recessed gate E-mode HEMT – is achieved through thinning the AlGaN barrier layer by etching, (c) implanted gate E-mode HEMT – the 2DEG is removed by implanting fluorine atoms into the AlGaN barrier where the F atoms cause a trapped negative charge effect within that area, and (d) *p*-GaN E-mode HEMT [287].

In the realisation of high electrical performance of D-mode and E-mode devices, gate dielectric can be used to replace Schottky-gate contact to form metal-insulator-semiconductor (MIS) structure to suppress the gate leakage currents. Several high-*k* dielectrics such as Al_2O_3 [288], [289], HfO_2 [290], CeO_2[291] and ZrO_2 [292] are previously investigated and are potentially used as dielectric materials for AlGaN/GaN MIS-HEMTs. Among many high-*k* dielectrics, Al_2O_3 deposited by atomic layer deposition (ALD) is one of the most attractive candidates as it offers additional advantages of a large conduction and valence band offsets (3.4 eV and 2.1

eV, respectively) [150], high dielectric constant (8.6−10), a large band gap (9 eV), high breakdown field (10–30 MV/cm), thermal stability, and chemical stability against GaN [143]. However, it has been reported that a high interface trap density of ~1 $\times 10^{13}$ cm^{-2} eV^{-1} at the Al_2O_3/GaN interface has been reported [293]. This poor interface quality has been associated with the native gallium oxide and dangling bonds on the GaN surface [294], resulting in large leakage current and a threshold voltage instability.

In order to reduce the interface state density, treatments have been suggested as critical procedures to remove native oxide on GaN or to passivate the GaN surface prior to dielectric deposition. The surface cleaning with HCl [295] or HF [296] is commonly used to eliminate the native oxide, but the exposed GaN surface suffers from re-oxidation before dielectrics deposition. Sulfide-based passivation schemes, such as aqueous $(NH_4)_2S$ solution, are capable of protecting the GaN surface from immediate re-oxidation by forming Ga-S bonds [297]. However, metal contamination of the $(NH_4)_2S$ solution and the limited stability of the $(NH_4)_2S$ passivation during the fabrication processes [298] are two limitations, which might be detrimental to devices performance. In contrast, a recent study [299] reported that the surface preparation using sacrificial 1-octadecanethiol (ODT) self-assembled monolayer (SAM) can protect insulator/GaAs interfaces from interfacial oxides. The surface passivated by ODT SAMs can improve the sulfide passivation stability in an air ambient environment [300]. In addition, studies have reported that oxidation of the GaN surface is able to fill up the Ga dangling bonds and form high quality Ga-oxides on the GaN surface [301]. Among these oxidation methods, oxygen plasma technique has been found to be an effective approach to passivate the dangling bonds and remove possible carbon contamination on the GaN surface [302]. Therefore, both the removal of the

native oxide on the GaN surface and the passivation of the GaN surface by Ga-S and Ga-O bonds are regarded as effective methods to reduce the interface state.

In this work, the electrical characteristics of MIS devices with ZrO_2, Al_2O_3, MgO and Ta_2O_5 as gate dielectrics deposited by sputtering technique were studied mainly by performing the current-voltage (*IV*) and capacitance-voltage (*CV*) measurements. Moreover, the effect of several surface treatment on the D-mode and E-mode GaN/AlGaN/GaN MIS-HEMT devices are investigated by comparing the samples without any treatment and with the HCl, oxygen plasma and ODT treatments prior to the gate dielectric (Al_2O_3)-atomic layer deposition. For ZrO_2-based MIS-HEMT devices, the effect of ODT surface treatment has been investigated as well.

5.2 GaN-based MIS-capacitors

5.2.1 Device fabrication

Dr Zaffar Zaidi, Dr Kean Boon Lee and Professor Peter Houston from the Department of Electronic and Electrical Engineering, University of Sheffield, UK are acknowledged for their contribution in the fabrication of GaN-based MIS-capacitor devices. Meanwhile, all oxides have been sputtered (our main contribution) in the Department of Electrical Engineering and Electronics, University of Liverpool, UK. In this work, several GaN-based MIS-capacitors were fabricated with different oxide layers: ZrO_2, Al_2O_3, MgO and Ta_2O_5. The surface treatment is performed first for all samples to remove any native oxides by immersing in acetone and methanol for 10 min and followed with immersing in 37% hydrochloric acid (HCl) for 20 min and then rinsed with deionised water. The fabrication of MIS-capacitor devices started with the formation of ohmic contacts by electron-beam evaporation of Ti/Al/Ni/Au: 20 nm/120

nm/20 nm/45 nm. The spacing between the metal gate and ohmic contacts was varied from 5 μm to 15 μm. The samples then underwent rapid thermal annealing (RTA) at 850 °C for 30 seconds in nitrogen (N_2) ambient. The oxide layers of ZrO_2, Al_2O_3, MgO and Ta_2O_5 with a nominal thickness of 20 nm were sputtered using radio frequency sputtering technique. The plasma power used for ZrO_2, MgO and Ta_2O_5 deposition was 60 W, while for Al_2O_3 it was 45 W with the chamber pressure of 1×10^{-3} mbar at room temperature (RT). The sputtering deposition rate was 0.1 Å/s for ZrO_2 and MgO, whereas for Al_2O_3 and Ta_2O_5 it was found to be 0.07 Å/s and 0.5 Å/s, respectively. Next step was followed by the deposition of the circular gate electrode of Ni/Au: 20 nm/180 nm with the diameter of metal gate, d varying from 20 to 200 μm and the spacing between metal gate and ohmic contacts, s varying from 5 μm to 15 μm. Figure 5.2 shows the schematic structure of the GaN MIS-capacitor with oxide layers (ZrO_2 or Al_2O_3 or MgO or Ta_2O_5) and the fabrication flow.

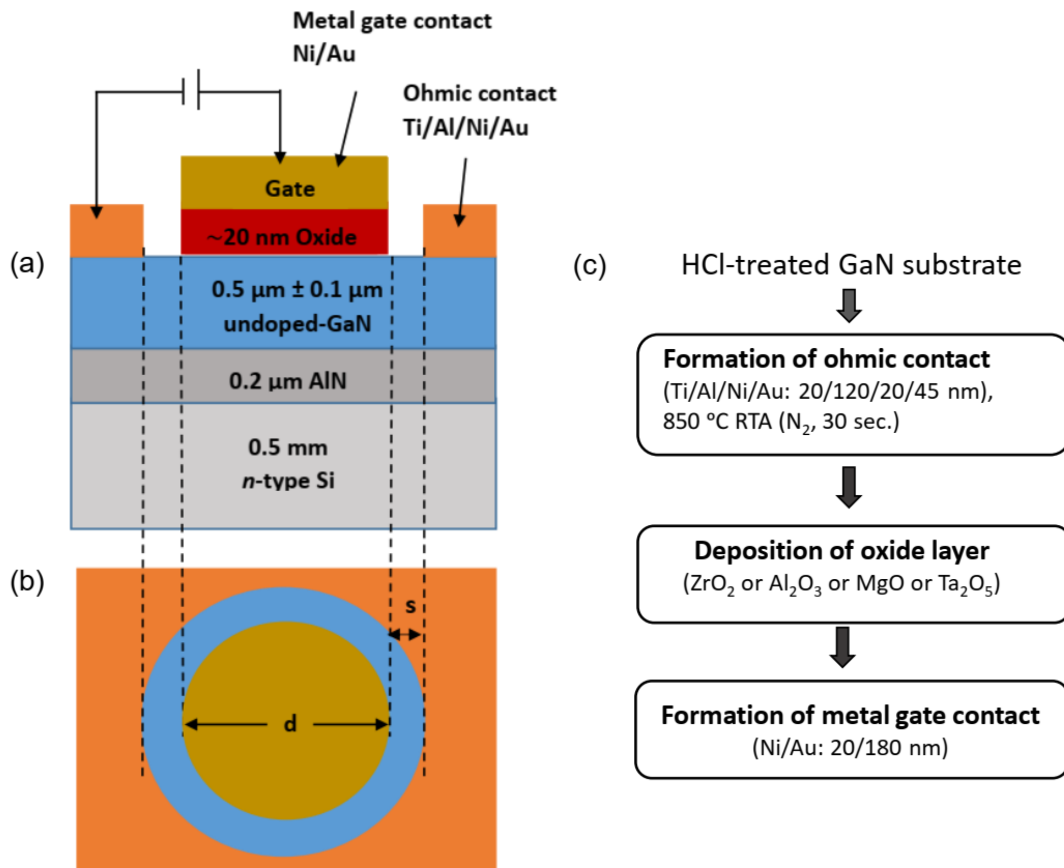

Figure 5.2: The schematic cross-section (a) side view and (b) top view with the diameter of metal gate, d and the spacing between metal gate and ohmic contacts, s; and (c) fabrication flow for the GaN-based MIS-capacitor with oxide layers (ZrO_2 or Al_2O_3 or MgO or Ta_2O_5).

5.2.2 Oxide thickness estimation using VASE

Room temperature VASE measurements were performed using a J.A.Woollam M2000 ellipsometer with a wavelength range of 241.1 nm–1686.7 nm which corresponds to an energy range of 0.7 eV–5.2 eV. There were three incident angles chosen at 60°, 65° and 70° around the Brewster angle in order to increase the resolution of the measurements for extracting thickness of the oxide layer. The experimental data extracted in the form of two angles (ψ, Δ) vs photon energy (E) were analysed using Complete EASE software program by developing a theoretical model to match the experimental results. The initial attempt was to model the Si substrate using the predefined Si model ("Si with native oxide model") which is available in the software

database since all the oxides were deposited on Si. Then, as seen in Figure 5.3, the relevant predefined oxide layers using “Cauchy layer” were superimposed to the Si reference model and extracted the thicknesses. This was achieved by placing a Si substrate in the chamber using the same parameters used for the deposition of oxides on GaN substrate to verify the thickness by VASE. It has been observed from Figure 5.3 that the extracted thicknesses of the ZrO_2, Al_2O_3, MgO, and Ta_2O_5 are 16.97 nm, 19.41 nm, 21.93 nm and 19.85 nm, respectively. The mean squared error (MSE) between the experimental and theoretical (fitted) curves was in all cases below 5, consistent with a good quality fit of the data. Table 5.1 shows the measured thickness of oxide layers (ZrO_2, Al_2O_3, MgO, and Ta_2O_5), where the nominal thickness for all deposited oxides is 20 nm.

Table 5.1: The thickness of oxide layers (ZrO_2, Al_2O_3, MgO, Ta_2O_5) extracted by VASE.

Oxide layer	Nominal thickness (nm)	Measured thickness by VASE (nm)
ZrO_2	20	16.95
Al_2O_3	20	19.41
MgO	20	21.93
Ta_2O_5	20	19.85

(a)

Layer # 2 = ZrO2 (Cauchy) Thickness # 2 = **16.95 nm** (fit)
Layer # 1 = NTVE_JAW Native Oxide = 1.99 nm
Substrate = SI_JAW

(b)

Layer # 2 = Al2O3 (Cauchy) Thickness # 2 = **19.41 nm** (fit)
Layer # 1 = NTVE_JAW Native Oxide = 1.99 nm
Substrate = SI_JAW

(c)

Layer # 2 = MgO (Cauchy) Thickness # 2 = **21.93 nm** (fit)
Layer # 1 = NTVE_JAW Native Oxide = 1.99 nm
Substrate = SI_JAW

(d)

Layer # 2 = Ta2O5 (Cauchy) Thickness # 2 = **19.85 nm** (fit)
Layer # 1 = NTVE_JAW Native Oxide = 1.99 nm
Substrate = SI_JAW

Figure 5.3: The VASE model used to extract thickness of RF-sputtered oxide layers for (a) ZrO_2/Si; (b) Al_2O_3/Si; (c) MgO/Si; and (d) Ta_2O_5/Si reference samples.

5.2.3 IV measurements

The current-voltage and current density-voltage (*JV*) characteristics of MIS-capacitors fabricated using the four different dielectrics are shown in Figure 5.4. The leakage current density of MIS-capacitor with 16.95 nm ZrO_2 gate dielectric is 6.2 $\times10^{-4}$ A/cm^2 at 1 V, which, taking into account the difference in oxide thickness, is lower than the previously reported value of 0.88 A/cm^2 at 1 V for 4.4 nm ALD-deposited ZrO_2/GaN MIS-capacitor [303]. Similarly, the 19.41 nm Al_2O_3-based MIS-capacitor shows a lower leakage current density than that of ZrO_2 of 5.3×10^{-6} A/cm^2 at 1 V gate bias. A value of 1×10^{-4} A/cm^2 at –10 V was reported for 25 nm Al_2O_3 on HF treated GaN deposited by ALD [265] and 5.33×10^{-2} A/cm^2 at 4 V for the ALD-deposited 14 nm Al_2O_3 on an HCl treated GaN substrate [304]. The leakage current density for the 21.93 nm MgO MIS-capacitor is 3.2 $\times10^{-6}$ A/cm^2 at 1 V. A value of 5 $\times10^{-3}$ A/cm^2 for 80 nm MgO in GaN MIS-FET (Field Effect Transistor) device at 2.2 V has been reported [305]. For 19.85 nm Ta_2O_5/GaN MIS-capacitor the leakage current density is found to be 7.7 $\times10^{-4}$ A/cm^2 at 1 V. Direct comparisons with the literature is problematic due to the different oxide thicknesses, but considering the

trends in the scaling of SiO_2, our oxides can be considered relatively low leakage. It is critically important that a gate dielectric has sufficient band offsets of at least 1 eV to ensure that carriers are confined mainly within the channel. The band offsets affect the gate leakage current with an exponential relationship. In our work, MgO exhibits the lowest leakage current density with the highest valence band offset (VBO) and conduction band offset (CBO) of 1.2 eV and 2.8 eV respectively, whereas ZrO_2-based devices have the highest leakage current density corresponding to VBO and CBO of 0.4 eV and 1.3 eV, respectively. Note that the referenced papers lack analysis of the leakage current data. A weak temperature dependence was noted for the oxide leakage in ALD deposited ZrO_2 on GaN [303] indicating the dominance of a tunnelling mechanism, but a barrier height (conduction band offset) was not extracted. The band offset values (VBO = 1 eV and CBO = 2.2 eV) obtained by Jia *et al.* [265] are comparable with this work (VBO = 1.1 eV and CBO = 2.2 eV) but the different test conditions make it difficult to compare leakage currents directly. Wei *et al.* [304], Irokawa *et al.* [305] and Kim *et al.* [306] have reported leakage currents similar to those of this work but did not investigate conduction mechanisms or extract band offset(s).

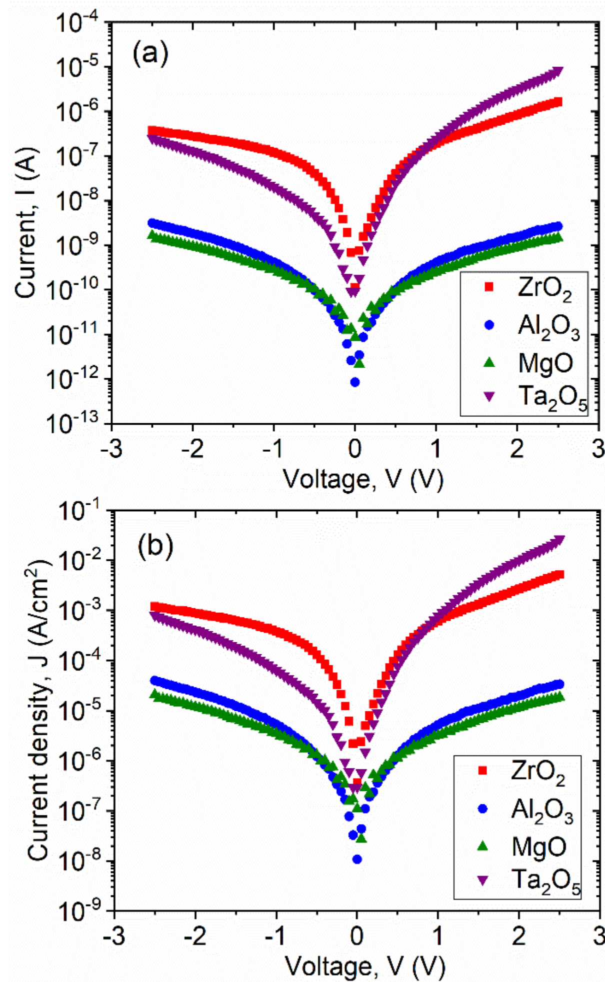

Figure 5.4: (a) The *IV* and (b) *JV* plots for MIS-capacitors on GaN with four different gate dielectrics (ZrO_2, Al_2O_3, MgO, and Ta_2O_5) deposited by RF sputtering technique.

The *IV* measurement for all devices were repeated for at least 10 devices for each samples and *JV* plots are represented as shown in Figures 5.5, 5.7, 5.9, and 5.11 to ensure the results are accurate. Non-uniformity of leakage current densities have been found for all GaN-based MIS-capacitors with different dielectrics: ZrO_2, Al_2O_3, MgO, and Ta_2O_5. Moreover, the *JV* plots showing the mean values with quite large standard deviation for all GaN-based MIS-capacitors as shown in Figures 5.6, 5.8, 5.10, and 5.12.

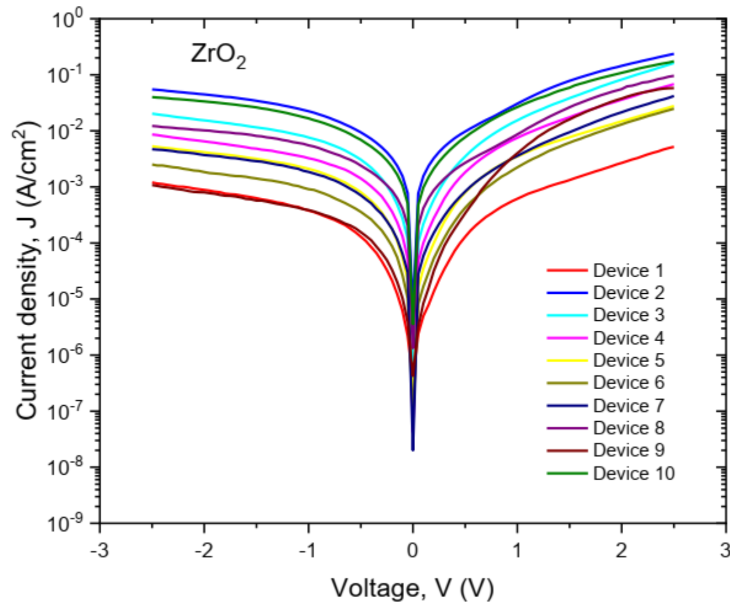

Figure 5.5: *JV* plots for the GaN-based MIS-capacitors with ZrO_2 gate dielectrics.

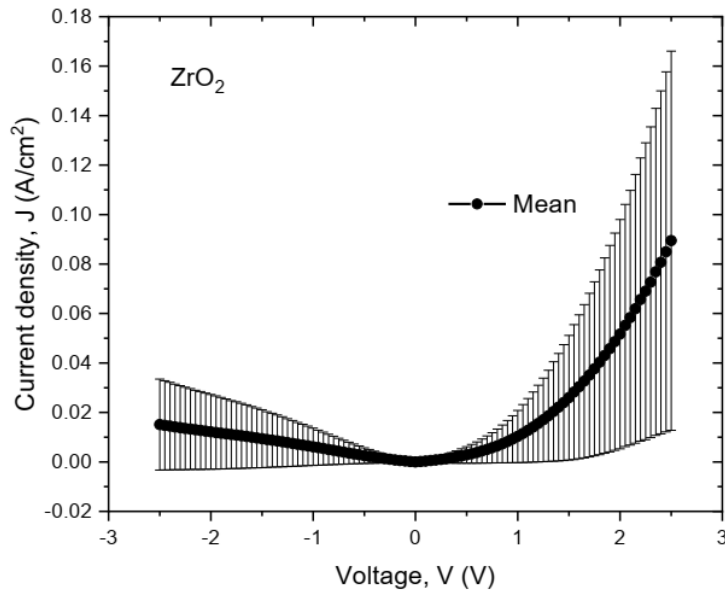

Figure 5.6: *JV* plots showing the mean and standard deviation for the GaN-based MIS-capacitors with ZrO_2 gate dielectrics.

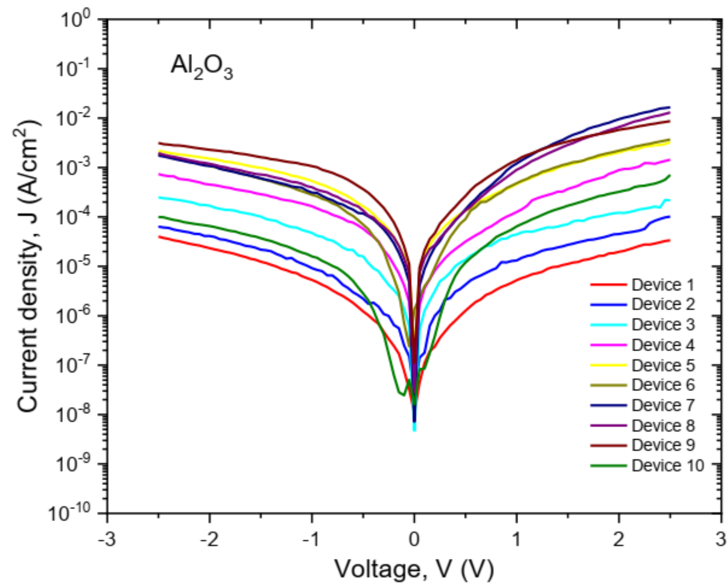

Figure 5.7: *JV* plots for the GaN-based MIS-capacitors with Al_2O_3 gate dielectrics.

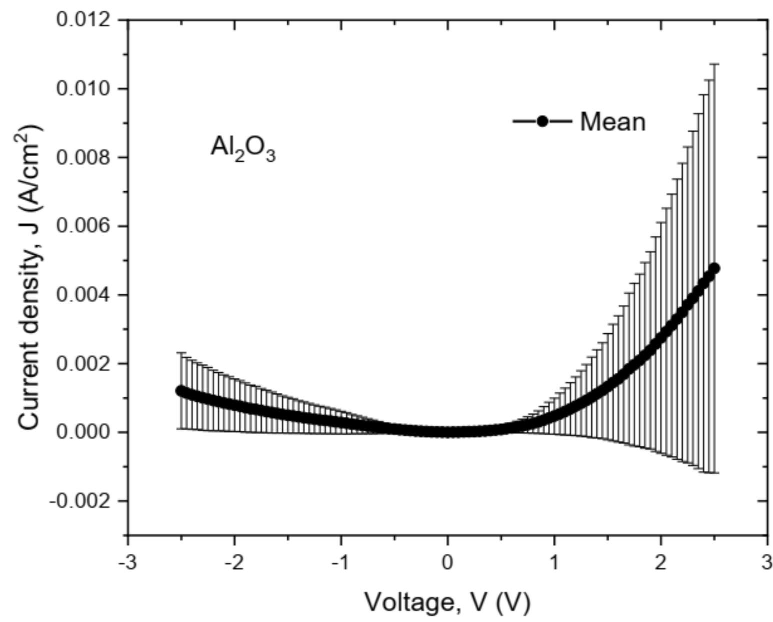

Figure 5.8: *JV* plots showing the mean and standard deviation for the GaN-based MIS-capacitors with Al_2O_3 gate dielectrics.

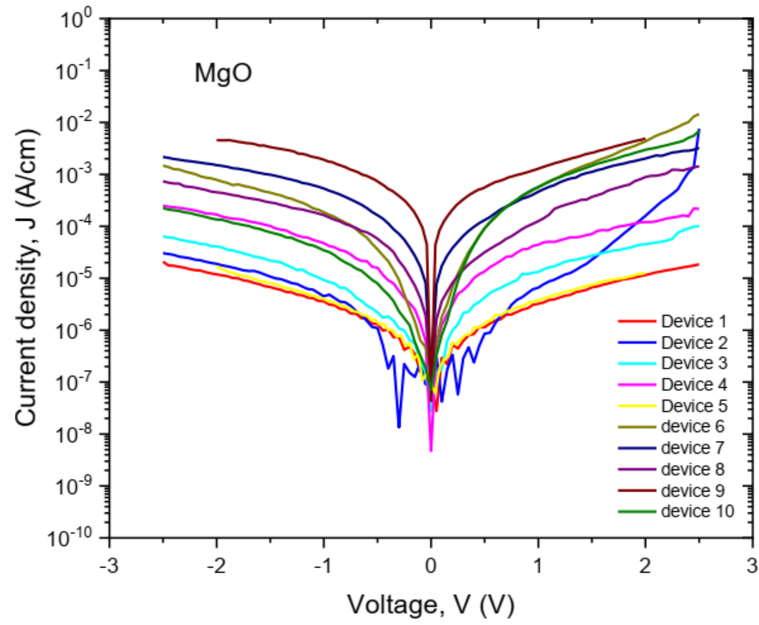

Figure 5.9: *JV* plots for the GaN-based MIS-capacitors with MgO gate dielectrics.

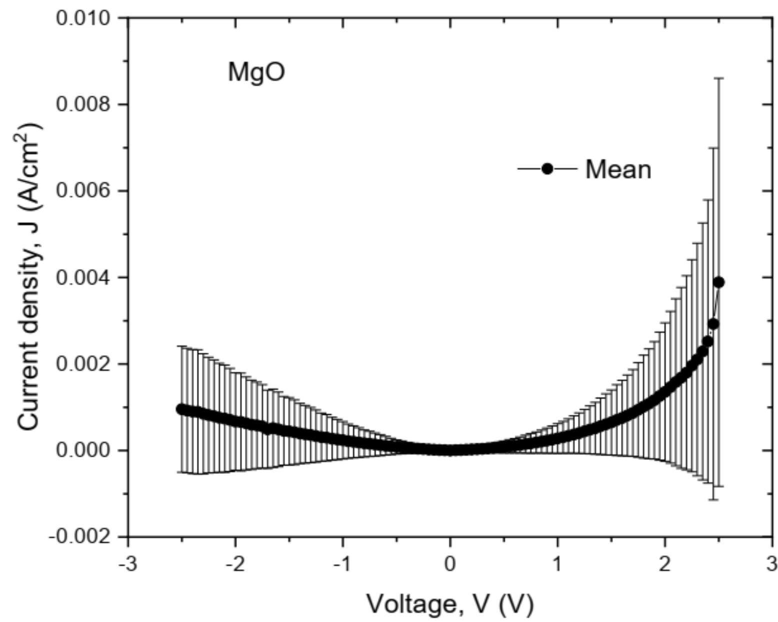

Figure 5.10: *JV* plots showing the mean and standard deviation for the GaN-based MIS-capacitors with MgO gate dielectrics.

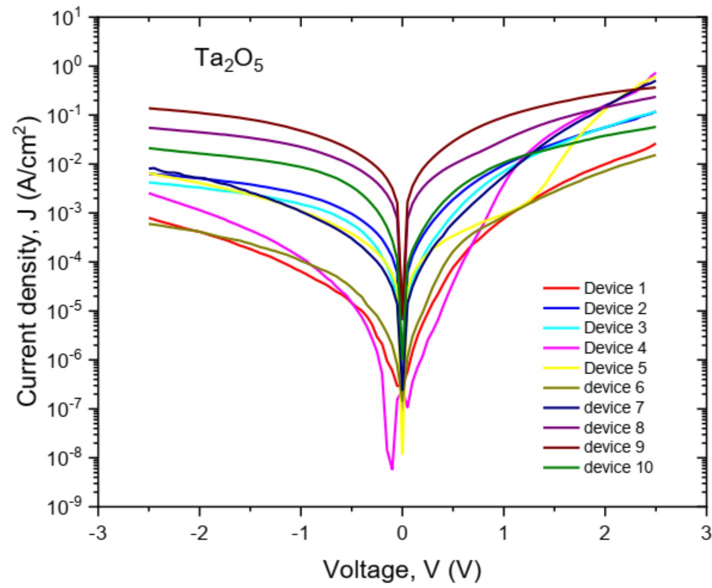

Figure 5.11: *JV* plots for the GaN-based MIS-capacitors with Ta_2O_5 gate dielectrics.

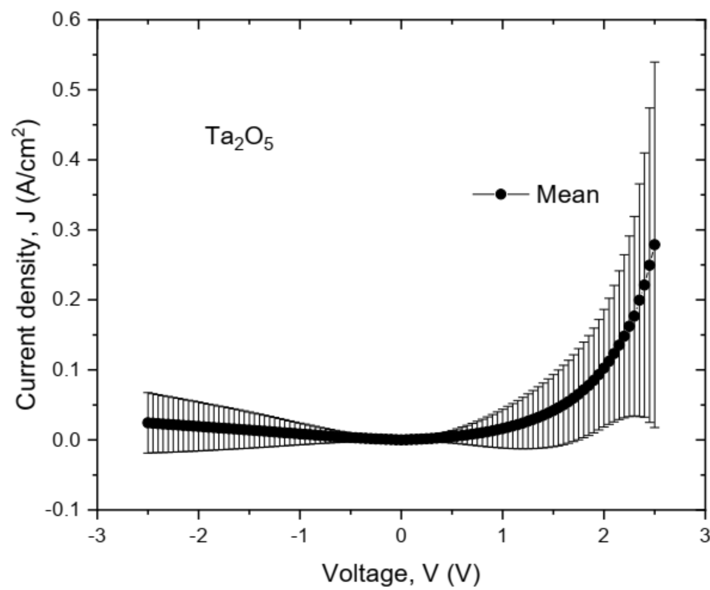

Figure 5.12: *JV* plots showing the mean and standard deviation for the GaN-based MIS-capacitors with Ta_2O_5 gate dielectrics.

Therefore, in our work the lowest current densities are used for comparison as shown in Figure 5.4. Similar trend is also found in the comparison of mean values as represented in the Figure 5.13. The lowest mean of leakage current density of 2.8×10^{-4} A/cm^2 at 1 V is found for MIS-capacitors with MgO gate dielectric. The MIS-

capacitors with Al_2O_3 gate dielectric provides a low mean J_{th} similar to the MIS-capacitors with MgO with value of 4.7×10^{-4} A/cm^2 at 1 V. The highest mean J_{th} of 1.7×10^{-2} A/cm^2 at 1 V is found for the MIS-capacitors with Ta_2O_5 and followed by the MIS-capacitors with ZrO_2 gate dielectric where the mean of J_{th} is found to be 1.0×10^{-2} A/cm^2 at 1 V. The values of mean, standard deviation, standard error for all devices are shown in Table 5.2.

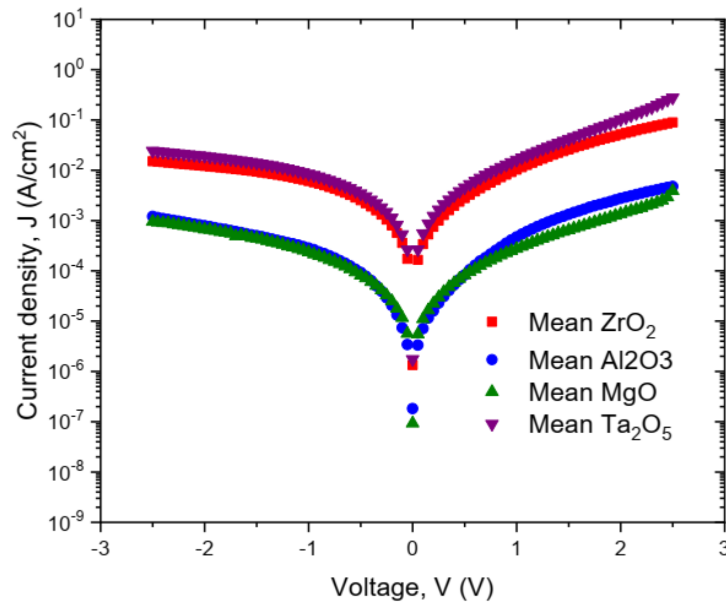

Figure 5.13: *JV* plots showing the comparison of the mean values of different GaN-based MIS-capacitors with different dielectrics (ZrO_2, Al_2O_3, MgO, and Ta_2O_5).

Table 5.2: The comparison values of mean, standard deviation, and standard error for different dielectrics (ZrO_2, Al_2O_3, MgO, and Ta_2O_5) MIS-capacitor devices.

Oxide	Mean at 1 V (A/cm^2)	Standard deviation at 1 V (A/cm^2)	Standard error of mean at 1 V (A/cm^2)
ZrO_2	1.0×10^{-2}	1.1×10^{-2}	3.3×10^{-3}
Al_2O_3	4.7×10^{-4}	5.3×10^{-4}	1.7×10^{-4}
MgO	2.8×10^{-4}	3.4×10^{-4}	1.1×10^{-4}
Ta_2O_5	1.7×10^{-2}	2.8×10^{-2}	8.8×10^{-3}

5.2.4 Conduction mechanisms

Further details of the leakage current require the analysis of the leakage current density versus electric field (*JE*) characteristics of the GaN-based MIS-capacitors. Figure 5.14 shows the comparison of *JE* plots for MIS-capacitors on GaN with four different gate dielectrics (ZrO_2, Al_2O_3, MgO, and Ta_2O_5) deposited by RF sputtering technique. It can be found that the GaN MIS-capacitor with MgO shows the lowest leakage current density of 1.4 $\times 10^{-5}$ A/cm^2 at 1 MV/cm compared to the MIS-capacitors with other gate dielectrics. Similarly, a low leakage current density of 1.9 $\times 10^{-5}$ A/cm^2 at the electric field of 1 MV/cm is found for MIS-capacitor with Al_2O_3. In comparison, very low current densities of 1.9 $\times 10^{-7}$ A/cm^2 and 2.2 $\times 10^{-8}$ A/cm^2 at 3 MV/cm have been reported for H_2O vapor or O_3 in thermal ALD and O_2 plasma in plasma-assisted ALD Al_2O_3 GaN MISFETs, respectively [307]. However, the MIS-capacitor with ZrO_2 exhibits the highest leakage current density of 1.8 $\times 10^{-3}$ A/cm^2 at 1 MV/cm. Moreover, a higher leakage current density of 1.0 $\times 10^{-3}$ A/cm^2 at 1 MV/cm is found for MIS-capacitor with Ta_2O_5.

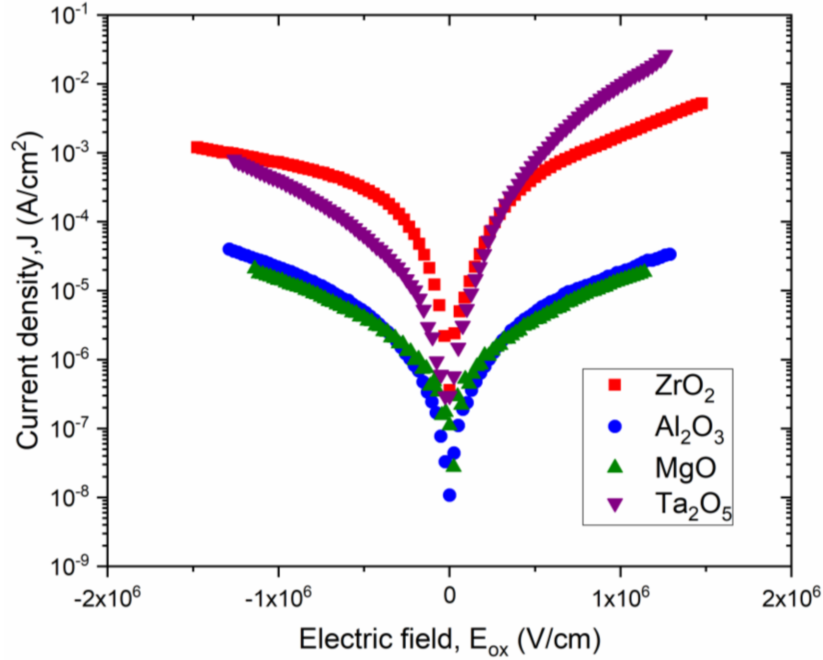

Figure 5.14: *JE* plots for MIS-capacitors on GaN with four different gate dielectrics (ZrO_2, Al_2O_3, MgO, and Ta_2O_5) at both negative and positive biases measured at room temperature measurement.

Moreover, it is important to study the leakage current mechanisms in order to find out effective ways to reduce the leakage current. In this work, the electrode-limited conduction mechanism such as Fowler-Nordheim (FN) tunnelling, as well as the bulk-limited conduction mechanisms such as Poole-Frenkel (PF) emission and space-charge-limited current (SCLC) were studied using the *IV* characteristics shown in Figure 5.4.

5.2.4.1 *Fowler-Nordheim tunnelling*

FN tunnelling is mainly applied to describe the leakage current for high electric fields E. The plot of ln (J/E^2) versus E^{-1} should be a straight line if the FN tunnelling exists. The FN plots at room temperature for different oxide layers: ZrO_2, Al_2O_3, MgO and Ta_2O_5 GaN-based MIS devices are presented here. The FN plots of ln (J/E^2) versus

E^{-1} for GaN-based MIS-capacitors with ZrO_2 and Ta_2O_5 as dielectric layers are shown in Figures 5.15 and 5.16 respectively. It can be seen that the FN plots are linear for high electric fields. The extracted value of barrier height, $\emptyset_B$ using Equation (2.15) as discussed previously in Chapter 2 for both ZrO_2-GaN based MIS and Ta_2O_5-GaN based MIS devices are found to be 0.02 eV. The $m_{ox} = 0.5m_o$ [308] is assumed for ZrO_2 and Ta_2O_5, where the m_o is free electron mass (m_o = 9.109 ×10^{-31} kg) and m_{ox} is the effective electron mass in oxide (or as decribed in Chapter 2 as the m_T^* referring to the tunnelling effective mass in the dielectric). The slope and intercept of the linear fitting of FN plots for GaN-based MIS-capacitor with ZrO_2 and Ta_2O_5 as well as the extracted barrier height are shown in Table 5.3. These extracted $\emptyset_B$ values were too small as compared to the conduction band offset (CBO) values from theoretical work: 1.1 eV for ZrO_2/GaN and 0.1 eV for Ta_2O_5/GaN [150] and from our experimental work: 1.3 eV for ZrO_2/GaN and 0.4 eV for Ta_2O_5/GaN. However, for Al_2O_3 (Figure 5.17) and MgO (Figure 5.18) GaN-based MIS devices, the linear region in high *E* were not clearly observed from FN plots. Therefore, it is not possible to extract the barrier height for Al_2O_3 and MgO-based samples.

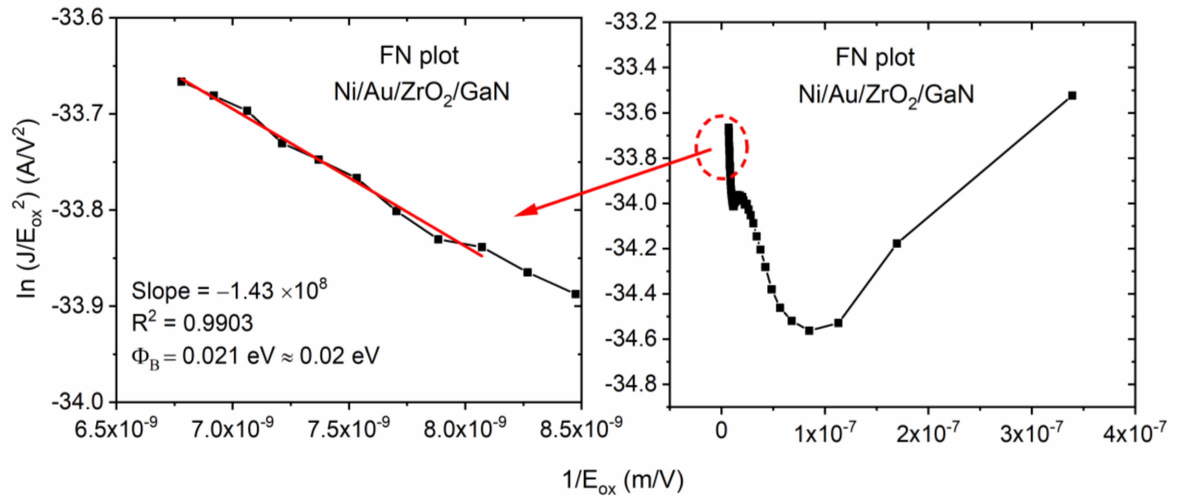

Figure 5.15: FN plots for GaN MIS-capacitor with ZrO_2 as a dielectric layer.

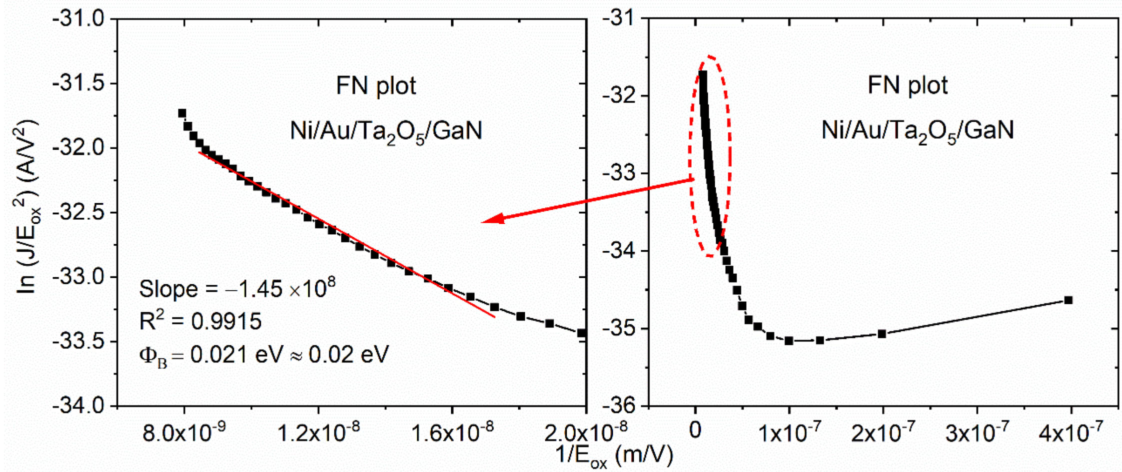

Figure 5.16: FN plots for GaN MIS-capacitor with Ta_2O_5 as a dielectric layer.

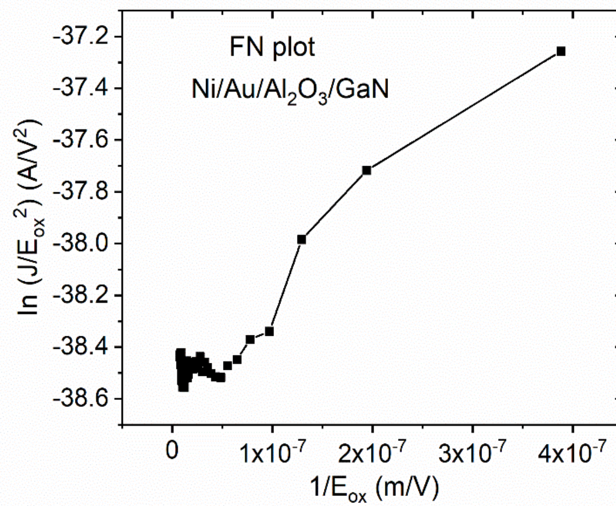

Figure 5.17: FN plot for GaN MIS-capacitor with Al_2O_3 as a dielectric layer.

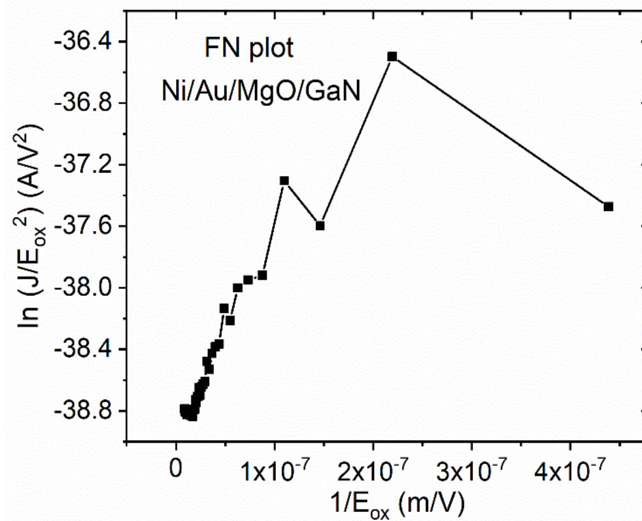

Figure 5.18: FN plot for GaN MOS-capacitor with MgO as a dielectric layer.

Table 5.3: A summary of the slope and intercept of the linear fitting from FN plots with the extracted barrier heights for ZrO_2/GaN and Ta_2O_5/GaN MIS capacitors.

Oxide	Intercept	Slope	R^2	$\emptyset_B$ (eV)
ZrO_2	−32.70	-1.43×10^8	0.9903	0.02
Ta_2O_5	−30.81	-1.45×10^8	0.9915	0.02

The FN conduction mechanism analysis for all devices were repeated for at least 5 devices for each samples and FN plots are represented as shown in Figures 5.19−5.35 to ensure the results are accurate. The FN plots of ln (J/E^2) versus E^{-1} for GaN-based MIS-capacitors with ZrO_2 as dielectric layers are shown in Figures 5.19−5.24. It can be seen that the FN plots for these 5 devices are linear at high electric fields. The extracted values of barrier height, $\emptyset_B$ are very small with the values between 0.01-0.02 eV as shown in the Table 5.4.

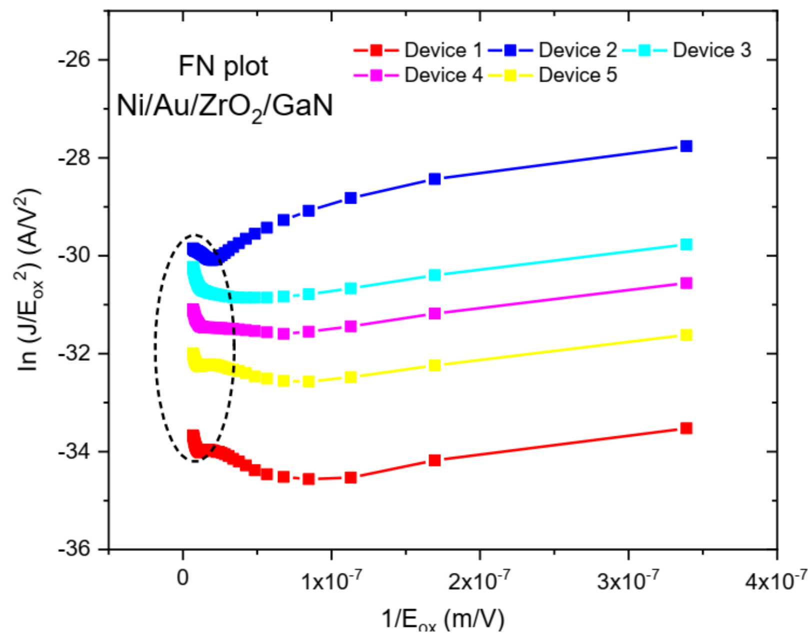

Figure 5.19: FN plots for the GaN-based MIS-capacitors with ZrO_2 as a dielectric layer.

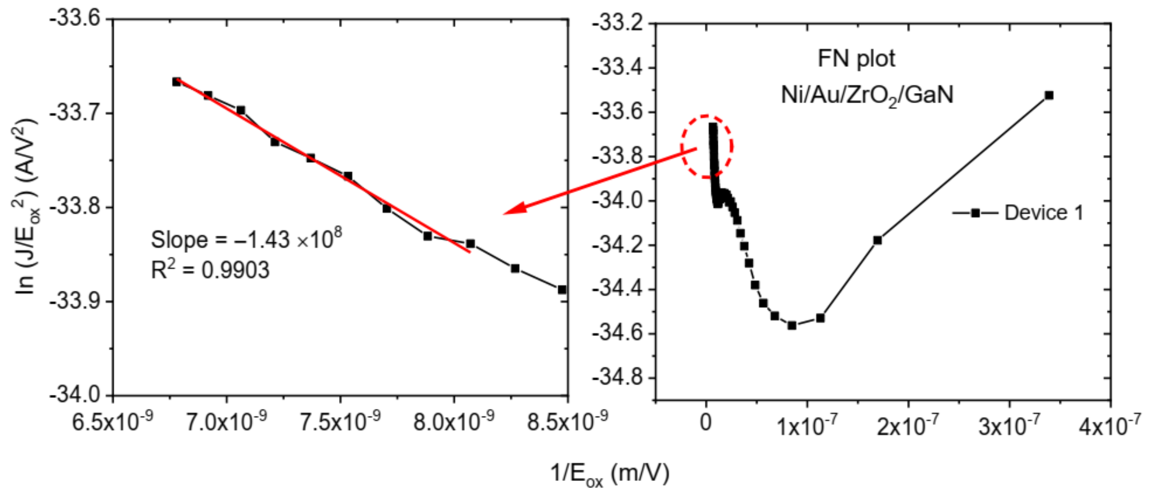

Figure 5.20: FN plots for the GaN-based MIS-capacitor with ZrO_2 as a dielectric layer (Device 1).

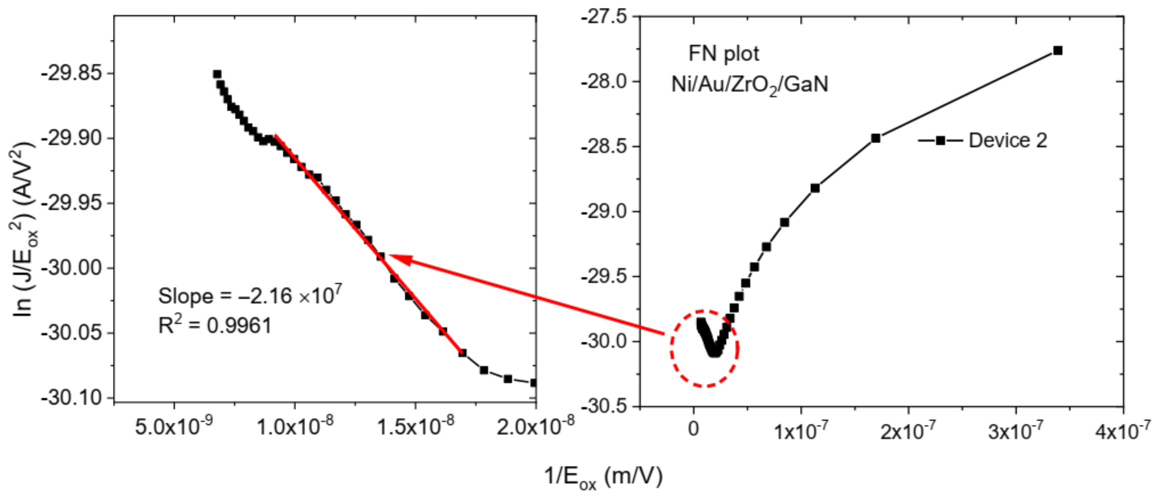

Figure 5.21: FN plots for the GaN-based MIS-capacitor with ZrO_2 as a dielectric layer (Device 2).

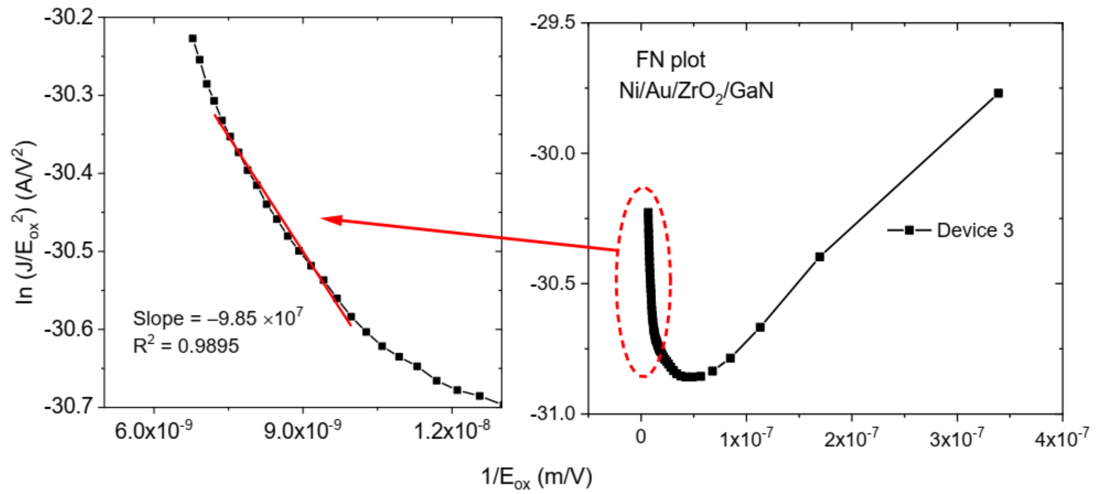

Figure 5.22: FN plots for the GaN-based MIS-capacitor with ZrO_2 as a dielectric layer (Device 3).

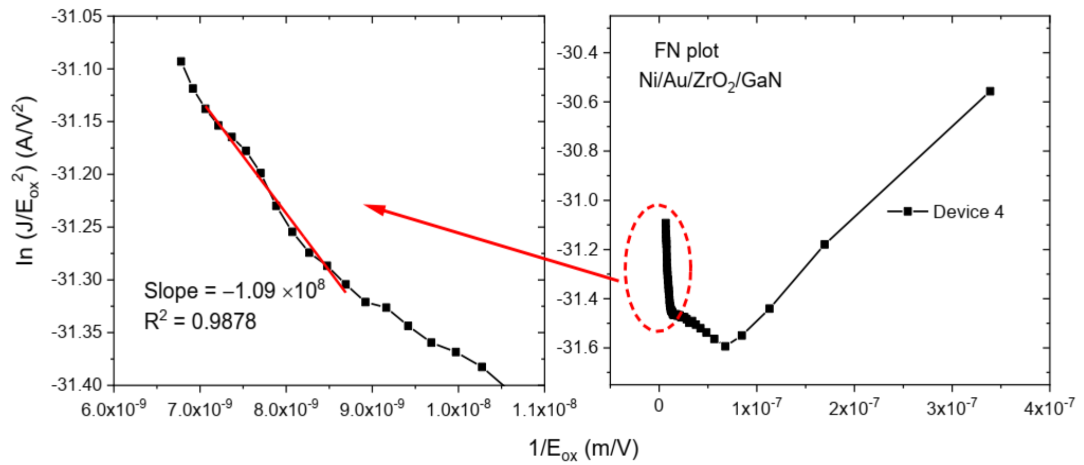

Figure 5.23: FN plots for the GaN-based MIS-capacitor with ZrO_2 as a dielectric layer (Device 4).

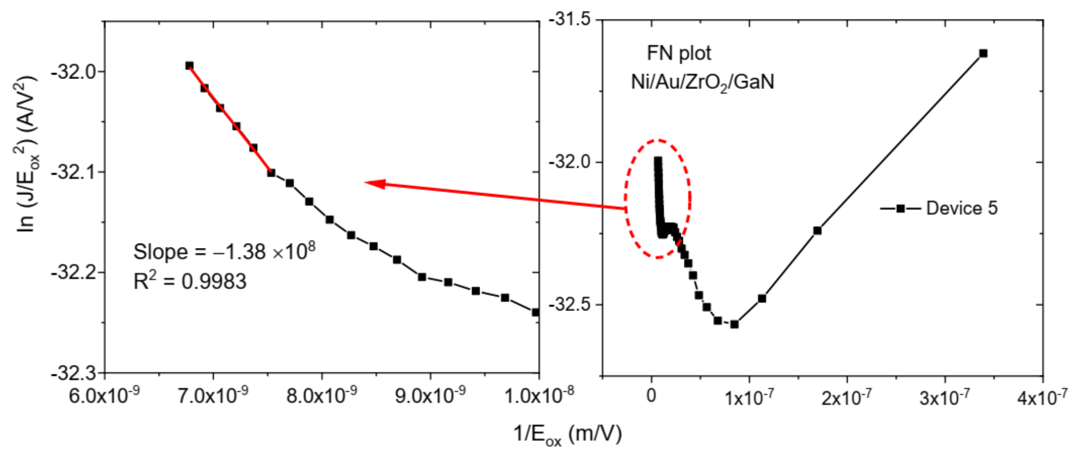

Figure 5.24: FN plots for the GaN-based MIS-capacitor with ZrO_2 as a dielectric layer (Device 5).

Table 5.4: The comparison of the slope and intercept of the linear fitting from FN plots with the extracted barrier heights for ZrO_2/GaN MIS-capacitor devices.

Oxide	Intercept	Slope	R^2	$\emptyset_B$ (eV)
ZrO_2 Device 1	−32.70	-1.43×10^8	0.9903	0.02
ZrO_2 Device 2	−29.70	-2.16×10^7	0.9961	$0.006 \approx 0.01$
ZrO_2 Device 3	−29.61	-9.85×10^7	0.9895	$0.016 \approx 0.02$
ZrO_2 Device 4	−30.37	-1.09×10^8	0.9878	$0.017 \approx 0.02$
ZrO_2 Device 5	−31.36	-1.38×10^8	0.9983	0.02

Moreover, the FN plots of ln (J/E^2) versus E^{-1} for GaN-based MIS-capacitors with Al_2O_3 as dielectric layers are shown in Figures 5.25 and 5.26. It can be seen that the FN plot for Device 4 is linear at high electric field where a very small of 0.01 eV barrier height, $\emptyset_B$ is extracted as shown in the Table 5.5.

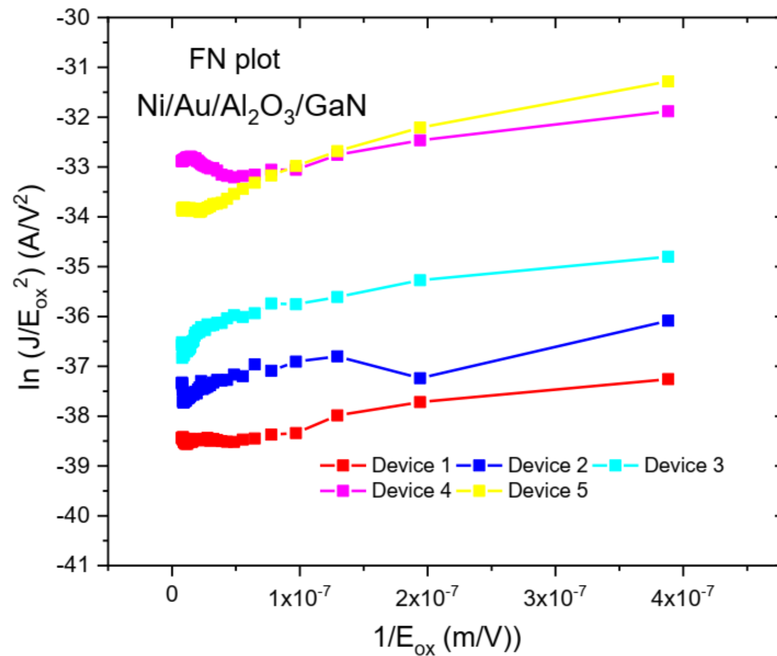

Figure 5.25: FN plots for the GaN-based MIS-capacitors with Al_2O_3 as a dielectric layer.

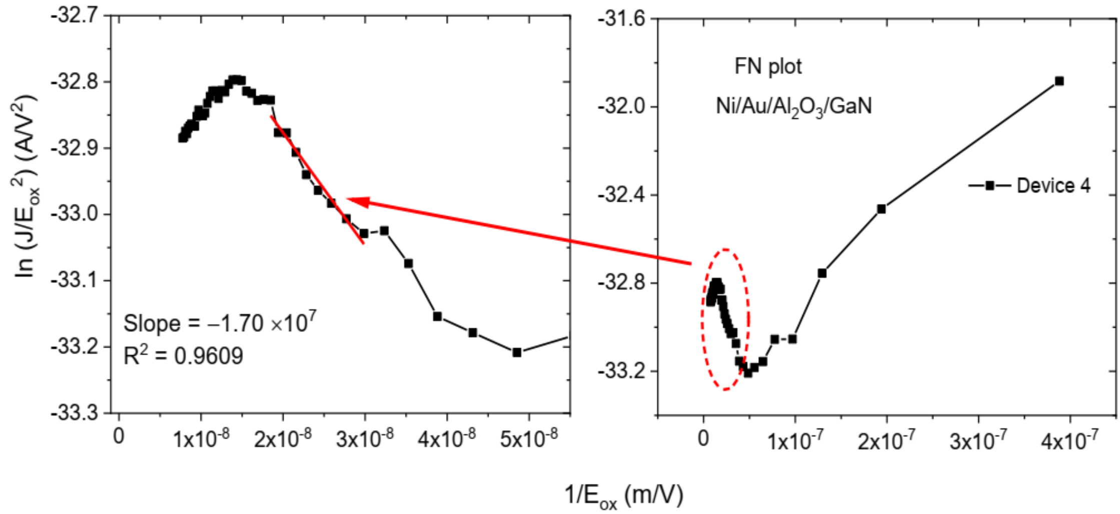

Figure 5.26: FN plots for the GaN-based MIS-capacitor with Al_2O_3 as a dielectric layer (Device 4).

Table 5.5: The slope and intercept of the linear fitting from FN plot with the extracted barrier height for Al_2O_3/GaN MIS-capacitor (Device 4).

Oxide	Intercept	Slope	R^2	$\emptyset_B$ (eV)
Al_2O_3 Device 4	−32.54	-1.70×10^7	0.9609	0.005 ≈ 0.01

Besides, the FN plots of ln (J/E^2) versus E^{-1} for GaN-based MIS-capacitors with MgO as dielectric layers are shown in Figures 5.27 and 5.29. It can be seen that the FN plots for Devices 2 and 5 are found to be linear at high electric field. Then, the extracted values of barrier height, $\emptyset_B$ are found to be 0.01 eV and 0.05 eV, respectively as shown in the Table 5.6.

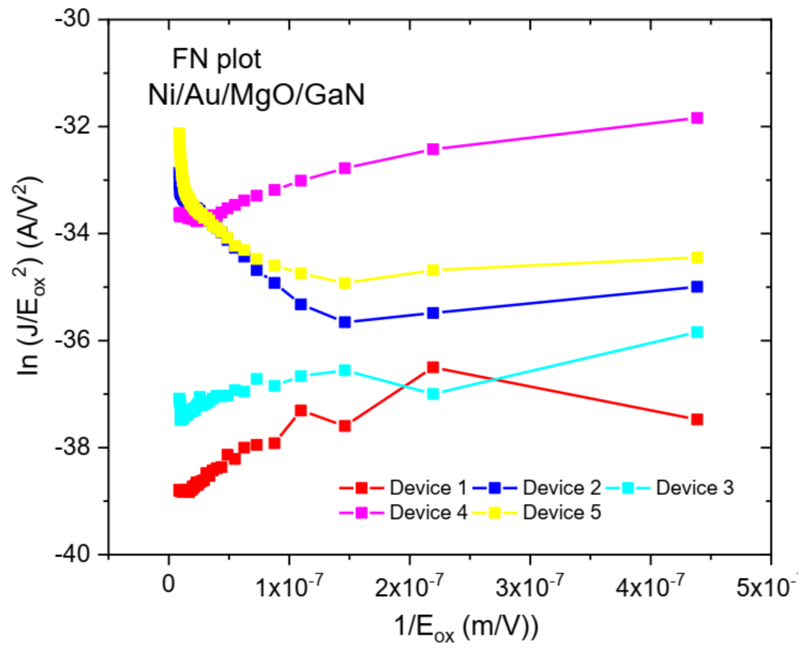

Figure 5.27: FN plots for the GaN-based MIS-capacitors with MgO as a dielectric layer.

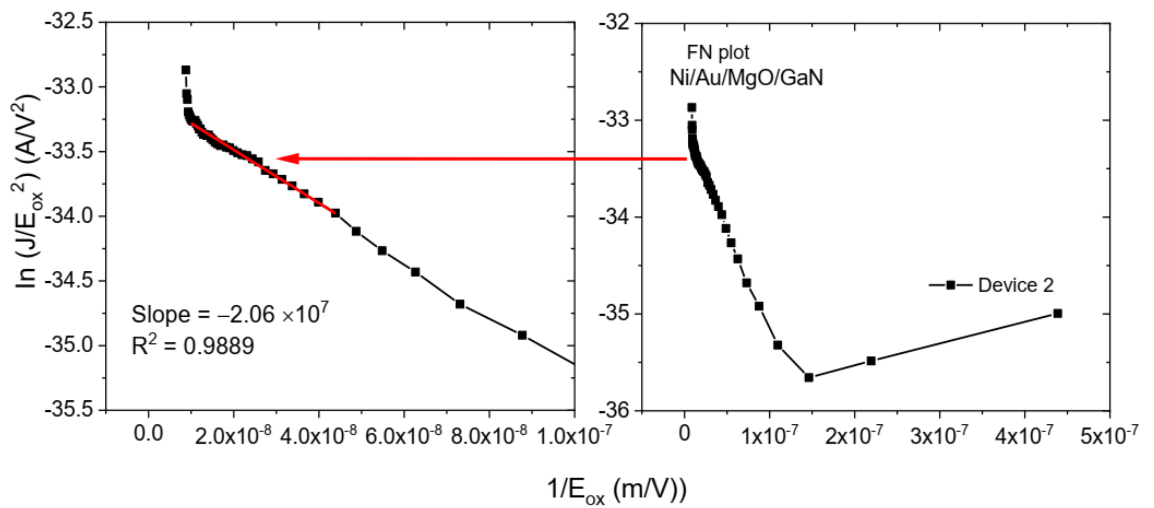

Figure 5.28: FN plots for the GaN-based MIS-capacitor with MgO as a dielectric layer (Device 2).

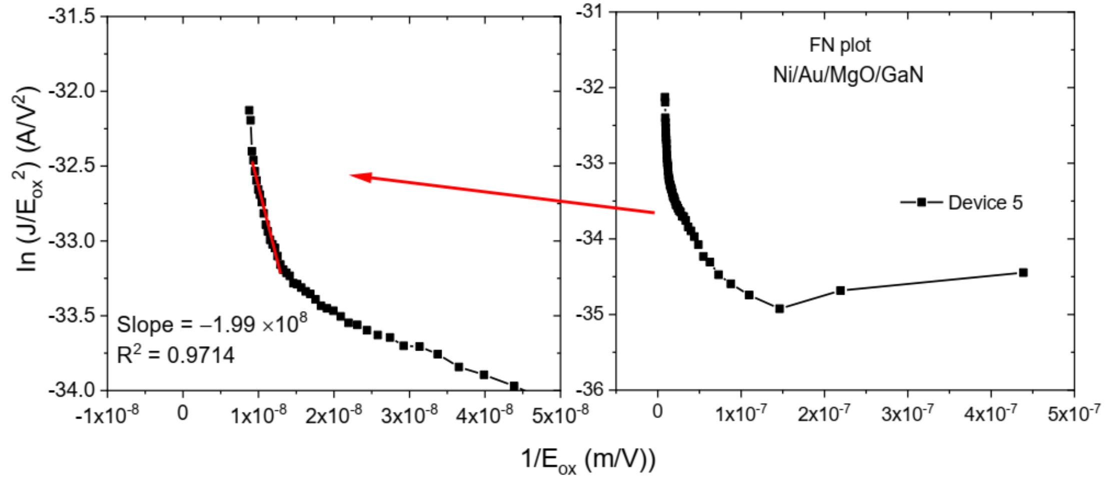

Figure 5.29: FN plots for the GaN-based MIS-capacitor with MgO as a dielectric layer (Device 5).

Table 5.6: The slope and intercept of the linear fitting from FN plot with the extracted barrier height for MgO/GaN MIS-capacitor devices.

Oxide	Intercept	Slope	R^2	$\emptyset_B$ (eV)
MgO Device 2	−33.08	-2.06×10^7	0.9889	0.006 ≈ 0.01
MgO Device 5	−30.65	-1.99×10^8	0.9714	0.045 ≈ 0.05

The FN plots of ln (J/E^2) versus E^{-1} for GaN-based MIS-capacitors with Ta_2O_5 as dielectric layers are shown in Figures 5.30−5.35. The FN plots for all devices (Devices 1−5) are found to be linear at high electric field. Then, the extracted values of barrier height, $\emptyset_B$ are between 0.01 eV − 0.06 eV as shown in the Table 5.7. Different gate stacks exhibited different FN characteristics at high fields due to the quality of deposited oxides. Besides, both band gap and the permittivity of the dielectrics influence the quality of oxides. Therefore, based on these FN analysis, it can be concluded that the FN tunnelling is not dominant conduction mechanism for all GaN-based MIS-capacitor samples with oxide layers: ZrO_2, Al_2O_3, MgO, and Ta_2O_5 indicating poor quality of oxide layer on GaN.

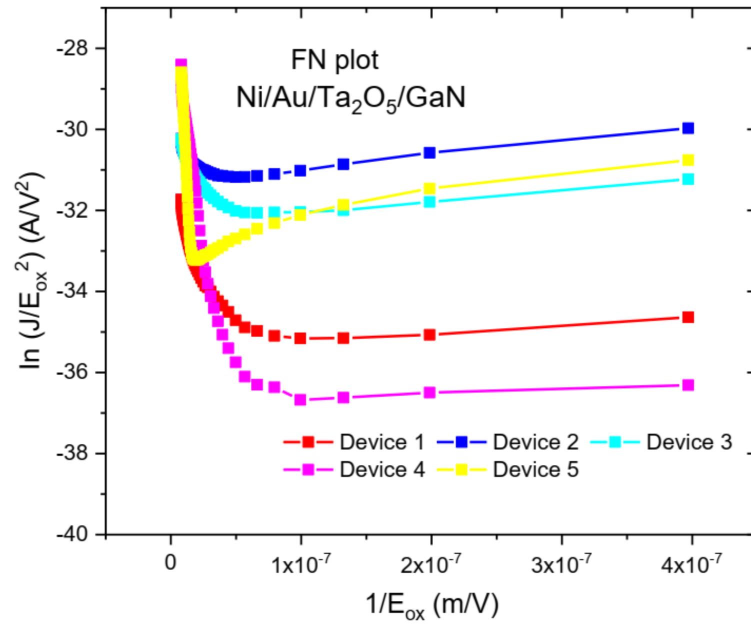

Figure 5.30: FN plots for the GaN-based MIS-capacitors with Ta_2O_5 as a dielectric layer.

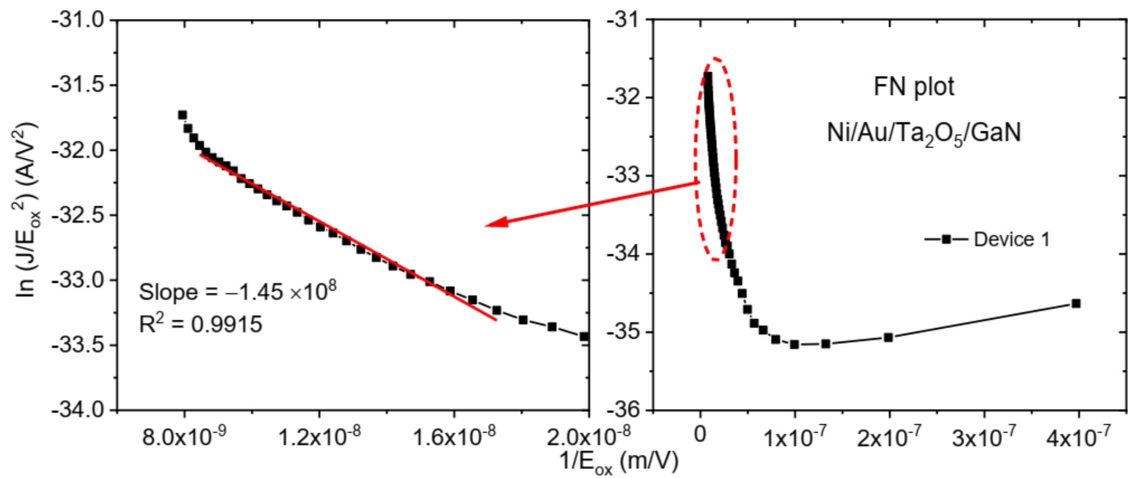

Figure 5.31: FN plots for the GaN-based MIS-capacitor with Ta_2O_5 as a dielectric layer (Device 1).

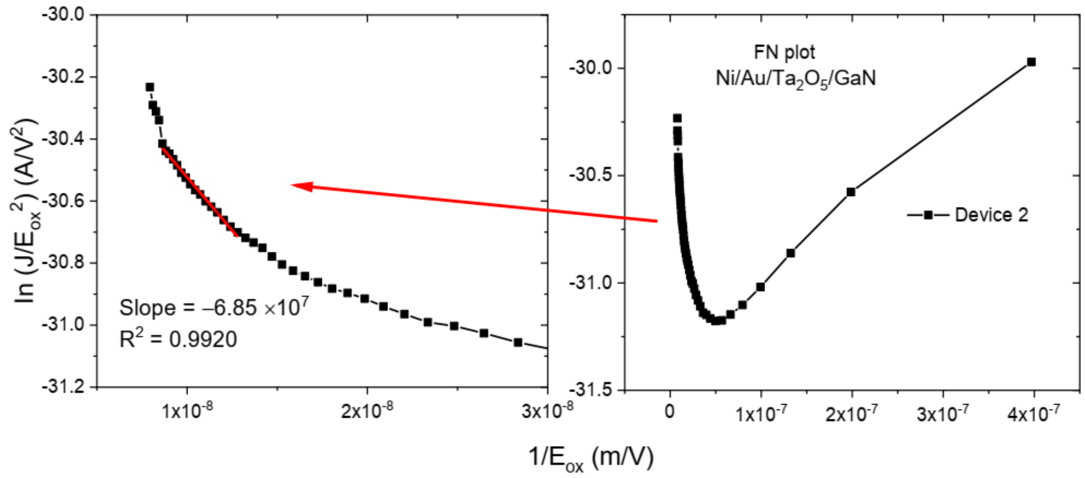

Figure 5.32: FN plots for the GaN-based MIS-capacitor with Ta_2O_5 as a dielectric layer (Device 2).

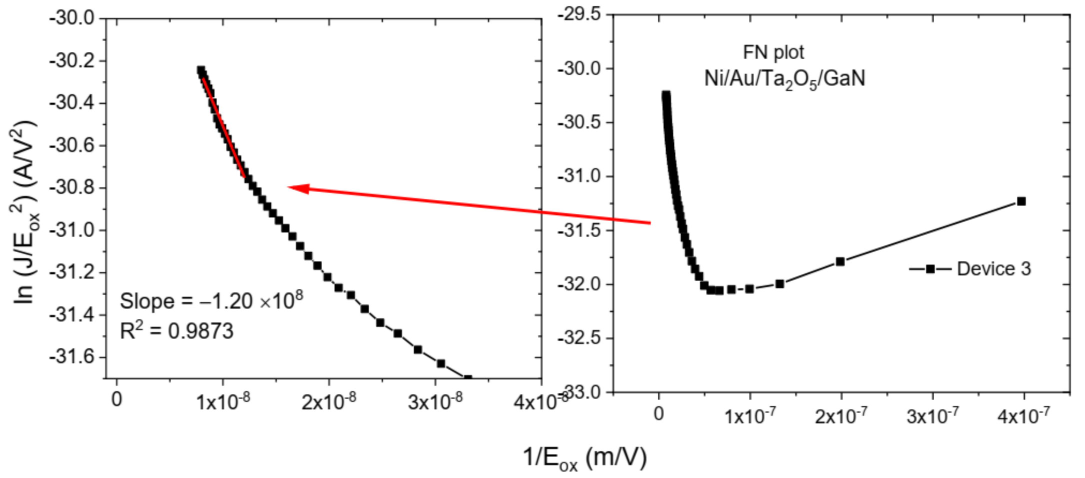

Figure 5.33: FN plots for the GaN-based MIS-capacitor with Ta_2O_5 as a dielectric layer (Device 3).

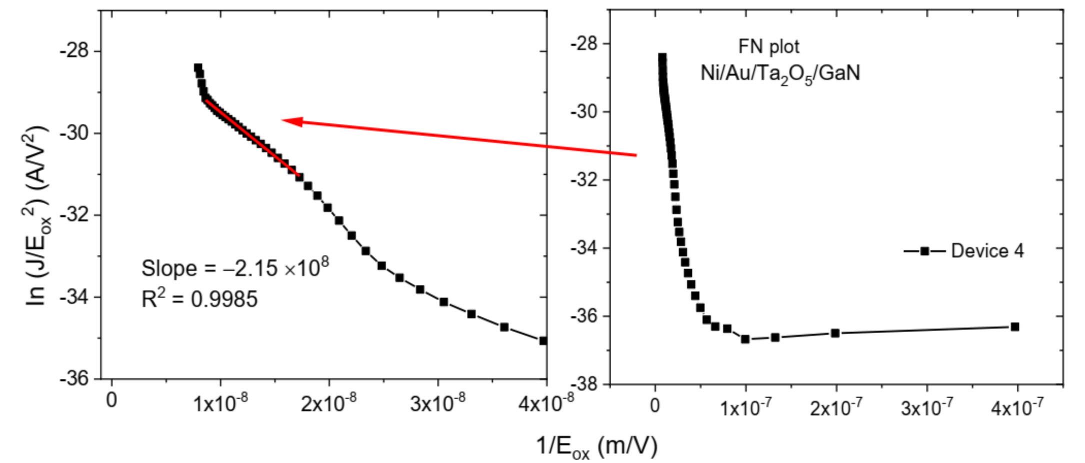

Figure 5.34: FN plots for the GaN-based MIS-capacitor with Ta_2O_5 as a dielectric layer (Device 4).

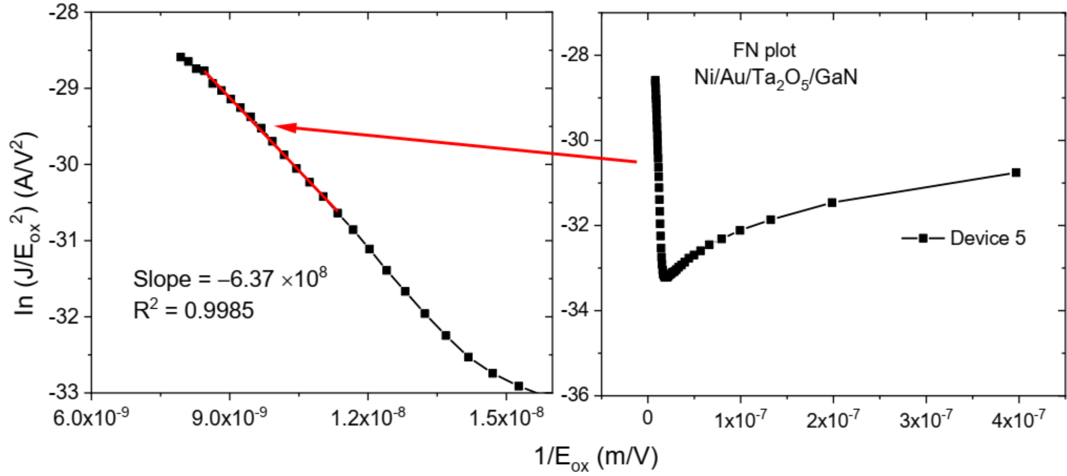

Figure 5.35: FN plots for the GaN-based MIS-capacitor with Ta_2O_5 as a dielectric layer (Device 5).

Table 5.7: The slope and intercept of the linear fitting from FN plot with the extracted barrier height for Ta_2O_5/GaN MIS-capacitor devices.

Oxide	Intercept	Slope	R^2	$\emptyset_B$ (eV)
Ta_2O_5 Device 1	−33.08	-1.45×10^8	0.9915	0.02
Ta_2O_5 Device 2	−29.84	-6.85×10^7	0.9920	$0.013 \approx 0.01$
Ta_2O_5 Device 3	−29.31	-1.20×10^8	0.9873	$0.018 \approx 0.02$
Ta_2O_5 Device 4	−27.33	-2.15×10^8	0.9985	$0.027 \approx 0.03$
Ta_2O_5 Device 5	−23.39	-6.37×10^8	0.9985	$0.056 \approx 0.06$

5.2.4.2 *Poole-Frenkel emission*

PF emission involves a mechanism of the thermal excitation of electrons which may emit from traps into the conduction band of the dielectric. Considering an electron in a trapping centre, the Coulomb potential energy of the electron can be reduced by an applied electric field across the dielectric film. The reduction in potential energy may increase the probability of an electron being thermally excited out of the trap into the conduction band of the dielectric. The current is ‘limited’ by the ability of carriers to make their way through the bulk of the oxide rather than the ability to tunnel through

a barrier: hence ‘bulk-limited’ conduction. For a coulombic attraction potential between electron and traps, the current density due to PF emission can be expressed by Equation (2.17) discussed in Chapter 2.

For PF emission, a plot log (J/E) versus $E^{1/2}$ should be linear as shown in Equation (2.17), where the trap barrier height can be extracted from the intercept of the PF plot and the dynamic dielectric constant ε_r can be determined from the slope of PF plot as expressed in Equation (2.18). For GaN-based MIS-capacitor with ZrO_2, the plot of log (J/E) versus $E^{1/2}$ is linear in two regions, indicating presence of PF emission over an electric field range of $3 \times 10^3 - 6 \times 10^3$ $(V/m)^{1/2}$ and $1 \times 10^4 - 1.2 \times 10^4$ $(V/m)^{1/2}$ as shown in Figure 5.36. Moreover, the plot of log (J/E) versus $E^{1/2}$ is found to be linear at an electric field range between $3.2 \times 10^3 - 6 \times 10^3$ $(V/m)^{1/2}$ for GaN-based MIS-capacitor with Al_2O_3 as shown in Figure 5.37. Furthermore, Figure 5.38 shows that the plot of log (J/E) versus $E^{1/2}$ is found to be linear at an electric field range between $5.8 \times 10^3 - 1.1 \times 10^4$ $(V/m)^{1/2}$ for GaN-based MIS-capacitor with MgO, whereas GaN-based MIS-capacitor with Ta_2O_5 shows linear plot of log (J/E) versus $E^{1/2}$ in two regions, at electric field range of $2.7 \times 10^3 - 6 \times 10^3$ $(V/m)^{1/2}$ and $8.5 \times 10^3 - 1.1 \times 10^4$ $(V/m)^{1/2}$ as shown in Figure 5.39.

A comparison of slopes and intercepts found from PF plots, as well as extracted dynamic permittivity ε_r values for all investigated GaN-based MIS-capacitors with different oxides: ZrO_2, Al_2O_3, MgO, and Ta_2O_5 at room temperature are listed in Table 5.8. Our extracted values of ε_r for different studied oxides: ZrO_2, Al_2O_3, MgO, and Ta_2O_5 are very large and indicate that PF emission is not the governing conduction mechanism in these samples.

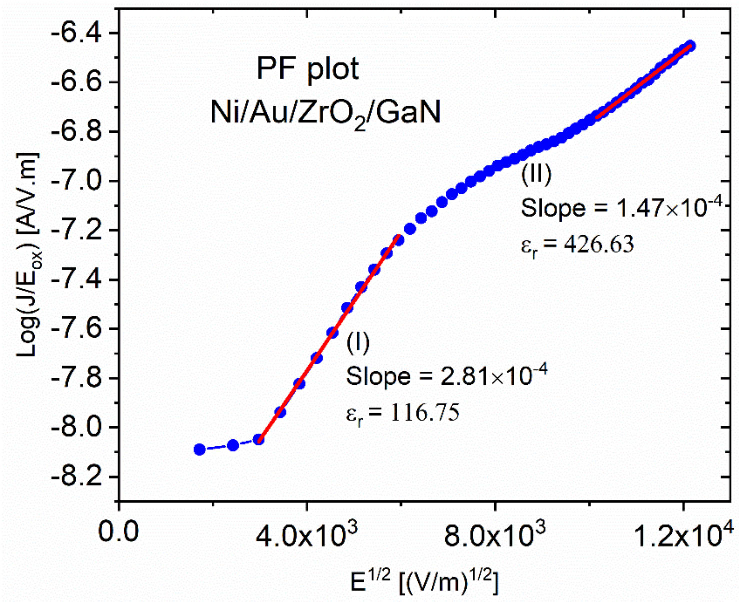

Figure 5.36: PF plot for GaN MIS-capacitor with ZrO_2 as a dielectric layer.

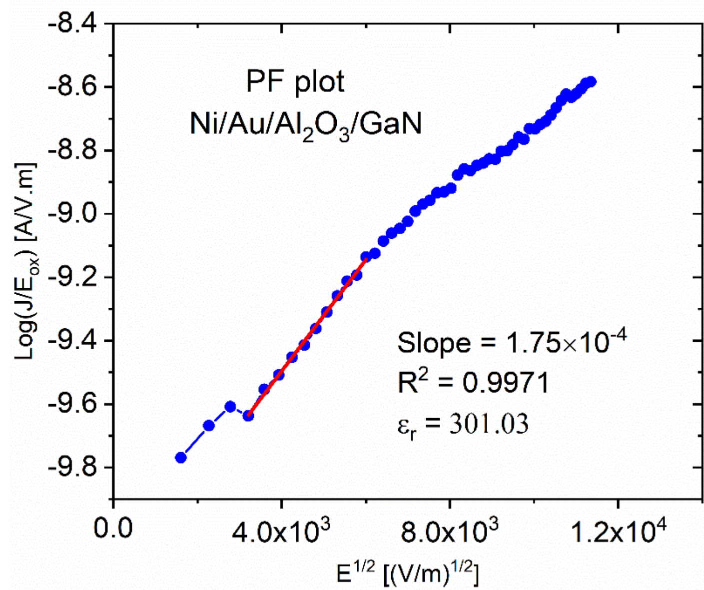

Figure 5.37: PF plot for GaN MIS-capacitor with Al_2O_3 as a dielectric layer.

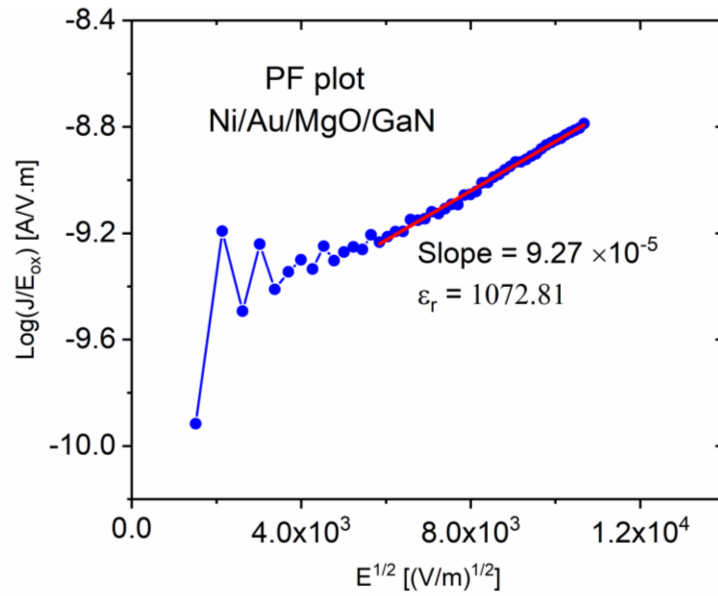

Figure 5.38: PF plot for GaN MIS-capacitor with MgO as a dielectric layer.

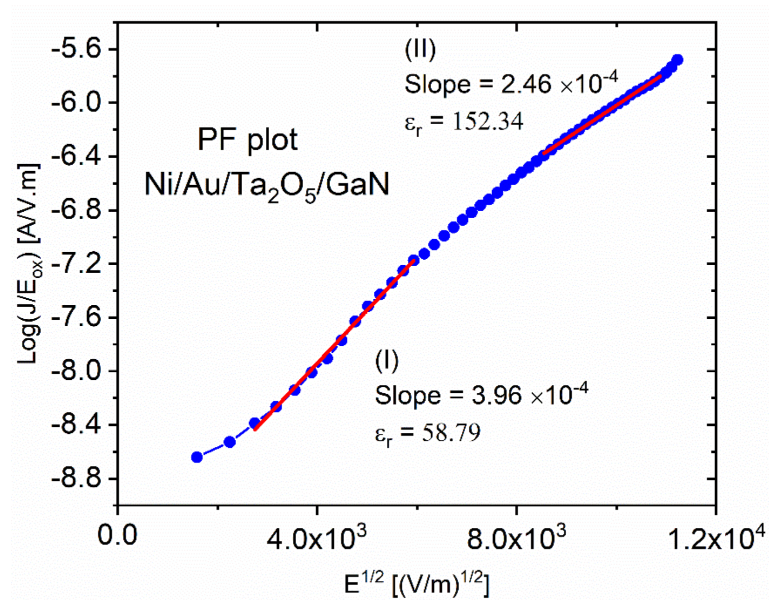

Figure 5.39: PF plot for GaN MIS-capacitor with Ta_2O_5 as a dielectric layer.

Table 5.8: The slope and intercept of the linear fitting of PF plots and the extracted dynamic dielectric constant for oxide/GaN samples.

Oxide	Intercept	Slope	R^2	ε_r
ZrO_2	−8.89	2.81×10^{-4}	0.9984	116.75
	−8.24	1.47×10^{-4}	0.9984	426.63
Al_2O_3	−10.2	1.75×10^{-4}	0.9971	301.03
MgO	−9.78	9.27×10^{-5}	0.9957	1072.81
Ta_2O_5	−9.52	3.96×10^{-4}	0.9964	58.79
	−8.48	2.46×10^{-4}	0.9983	152.34

5.2.4.3 *Space-charge-limited current*

The JV characteristic in the Log(J)-Log(V) plane is bounded by three limited curves if followed by SCLC mechanism, namely ohm's law ($J_{Ohm} \propto V$), traps-filled limit (TFL) current ($J_{TFL} \propto V^2$), and Child's law ($J_{Child} \propto V^2$) as discussed in Chapter 2. The SCLC plots at room temperature for different oxides are shown in Figures 5.40, 5.41, 5.42, and 5.43 corresponding to ZrO_2, Al_2O_3, MgO, and Ta_2O_5 GaN-based MIS devices, respectively.

For ZrO_2 GaN-based MIS device, the Log(J)-Log(V) plot (Figure 5.14) shows three different regions: region (I) in the very low applied voltage at a range of 0.05 − 0.15 V, the slope is equal about unity ($J \approx V^{1.08}$) corresponding to the ohmic region; region (II) in the voltage range of 0.2 − 0.72 V, the slope is found to be 2.5 ($J \approx V^{2.5}$) corresponding to TFL law because the slope is larger than two [309]; region (III) in a voltage range of 1 – 2 V, the slope is equal about two ($J \approx V^{2.04}$) corresponding to Child's law or the trap free SCLC region. Moreover, the Log(J)-Log(V) plot (Figure 5.41) for Al_2O_3 GaN-based MOS device shows three different regions too: region (I) in the very low applied voltage at a range of 0.05 − 0.15 V the slope is equal about

unity ($J \approx V^{1.34}$) corresponding to the ohmic region; region (II) in the voltage range of 0.2 − 0.6 V the slope is found to be 1.87 ($J \approx V^{1.87}$) hence, not satisfying the TFL law; region (III) in a voltage range of 1.3 – 2.4 V, the slope is equal about two ($J \approx V^{2.08}$) corresponding to the trap free SCLC region. For GaN-based MOS-capacitor with MgO as dielectric layer, no Ohmic and TFL regions have been observed as the slopes of JV plot for regions (I) ($J \approx V^{3.41}$) and (II) ($J \approx V^{1.36}$) do not satisfy these laws, however for region (III) at higher voltages of 1.2 – 2.5 V the slope is equal about two ($J \approx V^{2.01}$) which represents the trap free SCLC (Figure 5.42). For Ta_2O_5 GaN-based MOS device, the Log(*J*)-Log(*V*) plot (Figure 5.43) shows that the slopes of regions (I) ($J \approx V^{1.51}$) and (III) ($J \approx V^{3.71}$) do not satisfy the Ohmic and trap free SCLC, however region (III) in the applied voltage range of 0.2 – 0.4 V shows the slope to be greater than two ($J \approx V^{2.63}$) corresponding to the TFL conduction.

Therefore, from the conduction mechanisms analysis using typical *JV* characteristics plotted on log-log scales, there is evidence of SCLC mechanism in the low electric field region (0-1.5 V) which would indicate that the current flow is inhomogeneous and bulk rather than electrode limited. It is not possible therefore, to extract barrier heights which might be compared to those derived from XPS.

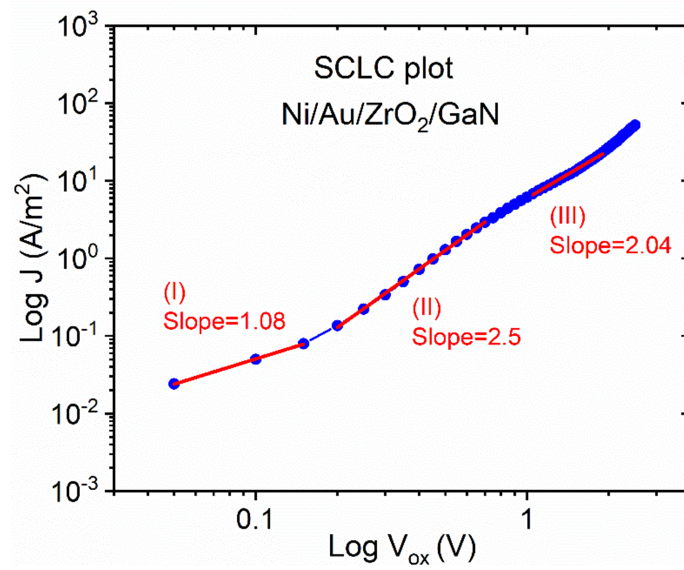

Figure 5.40: SCLC plot for GaN MIS-capacitor with ZrO_2 as a dielectric layer.

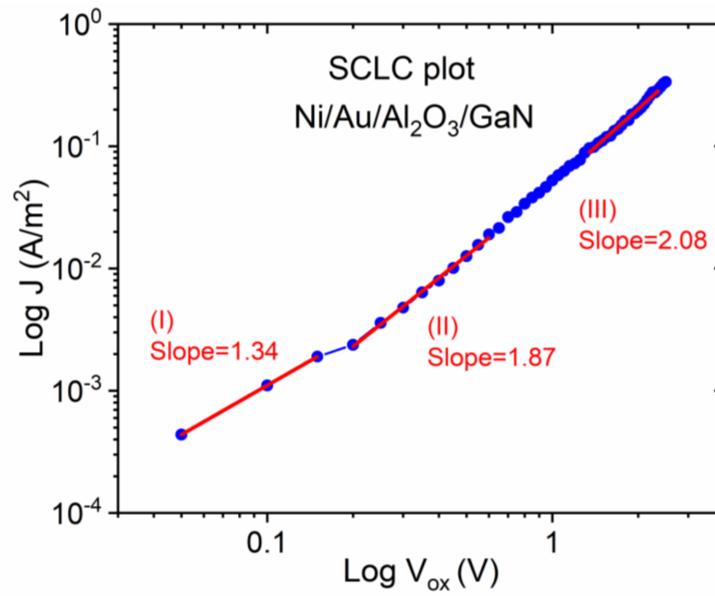

Figure 5.41: SCLC plot for GaN MIS-capacitor with Al_2O_3 as a dielectric layer.

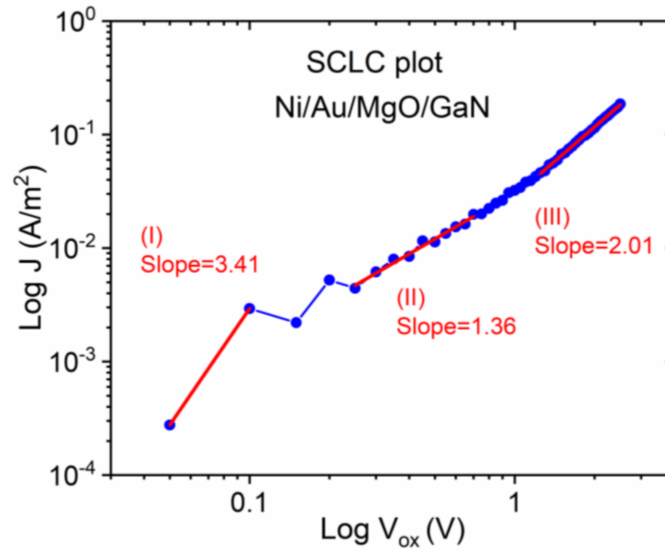

Figure 5.42: SCLC plot for GaN MIS-capacitor with MgO as a dielectric layer.

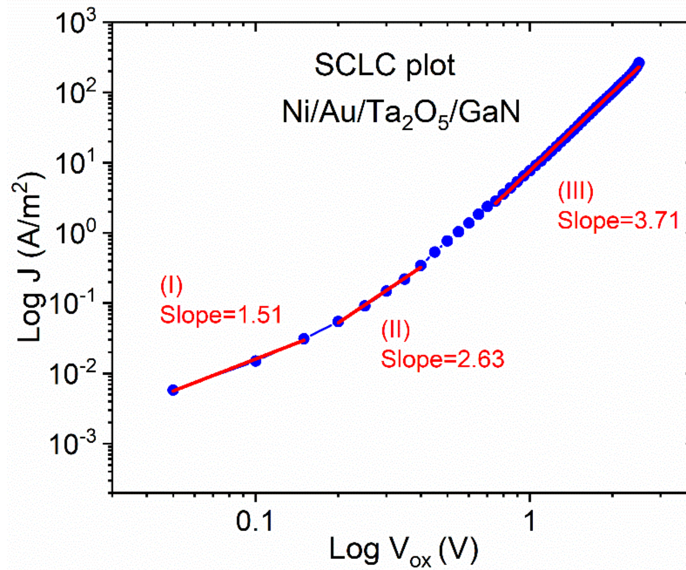

Figure 5.43: SCLC plot for GaN MIS-capacitor with Ta_2O_5 as a dielectric layer.

5.2.5 CV measurements

The capacitance-voltage (*CV*) measurements were performed using Agilent LCR meter E4980A system. The *CV* curve was obtained with a gate voltage swept from accumulation to inversion region at room temperature. The charge configuration inside the MOS device during accumulation is analogous to that of a parallel plate capacitor that gives capacitance as expressed in Equation (5.1) [182]:

$$C_{accumulation} \approx C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{t_{ox}}, \quad (5.1)$$

where ε_o is the vacuum permittivity, ε_{ox} is the oxide permittivity, t_{ox} is the oxide thickness, and A is the gate area.

The *CV* plot for Al_2O_3 GaN-based MOS device showed a large frequency dispersion at accumulation region (Figure 5.44 (a)) as frequency increased from 1 kHz to 1 MHz. At a frequency of 1 MHz, the maximum capacitance at accumulation region is 1.83×10^{-3} F/m^2. Therefore, the extracted ε_{ox} using Equation (5.1) is found to be 4, which is small compared to the reported values of ~9-10 [304].

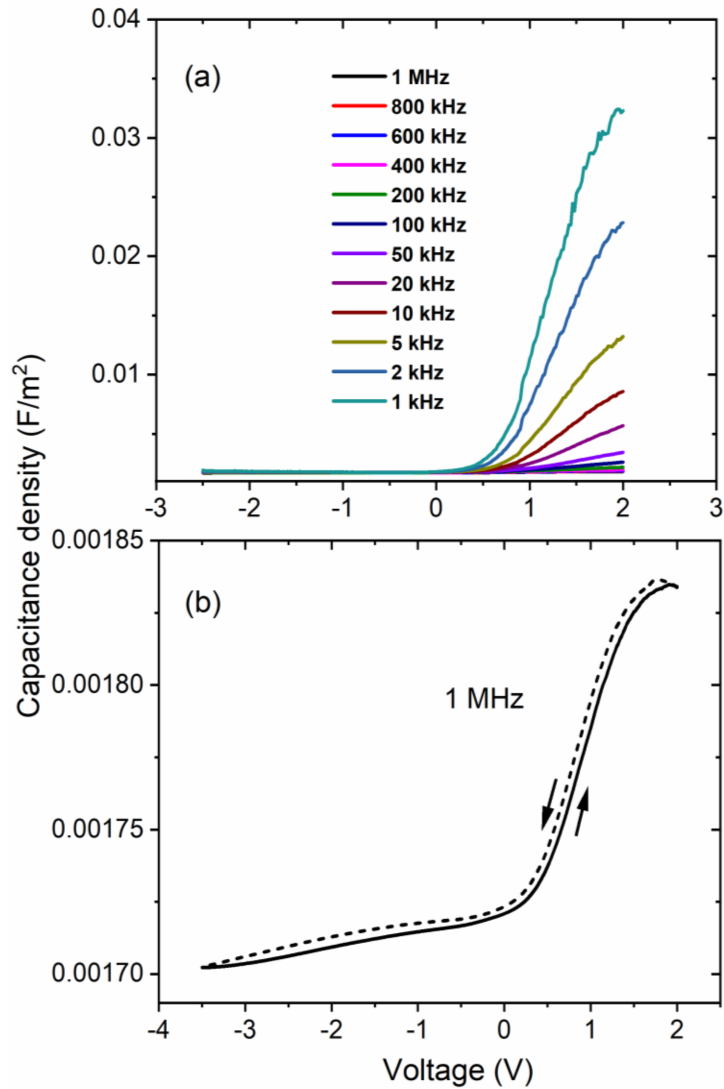

Figure 5.44: The *CV* plot: (a) frequency dependent and (b) hysteresis at a frequency of 1 MHz for GaN MIS-capacitor with Al_2O_3 as a dielectric layer.

Furthermore, the *CV* plots at room temperature for GaN-based MOS devices with ZrO_2 (Figure 5.45 (a)), MgO (Figure 5.46 (a)) and Ta_2O_5 (Figure 5.47 (a)) show a large frequency dispersion, where no accumulation and inversion regions were observed as frequency increased from 1 kHz to 1 MHz. These measured *CV* curves showed a slight kink, which could be due to deep depletion behaviour for negative bias voltage. The deep depletion feature with no inversion capacitance characteristics is typical of wide-gap semiconductor MIS structures due to the slow generation rate of the minority carriers at room temperature. The hysteresis is observed for both sweep

directions; one is from negative to positive voltage and vice versa. The hysteresis in the *CV* plots swept to the left-hand side could be due to mobile charges in the oxides for GaN-based MOS devices with: Al_2O_3 (Figure 5.44 (b)), ZrO_2 (Figure 5.45 (b)) and MgO (Figure 5.46 (b)). As a large positive bias is applied, these positive mobile charges are pushed to the oxide-semiconductor interface and effectively increase the capacitance measured. On the reverse bias, a negative voltage attracts these positive mobile charges towards the metal-oxide interface, and they do not have an effect on the capacitance. The hysteresis in the *CV* plots swept to the right-hand side for GaN-based MOS device with Ta_2O_5 (Figure 5.47 (b)) is likely to be due to the slow-trapping effect.

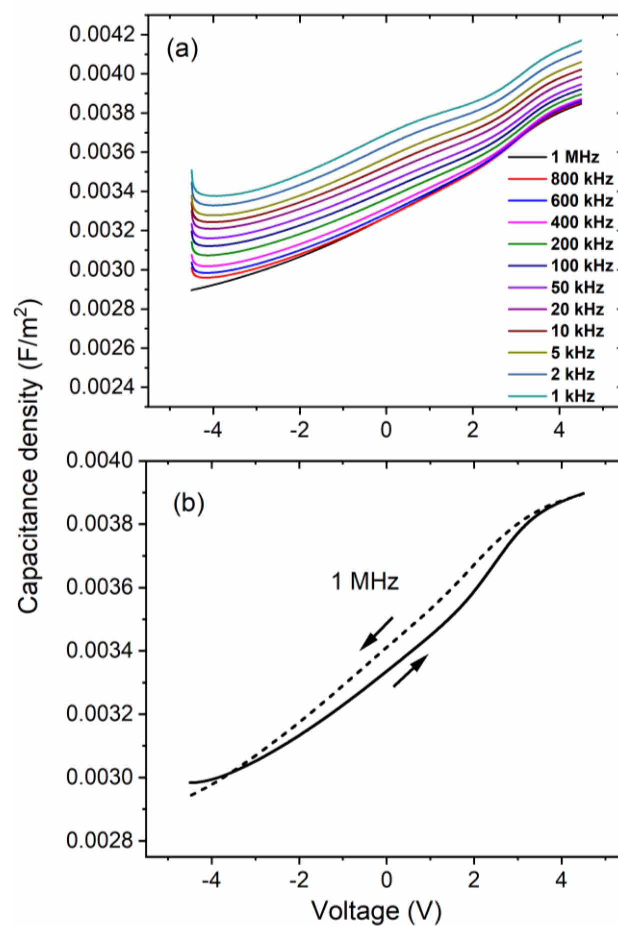

Figure 5.45: The *CV* plots: (a) frequency dependent and (b) hysteresis at frequency 1 MHz for GaN MIS-capacitor with ZrO_2 as a dielectric layer.

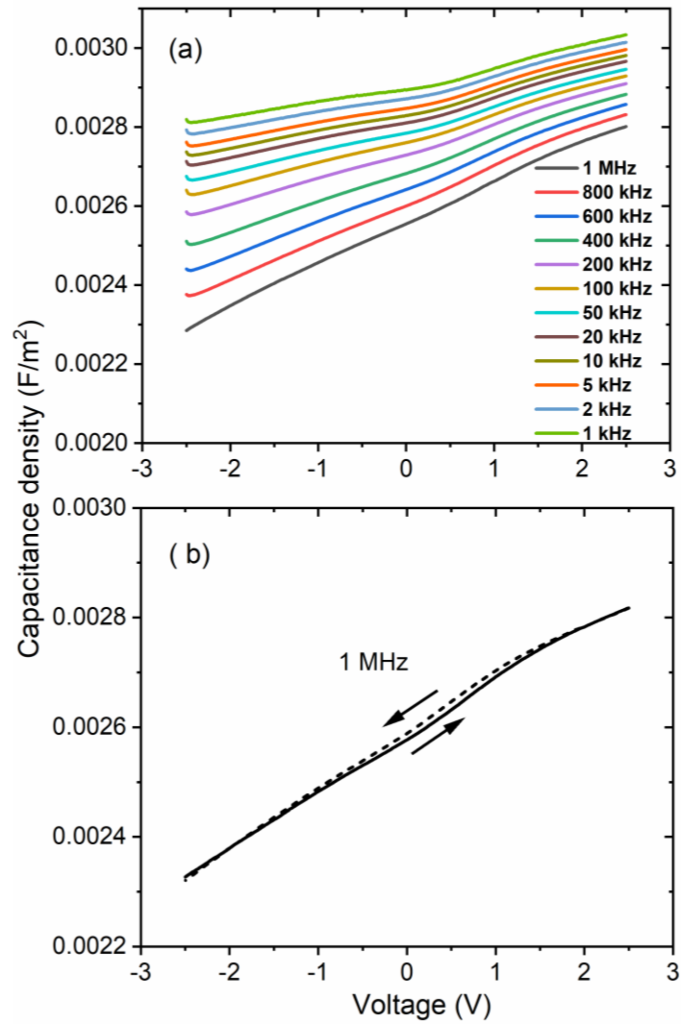

Figure 5.46: The *CV* plots: (a) frequency dependent and (b) hysteresis at frequency 1 MHz for GaN MIS-capacitor with MgO as a dielectric layer.

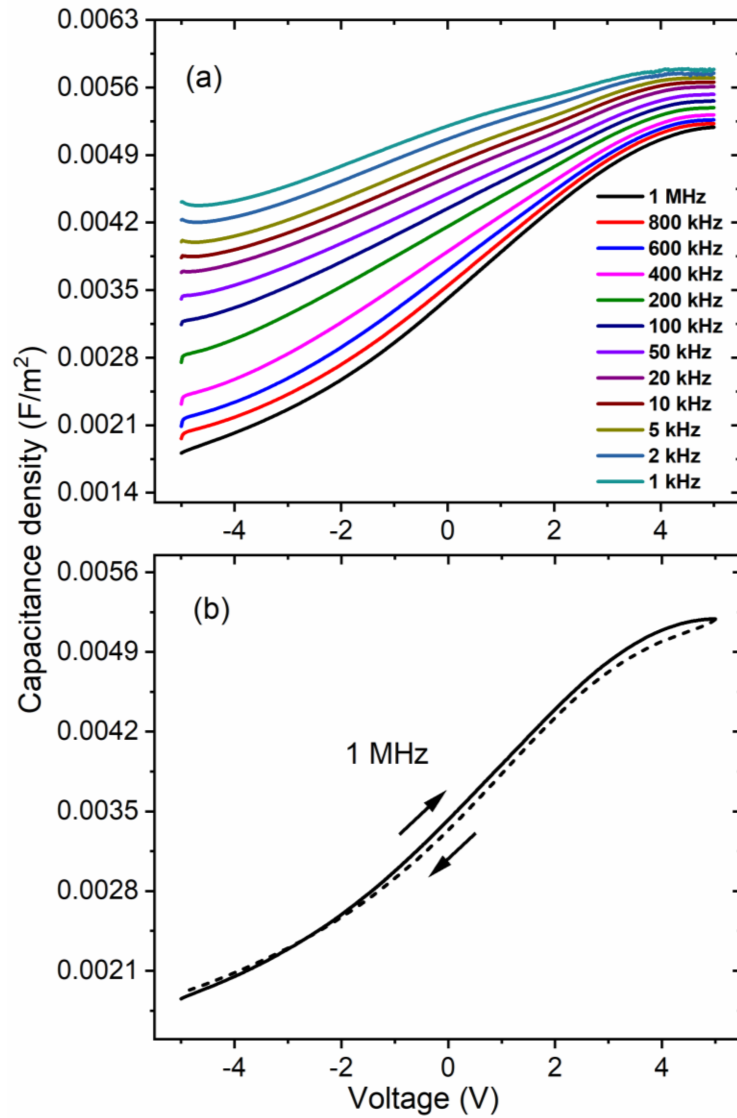

Figure 5.47: The *CV* plots: (a) frequency dependent and (b) hysteresis at frequency 1 MHz for GaN MOS-capacitor with Ta_2O_5 as a dielectric layer.

5.3 Al_2O_3-based MIS-HEMTs

5.3.1 Device fabrication

Yutao Cai and Miao Ciu from Xi'an Jiaotong-Liverpool University (XJTLU), China are acknowledged for their contribution in the fabrication and several measurements of GaN HEMT and MIS-HEMT devices. In this work, several GaN-based devices including the conventional HEMT without gate dielectric, D-mode and E-mode AlGaN/GaN MIS-HEMTs, with and without GaN cap layer as well as MIS-

capacitors (or MOS-capacitors) were fabricated at XJTLU, China. Table 5.4 shows the list of all fabricated samples.

Table 5.9: List of fabricated HEMT devices.

Sample	Transistor	D-mode (recess cycles)	E-mode (recess cycles)	ALD Al_2O_3 Thickness (nm)
A	HEMT (without Al_2O_3)	−	45×	−
B	MIS-HEMT (with Al_2O_3)	−	40×	15
C	MIS-HEMT (with Al_2O_3)	−	45×	15
D	MIS-HEMT (with Al_2O_3 & without GaN cap layer)	5×	50×	15
E	Non-treated MIS-HEMT (with Al_2O_3 & with GaN cap layer)	3×	−	20
F	HCl treated MIS-HEMT (with Al_2O_3 & with GaN cap layer)	3×	−	20
G	O_2 plasma treated MIS-HEMT (with Al_2O_3 & with GaN cap layer)	3×	−	20
H	ODT treated MIS-HEMT (with Al_2O_3 & with GaN cap layer)	3×	−	20

5.3.1.1 *Fabrication process of HEMTs and MIS-HEMTs (D-mode and E-mode)*

The epitaxial layer structure of AlGaN/GaN devices as shown in Figure 5.48 (a) consists of a 4 µm GaN buffer on a Si substrate, a 0.4 µm AlN spacer, 23 nm $Al_{0.25}Ga_{0.75}N$ barrier and a 3 nm GaN cap layer except for samples D, where the GaN cap layer were etched to remove the GaN cap layer. The main steps involved in the process flow of fabricating D-mode and E-mode devices are summarised in Figure 5.48 (b). The fabrication of both D-mode and E-mode devices started with mesa etching using BCl_3/Cl_2 and followed by the formation of Au-free source and drain ohmic contacts by e-beam evaporation of Ti/Al/Ni/Au with thicknesses of

25/125/45/55 nm, respectively. The surface treatment is performed for all samples to remove any native oxides prior to dielectric deposition by immersing in acetone, isopropanol, 1:10 HCl: H_2O for 5 min sequentially and then rinsed with deionised water. The sample was then undergone rapid thermal annealing (RTA) at 800 °C for 45 seconds in N_2 ambient. Then, a 300 nm of SiN_x was deposited by plasma enhanced chemical vapour deposition (PECVD) as etching hard mask for the E-mode gate recess. Next step, the GaN surface was treated by O_2 plasma by digital etching for 3 min at a temperature of 60 °C with an RF power of 100 W. The oxidation layer was removed by wet etching in 1:10 HCl for 1 min, after 40 cycles of digital etching. Table 5.4 shows the number of etching cycles for D-mode and E-mode devices. The difference between samples B and C is the number of etching cycles for E-mode device, which is 40 cycles for sample B and 45 cycles for sample C. The deposition of 15 nm Al_2O_3 gate dielectric for E-mode and D-mode devices was performed by atomic layer deposition (ALD) technique with Trimethyl aluminium (TMA) as a precursor and H_2O as an oxidant source. For comparison purposes, HEMT without Al_2O_3 as dielectric layer (Sample A) has been fabricated as well. The final step was followed by depositing the gate electrode Ni/TiN as the gate metal.

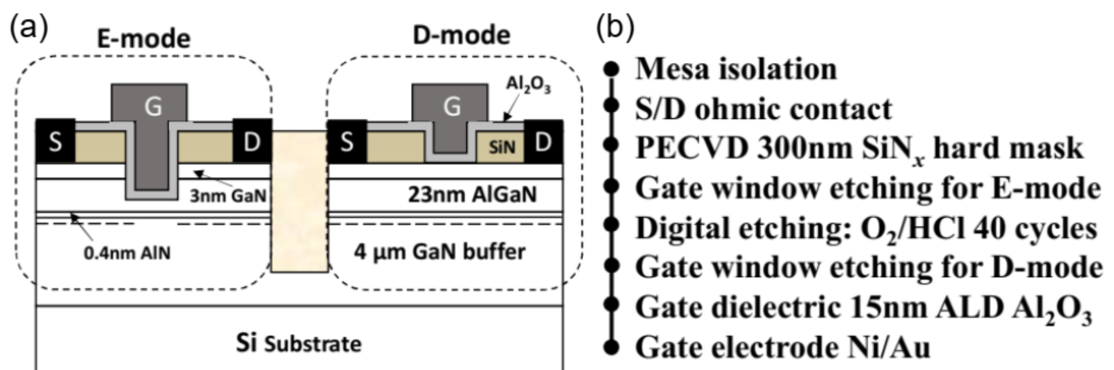

Figure 5.48 (a) The schematic structure and (b) fabrication steps of E- and D-mode MIS-HEMTs.

5.3.1.2 *Fabrication of Al_2O_3-MIS-HEMTs with different surface treatments (without, HCl, O_2 plasma and ODT)*

The cross-sectional view of the fabricated GaN-based MIS-HEMT device is shown in Figure 5.49. The investigated GaN-based material stack consists of a 1 nm undoped GaN cap layer, a 22 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer, a 0.33 µm GaN channel layer, and a 5.4 µm highly resistive buffer on a 1 mm Si substrate. Firstly, the Au-free source and drain were formed by e-beam evaporation of Ti/Al/Ti/TiN (25/125/45/55 nm) patterned by a photolithography and a lift-off process and annealed at 840 °C in N_2 ambient for 40 s by RTA. After the formation of ohmic contact, the mesa isolation region was formed by BCl_3/Cl_2 gas reactive ion etching. After the organic cleaning processes, sample E was without any treatment. Then, the sample F, G and H were treated in 2M HCl solution at room temperature for 5 min to remove the native oxide. In addition, sample G was subjected to O_2 plasma in a reactive ion plasma system with a low RF power of 50 W and an O_2 flow of 50 sccm for 3 min. The sample H was immersed in a 5 mM 1-Octadecanethiol (ODT) in ethanol at RT for 24 hours to passivate the GaN surface. After the ODT exposure, the sample H was immersed in ethanol and ultrasonically cleaned for 10 min followed by N_2 drying. Furthermore, before the ALD, the sample H was exposed to 30 H_2O pulses with the same pulse/purge duration as used in the ALD process at 260 °C in the ALD reactor, to in-situ cleave the S-C bonds of ODT self-assembled monolayer (SAM). The Al_2O_3 films with a nominal thickness of 20 nm were grown by ALD with TMA as the precursor and H_2O as the oxidant source. The 180 ALD cycles were run at 260 ºC at a chamber pressure of ~50 Pa. High purity N_2 (20 sccm) was used as the precursor carrier and purge gas. After local Al_2O_3 removal with 1% HF, another photolithography process was used to define Ni/TiN (50/100 nm) gate electrodes.

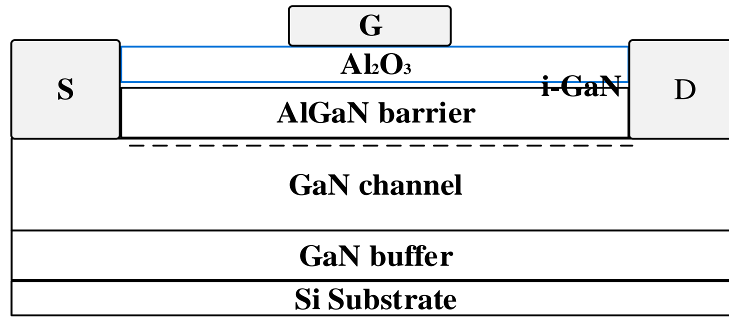

Figure 5.49: Schematic cross-sectional view of the fabricated MIS-HEMT without GaN cap layer.

Figure 5.50 shows the schematic of the chemical composition on the GaN surface during the ODT treatment. Firstly, the wet chemical etching in 2M HCl is used to remove the native oxide on GaN wafer (Figure 5.50 (a)). Secondly, by immersing the wafer in the ODT solution at RT for 24 hours, the GaN surface is left with the ODT SAM (Figure 5.50 (b)). The presence of chemisorbed Ga-S bonds on the GaN surface depicted in the schematic in Figure 5.50 (c) can be proven by the XPS Ga-S sub-peak shown in Figure 5.51 (d). Thirdly, the exposure of the surface to H_2O vapour at 260 °C in the ALD reactor led to removal of the alkane chain of the ODT SAM. This alkane chain reduction may be attributed to the thermal cleavage of S-C bonds [299]. Finally, the Ga-S bonds on the GaN surface act as a barrier to suppress the Ga-O bond formation during the subsequent Al_2O_3 deposition (Figure 5.50 (d)), which could result in a high quality interface between ALD-Al_2O_3 and GaN-cap.

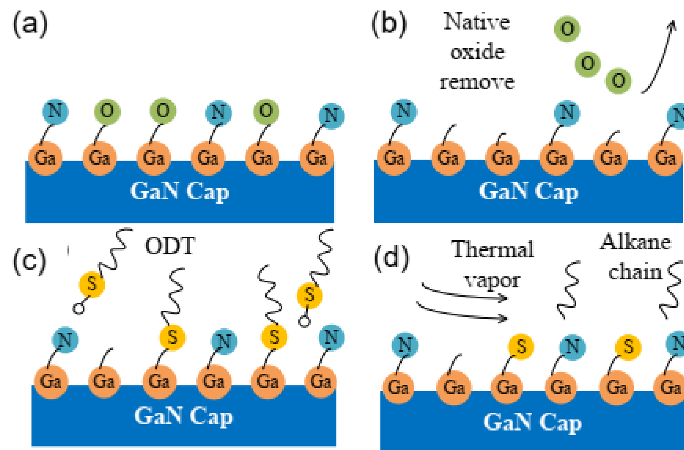

Figure 5.50: Schematic of the ODT treatment procedure: (a) the non-treated GaN cap; (b) the HCl treatment for removal of the native oxide; (c) the formation of a dense ODT SAM on the HCl-cleaned GaN surface; (d) the in vacuo thermal vapour removal of the carbon chain, leaving sulphur atoms behind [310].

5.3.2 XPS measurements of Al_2O_3/AlGaN/GaN with different GaN surface treatments

The XPS analysis has been performed to investigate the chemical composition variation on the GaN surface induced by different surface treatments: without treatment (sample E), HCl treatment (sample F), O_2 plasma treatment (sample G), and ODT treatment (sample H). Figure 5.51 shows the deconvoluted XPS Ga 3d core level (CL) spectra for these samples. The Ga 3d CL can be deconvoluted into two main components corresponding to Ga-N bond in the substrate at the binding energy (BE) of 19.7 eV and Ga-O bond at higher BE of 20.4 eV.

The Ga 3d spectrum of the non-treated sample in Figure 5.51 (a) exhibits a high Ga-O sub-peak which indicates the existence of amorphous native oxide at the Al_2O_3/GaN interface. The HCl surface treatment has been reported to effectively remove the native oxide on the GaN surface [311]. However, it can be seen from Figures 5.51 (a) and (b) that the intensity of Ga-N and Ga-O bonds is very similar for both E and F samples. The possible reason for this could be the exposure to air of the

HCl-treated GaN sample prior the ALD process, and the reoxidation could have occurred during this interval.

Moreover, the Ga 3d centroid peak of the O_2 plasma treated sample as shown in Figure 5.51 (c) is shifted to a higher BE for 0.2 eV in comparison to the non-treated sample. In this case, a broader centroid peak is visible with a larger fitted Ga-O subpeak. This is mainly due to the GaN-cap layer being oxidised and GaO_x formed on the surface [301]. Hence, it can be deduced that the O_2 plasma treatment effectively filled the N vacancies with oxygen atoms, where carrier trapping could be induced. In addition, we also notice a phenomenon that the O_2 plasma treatment has removed the carbon contamination on the GaN surface, which corresponds to a lower C/N ratio of 1.1 as compared to the value of 1.6 for the non-treated sample.

The Ga 3d CL spectrum of the ODT treated sample in Figure 5.51 (d) shows a slightly higher BE of the centroid peak than that of the non-treated sample. The fitted Ga-O sub-peak component appears to be reduced indicating the amount of oxide on the GaN surface has been decreased. There is an extra deconvoluted sub-peak in the Ga 3d CL spectrum at the BE of 20.6 eV, which corresponds to the bond formation between gallium and sulphur atoms [297]. This suggests that the ODT treatment can suppress the oxidation of the GaN surface by forming Ga-S bonds before the subsequent Al_2O_3 deposition. Furthermore, the Ga-S bonds remained at the surface after exposure to thermal H_2O vapour pulses during ALD. This indicates that the Ga-S bonds are thermally stable at least up to 260 °C, in agreement with previous studies [312], where it has been stated that the Ga-S bonds remain stable up to 400 °C. In summary, it can be deduced from the XPS study that the ODT self-assembled monolayer can provide good passivation of the GaN surface even during a high

temperature fabrication process, and this feature could allow integration of the ODT treatment into the MOSFET process flow.

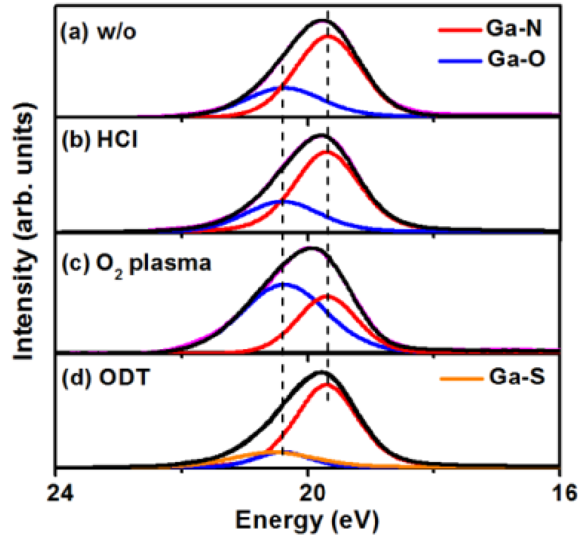

Figure 5.51: The XPS Ga 3d CL spectra for GaN samples: (a) A-without treatment; (b) B-with the HCl; (c) C-with the O_2 plasma; (d) D-with the ODT for 24 hours surface treatments [310].

5.3.3 Electrical measurements

5.3.3.1 *AlGaN/GaN HEMTs and capacitors*

The *IV* measurements were performed using an Agilent B1500 semiconductor device analyser, whereas the *CV* measurements were performed using Agilent LCR meter E4980A systems. Figure 5.52 shows the output and transfer characteristics of D-mode AlGaN/GaN HEMT for sample A. For drain current (I_D) against drain voltage (V_{DS}) measurement, the drain voltage is measured from 0 V to 10 V with a step of 0.1 V and the measurement gate voltage (V_{GS}) is swept from -8 V to 2 V. Whereas, for I_D against V_{GS} measurement, the V_{GS} is varied from -8 V to 0 V ith a step of 0.1 V. It can be seen that the maximum output drain current I_{Dmax} for D-mode HEMT is found to be 0.46 A/mm at 2 V (Figure 5.52 (a)), whereas the threshold voltage V_T is -4.1 V at 1

mA/mm (Figure 5.52 (b)). For HEMT, the reverse leakage current is around 1 mA/mm (Figure 5.52 (b)). The insertion of Al_2O_3 dielectric can reduce the leakage current as observed in sample C (Figure 5.55 (b)). The subthreshold slope (*SS*) was found to be 326 mV/dec for sample A.

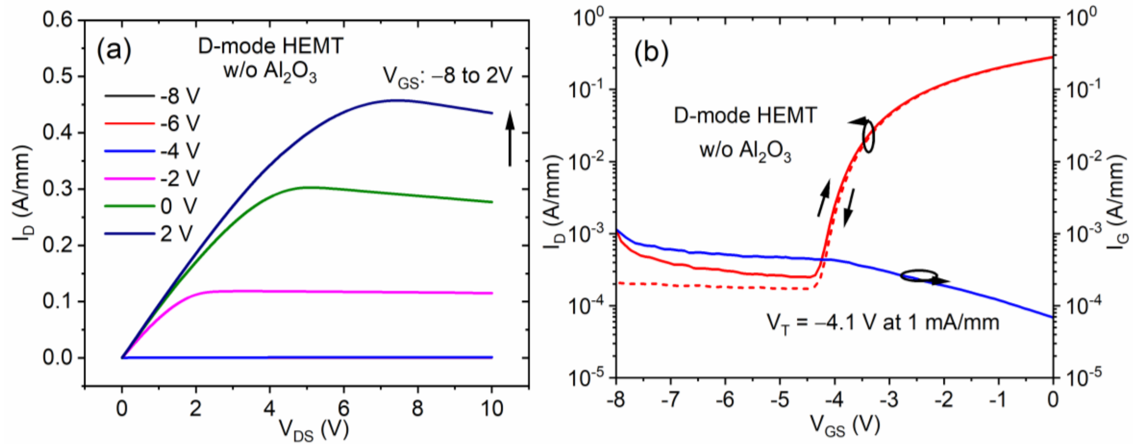

Figure 5.52: (a) Output characteristics and (b) transfer characteristics of D-mode HEMT for sample A. Device dimension: $L_{GS}/W_{GS}/L_G/L_{GD}$ = 5/50/3/10 µm.

Figure 5.53 shows the *CV* curves for sample A for D-mode capacitor where the measurement voltage was swept from -5 to 0.5 V with a step of 20 mV, and the frequency was varied from 1 MHz down to 1 kHz. The D-mode *CV* curve shows high noise at low frequency which might be caused by high leakage current since there is no Al_2O_3 dielectric layer.

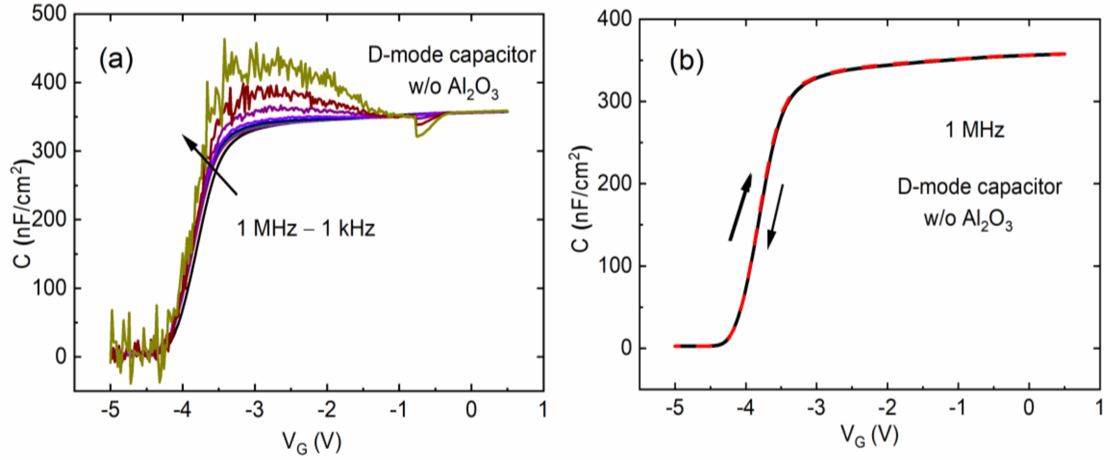

Figure 5.53: *CV* curves for D-mode capacitor for sample A: (a) frequency dependent, (b) hysteresis at 1 MHz.

5.3.3.2 *D-mode and E-mode MIS-HEMTs and MIS-capacitors with Al_2O_3 as gate dielectric*

Figure 5.54 shows the output and transfer characteristics of D-mode AlGaN/GaN MIS-HEMT with Al_2O_3 for sample B. For I_D versus V_{DS} measurement, the V_{DS} is measured from 0 V to 10 V with a step of 0.1 V and the V_{GS} is swept from -13 V to 5 V. Whereas, for I_D against V_{GS} measurement, the V_{GS} is varied from -13 V to 5 V with a step of 0.1 V. The I_{Dmax} is 0.62 A/mm at 5 V (Figure 5.54 (a)) and the V_T is found to be -11.3 V from linear extrapolation of *IV* curve (Figure 5.54 (b). For this device, the high leakage current is due to the problem in fabrication process. sample B is also found to have very large subthreshold slope of 1700 mV/dec.

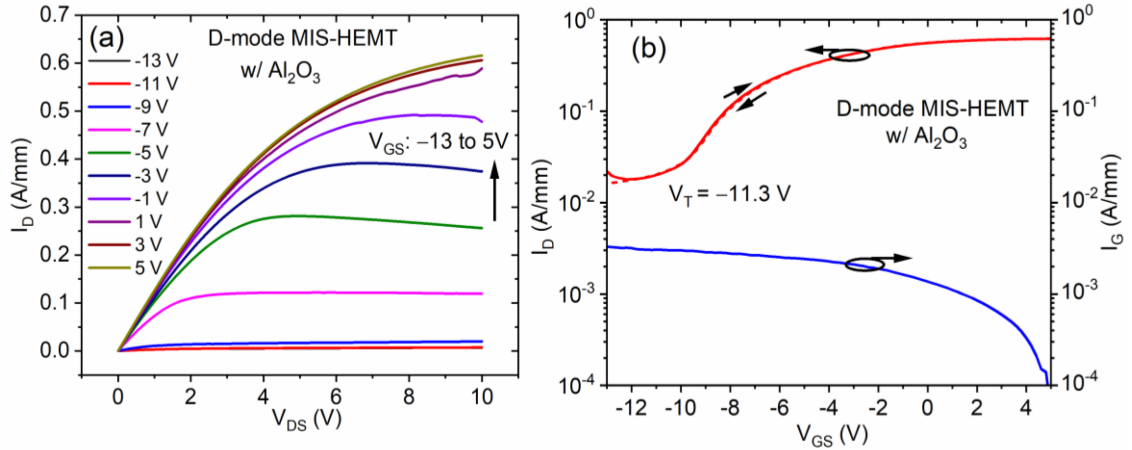

Figure 5.54: (a) Output characteristics and (b) transfer characteristics of D-mode MIS-HEMT for sample B. Device dimension: $L_{GS}/W_{GS}/L_G/L_{GD}$ = 5/100/3/5 µm.

Figure 5.54 shows the output and transfer characteristics of D-mode AlGaN/GaN MIS-HEMT for sample C. For I_D versus V_{DS} measurement, the V_{DS} is measured from 0 V to 10 V with a step of 0.1 V and the V_{GS} is swept from -13 V to 5 V. Whereas, for I_D against V_{GS} measurement, the V_{GS} is varied from -13 V to 5 V with a step of 0.1 V. The I_{Dmax} is 0.41 A/mm at 5 V (Figure 5.55 (a)) and the V_T is -6.9 V at 1 µA/mm (Figure 5.55 (b)). The V_T hysteresis is very small, = 50 mV. The leakage current is very small, less than 1 nA/mm. A relative positive V_T (-6.9 V) indicates reduced positive charges at the Al_2O_3/GaN interface. The subthreshold slope was found to be 139 mV/dec for sample C. A small V_T hysteresis and subthreshold slope indicate a high quality Al_2O_3/GaN interface. On the other hand, for E-mode MIS-HEMT as shown in Figure 5.56, for I_D versus V_{DS} measurement, the V_{DS} is measured from 0 V to 10 V with a step of 0.1 V and the V_{GS} is swept from -6 V to 6 V. Whereas, for I_D against V_{GS} measurement, the V_{GS} is varied from -6 V to 6 V with a step of 0.1 V. the I_{Dmax} is 0.06 A/mm at 6 V (Figure 5.56 (a)) and the V_T is 2.9 V at 1 µA/mm (Figure 5.56 (b)). The surface leakage current is suppressed, and the vertical leakage current plays a major role. The off-state leakage current depends on the gate leakage current. A positive V_T (2.9 V) indicates the E-mode operation and the AlGaN barrier

layer is fully recessed (2DEG have been fully removed). A small V_T hysteresis of 50 mV and small subthreshold slope of 80 mV/dec indicate a high quality Al_2O_3/GaN interface.

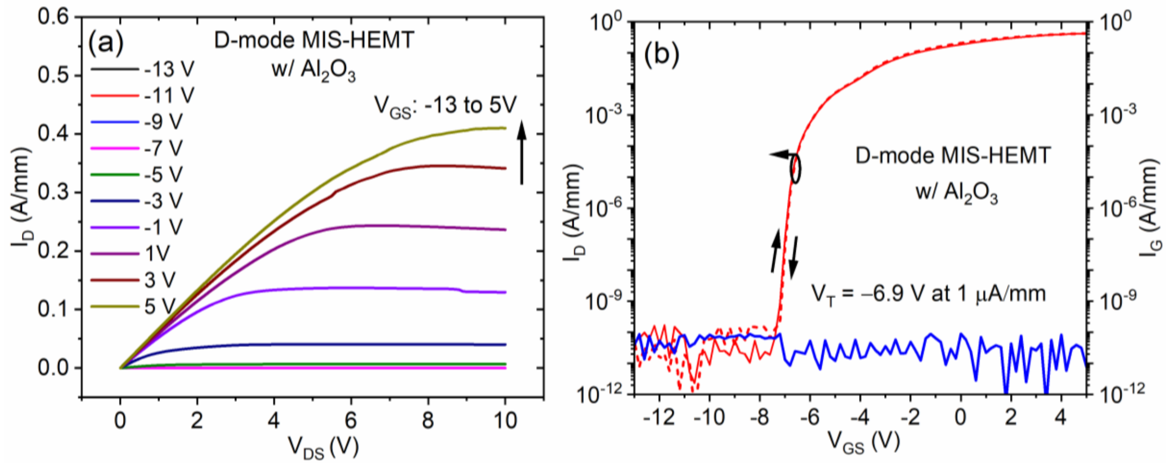

Figure 5.55: (a) Output characteristics and (b) transfer characteristics of D-mode MIS-HEMT for sample C. Device dimension: $L_{GS}/W_{GS}/L_G/L_{GD}$ = 5/100/3/5 µm.

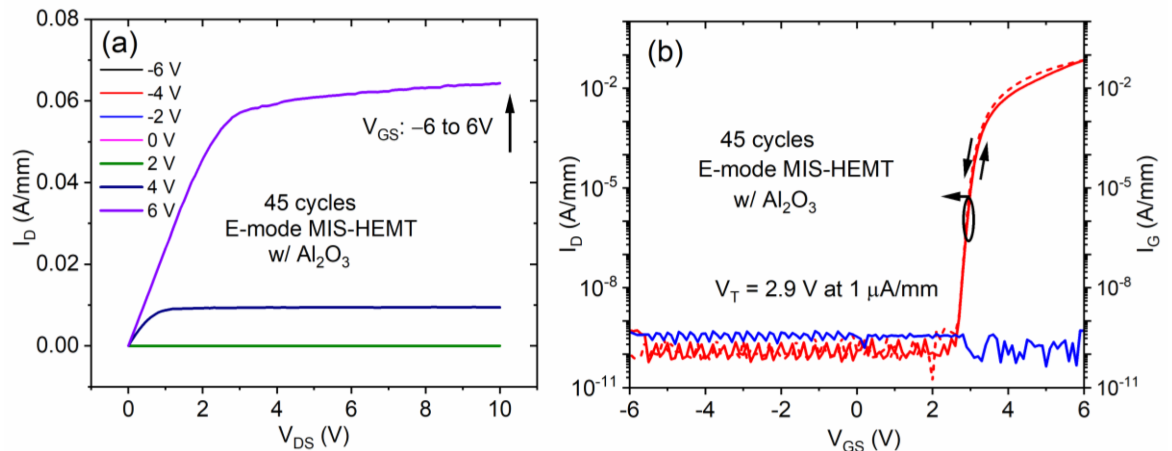

Figure 5.56: (a) Output characteristics and (b) transfer characteristics of E-mode MIS-HEMT for sample C. Device dimension: $L_{GS}/W_{GS}/L_G/L_{GD}$ = 5/50/3/5 µm.

Figure 5.57 shows the output and transfer characteristics of D-mode AlGaN/GaN MIS-HEMT (with Al_2O_3 and without GaN cap layer) for sample D. For I_D versus V_{DS} measurement, the V_{DS} is measured from 0 V to 10 V with a step of 0.1 V and the V_{GS} is swept from -13 V to 5 V. Whereas, for I_D against V_{GS} measurement, the

V_{GS} is varied from -13 V to 5 V with a step of 0.1 V. It has been found that the I_{Dmax} is 0.33 A/mm at 5 V (Figure 5.57 (a)), whereas the V_T is -5.9 V at 1 μA/mm with the V_T hysteresis being very small of 80 mV (Figure 5.57 (b)). The subthreshold slope was found to be 97 mV/dec. The leakage current is very small, around 1 nA/mm. Furthermore, for E-mode MIS-HEMT for sample D as shown in Figure 5.58, for I_D versus V_{DS} measurement, the V_{DS} is measured from 0 V to 10 V with a step of 0.1 V and the V_{GS} is swept from -6 V to 6 V. Whereas, for I_D against V_{GS} measurement, the V_{GS} is varied from -6 V to 6 V with a step of 0.1 V. The I_{Dmax} is 0.03 A/mm at 6 V (Figure 5.58 (a)), whereas the V_T is found to be 1.9 V at 1 μA/mm with the V_T hysteresis considerably small of ~150 mV (Figure 5.58 (b)). The subthreshold slope is found to be 232 mV/dec. A relative positive V_T (−5.9 V) has been observed because of the 5 cycles recess of the GaN cap (~2.5 nm).

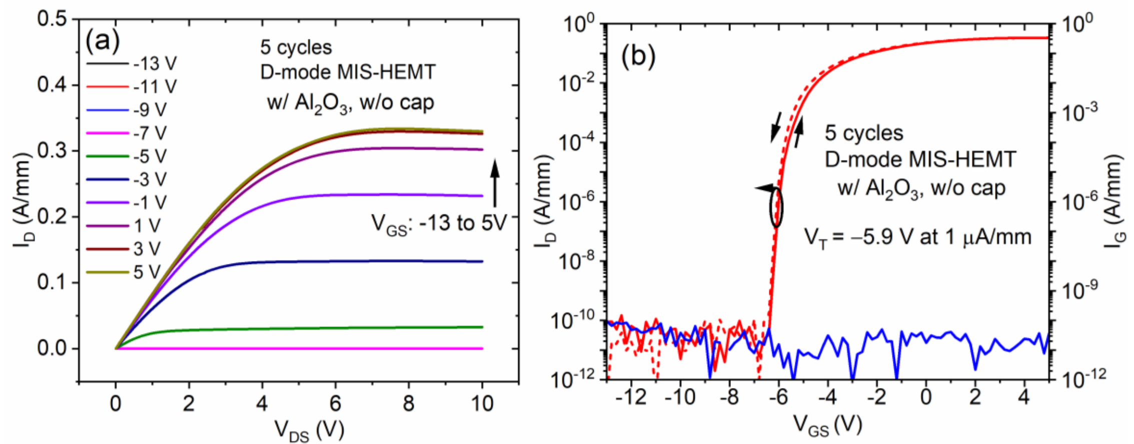

Figure 5.57: (a) Output characteristics and (b) transfer characteristics of D-mode MIS-HEMT for sample D. Device dimension: $L_{GS}/W_{GS}/L_G/L_{GD}$ = 5/100/3/5 μm.

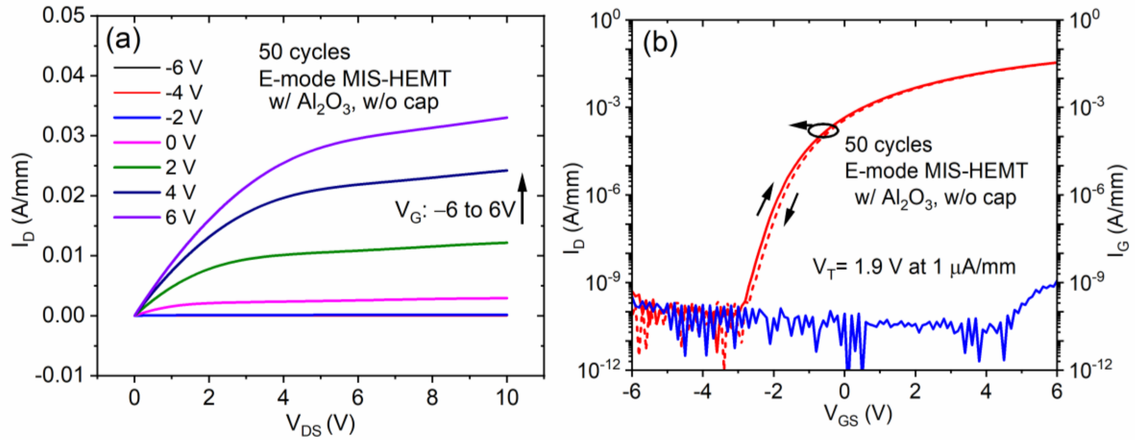

Figure 5.58: (a) Output characteristics and (b) transfer characteristics of E-mode MIS-HEMT for sample D. Device dimension: $L_{GS}/W_{GS}/L_G/L_{GD}$ = 5/100/3/5 μm.

Figure 5.59 shows the comparison of sub-threshold graphs for samples A, B, C, and D. It can be observed that the MIS-HEMT of sample C shows the lowest value of *SS* of ~80 mV/dec for E-mode device, whereas the *SS* slope of ~139 mV/dec for D-mode device. The MIS-HEMT of sample B shows a small value of *SS* slope of ~97 mV/dec for D-mode device, while the *SS* slope for E-mode device is found to be ~232 mV/dec. However, the D-mode HEMT has a large *SS* slope of ~326 mV/dec as compared to both samples B and C. Besides, the MIS-HEMT of Sample B is also found to have very large *SS* slope of ~1700 mV/dec.

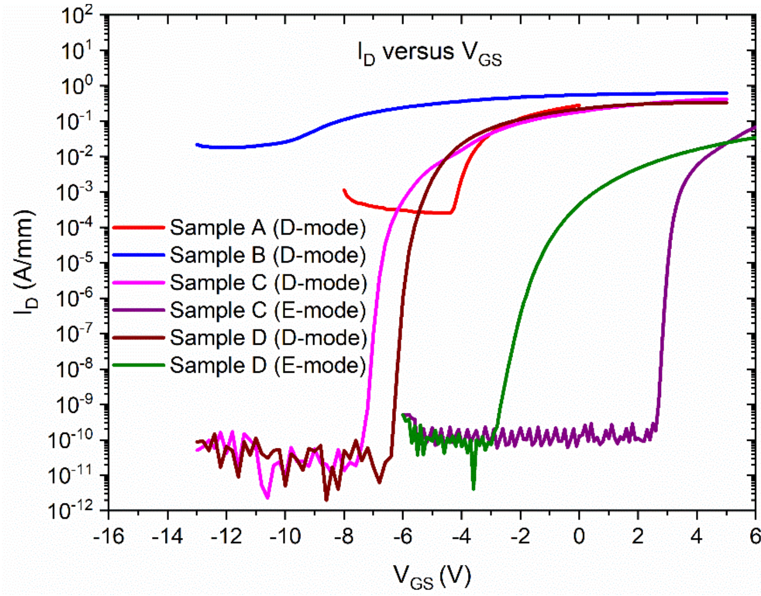

Figure 5.59: The comparison of sub-threshold graphs for all samples (A, B, C, and D).

The Al_2O_3/GaN interface trap density, D_{it} can be extracted using the capacitance techniques [313]–[316] focusing on the second slope of the onset voltage (V_{ON}) in the CV curves, which are capable of addressing the complications originating from the polarized barrier layer in III-V MIS-HEMTs, and accurately mapping out the distribution of interface traps over a broad time constant range. The onset voltage dispersion (ΔV_{ON}) occurs at two measurement frequencies (f_1, f_2) due to interface traps existing in the energy range from $E_{Trap}(f_1)$ to $E_{Trap}(f_2)$. The detectable energy of the interface trap $E_{Trap}(f_m)$ as a function of measurement frequency f_m can be represented by:

$$E_{Trap}(f_m) = E_C - E_T = KTln\left(\frac{v_{th}\sigma_n N_c}{2\pi f_m}\right) \quad (5.1)$$

where K is the Boltzmann's constant, T is the measurement temperature, $N_c = 2.7\times10^{18}$ cm^{-3} is the effective density of states in the conduction band of GaN, σ_n is the electron capture cross section, and $v_{th} = 2\times10^7$ $cm\cdot s^{-1}$ is the thermal velocity of electrons. An

equivalent average energy level of the interface state (E_{Avg}) in the energy range from $E_{Trap}(f_1)$ to $E_{Trap}(f_2)$ can be found as:

$$E_{Avg} = \frac{E_{Trap}(f_1) + E_{Trap}(f_2)}{2}. \tag{5.2}$$

According to the interface state density - energy level mapping method proposed by Yang et al. [314], distribution of the Al_2O_3/GaN interface states can be obtained by Equation (5.3):

$$D_{it}(E = E_{AVG}) = \frac{C_{OX} \cdot \Delta V_{ON}}{q\Delta E_{Trap}} - \frac{C_{ox} + C_B}{q^2} \tag{5.3}$$

where C_{ox} is the capacitance of ALD-Al_2O_3 dielectric, C_B is the capacitance of the AlGaN barrier layer, ΔE_{Trap} is the interface trap frequency dependent energy difference, and ΔV_{ON} is the onset voltage frequency dependent shift. The energy difference of interface states ΔE_{Trap} is described by Equation (5.4) [314] and can be calculated as:

$$\Delta E_{Trap} = E_{Trap}(f_1) - E_{Trap}(f_2). \tag{5.4}$$

The frequency dependent shift of the onset voltage ΔV_{ON} can be extracted using the Equation (5.5):

$$\Delta V_{ON} = \mathrm{V}_{ON}(f_1) - \mathrm{V}_{ON}(f_2). \tag{5.5}$$

The insertion of gate dielectric Al_2O_3 has a significant effect to the *CV* curve where two rising edges were observed for D-mode MIS-capacitor for sample B as shown in Figure 5.60 (a). The *CV* curve features two rising edges, where the first rising edge at negative V_G corresponds to the formation of the 2DEG channel, and the second

rising edge at positive V_G relates to the spill-over of the 2DEG to the Al_2O_3/GaN interface. The second slope can be used to extract the D_{it} as shown in Figure 5.61 where the average value of D_{it} was found to be 2.5 $\times 10^{13}$ cm^{-2}eV^{-1} using capacitance technique as described in the Equations (5.1)−(5.5). Meanwhile, the *CV* second slope for 40 cycles E-mode MIS-capacitor for sample B as shown in Figure 5.60 (b) exhibits only one slope and frequency dependent capacitance due to parasitic effects. However, the *CV* curves are not showing clear two rising edge features for both D and E-modes MIS-capacitors for sample C as shown in Figures 5.62 and 5.63, respectively. Moreover, the *CV* curve for D-mode MIS-capacitor of sample D shows the presence of the second slope and a large frequency dispersion as can be seen in Figure 5.64 (a). The extracted average D_{it} as shown in Figure 5.65 was found to be 5.6 $\times 10^{13}$ cm^{-2}eV^{-1}. Figure 5.66 shows the *CV* curve for E-mode MIS-capacitor of sample D with very large frequency dispersion observed which might be caused by over-etching of barrier layer.

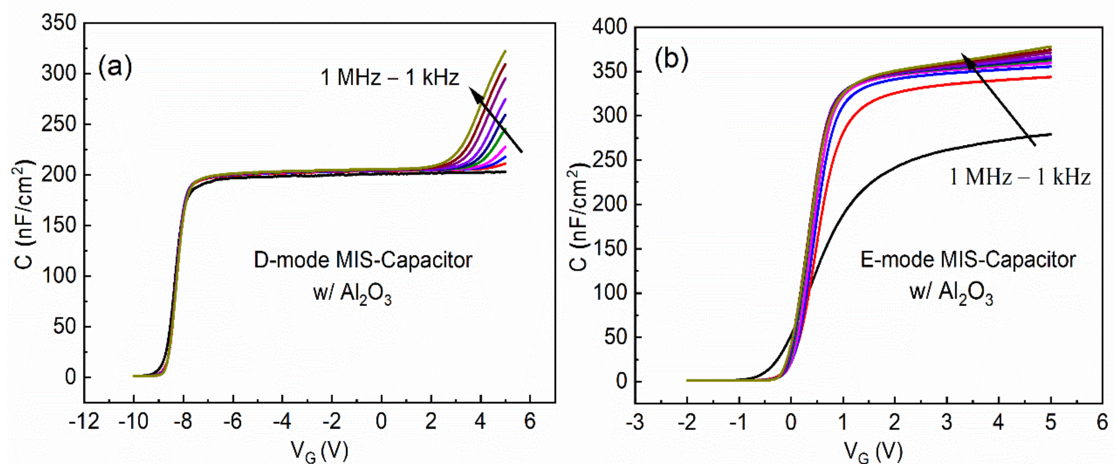

Figure 5.60: *CV* curves of MIS-capacitor for sample B (a) D-mode frequency dependent, (b) E-mode frequency dependent.

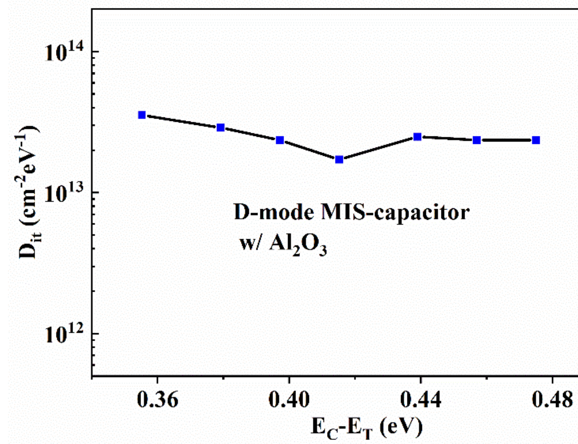

Figure 5.61: Extracted D_{it} from *CV* curves for sample B (D-mode MIS-capacitor with Al_2O_3 as gate dielectric).

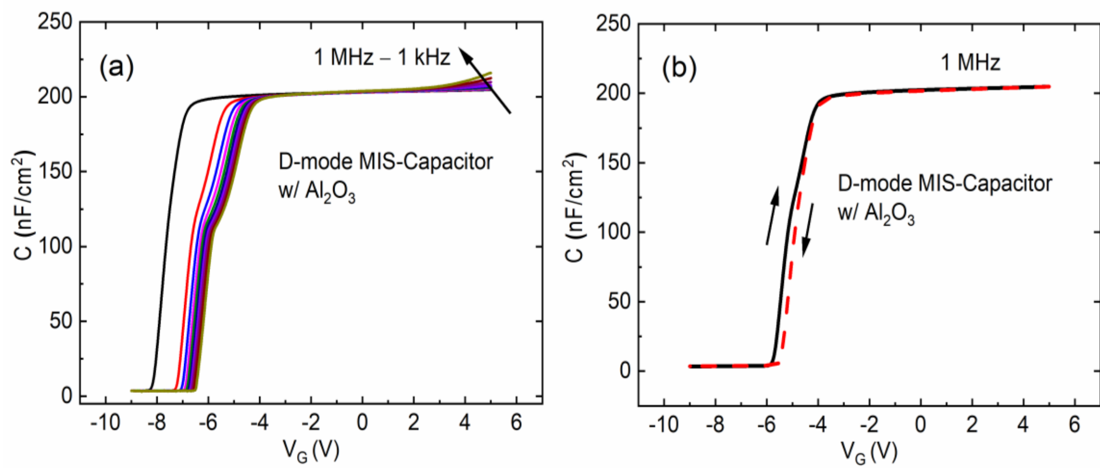

Figure 5.62: *CV* curves of MIS-capacitor for sample C (a) D-mode frequency dependent, (b) D-mode hysteresis at 1 MHz.

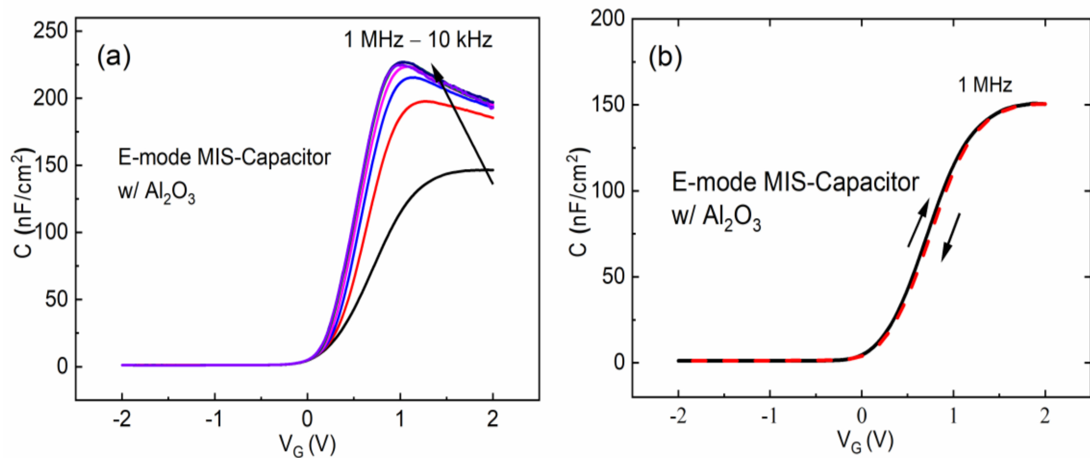

Figure 5.63: *CV* curves of MIS-capacitor for sample C (a) E-mode frequency dependent, (b) E-mode hysteresis at 1 MHz.

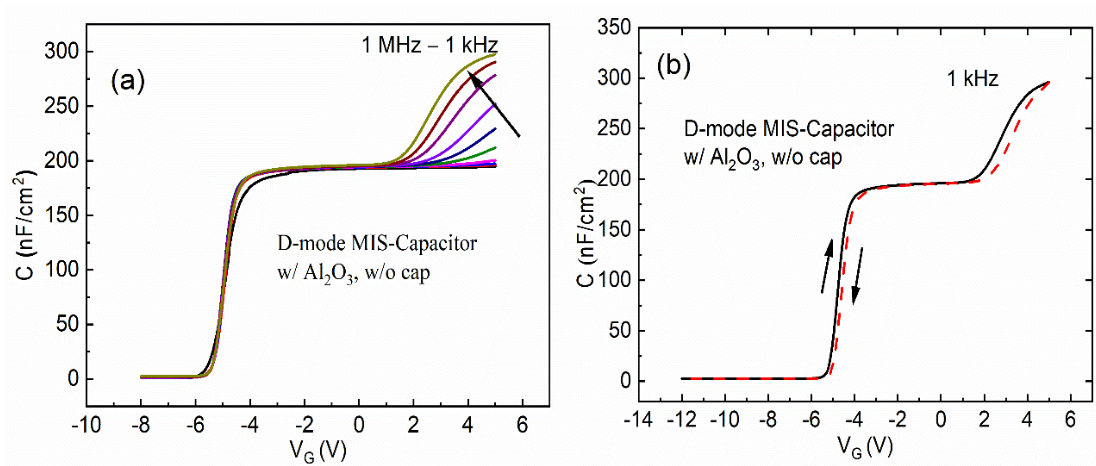

Figure 5.64: *CV* curves MIS-capacitor for sample D (a) D-mode frequency dependent, (b) D-mode hysteresis at 1 MHz.

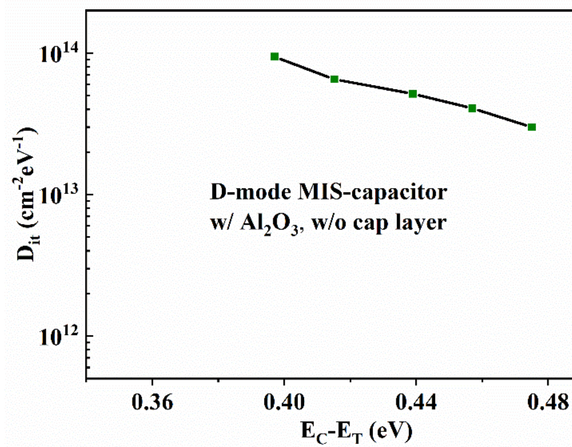

Figure 5.65: Extracted D_{it} from *CV* curves for sample D (D-mode MIS-capacitor with Al_2O_3 as gate dielectric, without GaN cap layer).

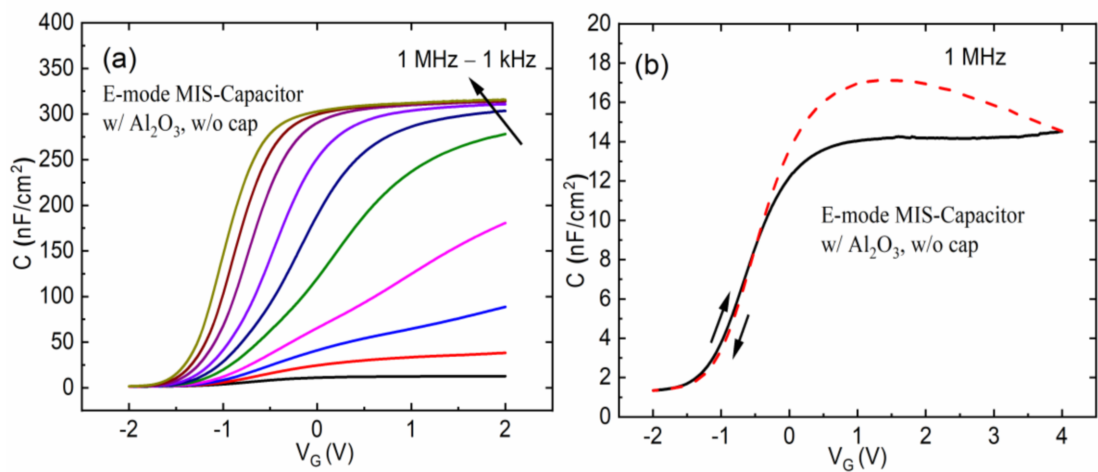

Figure 5.66: *CV* curves of MIS-capacitor for sample D (a) E-mode frequency dependent, (b) E-mode hysteresis at 1 MHz.

The D-mode and E-mode Al_2O_3 MIS-HEMTs were successfully investigated using IV and CV characterisations. The gate leakage current can be significantly reduced by using the MIS structures. The Al_2O_3 with a high permittivity and a large band offsets is a promising material as the gate dielectric of GaN based MIS-HEMTs. Based on our results for samples A, B, C and D, it can be found that the MIS-HEMTs of sample C show the best DC *IV* characteristics with a small *Vth* hysteresis of ~0.05 V for both D-mode and E-mode devices. Moreover, small sub-threshold slopes of ~80 mV/dec and ~139 mV/dec are found for E-mode and D-mode devices, respectively. However, we could not compare the sub-threshold and D_{it} results for all samples since the D_{it} can be only extracted from *CV* plots of samples B and D.

5.3.3.3 *Effect of different GaN surface treatments on Al_2O_3 based AlGaN/GaN MIS-HEMTs properties*

The DC transfer characteristics for the four samples are shown in Figure 5.67. The gate leakage current of the non-treated sample was two orders of magnitude larger than that of other three groups at a gate voltage of -10 V. The suppressed gate leakage currents of the ODT treated and O_2 plasma treated samples is probably due to the reduction of shallow interface state. The breakdown voltage of the gate dielectric is defined as the gate voltage when the gate current reaches 1 µA/mm. It can be observed that the gate breakdown voltages for the samples E, F, G and H are 10.1 V, 11.1 V, 13.2 V and 12.5 V, respectively. The highest breakdown electric field of 6.6 MV/cm is obtained for the O_2 plasma treated sample. The latter can be attributed to the formation of a thin oxidised GaN layer in the gate region [302]. An increase of the actual gate dielectric thickness can also be confirmed from the decrease of the capacitance visible for the O_2 plasma treated sample in Figure 5.67 and increased

intensity of the Ga-O component from the XPS Ga 3d CL fitting shown in Figure 5.51 (c). Note that the breakdown characteristic for the ODT treated sample is slightly improved from that of the HCl treated sample, but not as good as for the O_2 plasma treated sample. The V_T of the samples E, F, G and H are extracted to be -13.1 V, -11.8 V, -10.4 V, -12.3 V, respectively, with a drain current criterion of 1 μA/mm. Compared with the sample E, V_T shifted towards positive direction for samples F, G and H likely to be due to the reduction of positive charges on the treated GaN surface prior to the formation of Al_2O_3. The presence of positive charges can be explained as Ga dangling bonds on the GaN surface acting as positive charge centres, being generated due to N diffusing and leaving Ga-N bonds [317]. The I_{ON}/I_{OFF} ratio for the four samples E, F, G and H are estimated to be ~7×10^6, ~2×10^9, ~10^{10}, ~10^{10}, respectively. For the samples with the ODT and O_2 plasma treatments, the off-state leakage current was suppressed by over 3 orders as compared to the sample without treatment. It suggests that the N vacancies and impurities on the GaN can be reduced by the ODT and O_2 plasma treatments, hence causing a suppressed gate-induced drain leakage effect [301]. The samples E and F exhibit a threshold hysteresis (ΔV_T) of ~0.3 V and ~0.18 V, the subthreshold slope of ~150 mV/dec and ~100 mV/dec, respectively, revealing higher interface trap density at the Al_2O_3/GaN interface. In contrast, a small ΔV_T of ~0.12 V as well as a small *SS* of ~73 mV/dec are observed for the ODT treated sample. The latter is another evidence that the interface traps have been suppressed effectively by the ODT treatment. The O_2 plasma treated sample also exhibits a reduced ΔV_T of ~0.10 V and a reduced *SS* of ~68 mV/dec, which are slightly smaller than that of ODT treated sample. This indicates that the O_2 plasma treatment can effectively suppress the interface trap related switching transient in MIS-HEMTs. It is worth noting that as a dry process, the O_2 plasma treatment has relatively high demands for the

experimental equipment. Among the three treatments, the low-cost ODT treatment has demonstrated remarkably improved gate control characteristics of associated MIS-HEMTs with an increased I_{ON}/I_{OFF} ratio, a reduced ΔV_T and a reduced SS.

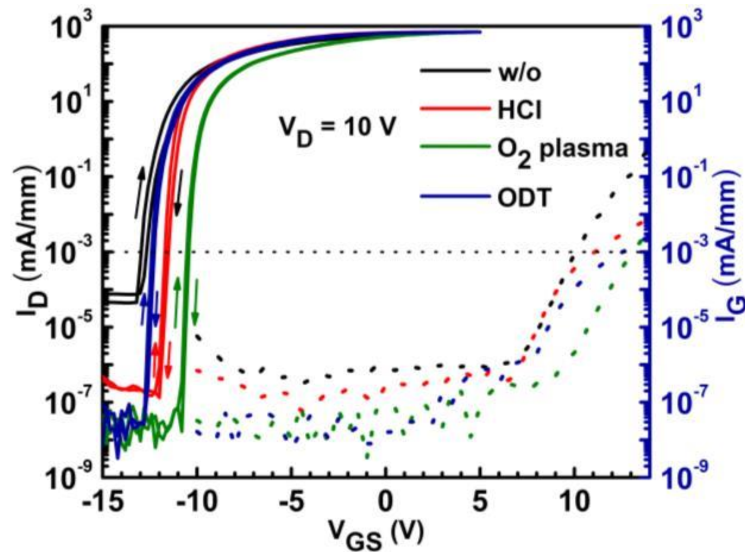

Figure 5.67: Transfer characteristics curves of the MIS-HEMT devices at V_{DS} of 10 V [310].

Multi-frequency CV characteristics of referring MIS-capacitor devices are shown in Figure 5.68. The measured V_G was swept from -14 to 5 V with a step of 20 mV, and the frequency was varied from 2 MHz down to 1 kHz. The CV curves feature two rising edges: the first rising edge at negative V_G corresponds to the formation of the 2DEG channel, and the second rising edge at positive V_G refers to the spill-over of the 2DEG at the Al_2O_3/GaN interface [316]. The frequency dispersion at the second rising edge has been observed in all samples and a larger frequency dispersion indicates a higher Al_2O_3/GaN interface traps density [318]. Furthermore, when applying a higher positive V_G, electrons start to distribute in the barrier AlGaN layer, leading to the increase of capacitance to the Al_2O_3 capacitance. The obvious horizontal frequency dispersion is detected in the second rising edge for the samples E, F and G. In contrast, by using the ODT GaN surface treatment (sample H), a rising edge with a smaller

frequency dispersion is observed. The value of C_{ox} can be extracted as maximum capacitance observed in CV plots in Figure 5.68 and is found to be 326 nF/cm^2 for the non-treated sample. The maximum capacitances were extracted from the CV curves at 1 kHz to avoid the low frequency limit effect [319]. The barrier layer capacitance can be calculated from the first plateau capacitance in Figure 5.68, as the latter refers to the series capacitance connection between C_{ox} and C_B. Figure 5.69 shows in detail the extraction of the gate voltage shift, ΔV_{ON}, from the second CV step for the capacitance method of extracting interface trap density. An accurate extraction of ΔV_f requires a noise-free measurement of capacitance increase, C_{detect}. The D_{it} distribution were estimated according to the interface state density-energy level mapping method. The ΔV_{ON} (f_m) is extracted by reading the voltage when the capacitance reached the 110% C_{floor}. Note that the C_{floor} is the total capacitance of ideal trap free dielectric-barrier gate stack.

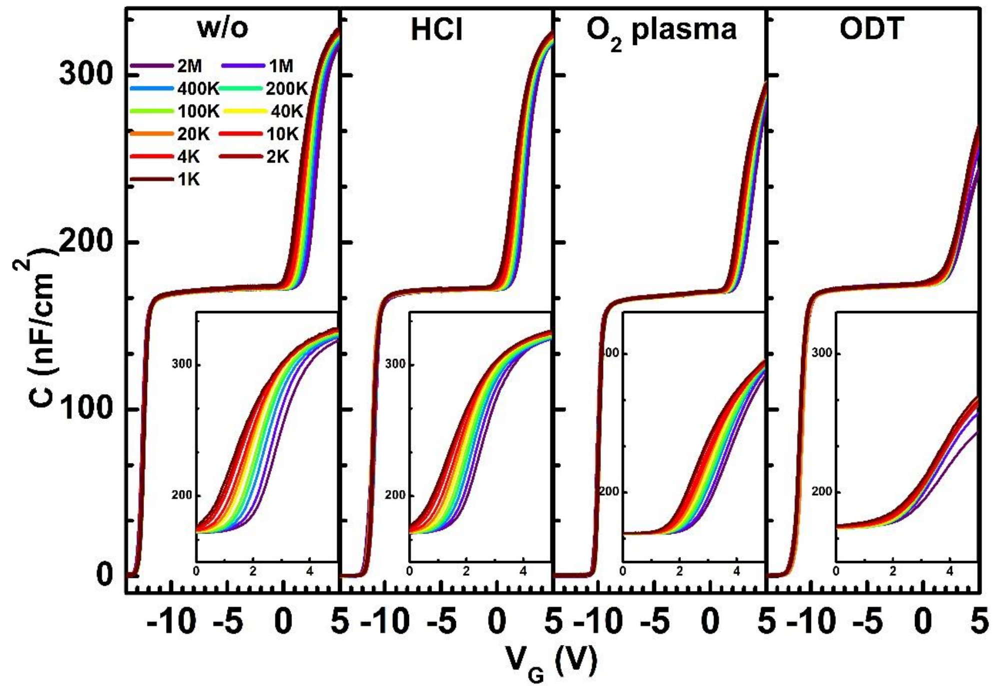

Figure 5.68: Multi-frequency CV characteristics of ALD-Al_2O_3/GaN/AlGaN/GaN MIS-capacitor structures (without (sample E) and with the HCl (sample F), O_2 plasma (sample G) and ODT (sample H) surface passivation treatments [310].

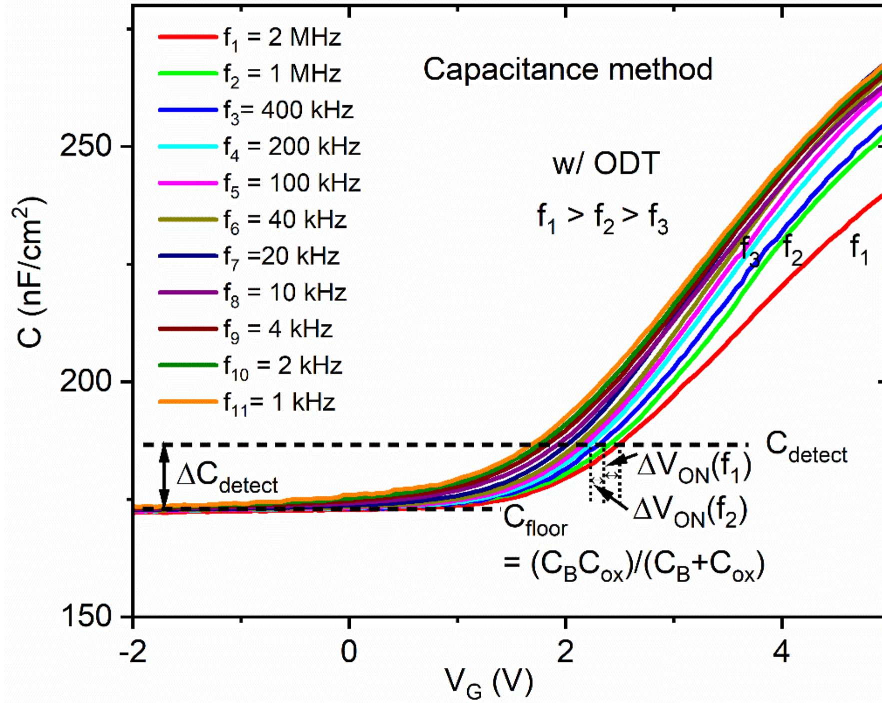

Figure 5.69: Schematic showing the extraction of the gate voltage shift, ΔV_f, from the second *CV* step for ALD-Al_2O_3/GaN/AlGaN/GaN MIS-capacitor structure with ODT surface treatment (sample H).

Figure 5.70 shows the results of the D_{it} at the Al_2O_3/GaN interface for the MIS-capacitor structures obtained using capacitance technique as described in the Equations (5.1) − (5.5). The electrons capture cross section at the interface σ_n was assumed to be 1.0×10^{-14} cm^2, giving values of D_{it} in the energy level range of ~0.28 eV to ~0.47 eV from the conduction band edge. For the HCl treated sample, the extracted D_{it} is calculated to be over 9 $\times 10^{12}$ $cm^{-2}eV^{-1}$ in this energy range, which is close to the reported value of 1.3×10^{13} $cm^{-2}eV^{-1}$ [320]. This is likely to be due to the re-oxidation of the exposed GaN surface before transferring the sample into the ALD chamber. For the O_2 plasma treated sample, D_{it} varies from 9.1 $\times 10^{12}$ to 4.8 $\times 10^{12}$ $cm^{-2}eV^{-1}$, when the energy level depth changes from 0.28 to 0.47 eV. In comparison, the ODT treated sample shows the lowest D_{it} among the four samples, from 6.1 $\times 10^{12}$ $cm^{-2}eV^{-1}$ down to 3.0 $\times 10^{12}$ $cm^{-2}eV^{-1}$, which is a relatively low value in comparison to reported ones

when Al_2O_3 was used as the gate dielectric in GaN-based MIS capacitor devices [294], [314], [316], [321]. The reduction of the D_{it} can be explained by the ability of the ODT treatment to fill in the N vacancies by creating Ga-S bonds, and hence by suppressing the re-oxidation which can occur before the ALD process. Meanwhile, the surface damage is minimized for the wet treatment; on the contrary, the O_2 plasma treatment may cause the GaN surface damage and lead to defects at the Al_2O_3/GaN interface as seen from this work and relevant studies reported in the literature. The reported values of D_{it} in Table 5.10 refer to the energy level of $E_C - E_T$ = ~0.47 eV. Note that the Al_2O_3/GaN interface state density obtained from the sample with the ODT treatment is close to that reported in the Refs. [294], [314], which is a fairly low compared to the others recently reported data (see Table 5.10). Furthermore, the cost and complexity of using the ODT treatment is much lower than that of the in site NH_3/Ar/N_2 plasma treatment with plasma enhanced ALD-Al_2O_3 gate dielectric. Table 5.11 shows the summary of DC characteristics for the Al_2O_3/GaN devices (samples A – H) from this work.

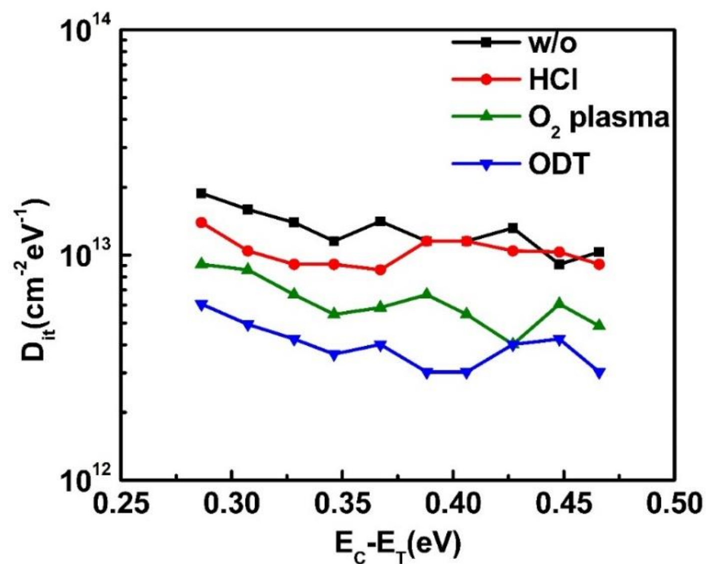

Figure 5.70: Distribution of D_{it} vs $(E_C - E_T)$ at an ALD-Al_2O_3/GaN interface for four types of GaN surface treatments used in this work [310].

Table 5.10: Summary of D_{it} values at $(E_C - E_T)$ = ~0.47 eV for the Al_2O_3/GaN interface from this work and literature [294], [314], [316], [321].

Reference	Dielectric	Deposition technique	Surface treatment	D_{it} ×10^{12} cm^{-2}eV^{-1}
[294]	Al_2O_3	PEALD	In site NH_3/Ar/N_2 plasma	~1
[314]	Al_2O_3	PEALD	In site NH_3/Ar/N_2 plasma	~2.2
[321]	Al_2O_3	ALD	N_2/O_2 plasma	~38
[316]	Al_2O_3	ALD	N_2/O_2 plasma	~9
This work	Al_2O_3	ALD	O_2 plasma	4.8
This work	Al_2O_3	ALD	ODT	3.0

Table 5.11: Summary of DC characteristics for the Al_2O_3/GaN HEMT (sample A) and MISHEMTs (sample B – H) from this work.

Sample	D-mode (recess cycles)				E-mode (recess cycles)			
	I_{Dmax} (A/mm)	V_T (V)	ΔV_T (V)	SS (mV/dec)	I_{Dmax} (A/mm)	V_T (V)	ΔV_T (V)	SS (mV/dec)
A	0.46 (at 2 V)	-4.1 (at 1 mA/mm)	~0.2	~326	–	–	–	–
B	0.62 (at 5 V)	-11.3	~0.1	~1700	–	–		–
C	0.41 (at 5 V)	-6.9 (at 1 µA/mm)	~0.05	~139	0.06 (at 6 V)	2.9 (at 1 µA/mm)	~0.05	~80
D	0.33 (at 5 V)	-5.9 (at 1 µA/mm)	~0.08	~97	0.03 (at 6 V)	1.9 (at 1 µA/mm)	~0.15	~232
E	0.61 (at 5 V)	-13.1 (at 1 µA/mm)	~0.3	~150				
F	0.6 (at 5 V)	-11.8 (at 1 µA/mm)	~0.18	~100				
G	0.53 (at 5 V)	-10.4 (at 1 µA/mm)	~0.1	~68				
H	0.59 (at 5 V)	-12.3 (at 1 µA/mm)	~0.12	~73				

5.4 ZrO_2-based MIS-HEMTs

5.4.1 Device fabrication

Yutao Cai from Xi'an Jiaotong-Liverpool University (XJTLU), China is acknowledged for his contribution in the fabrication of GaN HEMT and MIS-HEMT devices. The investigated GaN-based material stack consists of a 1 nm undoped GaN cap layer, a 22 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer, a 0.33 µm GaN channel layer, and a 5.4 µm highly resistive buffer on a 1 mm Si substrate. Firstly, the Au-free source and drain were formed by e-beam evaporation of Ti/Al/Ti/TiN (30/120/55/75 nm) patterned by a photolithography and a lift-off technology and annealed at 870 °C in N_2 ambient for 45 s by RTA. After the formation of ohmic contact, the mesa isolation region was formed by BCl_3/Cl_2 gas reactive ion etching. The surface treatment is performed for all samples to remove any native oxides prior to dielectric deposition by immersing in acetone, isopropanol, 1:10 $HCl:H_2O$ for 5 min sequentially and then rinsed with deionised water. After the organic cleaning processes, the sample was without any treatment. Another sample with ODT treatment was immersed in a 5 mM ODT in ethanol at RT for 24 hours to passivate the GaN surface. After the ODT exposure, the sample was immersed in ethanol and ultrasonically cleaned for 10 min followed by N_2 drying. Furthermore, before the ALD, the sample was exposed to 30 H_2O pulses with the same pulse/purge duration as used in the ALD process at 260 °C in the ALD reactor. The ZrO_2 films with a nominal thickness of 20 nm were grown by ALD at 250 ºC at a chamber pressure of ~50 Pa as the gate dielectric using tetrakis (ethylmethylamino) zirconium as the precursor and H_2O as the oxidant source. The ZrO_2 growth rate was 1.2 Å/cycle. High purity N_2 (20 sccm) was used as the precursor

carrier and purge gas. After local ZrO_2 removal with 1% HF, another photolithography process was used to define Ni/TiN (50/50 nm) gate electrodes.

5.4.2 Effect of ODT GaN surface treatment on ZrO_2-based AlGaN/GaN MIS-HEMTs properties

Figure 5.45 shows the output and transfer characteristics of ZrO_2-based D-mode AlGaN/GaN MIS-HEMT without ODT surface treatment. For I_D versus V_{DS} measurement, the V_{DS} is measured from 0 V to 10 V with a step of 0.1 V and the V_{GS} is swept from -9 V to 3 V. Whereas, for I_D against V_{GS} measurement, the V_{GS} is varied from -9 V to 3 V with a step of 0.1 V. The I_{Dmax} is found to be 0.57 A/mm at 3 V (Figure 5.45 (a)), whereas the V_T is -7.3 V at 1 mA/mm (Figure 5.45 (b)). A small ΔV_T and subthreshold slope of ~0.05 V and 84 mV/dec, respectively have been found. For this device, the leakage current is very small, less than 1 nA/mm.

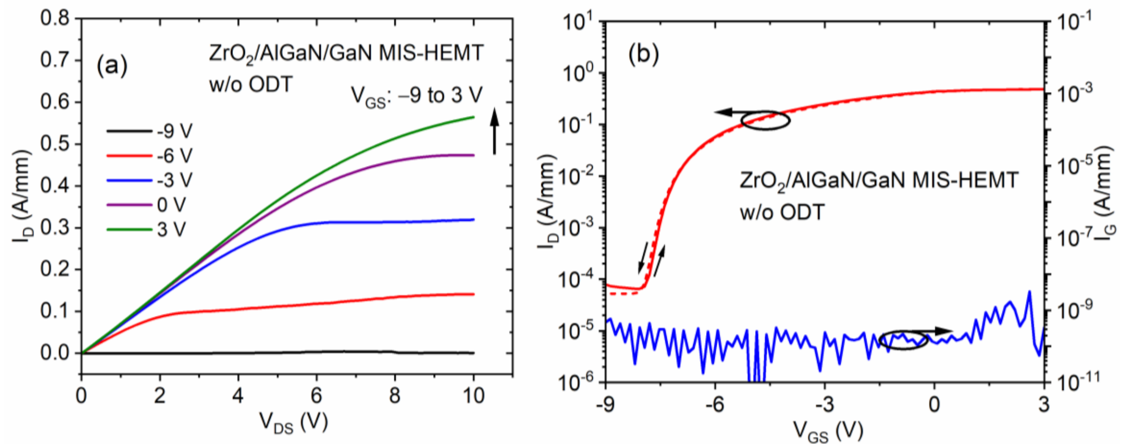

Figure 5.71: (a) Output characteristics and (b) transfer characteristics of D-mode ZrO_2-based MIS-HEMT without ODT surface treatment. Device dimension: $L_{GS}/W_{GS}/L_G/L_{GD}$ = 3/50/3/10 μm.

Figure 5.72 shows the output and transfer characteristics of ZrO_2-based D-mode AlGaN/GaN MIS-HEMT with ODT surface treatment. For I_D versus V_{DS} measurement, the V_{DS} is measured from 0 V to 10 V with a step of 0.1 V and the V_{GS} is swept from -12 V to 3 V. Whereas, for I_D against V_{GS} measurement, the V_{GS} is varied from -17 V to 3 V with a step of 0.1 V. It was found that the I_{Dmax} is reduced to 0.35 A/mm at 3 V (Figure 5.72 (a)) and the V_T is shifted to negative side which give the value of -13.2 V at 1 mA/mm (Figure 5.72 (b)). The ΔV_T and subthreshold slope are large compared to the device without ODT and found to be 0.2 V and 330 mV/dec, respectively. The leakage current is very small, less than 1 nA/mm, but it increases largely when negative bias is applied after -6 V. Table 5.12 shows the summary of DC characteristics for the ZrO_2/GaN MIS-HEMTs with and without ODT surface treatment.

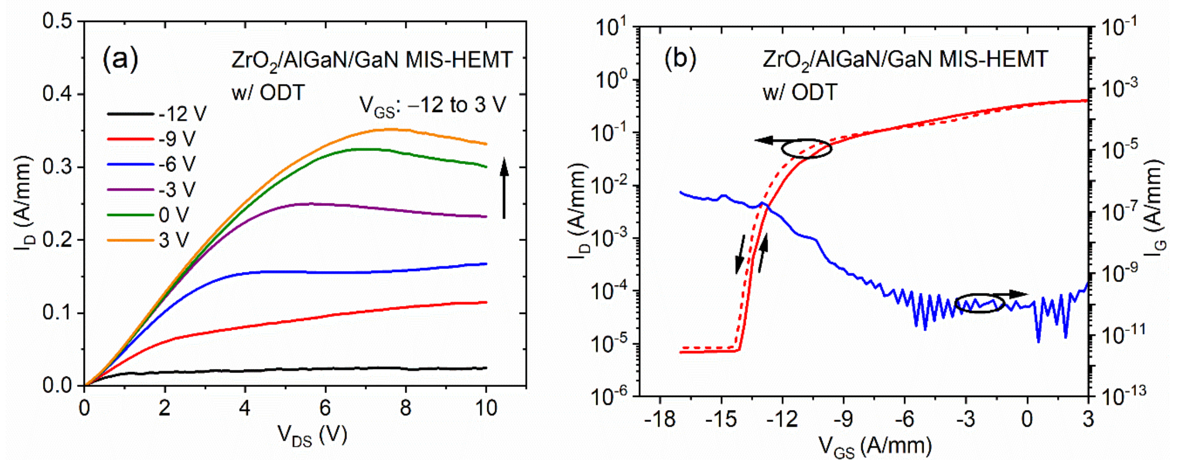

Figure 5.72: (a) Output characteristics and (b) transfer characteristics of D-mode ZrO_2-based MIS-HEMT with ODT GaN surface treatment. Device dimension: $L_{GS}/W_{GS}/L_G/L_{GD}$ = 3/100/3/10 µm.

Table 5.12: Summary of DC characteristics for the ZrO_2/AlGaN/GaN MIS-HEMT devices fabricated in this work

ZrO_2-based MIS-HEMT	D-mode			
	I_{Dmax} (A/mm)	V_T (V)	ΔV_T (V)	SS (mV/dec)
Without ODT	0.57 (at 3 V)	-7.3 (at 1 µA/mm)	~0.05	~84
With ODT	0.35 (at 3 V)	-13.2 (at 1 µA/mm)	~0.2	~330

Figure 5.73 shows the *CV* curves for D-mode AlGaN/GaN MIS-capacitor with ZrO_2 without ODT surface treatment where the measurement voltage was swept from -10 to 3 V with a step of 20 mV, and the frequency was varied from 1 MHz down to 10 kHz. The D-mode *CV* curves show not very clear two rising edge features with a large frequency dispersion in accumulation region. The *CV* curves for the device with ODT GaN surface treatment are shown in Figure 5.74, where the measurement voltage was swept from -15 to 3 V with a step of 20 mV, and the frequency was varied from 1 MHz down to 40 kHz. The D-mode *CV* curves show not very clear two rising edge features and small frequency dispersion in the accumulation region. The *CV* clockwise hysteresis for the sample without ODT (Figure 5.73 (b)) is likely to be due to the slow-trapping effect, whereas the anti-clockwise hysteresis observed for sample with ODT treatment (Figure 5.74 (b)) could be due to mobile charges in the oxide.

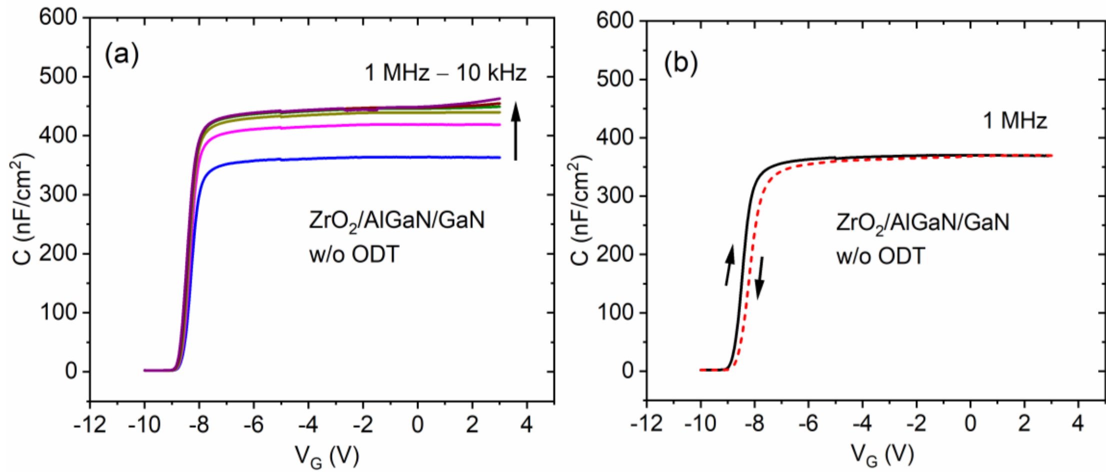

Figure 5.73: *CV* curves for ZrO_2-based MIS-capacitor without ODT surface treatment. (a) frequency dependent, (b) hysteresis at 1 MHz.

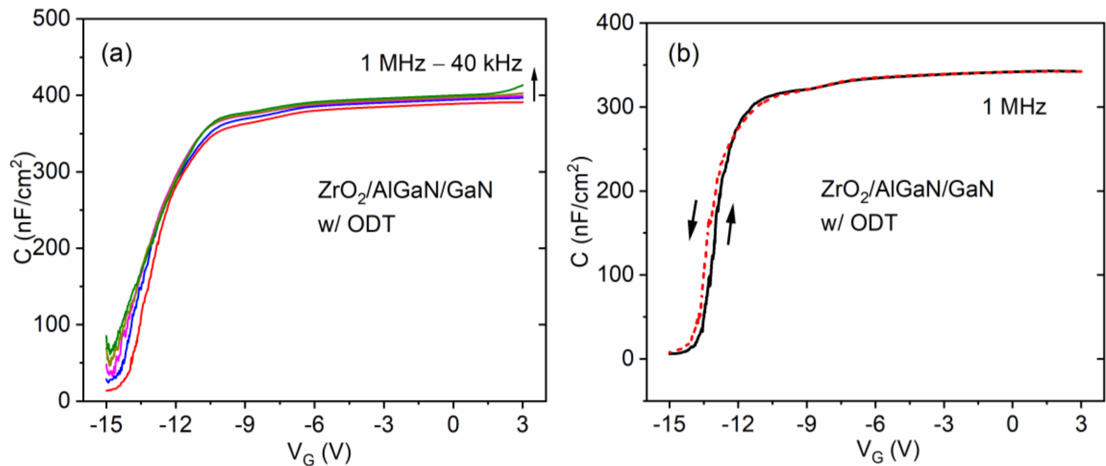

Figure 5.74: *CV* curves for ZrO_2-based MIS-capacitor with ODT surface treatment. (a) frequency dependent, (b) hysteresis at 1 MHz.

The MIS-HEMT devices for Al_2O_3-based with ODT treatment were found to be more effective as compared to ZrO_2-based with ODT treatment in term of its electrical characteristics with a low V_T hysteresis of 0.12 V and a small *SS* of 73 mV/dec. ZrO_2-based MIS-HEMTs showed a large negative shift in V_T as well as a higher value of *SS* after ODT GaN surface treatment.

5.5 Conclusion

The electrical characterisation of MIS-capacitors processed with different gate dielectrics (ZrO_2, Al_2O_3, MgO and Ta_2O_5) have been performed. The *JV* characteristics of MIS-capacitors with gate dielectrics MgO and Al_2O_3 show low leakage current of 3.2×10^{-6} A/cm^2, 5.3×10^{-6} A/cm^2 at 1 V respectively at a positive bias of 1 V, whereas, a high leakage current of 6.2×10^{-4} A/cm^2 at 1 V and 7.7×10^{-4} A/cm^2 has been observed for the MIS-capacitor with ZrO_2 and Ta_2O_5 gate dielectrics. The conduction mechanisms analysis using typical *JV* characteristics plotted on log-log scale shows evidence of SCLC mechanism in the low electric field region (0-1.5 V) which would indicate that the current flow is inhomogeneous and bulk rather than electrode limited. It has not been possible therefore to extract barrier heights which might be compared to those derived from XPS in Chapter 4.

Furthermore, the effect of surface treatments prior to ALD-Al_2O_3 deposition on the GaN/AlGaN/GaN heterostructure have been investigated. GaN surface passivation process based on the ODT treatment has been proposed to improve the Al_2O_3/GaN interface quality. The GaN surface was also treated by HCl and O_2 plasma. According to the XPS results, the re-oxidation has been hard to be avoided on the HCl treated GaN surface. In addition, the O_2 plasma treatment has been found to be able to fill the N vacancies on the GaN surface by oxygen atoms. Moreover, the ODT treatment has been found to passivate N vacancies by sulphur atoms and prevent the formation of detrimental native oxide. The multi-frequency *CV* results indicate that the ODT treatment reported here is a useful process to reduce the Al_2O_3/GaN interface state density. In addition, the *IV* characteristics point out that the O_2 plasma treatment is capable to reduce the positive charges on the GaN surface and reduce the positive bias-induced V_T instability considerably. The MIS-HEMTs fabricated using the low-

cost ODT GaN surface treatment have been found to exhibit effective characteristics which are highly desirable in power switching applications such as a low V_T hysteresis of 0.12 V, a small SS of 73 mV/dec, and a low D_{it} of 3.0 $\times 10^{12}$ cm^{-2}eV^{-1}.

CHAPTER 6

Study of surface treatments on III-V compound semiconductors

6.1 Introduction

III-V compound semiconductors have received increased attention in the development of nanometre-scale logic transistors because they have the highest electron mobility amongst all the conventional semiconductors, making them an extremely attractive candidate for the channel materials. Due to their unique optical and electronic properties, the III–V compound semiconductors are already widely used in high speed, high-frequency electronics, lasers, light-emitting diodes and detectors for optical communications, instrumentation and sensing. Figure 6.1 shows the extraordinary electron and hole mobility for various III-V semiconductor compounds [93].

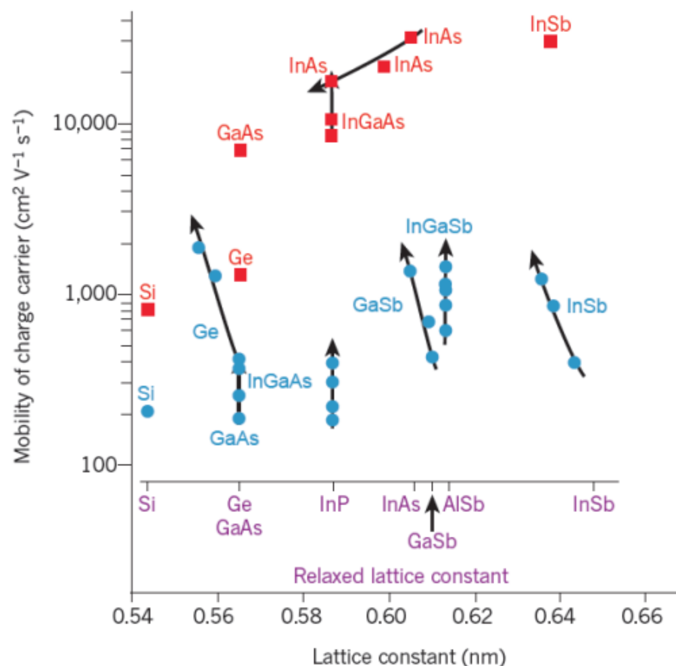

Figure 6.1: Electron and hole mobility versus lattice constant for different conventional semiconductors [93].

III-V materials with high electron velocities are considered as one of the promising candidates for *n*-channel transistors, where non-planar device architectures such as FINFETs (Fin Field Effect Transistors) or nanowires [93] are required. The fabrication of these devices requires low damage etching processes for fin/wire formation and a high-quality metal-oxide-semiconductor (MOS) interface on a variety of surface orientations. Moreover, from a fabrication side, there is a requirement that there are no wet chemical cleans or passivation treatments in the process flow. It has been shown that inductively coupled plasma (ICP) etching in a $Cl_2/CH_4/H_2$ based chemistry provides vertical InGaAs sidewall profiles as required for non-planar III-V devices [322]. However, recent electrical results on MOS capacitor structures showed that the etched InGaAs surface required an oxygen plasma/acid wet clean "digital etch" after the ICP etching, and a subsequent wet chemical sulphur passivation prior to atomic layer deposition (ALD) of Al_2O_3 to achieve low density of interface states (D_{it}) [322], [323]. Hence, clustering ICP etch and ALD tools prevent the native oxide formation on etched surfaces and allow performing a sequence of etch processes to form highly anisotropic structures which can then be cleaned by low damage plasma techniques. Furthermore, cyclic tri-methyl-aluminum (TMA) precursor and plasma gas pre-treatment with N_2 and H_2 prior to high-k gate dielectric deposition can accomplish sulphur-free native III-V surface preparations with low D_{it} [96], [103], [324]. The first use of a clustered ICP etch and ALD tool to assess the impact of in-situ plasma treatments on (100) and (110) oriented InGaAs MOS capacitors has been reported by University of Glasgow [325]. This study compares the use of in-situ cyclic plasma N_2/TMA and plasma H_2/TMA processes after ICP etching and prior to ALD deposition of HfO_2. It has been shown that plasma H_2 is effective in recovering the etch damage on both oriented InGaAs layers (100) and (110). The quality of the

interface between ALD HfO_2/InGaAs has been assessed by X-ray photoelectron spectroscopy (XPS), in particular looking into the effect of different substrate orientations (100) and (110) and H_2/TMA/H_2 surface plasma treatment on electrical properties reported in [325].

Furthermore, antimony-based compound semiconductors are promising candidates for future complementary metal-oxide-semiconductor (CMOS) devices [326], tunnel field effect transistors (TFETs) [327], and mid-infrared optoelectronics [328]. Antimonides exhibit excellent transport properties for both electrons and holes, e.g. InSb and GaSb have bulk electron/hole mobilities of 77000/1000 cm^2/Vs respectively [329], [330] and therefore could circumvent the bottleneck in III-V *p*-type MOSFET performance. An all III-V CMOS technology would offer substantially reduced fabrication complexity in comparison to hybrid CMOS, where *p* and *n*-type devices of different (largely lattice mismatched) materials require co-integration on a common substrate, and each device polarity has a significantly different thermal budget [331]. Much has been published with regards to the potential benefits of III-V CMOS for low power digital logic [93]; however, it is also of interest for millimetre-wave applications. In recent years, III-V *n*-type MOSFETs have progressed such that their performance is now competitive with that of high electron mobility transistors (HEMTs) [332]. This development illustrates the potential for III-V CMOS to outperform Si RF CMOS while retaining the benefits of lower power consumption and increased scalability in comparison to HEMT technology. $In_xGa_{1-x}Sb$ ternary compounds offer the combined optimal performance for electrons and holes in the same material. The incorporation of In maintains excellent electron transport [332], while room temperature hole mobilities as high as 1500 cm^2/Vs have been demonstrated in strained *p*-$In_{0:4}Ga_{0:6}Sb$ quantum wells [117]. As such, complementary

devices which have a common channel material of $In_xGa_{1-x}Sb$ have the potential to offer the simplest manifestation of III-V CMOS, where *p* and *n*-type devices can be fabricated with a unified process. Forming an unpinned dielectric interface to InGaSb with a low interface trap density is critical in order to fully exploit its advantageous material properties. To date, while InGaSb devices have been demonstrated [333], [334], systematic studies on improving the electrical properties of the dielectric interface to antimonides have been limited to GaSb [98], [335], [336]; and InSb only [99], [337]. For the former, ex-situ hydrochloric acid (HCl) [335] and $(NH_4)_2S$ [336] surface treatments as well as in-situ H_2 plasma exposure [98] have yielded promising results.

In this chapter, the effect of several surface treatments on both *n* and *p*-type $In_{0.3}Ga_{0.7}Sb$ has been investigated prior to ALD deposition of Al_2O_3. The surface treatments include HCl only, both ex-situ HCl and in-situ H_2 plasma exposure ($HCl+H_2$) at two different plasma powers of 150 W and 250 W. The characterisation has been performed mainly using XPS measurements to understand the chemical composition of the Al_2O_3/InGaSb interface with different surface treatments and correlate with electrical results. The electrical characterisation for all samples has been done by our collaboration group from University of Glasgow, UK.

6.2 InGaAs orientation and surface treatments effect on electrical properties of HfO_2/InGaAs based MOS capacitors

6.2.1 Process flow of the HfO_2/InGaAs samples

The 200 nm *n*-$In_{0.53}Ga_{0.47}As$ layers were grown by molecular beam epitaxy (MBE) on (100) and (110) oriented InP, uniformly doped with Si at 1×10^{17} cm^{-3} and

4×10^{17} cm^{-3} respectively. The wafer was initially degreased for 1 min each in acetone, methanol, and isopropanol. Then, the *n*-type (100) and (110) oriented $In_{0.53}Ga_{0.47}As$ surfaces were etched in inductively coupled plasma (ICP) chamber using $Cl_2/CH_4/H_2$ etch chemistry, transferred via a central vacuum chamber to an ALD chamber and subjected to 10 cycles plasma H_2/TMA pre-treatment in the ALD chamber prior to plasma HfO_2 gate dielectric deposition. A control sample which went through ICP etching and had plasma HfO_2 deposition without plasma pre-treatments was included in the study. Each plasma pre-treatment cycle comprised a plasma H_2 pulse, a pump step, a short TMA pulse, followed by an Ar gas draw/purge step and a plasma H_2 pulse followed by 4 s of a H_2 stabilisation step [338]. 25 cycles of plasma HfO_2 were then deposited at 300°C by ALD. The formation of Pt/Au gate electrode deposited by e-beam evaporation using shadow mask is performed before forming gas annealing in $H_2:N_2$ = 5 %:95 % at 350°C for 15 minutes. The last step is the formation of back side contacts, which are defined by blanket deposition of Au/Ge/Ni/Au. The process flow of InGaAs samples is shown in Figure 6.2, and the fabricated samples with different surface treatments are listed in Table 6.1. The control samples which labelled as (100) and (110) went through the ICP etching using $Cl_2/CH_4/H_2$ and had plasma HfO_2 deposition without plasma pre-treatments, whereas samples with FGA treatment are labelled as (100F) and (110F). The samples using both plasma gas treatment (H_2/TMA/ H_2) and FGA are labelled as (100HTH) and (110HTH). Dr David Millar from School of Engineering, University of Glasgow, UK is acknowledged for his contribution in the sample preparation as well as the electrical measurements of the devices. Meanwhile, we have done the XPS measurements in the Department of Physics and Stephenson Institute for Renewable Energy, University of Liverpool, UK. These fabricated samples are summarised in Table 6.1.

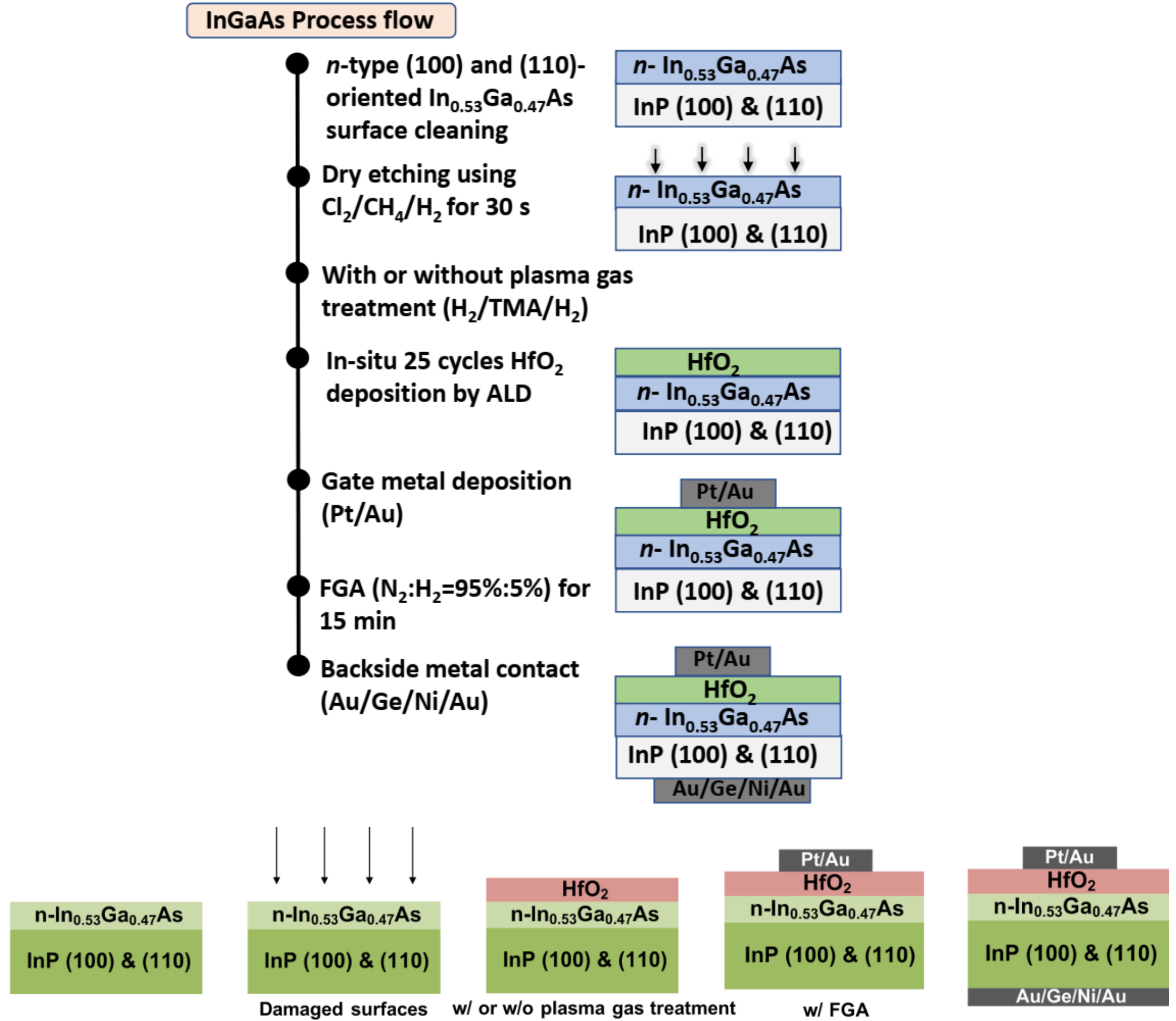

Figure 6.2: The process flow of *n*-type InGaAs MOS-capacitor.

Table 6.1: The list of *n*-type $In_{0.53}Ga_{0.47}As$ samples with different surface treatments.

Sample description	Sample label
(100) InGaAs blanket sample	InGaAs (100)
(110) InGaAs blanket sample	InGaAs (110)
HfO_2/(100) InGaAs control sample	100
HfO_2/(110) InGaAs control sample	110
HfO_2/(100) InGaAs with FGA	100F
HfO_2/(110) InGaAs with FGA	110F
HfO_2/(100) InGaAs with H_2/TMA/H_2 + FGA	100HTH
HfO_2/(110) InGaAs with H_2/TMA/H_2 + FGA	110HTH

6.2.2 XPS studies of HfO_2/InGaAs interface

The XPS measurements were performed using non-monochromatic XPS system with Al Kα (1486.6 eV) radiation operated at a power of 144 W. The spectrometer consisted of a Scienta SES200 hemispherical electron energy analyser which was operated such that the resolution is limited by the source. The precision of measurement is about ± 0.2 eV. All the spectra were fitted with Gaussian-Lorentzian line shapes after Shirley-type background subtraction. For InGaAs substrates, the binding energy (BE) for all core level (CL) spectra were corrected using C 1s at 284.6 eV. Then, the BE for all CL spectra for HfO_2/InGaAs samples was corrected to the As $3d_{5/2}$ CL at 40.47 eV from the InGaAs substrate as the reference sample. For As 3d CL, the branching ratio and the spin orbit splitting values of 3:2 and 0.7 eV for the As 3d doublet (5/2 and 3/2) are considered for the fit.

6.2.2.1 *XPS analysis of InGaAs blanket samples*

For InGaAs (100) blanket sample, the In $3d_{5/2}$ CL spectrum (Figure 6.3 (a)) has an asymmetric shape with tailing towards higher BE, suggesting the existence of the In oxides. Therefore, this lineshape can be fitted using two peaks, where the main peak at BE of 443.62 eV is related to InGaAs substrate and the small peak at BE of 444. 47 eV corresponds to In-O. The BEs of deconvoluted In $3d_{5/2}$ CL for InGaAs (110) blanket sample are found to be at 443.56 eV and 444.41 eV referring to InGaAs substrate and In-O, respectively (Figure 6.3 (b)).

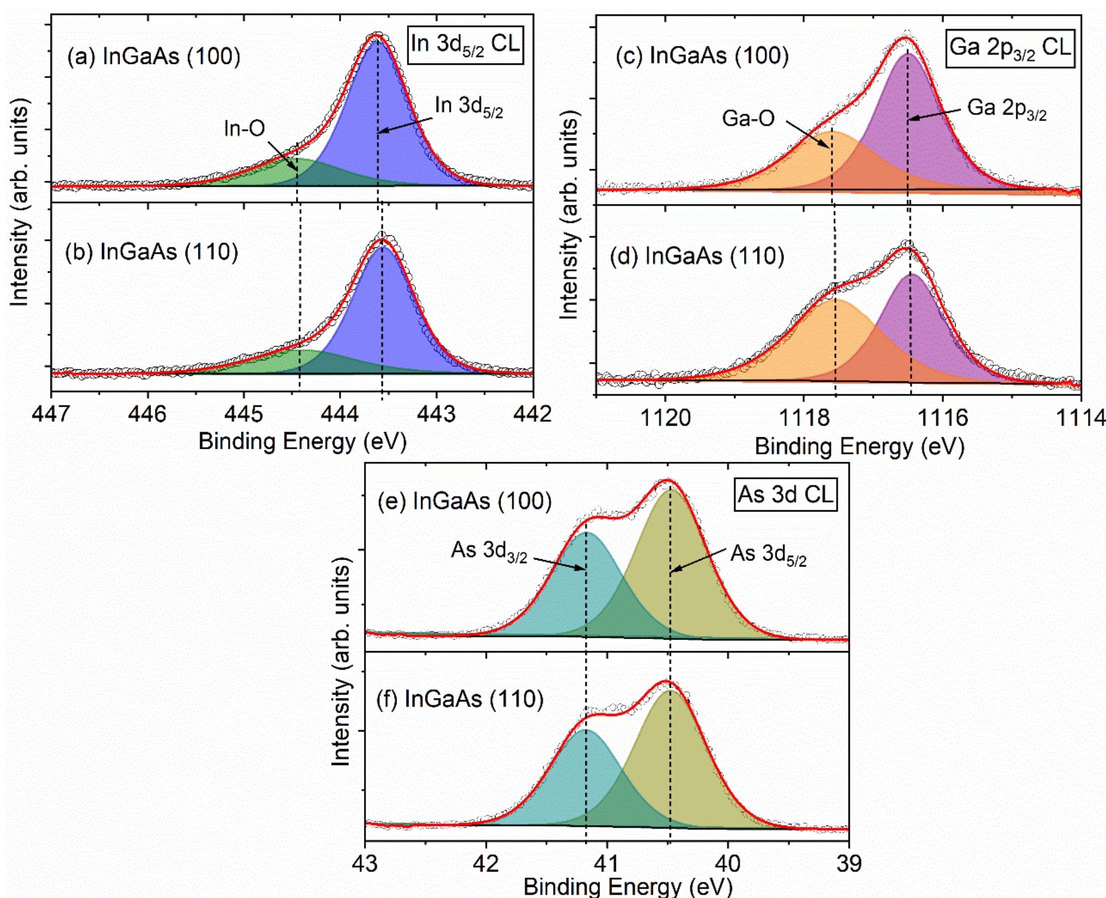

Figure 6.3: The deconvoluted XPS spectra for (100) and (110) InGaAs blanket samples of (a) In $3d_{5/2}$, (b) Ga $2p_{3/2}$ and (c) As 3d CLs.

The difference in BE between the main substrate peak and the oxide peak is 0.85 eV for both (100) and (110) InGaAs blanket samples. Previous work reported that In $3d_{5/2}$ for InGaAs is located at BE of 444.1 eV and In_2O_3 was found at BE of 444.8 eV, which constitutes 0.7 eV shift towards higher BE from InGaAs substrate peak [339]. Other work also reported a shift of 0.73 eV and 1.2 eV towards higher BE from InGaAs substrate peak assigned to In_2O_3 and In_2O_5, respectively [340].

For InGaAs (100) blanket sample, two components are needed to fit the Ga $2p_{3/2}$ spectra (Figure 6.3 (c)): the component at the lower BE of 1116.5 eV represents Ga $2p_{3/2}$ of InGaAs substrate, while the one on the high BE side at 1117.6 eV with a chemical shift of 1.1 eV from the bulk peak represents Ga-O bond. For InGaAs (110)

blanket sample, these peaks appear at BEs of 1116.44 eV and 1117.54 eV, respectively (Figure 6.3 (d)). These peaks slightly shift within the experimental error of ± 0.2 eV as compared to (100) InGaAs blanket sample. The difference in BEs between the InGaAs main substrate peak and the oxide peak was found to be 1.1 eV. It has been reported that the sub-peak with the chemical shift of 0.6–1 eV from the bulk peak represents Ga_2O_3 [339]. Hence, it can be deduced that a small amount of Ga_2O_3 is present on the surface of both samples, where the Ga-O bond is more pronounced for (110) orientation than for (100) (see Figure 6.3 (c) and (d)).

Furthermore, the As 3d CL spectra for both (100) and (110) InGaAs blanket samples shown in Figures 6.3 (e) and (f) can be deconvoluted into two peaks at BEs of 40.47 eV and 41.17 eV corresponding to the As 3d doublet (5/2 and 3/2) for InGaAs. Previous work has reported BEs of 40.82 eV for As $3d_{5/2}$ and 41.52 eV for As $3d_{3/2}$ assigned to InGaAs substrate [339].

6.2.2.2 *XPS analysis of HfO_2/InGaAs samples after H_2/TMA/H_2 plasma exposure and forming gas anneal*

In $3d_{5/2}$ CL spectra for samples with HfO_2 deposited on (100) and (110) InGaAs under different conditions are shown in Figure 6.4. For HfO_2/(100) InGaAs samples (Figures 6.4 (a)-(c)), In $3d_{5/2}$ CL can be fitted using two components at BEs of 443.85 eV and 444.51 eV for (100) sample (Figure 6.4 (a)); 443.83 eV and 444.62 eV for (100F) sample (Figure 6.4 (b)); and 443.85 eV and 444.51 eV for (100HTH) sample (Figure 6.4 (c)); the respective peaks are related to InGaAs substrate and In-O. The difference in BEs between InO_x and InGaAs substrate peak is 0.66 eV for (100) sample. However, the oxide peak shifts to 0.79 eV and 0.85 eV from the main bulk InGaAs peak for (100F) and (100HTH) samples, respectively. This could be due to

stoichiometric changes in InO_x, although it is noted that these slight changes in BEs are within the experimental error of ± 0.2 eV.

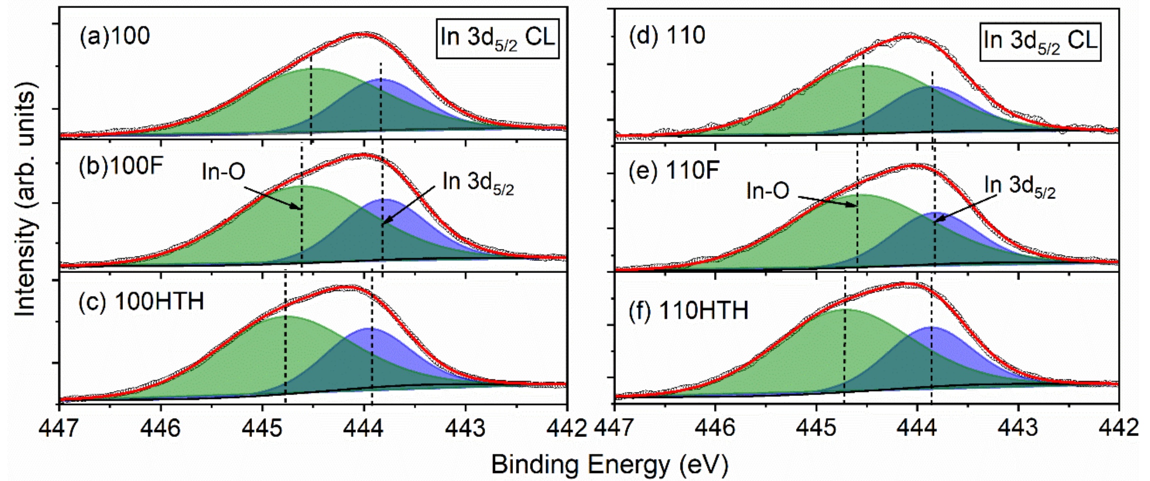

Figure 6.4: The deconvoluted XPS spectra of In $3d_{5/2}$ CL for HfO_2/(100) InGaAs samples under different surface treatments: (a) control sample 100, (b) after FGA 100F and (c) plasma surface treatment and FGA, 100HTH; in comparison to the same samples but on (110) InGaAs substrate: (d) 110, (e) 110F and (f) 110HTH.

Figures 6.4 (d)-(f) show no dramatic changes in the BE positions to the ones found for the HfO_2/(100) InGaAs samples. The line shapes of In $3d_{5/2}$ CLs were fitted with two components at BEs of 443.88 eV and 444.51 eV for (110) sample (Figure 6.4 (d)), 443.85 eV and 444.58 eV for (110F) sample (Figure 6.4 (e)), and 443.88 eV and 444.74 eV for (110HTH) sample (Figure 6.4 (f)), which are the peaks corresponding to bulk and its oxide, respectively. The difference in BEs between InO_x and main InGaAs substrate peak is 0.63 eV for (110) sample, 0.73 eV for (110F) sample, and 0.86 eV for (110HTH) sample. It can be seen that the In in InGaAs is significantly oxidised after HfO_2 deposition.

As 3d XPS CLs for HfO_2/(100 and 110) InGaAs samples prepared under different conditions are shown in Figure 6.5. Figures 6.5 (a)-(c) show As 3d CL spectra for HfO_2/(100) InGaAs samples in which the line shapes can be deconvoluted into five

peaks corresponding to the main component of InGaAs substrate at BE of 40.47 eV and 41.17 eV (As 3d doublet of 5/2 and 3/2); a sub-peak present on the higher BE side to the main component As 3d CL referring to As-O at BE of 43.84 eV and 44.54 eV (As 3d doublet of 5/2 and 3/2); and other component from Hf $5p_{1/2}$ at BE of 39.27 eV. Previous work has reported BEs of 40.82 eV and 41.52 eV as InGaAs substrate peaks related to As $3d_{5/2}$ and As $3d_{3/2}$, while the one shifted to higher BE of 3.58 eV from the bulk corresponds to As_2O_5 [339]. In this work, the BE shifts towards higher BE of 3.4 eV ± 0.1 eV, being in agreement with literature values of ~3.4 eV [96] and 3.5 eV [341]; the latter peaks are assigned to As_2O_3 [341].

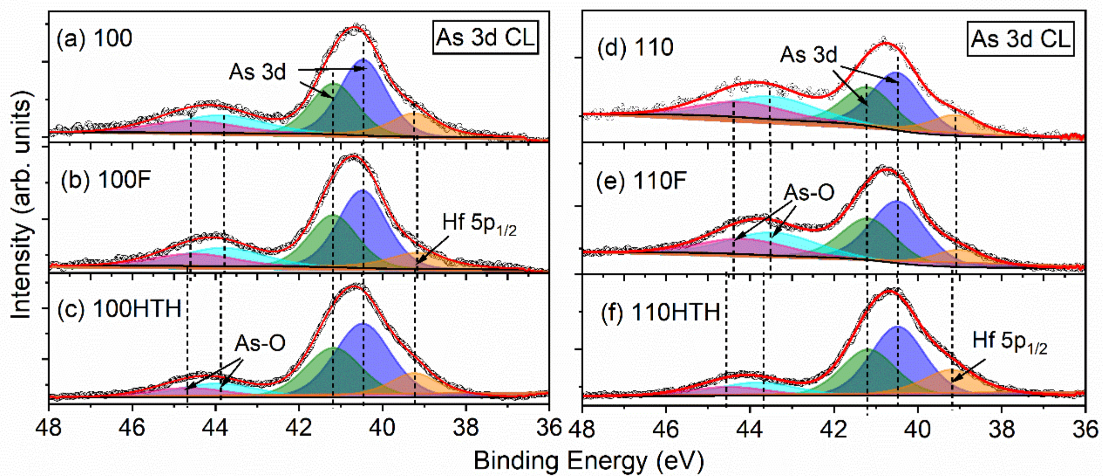

Figure 6.5: The deconvoluted XPS spectra of As 3d CL under different surface treatments for HfO_2/(100) InGaAs samples: (a) 100, (b) 100F and (c) 100HTH; in comparison to HfO_2/(110) InGaAs samples: (d) 110, (e) 110F and (f) 100HTH.

Similarly for HfO_2/(110) InGaAs samples (Figures 6.5 (d)-(f)) the line shapes can also be fitted with peaks corresponding to InGaAs substrate at BEs of 40.47 and 41.17 eV (As 3d doublet of 5/2 and 3/2); non stoichiometric AsO_x at BEs of 43.51 eV and 44.21 eV (As 3d doublet of 5/2 and 3/2); and other component from Hf $5p_{1/2}$ at BE of 39.09 eV. The oxide is shifted to 3.03–3.33 eV in these samples, close to the value seen for the (100) samples.

Table 6.2 shows the ratio of the surface oxides accounted for the In and As atoms after surface treatments, which are obtained by calculating the oxide and InGaAs peak areas. It has been found that the intensity ratio of In-O to InGaAs substrate is slightly higher for (110) sample as compared to (100) sample. This ratio remains constant after FGA treatment as well as after the additional plasma treatment on (100) InGaAs. However, for (110) orientation samples, the ratio is slightly reduced after FGA treatment, and decreases significantly when InGaAs surface is subjected to plasma treatment.

Table 6.2: Comparison of XPS intensity ratios for the In-O/In $3d_{5/2}$ and As-O/As 3d for the set of samples of HfO_2/(100) and (110) InGaAs prepared under different conditions.

Sample	In-O/InGaAs	As-O/InGaAs
100	2.08	0.43
100F	2.08	0.39
100HTH	2.07	0.26
110	2.48	0.67
110F	2.40	0.58
110HTH	2.23	0.24

The most notable difference for the two substrate orientations can be observed in the area of the As-O sub-peak, where the ratio of As-O to InGaAs substrate peak for HfO_2/(110) InGaAs samples is higher compared to HfO_2/(100) InGaAs samples as shown in Table 6.2. This ratio is slightly reduced for both (100) and (110) samples after FGA. It can be seen that plasma based surface pre-cleaning using H_2/TMA/H_2 is more effective in reducing AsO_x for HfO_2/(110) InGaAs than for HfO_2/(100) InGaAs sample.

For HfO_2/(100 and 110) InGaAs samples, the HfO_2 overlayer meant that Ga 2p CL spectra could not be detected accurately due to the lower electron mean free path. As shown in Figure 6.6, the peak was too small for HfO_2/InGaAs samples to be able to fit. Some difference can be seen in the Ga $2p_{3/2}$ peak in Figure 6.6. The Ga $2p_{3/2}$ regions are broadened for the FGA samples. This could indicate a small amount of Ga_2O_3 present in HfO_2/InGaAs FGA samples. For the blanket InGaAs samples, (110) orientation seems to be more prone to oxygen, i.e. more oxidized than (100) as the sub-peak to Ga $2p_{3/2}$ CL which refers to Ga-O bond is more pronounced for (110) orientation than for (100) as seen in Figures 6.3 (c) and (d).

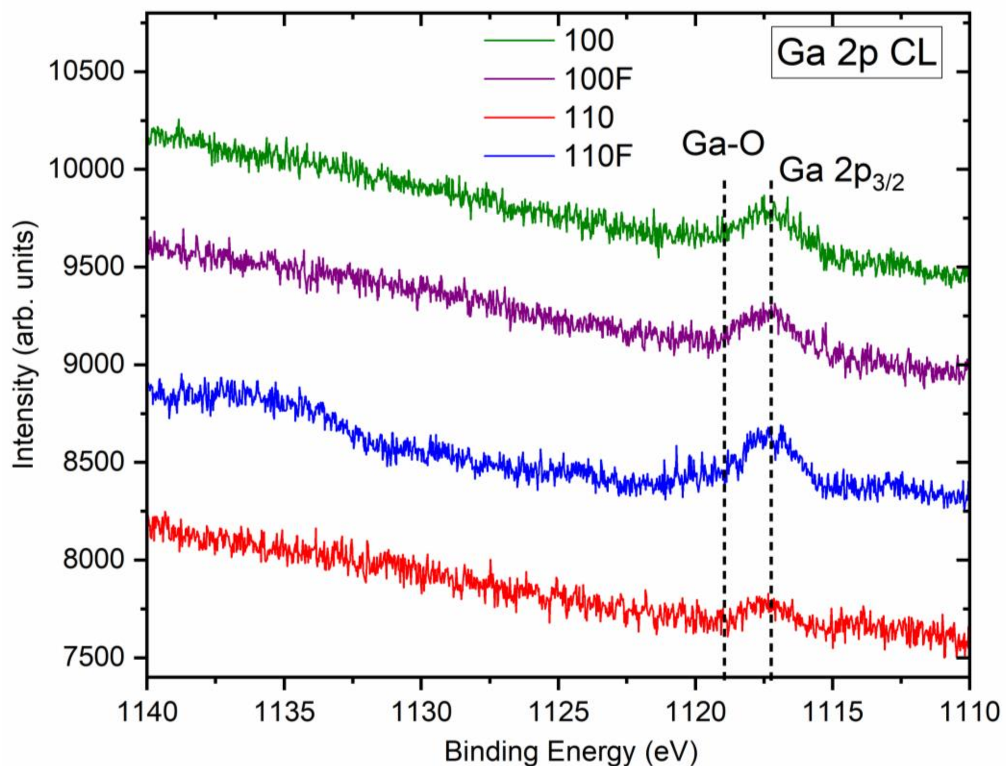

Figure 6.6: Ga 2p XPS CL for HfO_2/(100) and (110) InGaAs samples w/ and w/o FGA.

6.2.3 The correlation between XPS analysis and electrical results

Figures 6.7 (a)-(c) show the capacitance-voltage (*CV*) plots measured at room temperature for HfO_2/(100) InGaAs samples after different conditions: without FGA

(100) control sample, with FGA (100F), with both H_2/TMA/H_2 pre-cleaning and FGA (100HTH). Figures 6.8 (a)-(c) show the *CV* plots measured at room temperature for referring samples but on (110) InGaAs. It can be observed from Figures 6.7 (a) and 6.8 (a) that the (110) control sample has larger etch damage than the (100) sample. These electrical results show a difference between MOS-capacitors processed on (100) and (110) substrates that have been identically fabricated with blanket plasma etching using a $Cl_2/CH_4/H_2$ of InGaAs followed by in-situ high-*k* (HfO_2)-ALD deposition. From the XPS analysis of In $3d_{5/2}$ (Figures 6.4 (a) and (d)) and As 3d (Figures 6.5 (a) and (d)) CLs, it seems that the InO_x and AsO_x are more pronounced for the (110) sample compared to (100) sample.

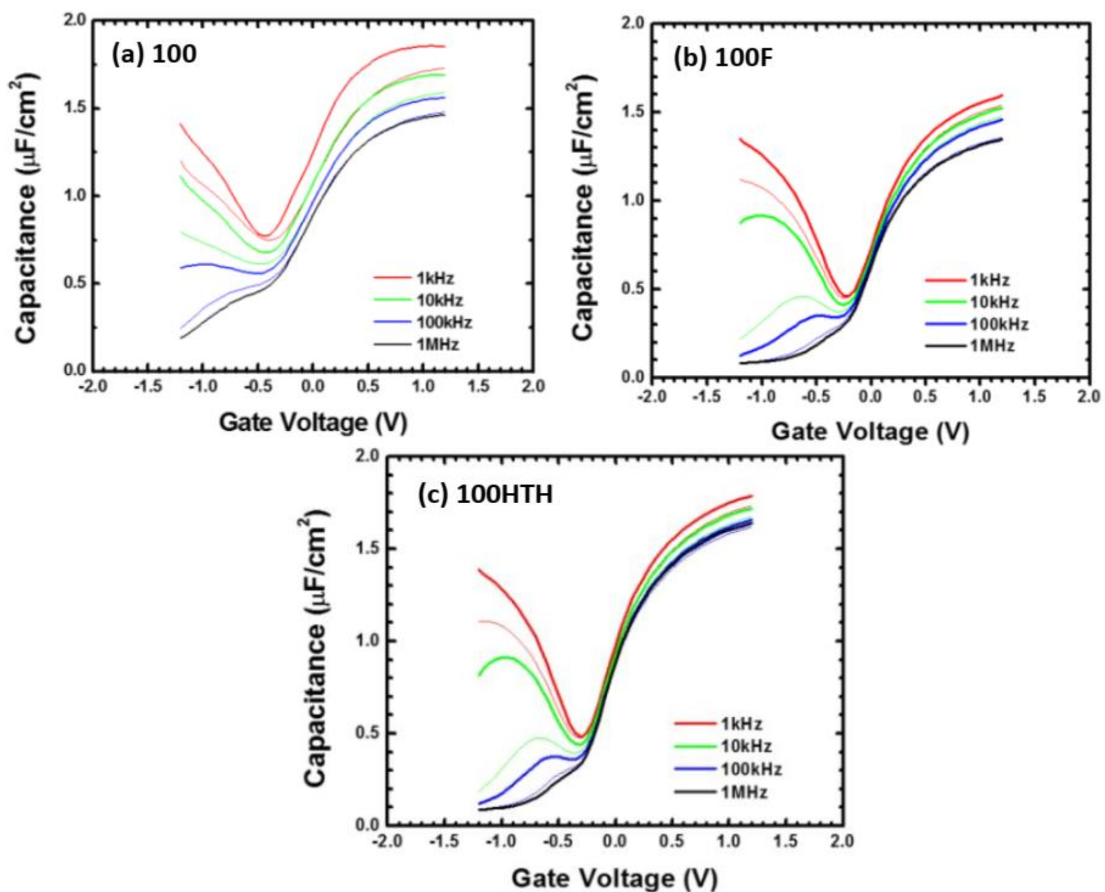

Figure 6.7: Room-temperature high frequency *CV* plots of Au/Pt/HfO_2/(100) *n*-InGaAs/InP MOS capacitors: (a) (100) control sample w/o FGA, (b) (100F) with FGA, and (c) (100HTH) plasma based surface pre-cleaning and FGA [325].

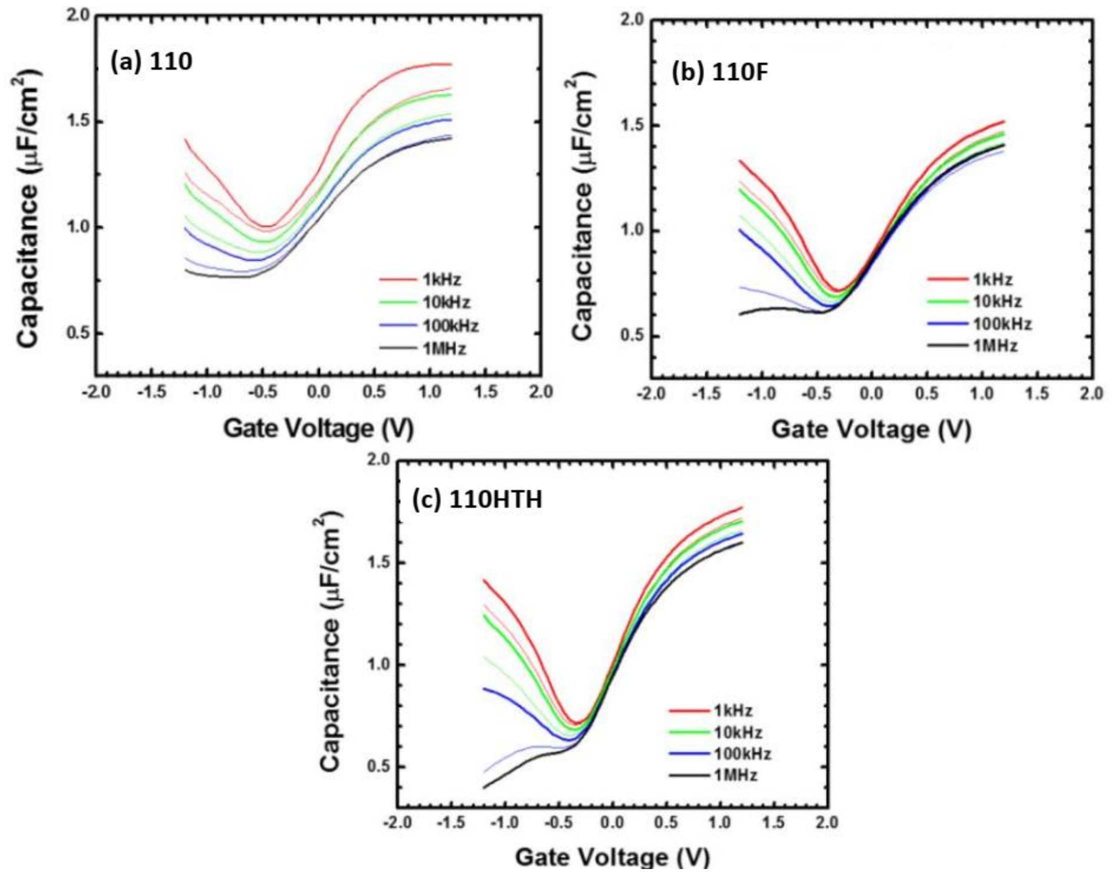

Figure 6.8: Room-temperature high frequency *CV* plots of Au/Pt/HfO_2/(110) *n*-InGaAs/InP MOS capacitors: (a) (110) control sample w/o FGA, (b) (110F) with FGA, and (c) (110HTH) plasma based surface pre-cleaning and FGA [325].

Figures 6.7 (b) and 6.8 (b) indicate that the FGA improves the *CV* response for both (100F) and (110F) samples. In correlation with XPS analysis, both (100F) and (110F) samples show the AsO_x being slightly reduced after FGA, while InO_x remains constant for (100F) sample only. Previous work [342] on HfO_2/(100) InGaAs suggests that the formation of As_2O_3 and Ga_2O_3 are important for interface passivation leading to improved *CV* characteristics. Considering (100) and (100F) samples, it appears from XPS spectra in Figure 6.6 that there is a broadening of the Ga $2p_{3/2}$ region after FGA, which could indicate a small amount of Ga_2O_3. This appears to be fairly consistent with the findings in [342]. Considering (110) and (110F), it appears from XPS that the area of AsO_x is significantly reduced after FGA and also appears to be smaller than for (100F) sample. However, the Ga $2p_{3/2}$ region is broadened after FGA, again indicating

a small amount of Ga_2O_3. Despite the reduction of the AsO_x area peak, there is an improvement in the electrical results after FGA.

In addition, by comparing Figures 6.7 (b) and (c), the in-situ etched (100) InGaAs MOS-capacitors have a slight reduction in frequency dispersion and bumps around mid-gap when plasma-based surface pre-cleaning using H_2/TMA/H_2 step was used + FGA treatment. This result indicates that H_2/TMA/H_2 and FGA treatment does not appear to have a large impact on *CV* apart from an increase in accumulation capacitance on (100HTH) sample. However, (110HTH) sample has shown a significant improvement in both parameters of the *CV* response and the accumulation capacitance (see Figures 6.8 (b) and (c)). The metrics of frequency dispersion in accumulation (C_{acc}), stretch-out (*dC/dV*) and hysteresis for (100HTH) and (110HTH) samples together with their percentage variations in comparison to the control capacitors are given in Table 6.3 [325]. It can be seen that using plasma H_2/TMA/H_2 pre-cleaning treatment increases *dC/dV* for ~17% and ~49% for (100HTH) and (110HTH) samples in comparison to both control (100) and (110) samples, respectively. Therefore, the electrical results indicate that the addition of the plasma H_2/TMA/H_2 pre-cleaning is very effective in recovering etch damage on both oriented InGaAs substrates, especially for (110) sample. In terms of XPS, it has been apparent that InO_x is less affected by substrate orientation than AsO_x, where more pronounced change has been observed for substrates of different orientation (an increase from (100) to (110)) and for samples with FGA and H_2/TMA/H_2 pre-cleaning step + FGA (in both cases, a reduction of AsO_x has been observed in comparison to control samples). There seems to be a strong correlation between a reduction of AsO_x and improvement of *CV* characteristics, which is an interesting observation contrary to the findings in [342].

Table 6.3: The analysis of frequency dispersion in accumulation (C_{acc}), stretch-out (dC/dV) and hysteresis of Au/Pt/HfO_2/(100 and 110)-oriented *n*-InGaAs/InP MOS-capacitors with their percentage variation of the metrics with respect to the control MOS capacitors [325].

Capacitor	C_{acc} *(% dec)*		*dC/dV at 1kHz*		*Hysteresis at 1MHz*	
	% dec	% variation	$\times 10^{-6}$ ($Fcm^{-2}V^{-1}$)	% variation	mV	% variation
100	5.21		1.87		68.5	
100HTH	2.78	−46.6	2.19	+17.0	65.1	+20.8
110	2.45		0.92		68.3	
110HTH	3.24	+32.3	1.37	+48.8	59.0	−13.7

6.3 InGaSb surface treatments

Antimonide-based compound semiconductors have recently emerged as a potential candidate for replacement of silicon in future high-performance, low power CMOS technologies, due to its excellent electron and hole transport properties [103], [117]. Both *n*- and *p*-channel devices of high performance have been demonstrated [110]–[112], [343], [344]. It has been recently shown that, qualitatively, surface treatments comprising a combination of ex-situ HCl treatment and in-situ H_2 plasma exposure prior to the ALD of Al_2O_3 gate dielectric yield significant improvement to the electrical properties of the $In_{0.3}Ga_{0.7}Sb$-Al_2O_3 interface [111], [112]. In this work, the chemical composition of the Al_2O_3/$In_{0.3}Ga_{0.7}Sb$ interface has been analysed by X-ray photoelectron spectroscopy, scanning transmission electron microscopy (STEM) and energy dispersive X-ray (EDX) spectroscopy.

6.3.1 Experimental details on surface and sample preparation

$In_{0.3}Ga_{0.7}Sb$ epitaxial layers were grown by Molecular Beam Epitaxy (MBE) on GaAs (100) substrates. The complete layer structure of the InGaSb samples used for the H_2 plasma power treatment is shown in Figure 6.9 (a) and comprised: (i) a semi-insulating (SI) GaAs (100) substrate; (ii) 250 nm GaAs regrowth and a 200 nm GaSb relaxed buffer layer, both of which were unintentionally doped; (iii) a 3 μm $In_{0.3}Ga_{0.7}Sb$ buffer layer, uniformly doped at a nominal value of 1×10^{18} cm^{-3}; and (iv) a 500 nm $In_{0.3}Ga_{0.7}Sb$ capacitor layer, uniformly doped at a nominal value of 2×10^{17} cm^{-3}. Both *p* and *n*-type variants were grown, for which beryllium and tellurium were the dopant elements, respectively. Prior to H_2 plasma exposure, all samples were subjected to an ex-situ HCl acid surface clean (HCl:H_2O, 1:2, for 3 minutes, followed by an isopropyl alcohol (IPA) rinse) and subsequently loaded into a central vacuum load lock, which is part of a clustered inductively coupled plasma – reactive ion etching (ICP-RIE) and ALD tool. The samples were transferred to the load lock in less than 1 minute. For the investigation into the effect of H_2 plasma power, the ICP-RIE parameters were as follows: H_2:Ar (1:7) plasma chemistry, 90 mT chamber pressure, 30 minute exposure time, 150 °C platen temperature, and 2 W platen power. The exposure time and temperature were based on promising results on GaSb [102]. The platen power was fixed at 2 W to minimise the DC self-bias and thus minimise any damage to the semiconductor surface due to sputtering. A control sample, subsequently referred to as 0 W, was included which had no plasma exposure and was used to compare with samples processed with ICP powers of 150 W and 250 W. Following H_2 plasma treatment, samples were transferred under vacuum to the ALD chamber where Al_2O_3 was deposited via a thermal process at 200 °*C*, comprising 80 alternating cycles of TMA and H_2O exposure. Prior to Al_2O_3 deposition, the samples

were processed with in-situ trimethyl-aluminium (TMA) pre-pulses (30 cycles, 20 ms TMA exposure, 3 s Ar purge) which have demonstrated self-cleaning properties on GaSb [345] and on other III-Vs [95]. MOS-capacitors (MOSCAPs) were fabricated with circular gate diameters ranging from 50 to 250 μm in size. The gate metal (20 nm Ti/ 200 nm Pt) was deposited by e-beam evaporation through a shadow mask. For the power series, Ti/Pt/Au (30 nm/50 nm/100 nm) top ohmic contacts were formed via photolithography, Al_2O_3 dry etch using SF_6 chemistry, and contact deposition by e-beam evaporation and lift off. Figure 6.9 (b) shows the process flow of Al_2O_3-based InGaSb MOSCAP samples. Yen Chun from School of Engineering, University of Glasgow, UK is acknowledged for his contribution in the sample preparation as well as the electrical measurements. Meanwhile, we have done the XPS measurements in the Department of Physics and Stephenson Institute for Renewable Energy, University of Liverpool, UK.

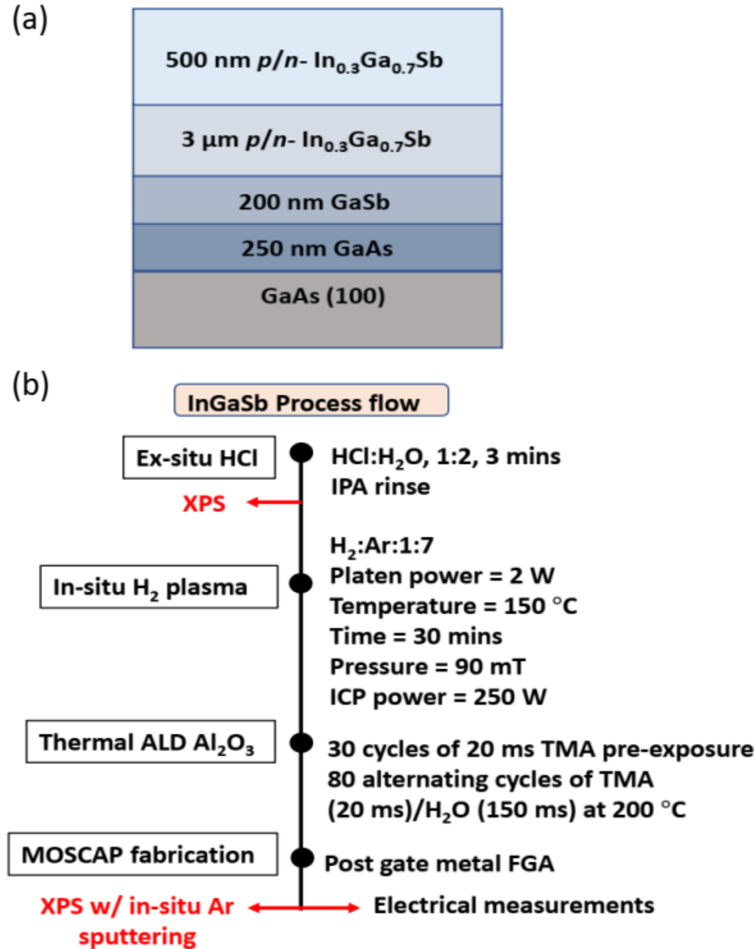

Figure 6.9: (a) The layer structure of the InGaSb samples; (b) the process flow depicting surface treatments used on InGaSb samples followed by fabrication of Al_2O_3-based MOSCAPs.

6.3.2 Experimental details on XPS measurements

The *n*- and *p*-type $In_{0.3}Ga_{0.7}Sb$ substrates were subjected to a wet HCl chemical clean ($HCl:H_2O$, 1:2) for 3 minutes, followed by an IPA rinse for 15 minutes and subsequently loaded into a high vacuum of an XPS system. As control samples, a native *n*- and *p*-type $In_{0.3}Ga_{0.7}Sb$ surfaces exposed to air, were used. To analyse the impact of $In_{0.3}Ga_{0.7}Sb$ surface H_2 plasma exposure, the Al_2O_3 oxide of the 250 W sample was thinned to approximately 4 nm using an in-situ Ar sputtering. The measurements involved XPS depth profiling using an Ar ion beam of energy 500 eV and 10 µA flux. The sputtering rate was 0.032 nm/min. The XPS measurement was

performed using non-monochromatic Al Kα (1486.6 eV) radiation as the source operated at a power of 144 W. The spectrometer consisted of a Scienta SE S200 hemispherical electron energy analyser which was operated such that the resolution was 0.2 eV. All the spectra were fitted with Gaussian-Lorentzian lineshapes after Shirley-type background subtraction. For InGaSb substrates, the binding energies were calibrated to the C 1s peak (present due to the stray carbon impurities) at 284.6 eV. Then, for Al_2O_3/InGaSb samples for all core level spectra was corrected by setting the Au $4f_{7/2}$ CL at 84 eV (present due to the contacts of the samples).

6.3.2.1 *Effect of HCl surface treatment on n- and p-InGaSb*

Comparison between the In $3d_{5/2}$, Ga $2p_{3/2}$, and Sb $3d_{3/2}$ core level spectra for *n*-type $In_{0.3}Ga_{0.7}Sb$ surface exposed to air and after the HCl treated surface is shown in Figure 6.10. The In $3d_{5/2}$ CL (Figure 6.10 (a)) of as-received InGaSb sample can be fitted with the main peak corresponding to InGaSb at the BE of 444.1 eV which is in close agreement with reported values of 444.3 eV for InSb [346]. A broad peak is observed at BE of 444.9 eV corresponding to the In-O bond which can be attributed to In_2O_3, which has been shown to exist at approximately +0.9 eV from the In $3d_{5/2}$ peak [347], [348].On the other hand, the Ga $2p_{3/2}$ peak (Figure 6.10 (b)) is evident at 1116.8 eV, in addition to a broad higher BE component at 1117.9 eV corresponding to the Ga-O bond. The energy range corresponding to the Sb $3d_{3/2}$ CL spectrum was measured rather than Sb $3d_{5/2}$ in order to avoid the overlap of O 1s and Sb $3d_{5/2}$ peaks. The Sb $3d_{3/2}$ CL (Figure 6.9 (c)) can be seen at 537.13 eV which is close to previously reported value of 537.17 eV for InSb [349], as well an associated oxide feature at an offset of +2.6 eV. Investigations into the oxide composition of the native GaSb surface have reported an Sb-O peak with a chemical shift from the bulk of ~3.0 eV, which has been

shown to comprise of Sb_2O_3 and Sb_2O_4 components at +2.5 and +3.1 eV respectively [350]. The oxide feature situated at +2.6 eV from the Sb $3d_{3/2}$ lineshape for the native InGaSb surface in Figure 6.10 (c), therefore appears to correspond predominantly to a Sb_2O_3 sub-oxide phase.

Cleaning the n-type $In_{0.3}Ga_{0.7}Sb$ surface with HCl reduces all In, Ga and Sb sub-oxides, with Ga-O remaining the most prominent as shown in Figures 6.10 (a)-(c) respectively. The Ga-O peak shifts by ~0.4 eV to a higher BE of 1118.3 eV, in agreement with reported values for Ga_2O_3 [351]. Note that the broad peak at a lower BE for the native surface in Figure 6.10 (b) is indicative of the presence of non-stoichiometric disordered GaO_x before the HCl treatment. After the HCl treatment, the oxide peak corresponds to Ga_2O_3. The ratio of the surface oxides (referring to the InO_x, GaO_x and SbO_x) to pure (main) InGaSb peak area for different samples is shown in Table 6.4. It can be seen that the intensity ratios for In-O, Ga-O and Sb-O to the bulk InGaSb are decreased from 0.72 to 0.39, 8.18 to 0.98 and 0.97 to 0.13, respectively after the HCl surface treatment (see Table 6.4).

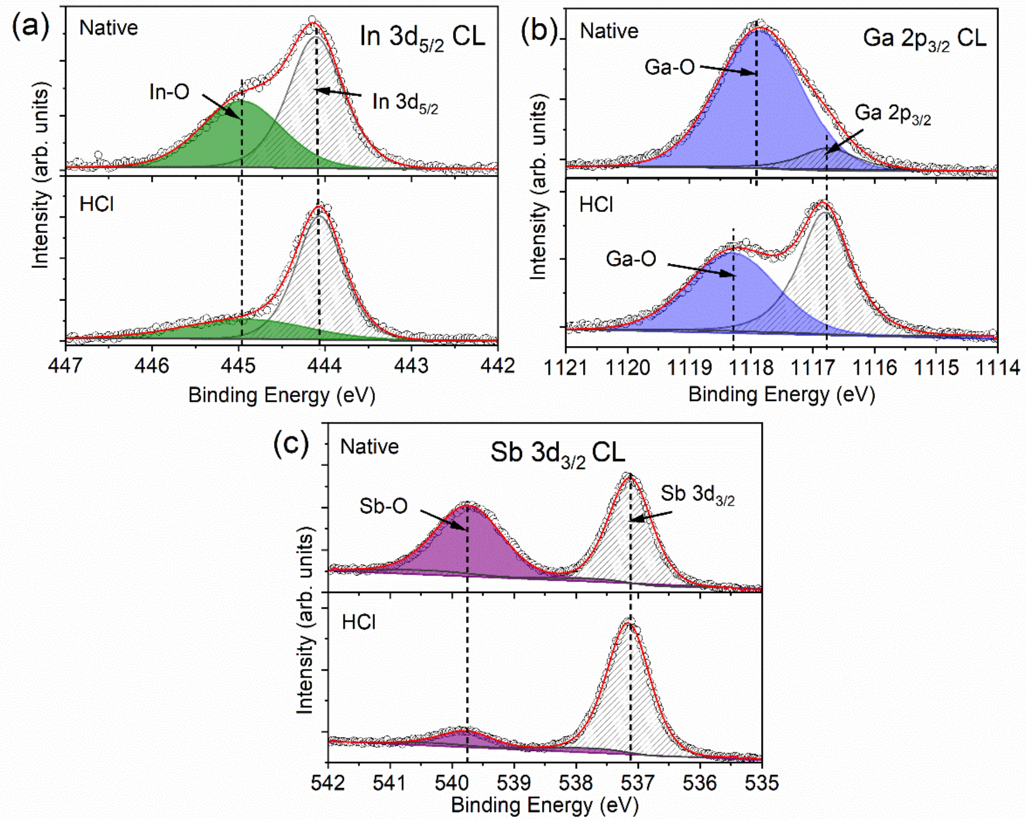

Figure 6.10: The deconvoluted XPS spectra of (a) In $3d_{5/2}$, (b) Ga $2p_{3/2}$ and (c) Sb $3d_{3/2}$ CLs for *n*-type $In_{0.3}Ga_{0.7}Sb$ before and after HCl cleaning.

Figure 6.11 shows the comparison between the In $3d_{5/2}$, Ga $2p_{3/2}$, and Sb $3d_{3/2}$ core level spectra for *p*-type $In_{0.3}Ga_{0.7}Sb$ surface exposed to air and after HCl treatment. The In $3d_{5/2}$ CL (Figure 6.11 (a)) of as-received InGaSb sample can be fitted with the main peak corresponding to InGaSb with the BE of 444.03 eV and a broad peak at BE of 444.89 eV attributed mainly to In_2O_3. On the other hand, the Ga $2p_{3/2}$ CL spectra (Figure 6.11 (b)) can be fitted with two peaks at 1116.80 and 1117.78 eV which are associated to Ga in InGaSb and Ga-O bond, respectively. Sb $3d_{3/2}$ CL spectra (Figure 6.11 (c)) can be fitted with two peaks at 537.1 eV and 539.7 eV which are associated to Sb in InGaSb and Sb_2O_3 respectively.

Similar to the case of *n*-type $In_{0.3}Ga_{0.7}Sb$, the HCl treatment of *p*-type $In_{0.3}Ga_{0.7}Sb$ surface effectively decreases the In-O, Ga-O and Sb-O as shown in Figure

6.10 and Table 6.4. In comparison to *n*-type $In_{0.3}Ga_{0.7}Sb$, there is more InO_x and SbO_x on the surface of *p*-type $In_{0.3}Ga_{0.7}Sb$ and slightly less GaO_x. Furthermore, the HCl is more efficient in reducing InO_x on p-type $In_{0.3}Ga_{0.7}Sb$ (only 19% left on the surface after HCl treatment) than on *n*-type $In_{0.3}Ga_{0.7}Sb$ (~54% left on the surface after HCl). The reduction of GaO_x and SbO_x is similar for both n- and p-type $In_{0.3}Ga_{0.7}Sb$ after HCl treatment and ranges from 12-14% (Table 6.4).

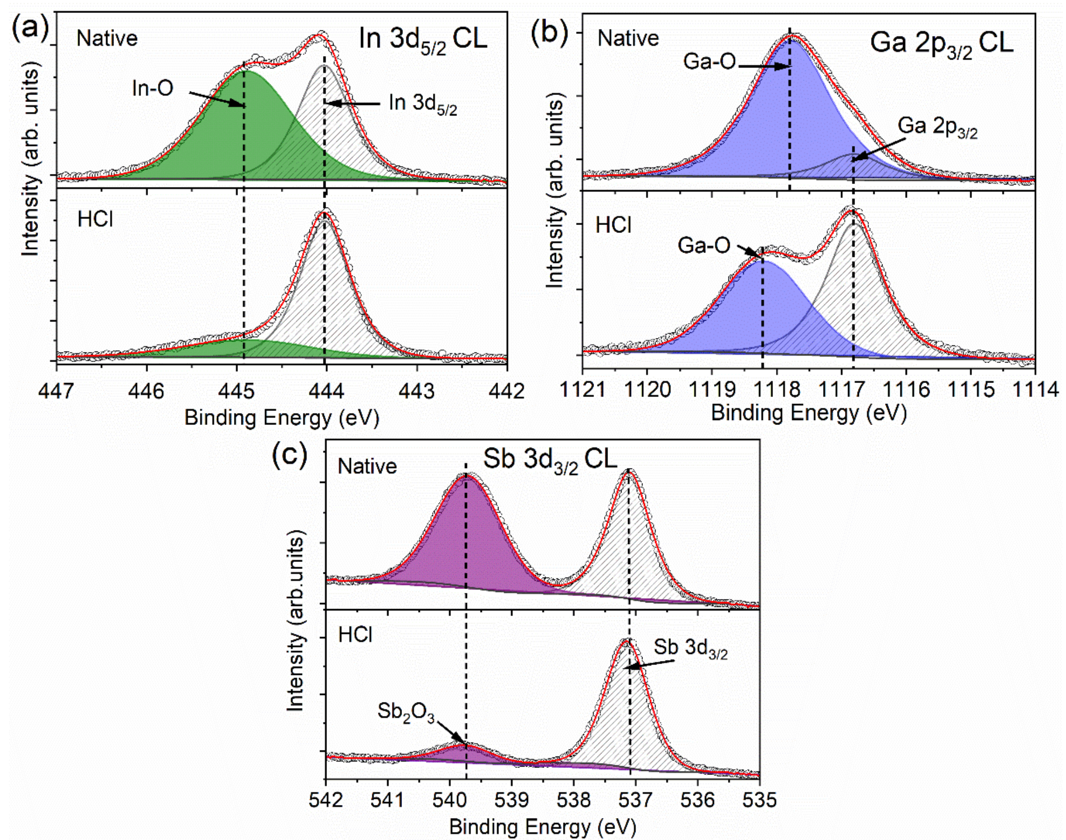

Figure 6.11: The deconvoluted XPS spectra of (a) In $3d_{5/2}$, (b) Ga $2p_{3/2}$ and (c) Sb $3d_{3/2}$ CLs for *p*-type $In_{0.3}Ga_{0.7}Sb$ before and after HCl cleaning.

6.3.2.2 *Effect of HCl and H_2 plasma exposure on Al_2O_3/n-InGaSb interface*

To analyse the impact of H_2 plasma exposure, the Al_2O_3 of the 250 W sample was thinned to ~ 4 nm using in-situ Ar sputtering. The estimated sputtering rate of 0.032 nm/min is obtained by dividing the nominal thickness of Al_2O_3 (~8 nm) with the

sputtering time of 250 min taken to remove all Al_2O_3. The sputtering time of 200 min was taken to remove all Al_2O_3 for 0 W control sample. Then, the XPS sputtering depth, d, can be obtained by multiplying the sputtering time with the sputtering rate. Since Al 2p CL has an overlapping region with the signal from In 4p, Au 5p, and Pt 4f CLs, Al 2s CL was used for the fitting. Figures 6.12 (a) and (b) show the Al 2s CL spectra for both samples, where n-InGaSb surface was subjected to H_2 plasma power of 0 W (control sample) and 250 W. The Al 2s CL spectra can be fitted with a single peak corresponding to Al_2O_3 at BE of 120.4 eV at d = 0.8 nm for both samples. The BE of Al_2O_3 is slightly varied within the experimental error (± 0.2 eV) which is possibly due to differential charging after sputtering by Ar+ ions. Subsequent spectra at greater sputtering depth could only be fitted by including a second peak corresponding to the appearance of non-stoichiometric Al_2O_x as ion beam reaches interface for both samples as shown in Figures 6.12 (a) and (b). The intensity ratio (Al_2O_x/Al_2O_3) of 0.2 was observed at a depth of 3.5 nm for 250 W sample, while at a greater depth of 4.8 nm for 0 W sample. This indicates that Al_2O_x at the interface is slightly higher for 250 W sample compared to 0 W sample as illustrated in Figure 6.13.

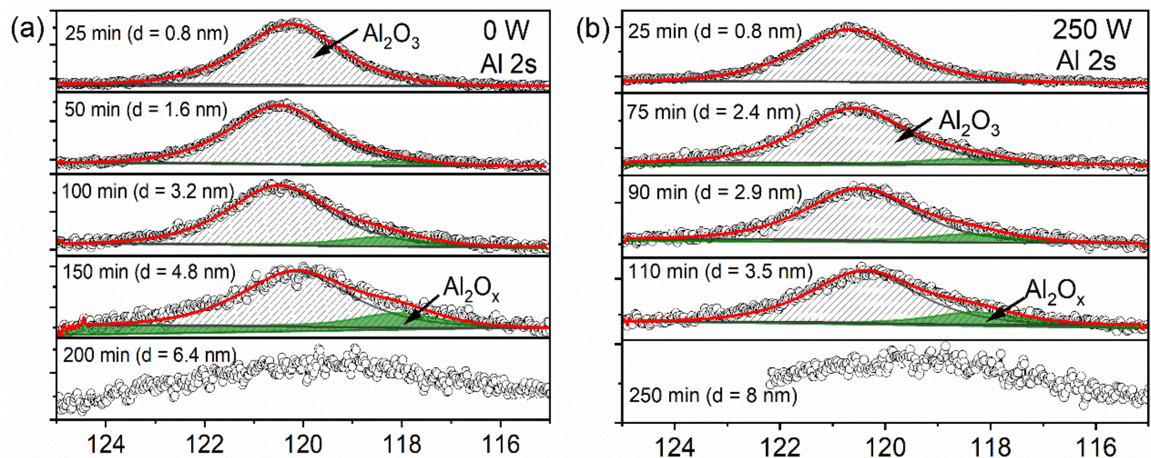

Figure 6.12: The deconvoluted XPS spectra of Al 2s CL for Al_2O_3/InGaSb after HCl and H_2 plasma surface treatments for plasma power of (a) 0 W and (b) 250 W.

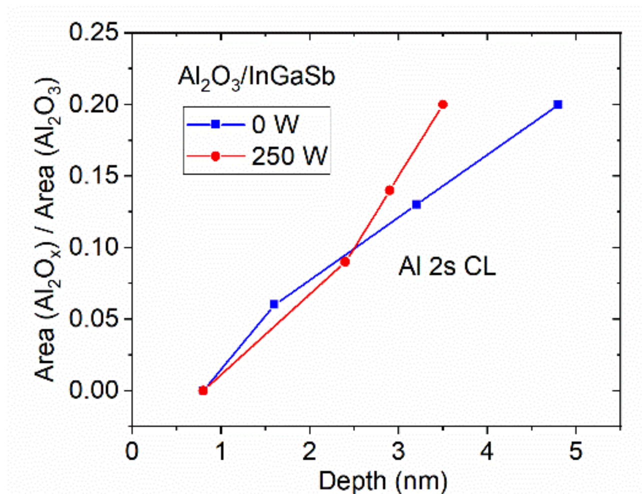

Figure 6.13: The intensity ratio of Al_2O_x/Al_2O_3 for 250 W sample as compared to 0 W sample as a function of XPS sputtering depth.

Figures 6.14 (a) and 6.15 (a) show that In $3d_{5/2}$ CL spectra can be fitted with a single peak corresponding to InGaSb at 444.0 eV. The BE of InGaSb peak is slightly varied within experimental error (± 0.1 eV). HCl and H_2 plasma treatment removes most of the native oxides, and the Al_2O_3 layer does not appear to affect the In in the substrate. Figures 6.14 (b) and 6.15 (b) show that Ga $2p_{3/2}$ CL spectra can be deconvoluted into two peaks at 1116.77 eV corresponding to InGaSb substrate and 1118.27 eV related to Ga_2O_3 [96], [352]. All Al_2O_3 layers are removed with no O 1s visible at the final sputtering time of 200 min (d = 6.4 nm) for 0 W sample (Figure 6.14) and 250 min (d = 8 nm) for 250 W sample (Figure 6.15), however the Ga 2p lineshape still requires fitting with two peaks, at lower BE of 1116.70 eV corresponding to bulk InGaSb, and a small peak at higher BE of 1119.08 eV. The high BE peak is not oxide related but is attributed to sputter damaged Ga on the surface. Moreover, Ga-O appears in both samples with the intensity ratio of Ga-O to InGaSb substrate to be slightly higher for 250 W sample (< 0.1) as compared to 0 W sample (< 0.08). Figures 6.14 (c) and 6.15 (c) show that Sb $3d_{3/2}$ CL spectra can be fitted using a single peak corresponding to bulk InGaSb at 537.2 eV. Al_2O_3 does not appear to affect the Sb in the InGaAs substrate. Table 6.4 shows the comparison of the intensity

ratio of In-O/In $3d_{5/2}$, Ga-O/Ga $2p_{3/2}$, and Sb-O/Sb $3d_{3/2}$ for all samples. It can be concluded from Table 6.4 and Figures. 6.14 and 6.15 that the addition of H_2 plasma surface treatment to HCl results in the complete removal of In and Sb sub-oxides. The Ga $2p_{3/2}$ XPS spectra show Ga_2O_3 to have persisted, however Ga-O:InGaSb ratio has been reduced from 8.18 in the HCl only sample to <0.1 (Table 6.4).

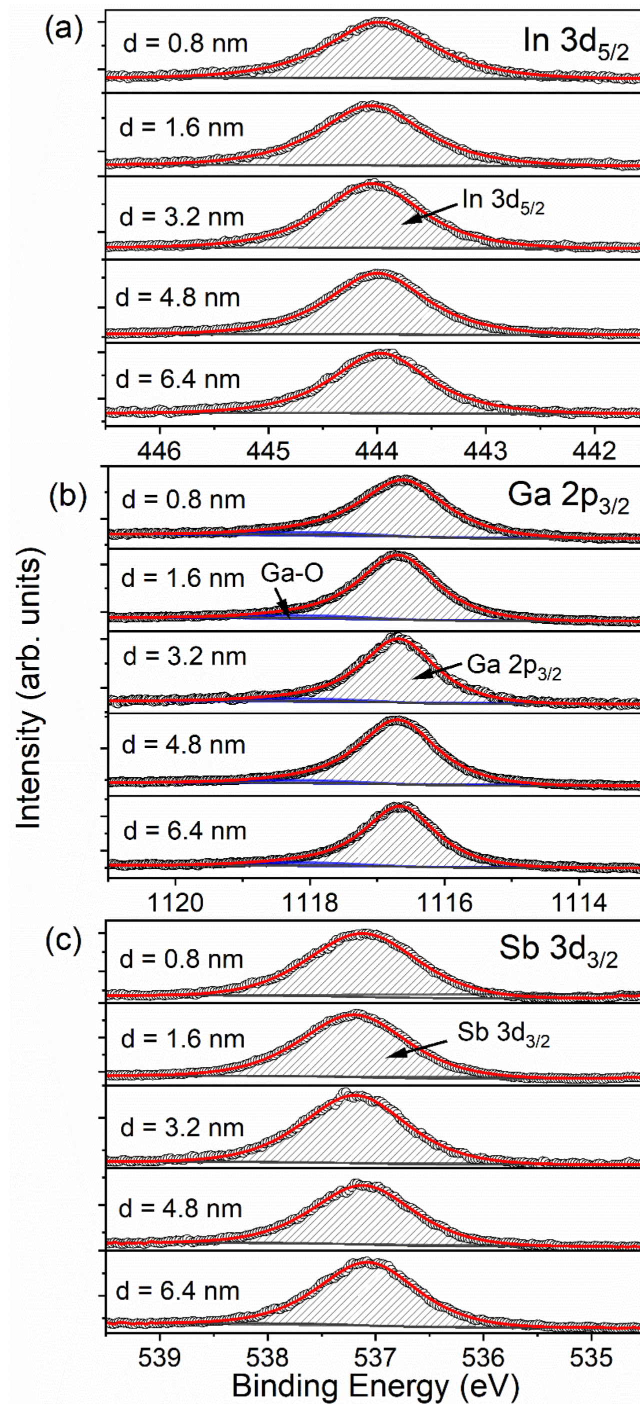

Figure 6.14: The deconvoluted XPS spectra of (a) In $3d_{5/2}$, (b) Ga $2p_{3/2}$ and (c) Sb $3d_{3/2}$ CLs for Al_2O_3/InGaSb (0 W sample) after HCl surface treatment, measured at different sputtering depth from 0.8 to 6.4 nm.

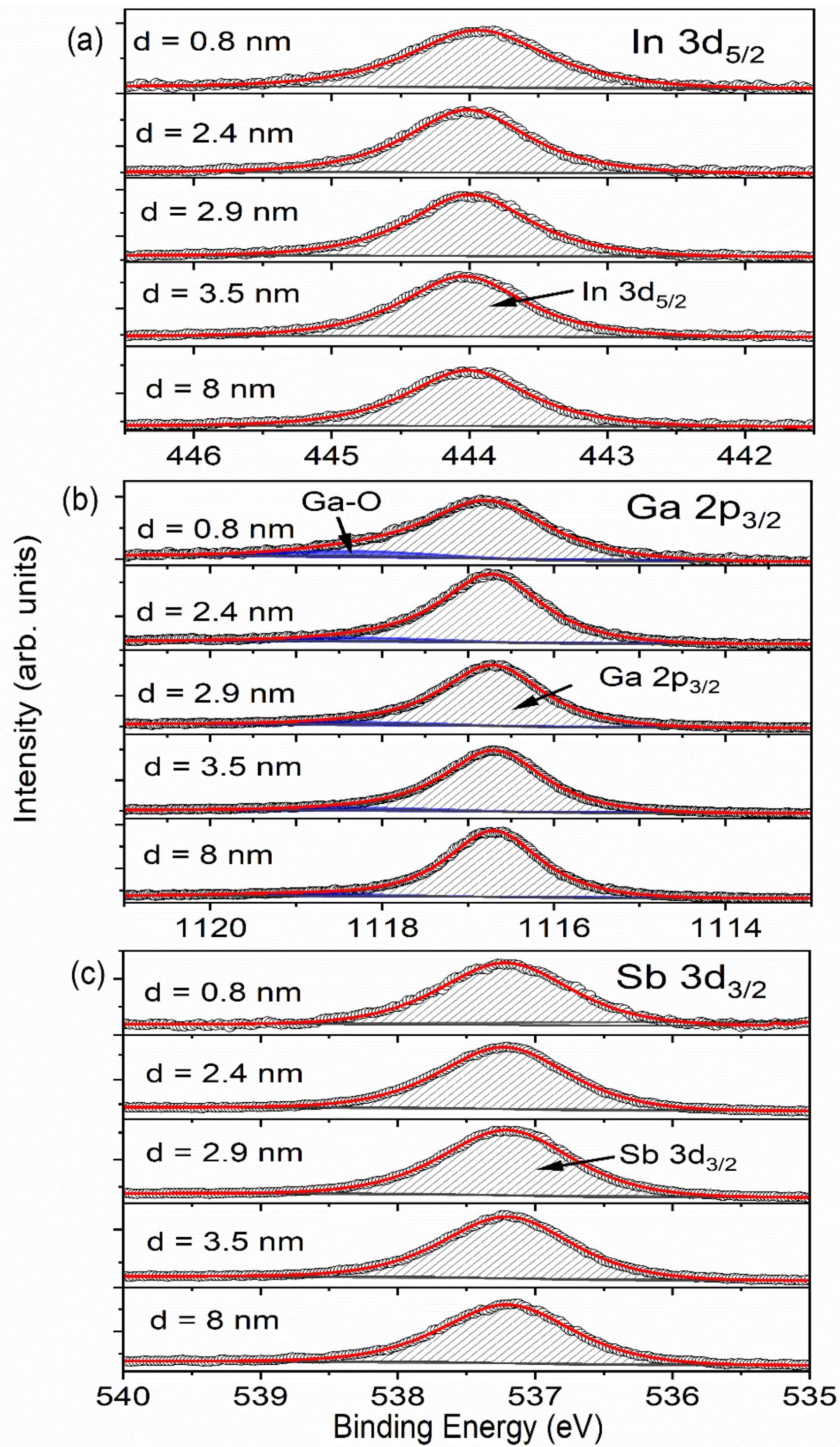

Figure 6.15: The deconvoluted XPS spectra of (a) In $3d_{5/2}$, (b) Ga $2p_{3/2}$ and (c) Sb $3d_{3/2}$ CLs for Al_2O_3/InGaSb (250 W sample) after HCl + H_2 plasma surface treatments, measured at different sputtering depths from 0.8 to 8 nm.

Table 6.4: Comparison of In-O/InGaSb, Ga-O/InGaSb, and Sb-O/InGaSb for all samples.

Sample	In-O/InGaSb	Ga-O/InGaSb	Sb-O/InGaSb
As-received *n*-InGaSb	0.72	8.18	0.97
HCl surface treatment *n*-InGaSb	0.39 (54.2%)	0.98 (12%)	0.13 (13.4%)
HCl + H_2 plasma *n*-InGaSb	0	< 0.1	0
As-received *p*-InGaSb	1.57	6.92	1.28
HCl surface treatment *p*-InGaSb	0.3 (19.1%)	0.96 (13.9%)	0.15 (11.7%)

6.3.3 The correlation between XPS analysis and STEM, EDX and electrical results

STEM and EDX measurements were performed to investigate the chemical composition of the $Al_2O_3/In_{0.3}Ga_{0.7}Sb$ interface. The measurements were performed using a JEOL ARM200F microscope operated at 200 kV and a liquid nitrogen free Si drift detector for sample treated with 150 W plasma power, and post FGA. The images are shown in Figure 6.16. The STEM image of the dielectric interface for the HCl+H_2 plasma sample (Figure 6.16 (a)) reveals the Al_2O_3 to be conformal and approximately 7.4 nm thick, with a 1.4 nm thick interfacial region visible at higher magnification (inset of Figure 6.16 (a)). Also, EDX image reveals the dielectric to be non-stoichiometric, with peaks of Al and O and at both interfaces to the gate metal and InGaSb, where the intermixing between In, Ga and Sb with Al_2O_3 is found within the interfacial layer (Figure 6.16 (b). This observation can be correlated with XPS results shown in Figure 6.12 for $Al_2O_3/In_{0.3}Ga_{0.7}Sb$ interface, where the appearance of slightly non-stoichiometric Al_2O_x was observed as ion beam reaches interface for both 0 W and 250 W samples. However, XPS spectra of Al 2s CL show that the main peak feature is attributed to Al_2O_3 suggesting that the Al_2O_3 is stoichiometric and that it has only a slight effect on Ga at the interface.

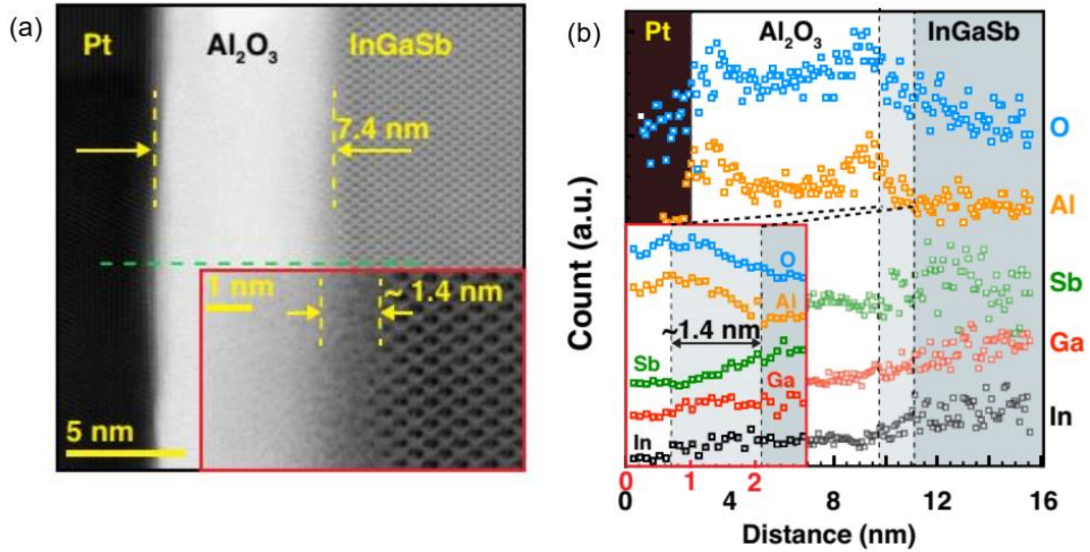

Figure 6.16: (a) STEM image of the Au/Pt/Al_2O_3/$In_{0.3}Ga_{0.7}Sb$ interface treated with HCl+H_2 plasma exposure at 150 W, post FGA; inset image: higher magnification STEM image showing the existence of an interfacial layer approximately 1.4 nm thick and (b) Qualitative EDX line scan over the region marked in green in (a), revealing the oxide to be non-stoichiometric. Inset image: high magnification EDX measurements over the interfacial region, showing intermixing or elemental diffusion of In, Ga, and Sb with the oxide. (courtesy of David A. J. Millar, University of Glasgow UK.)

The impact of plasma power on the electrical properties of the referring MOSCAPs was assessed, with and without a 15 minutes FGA at 350 °C, using room temperature, multifrequency, capacitance-voltage (*CV*) measurements, over a frequency range of 1 kHz to 1 MHz in a dark environment. The results were characterised qualitatively in terms of the following metrics: C_{mod} defined in Eq. (6.1), stretch out, and frequency dispersion in accumulation, which pertain to freedom of Fermi level movement, the magnitude of D_{it} [353], and magnitude of border trap density [354] respectively. C_{mod} can be expressed as:

$$C_{mod} = \left[\left(C_{max,HF} - C_{min,HF}/C_{max,HF}\right)\right] \times 100\% \qquad (6.1)$$

The CV measurements were performed at room temperature using Keysight B1500A semiconductor parameter analyser to investigate the effect of plasma powers of 150 W and 250 W to control 0 W sample.

Figure 6.17 shows the room temperature CV measurements for p-type $Au/Pt/Al_2O_3/In_{0.3}Ga_{0.7}Sb$ samples, processed with and without the FGA, exposed to H_2 plasma powers of 0 W, 150 W, and 250 W, with the corresponding qualitative metrics summarised in Figure 6.18. It should be noted that for ICP powers > 250 W, no capacitance modulation was observed. The combination of H_2 plasma exposure and FGA yield significantly improved metrics over the control sample, with the 150 W plasma treatment giving both the highest C_{mod} and lowest stretch out. For this sample, the FGA increases C_{mod} and $[dC/dV]_{max}$ by 122 % and 176 % respectively. It should be noted that frequency dispersion was extracted over a frequency range of 1 kHz to 100 kHz in order to avoid the impact of series resistance. The latter was found to vary depending on the surface treatment and dominate the dispersion for some samples at high frequency. These electrical results can be correlated with XPS analysis in Table 6.4, where the use of H_2 plasma effectively reduces Ga_2O_3 content and completely removes Sb_2O_3 and In_2O_3 at the surface (leading to improved CV plots, Figures 6.17 (c) and (f)) in comparison to HCl only surface treatment (0 W sample), which shows reduced electrical performance (Figures 6.17 (a) and (d)).

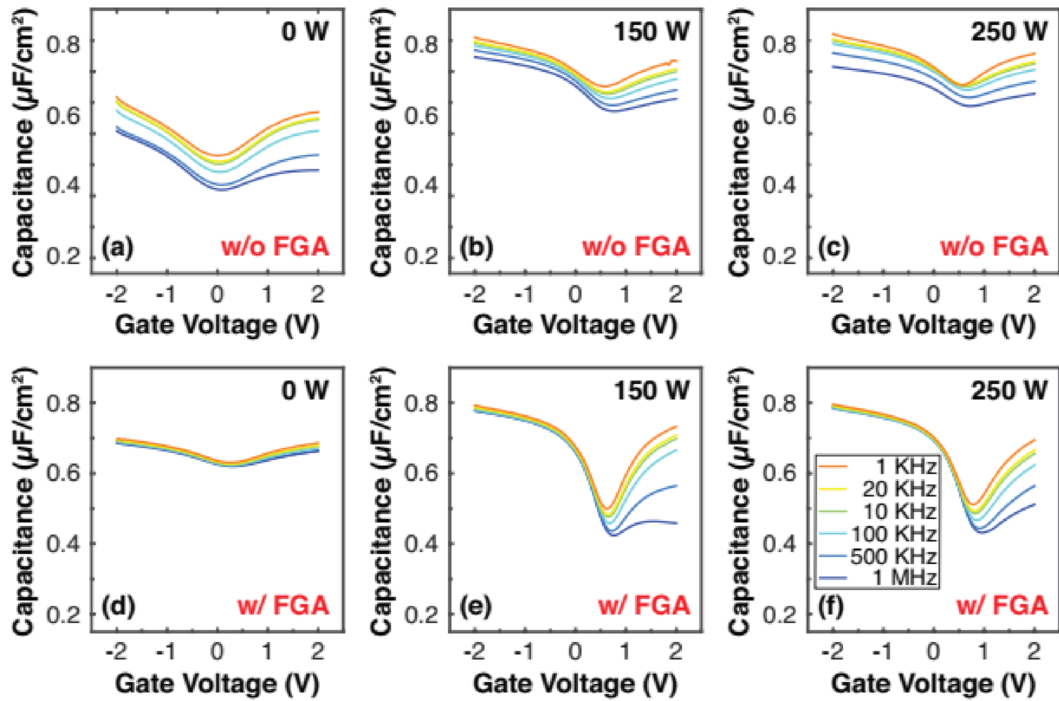

Figure 6.17: Room temperature CV measurements over a frequency range of 1 kHz to 1 MHz for *p*-type Au/Pt/Al_2O_3/$In_{0.3}Ga_{0.7}Sb$ samples, processed with and without a FGA, exposed to H_2 plasma power of (a,d) 0 W, (b,e) 150 W, and (c,f) 250 W. (courtesy of David A. J. Millar, University of Glasgow UK.)

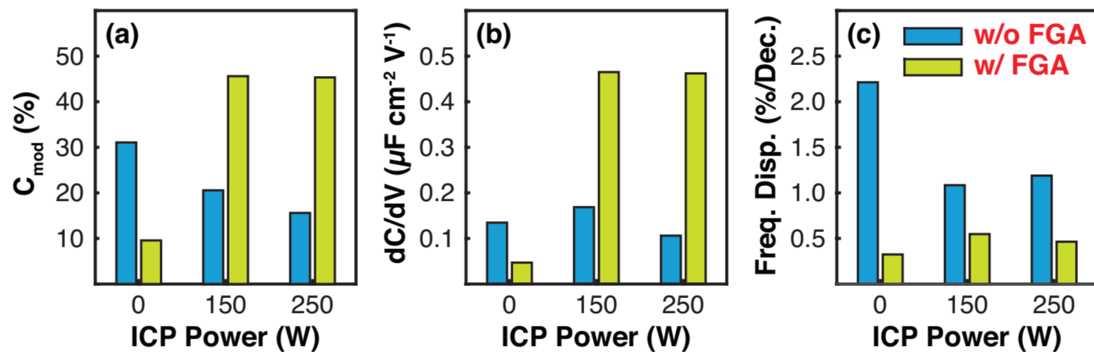

Figure 6.18: (a) Capacitance modulation, C_{mod}, (b) stretch out and (c) frequency dispersion in accumulation for p-type Au/Pt/Al_2O_3/$In_{0.3}Ga_{0.7}Sb$ samples, processed with and without a FGA, exposed to H_2 plasma powers of 0 W (HCl only), 150 W and 250 W (courtesy of David A. J. Millar, University of Glasgow, UK).

6.4 Conclusion

This chapter has shown comprehensive novel study of HfO_2/InGaAs and Al_2O_3/InGaSb interfaces, in particular focusing on the effect of different surface treatments on electrical properties of processed MOSCAP devices. Compares the use of in-situ cyclic plasma N_2/TMA and plasma H_2/TMA processes after ICP etching and prior to ALD deposition of HfO_2. It has been shown that plasma H_2 is effective in recovering the etch damage on both oriented InGaAs layers (100) and (110). The quality of interface between ALD HfO_2/InGaAs has been assessed by X-ray photoelectron spectroscopy, in particular looking into the effect of different substrate orientations (100) and (110) and H_2/TMA/H_2 surface plasma treatment on electrical properties. For the blanket InGaAs samples, (110) orientation has been found to be more prone to oxygen, i.e. more oxidised than (100). The XPS analysis of In $3d_{5/2}$ and As 3d core levels of HfO_2/InGaAs interface shows the presence of both InO_x and AsO_x sub-oxides. It has been found that (110)-oriented InGaAs substrate layer has a higher intensity ratio of In than As sub-oxides indicating that the In is heavily oxidised as compared to As. The most notable difference for the two substrate orientations has been observed in the area of the As-O sub-peak, where the ratio of As-O to InGaAs substrate peak for HfO_2/(110) InGaAs samples is higher compared to HfO_2/(100) InGaAs samples. This ratio has been slightly reduced for both (100) and (110) samples after FGA. Furthermore, the plasma-based surface pre-cleaning using H_2/TMA/H_2 has been found to be more effective in reducing AsO_x for HfO_2/(110) InGaAs than for HfO_2/(100) InGaAs sample. The Ga $2p_{3/2}$ regions are broadened for the FGA samples. This could indicate a small amount of Ga_2O_3 present in HfO_2/InGaAs FGA samples. Despite the reduction of the AsO_x area peak, there has been an improvement in the electrical results for samples after FGA. The addition of the plasma H_2/TMA/H_2 pre-

cleaning has been found to be very effective in recovering etch damage on both oriented InGaAs substrates, especially for (110) sample and led to the improvement of electrical characteristics. In terms of XPS, it has been apparent that InO_x is less affected by substrate orientation than AsO_x, where more pronounced change has been observed for substrates of different orientation (an increase from (100) to (110)) and for samples with FGA and H_2/TMA/H_2 pre-cleaning step + FGA (in both cases, a reduction of AsOx has been observed in comparison to control samples). There seems to be a strong correlation between a reduction of AsO_x and improvement of *CV* characteristics.

Furthermore, the results of the first investigation into the impact of in-situ H_2 plasma exposure on the physical and electrical properties of the Al_2O_3/*p* or *n*-$In_{0.3}Ga_{0.7}Sb$ interface are presented. Samples were processed using a clustered inductively coupled plasma reactive ion etching and atomic layer deposition tool. Metal oxide semiconductor capacitors were fabricated subsequent to H_2 plasma processing (at plasma power of 150 W and 250 W) of InGaSb surface, followed by Al_2O_3 deposition and the corresponding capacitance-voltage plots were measured. X-ray photoelectron spectroscopy analysis of samples processed as part of the plasma power series reveals a combination of ex-situ HCl cleaning and in-situ H_2 plasma exposure to completely remove In and Sb sub oxides, with the Ga-O content reduced to Ga-O:InGaSb < 0.1. The combination of H_2 plasma exposure and FGA yield significantly improved metrics over the control HCl-treated sample, with the 150 W plasma treatment giving both the highest C_{mod} and lowest stretch out.

The results shown in this chapter represent a critical advancement towards achieving III-V CMOS.

CHAPTER 7

Conclusion and future work

The research work presented in this thesis primarily focused on two emerging applications of high-*k* dielectrics, in Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and Metal-Insulator-Semiconductor High Electron Mobility Transistors (MIS-HEMTs). The main aim of this thesis has been to propose the best routes for passivation of semiconductor/high-k oxide interfaces for semiconductor devices by investigating the band alignments and interface properties of several oxides, such as Tm_2O_3, Ta_2O_5, ZrO_2, Al_2O_3 and MgO, deposited on different semiconductors: Si, Ge, GaN, InGaAs and InGaSb. The research in this thesis has made contribution in selection of suitable candidates for future Si, Ge and III-V CMOS devices as well as for GaN-based HEMT technology.

The main results of this thesis are summarised here.

Integration of a high-*k* interfacial layer (IL) has been identified as the most promising route to improve the scalability of high-*k*/metal gate stacks. The favourable properties of Tm_2O_3 in terms of its large band offsets, i.e. valence band offset (VBO) of 2.8 ± 0.2 eV and conduction band offset (CBO) of 1.9 ± 0.2 eV, have been determined using X-ray photoelectron spectroscopy (XPS) measurements and Kraut's method. These large values of band offsets are important to provide a sufficiently high barrier height for both electrons and holes. The TmSiO IL has been successfully grown in the sub-nm/nm regime via thermal reaction of Tm_2O_3 with Si at different post deposition annealing (PDA) temperatures of 550 °C, 650 °C, and 750 °C. The best-scaled stack has been formed at 550 °C with 0.9 nm TmSiO at the interface observed

by high resolution transmission electron microscopy (HRTEM) and revealed a graded interface layer with a strong SiO_x component (Si^{3+} species) by XPS. Annealing at higher PDA temperatures pushes the thickness of IL above 1 nm, and also leads to more Tm-Si-O bonds and less +3 Si oxidation state at the interface. The Tm_2O_3/TmSiO/Si samples which had undergone etching off Tm_2O_3 from the surface and subsequent capping with 3 nm HfO_2 showed no Tm present in the IL, both by XPS and from the elemental depth profiles derived from electron energy loss spectra (EELS). There has been rather thick SiO_2 detected at the interface. This anomaly could be the result of some unintentional error during processing of these stacks, most likely during the etching off Tm_2O_3. The key finding from this study was that the beneficial electrical properties of 550 °C processed TmSiO IL, such as reduced equivalent oxide thickness (EOT), low density of interface states and high channel mobility, could be ascribed to graded Si 3+ rich interface. Therefore, TmSiO IL could be a promising candidate for high-*k* IL integration in future CMOS technology nodes. Furthermore, the XPS results of sub-nm thick TmO_x on Ge deposited by atomic layer deposition using 3 and 7 cycles of Tm precursor, have shown Ge-rich interface and a very small intensity of Tm 4d core level (CL). The latter provided evidence of non-stoichiometric TmO_x. The formation of GeO_x sub oxides have been seen from Ge 3d XPS CL spectra in all (as-deposited and annealed) samples, where Ge +2 and Ge +3 oxidation states are present and have been associated with GeO and Ge_2O_3. Some samples were annealed in O_3 at 350 °C and some in N_2 at 550 °C. A small Ge^{4+} sub-peak, being a signature of GeO_2 at the TmO_x/Ge interface, has been apparent only for samples annealed in O_3. The Ge +2 oxidation state has been found to increase in intensity, while Ge +3 oxidation state decreases slightly for TmO_x/Ge samples when the ALD cycle is

increased from 3 to 7. It can be concluded that 3 and 7 ALD cycles are insufficient to produce stoichiometric Tm_2O_3 films on Ge.

Several high-*k* dielectrics films, such as Ta_2O_5, ZrO_2, Al_2O_3 and MgO, were deposited on GaN using sputtering technique, with the aim of determining their suitability for MIS-HEMT applications in terms of their band alignments on GaN. Prior to oxide deposition, GaN surface was cleaned using the following sequence: acetone for 10 minutes in an ultrasonic bath, 10 minutes in methanol, 20 minutes in 37 % HCl solution and finally a deionised water rinse. The effect of differential charging and band bending at oxide/semiconductor interface has been considered for all samples. The former has been found negligible for Ta_2O_5/GaN and ZrO_2/GaN, while present in case of Al_2O_3/GaN and MgO/GaN and corrected using thickness dependent XPS core level method. Furthermore, band bending has been evaluated from angle resolved XPS data and found to be small upward (0.05 eV) for Ta_2O_5/GaN, while downward (up to 0.3 eV) for ZrO_2, Al_2O_3 and MgO on GaN. Therefore, the corrected VBO values (± 0.25 eV) for Ta_2O_5, ZrO_2, Al_2O_3 and MgO on GaN using Kraut's method were found to be 0.7 eV, 0.4 eV, 1.1 eV and 1.2 eV with corresponding CBOs of 0.4 eV, 1.3 eV, 2.2 eV and 2.8 eV respectively. The band gaps of GaN (3.34 eV) and Ta_2O_5 (4.4 eV) were extracted using variable angle spectroscopic ellipsometry (VASE), whereas the band gaps of ZrO_2 (5.1 eV), Al_2O_3 (6.5 eV) and MgO (7.4 eV) were determined from XPS O 1s energy loss spectroscopy. The band offset results from this study have been critically compared with the literature and indicate intrinsic limitations of using XPS and Kraut's method in evaluating valence band offset in addition to discrepancies induced by various surface cleaning treatments of GaN and different deposition methods used for fabricating oxide materials. The presented band

offset measurements have importance for developing and designing future GaN-based MIS-HEMTs.

The electrical characterisation of MIS-capacitors with different gate dielectrics (Ta_2O_5, ZrO_2, Al_2O_3, and MgO) have also been performed. The leakage current of MOS-capacitors with oxide layers of Ta_2O_5, ZrO_2, Al_2O_3 and MgO at 1 V was found to be 7.7 $\times 10^{-4}$ A/cm^2, 6.2 $\times 10^{-4}$ A/cm^2, 5.3 $\times 10^{-6}$ A/cm^2 and 3.2 $\times 10^{-6}$ A/cm^2 respectively. The band offsets affect the gate leakage current in such a way that it will increase exponentially with their decrease. The results from this work show that devices with MgO as gate dielectric have the lowest leakage current density in agreement with the highest VBO and CBO values of 1.2 eV and 2.8 eV respectively derived by physical characterisation (XPS and VASE). On the contrary, Ta_2O_5-based MOS device has the highest leakage current density which can correlate with both VBO (0.7 eV) and CBO (0.36 eV) being < 1 eV. The analysis of conduction mechanisms using typical *JV* characteristics plotted on log-log scales shows evidence of space-charge-limited current (SCLC) mechanism for all MIS-capacitors, which would indicate that the current flow is inhomogeneous and bulk rather than electrode limited. The latter led to not being able to evaluate barrier heights from Fowler-Nordheim plots and hence compare them with the band offsets determined by physical characterisation using VASE and XPS.

Furthermore, the effect of surface treatments prior to ALD-Al_2O_3 deposition on the GaN/AlGaN/GaN heterostructure have been investigated. GaN surface passivation process based on the octadecanethiol (ODT) treatment has been proposed to improve the Al_2O_3/GaN interface quality. The GaN surface was also treated by HCl and O_2 plasma. According to the XPS results, the re-oxidation was hard to avoid on the HCl treated GaN surface. The O_2 plasma treatment can fill the N vacancies on the

GaN surface by oxygen atoms, whereas the ODT treatment can passivate N vacancies by sulphur atoms and prevent the formation of detrimental native oxide. The MIS-HEMTs fabricated using the low-cost ODT GaN surface treatment have been found to exhibit excellent characteristics which are highly desirable in power switching applications such as a low threshold voltage, V_T, hysteresis of 0.12 V, a small subthreshold slope, SS of 73 mV/dec, and a low density of interface states, D_{it} of 3.0 $\times 10^{12}$ $cm^{-2}eV^{-1}$. The MIS-HEMT devices for Al_2O_3-based with ODT treatment were found to be more effective as compared to ZrO_2-based with ODT treatment in term of its electrical characteristics. ZrO_2-based MIS-HEMTs showed a large negative shift in V_T as well as a higher value of SS after ODT GaN surface treatment.

Finally, a comprehensive novel study of HfO_2/InGaAs and Al_2O_3/InGaSb interfaces have been conducted, in particular focusing on the effect of different surface treatments on electrical properties of processed MOS capacitor devices. The former HfO_2/InGaAs interface study compares the use of in-situ cyclic plasma N_2/TMA and plasma H_2/TMA processes after inductively coupled plasma (ICP) etching and prior to atomic layer deposition (ALD) deposition of HfO_2. It has been shown that plasma H_2 is effective in recovering the etch damage on both oriented InGaAs layers (100) and (110). The quality of interface between ALD HfO_2/InGaAs has been assessed by X-ray photoelectron spectroscopy, in particular looking into the effect of different substrate orientations (100) and (110) and H_2/TMA/H_2 surface plasma treatment on electrical properties. For the blanket InGaAs samples, (110) orientation has been found to be more prone to oxygen, i.e. more oxidised than (100). The XPS analysis of In $3d_{5/2}$ and As 3d core levels of HfO_2/InGaAs interface shows the presence of both InO_x and AsO_x sub-oxides. The most notable difference for the two substrate orientations has been observed in the area of the As-O sub-peak, where the ratio of As-O to InGaAs

substrate peak for HfO_2/(110) InGaAs samples is higher compared to HfO_2/(100) InGaAs samples. This ratio has been slightly reduced for both (100) and (110) samples after forming gas anneal (FGA). Furthermore, the plasma based surface pre-cleaning using H_2/TMA/H_2 has been found to be more effective in reducing AsO_x for HfO_2/(110) InGaAs than for HfO_2/(100) InGaAs sample. The Ga $2p_{3/2}$ regions are broadened for the FGA samples. This could indicate a small amount of Ga_2O_3 present in HfO_2/InGaAs FGA samples. Despite the reduction of the AsO_x area peak, there has been an improvement in the electrical results for samples after FGA. The addition of the plasma H_2/TMA/H_2 pre-cleaning has been found to be very effective in recovering etch damage on both oriented InGaAs substrates, especially for (110) sample and led to the improvement of electrical characteristics.

In terms of Al_2O_3/InGaSb interface study, the results of the first investigation into the impact of in-situ H_2 plasma exposure on the physical and electrical properties of the Al_2O_3/ *p* or *n*-$In_{0.3}Ga_{0.7}Sb$ interface have been presented. Samples were processed using a clustered inductively coupled plasma reactive ion etching and atomic layer deposition tool. Metal oxide semiconductor capacitors were fabricated subsequent to H_2 plasma processing (at plasma power of 150 W and 250 W) of InGaSb surface, followed by Al_2O_3 deposition and the corresponding capacitance-voltage plots were measured. X-ray photoelectron spectroscopy analysis of samples processed as part of the plasma power series have revealed a combination of ex-situ HCl cleaning and in-situ H_2 plasma exposure to completely remove In and Sb sub oxides, with the Ga-O content reduced to Ga-O:InGaSb < 0.1. The combination of H_2 plasma exposure and FGA yielded significantly improved metrics over the control HCl-treated sample, with the 150 W plasma treatment giving both the highest C_{mod} and lowest stretch out. The results present a critical advancement towards achieving III-V CMOS devices.

For future work in band engineering study, promising wide band gap oxides, such as Al_2O_3 and MgO, can be possibly doped with other alternative materials to boost permittivity (*k*) while retaining high band offsets for leakage current control; possible contenders are Y_2O_3, Ga_2O_3, Ta_2O_5, ZrO_2, Sc_2O_3, BaO and preferred deposition method is atomic layer deposition to achieve precise control of the composition and thickness by using optimized number of ALD cycles of two or more constituent oxides in the mixed oxide or nanolaminate. Moreover, spectroscopic ellipsometry measurements can be done in more detail to study the optical properties of mixed oxides and their correlation with electrical characteristics. Further characterisation of the defects in the mixed oxides bulks and at oxide/semiconductor interfaces can also be carried out using other techniques, such as electron spin resonance (ESR) and photoluminescence (PL). Future work also includes the extraction of conduction band maximum (CBM) of mixed oxides by inverse photoemission (IPES) measurements.

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