Embedded Sacrificial Layers for CMUT Fabrication

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***Abstract*—Capacitive Micromachined Ultrasonic Transducers (CMUTs) are generally fabricated either by conventional sacrificial release process or by wafer bonding technique. In the former, sacrificial layers are patterned with deposited materials on the substrate. This current work reports a development on the aforementioned technique wherein sacrificial islands are embedded inside grooves opened by DRIE in the substrate itself. The depth of the grooves and the thickness of the sacrificial layer are identical in dimension. As the first membrane layer between the top electrode and vacuum gap reduces the device sensitivity, it needs to be kept as thin as possible. Conformality of the deposition technique, however, requires a deposition thickness at least equal to the sacrificial layer. Hence one cannot go below a certain first membrane layer thickness. The present method is expected to solve such problems in CMUT fabrication. The present technique keeps the substrate completely flat even after sacrificial patterning, hence aiding the consecutive process steps such as electrode deposition and patterning. The described method does not increase process complexity other than an additional RIE step. Using this technique CMUTs with 5.6 MHz center frequency have been manufactured and tested.**

I. Introduction

Capacitive transducers were built initially with conventional machining tools constituting a metal surface as the back electrode and a mylar membrane forming the top electrode [1]. First generation micromachined versions of capacitive transducers were introduced and named as CMUTs in 1994 to differentiate them from the piezoelectric counterparts [2]. Fabrication was done using the well known sacrificial release process. Even though wafer bonded CMUT arrays have been reported more recently sacrificial release process still remains the standard method. Numerous variations of sacrificial release processes have been published over years, all of which are based on some basic simple steps. The cavity underneath the membrane is defined by pattering a layer of material on a conducting silicon wafer substrate. In the next step a conformal layer of membrane material is deposited throughout following which metal electrodes smaller than the sacrificial layer are patterned. Sometimes they are then buried with another thick layer of membrane material else it is kept open, depending on the nature of etchant being used for release. A lithography step followed by reactive ion etching (RIE) opens etch holes through which etchant flows in and selectively etches the sacrificial patterns to release the membrane. The choice of materials and chemicals are very important in such a process as the etchant must not harm the substrate and membrane material. The etch holes are sealed with a final layer of membrane material defining the full thickness of the membrane. The conducting substrate acts as the back electrode.

In the current paper we propose a development on sacrificial layer patterning for fabrication of CMUTs in general. The method obviates the need for a thick conformal coating on the sacrificial layer, and provides a flat surface for the subsequent process steps.

II. Embedded Sacrificial Layers: Motivation

The conventional sacrificial release process has been used extensively through the last two decades for CMUT fabrication. Some important considerations which control the final device yield includes material choice for various process steps, proper processing of wafer between two consecutive layer patterning, maintaining exact temperature and conditions during photolithography, PVD deposition etc. A broad search of literature reveals that LPCVD or PECVD Silicon rich Silicon Nitride is very well suited as the membrane material because of its very fine dielectric and mechanical properties. The sacrificial layer, on the other hand, can be chromium, or SiO, both of which provide a reasonable selectivity. The electrode is typically Ti-Au or Cr-Au.

TABLE I
Material Choice for Various Structural Layers

Layer	Material used
Substrate and electrode	Conductive p- Silicon wafer
Sacrificial Layer	200 nm Chromium
Membrane Material	PECVD Silicon Nitride
Top Electrode	150 nm Gold on 20 nm Chromium

The substrate which acts as the mechanical backing for the CMUT can also be used as one of the device

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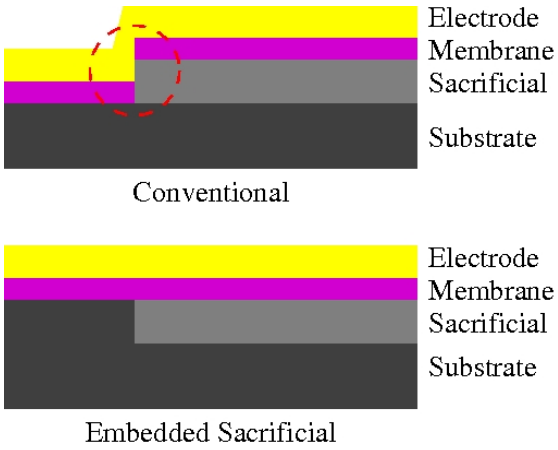


Fig. 1. The conventional fabrication method requires a first silicon nitride layer to be atleast as thick as the sacrificial to separate the device electrode form the sacrificial layer. A nonconformal thinner layer produces a profile as marked by the circle in the upper plot. The proposed method alleviates this problem by embedding the sacrificial layer.

electrode. For the fabrication of the devices presented in this work we have extensively used p- type Boron doped low resistivity (0.01-0.02 ohm-cm) 4 inch Silicon wafers with thickness of 525 μm. The choice of materials for CMUT manufacturing reported herein are listed in Table I. Fabrication of the device array starts with the deposition and patterning of the sacrificial layer. This is followed by the deposition of the first silicon nitride film. For the conventional method, this layer has to be at least as thick as the sacrificial layer, if not thicker, depending on the conformality of the deposition method. If this condition is not met, the subsequently deposited electrode layer may get into contact with the sacrifical material, as depicted in Fig. 1. The chemicals used in the underetch process are usually mixtures of various acids which may attack the electrode under these circumstances. Hence, the first nitride layer has to be kept considerably thick. However, this layer increases the effective gap of the device, reducing receive sensitivity. In order to keep this layer arbitrarily thin, we propose and demonstrate the embedded sacrificial layer method.

III. Grooved sacrificial Layers:Fabrication

In context to the above discussed issues that originate from the interaction of the sacrificial and the initial membrane layers, we propose a small development on the sacrificial technique. In place of depositing chromium as the first step for CMUT fabrication, we start with a surface micro-machining step for defining 200 nm deep grooves on the silicon wafer. The process steps include an image reversal lithography followed by a DRIE step which defines the grooves of exactly same dimensions as the sacrificial patterns. For etching we have used Oxford Plasma lab 100 ICP 300 Deep RIE system. The etching conditions are given in Table II. A lift off process with 200 nm of chromium fill the grooves. Such a sacrificial patterning process was incorporated to make sure that the surface is absolutely flat before the first nitride layer deposition. The flatness of the surface makes sure that even for very thin layer of initial membrane deposition, the conformality of the layer is not hampered. The conformality in turn makes sure that very small thickness of membrane material can be deposited as the initial layer on which the metal electrodes can be deposited and the membranes can be released as well.

TABLE II
Silicon and Silicon nitride etching parameters:

Parameters	Value
SF_6 flow	45 sccm
Pressure pumped to	7.5×10^{-9} Torr
DC Forward power	50 Watts
RF Forward power for Silicon Etching	1200 Watts
RF Forward power for Silicon Nitride Etching	2000 Watts
Table Temperature	$10°C$
Etch rate of Silicon	40 - 45 nm/sec
Etch rate of Silicon Nitride	8 - 10 nm/sec

A controlled etching was able to open up approximately 200 to 210 nm deep grooves. The available TORR Electron Beam Evaporator has an error margin of approximately 10%. So it was little difficult to level the chromium islands exactly with the top edge of the grooves. We thus define a convention for the leveling offset. If the chromium is above the upper groove edge we call it positive offset. Negative offset is for the reverse case. We tried fabricating some devices with positive offsets of 20 nm, 40 nm, etc. What we have observed for positive offset is that, more the embedding, flatter the surface after sacrificial patterning and greater is the conformality with thin initial membrane layer. After some trial and errors finally we were able to reach a positive offset of approximately 5-8 nm. As an initial test we have used an initial nitride thickness of approximately 100 nm. Using sacrificial embedding with negative offset for device manufacturing has been avoided intentionally; as, after release the membranes will form isolated troughs over the ring arrays. We were not sure about any possible structural or performance related constraints resulting from such surface profiles. Fig. 2 shows SEM images of sacrificial grooves drilled on Silicon wafer, various positive and negative offset profiles after Chromium liftoff .and a profilometric measurement of an almost leveled surface after sacrificial patterning.

The next fabrication steps are conventional. We buried 33 micron diameter top electrodes (20 nm Chromium ad-

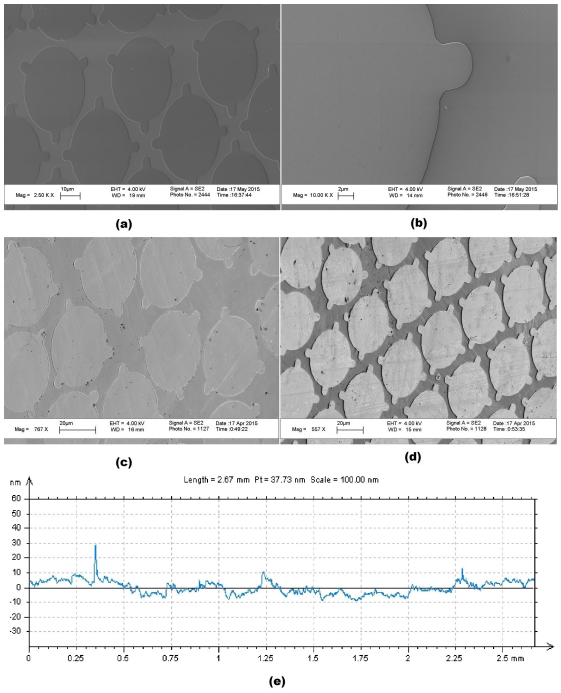


Fig. 2. (a) Sacrificial grooves on Silicon wafer, (b) Sacrificial Chromium with negative offset leveling, (c) Almost leveled(¡10 nm positive offset) sacrificial patterns, (d) Patterns with considerably higher positive offset, (e) Profilometric measurement showing less than 10 nm step difference between patterns andSilicon surface after sacrificial patterning.

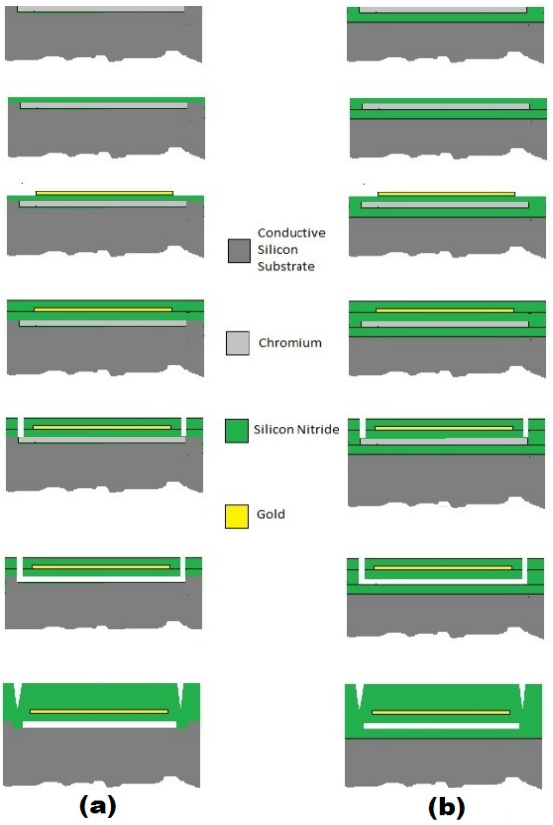
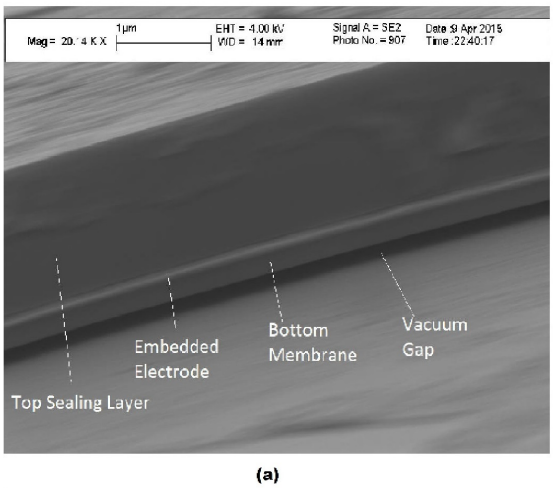


Fig. 3. Process flow for (a) Sacrificial groves on Silicon wafer, (b) Sacrificial grooves on insulating Silicon Nitride coating on Silicon)

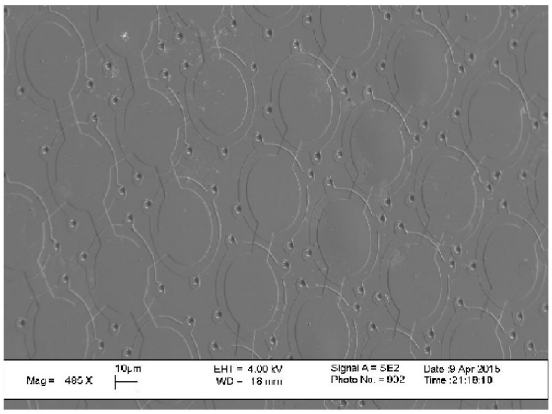
hesion layer followed by 150 nm of Gold) under another 600 nm of nitride. 2 micron etch holes were drilled deep upto the Chromium layer. The DRIE recipe is same as the one described in Table II particularly for the Silicon Nitride case. The sample is set for under-etching and release. We have used commercially available Chromium etchants from Technic, France. Methanol has been used to clean Chromium etchants from the grooves, as it has lesser viscosity and surface tension than water. Hence, the effect of capillary force leading to stiction, if any, can be negated. After proper drying, the arrays are coated with a 1.6 micron final thick layer of Silicon nitride to seal the holes.

IV. Device Testing and Improvement:

As an initial test of device performance fabricated by our proposed process we shorted all top electrode pads with conductive silver epoxy and did a pressure measurement with needle hydrophone. Since we are aiming for immersion application and epoxy is conducting we used a drop of vegetable oil (insulator) as the continuum. As of the first test we incorporated 45 Volts DC bias superposed by 10 Volts AC peak to peak. The hydrophone measurements showed 2 mV deflection on the oscilloscope which correspond to 10 kPa pressure. We experienced some leakage current in our measurements which is intrinsic to such devices as minute pinholes are always present even though low frequency densification is used during PECVD nitride deposition. Such pinholes result in short circuit between the top electrode connection pads and the conducting wafer which is used as the bottom electrode. To avoid such leakage issues researchers have reported the use of an insulation layer below the sacrificial islands. The layer being few 100 Å thick also acts as the etch stop layer for materials with less selectivity. For our devices with embedded sacrificial layers we also incorporated such an insulation layer of PECVD Silicon Nitride. The process steps started with deposition of 350 nm of nitride on the conducting wafer and then drilling the 200 nm deep sacrificial grooves on the same, thus offering considerable insulation sandwiched between the top electrode pads and the ground electrode. Another advantage of using the insulating nitride layer is that the



(a)



(b)

Fig. 4. CMUT Devices (a) Layers of a single CMUT cell, (b) SEM of array elements, (c) A ring array formed by the CMUT devices.

RIE etch rate is smaller than that of silicon with our currently available DRIE recipe, offering more control on the process step. The process flow for both (with and without insulation layer) reported fabrication steps are shown in Fig. 3.

The new devices with grooves on the insulation layer were also tested in an impedance analyzer yielding resonance at 5.66 MHz. Fig. 4 exhibits SEM images of the fabricated devices and the cross section of a single cell exhibiting multiple layers. The impedance measurement result is shown in Fig. 5.

V. Conclusion

A technological development on the sacrificial release method of CMUT fabrication has been proposed and reported. Chromium sacrificial layers embedded in both conducting and insulating layers are exhibited. The technique yields a perfectly flat surface before initial

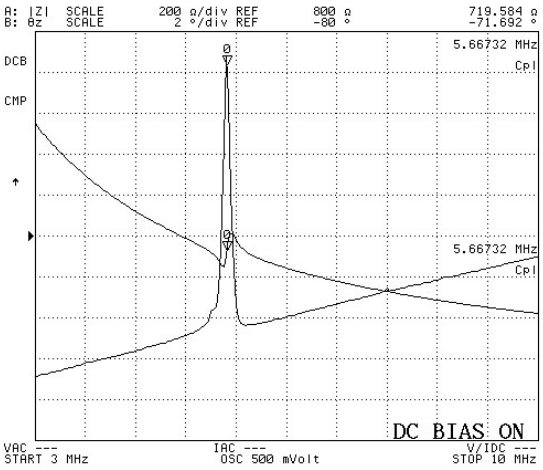


Fig. 5. Impedance analyzer measurement result.

membrane material deposition. It is expected that by such a process very thin initial layer can be sustained for release without conformality problems. The devices are tested with impedance analyzers for resonance frequency and they have also shown response to hydrophone based pressure measurements, exhibiting their operational capability. Work is in progress to optimize the thinnest possible initial nitride layer which the technology can support, yielding extremely sensitive CMUT arrays for imaging modalities.

VI. Acknowledgment

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References

[1] M. Rafiq and C Wykes, "The performance of capacitive ultrasonic transducers using v grooved backplates," Meas. Sci. Technol.,Vol.2. , pp. 168- 174.1991.

[2] M I Haller and B T Khuri-Yakub, " A surface micromachined electrostatic ultrasonic air transducer," Proc. IEEE Ultrason. Symp., pp 1241-4, 1994.

[3] A S Ergun, Y Huang, X Zhuang, O Oralkan, G G Yaralioglu, and B T Khuri-Yakub, "Capacitive Micromachined Ultrasonic Transducers: Fabrication Technology," IEEE Trans. Ultrason., Ferroelectr., Freq. Control, Vol.52, No:12, pp. 2242-2257, Dec. 2005.