An X-band 6-Bit Active Phase Shifter

Kerim Kibaroglu, Emre Ozeren, Ilker Kalyoncu, Can Caliskan, Hüseyin Kayahan, Yasar Gurbuz

Sabanci University, Faculty of Engineering and Natural Sciences, Istanbul – FENS, Orhanli – Tuzla, 34956, Turkey

Abstract — **This paper presents a 6-bit active phase shifter using a new vector-sum method for X-band (8-12 GHz) phased arrays in 0.13 μm SiGe BiCMOS process. An RC filter is used to generate two orthogonal vectors which are then fed into four VGAs, two using the common-base and two using the common-emitter topology. This generates 4 vectors of 0°, 90°, 180° and 270° which are scaled and added by varying the gains of the VGAs to generate any phase between 0-360°. The gains of the VGAs are adjusted with analog voltage control using the current-steering method. The outputs of the VGAs are connected together with a common load in order to add the vectors in current-domain. The phase shifter achieves < 5.6° RMS phase error over 8-12 GHz and < 3.1° RMS phase error over 9-11 GHz. The phase shifter has a power consumption of 16.6 mW from a 2V supply. The chip size is 850 μm x 532 μm including the probing pads. These performance parameters are comparable with the state of the art of the technology in literature.**

Index Terms — **Active phase shifter, vector modulator, phased array, X-band, SiGe BiCMOS, T/R module.**

I. INTRODUCTION

The performance of transmit/receive modules are critical in achieving fast beam scanning and electronic beam control functions in modern phased arrays. The block diagram of a typical T/R module is shown in Fig. 1. The performance of the phase shifter determines the phase resolution of the overall module. With the developments in silicon process technologies, it became possible to satisfy the performance requirements for such T/R modules with Si-based highly compact and low cost phase shifters rather than the costly III-V technologies which offer the highest performance [1, 4].

In this paper, a 6-bit active phase shifter using a single-ended vector modulator topology in 0.13 μm SiGe BiCMOS process is presented. The proposed topology uses an RC filter to generate two orthogonal vectors. These vectors are then fed into two identical blocks which introduce another 180° phase shift by amplifying the same vector with inverting and non-inverting variable gain amplifiers. The amplitudes of the vectors are then scaled with the current steering method as needed to obtain any phase between 0-360°. Two of the vectors are selected at a time and added to generate any phase between these vectors. The proposed active phase shifter exhibits low RMS phase error, low power consumption and very small chip area at the cost of higher insertion loss.
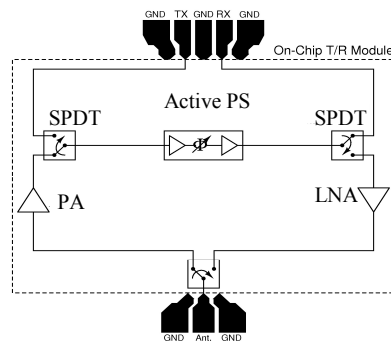

Fig. 1: Block diagram of a SiGe BiCMOS On-chip T/R module

II. CIRCUIT DESIGN

The proposed schematic of active phase shifter is shown in Fig. 2a. A single-ended vector modulator topology with analog control was chosen to achieve low RMS phase error. RC filter is utilized to generate two orthogonal vectors which are then scaled and added by the following VGA block each consisting of two signal paths, one inverting and the other non-inverting.

A. RC filter

The operating bandwidth of the active phase shifter is set by the accuracy of the vector generation filter. It was analyzed in [6] that to achieve 6-bit operation an amplitude error < 1 dB and a phase error < 2.8° are required for the filter. An LC configuration was used in previous studies to generate orthogonal vectors with low phase error and low insertion loss [5]. However, this configuration cannot generate vectors with low phase and amplitude imbalance when loaded with capacitive or inductive loads. Therefore, a simple RC filter was used, despite its 10 dB insertion loss, to generate two orthogonal vectors with less than 0.5° phase error over the entire X-band. A serial inductor is added for matching.

B. Variable Gain Amplifiers

The vector generation filter is followed by a VGA block consisting of two signal paths. One of these paths contains a two-stage common base amplifier and the other contains a cascode amplifier. Since the common-base stage is non-inverting and the cascode stage is inverting, an additional 180° phase shift is added to the initial 0° and 90° vectors.
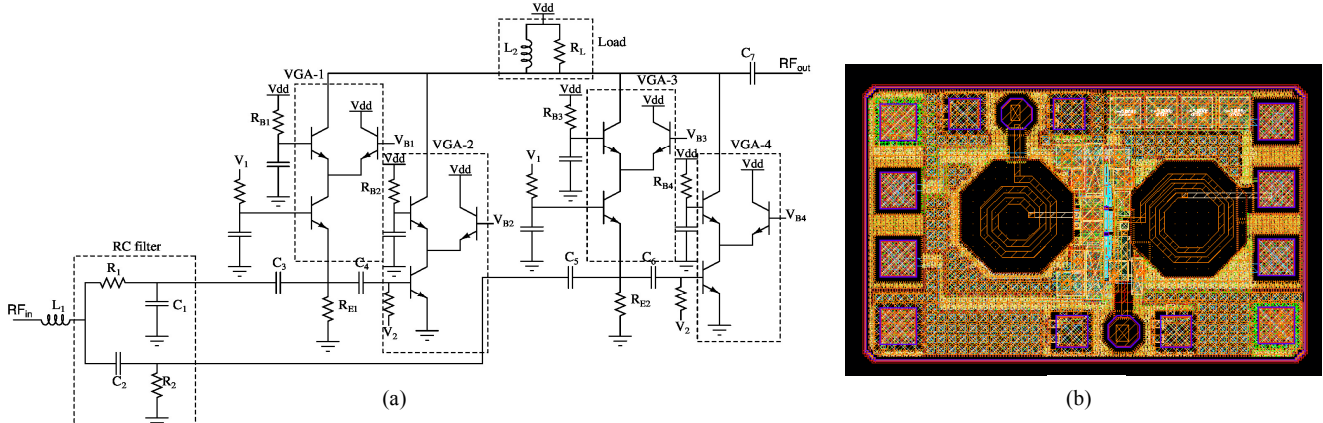
Fig. 2: a) Schematic b) Layout of active phase shifter using an RC vector generation filter and VGAs

This generates four vectors of 0°, 90°, 180° and 270° to scale and add to obtain any phase between 0-360°. A similar circuit was used in [3] as an active balun.

In order to scale the vectors, a current-steering transistor is added to both paths. By change the base voltage of these transistors, VB1-VB4, the gain of each path can be adjusted. In order to have the maximum gain, VBX (one of VB1-VB4) is set to 1.6V and all of the signal will flow to the output. On the other hand, setting VBX to 2.1V will direct the signal entirely to VDD, so that it will not contribute to the output. Applying any other value to VB1-VB4 will allow us to vary the gain of the amplifier. The vectors are added two at a time by cancelling the contribution of the undesired two vectors at the output by setting VBX to 2.1V. Both common-base and cascode paths have a maximum gain of 1 dB.

A gain control range of 15 dB is required in each path to obtain all 64 phases between 0-360°. For this purpose the bias current is set to 2 mA for each stage. The transistors were scaled such that they would operate with the maximum f_t at the chosen bias current, to obtain the maximum possible gain. The bias voltages V1 and V2 are chosen to be 1.25 V and 841 mV respectively to obtain bias currents of 2 mA. The bias voltages are generated by on-chip bias networks. Large DC blocking capacitors (C4 & C6) are added between the common-base and cascode stages in order to bias them separately. A large resistor (RB1-RB4) is added to the base of the upper transistors in both stages to minimize the difference in insertion phase for different amplifier gains.

In order to add the selected vectors, the outputs of the VGAs are simply connected together with a common load to add the two signals in current domain. The shunt inductor and resistor and the series capacitor at the output are also used to match the output of the entire block to 50 Ω. The inp ut resistance of this block is 15 Ω as it is with the parallel resistor (RE1 & RE2) included to provide a DC path for the common-base stage. Therefore, the RC filter preceding this block is designed for a 15 Ω load rather than a 50 Ω load.

Since current steering method is used to adjust the gain, the DC current flowing through the lower transistors in both stages is constant as the gain is varied. Therefore, the input impedance of the block is not sensitive to the differences at gain states. Even though the vectors from the same common-base and cascode block will never be selected to be added since they are 180° out of phase, both of the signal paths are biased, in order to reduce RMS phase error.

The layout of the full circuit can be found in Fig. 2b. The layout is designed to be as compact as possible to reduce the chip area as well as to prevent additional phase errors due to parasitics. Two VGA blocks following the RC filter are designed to be perfectly symmetrical to avoid additional phase errors. The inductors L1 and L2 are custom designed and the chip area is 0.452 mm2.

III. RESULTS AND COMPARISON

After the layout was completed, simulations were run to determine the precise voltages, VB1-VB4, to obtain the required phases between 0-360° for 6-bit operation. The relative insertion phases for each state are shown in Fig. 3 over 8-12 GHz. Each state is separated by 5.625° at the center frequency of 10 GHz as required for 6-bit operation.

RMS phase error was calculated using the insertion phase curves and it is shown in Fig. 4. Since the bias voltages for the VGAs are chosen to achieve the required phase at the center frequency, the minimum phase error is achieved around 10 GHz to be < 1°. RMS phase error increases towards the band edges reaching a maximum of 5.6° at 8 GHz and 12 GHz. RMS phase error is <3.1^0 between 9-11 GHz.
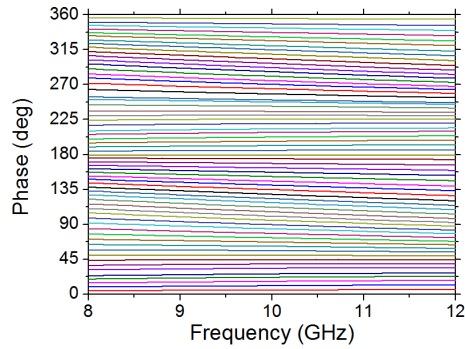
Input and output matching of this circuit changes

Fig. 3: Relative phase shift for all 64 states

Figure 4: RMS phase error

slightly for different states. Both S11 and S22 are well below -10 dB. The output specifically needs to be well matched for this topology as the phase error strongly depends upon it.

Recently reported phase shifters are compared in Table 1. [1] uses a similar vector modulator topology with 3 vectors rather than 4, but consumes a significantly larger area and has higher RMS phase error. Passive phase shifters do not consume DC power, but they have higher insertion loss [2] and consume larger chip area [4]. Differential vector modulator topologies are used in [3] and [5]. [3] offers low RMS phase error and area at a lower frequency range and bandwidth. [5] utilizes a differential quadrature all-pass filter for vector generation which provides low RMS phase error over a wide bandwidth and high gain at the cost of higher DC power consumption. The work presented in this paper provides a single-ended alternative with low RMS phase error, low power consumption and very low chip area that can compete with differential phase shifters.

IV. CONCLUSION

In this paper, a 6-bit active phase shifter in 0.13-μm SiGe BiCMOS process technology is presented. Two orthogonal vectors are generated by an RC filter and then scaled and added by two blocks containing common-base and cascode amplifiers. With this proposed single-ended active phase shifter topology, low RMS phase error, low power consumption and very low chip area can be achieved at the cost of higher insertion loss. RMS phase error is less than 5.6° over a 4-GHz bandwidth with a power consumption of 16.6 mW, insertion loss of 10 dB and chip area of 0.452 mm2. The phase shifter is designed and optimized for on-chip X-band phased array systems.

ACKNOWLEDGEMENT
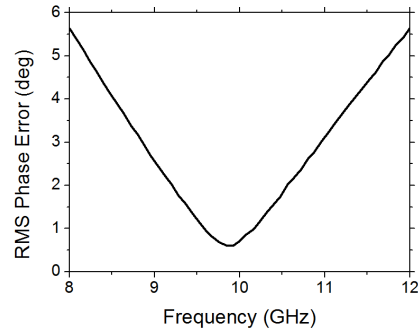
TABLE I.
COMPARISON OF RECENT PHASE SHIFTERS

Process	Freq GHz	Ph. Er. (°)	Gain dB	Phase range	Area mm^2	DC pow. mW	Ref
0.25 μm SiGe HBT	6-9	7	12 ±1	360°	7.2	15.36	[1]
0.13 μm CMOS	8.5-10.5	4.1	-11.2 ±1	360° (6-bit)	0.51	0	[2]
0.18 μm CMOS	2-3	5	1.5 ±1.5	360°	0.38	24	[3]
0.18 μm CMOS	8.5-10.5	4	-	360° (6-bit)	8.5	0	[4]
0.18 μm SiGe HBT	6-18	5.6	18 ±1.5	360° (5-bit)	0.9	62	[5]
0.13 μm SiGe HBT	8-12	5.6	-10 ±1	360° (6-bit)	0.45	16.6	This Work
0.13 μm SiGe HBT	9-11	3.1	-10 ±1	360° (6-bit)	0.45	16.6	

REFERENCES

[1] Dogan, M.; Tekin, I., "An X-band RFIC Active Phase Shifter," European Microwave Conference, Amsterdam, Netherlands, 2012.

[2] Sim, S.; Jeon, L.; Kim, J-G., "A Compact X-Band Bi-Directional Phased-Array T/R Chipset in 0.13 μm CMOS Technology," Microwave Theory and Techniques, IEEE Transactions on, vol.61, no.1, pp.562-569, January 2013.

[3] Zheng, Y.; Saavedra, C. E., "Full 360 Vector-Sum Phase-Shifter for Microwave System Applications," Circuits and Systems, IEEE Transactions on, vol.57, no.4, pp.752-758, April 2010.

[4] KimGharibdoust, K.; Mousavi, N.; Kalantari, M.; Moezzi, M.; Medi, A.; "A Fully Integrated 0.18 μm CMOS Transceiver Chip for X-Band Phased-Array Systems," Microwave Theory and Techniques, IEEE Transactions on, vol.60, no.7, pp.2192-2201, July 2012.

[5] Koh, K-J.; Rebeiz, G.M., "A 6–18 GHz 5-Bit Active Phase Shifter," Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International, vol., no., pp.792,795, 23-28 May 2010.

[6] Kim, S. Y.; Kang, D.-W.; Koh, K.-J.; Rebeiz, G.M., "An Improved Wideband All-Pass I/Q Network for Millimeter-Wave Phase Shifters," Microwave Theory and Techniques, IEEE Transactions on, vol.60, no.11, pp.3431-3439, November 2012.