AN ULTRA WIDE TEMPERATURE RANGE R-2R BASED 8 BIT D/A CONVERTER FOR 90NM CMOS TECHNOLOGY

by

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AN ULTRA WIDE TEMPERATURE RANGE R-2R BASED 8 BIT D/A CONVERTER FOR 90NM CMOS TECHNOLOGY

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Keywords: DAC, cryogenic circuits, ultra wide temperature (UWT), CMOS D/A converter, R-2R

Abstract

Digital-to-analog converters have a wide range of applications from converting stored digital/audio signals to data processing and to data acquisition systems. Another application area could be a supporting building block in either cooled or un-cooled Read-out integrated circuits (ROICs). For this aspect, the capability of ultra wide temperature range operation may prove useful providing freedom to the designer and the consumer.

In this thesis, design of an 8-bit, fully binary R-2R based digital-to-analog converter is realized with 90nm CMOS technology to operate in a wide temperature range (-200°C to 120°C) to be used in an ongoing Digital Read-out Integrated Circuit (DROIC) for infrared (IR) imaging systems. UWT range of operation is obtained via a temperature compensated voltage reference generator circuit consisting of only MOSFETs. In order to aid the matching of the resistors, a common-centroid layout technique is applied to the resistor core of the circuit which eliminates the process gradients. TSMC's 90nm 1 poly, 9 metal Mixed – Signal RF technology and a power supply of 1.2V are used for this design. For accuracy, the best performance is obtained at the room temperature where the fastest operation is possible at cryogenic temperatures at the expense of precision. It has a DNL and INL of ±0.3LSB at room temperature and ±0.45LSB at 120°C. The DAC can operate up to 20MHz. The circuit

dissipates only 0.43mW in full scale range at cryogenic temperatures where 1.1mW at room. It occupies a chip area of only 0.015mm^2.

90NM CMOS TEKNOLOJİSİ İÇİN ÇOK GENİŞ SICAKLIK ARALIKLI R-2R TABANLI 8 BIT D/A DÖNÜŞTÜRÜCÜ

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Abstract

Dijital-analog dönüştürücüler depolanmış dijital ses sinyallerinin dönüştürülmesinden bilgi edinme ve işleme sistemlerine kadar çok geniş bir kullanım alanına sahiptir. Birbaşka uygulama alanı da soğutulmuş veya soğutulmamış okuma entegre devrelerinde (ROIC) yardımcı devre elemanı olarak kullanılmalarıdır. Bu yönüyle, çok geniş sıcaklık aralığında çalışabilme yeteneği hem tasarımcıya hem de son kullanıcıya özgürlük sağlamaktadır.

Bu tez çalışmasında, 8-bit R-2R tabanlı, çok geniş bir sıcaklık aralığında (-200°C to 120°C) çalışabilen bir dijital-analog dönüştürünün 90nm CMOS teknolojisi ile, halen sürmekte olan ve kızılötesi görüntüleme sistemlerinde kullanılacak olan bir dijital okuma entegre devresinde (DROIC) kullanılmak üzere tasarımı gerçekleştirilmiştir. Çok geniş aralıklı çalışma kabiliyeti sıcaklık kompanzasyonu gerçekleştirilen ve sadece MOSFET'lerden oluşan bir gerilim refereans devresi ile temin edilmiştir. Dirençlerin eşleştirilmesini iyileştirmek maksadıyla devrenin direnç çekirdeğine proses gradyanlarını elimine eden common-centroid serim tekniği uygulanmıştır. Tasarımda TSMC firmasının 90nm 1 poly, 9 metal Mixed – Signal RF technolojisi ve 1.2V'luk besleme gerilimi kullanılmıştır. Doğruluk için en iyi performans oda sıcaklığında elde edilirken en hızlı çalışma frekansına ise kriyojenik sıcaklıklarda hassaslıktan ödün vermek suretiyle ulaşılmıştır. Devre, oda sıcaklığında ±0.3LSB ve 120°C'de ±0.45LSB

lik DNL ve INL performansına ulaşmaktadır. DAC, 20MSps hızına kadar çalışabilmektedir. Devre, tam ölçekli çıkışta kriyojenik sıcaklıkta sadece 0.43mW ve oda sıcaklığında 1.1mW güç tüketmektedir. Çip sadece 0.015mm^2'lik alan kaplamaktadır.

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1 INTRODUCTION

1.1 Digital-to-Analog Converter

A digital-to-analog converter (DAC) is a device which converts digital information to analog signal e.g. voltage, current or charge. Digital-to-analog conversion is an essential function in data processing systems. D/A converters interface the digital output of signal processors with the analog world. Also, multistep analog-to-digital converters employ inter-stage DACs to reconstruct analog estimates of the input signal. Each of these applications imposes certain speed, precision, and power dissipation requirements on the DAC, mandating a good understanding of various D/A conversion techniques and their trade-offs [1].

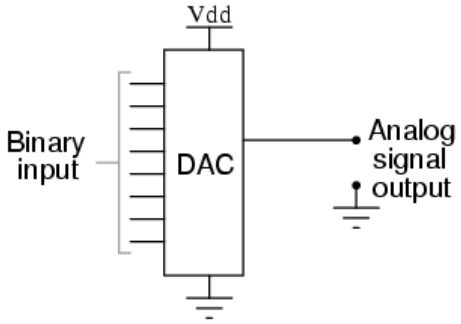

Figure 1.1 Basic diagram of an 8 bit DAC.

1.2 DAC Applications

The most popular digital-to-analog converter application is converting stored digital audio and/or video signals. For instance, stored digital information in MP3 format can be converted into music via a high precision DAC [2].

Many high speed DAC specifications are generated by the video market needs. Video signals from a digital source, such as a computer or a DVD, are often displayed on analog monitors, thus requiring high-speed DACs. High performance DACs are also used for TV: HDTV quality pictures require HDTV quality displays. An analog NTSC TV displays 525 lines each frame while a good HDTV monitor displays more than 1000 lines per frame. In addition to the higher resolution a HDTV monitor also provides a higher contrast ratio and a more detailed color range. Unlike an analog TV which has about 8-bit contrast ratio, a digital light processing (DLP) or plasma TV provide contrast ratios that exceed 11-bits. DNL, conversion-rate, glitch energy and minimum

chip area are key parameters for such video DACs. To maximize the viewing quality on a state-of-art display technology, 12-bit and 150 MSPS conversion rate are therefore often necessary.

DACs are also used for wired and wireless communications that use a variety of modulation and encoding schemes to exchange digital information. DACs for ADSL or ADLS2+ must handle signal bands of 1.1 MHz or 2.2 MHz with 12-bit of resolution. Wireless applications such as UMTS, CDMA2000, and GSM/EDGE require both high conversion rates and high resolution especially when multiple carriers are used instead of a single signal generating source. UMTS uses up to four carriers per transmitter, and GSM/EDGE and CDMA2000 applications may employ four to eight carriers for a single transmitter. Thus, the generation of a complex modulation waveform involves complex digital processing but also requires high performance DACs. Conversion rates of 200MSpS - 1GSpS and resolutions from 12-bit to 16-bit can be necessary.

An analogue signal processor can use DACs to replace potentiometers. A digitally controlled resistance allows functions like digital gain and offset cancellation, programmable voltage and current sources, and programmable attenuation. The solution is a resistive divider DAC whose wiper position is selected via an n-bit register value. The setting is updated infrequently and often the DAC uses a slow serial interface with volatile or non volatile memory to store the setting.

A signal from a microphone or other sound source is converted to a digital signal for storage in a computer, where it can be edited if necessary or placed in some storage devices. Headphones or speakers playback the sound after the DAC conversion is realized. The resolution used is high (16-bit or more) with a typical sampling-rate of 44 kSpS. Since the signal bandwidth is relatively low, DACs used for audio applications normally exploit oversampling [2].

Digital to analog converters could also be used in read-out integrated circuits (ROICs). General ROIC architecture is composed of various components such as preamplifier, multiplexer, noise suppression stage, memory storages, analog digital converter (ADC) and output buffer. Moreover, additional supporting stages are needed to complete ROIC like digital synthesized control circuit, level shifter, digital analog converter, comparator, current sources and current mirrors.

1.3 DAC Performance Characteristics [3]

Figure 1.2 demonstrates the block diagram of a digital-to-analog converter.

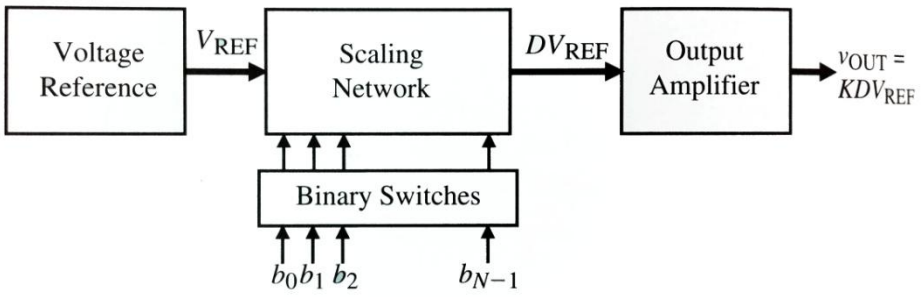

Figure 1.2 Block diagram of a DAC[3]

The characteristics of a DAC could be divided into two subsections. The first one is static properties and the second is the dynamic properties.

1.3.1 Static Properties

The *resolution* of a DAC stands for the number of bits that the converter accepts at its input and is expressed as N-bits, where N is the number of bits. Figure 1.3 indicates the input and output characteristics of a 3-bit DAC.

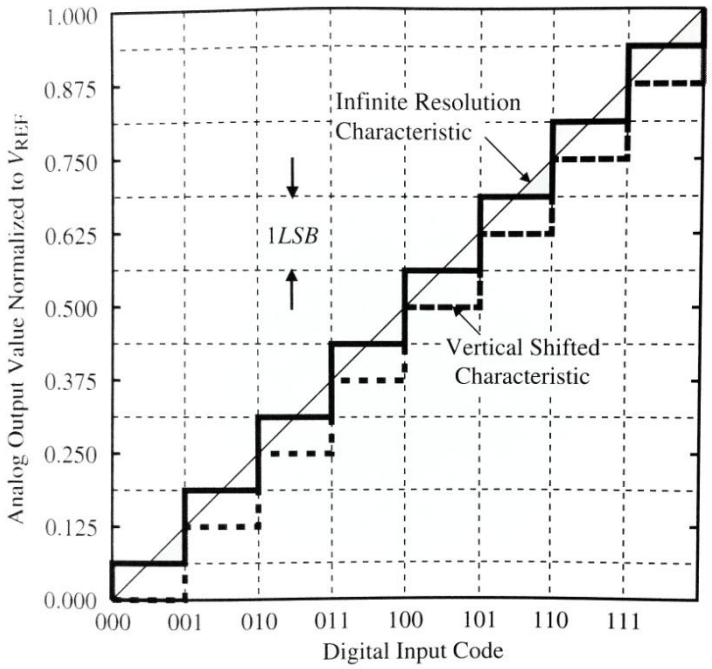

Figure 1.3 Ideal input-output characteristics of a 3-bit DAC [3]

Another parameter is the term *LSB* (least significant bit) and could be given as in (1.1).

$$LSB = \frac{V_{REF}}{2^N} \tag{1.1}$$

1-bit increase in the digital word corresponds to an increase of 1 LSB at the output. Since the resolution of the DAC is finite, the maximum output voltage which corresponds to the largest digital word (111 in the case of a 3-bit DAC) is not equal to $V_{REF.}$ As indicated by (1.2) the term *full scale* (FS) defines this phenomenon.

$$FS = V_{REF} - LSB = V_{REF}(1 - \frac{1}{2^N}) \tag{1.2}$$

Another definition is *full scale range* (FSR) which is for an infinite resolution DAC and equals to V_{REF}. One of the other most important parameters is *quantization noise* and is depicted in Figure 1.4. This phenomenon is intrinsically present in data converters and could be defined as the uncertainty in digitizing an analog value with a finite resolution converter. The quantization noise or sometimes called quantization error is basically the analog output of the infinite-bit DAC minus the analog output of the finite-bit DAC. Figure 1.4 could be easily drawn from the Figure 1.3 using this definition.

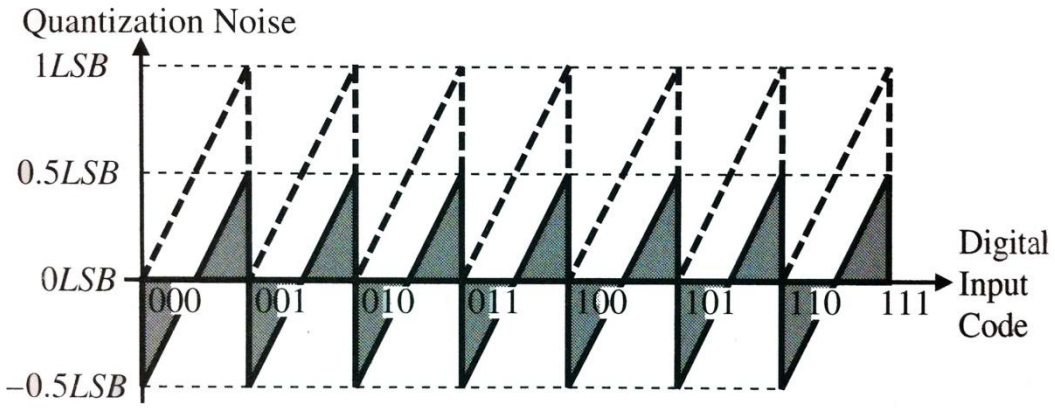

Figure 1.4 Quantization noise for the 3-bit DAC [3]

It could be observed that the quantization noise is a saw tooth waveform having a peak-to-peak value of 1*LSB*. It is useful to note that 0.5*LSB* is equal to $FSR/2^{N+1}$ and this defines the accuracy of the converter. It is possible to reduce the inaccuracies of the

converter within ±0.5*LSB* but further decrease is limited by the quantization noise which can only be reduced by increasing resolution.

The *dynamic range (DR)* of a DAC is the ratio of the FSR to the smallest difference that could be resolved (i.e., an *LSB*). It is given as

$$DR = \frac{FSR}{LSB} = \frac{FSR}{(FSR/2^N)} = 2^N \tag{1.3}$$

also given in decibels,

$$DR(dB) = 6.02N \text{ dB} \tag{1.4}$$

The *signal-to-noise ratio (SNR)* for the DAC is defined as the ratio of the full scale value to the rms value of the quantization noise which is given in (1.5).

$$\sqrt{\frac{1}{T}\int LSB^2(\frac{t}{T}-0.5)^2 dt} = \frac{LSB}{\sqrt{12}} = \frac{FSR}{2^N\sqrt{12}} \tag{1.5}$$

And finally SNR becomes,

$$SNR = \frac{v_{OUT}rms}{(FSR/2^N\sqrt{12})} \tag{1.6}$$

The largest possible rms value of v_{OUT} is $(FSR/2)/\sqrt{2}$ or $V_{REF}/2\sqrt{2}$ assuming a sinusoidal waveform. Therefore, the maximum SNR required for a DAC is

$$SNR_{max} = \frac{FSR/(2\sqrt{2})}{FSR/(2^N\sqrt{12})} = \frac{2^N\sqrt{6}}{2} \tag{1.7}$$

it becomes the well-known formula in decibels as given in (1.8).

$$SNR_{max}(dB) = 6.02N + 1.76 \tag{1.8}$$

The *effective number of bits (ENOB)* can be defined from this as

$$ENOB = \frac{SNR_{actual} - 1.76}{6.02} \tag{1.9}$$

where SNR_{actual} is the actual *SNR* of the converter.

For each digital word, there should be a unique analog output signal. Any deviations from Figure (1.3) fall into the category of static-conversion errors. Static-conversion errors include offset errors, gain errors, integral nonlinearity, differential nonlinearity, and monotonicity. An *offset error* is a constant difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured at any vertical jump. This error is illustrated in Figure (1.5.a). This error could be eliminated by shifting the resulting characteristic vertically. *Gain error* is the difference between the actual finite resolution and an infinite resolution characteristic measured at the rightmost vertical jump. Gain error is proportional to the magnitude of the DAC output voltage. This error is illustrated on the 3-bit DAC characteristic shown in Figure (1.5.b).

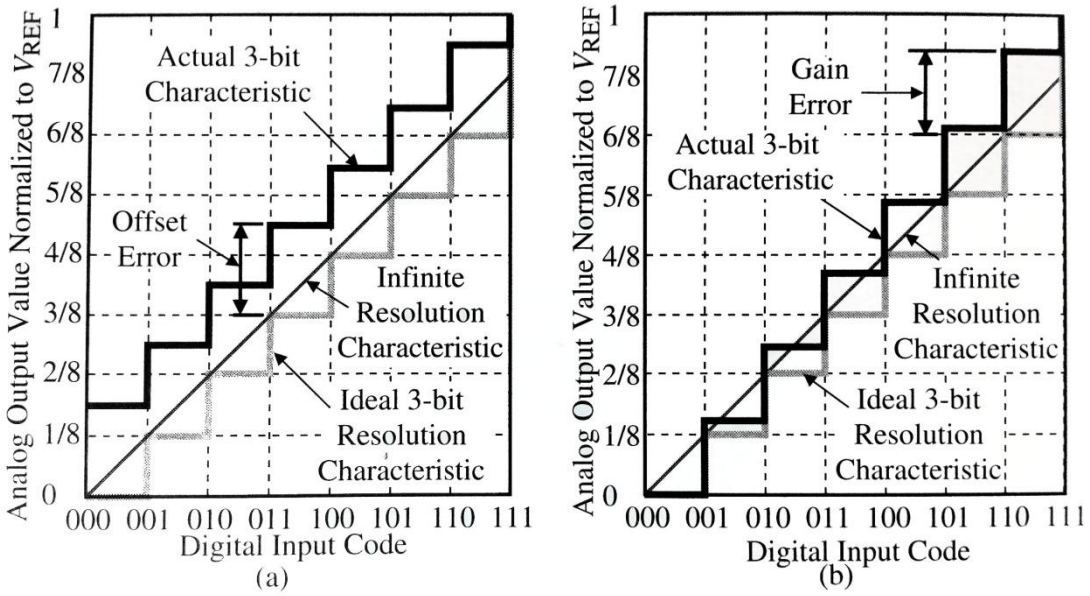

Figure 1.5. a. Illustration of offset error in a 3-bit DAC

b. Illustration of a gain error in a 3-bit DAC[3]

Integral nonlinearity (INL) is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically. Integral nonlinearity can be expressed as a percentage of the full scale range or in terms of the least significant bit. Integral nonlinearity has several subcategories, which include absolute, best- straight-line, and end-point linearity [4], The *INL* of a 3-bit DAC characteristic is illustrated in Figure 1.6. The *INL* of an AT-bit DAC can be expressed as a positive *INL* and a negative *INL* The positive *INL* is the maximum positive *INL* The negative *INL* is the maximum negative *INL*. In Figure 1.6, the maximum +*INL* is 1.5LSB and the maximum -*INL* is -1.0LSB.

Differential nonlinearity (*DNL)* is a measure of the separation between adjacent levels measured at each vertical jump. Differential nonlinearity measures bit-to-bit deviations from ideal output steps, rather than along the entire output range. If V_{cx} is the actual voltage change on a bit-to-bit basis and V_s is the ideal change, then the differential nonlinearity can be expressed as

$$DNL = \left(\frac{V_{cx} - V_s}{V_s} \right) x100\% = \left(\frac{V_{cx}}{V_s} - 1 \right) LSBs \tag{1.10}$$

For an N-bit DAC and full scale voltage range of VFSR,

$$V_s = \frac{V_{FSR}}{2^N} \tag{1.11}$$

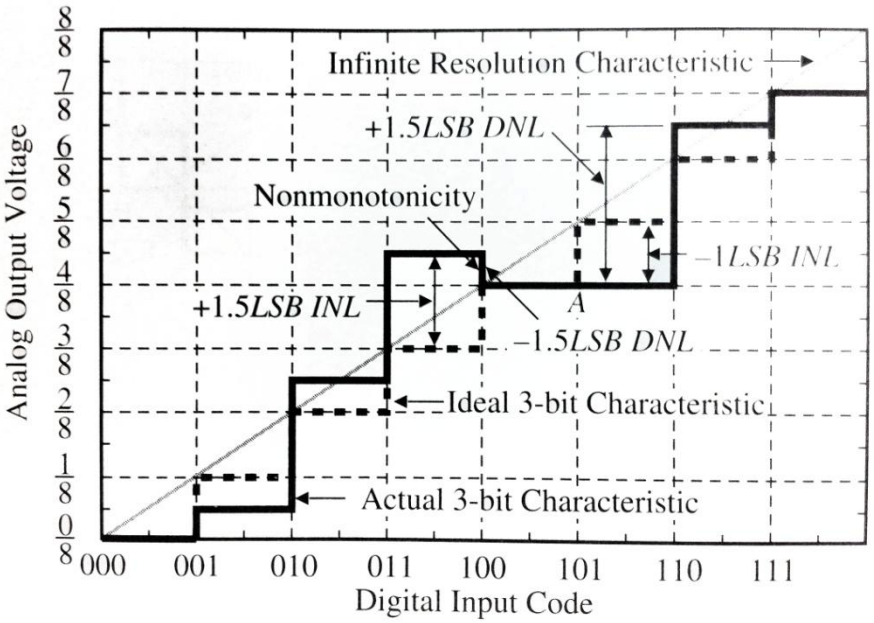

Figure 1.6 Illustration of INL, DNL and nonmonotonicity in a 3-bit DAC.[3]

Figure 1.6 also illustrates differential nonlinearity. Note that *DNL* is a measure of the step size and is totally independent of how far the actual step change may be away from the infinite resolution characteristic at the jump. The change from 101 to 110 results in a maximum *+DNL* of *1.5LSBs* {$V_{cx}IV_s$ = 2.5*LSBs).* The maximum negative *DNL* is found when the digital input code changes from 011 to 100. The change is -0.*5LSB* (V_{cx}/V_s =-0.5*LSB),* which gives a *DNL* of *-1.5LSBs.* It is of interest to note that as the digital input code changes from 100 to 101, no change occurs (point A). Because we know that a change should have occurred, we can say that the *DNL* at point *A* is -1*LSB.*

Monotonicity in a DAC means that as the digital input to the converter increases over its full scale range, the analog output never exhibits a decrease between one conversion step and the next. In other words, the slope of the transfer characteristic is never negative in a monotonic converter. Figure 1.6 exhibited non-monotonic behavior as the digital input code changed from 011 to 100. Obviously, a non-monotonic DAC has very poor *DNL.* As a matter of fact, a DAC that has a *-DNL* that is - 1*LSB* or more negative will always be non-monotonic.

1.3.2 Dynamic Properties

The above considerations of the DAC have been time-independent or static. The time- dependent or dynamic characteristics are also an important part of the characterization of the DAC. The primary dynamic characteristic of the DAC is the *conversion speed.* The conversion speed is the time it takes for the DAC to provide an analog output when the digital input word is changed. The conversion speed may vary from milliseconds to nanoseconds depending on the type of DAC.

The factors that determine the speed of the DAC are the parasitic capacitors and the gain bandwidth and slew rate of op amps, if they are used. Parasitic capacitors exist at every node in a circuit (particularly an integrated circuit). If the node is a high-resistance node, then a pole results that is equal to the negative reciprocal of the product of the resistance to ground and the capacitance to ground. Fortunately, most nodes are not high-resistance nodes. Such nodes include the input node (driven by a voltage source), the negative input node of an op amp in the inverting configuration, and the output node of the op amp with feedback.

The op amp can impact the DAC performance from both static and dynamic viewpoints. The *gain error* of an op amp is the difference between the desired and actual output voltage of the op amp and is due to a finite value of $A_{vd}(0)$. For the inverting amplifier using resistors or capacitors, the closed-loop gain for a finite value of $A_{vd}(0)$ is expressed as

$$\frac{V_{out}}{V_{in}} = -\left(\frac{R_2}{R_1}\right)\frac{|LG|}{|LG|+1} = -\left(\frac{C_1}{C_2}\right)\frac{|LG|}{|LG|+1} \tag{1.12}$$

If the loop gain, *LG,* is not infinite, then an error exists between the desired output, and the actual output, V'_{out}. A *gain error* for the op amp in the inverting configuration for identical inputs could be given as

$$Gain\ error = \frac{V_{out} - V'_{out}}{V_{out}} = 1 - \frac{|LG|}{|LG|+1} = \frac{1}{|LG|+1} \tag{1.13}$$

1.4 DAC Architectures

1.4.1 Charge division architecture

Charge division DAC is popular in CMOS technology. From Figure 1.7, Capacitors C1 to CN are all identical, and each capacitor inject the amount of charge Q = C*VREF to the output node. Each switch is controlled by the digital thermometer code, and thus the number of nodes turned on determines the charge on the output node [1]. Other topologies can also be implemented in a binary version by using different capacitors. A significant problem with charge -division architectures is that building capacitors takes up a substantial amount of chip area. Also several nonlinearities arise and this type DAC becomes relatively inaccurate.

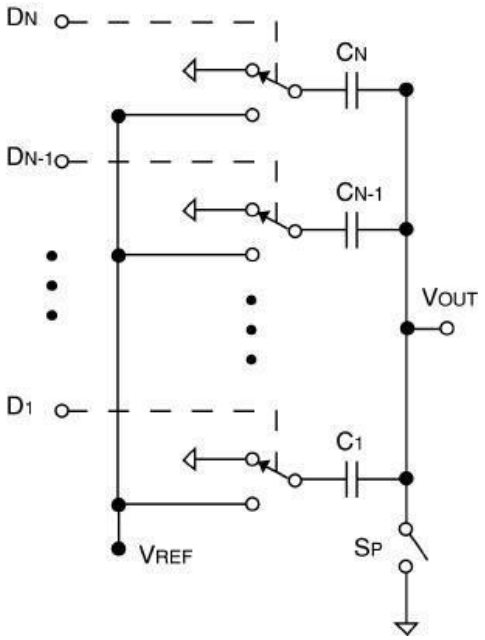

Figure 1.7 Charge Division DAC

1.4.2 Current division architecture

Typical current division architecture is shown in Fig. 1.8. The four devices on the leftmost side draw 4/7 of the reference current, while the center and right sides draw 2/7 and 1/7 of the reference, respectively. The selected currents add, giving the analog current representation of the digital input. Two major drawbacks exist in this topology. First, the stack of current dividing transistors positioned above IREF reduces the available output voltage range, and thus impractical in low voltage circuits. Second,

since each device divides the reference current, IREF must be N times greater than each of the output currents. This can require a huge device to provide the current source. [1]

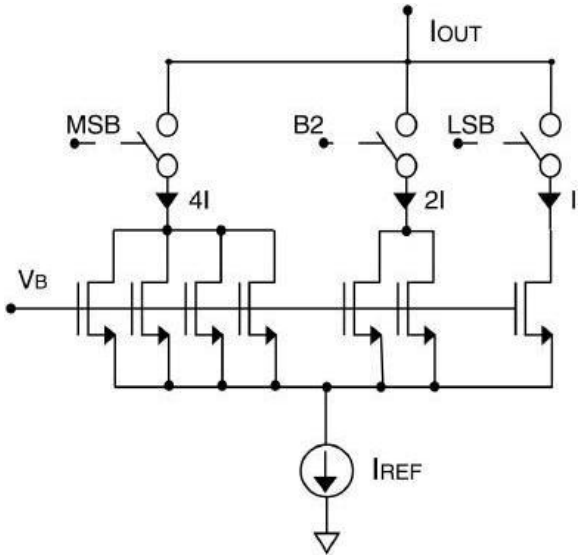

Figure 1.8 Current Division DAC

1.4.3 Current steering architecture

Current steering architecture replicates a reference current source rather than divides it in each branch of the DAC. Each branch current is switched on or off based on the input codes [5]. The architecture can achieve high speed at the cost of complex structure and relatively large power and chip area. The key part is a precise current source. There are two different kinds of current-steering DAC, binary current–steering and unit-element current-steering.

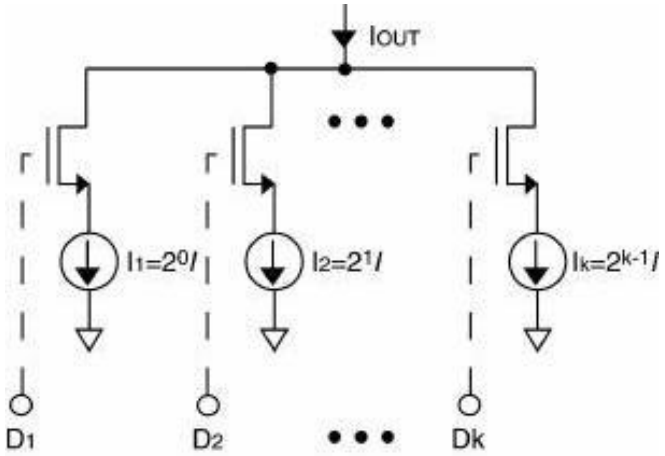

Figure 1.9 Binary Current-Steering DAC

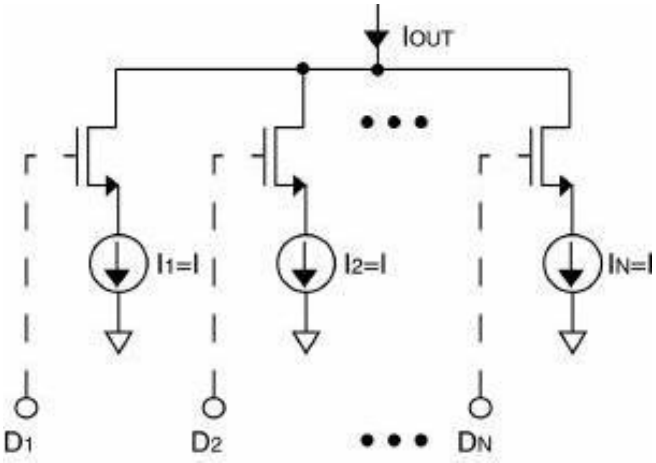

Figure 1.10 Unit-element Current-Steering DAC

In binary type, the reference current is multiplied by two and larger currents represent higher magnitude digital signals. While in unit-element architecture, each branch produces equal currents, and 2^N current source elements are needed for the N bit DAC. Therefore, when the digital input increases by 1 LSB, one addition current source is turned on and avoid the problem of two signals switching to opposite directions simultaneously. Unit-element current steering has better performance than binary ones in the following aspects. First, it can obtain higher speed. It has inherently high current and thus widely used in high-speed cases. It is traditionally fabricated with bipolar technology, but now CMOS becomes a good alternative because of matched current mirrors. Secondly, the matching performance is better. Since each current source is identical, the current produced in each branch is the same. Finally, it can ensure monotonicity. That is, the digital input increments in either direction, analog output is varied by one switch turning on or off and this type reduce glitches in this aspect. But its drawbacks are that it has complex structure. And since it needs 2^N current sources, it occupies large area, leading to large power consumption.

1.4.4 Resistor string architecture

The simplest DAC topology is resistor string architecture. It consists of 2^N identical resistors and switches. The analog output is the voltage division of the resistors. This structure results in good accuracy and is inherently monotonic. This is also fast for 8-10 bits DAC and compatible with purely digital technologies. The

disadvantage of this topology is that the output is always connected to 2^N -1 number of switches in “off” state and one switch in “on” state. When resolution becomes a big value, a large parasitic capacitance appears at the output and conversion speed becomes much slower. Also this architecture occupies large area. In addition, the settling time is large, especially for DAC with 10 bit or higher resolution. [1]

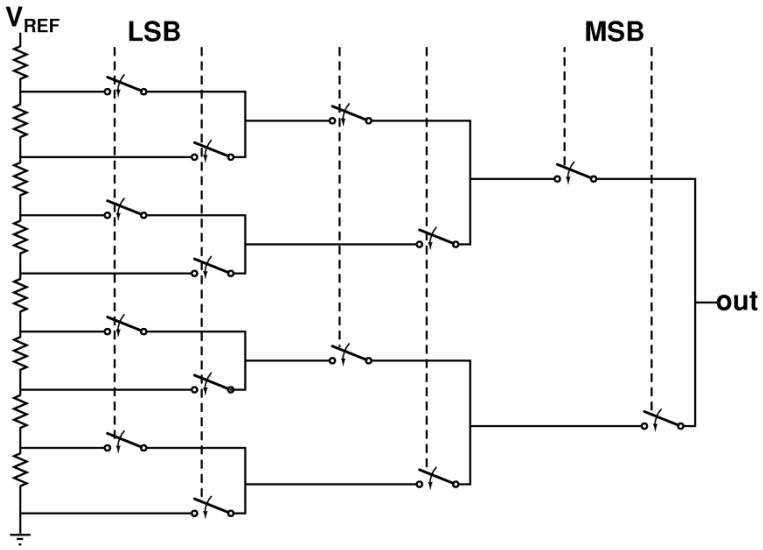

Figure 1.11 Resistor String DAC

1.4.5 R-2R Ladder architecture

Another DAC is called R-2R ladder network which consists of resistors R and 2R. For example, analyzing a 3-bit resistor ladder DAC is as follows:

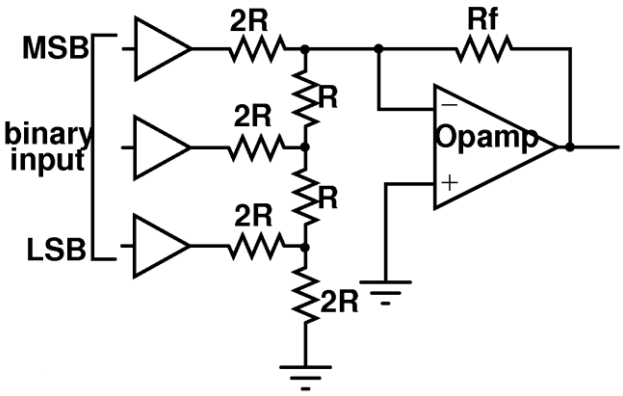

Figure 1.12 Resistor Ladder DAC

The R-2R ladder is a simple and compact resistive circuitry which can produce binary weighted current or voltage levels and is mostly used in digital-to-

analog converters [6]. Based on a reduced set of identical components, they are well suited to layout optimization for reaching low mismatch levels, critical in high-resolution flash converters. Furthermore, resistive networks are suited to laser trimming matching enhancement, allowing even higher resolution products [7].

R-2R structure can be divided into 2 subsections: one is current mode and the other one is voltage mode topology. The topologies discussed here are fully binary weighted. In other words, there is no segmentation in these topologies.

a. Current Mode R-2Rs

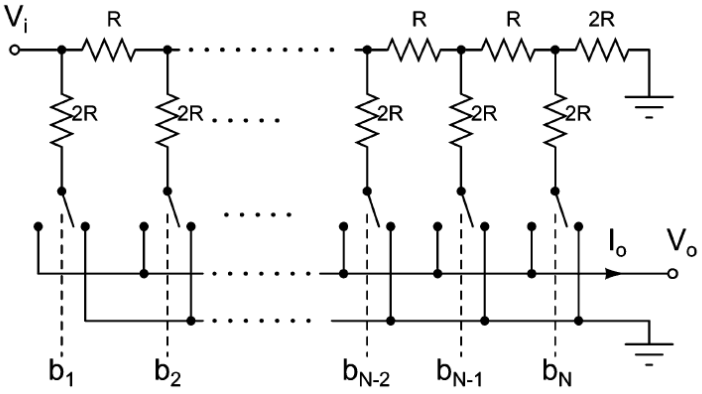

Figure 1.13 Current-mode R-2R DAC

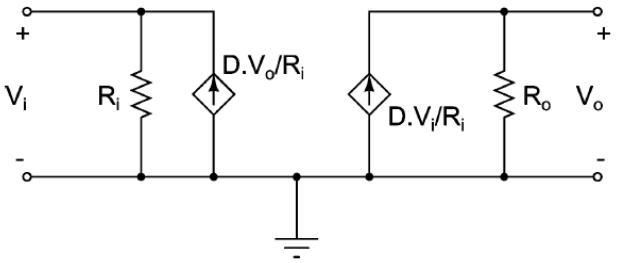

Figure 1.14 Zurada and Goodman's current-mode R-2R DAC equivalent circuit [8]

Figure 1.13 shows a current-mode ladder with N–bit resolution. The equivalent circuit proposed by Zurada and Goodman [8] is shown in Figure 1.14. In this configuration, the input impedance R_i is simply equal to R , and most of the model's complexity lies in the expression of the output resistance (Ro), which is code dependent [9].

$$Ro = \frac{3R}{\sum_{x=1}^{N} b_x(1+2^{1-2x}) - \sum_{x=2}^{N-1}\sum_{y=x+1}^{N} b_x b_y (2^{2x-2}-1)(2^{2-x-y})} \tag{1.1}$$

It should be noted that the output current source is proportional to the digital input D.

$$D = b_1 2^{-1} + b_2 2^{-2} + ... + b_N 2^{-N} \tag{1.2}$$

b. Voltage-mode R-2R

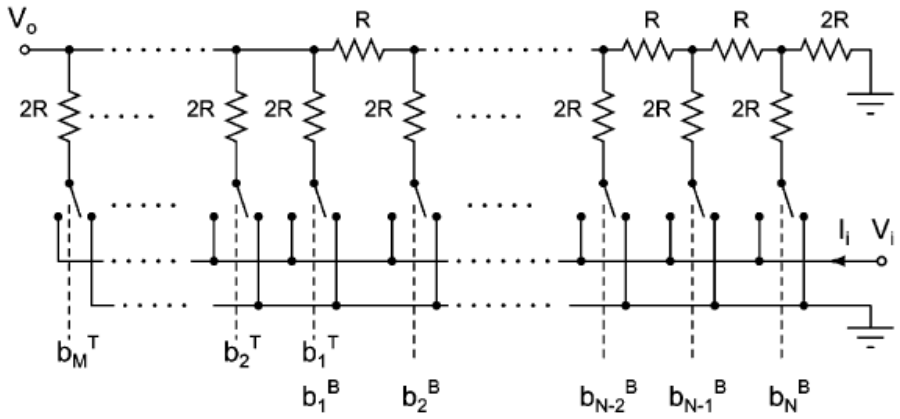

Figure 1.15 Voltage-mode R-2R

Voltage-mode operation is another common use of ladders. Figure 1.15 shows a voltage-mode R-2R ladder with resolution N. In this case, input impedance becomes code dependent, and output impedance is constant. Output impedance, when no segmentation is used, is not affected by the resolution of the converter and equal to R. This time input resistance is code-dependent and given as follows [7]:

$$Ri = 3R\left[\sum_{x=1}^{N} b_x^B (1-2^{-2x}) - \sum_{x=1}^{N-1}\sum_{y=x+1}^{N} b_x^B b_y^B (2^{2x-2}+1)(2^{-x-y+1})\right]^{-1} \tag{1.3}$$

1.5 Advantages of Cryogenic Operation

Cryogenic operation is generally stands for operation at 77 K. Many detectors for detecting faint light have to be cooled down to cryogenic temperatures to reduce thermal noise sufficiently [10]. For CMOS circuits, liquid-nitrogen (LN_2) temperature (77 K) operation provides significant performance advantages. For example, enhanced carrier mobility and reduction in wiring resistance in LN2 improve operation speed

[11]. Other improvements at 77 K include higher transconductance, higher threshold conductivity, lower power consumption and lower junction leakage current [12]. For non-planar semiconductors, such as Ge and Si, the presence of acoustic phonons and ionized impurities results in carrier scattering which significantly affects the mobility. The mobility from acoustic phonon interaction, μ_1, is given by [13]

$$\mu_1 = \frac{\sqrt{8\pi} q h^4 C_{11}}{3 E_{ds} m^{*5/2} (kT)^{3/2}} \sim (m^*)^{-5/2} T^{-3/2} \tag{1.4}$$

where h is Planck's constant, q is the electron charge, C_{11} is the average longitudinal elastic constant of the semiconductor, E_{ds} the displacement of the edge of the band per unit dilation of the lattice, and m^* is the conductivity effect mass. As can be seen from (1.4), mobility is inversely proportional to the temperature enhancing the operation speed in cryogenic temperatures.

1.6 Motivation

In this study, a voltage mode fully binary-weighted 8 bit R-2R for an ultra wide temperature range (-200 ˚C to 120 ˚C) is designed using TSMC's 90nm CMOS Mixed Signal RF Low Power 9 metal 1 poly technology. Power supply voltage (Vdd) is 1.2V. The main motivation of this DAC design is to be used in one of the ongoing DROIC (digital read-out integrated circuit) study in which a new technique is used for improving noise performance of the DROIC. The reason for choosing R-2R structure for design is that this topology is more robust than other DAC topologies for its simplicity and using less active elements [14]. 1MSps of operation with a precision of maximum 1 LSB of DNL and INL is expected. Smallest possible area is needed to balance the cost of the DAC.

The need for wide temperature range of operation can be attributed to the detector to be read-out. Considering that there are cooled and un-cooled detectors and their ROIC counterparts, wide temperature range of operation becomes essential. Also, the general approach is to make the circuit to be able to operate in room temperature as well regardless of the actual aimed temperature of operation (cryogenic or not).

Having said the need for cryogenic operation for detectors and thus read-outs, another application area of the designed DAC could be aerospace exploration or lunar

applications. The extreme temperature conditions on lunar surface can invalidate conventional electronic components and systems for control, sensing and communication. This is problematic, since the development of modular, expandable, and reconfigurable human and robotics systems for lunar missions obviously requires electronic components and integrated packaged electronics modules which can operate robustly without external thermal control [14].

The choice of DAC architecture is driven by application needs. When high speed is the motivation for instance video signal processing, wireless and wired communication systems such as cellular base stations and cable modems, current steering DACs in which an array of current sources are steered to the output resistive load directly are preferred since they are able to achieve high speed and high resolution [15, 16, 17]. Also embedded applications get benefit of this topology [18]. Even extreme environment applications like aerospace exploration frequently use current steering type of DACs [19, 20]. All of these benefits has a trade-off with power consumption and area, eventually cost.

In this project, however, a voltage mode R-2R topology is used since it enables very low power operation with reasonable accuracy, provided that the resistors are well matched added to the relatively small area. Speed on the other hand is not the best aspect of the topology. Another drawback is that it is not feasible to realize 10 bits or more with the resistor based structures. As the chosen application area of the designed circuit, DROIC, will use the DAC inside the fine quantization part which enables a satisfactory accuracy even with 8-bits. The DAC reaches up to 20 MSps at cryogenic temperature (-200 $^{\circ}$C) and 8 MSps at room conditions. This is much greater than the needs of the DROIC circuitry. Also, the low power operation (425 μW for cryo and only 1.1mW for room) wouldn't have been achieved with the current steering topologies since the similar circuits are consuming powers from tens to a few hundreds of mW.

In this thesis, by considering the extreme temperature capability and the advantages explained above, an R-2R resistor ladder is chosen for design.

1.7 Thesis organization

In Chapter 2, the R-2R design is given in detail including bandgap based voltage reference for wide temperature range of operation, summing amplifier and the buffer and finally digital circuitry (switches),. This section both includes schematic and layout level designs. Also, the laying out of the resistor string is studied in detail and explained the elimination of possible gradients which could be attributed to the fabrication defects. Also, post-layout simulation results for each building block is given and discussed. Complete circuit's schematic and post-layout simulations are also discussed in this section.

Finally, in Chapter 3, conclusions of the study are provided, problems are defined and the future study is addressed.

2 DAC BUILDING BLOCKS

The designed DAC consists of several sub-circuits. These are voltage reference generator, operational amplifier, the resistor network and switches. In this section each building block will be examined, their simulation results will be discussed and finally the design of complete circuitry will be presented.

2.1 Voltage Reference Circuit

2.1.1 2.1.1. Design of the circuit

Voltage reference generators are indispensable in many analog integrated circuits one of which is digital-to-analog converter. The reason why the voltage reference circuit is so important is that it can generate stable reference voltage, which is insensitive to the variation of the temperature and the supply voltage [21].

Voltage reference circuits are generally based on the band-gap approach introduced by Robert Widlar in the integrated circuit LM113 [22, 23]. Since the band-gap phenomenon is basically based on BJTs it is rather challenging to realize these circuits with purely CMOS technologies. It is possible to realize BJTs with CMOS technology however they require more fabrication steps and lithography masks. Furthermore, traditional band-gap circuits are generating typically around 1.2V which is close to the band-gap of Silicon. This means that at least a supply voltage of 1.4 V is necessary which makes it not feasible for use in low-voltage circuits [24].

In this project, the design proposed by [21], where sub-threshold MOSFETS are utilized, is adopted and realized a wider temperature range of operation at the expense of increased average power consumption within the range covered. The design is based on the well-known proportional-to-absolute-temperature (PTAT) circuit [25]. Schematic of the circuit is given in Figure 2.1.

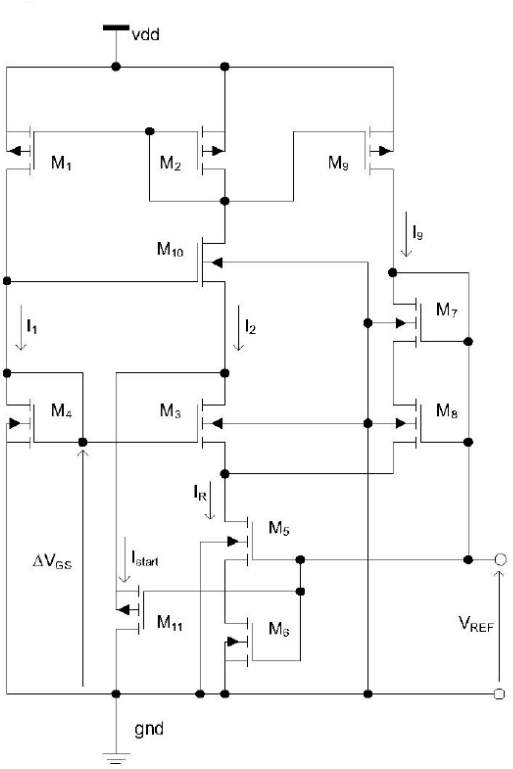

Figure 2.1 Schematic of the voltage reference circuit [21]

Table 2.1 Transistor sizes used in the design

Transistor	**W/L (µm)**
M_1, M_2, M_9	5 / 9
M_3	152 / 0.4
M_4	40 / 0.4
M_5, M_6, M_7, M_8	5 / 1.37
M_{10}	10 / 2
M_{11}	40 / 0.2

The transistor sizes are given in Table 2.1. In this topology, M_1 to M_4 basically realize the well-known PTAT circuitry. As current sources, both M_1 and M_2 operate in saturation where M_3 and M_4 are in sub-threshold region. These four realize a close loop greater than unity. As long as M_3 and M_4 remain in sub-threshold, their gate voltage could be written as in (2.2) [21]

$$\Delta V_{GS} = V_T \ln(K) \tag{2.2}$$

where $V_T=kT/q$ is the thermal voltage, $K=(S_1/S_2)*(S_3/S_4)$ and S_1,S_2,S_3,S_4 are W/L ratios of the corresponding transistors. The compensation circuitry is realized by transistors M_5 to M_8. I9, I_1 and I_2 are equal current sources. The voltage indicated by (2.2) is summed with Vds7 and Vds8, which have negative temperature coefficients [21]. This makes Vref robust against temperature variations.

The p-type current sources M_1, M_2 and M_9 are 2.5V tolerant MOSFETs supplied by the technology to make it possible to make the circuit robust against the supply voltage variations. M_{10} is also 2.5V tolerant but it is a native NMOS (depletion-mode transistor which has negative threshold voltage around -80mV, also supplied by the technology) which secures voltage level of M_3 drain to be always close to (2.2) thus enabling the isolation of these high-voltage tolerant devices from the rest of the transistors which are 1.2V tolerant only. The purpose of M_{11} is to act as a startup circuitry. Since the PTAT current generator could also be stable for zero current, the use of M11 which is biased by the stable output voltage V_{REF} causes a current spike in the current generator circuitry and eventually turns off since its gate to source voltage becomes close to zero.

In a weak inversion region, equations (2.3) and (2.4) could be used [21].

$$I_9 = I_S e^{\frac{V_{REF}-V_{THn}-n\Delta V_{GS}}{nV_T}} \tag{2.3}$$

$$I_R = I_S e^{\frac{V_{REF}-V_{THn}}{nV_T}} \left(1-e^{-\frac{\Delta V_{GS}}{V_T}}\right) \tag{2.4}$$

where I_S is the specific current, n is the subthreshold slope factor whose value is determined by the process, V_{THn} is the threshold voltage of the NMOS transistor. Furthermore, (2.5) can easily be seen from Figure 2.1 as

$$I_R = 2I_9 \tag{2.5}$$

If (2.3) and (2.4) is substituted into (2.5), then (2.6) and (2.7) could be obtained respectfully.

$$I_S e^{\frac{V_{REF}-V_{THn}}{nV_T}}\left(1-e^{-\frac{\Delta V_{GS}}{V_T}}\right)=2I_S e^{\frac{V_{REF}-V_{THn}-n\Delta V_{GS}}{nV_T}} \tag{2.6}$$

$$\frac{\Delta V_{GS}}{V_T}=\ln 3 \tag{2.7}$$

Substituting (2.7) into (2.3) will yield (2.8).

$$I_9=\frac{1}{3}I_S e^{\frac{V_{REF}-V_{THn}}{nV_T}} \tag{2.8}$$

Finally, if (2.8) is rearranged and natural logarithm of both sides are taken reference voltage expression is obtained as follows,

$$V_{REF}=nV_T\ln\left(3I_9\right)+V_{THn} \tag{2.9}$$

Here, thermal voltage V_T is the PTAT part and the threshold voltage is inversely proportional to the temperature (CTAT) which overall realizes a temperature invariant reference voltage.

The layout of the designed circuit is shown in Figure 2.2. The layout of the circuitry may seem strangely apart and far from being compact however there have been some issues during this floor planning. One is that the native NMOS has strict DRC rules unlike the enhancement mode MOSFETS which caused some certain seperation. Another issue is that the transistor M_3 of the PTAT circuitry has a large aspect ratio of 152/0.4 in order to realize the desired output voltage level which could be attributed to the (2.2) and (2.3). During schematic level design, initially no fingering was used in any of the transistors. During the laying out process, it was observed that fingering has quite an impact on the circuit even in schematic level simulations unlike the traditional saturation mode MOSFET based designs.

It is found out the sub-threshold slope does not only depend on the gate length but also on the number of gate finger. The dependence of number of gate finger is more obvious in shorter channel length devices because of more obvious drain-induced barrier lowering effect and poorer electrostatic integrity [26]. For this reason, the previously designed channel lengths are increased from 200nm to 400nm in the

circuitry, with their widths increased as well, and this effect lessened. Further fingering could have been possible but at the cost of larger transistor sizes. Considering that the current width of M3 is already 152µm, this path isn't chosen. Finally, some extra separation is done to realize a rectangle like shape for the building block.

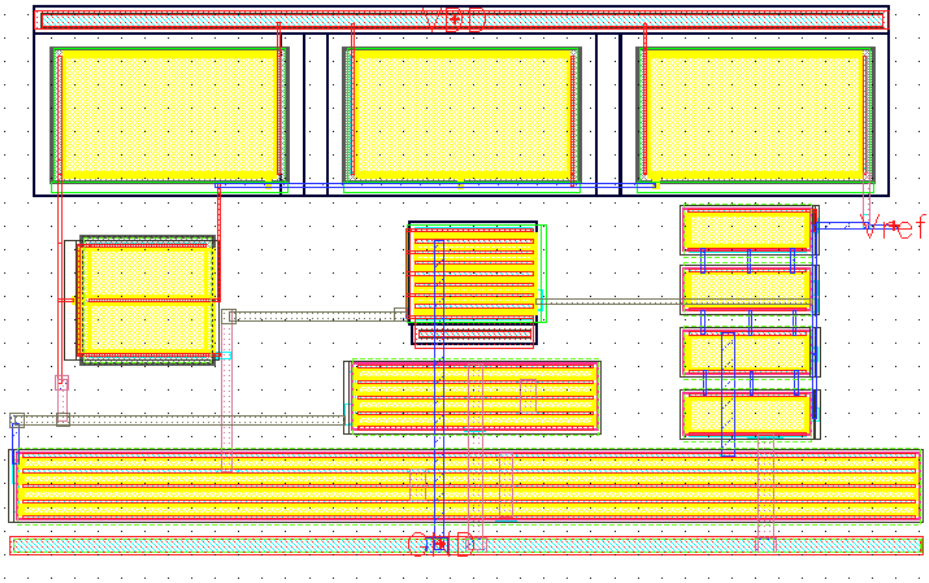

Figure 2.2 Layout of the voltage reference circuit (23.5µm x 39µm)

2.1.2 Simulation Results

The generated voltage reference is given in Figure 2.3 as a function of the temperature. The bandgap based voltage generator has a temperature coefficient of **46ppm/°C** within the range of -150°C to 120°C. From -150°C to -200°C, the produced reference voltage begins to lose its immunity against the temperature variation. This is because the current sources M_1, M_2 and M_9 start to operate in the sub-threshold region where they are supposed to stay in the saturation.

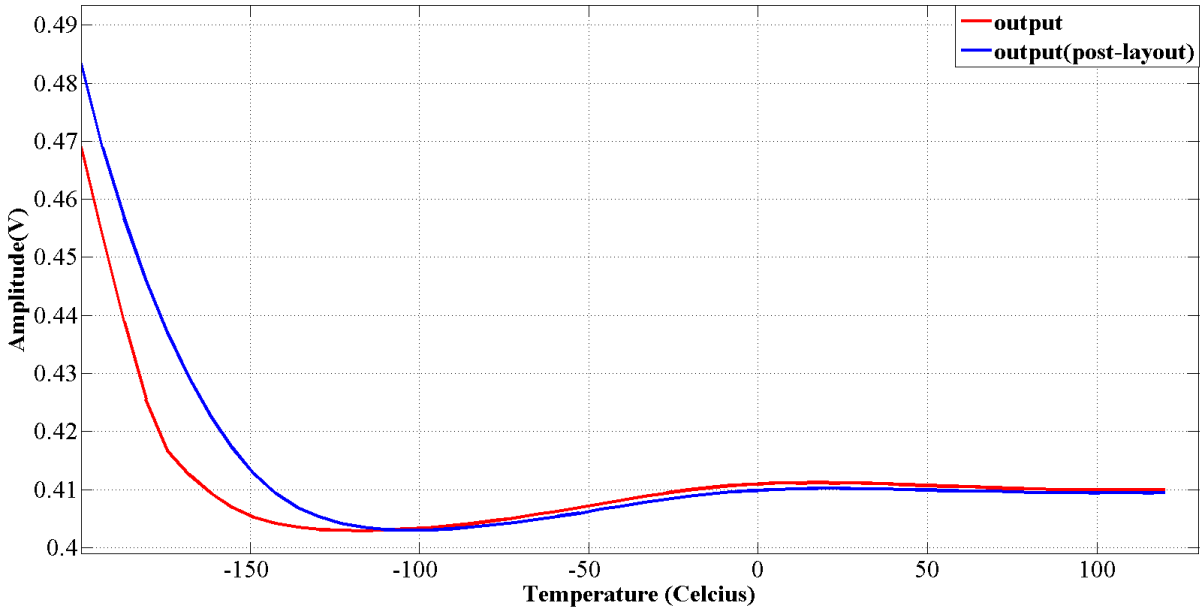

Figure 2.3 The output voltage versus temperature for Vdd=1.2V

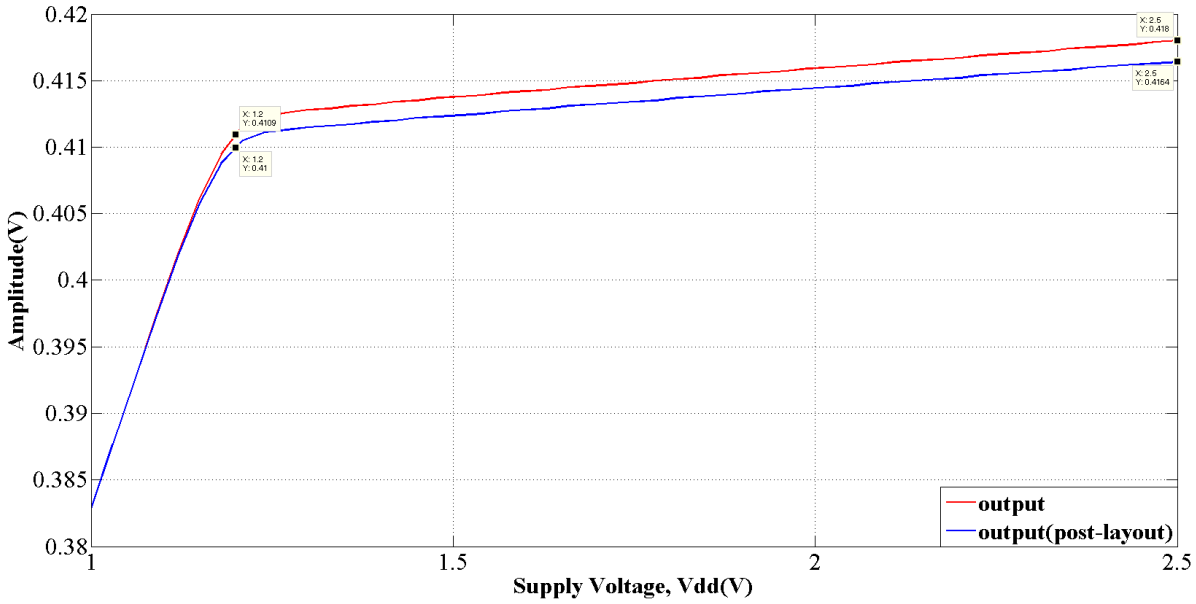

Figure 2.4 The reference voltage V_{REF} as a function of supply voltage Vdd

The excessive power supply immunity of the designed circuit can be observed in Figure 2.4. The voltage reference is quite robust against the variation of the Vdd from 1.2V to 2.5V. This property is obtained through the use of 2.5V tolerant PMOS

transistors as current sources and a native NMOS to isolate the remaining circuitry from the excessive supply voltage.

The total current drawn from the power supply is only **585nA** for 27°C and this corresponds to a total power consumption of **700nW** for a Vdd of 1.2V which indicates that it could be used in some low power applications where 1.2V Vdd is acceptable.

2.2 Operational Amplifier

2.2.1 Design of the circuit

In this thesis, an operational amplifier is designed and used in two different configurations. First one is the buffer in order to drive the resistive network at the output of the previously designed voltage reference circuit as the circuit fails to drive the network without a buffer. The second use is as a summing amplifier at the output of the resistive network. The analog voltage corresponding to the specific digital word needs to be summed over a resistive feedback through an amplifier. The output of the amplifier, being also the output of the whole circuitry, should be able to drive the output pad of the circuit and also the oscilloscope probe which will be used in measurement later on. The amplifier designed is a basic two-stage OTA and the schematic is given in Figure 2.5. At the input stage of the amplifier, PMOS transistors are preferred for some reasons. First reason is that PMOS transistors are basically more robust against the noise thanks to the nwell they are built in. Also the speed is not the first concern in this project that is why there is the freedom to avoid NMOS counterparts. The second reason is that the output voltage of the reference circuit is around 410mV in a wide range of temperature (from -150 °C to 120 °C) and this voltage is also biasing the positive input terminal of the summing amplifier. Since for a Vdd of 1.2V, this 410mV maybe a problem for NMOS input transistors since when it is the case, the minimum common mode voltage level should be $2V_{ov}+V_{TH}$ ($1V_{ov}$ for the tail current source and 1 V_{GS} for the input transistor operation). This may not seem problematic with this technology (there are NMOS transistors having a threshold voltage of as low as 350mV) however it is only feasible at room temperature and above. This could be attributed to the negative temperature dependency of the threshold voltages as indicated by [13]

$$V_{TH}(T) = V_{TH}(T_0) - k(T - T_0) \tag{2.10}$$

The interpretation of (2.10) is that as the temperature goes down, threshold voltages are basically building up (2mV per K is observed at 90nm technology) making it impossible to operate with a bias voltage as low as 400mV for an NMOS input pair. This makes it obligatory use PMOS which gives a better noise performance yet a slower operation for the same size NMOS.

In order to realize bias current of the amplifier the popular cascode current source topology is used (M_9 to M_{12} and the bias resistor R_b). For stability issue, famous RC compensation is preferred. As a compensation capacitor, MIM (metal-insulator-metal) capacitors supplied by the technology are used. Layout of the circuit is depicted in Figure 2.6. In order to optimize the area fingering is used in transistors. This enables reasonable aspect ratios for devices also the frequency response of the circuit is aided thanks to the reduced source/drain capacitances as well as reduced gate resistances.

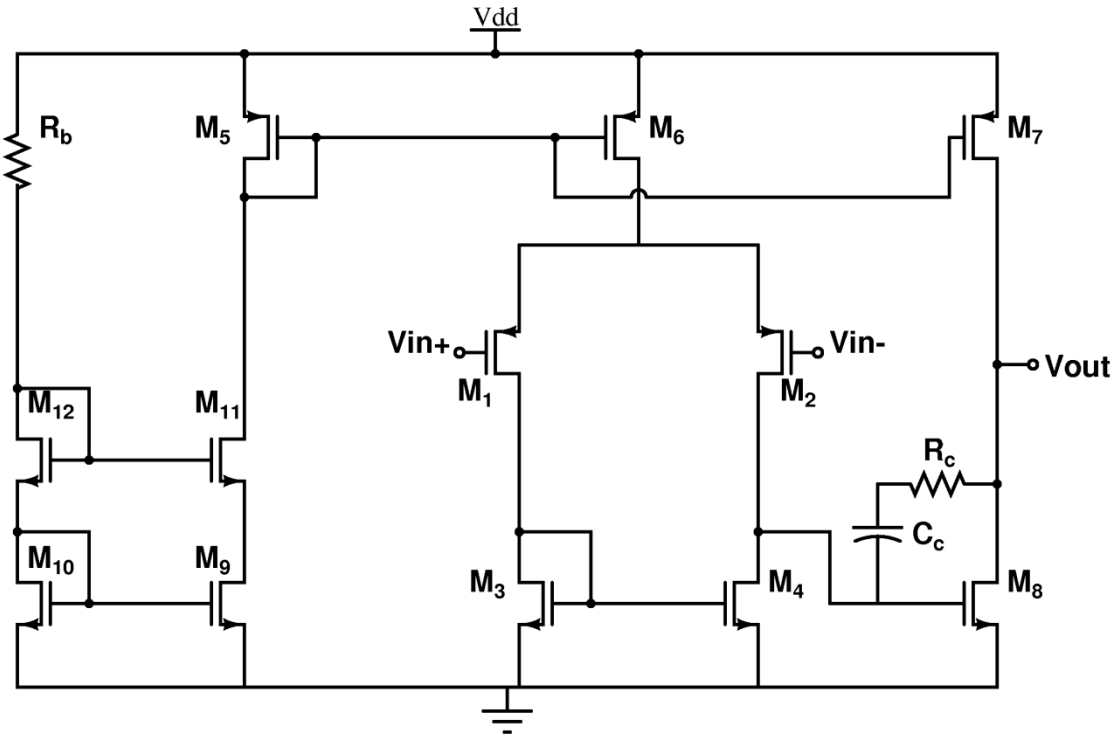

Figure 2.5 Schematic of the operational amplifier

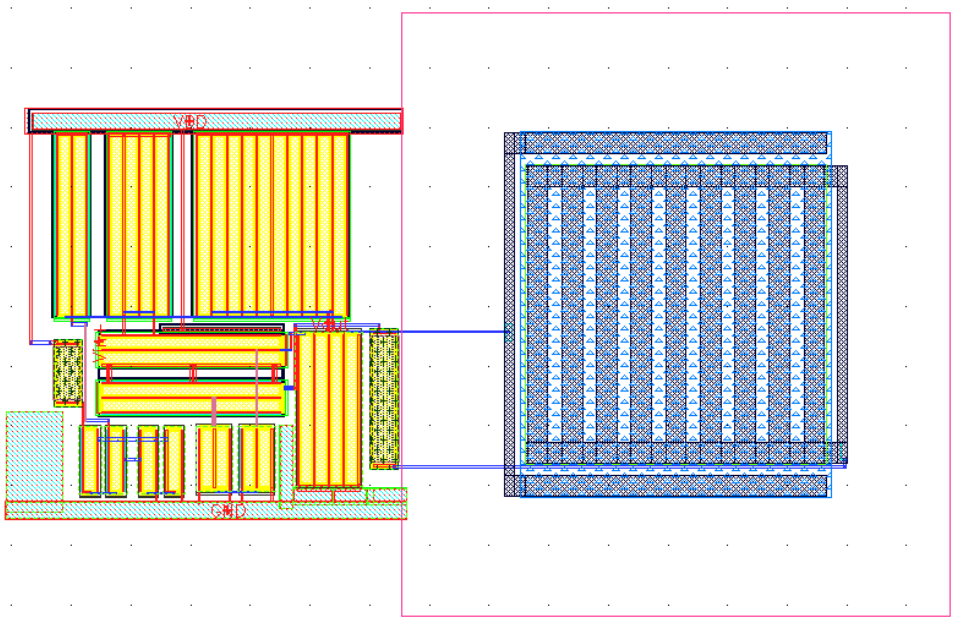

Figure 2.6 Layout of the operational amplifier (80µm x 50µm)

The components used in the design are summarized in Table 2.2.

Table 2.2 Device metrics used in the design of two-stage Opamp

Device Name	Parameter
M_1, M_2	30µm/1µm
M_3, M_4	10µm/1µm
M_5	30µm/1µm
M_6	60µm/1µm
M_7	150µm/1µm
M_8	50µm/1µm
M_9, M_{10}, M_{11}, M_{12}	5.2µm/1µm
R_b	1kΩ
R_C	2.3kΩ
C_C	1.3pF

2.2.2 Simulation Results

The operational amplifier designed to be used in two different purposes. The first one is the output buffer for the V_{REF} generator circuit since it is unable to drive the

resistive network without a buffer. The second one is a summing amplifier in a resistive feedback configuration.

In this section, basic open-loop characteristics like gain and phase margin and also the pulse response of the designed opamp will be given. Figure 2.7 depicts the open-loop DC gain and the phase of the amplifier for three temperature values. Figure 2.8-9 on the other hand, depicts the pulse responses regarding 1MHz and 10MHz inputs for buffer configuration.

The post-layout simulation results of the operational amplifier are summarized in Table 2.3. Comparing the characteristics through the table, it is interesting that the power consumption at cryogenic temperature is dramatically reduced. This is expected because the cascode bias current source of the amplifier is not temperature independent and the current drawn from the amplifier is reduced as the temperature goes down due to the increase of the threshold voltages as explained in section 1.5. On the other hand, cryogenic temperature still has the best bandwidth and the gain thanks to the benefits of the temperature decrease which is also covered in Chapter 1.5. Similarly, as the temperature increases, these performance metrics get worse which could also be seen in Table 2.3 provided that column 2 and 3 are compared.

Table 2.3 Performance metrics of the operational amplifier

Parameter	**-200°C**	**27°C**	**120°C**
DC Gain	60.55 dB	51.35 dB	47.22 dB
Phase Margin(deg)	59.9	62.9	60.8
Gain BW	96.03 Mhz	45.5Mhz	37.2Mhz
Power Consumption	196 µW	550µW	600µW
Slew-Rate	7.92 V/µs	8 V/µs	6.95 V/µs
Load	10MΩ // 10pF	10MΩ // 10pF	10MΩ // 10pF

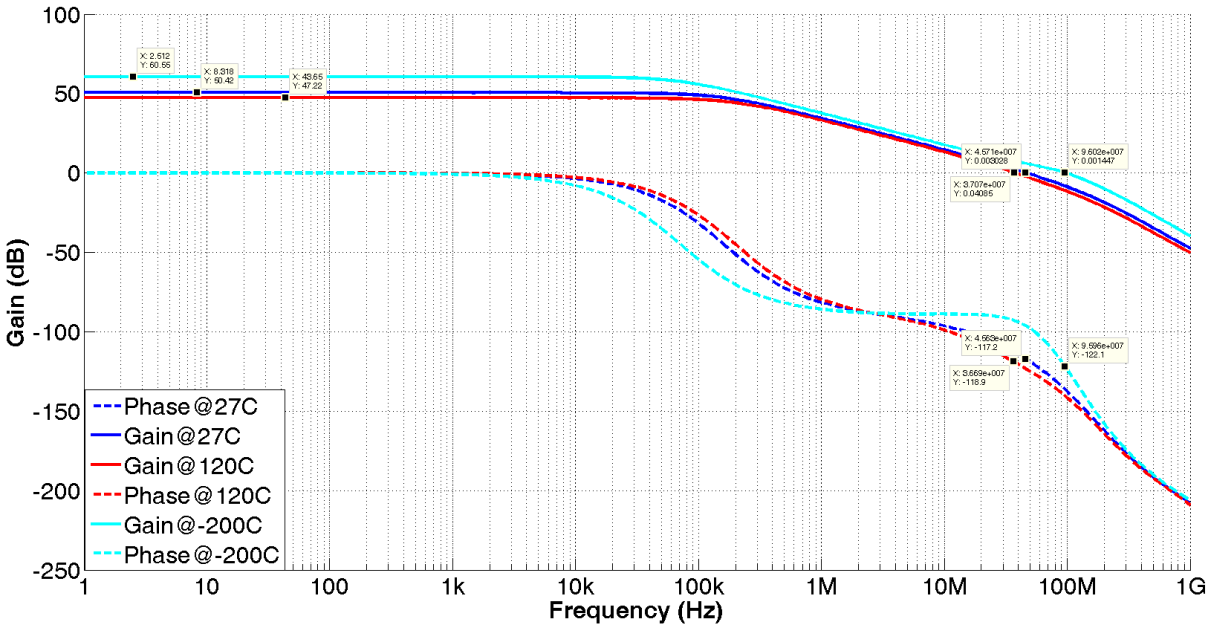

Figure 2.7 Gain and phase of the operational amplifier for three temperatures

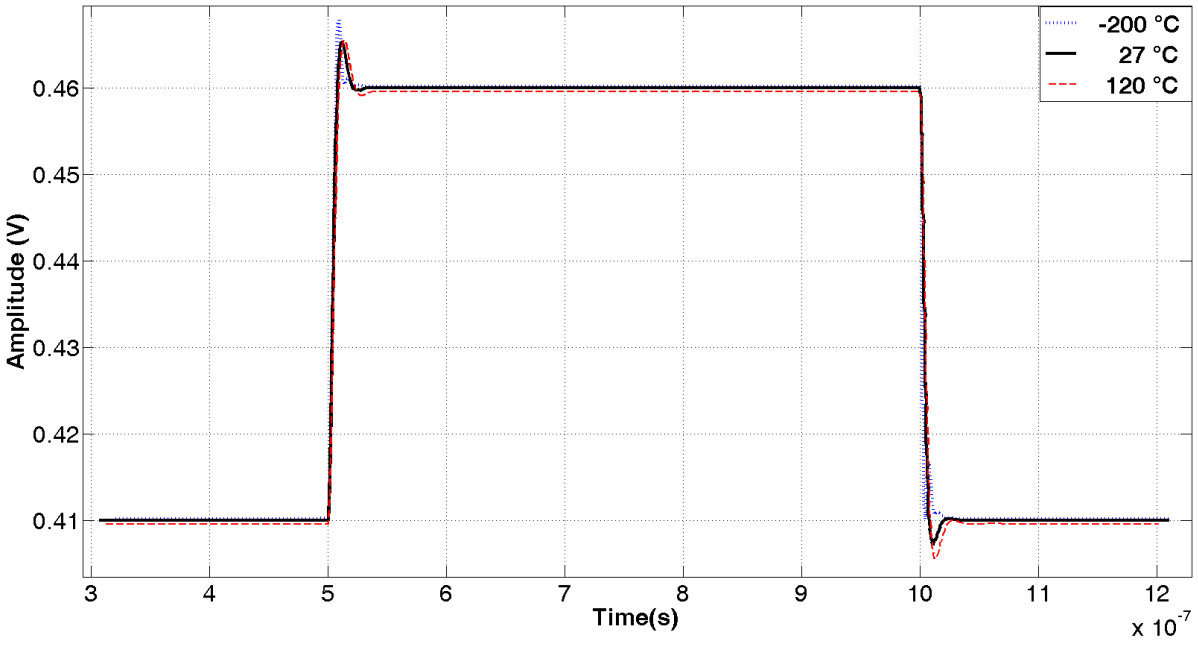

Figure 2.8 1 MHz pulse response of the buffer

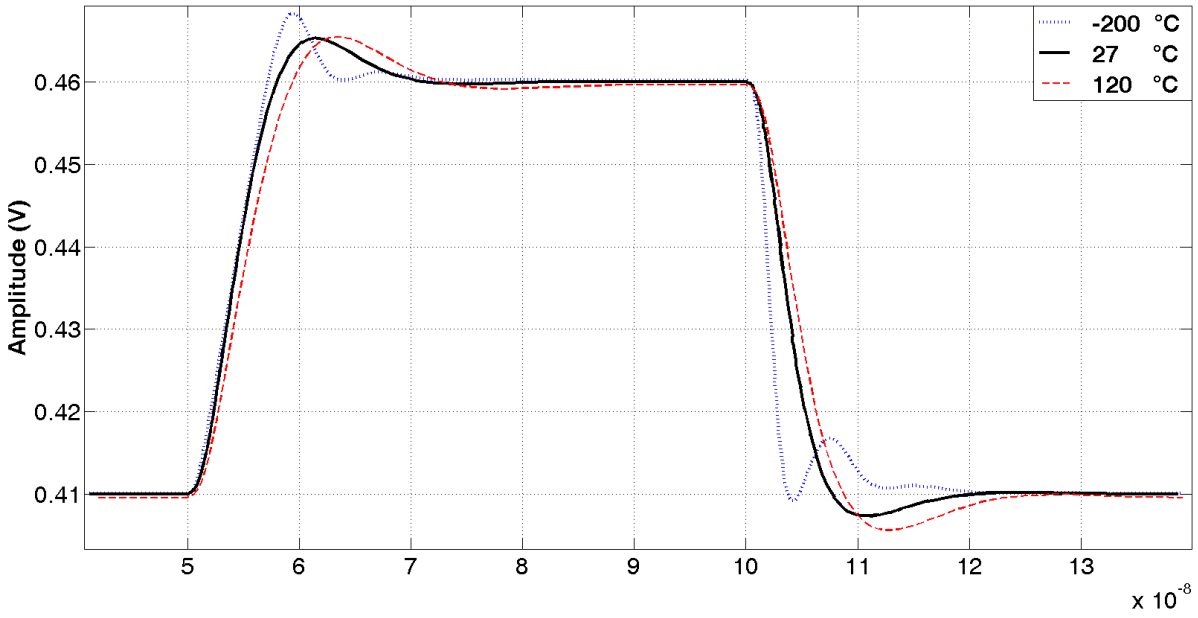

Figure 2.9 10 MHz pulse response of the buffer

It is important to note that for a pulse with 50mV amplitude, in all three temperature conditions, the operational amplifier manages to settle before the next transition occurs even in 10MHz frequency. Having said that the amplifier is capable of operation with a pulse of 10MHz, it suits better to 1MHz operation except for cryogenic temperature.

2.3 R-2R DAC Core

2.3.1 Design of the circuit

The core of the designed DAC can be seen in Figure 2.10. It should be noted that Vdc is generated through the use of a replica Vref generator circuitry and thus no external bias is needed for the operational amplifier. The principle of operation of this R-2R topology is very straight forward. It could be explained with the help of Thevenin's theorem. Just to illustrate the principle, a 4-bit representation will be used for ease. 4-bit version of the topology is given in Figure 2.11.

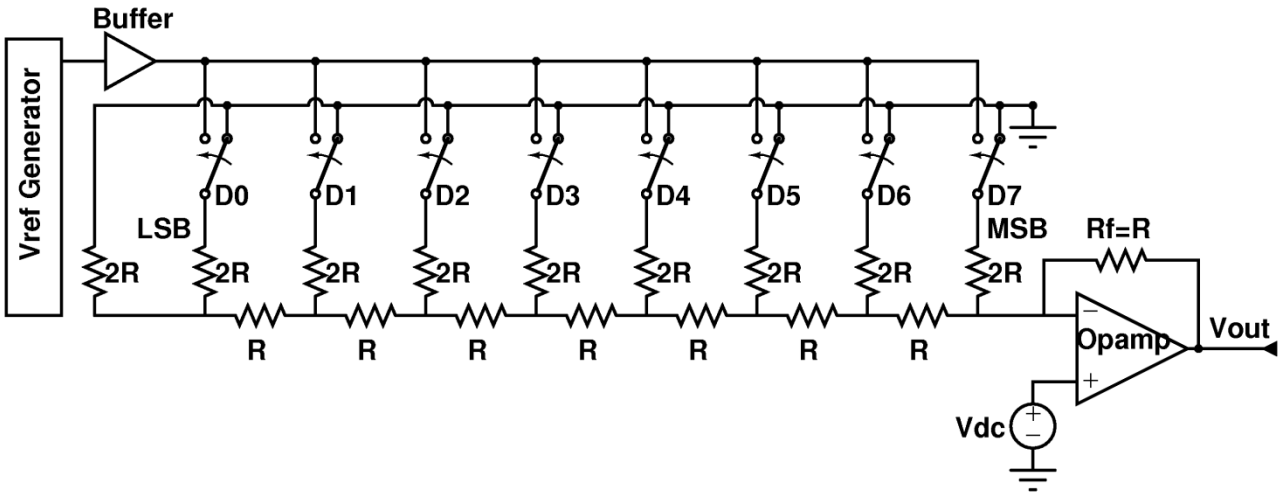

Figure 2.10 Core of the designed R-2R DAC

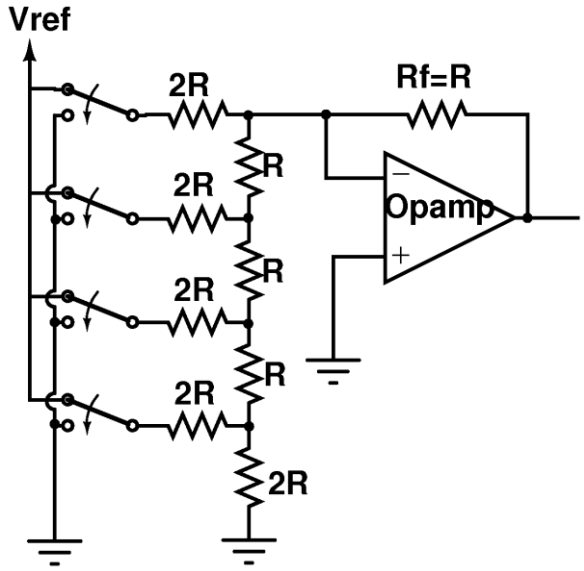

Figure 2.11 4 bit R-2R Ladder DAC

Using superposition technique, all the higher order bits are grounded where the LSB is driven by the voltage V_0 as indicated in Figure 2.12. Thevenin's equivalent of the circuit in the box 1 is basically a V_{TH} of half of the prior and a R_{TH} of R. If the equivalent process is continued in this manner, it is not challenging to reach the final circuitry given in the box 5. As can be observed, LSB makes a contribution of $V/(2^N)$ to the output, here N is equal to 4. Similar procedure could be followed for the higher order bits and it is easy to end up with a contribution of V/2 by MSB. Finally, according

to the superposition principle, all these contributions are summed and the input-output relationship of the DAC could be derived. What is left with is basically a summing amplifier expression. For 4-bit equivalent, following relation is obtained,

$$V_{out} = -\frac{R_f}{R} V_{REF} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right] \tag{2.11}$$

where D_n stands for the corresponding bit either 0 or 1 according to the value of the binary-weighted digital word.

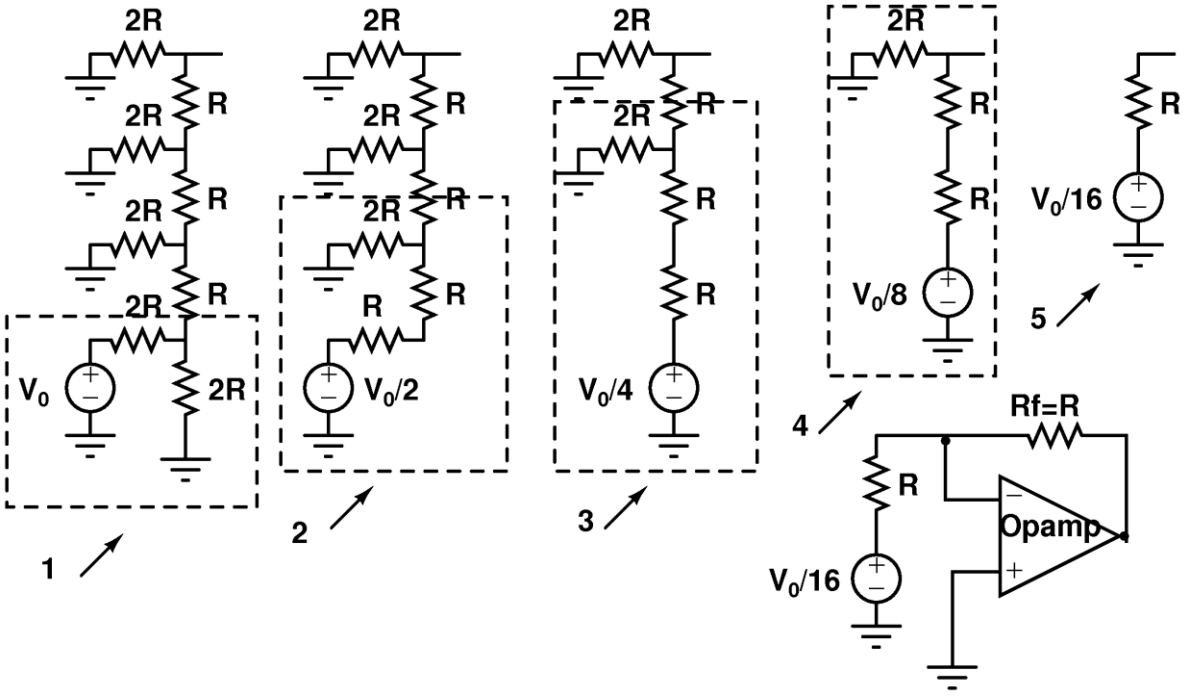

Figure 2.12 Explanation of the principle of operation for a 4bit R-2R DAC

The result obtained in (2.11) could be generalized and for 8-bits (2.5) is easily derived as

$$V_{out} = -\frac{R_f}{R} V_{REF} \left[\frac{D_0}{256} + \frac{D_1}{128} + \frac{D_2}{64} + \frac{D_3}{32} + \frac{D_4}{16} + \frac{D_5}{8} + \frac{D_6}{4} + \frac{D_7}{2} \right] \tag{2.12}$$

In our case, it should be noted that the summing amplifier's positive node is connected with a DC level, which is also equal to the V_{REF} taken from the other voltage reference circuit and this gives a DC shift of V_{REF} to the output. This concludes that our scaling range is from V_{REF} to V_{REF} + (2.12), which is almost equal to 2*V_{REF} for full scale.

To eliminate the minus sign in (2.12) and obtain an analog output which is increasing or decreasing in the same direction of the digital word, the switches are reversely controlled rather than realizing the summing part in a positive manner.

In order to eliminate possible gradients which occur during the fabrication, the quadrature layout style where each component is split into four and placed in a symmetrical manner for each axis could be used. This layout style compensates the effects of gradients or other systematic mismatches [27, 28]. Another way to obtain a similar performance could be the use of method proposed by [29] and split every resistor into two and place them symmetrical as well. This method, so called cross-coupled pair, is preferred due to the area advantage. Furthermore, splitting resistors into four rather than two makes it a very challenging task to route them.

In the design R is chosen as 10k. Every R is split into two and realized as combination of two 5ks. This so called two dimensional common centroid methodology is depicted in Figure 2.13. With this method, a 2R or two Rs are then obtained in a square. Since the elements are placed in a symmetrical manner, provided that a linear gradient occur at each axis, this technique is able to eliminate the possible errors on the resistor values.

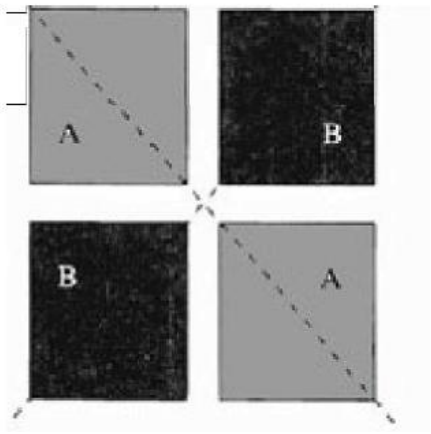

Figure 2.13 Two dimensional common centroid array [29]

The resistive network is given in Figure 2.14. As can be followed from the figure, a total of 50 resistors are needed. The method above is applied to a larger scale and these resistors are placed symmetrically. The layout of the string is depicted in Figure 2.15. It can be seen that there are unused resistors in the floor planning. These are determined as dummy resistors in order to realize a similar environment for the resistors and also avoid etching problems for the resistors at the sides. Also, a square like aspect-ratio is preferred in order to make circuit as compact as possible [29].

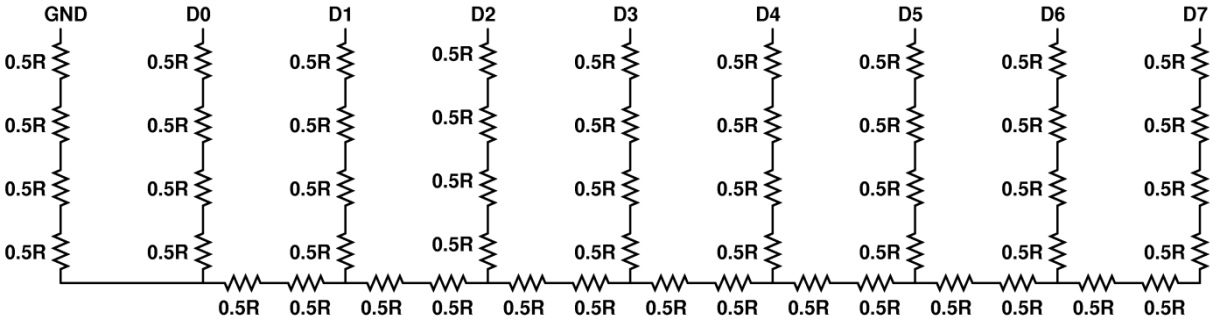

Figure 2.14 Schematic of the resistor string

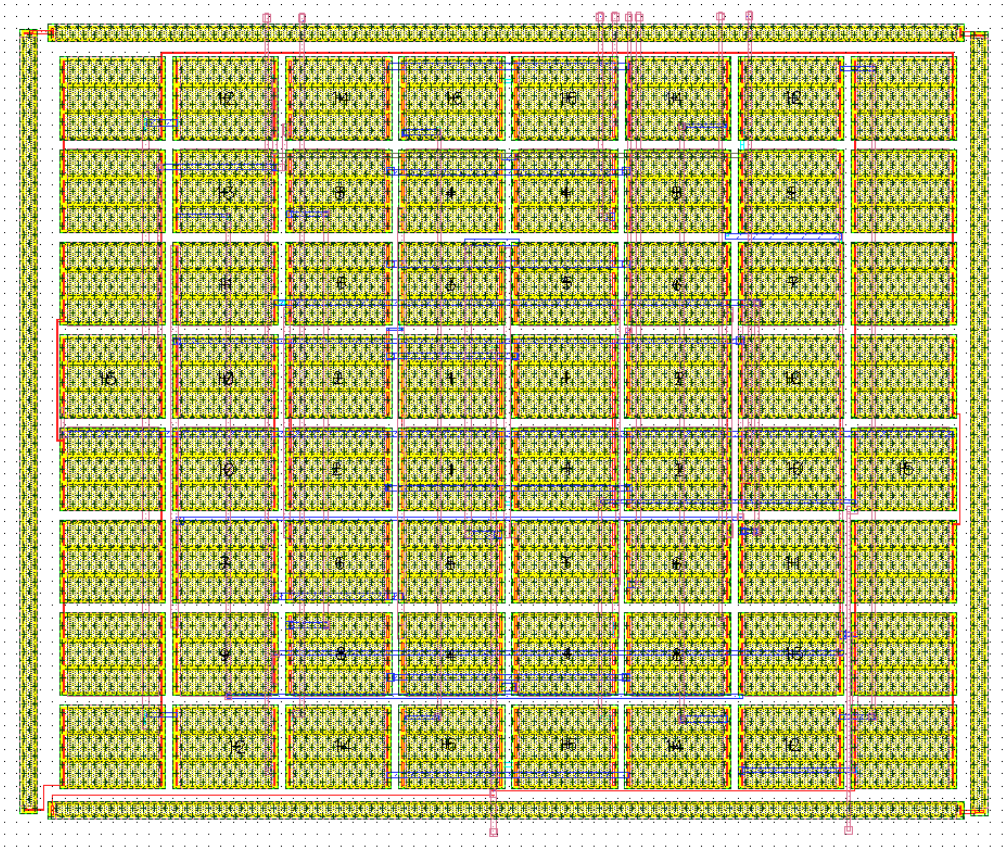

Figure 2.15 Layout of the resistor string (65µm x 80µm)

2.4 Digital Circuitry (Switches)

2.4.1 Design of the circuit

Since the chosen topology necessities the connection of either reference voltage or the ground to the corresponding bit, as a simple solution two NMOS transistors are used for this purpose. The gates of the two must be fed with an inverse control signal giving the circuit ability to choose either Vref or Gnd connection. This could also be considered a simple 1-to-2 multiplexer. For inverting the control signal a CMOS inverter is used. The schematic of the switch is given in Figure 2.16.

The chosen W/L of NMOS switches are both 5u/100n. 2.5u/100n and 1u/100n are the sizes of NMOS and PMOS used in the inverter. The reason why NMOS transistors are used instead of PMOS is that they are faster compared to a same-sized PMOS due to the fact that the mobility values are generally 2 to 3 times higher at NMOS transistors. This is surely because of the superiority of the electrons which are the carriers of NMOS, over electron holes which are the carriers of PMOS.

In addition to speed issues, another thing to keep in mind is on resistance of the switches. This phenomenon, denoted as Ron is given in (2.13)

$$Ron = \frac{1}{\mu nCox \frac{W}{L}(V_{GS} - V_T)} \tag{2.13}$$

The technology used in this project, TSMC 90nm, has been found out to have a $\mu nCox$ of 370μA/V^2 for typical NMOS transistors. W/L is chosen as 5u/100n. Since at the summing point of the resistor string there is the bias voltage of the amplifier, which is also generated by the voltage reference circuit and equal to V_{ref}=412mV for room temperature, this causes a voltage shift at the source terminal of the NMOS transistor which in turn causes a lower V_{GS} . Taking this value in account, for an on switch, V_{GS}=791mV and the corresponding V_T=587mV. Using these values in (2.1), Ron has been calculated as 265 Ω which is considerably small compared to 2R=20 k Ω which is in series to the switch. As can be seen from (2.1), one can to choose to make the W/L ratio as big as possible however there is certainly a trade-off between speed, area consumption and also glitches. The bigger the device is, it is more likely to generate glitches in the output.

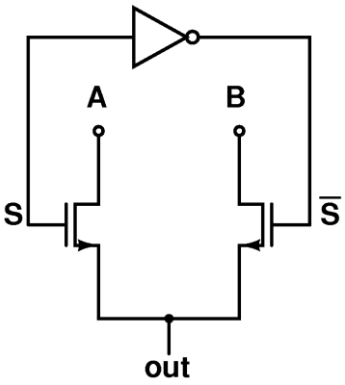

Figure 2.16 Schematic of the NMOS switch

Figure 2.17 illustrates the layout of the designed switch. Since the transistors used in this design are considerably small and do not have a large aspect ratio, fingering is not used here. However, if it was needed to reduce the gate resistance due to the parallel connection of the poly and the source/drain capacitances thanks to the sharing it could have been fingered as well.

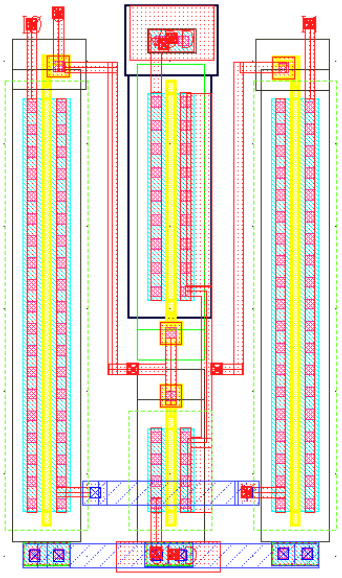

Figure 2.17 Layout of the designed switch (8 switch, total area 32µm x 9µm)

2.4.2 Simulation Results

In this section, pulse response of the designed inverter is observed. For this purpose, two different clock frequencies, 1 MHz and 10 MHz respectively, are applied to the input of the circuit and three different temperature regions are examined. As the

load of the inverter, the equivalent of the oscilloscope probe which is a 10 MΩ // 10pF is used. Similar procedure is followed for the NMOS switches and through a control signal of 1 MHz and 10 MHz, the circuitry is switched from V_{REF} to ground back and forth. This time, switches are connected directly to the resistive network in order to evaluate the actual performance.

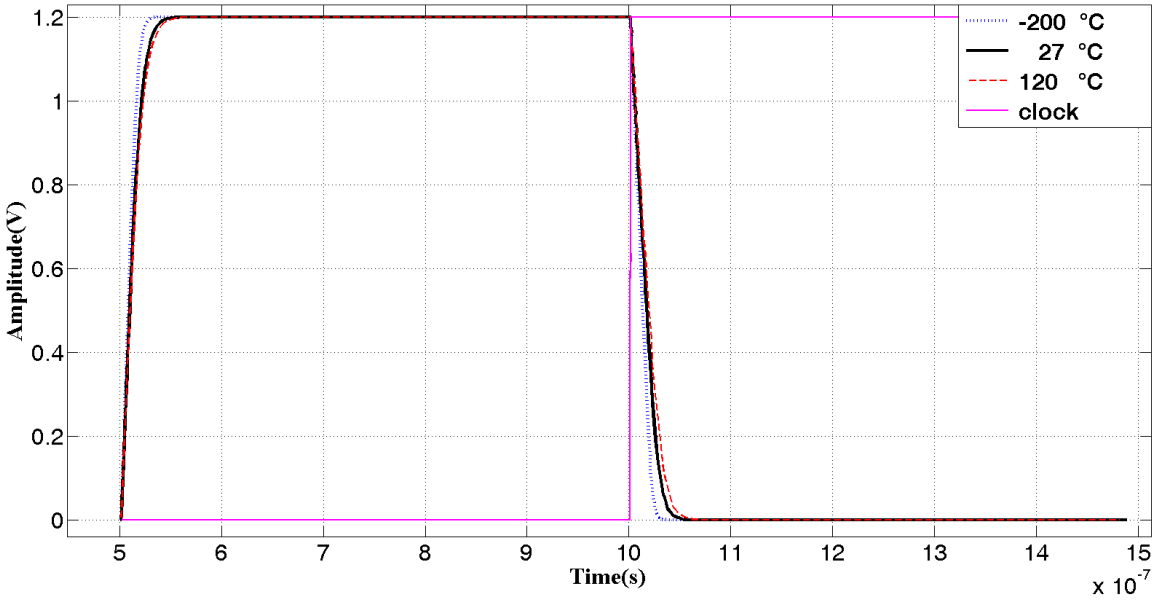

Figure 2.18 Inverter response for a 1 MHz input clock

As can be observed from the Figure 2.18, the designed inverter offers satisfactory performance for all three temperatures for 1 MHz frequency. Especially, the cryogenic operation shows its strength and settles less than 4ns even with the 10pF load thanks to the increased mobility as mentioned in the section 1.5.

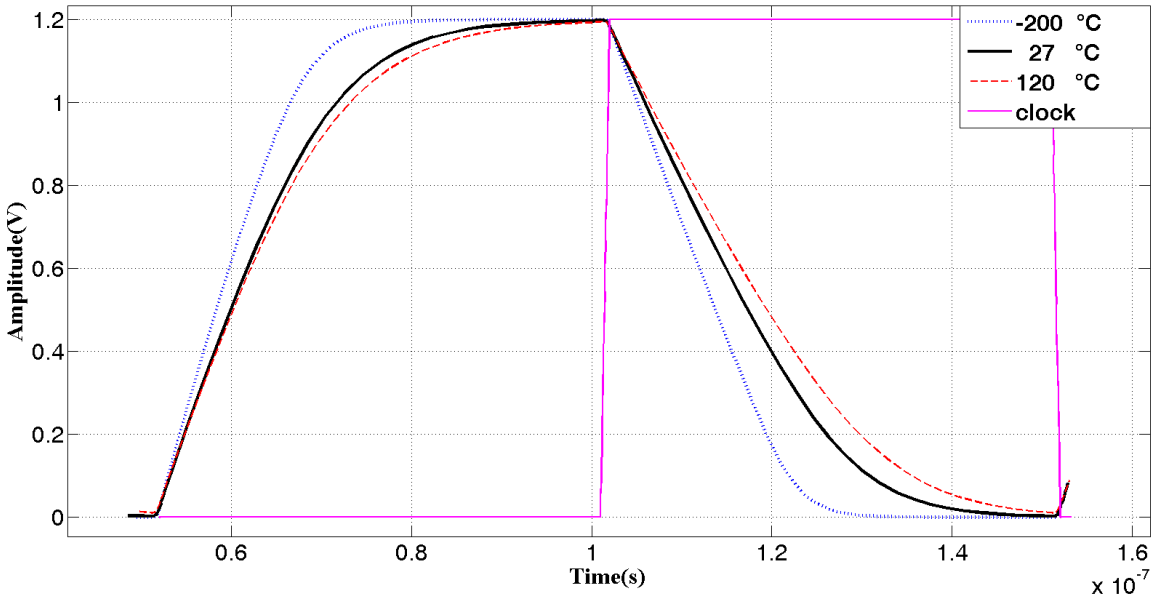

Figure 2.19 Inverter response for a 10 MHz input clock

After application of a higher frequency to the input of the inverter, it could be argued that the circuit fails to give satisfactory performance especially at 120°C. At room temperature, the inverter almost catches the input through the end of the transition. This is not problematic because the actual load of the inverter is the gate of NMOS switch which has only a few femto farads capacitance.

As indicated in the Section 2.1, 2.5u/100n and 1u/100n are the sizes of the transistors of the inverter. In order to operate the inverter faster at least for the hot condition, one can choose to use larger transistors via increasing W (since the L is already minimum channel length of the technology). This path hasn't been chosen due to the occurrence of glitches in the output of the overall circuitry which could be attributed to the phenomenon called charge injection. When the inputs of the switch changes, the output of the switch is injected an amount of charge and it appears as a large voltage or current glitch. Charge injection cancellation techniques could be used to operate the inverters faster without causing glitches in the output. Extra circuitry isn't used here and instead inverters are kept rather small.

Basic performance parameters of the designed inverter are given in Table 2.4.

Table 2.4 Performance metrics of the inverter for different temperatures

Temperature	**-200°C**	**27°C**	**120°C**
τ_r	15.5n	21.8n	24ns
τ_f	17.54n	25.44n	29.685n
τ_{pd} **(average)**	9.32n	11.8n	13.025n
Load	10pF//10MΩ	10pF//10MΩ	10pF//10MΩ

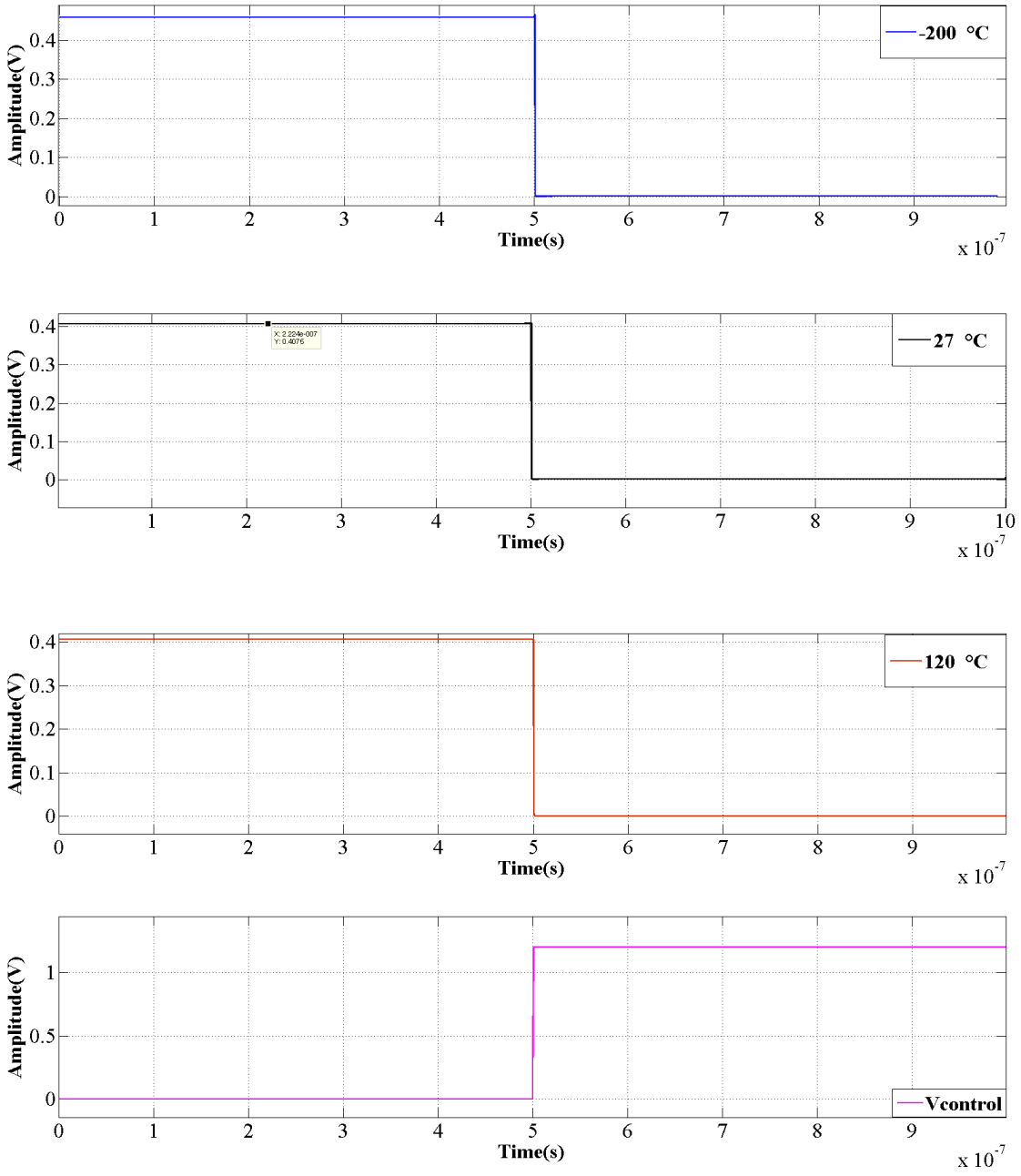

Figure 2.20 Switch transition for a 1 MHz input clock

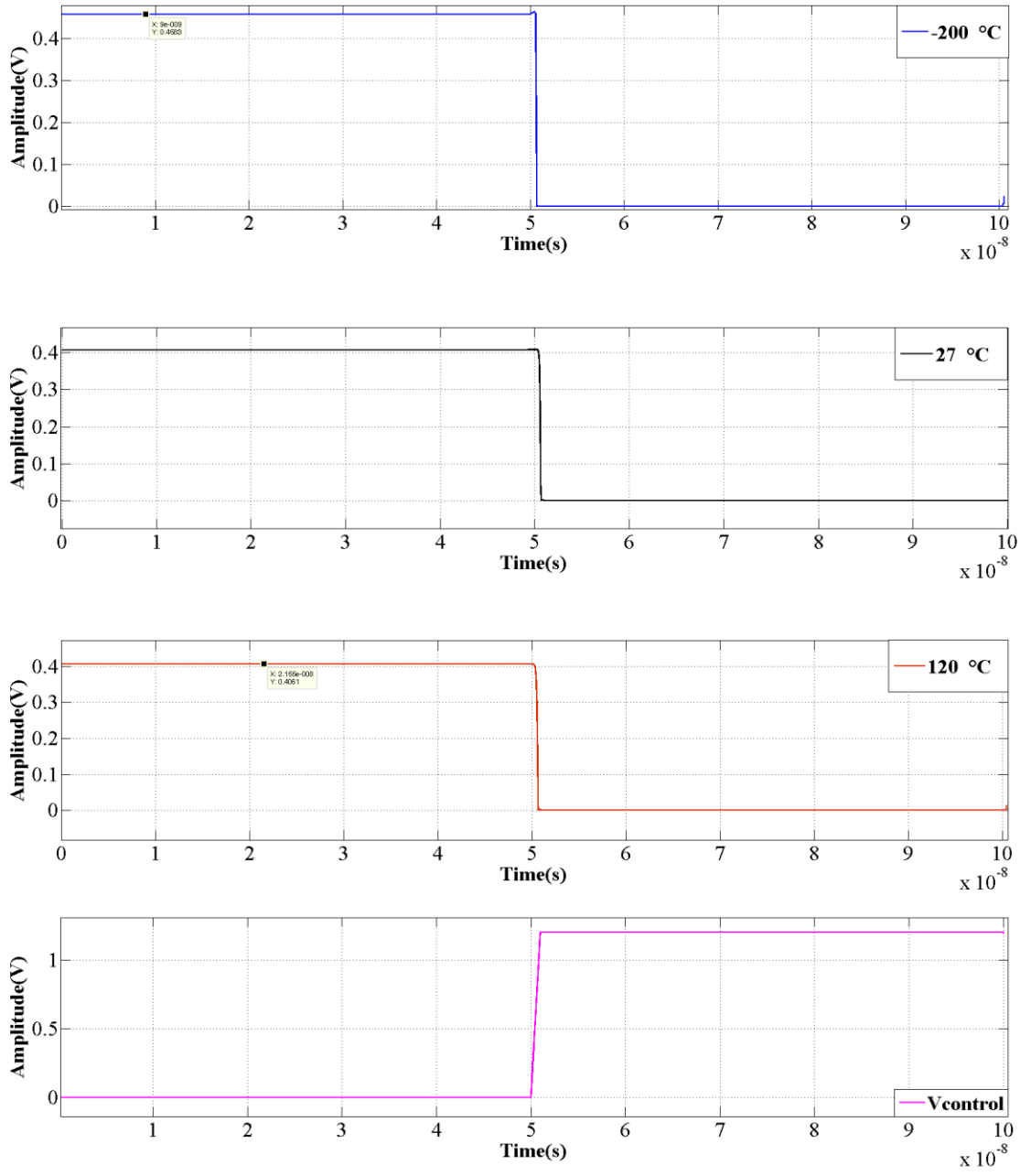

Figure 2.21 Switch transition for a 10 MHz input clock

As can be seen from the Figure 2.20-21, switches are capable of operating well at 10MHz for all three temperatures. One thing should be noted that the switching algorithm is in a reverse manner as previously stated. This is because of the inverting amplifier at the end of the complete circuitry and to make sure that the directions of both the digital word and the analog output are in the same direction.

2.5 Whole circuitry

Figure 2.22 depicts the overall setup for the simulation of the complete circuitry. As the output load, the equivalent of the oscilloscope probe is used. Reference voltage generators are not shown in the figure. In order to bias the positive input of the summing amplifier, another replica of the voltage reference circuit is used. The reason for using another replica is that a single voltage reference circuitry fails to drive the resistor string and the positive input node of the operational amplifier together.

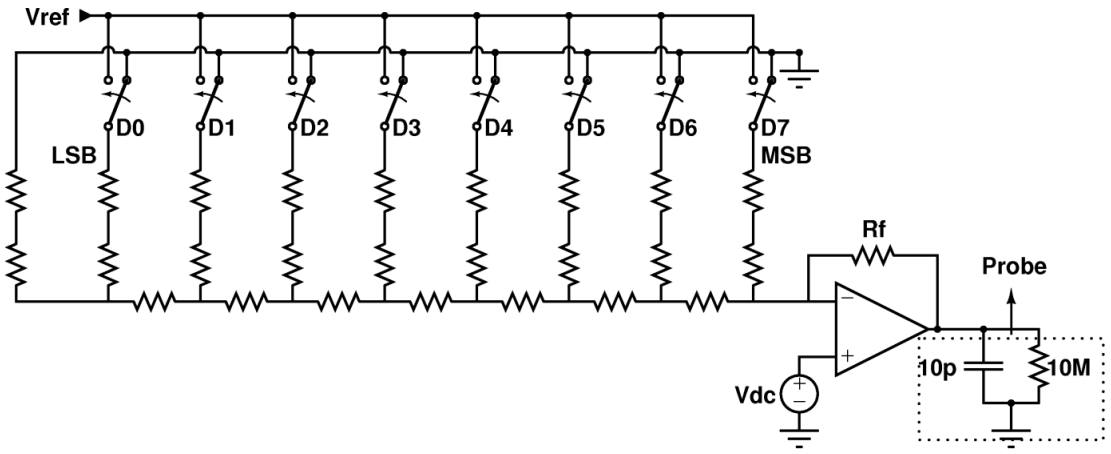

Figure 2.22 Schematic of the complete DAC

Figure 2.23 indicates the layout of the whole circuit. Top metal connection (metal 9) is not shown in the figure.

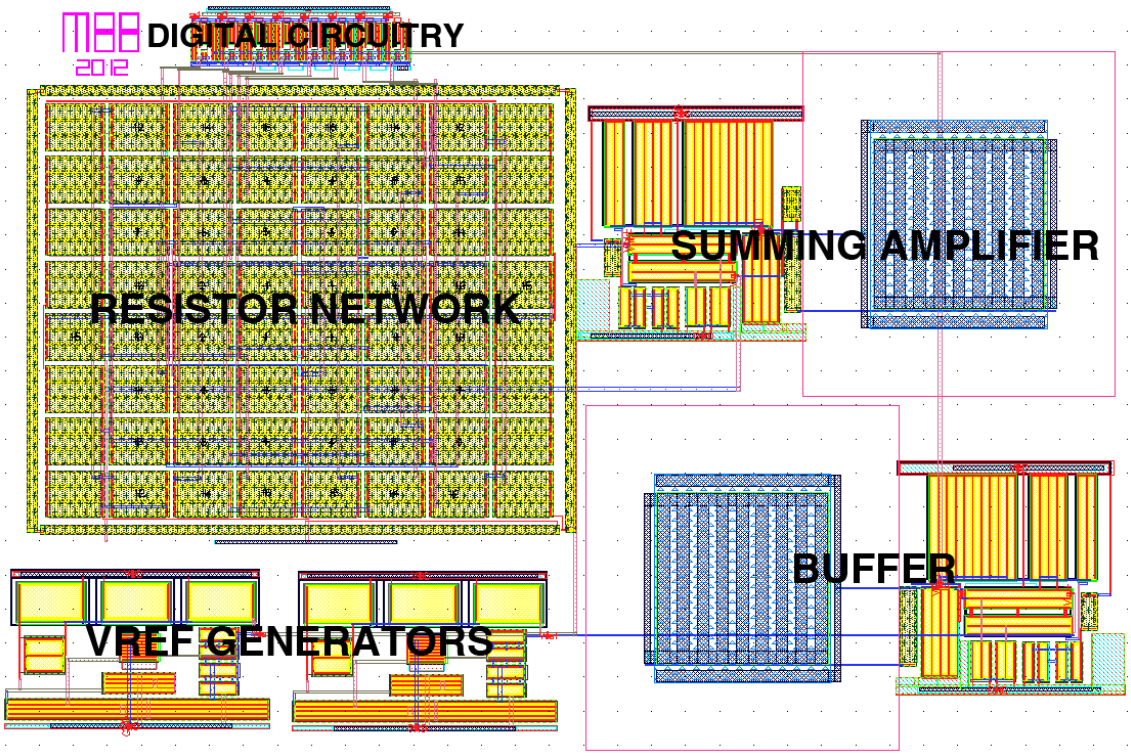

Figure 2.23 Layout of the complete DAC (100µm x 150µm)

2.5.1 Simulation Results

In this section, schematic and post-layout simulation results of the complete DAC circuitry are given. In order to simulate the circuitry, an increasing digital word from "00000000" to "11111111" is applied to the input of the 8-bit DAC and the analog output level of the circuit is observed. The realization of the digital word is obtained through the use of consecutive pulses from LSB to MSB. The sampling frequency is determined by the frequency of the LSB. In this manner, the x-axis of Figures 2.24-31 not only corresponds to the time but also every transition is stands for a new digital word acquired at the input of the DAC. This concludes that the time 0 represents the digital word "00000000" and the biggest time value at the axis represents the digital word "11111111". For instance, for 2MSps operation, every digital word transition happens at 500ns and since DAC is 8 bits and this corresponds to a 2^8=256 codes, 256*500ns=128µs which is when the last transition happens and "11111111" is converted to analog output.

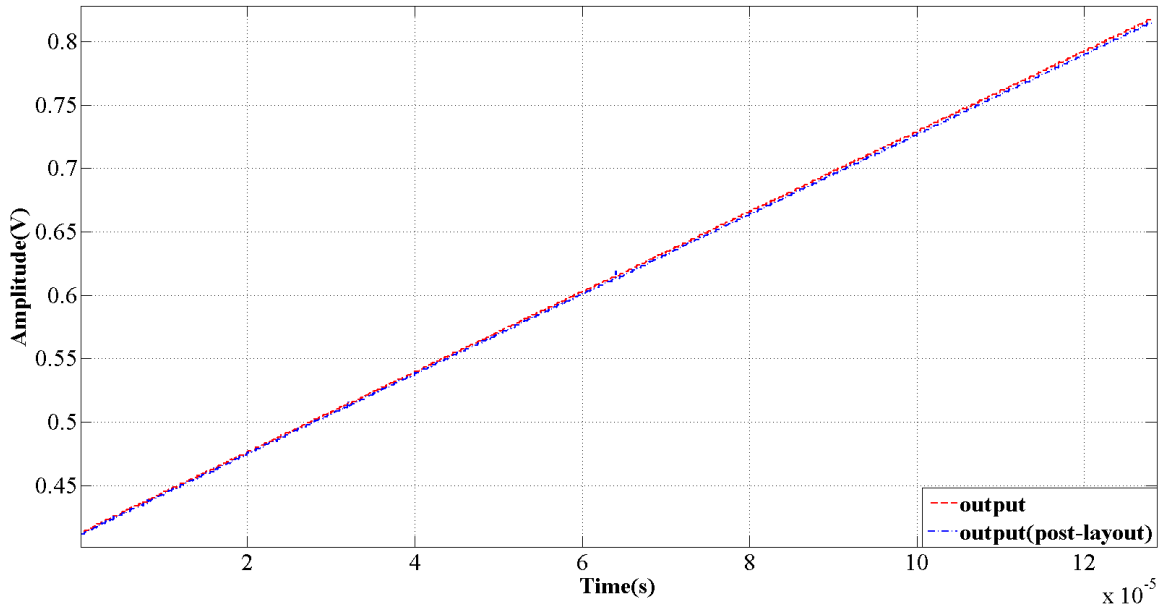

Figure 2.24 Analog output for an increasing 2MSps digital word sequence at 27°C

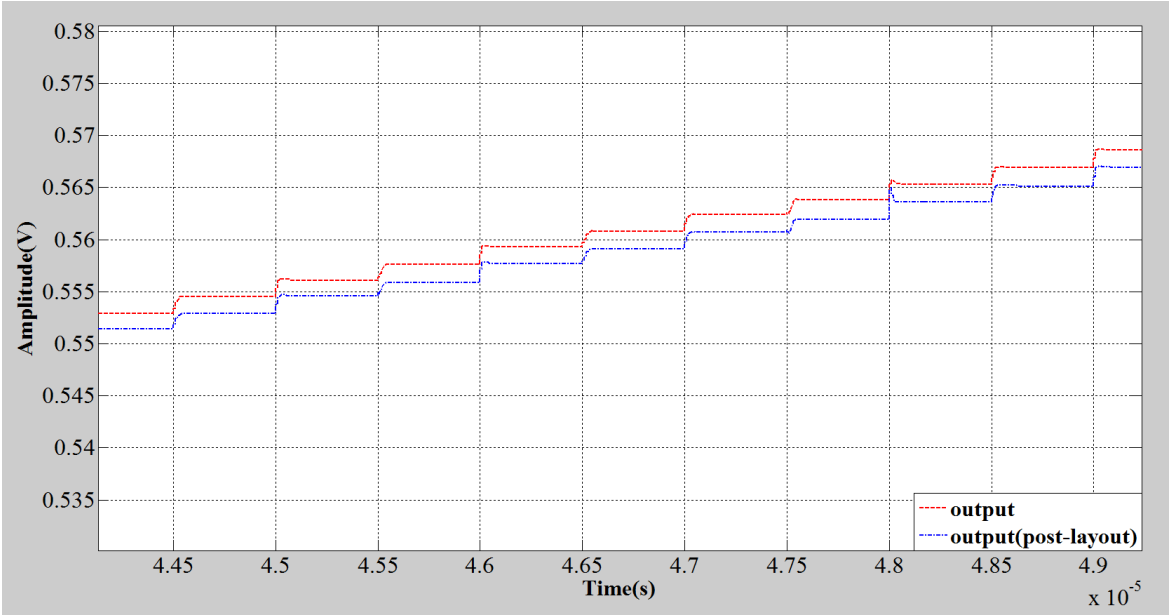

Figure 2.25 Analog output for an increasing 2MSps digital word sequence at 27°C, zoomed

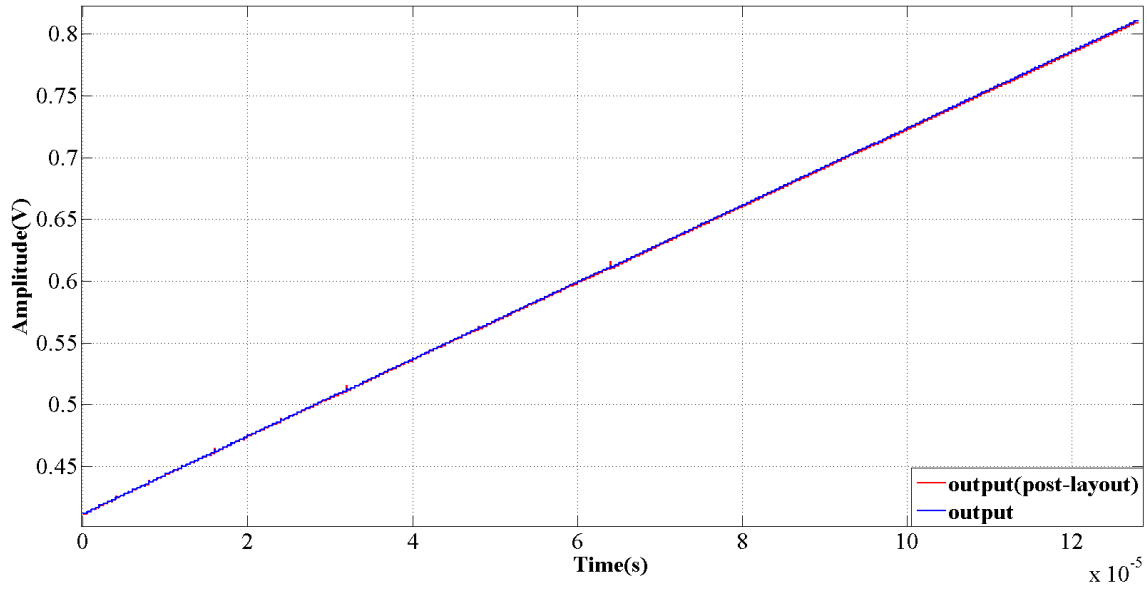

Figure 2.26 Analog output for an increasing 2MSps digital word sequence at 120°C

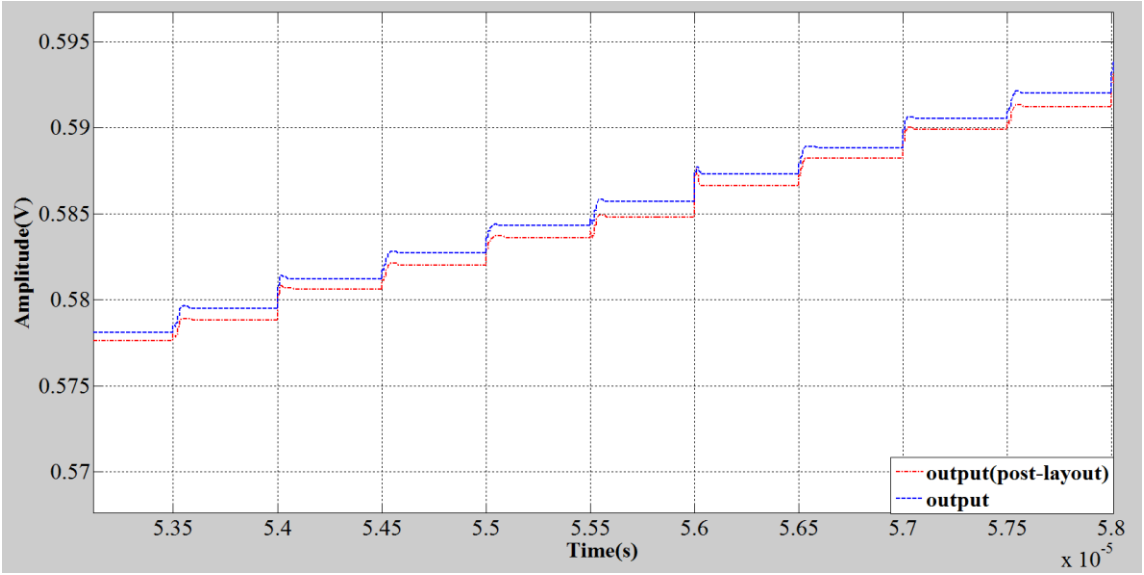

Figure 2.27 Analog output for an increasing 2MSps digital word sequence at 120°C, zoomed

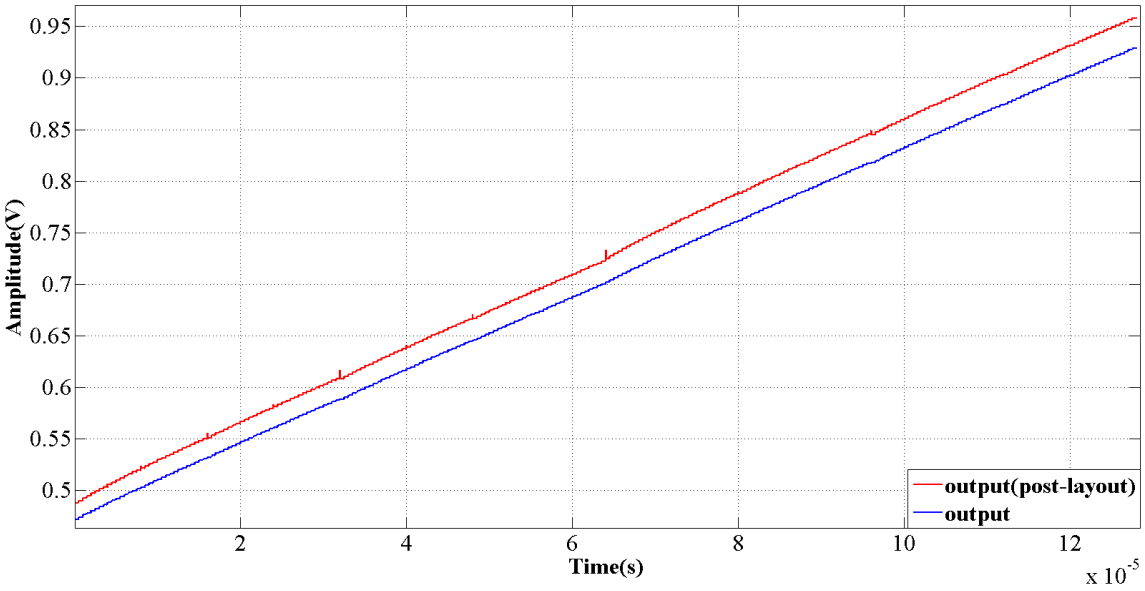

Figure 2.28 Analog output for an increasing 2MSps digital word sequence at -200°C

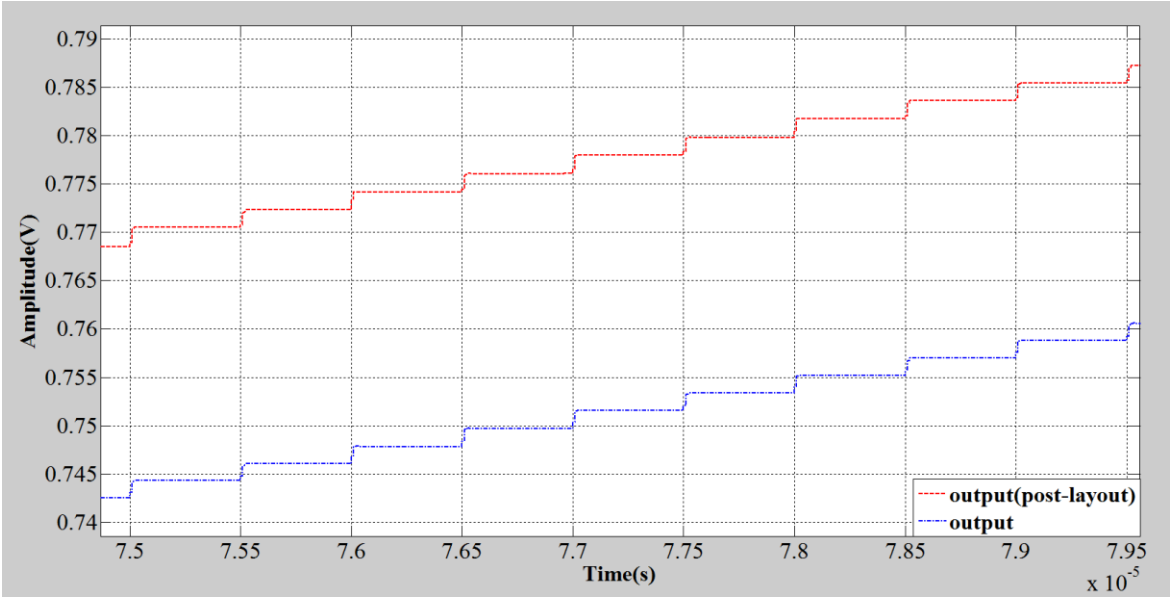

Figure 2.29 Analog output for an increasing 2MSps digital word sequence at -200°C, zoomed

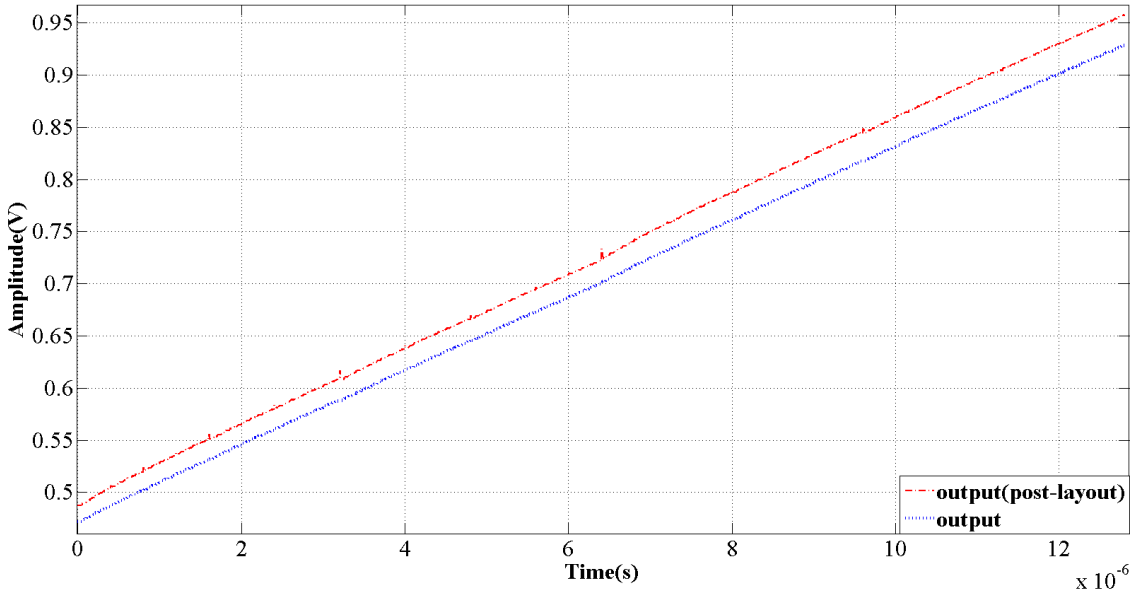

Figure 2.30 Analog output for an increasing 20MSps digital word sequence at -200˚C

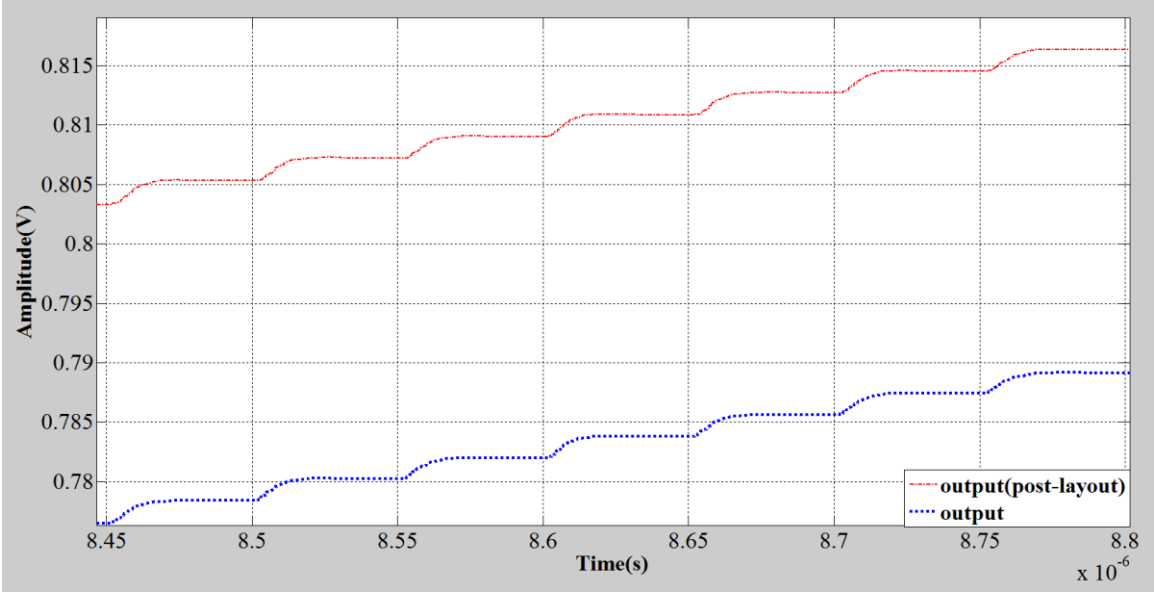

Figure 2.31 Analog output for an increasing 20MSpsdigital word sequence -200˚C, zoomed

In Figures 2.24-2.31, for three different temperature levels, DAC operation is presented via an increasing digital word versus analog output representation. Looking through the waveforms, one can conclude that the DAC indeed operates at the given frequency values in the graphs. 2 MSps operation however, seems to be the leading simulation compared to others for all temperature regions. This is interesting because neither digital circuitry nor operational amplifier is limited to 2MSps. The answer lies within the summing amplifier. Bandwidth of the summing amplifier is decreased in proportion to the effective resistance between inverting terminal and ground.

If the graphs are carefully examined, especially at cryogenic temperature (-200°C) and excessively hot situation (120°C) there are some glitches especially at post-layout simulations. These momentary spikes probably cause DNL errors and since INL is the integration of the DNLs, eventually lead to INL. It'll be shown in following figures.

For the calculation of DNL and INL, first their definitions should be examined. DNL is a measure of how different than 1 LSB a consecutive bit transition is. Meaning, it measures the actual transition when it should be exactly 1 LSB for each. INL on the other hand is basically the sum of whole DNL errors. This is a measure of being how far from the ideal transfer curve eventually. In order to calculate these parameters, the dataset of the graphs for a full scale is extracted. Next step is the creation of the ideal transfer curve where there is no offset or gain error and every transition is exactly 1 LSB. Considering the above definitions of DNL and INL, it must be noted that to find their actual values, possible gain errors and offsets should be eliminated at first. Since at the graphs there is a certain shift between the schematic and post-layout simulation results, this indicates that there is an offset at the amplifier stage. This could be eliminated from the dataset via normalizing the set to make it start from zero, by subtracting the first value from whole set. Next is to eliminate the possible gain error which is indeed present since the gain of the amplifier even falls below 50dB in hot environment. Elimination of gain error is explained in Appendix A.

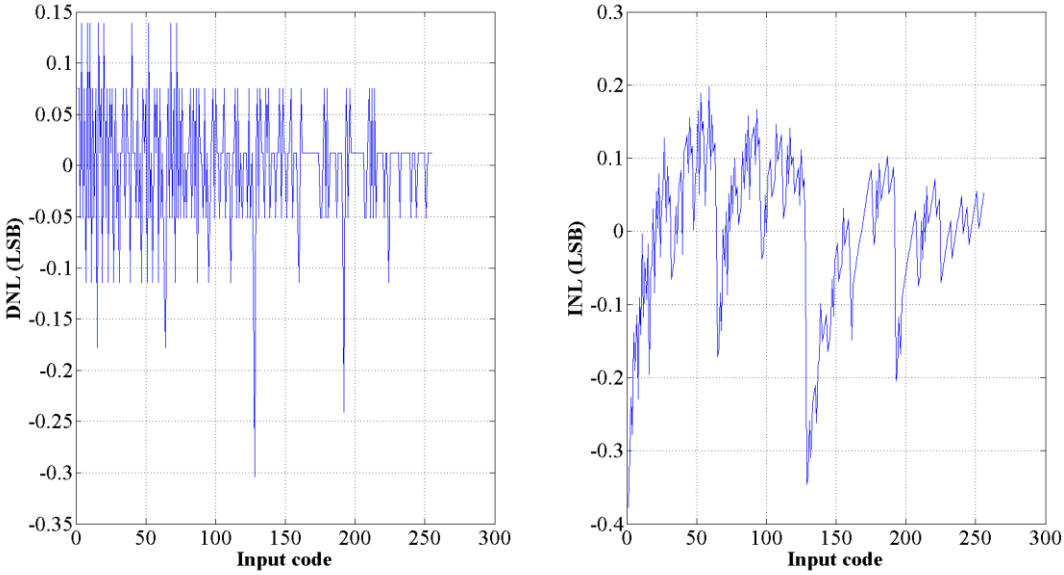

Figure 2.32 a. DNL b. INL of DAC at 27˚C

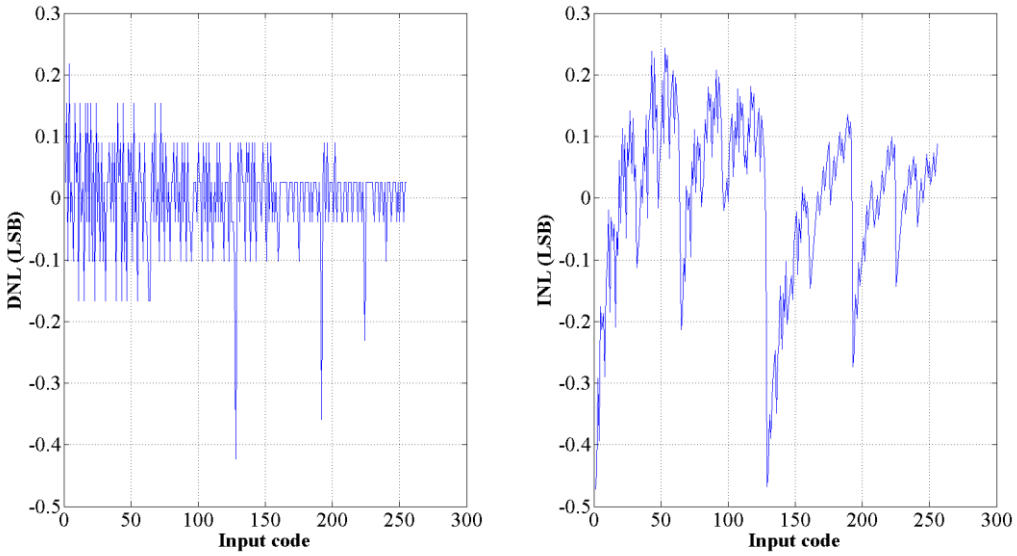

Figure 2.33 a. DNL b. INL of DAC at 120˚C

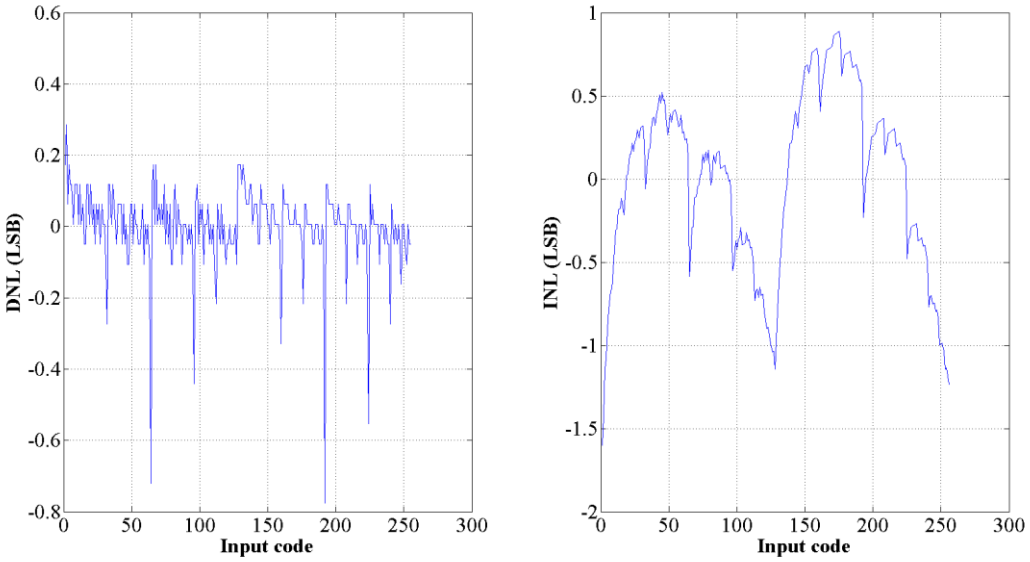

Figure 2.34 a. DNL b. INL of DAC at -200°C

Figures 2.32-34 indicates that the minimum DNL and INL is encountered at room temperature. This could have been predicted since there is no visible glitch at the room temperature waveforms compared to other two temperatures.

To prevent glitches, charge injection schemes could be used. Also, since this topology is fully binary and there is transitions like from “01111111” to “10000000” where there is the need for simultaneous switching to opposite directions, this makes it is prone to glitches. One solution could be the use of segmented structures which this project did not give attention as the circuitry is aimed to be kept as simple as possible. Segmented topologies use thermometer coded branches which guarantee monotonicity at the cost of complex digital circuitry and more number of components at the core as well.

Finally, DAC's performance is summarized in Table 2.5.

Table 2.5 Performance summary of the DAC

Parameter	**27°C**	**120°C**	**-200°C**
Maximum Frequency	8 MHz	2 MHz	20 MHz
Full-Scale output(V)	0.41-0.814	0.41-0.81	0.48-0.96
DNL/INL (LSBs)	±0.3/0.34	±0.42/0.46	±0.78/1.14
Power Dissipation	1.1mW	1.2mW	425µW
Power Supply	1.2V		
Technology	CMOS 90nm 1P9M		
Resolution	8		
Type	Full Binary R-2R		
Size	100µm x 150µm (pads excluded)		

In order to evaluate the performance of the designed digital-to-analog converter, Table 2.6 is generated below.

Table 2.6 Comparison of the DAC with [14]

Parameter	**Performance of DAC in [14]**	**Performance of designed DAC**
Technology	0.5µm SiGe BiCMOS	**90nm CMOS**
Temperature Range	-180°C ~ 120°C	**-200°C ~ 120°C**
Resolution	8	8
Type	Segmented R-2R	Full Binary R-2R
Maximal Sampling Frequency	10 MS/s	**20 MS/s**
Full-scale output	32µA	470mV-930mV
DNL/INL (LSB)	±0.22/0.3 at 27°C	±0.3/0.34 at 27°C
	±0.2/0.53 at 120°C	±0.42/0.46 at 120°C
	±0.6/0.85 at -180°C	**±0.35/0.49 at -180°C**
	N/A at -200°C	±0.78/1.14 at -200°C
Power Supply	3.3 V	**1.2 V**
Power dissipation	3 mW @ 10 MS/s	**425µW@ 20 MS/s**
Die Size	0.25 mm^2	**0.015 mm^2**

The DAC design is based on a voltage-mode operation where [14] is current-mode. In our design, it is shown that a much faster and lower power operation is achieved within a less than 10% area of [14]. It can be seen that linearity performances of the DAC at room temperature and 120°C are compatible with [14]. At -180°C, the

designed circuit has a better linearity than [14]. Since there is no data for -200°C at [14], it is not possible to do a comparison for that temperature.

It should be noted that a more fair comparison needs to be done after the fabrication of the designed circuit. Furthermore, an SFDR (spurious-free dynamic range) analysis should be done to compare the two designs. All in all, with this data at hand, it is fair to claim that a much lower power consuming, two times faster and compatibly accurate (at -180°C, even more accurate) and a much more compact (about 6% of area excluding pads) design is realized using a 90nm CMOS technology.

3 CONCLUSION

In this thesis, an R-2R based 8 bit DAC converter is designed with TSMC's 90nm CMOS 1P9M technology for use in a wide temperature range from cryogenic temperatures to excessive temperatures as high as 120°C. The DAC is to be used in an ongoing Digital Read-out Integrated Circuit (DROIC) project. The R-2R topology is simple and robust due to the fact that it uses less active elements and suits well for challenging environmental conditions, especially temperature and radiation. This project does not focus on radiation hardening rather on the ability to operate in a wide temperature range.

The designed DAC is a voltage-mode R-2R with R chosen as 10kΩ for an optimization of precision and area consumption. The D/A converter includes a digital part where the switching operation is realized, resistor string that realizes the very body of the circuit and responsible for the conversion, two identical temperature invariant voltage reference generator circuits and two operational amplifiers. One of the V_{REF} circuits is used along with the operational amplifier in buffer configuration to feed the resistor string and the other V_{REF} basically biases the second operational amplifier's positive input and thus defines the floor of the output voltage of the system. The latter operational amplifier is in a summing circuit configuration and is used for summing the fragments of the analog voltage from the corresponding bit and form the overall analog output voltage.

Since the matching of the resistors is vital for accuracy, in order to suppress possible gradients which could come during the fabrication process a common centroid-like layout technique is used during the laying out of the resistor string. Also, dummy resistors are used to create a similar environment for all resistors as well. Aspect ratio of the string is kept close to a square which is generally desired when laying out the integrated circuits.

Ultra wide temperature range of operation is obtained via a temperature compensated voltage reference generator circuit consisting of only MOSFETs. For accuracy, best performance is obtained at the room temperature where the fastest operation is possible at cryogenic temperatures at the expense of precision. It has a DNL and INL of ±0.3/0.34LSB only at room temperature, ±0.42/0.46LSB at 120°C and

±0.35/0.49LSB at -180°C. The DAC can operate up to 20MSps where the given specification is only 1MSps. The circuit dissipates only 0.43mW in full scale range at cryogenic temperatures where only 1.1mW at room and thus it suits for low power applications. It occupies a chip area of only 0.015mm^2.

The performance of the DAC at -200°C is still acceptable as far as the precision is concerned. The reason of glitches at the output which are causing increased INL and DNL values should be addressed carefully. One solution to the problem maybe the use of minimum size switches. This will reduce charge injection and also relax the damping coefficient of the DAC output. As stated in the previous chapter, segmentation may be used for elimination of glitches. This will however bring more digital circuitry (a binary to thermometer decoder) and extra units of elements to the core as well. While doing so, number of bits could be increased, too in order to reduce the quantization noise, improve the SNR of the circuitry and thus make it more accurate and precise.

Another improvement could be made at the operational amplifier side. Especially at extreme hot conditions, due to the reduced mobility, bandwidth, thus the speed is limited. Since the closed loop configuration basically lessens the bandwidth, thus speed of the device, precautions for bandwidth improvement could be made. The loss of bandwidth is proportional to the value of the feedback resistor. This could be lowered while Rs in the string kept the same. This in turn, causes a narrower full scale range as the input output relation of the topology, which is derived in section two, predicts. Also, transconductance of the amplifier could be increased via drawing more current from the device or using a wider input transistor pair, etc.

From -200°C to about -140°C, the reference voltage generator fails to perform as well as it does in the remaining part of the range. The reason for this was explained in the previous sections. Current source transistors are starting to turn off due to the increased threshold levels which is the result of the decreased temperature. This could be prevented through the realization of a lower V_{REF}, or drawing more current from the circuitry at higher temperatures. If large enough currents are used, the current sources will not operate in sub-threshold region and thus provide a more robust and fixed voltage through the cryogenic part of the temperature range. Again, this has a trade-off with power consumption and a challenging task to do because it may get more difficult

to keep the voltage constant through the rest of the range this time. Also, due to the career freeze out effect poor matching among similar devices occurs at cryogenic temperatures [31] and this could deteriorate the temperature compensation performance of the reference voltage circuit.

Finally, another improvement could be the use of self-compensated operational amplifiers like folded cascode topologies. This could save area and cost drastically as it can be observed that the MIM compensation capacitors are almost half the design. At this technology node however, it is more challenging to obtain reasonable gains which could be attributed to the channel length modulations, thus output resistances of the MOSFETs. This should be properly addressed if folded cascode structures are to be used.

To summarize, an ultra wide temperature range capable 8-bit DAC is designed with 90nm CMOS technology. To our knowledge, this circuit has the widest temperature range among published DAC materials. It occupies a very small area and is suitable for low power applications.

For future work, the design will be prepared for the tape-out after obtaining the output pads from the foundry. Output pads are likely to bring more capacitance to the output of the amplifier which in turn decreases the bandwidth. This should be carefully addressed. Also, a few pF should be added to the output during simulations to represent the parasitic capacitor which will come from the test board during the measurement of the chip.

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5 Appendix A

Best Fitting for INL

To eliminate gain error there are two approaches: End-point line and Best-fitting line. After choosing best-fitting method, an algorithm could be used in Matlab to determine the DNL and INL from the dataset (See the Appendix for the formula and the generated algorithm). Finally, for three temperatures, following DNL and INL values are extracted.

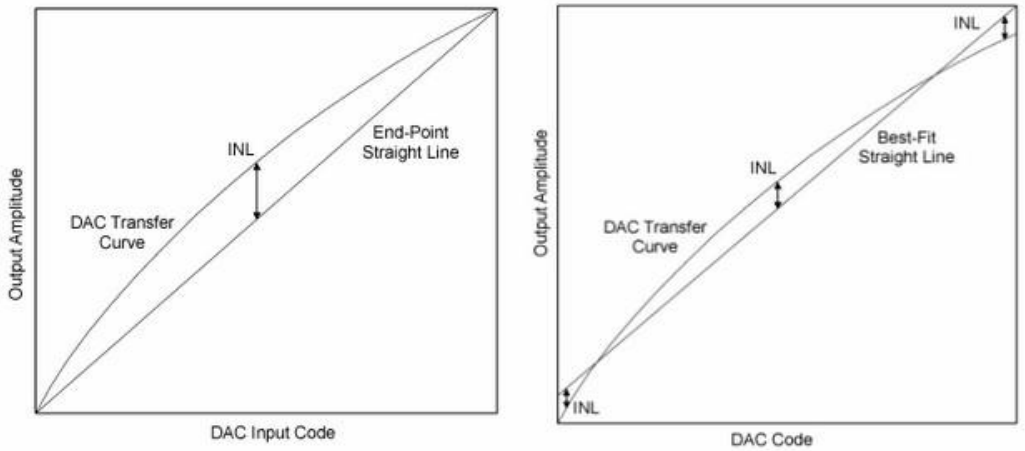

Figure 5.1 a. End-point line b. Best-fitting line for INL [30].

The best fitting line calculation uses all voltages. Also here, the least-squares linear regression algorithm is used. For the completeness, again the equation of the best fitting line [30] (y = ax + b):

$$Offset = b = \frac{\left(\sum (x \cdot y) \bullet \sum x\right) - \left(\sum x^2 \bullet \sum y\right)}{\sum x \bullet \sum x - \sum (x^2) \bullet N}$$

$$Slope = a = \frac{\sum y - (b \bullet N)}{\sum x}$$

Where:

a	= Slope
b	= Offset
N	= Number of data points
x	= x value
y	= y value

Below is the Matlab code for calculation of both INL and DNL according to the formula given above (for 10Mhz clocked, 20MSps output).

```
%% Matlab code for generating DNL and INL graphs

%% csv file import
importfile('10mhz_cryo.csv');
time = data(:,1);

%% offset cancellation
actual = data(:,2)-data(1,2);

%% centre point of each code
index = 25e-9 : 50e-9 : 12775e-9;
result = zeros(1,255);
for i=1:length(index)
   I = find((time <= index(i)+5e-9) & (time >= index(i)-5e-9));
   if (I > 0)
      result(i) = actual( I(1) );
   end
end

%% best-fit line (the least squares algorithm)
x = (1:1:256);
y = result;
b = ( sum(x.*y)*sum(x) - sum(x.*x)*sum(y) ) / ...
   ( sum(x)*sum(x) - sum(x.*x)*x(end) );
a = ( sum(y) - b*x(end) ) / sum(x);
line = a.*x + b;

%% dnl
dnl = zeros(1,255);
for i = 1:255
   vcx = result(i+1)-result(i);
   vs = line(i+1)-line(i);
   dnl(i) = (vcx / vs) - 1;
end

%% inl
inl = ( result - line );
inl = inl/a;

%% figure
figure(1)
subplot 121, plot(dnl)
subplot 122, plot(inl)
```