Investigation of Large-Signal Performance on BST Thin Film Varactors for Microwave Device Applications

Muhammad Farid Abdul Khalid

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Investigation of Large-Signal Performance on BST Thin Film Varactors for Microwave Device Applications

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Muhammad Farid Abdul Khalid
M.Sc.(Eng), B.Eng.(Hons)

School of Electrical and Computer Engineering
College of Science, Engineering and Health
RMIT University
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Declaration

I certify that except where due acknowledgement has been made, the work is that of the author alone; the work has not been submitted previously, in whole or in part, to qualify for any other academic award; the content of the thesis is the result of work which has been carried out since the official commencement date of the approved research program; and, any editorial work, paid or unpaid, carried out by a third party is acknowledged.

Muhammad Farid Abdul Khalid

March 2014

To my beloved mom and dad

Hindon Ismail and Abdul Khalid Ali

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List of Abbreviations

ADS   Advanced Design System

BST   Barium Strontium Titanate

CCVD   Combustion Chemical Vapour Deposition

C_{max} Peak Capacitance

CPW   Coplanar Waveguide

CSD   Chemical Solution Deposition

CST   Computer Simulation Technology

C-V   Capacitance-Voltage

CVD   Chemical Vapour Deposition

DC   Direct Current

DCS   Digital Communication System

DI   De-Ionised (Water)

DUT   Device Under Test

EM   Electromagnetic

GaAs   Gallium Arsenide

GSG   Ground-Signal-Ground

HF   Hydrofluoric Acid

HMDS	Hexamethyldisilazane
IDC	Interdigital/Interdigitated Capacitor
IM_3	Third-Order Intermodulation Distortion
IP_3	Third-Order Intercept Point
IPA	Isopropyl Alcohol
MEMS	Microelectromechanical Systems
MMIC	Monolithic Microwave Integrated Circuit
MMTC	Microelectronics and Materials Technology Centre
MOCVD	Metal-organic Chemical Vapour Deposition
PCS	Personal Communication System
PEC	Perfect Electric Conductor
PHC	Power Handling Capability
PLD	Pulse Laser Deposition
PVD	Physical Vapour Deposition
RF	Radio Frequency
RMMF	RMIT Microscopy and Microanalysis Facility
SEM	Scanning Electron Microscope
SMT	Surface-Mount Technology
SOG	Silicon-on-Glass
SoS	Silicon-on-Sapphire
UV	Ultraviolet
VNA	Vector Network Analyser
XPS	X-Ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction

Abstract

The development of future wireless communication and information systems is driven towards small-scaled and lighter-weight systems with the capability of being more adaptable and reconfigurable. The emergence of ferroelectric materials such as barium strontium titanate (BST) which has high dielectric tunability and low microwave loss at room temperature has sparked research interest in the last 20 years due to the developments in device electronics and material technology. One of the major areas where BST can play a significant role is in the RF and microwave systems.

BST thin film in paraelectric phase exhibits a nonlinear characteristic when an electric field is applied and the physical tuning of its dielectric permittivity is fundamental in realising an electronically tunable microwave component known as a variable capacitor or varactor.

The aim of this PhD research is to investigate the large-signal performance of BST thin film varactors fabricated on sapphire substrates for microwave device applications. Sapphire exhibits excellent microwave properties with very low loss at microwave frequencies, presents close lattice match to BST thin film and has a relatively low cost.

A novel method for the theoretical analysis of the third-order intermodulation distortion (IM$_3$) in BST thin film interdigital capacitors (IDCs) was established. BST thin films were initially grown directly on r-plane sapphire substrates, which have the potential to be

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integrated with existing semiconductor technologies through silicon-on-sapphire (SoS) process. Two circuit topologies - the "dual" and "series dual" BST varactor circuits - were proposed for linearity improvement and their theoretical models, along with simulated and measured results, were presented. Low IM_3 was demonstrated and experimentally verified. By proper selective biasing, very low nulls were observed in both dual and series dual BST varactor circuit topologies. This indicated minimum distortion.

An investigation of the power handling capability of BST thin film varactors fabricated on c-plane sapphire substrate was established. The research objective was to analyse the effects of varying the geometry of the BST IDC on the shape of the nonlinear *C-V* curves. Depending on the geometry selections, the *C-V* curves will become narrower or broader. The optimised narrow, broad and intermediate curves were demonstrated and their 1 dB compression points were extracted. The relationships between their tunabilities and 1 dB compression points were subsequently shown by simulations and measurements.

Chapter 1

Introduction

1.1 Motivation

Complex-oxide thin films are gaining ground in the development of future wireless communication and information systems. The emergence of ferroelectric materials, in particular barium strontium titanate (BST) which has unique microwave properties of large dielectric tunability and low microwave loss at room temperature, has sparked research interest for the past 20 years. One of the major areas where ferroelectric materials can play a significant role is in the RF and microwave systems which are increasingly broadband, leverage digital solutions, and demand extremely high linearity, seeking also to minimize size, weight, power and cost (SWAP-C) [1]. Examples of the current device technologies are smartphones, laptops, tablet computers, video game consoles and smart television, which all have access to the internet. The growing demand for higher broadband/bandwidth and

multiple channels requires the current and future wireless systems to be more adaptable and reconfigurable.

Ferroelectric materials are attractive to microwave and optical applications due to their physical properties that are sensitive towards external electric, magnetic and mechanical fields as well as to temperature. The physical properties include permittivity, permeability, polarization and refractive index [2]. BST thin film in paraelectric phase exhibits a nonlinear characteristic when an electric field is applied and the physical tuning of its dielectric permittivity is fundamental in realising an electronically tunable microwave component known as a variable capacitor or varactor. The two common parameters that are associated with the BST electric-field-dependent permittivity are tunability and lost tangent. The tunability, n is defined as the ratio of the dielectric permittivity at zero electric field bias to the permittivity under electric bias, E. The relative tunability, n_r is defined as the change of the permittivity between zero bias and bias in a field E with respect to the zero-bias value. Both equations are expressed below [3].

$$
\begin{aligned}
n &= \varepsilon^{'}(0)/\varepsilon^{'}(E), \\
n_r &= (\varepsilon^{'}(0) - \varepsilon^{'}(E))/\varepsilon^{'}(0)
\end{aligned}
\tag{1}
$$

The second most important parameter is the lost tangent, $tan\,\delta$ or quality factor, which is the ratio of the imaginary and real parts of the permittivity and given as follows.

$$
\begin{aligned}
\tan\partial(E) &= \varepsilon^{''}(E)/\varepsilon^{'}(E), \\
Q(E) &= 1/\tan\partial(E)
\end{aligned}
\tag{2}
$$

The BST thin film can be grown using different thin film deposition techniques. The two most common are sputtering [4-6] and pulse laser deposition (PLD) [7-9]. These techniques are widely available in most research laboratories. The choice of the host substrates is essential and lattice-matched single crystal substrates such as MgO, $SrTiO_3$ and sapphire

enable epitaxial growth of the BST film. They also exhibit low microwave loss at high frequencies which is attractive for the fabrication of high performance microwave devices.

The BST thin film varactors have a significant impact on the realisation of many adaptive, flexible and reconfigurable microwave devices such as electronically tunable filters for receiver preselection and transmit filtering [10, 11], phase shifters for electronically steerable satellite communication and radar systems [12, 13], matching networks in amplifiers [14] and a varactor shunt switch for wireless sensor applications [15]. A plethora of research studies have focused on enhancing the tunability and lowering the microwave losses of the varactors to be implemented in these microwave devices. Only a few research studies have emphasized the large-signal performance of nonlinear BST thin film varactors. In this case, two other important device parameters are considered: linearity and power handling capability. This PhD thesis is therefore driven towards these parameters and consequently contributing to the body of knowledge.

1.2 Objectives and Research Questions

The aim of this research is to investigate the large-signal performance of tunable barium strontium titanate (BST) thin film varactors fabricated on both c-plane and r-plane sapphire substrates for frequency agile microwave applications. Therefore, several objectives were set which include the following.

- Investigation and development of a novel method for the theoretical analysis of the third-order intermodulation distortion (IM_3) in nonlinear BST thin film varactors fabricated on r -plane sapphire substrates.
- Investigation and development of high dynamic range or highly linear BST thin film varactors fabricated on r-plane sapphire substrates.

- Material deposition and characterisation of BST thin films deposited on c-plane sapphire substrates.

- Fabrication and microwave characterisation of BST thin film varactors fabricated on c-plane sapphire substrates.

- Investigation and development of BST thin film varactors with high power handling capability fabricated on c-plane sapphire substrates.

In order to achieve these objectives, several research questions were outlined.

- What is the suitable theoretical model for analysing IM_3 in nonlinear BST thin film varactors? And how to develop it?

- What are the BST thin film varactor circuit topologies that could improve the IM_3 and achieve highly linear varactors? And how to develop them?

- What are the suitable methods for the material deposition and characterisation of BST thin film?

- What are the variations in the BST interdigital capacitor (IDC) geometry that could achieve high power handling capability? And how to develop them?

In this PhD thesis, the development of a novel method for the theoretical analysis of the IM_3 in BST thin film varactors fabricated on r-plane sapphire substrates was demonstrated. A polynomial equation related to the measured capacitance values of the BST thin film varactor was initially derived and converted into the general nonlinear capacitor equation. The coefficients extracted from this equation were subsequently substituted into the well-known IM_3 model for varactor diodes, where it was found to be ideal for the analysis of BST thin film varactors. The IM_3 model along with its mathematical expansions was slightly modified in order to implement two BST thin film varactor circuit topologies proposed for linearity

improvement. The details of this work can be viewed in Chapter 4. The development of BST thin film varactors with high power handling capability fabricated on c-plane sapphire substrates was also demonstrated. The effects of varying the physical IDC geometry on the shape of the nonlinear *C-V* curves were investigated. The optimised *C-V* curves were identified and the relationship between their tunabilities and 1 dB compression points were established. The details of this work can be viewed in Chapter 5.

1.3 Original Contributions

This PhD research has led to a number of significant findings which contribute to the body of knowledge in the field of BST thin films varactors for frequency agile microwave applications. The research findings can be summarised as follows.

- **A novel method for the theoretical analysis of IM$_3$ in BST thin film varactors fabricated on r-plane sapphire substrates was established.**

  The theoretical analysis of IM$_3$ in BST thin film varactors was demonstrated for the first time in single, dual and series dual varactor circuit topologies. The conversion from the polynomial equation, *C(Vsum)* to the general nonlinear capacitor equation *C(v)* was successfully solved. The original IM$_3$ theoretical model and its equation expansions were slightly modified by redefining IM$_3$ as average output power, P_{av} to match the simulated data. The exclusion of the inductance contributions for the mathematical expansions of this equation was also implemented.

- **Two BST varactor circuit topologies were proposed to improve IM$_3$ and subsequently highly linear varactors fabricated on r-plane substrates were established.**

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Both topologies were theoretically analysed, simulated and experimentally verified for the first time. The simplified topologies were successfully implemented with DC blocking capacitors for biasing purposes.

- **The relationship between the varactor's tunability and the 1 dB compression point was established.**

  The relationship between the tunability and the 1 dB compression point of BST thin film varactors was demonstrated for the first time. The modelling of the BST IDC geometry using commercial 3D software (CST) was successfully implemented. Parametric analysis was successfully demonstrated. The effects of changing the IDC geometry on the shape of the nonlinear *C-V* curves were analysed. Three distinct *C-V* curves were optimised and the 1 dB compression points were extracted.

- **BST thin film varactors with high 1 dB compression points fabricated on c-plane sapphire substrates were established.**

  The transformation of the *C-V* curves into the physical form of varactors was implemented. The narrow, broad and intermediate varactors were fabricated and the high 1 dB compression points achieved were comparable to the simulated results.

1.4 Author's Achievements

The significant findings in this research have successfully contributed to a number of publications.

1.4.1   Peer-Reviewed Journal Publications

- **M. F. Abdul Khalid**, E. A. Fardin, J. R. Scott, A. S. Holland and K. Ghorbani, "Low Third-Order Intermodulation Distortion in $Ba_{0.6}Sr_{0.4}TiO_3$ Interdigital Capacitors," *Progress in Electromagnetics Research C,* vol. 44, pp. 225-238, 2013.

- **M. F. Abdul Khalid**, K. Latham, A. S. Holland and K. Ghorbani, "BST Varactors with High 1 dB Compression Points Fabricated on Sapphire Substrates" (In Preparation).

1.4.2   Peer-Reviewed Conference Publications

- **M. F. Abdul Khalid**, A. S. Holland, J. R. Scott and K. Ghorbani, "Analysis of Third-Order Intermodulation Distortions in BST Varactors", *Proc. 2010 Asia-Pacific Microwave Conference (APMC 2010)*, 7 – 10 December 2010, Yokohama, Japan.

- **M. F. Abdul Khalid**, A. S. Holland and K. Ghorbani, "Barium Strontium Titanate Varactors with High 1 dB Compression Points", *Proc. 2012 European Microwave Conference (EuMC 2012)*, 29 October – 1 November 2012, Amsterdam, Netherlands.

1.5 Thesis Outline

This PhD thesis focuses on investigating the large-signal performance of BST thin film varactors fabricated on sapphire substrates. The main chapters of this thesis are outlined as follows.

Chapter 2 presents the literature review of BST thin film. This chapter begins with a brief introduction to BST thin film varactor and other competing microwave varactor technologies.

The overview of BST material properties and various thin film deposition techniques are discussed. Two types of BST varactor configurations - co-planar and parallel-plate varactors - are considered and their implementations in a diversity of agile microwave devices are outlined. Several research works relating to the intermodulation distortion and power handling capability of BST thin film varactors are reviewed.

Chapter 3 begins with the material deposition and characterisation of BST thin film fabricated on c-plane sapphire substrates. RF magnetron sputterer is utilised to deposit the films and different analytical techniques are employed to characterise the deposited films. The influence of post-annealing the BST thin films in vacuum oven and air is investigated. Fabrication of the BST thin film varactors using standard photolithography process and eventually gold electroplating for the electrodes are outlined. Microwave characterisations are performed on both unannealed and annealed varactors and the correlation between the microwave and material properties of the BST thin films are discussed.

Chapter 4 introduces a novel method for the theoretical analysis of IM_3 in BST thin film varactors fabricated on r-plane sapphire substrates. Two varactor circuit topologies are proposed for linearity improvement and their theoretical model, simulated and measured results are presented.

Chapter 5 describes the BST thin film varactors with high power handling capability fabricated on c-plane sapphire substrates. Parametric analysis was performed by varying the BST IDC geometry, leading to the optimisation of three C-V curves and the relationship between their tunabilities and 1 dB compression points are investigated.

Chapter 6 concludes the thesis and presents significant findings along with possible future work.

Chapter 2

Literature Review

2.1 Introduction

The potential applications of ferroelectric materials in microwave devices have been studied since the 1960s [16] but only in the last 20 years have intensive efforts been made due to the developments in device electronics and material technology [17]. The driving force behind this is the potential for miniaturization of microwave components and integration with microelectronic circuits due to the developments of thin and thick film ferroelectric technologies [17].

Barium Strontium Titanate (BST) continues to be one of the most studied ferroelectric materials due to its strong electric-field-dependent high permittivity and relatively low dielectric loss at microwave frequencies [3]. It exhibits a nonlinear response which can be controlled by applying an electric field. This tunable nonlinear response can be exploited by realising electronically variable capacitors which is also known as varactors. The high dielectric constant (for thin films > 100) is crucial for size reduction of device components.

The main advantages of BST thin film varactors in microwave applications include high tunability (at least 50 %), relatively low loss (Q-factor > 100 at 10 GHz), high tuning speed (<1 ns), low tuning voltage (< 30 V), extremely small leakage currents and high breakdown field [2, 3]. A comparison between BST thin film varactors and competing microwave varactor technologies such as GaAs and MEMS are shown in Table 2.1.

Table 2.1: Comparison of GaAs, MEMS and BST varactors [3].

	GaAs	MEMS	BST
Tunability (n)	~2–6 : 1[a]	~1.5–3 : 1[b]	~2–4 : 1
RF Loss (Q)	~20–50 at 10 GHz[a]	Very high	~20–100 at 10 GHz
Control voltage	<15 V[a]	<50 V[b]	<15 V (parallel plate type)
Tuning speed	~10^{-6} s	>10^{-5} s	~10^{-9} s[c]
Reliability	Good[a]	Poor	Good
Cost	High	High	Low
Power handling	Poor	Good	Good[c]

[a] Refer to http://www.mbelectronique.fr/
[b] Refer to Peroulis D *et al* 2003 *MTT-S Int. Microwave Symp. Digest* vol 2, pp 1117.
[c] Refer to Kozyrev *et al* 1998 *Integr. Ferroelectr.* **22** 329.

Semiconductor varactors such as GaAs and Si based are widely used in tunable microwave devices since they are easily integrated with monolithic microwave integrated circuits (MMICs). However, their Q-factor decreases drastically (Q ~ 1/f) at frequencies above 10 GHz and this region, known as a 'varactor gap', can be filled by the BST varactors where the Q-factor remains quite high. Other advantages of BST varactors over semiconductor varactors include higher tuning speed, power handling and lower cost. The key feature of MEMS varactors is their very high Q-factor compared to GaAs and BST varactors. However, they suffer from lower tuning speed, higher control voltage, higher cost and reliability issues affected by vibrations, temperature and moisture compared to the other two [3].

To date, BST thin film varactors have been employed in various tunable microwave devices such as filters, phase shifters, matching networks and switches [10, 12, 15, 18]. However, while most publications have addressed the issues of tunability and dielectric loss, only a few have discussed the intermodulation distortion that can occur within the BST thin film varactors [19, 20]. Intermodulation distortion can be a significant problem in nonlinear devices such as BST and semiconductor varactors as it causes distortion of the output signals and reduces the dynamic range. Whilst some unwanted frequency components can be easily removed by filtering, the third-order intermodulation products $2f_1 - f_2$ and $2f_2 - f_1$ occur very close to the fundamental signals and are therefore difficult to remove [21]. Power handling capability is another field that needs further investigation. Research about the behaviour of ferroelectric thin films under elevated microwave power is currently limited [22-25]. Tunable microwave devices such as BST thin film varactors have good power handling capabilities compared to GaAs varactors and this is promising for implementation in high power microwave systems [24].

In this chapter, an overview of the material properties of BST bulk ceramic and thin films is presented, followed by the most common BST thin film deposition techniques. The current research of BST thin films for agile microwave applications is then outlined. Next, a review of the intermodulation distortion issue along with the research techniques to analyse and improve the linearity of the BST thin film varactors are presented. A review of the limited research on the power handling capability of BST varactors is also discussed. Finally, based on these findings, prospects for further investigations are discussed.

2.2 BST Material Properties

BST is a type of complex metal oxide ferroelectrics with a perovskite structure similar to $BaTiO_3$ shown in Figure 2.1. Perovskites are characterised by a chemical formula, ABO_3 and have the same crystal structure with the oxygen located in the face centers. For BST, Ba and Sr atoms occupy the A positions while Ti atoms occupy the B positions. In the non-polar or paraelectric phase above the phase transition temperature as illustrated in Figure 2.1 (a), it has a cubic crystal structure with no spontaneous polarization that contributes to hysteresis. In this region, it has a high dielectric permittivity which can be tuned by an electric field and is also temperature and mechanical stress dependent. The tuning of the dielectric permittivity is used in tunable microwave components such as a tunable capacitor.

Figure 2.1 (b) shows the polar or ferroelectric phase below the phase transition temperature. Its crystal structure becomes non-cubic with the center atoms of negative and positive charges per unit cell slightly shifted to the top or bottom. This is called spontaneous polarization which defines the hysteresis loop. Under the influence of an electric field, the center atoms may be shifted from top to bottom or vice versa, thus changing the direction of the polarization vector. However, changing the direction of the electric field will shift the center atoms back to their original positions. This reversing mechanism is useful in building nonvolatile memory cells [26-28].
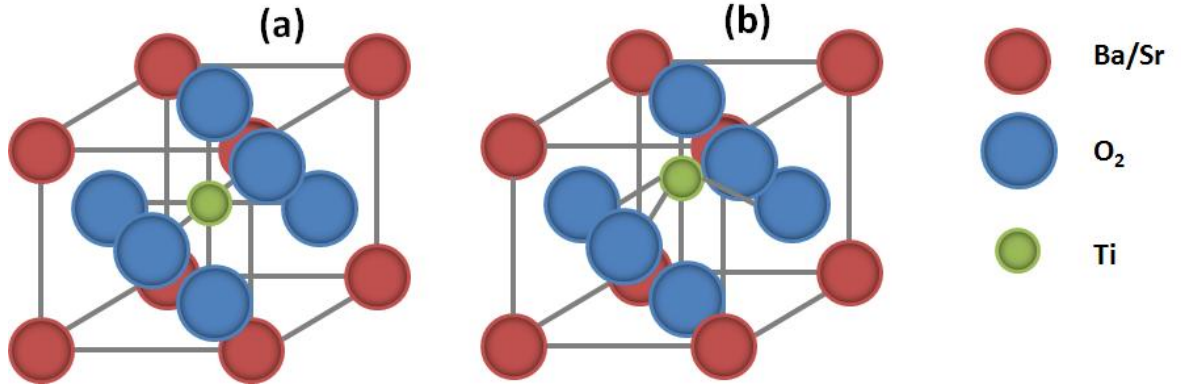
Figure 2.1: 3D unit cell of BaSrTiO$_3$ perovskites in (a) paraelectric and (b) ferroelectric phases.

Figure 2.2 shows the temperature-dependent dielectric constant of bulk ceramic Ba$_{0.7}$Sr$_{0.3}$TiO$_3$ in comparison with its thin film of the same composition [29]. The bulk ceramic has a sharp dielectric constant peak at the polar to non-polar phase transition near room temperature while the thin film has no peak and maintains its dielectric constant over a wide temperature range. BST bulk material has a very high dielectric constant compared to the thin film. The lower dielectric constant and tunability of the thin film are attributed to stresses, "dead" layers at the interfaces with the electrodes (of a tunable capacitor), non-stoichiometry, misfit strains, voids in the granular or columnar structures and also fundamental effects in relation to the surfaces or interfaces near the film [2].

The thickness of the "dead" layer is assumed to be of the order of several nanometers and its effect is prominent if it has comparable thickness to the thin film [30]. In [31], the pure bulk single crystal SrTiO$_3$ has no polar phase at any temperature. However, it is observed that at 155 K, polar phase transition occurred near the surface layer. This explains that the surface of the bulk crystals do not necessarily have the same properties as the bulk crystals themselves.
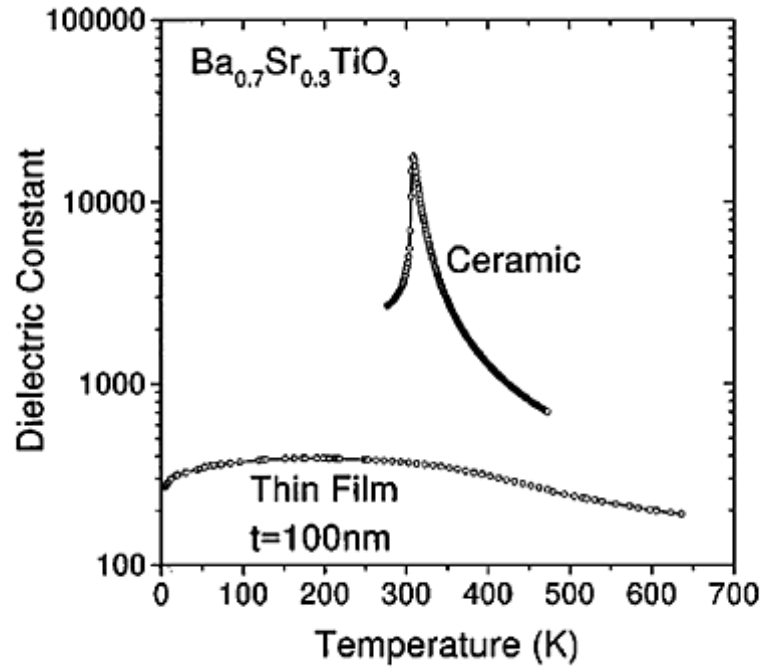
Figure 2.2: Variations of the dielectric constant of BST ceramic and thin film as a function of temperature [29].

In general, the tunable microwave devices of ferroelectrics, specifically BST should be in non-polar (paraelectric) phase. BST in polar (ferroelectric) phase is also piezoelectric and this transformation can lead to high dielectric losses at relatively low microwave frequencies of less than 10 GHz. Domain wall motion in piezoelectric causes mechanical damping that can also contribute to the dielectric losses. Another factor not to pursue microwave applications in the polar phase mode is due to the hysteresis behaviour. However, some microwave devices in polar phase have been demonstrated. Reasonable tunability and high Q-factor of 13% and 15 to 80 respectively at 40 GHz were achieved in the $Na_{0.5}K_{0.5}NbO_3$ /SiO_2/Si structure [32]. An interesting finding from this research was the low dielectric losses achieved above 20 GHz. This is in contrast with BST and other semiconductor varactors where the Q-factor deteriorates with increased frequency.

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Microwave losses in the paraelectric phase of ferroelectrics including BST are separated into intrinsic and extrinsic losses as shown in Figure 2.3 [2]. In a perfect crystal, intrinsic losses occur due to the interaction between phonons and microwave energy. The free charge carriers also absorb the microwave energy but their contribution is too small and can be ignored. The microwave energy is absorbed by thermal phonons and heats up the crystal and the absorption process takes three- and four - quantum mechanisms. Three-quantum and four-quantum mechanisms involve the interaction of microwave energy with two and three phonons respectively. However, in the paraelectric phase, the three-quantum mechanism becomes dominant. Apart from the fundamental losses, induced DC field on ferroelectrics can also contribute to intrinsic losses. When a DC field is applied, the centre ions of the cubic crystal structure are shifted and the microwave energy experiences similar losses to that of a non-cubic crystal structure. The induced DC field introduces a Quasi-Debye mechanism and microwave to acoustic transformation losses. These intrinsic losses are unavoidable and represent the minimum value of the whole microwave losses or loss tangent of the ferroelectrics.

In real crystals with defects, the extrinsic losses associated with these defects are much higher than the intrinsic losses. However, these losses can be decreased by reducing the density of the defects. The most common extrinsic loss that occurs in all dielectrics is the Universal (Curie-von-Schweidler) relaxation mechanism. On the other hand, charged defects create a local static electric field and within this field, the microwave waves generate acoustic waves which cause microwave losses in the crystal. The loss tangent in this case is proportional to the permittivity which indicates that it is also temperature and electric field dependent. These charged defects can be found at the interfaces of grains and electrodes or uniformly distributed in the crystal. Oxygen vacancies are known to be the main charged defects. Other forms of extrinsic losses are due to the local polar regions that usually occur at the interfaces between the grains, electrodes, dielectric and metallic layers.

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It is worth noting that a crucial distinction between intrinsic and extrinsic losses in relation to the loss tangent dependence on the electric field is that the intrinsic and extrinsic losses become stronger and weaker respectively under the influence of an electric field. More details of these losses in the paraelectric phase can be found in these references [2, 33].
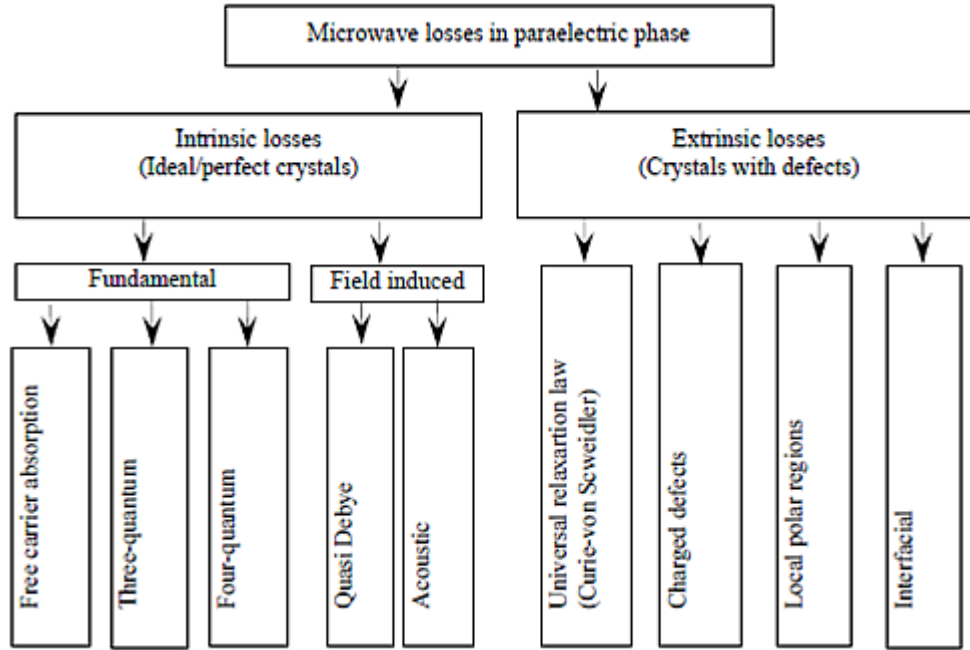
Figure 2.3: Microwave losses in paraelectric phase of ferroelectrics [2].

Strain can have significant effects on the properties of ferroelectric thin films compared to their bulk counterparts. In [34], polar (ferroelectric) behaviour is observed at room temperature in $SrTiO_3$ thin films epitaxially grown on a closely matched $DyScO_3$ substrate. As mentioned earlier, bulk $SrTiO_3$ has no polar phase at any temperature but in this case, strain can actually shift its Curie temperature.

Strain is also caused by misfit strain due to the lattice and thermal expansion coefficients mismatch between the thin film and substrate. A phenomenological thermodynamic theory using a thermodynamic potential approach is developed for $BaTiO_3$ and $PbTiO_3$ thin films epitaxially grown on different cubic substrates [35]. It is shown that the misfit strain between

these films and substrates not only shifts the Curie temperatures but can also change the phase diagrams significantly. In [36, 37], based on the Landau-Devonshire phenomenological model, the phase diagrams for BST thin films on cubic substrates are developed and the relations between misfit strain, film thickness and tunability are demonstrated. It is shown that by proper selection of substrate and film thickness, a high tunability can be achieved.

2.3 BST Thin Film Deposition

There are two methods for BST thin film deposition; the chemical deposition and physical deposition methods. The chemical depositon method includes the chemical solution deposition (CSD) and chemical vapour deposition (CVD): both employ chemical precursors which experience chemical reactions for the production of BST thin films [2]. There is quite a lot of research depositing BST thin films using sol-gel technique [38-51] and metal-organic CVD (MOCVD) [10, 22, 26, 52-56], where both are part of the CSD and CVD families respectively.

The sol-gel technique has the advantages of low-cost, effectiveness and large-area deposition capability [3]. It involves preparation of a suitable solution from precursors according to the designated BST composition and chemical route. BST thin film is then realised by spin-coating the solution on a substrate, in which the wet film will experience condensation, drying and hydrolysis relating to the chemical route [2]. The thin film is subsequently annealed to achieve crystallinity.

The MOCVD system is suitable for the synthesis of multilayer thin films on selective substrates [3]. It involves three pressure-regulated, temperature-controlled liquid-source bubblers containing metalorganic precursors of Ba, Sr and Ti. They are then mixed and

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flowed into the cold-wall quartz reactor containing the substrate; thin film will then be deposited onto the substrate which is located on the resistively heated inconel susceptor [2].

Combustion CVD (CCVD) technique is another deposition method initially developed by a research group from Georgia Institute of Technology. Intensive research based on this technology has progressed in recent years [12, 20, 57-66]. This technique has the advantage of utilising a wide variety of deposited materials and substrates. The deposition of thin film on substrate is done in an open atmosphere with no vacuum chamber needed. Precursors are dissolved in a solution (combustible fuel) and the solution is atomised to form microscopic droplets. These droplets are carried by an oxygen stream to the flame where they are combusted. The flame is moved above the surface of the substrate to be coated and the heat from the flame provides energy which vaporises the droplets, the precursors react and deposit on the substrate.

The physical deposition method includes physical vapour deposition (PVD). The deposition of thin film on substrate usually follows these common steps:

a) The deposited material is converted into vapour by physical means;

b) The vapour is carried from the target source to the substrate across a low pressure area, and

c) Condensation (deposition) of vapour on the substrate produces the thin film.

There is a vast amount of literature on the synthesis of BST thin films using sputtering [4-6, 67-91] and pulse laser deposition (PLD) [7-9, 92-118] as these two are the most common techniques of PVD. Table 2.2 below summarises the advantages and limitations of the BST thin film deposition techniques.

Table 2.2: Comparison of different methods for the synthesis of BST thin film [119].

GROWTH METHOD	ADVANTAGES	LIMITATIONS
SOLUTION		
Sol-Gel and Chemical Deposition	• Inexpensive • Rapid turnaround and sampling	• Phase control • Composition control • Morphology • Reproducibility • Scalability
ENERGETIC		
Sputtering	• Uniformity • Scalability • Low thermal budget	• Point defect concentrations • Limited compositional control • High residual stress • Poor conformality
Pulse Laser Deposition (PLD)	• Rapid sampling • Quickly produce new materials	• Morphology (bouldering) • Point defect concentrations • Scalability • Uniformity • High residual stress

VAPOUR		
Metal Organic Chemical Vapour Deposition (MOCVD)	• Uniformity • Morphology • Composition control • Low thermal budget • Scalability • High conformality	• Expensive • Precursor availability • Precursor stability • *Still a relatively immature technology*

2.4 BST Thin Film Varactors for Agile Microwave Applications

BST thin film varactors are commonly fabricated in parallel-plate and co-planar plate varactor configurations. The parallel-plate varactor configuration has a structure in which the BST thin film is sandwiched between the top and bottom metal electrodes. On the other hand, the co-planar plate configuration has metal electrodes patterned directly on top of the BST thin film and it is easier to fabricate and integrate it into circuits compared to the parallel-plate varactors. Further, it allows epitaxial growth of BST thin films directly on close-matched crystalline substrates. Agile microwave devices such as filters, phase shifters, switches and matching networks usually employ varactors as their tuning circuit elements.

2.4.1 Co-planar plate BST Thin Film Varactor Configuration

Figure 2.4 shows the general fabrication process of a co-planar plate varactor. The first step is the growth of BST films, whether epitaxially or on a deposited buffer layer substrates as

shown in Figure 2.4 (A). The next step is the metal deposition and finally the patterning of the electrodes, either by lift-off or wet/dry etching processes (Figure 2.4 (B) and (C)).

For the route of the lift-off process, the electrodes are initially patterned through a basic photolithography process. This involves spin coating a thin photoresist on top of the BST/substrate or BST/buffer layer/substrate followed by UV light exposure through a chrome mask and, finally, soaking it in a suitable developer which creates the openings for metal deposition. The suitable deposition of the metal layers is by electron beam evaporation which allows a very thin layer to be deposited. The sample is then immersed in an ultrasonic bath filled with acetone and the agitation will assist in washing away the photoresist together with the metal layers on top of it and eventually the patterning of the electrodes. Prior to this, the formation of undercuts of the photoresist as in Figure 2.4 (B) is important to separate the deposited metal layers on the BST/substrate and the metal layers on the photoresist. A suitable photoresist is therefore required to create these undercuts such as AZ5214E or soaking the already exposed AZ1512 photoresist sample in a chlorobenzene solution before developing the pattern.

In the case of wet/dry etching alternatives, the metal layers are evaporated on top of the BST/substrate before patterning the electrodes using suitable etchants. However, this method is quite risky as it could potentially damage the BST layer and produce an underetch pattern.
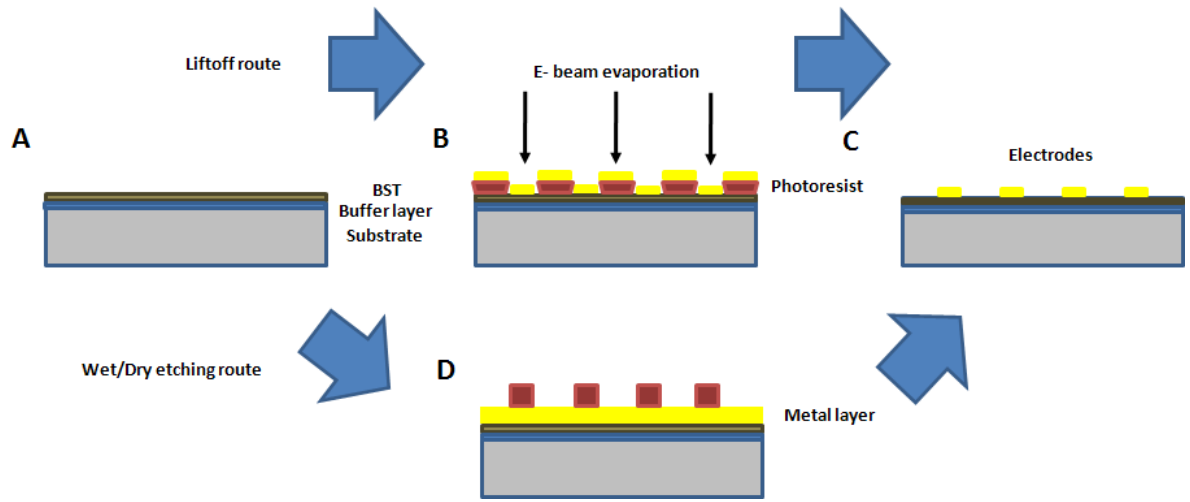
Figure 2.4: The general fabrication process of the co-planar plate varactor.

2.4.2 Parallel-plate BST Thin Film Varactor Configuration

The high tunability at low tuning voltages is an attractive trait for the parallel-plate capacitor compared to the co-planar capacitor. However, this comes at a cost due to the complexity of its fabrication process. One of the methods of the fabrication proposed in [120, 121] is depicted in Figure 2.5. By using the crossover dielectrics in the process, it helps to lower the breakdown voltages. Premature breakdown is caused by the higher EM fields at the edges of the bottom electrode when high bias voltages or large RF signals are applied [2]. The bottom electrode in Figure 2.5 (A) was initially deposited with refractory metals such as Pt and/or Au which can tolerate the high temperature deposition of the BST thin film layer on top of it (Figure 2.5 (B)). E-beam evaporation and RF magnetron sputtering were used for the deposition of the Ti/Au/Pt bottom electrode and the 300 nm BST thin film respectively. The Pt/Au top electrode was deposited and patterned by lift-off process and the BST thin film was etched down to the bottom electrode using buffered hydrofluoric acid (HF) to facilitate ohmic contacts (Figure (C) and (D)). A 300 nm SiO_2 in Figure (E) was used as a dielectric crossover to isolate the top contact from the edges of the bottom electrode (which was the main cause of the premature breakdown) and encapsulated the BST thin film from exposure to subsequent

contamination in processing or operation. The final step was to deposit a thick interconnect stack Ti/Au by e-beam evaporation and patterning by lift-off (Figure (F)). Nevertheless, this method may still suffer from the premature breakdown due to the vertical side walls in the bottom electrode. An alternative way to increase the breakdown voltage is for the bottom electrode to have sloped sidewalls which allows conformal coverage of the slope by subsequently deposited layers [2].
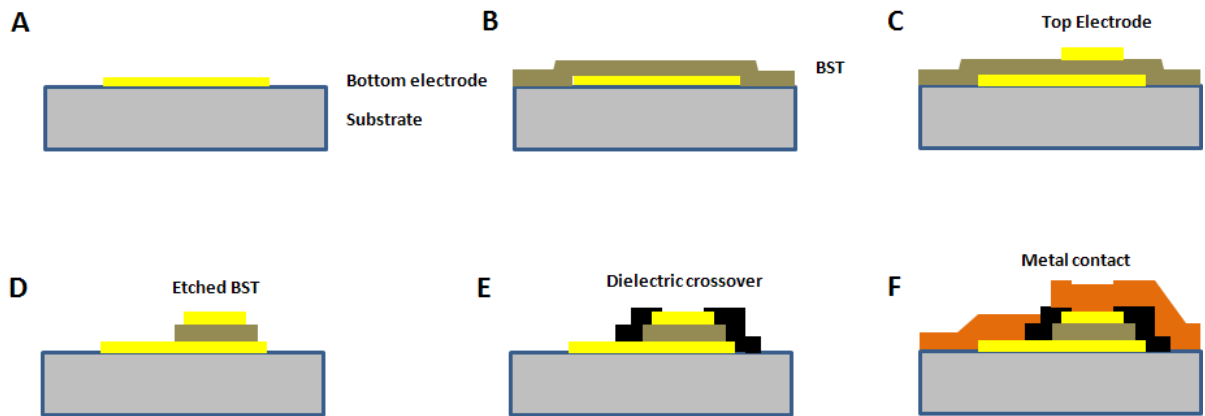
Figure 2.5: The fabrication process of the parallel-plate BST varactor with crossover dielectrics [120, 121].

2.4.3 Agile Microwave Devices

There is a great deal of literature on the applications of co-planar and parallel-plate BST thin film varactors in agile microwave devices. These potential devices include tunable filters, phase shifters, switches and matching networks. In this section, several potential devices based on BST thin film varactors are discussed.

Tunable BST thin film lowpass and bandpass filters were developed by a North Carolina State University group. This filter used a parallel-plate capacitor as the tuning element which was fabricated on Si wafer coated with SiO_2 followed by alternate layers of IrO_2 and Pt. The MOCVD technique was used to deposit the 300 nm thick BST films. The filters operated at

low frequencies, between 100 and 300 MHz and low third-order intercept point (IP$_3$) of 19 dBm was achieved in the bandpass filter [10]. However, the tuning range is small, from 0 to 9 V. An electronically tunable third-order combline bandpass filter was also achieved by the same group [11]. A 600 nm thick BST thin film was grown on c-plane sapphire by the RF magnetron sputtering technique and an interdigitated capacitor (IDC) was built. Three such capacitors were placed at the ends of the microstrip line resonators to tune the centre frequency of the bandpass filter. Figure 2.6 shows the bandpass filter which operated from 2.44 to 2.88 GHz with an applied voltage of 0 to 200 V and a high IP$_3$ of 41 dBm was achieved. The maximum insertion loss was 5.1 dB at zero bias while exceeding 13 dB return loss over the bias range.

Other combline bandpass filters operating at X-band and Ku-band were also reported [122]. The synthesis of compositionally graded BST thin film on alumina substrate was realised using CSD technique and then annealed. IDCs were then fabricated and integrated with the filters. Figure 2.7 shows the X- and Ku-band filters operated from 8.75 to 10.96 GHz and from 11.7 to 14.3 GHz within a tuning range of 0 to 100 V and maximum of 8 dB and 10 dB insertion losses respectively.

Several other BST-based tunable filters have also been developed. These include tunable dual-mode bandpass filter and tunable slotted ground structured bandstop filter [123, 124], X-band back-to-back tunable resonator filters on flexible liquid crystal polymer substrates and X-band tunable quasi-elliptic bandpass filter [63, 65], and Ka- and U-band tunable bandpass filters [66].

Tunable phase-shifters operating at 20 and 30 GHz were developed by nGimat Company in collaboration with the Georgia Institute of Technology [12]. A phase shifter is an important device in electronically-scanned phase array antennas. The IDCs as well as a low voltage gap capacitor [20] were fabricated on BST thin films on r-plane sapphire substrates, in which the 300 nm films were deposited using the CCVD process. For the 20 GHz phase shifter shown in

Figure 2.8, the maximum phase shift achieved was 330º at 21.7 GHz. The insertion and return losses varied from 6.1 to 3.9 dB and from 15.2 to 4.7 dB respectively. The maximum phase shift for the 30 GHz phase shifter was 360º at 32 GHz, with the insertion and return losses varying from 7.0 to 4.3 dB and from 29 to 4.8 dB respectively. The former had a figure of merit of 54º/dB and the latter, 51º/dB. This group had also achieved low-voltage flip-chip mounted BST phase shifters operating at L- and C- bands from previous research work [125].
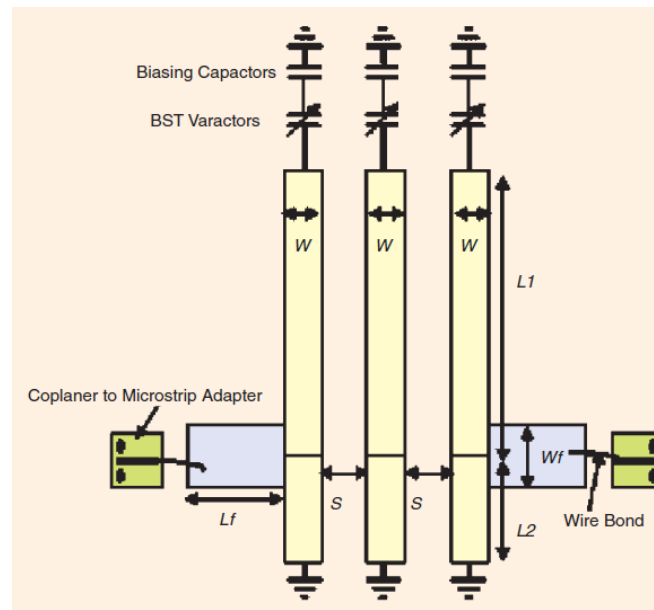
Figure 2.6: Schematic of the tunable third-order combline bandpass filter [11].
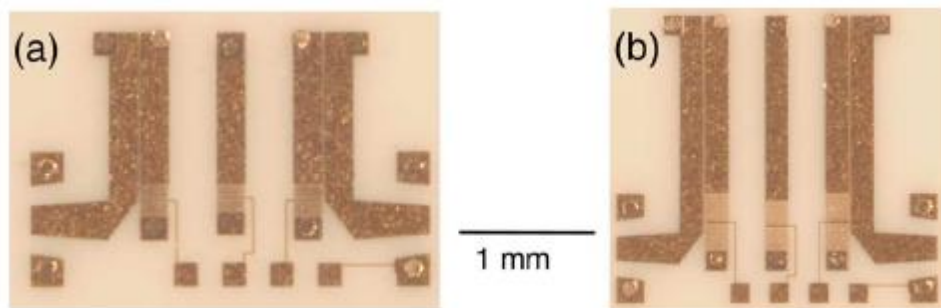
Figure 2.7: Optical micrographs of the a) Ku-band and (b) X-band tunable combline bandpass filter [122].

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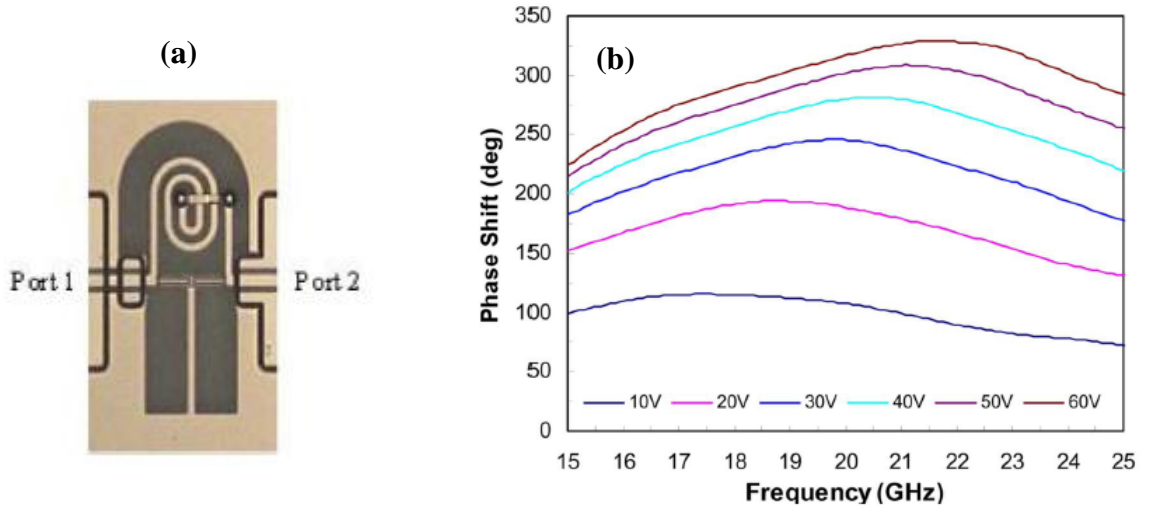
Figure 2.8: (a) The fabricated 20 GHz phase shifter with a dimension of 0.95 x 1.32 x 0.5 mm^2 and (b) the measured phase shifts from 10 to 60 V [12].
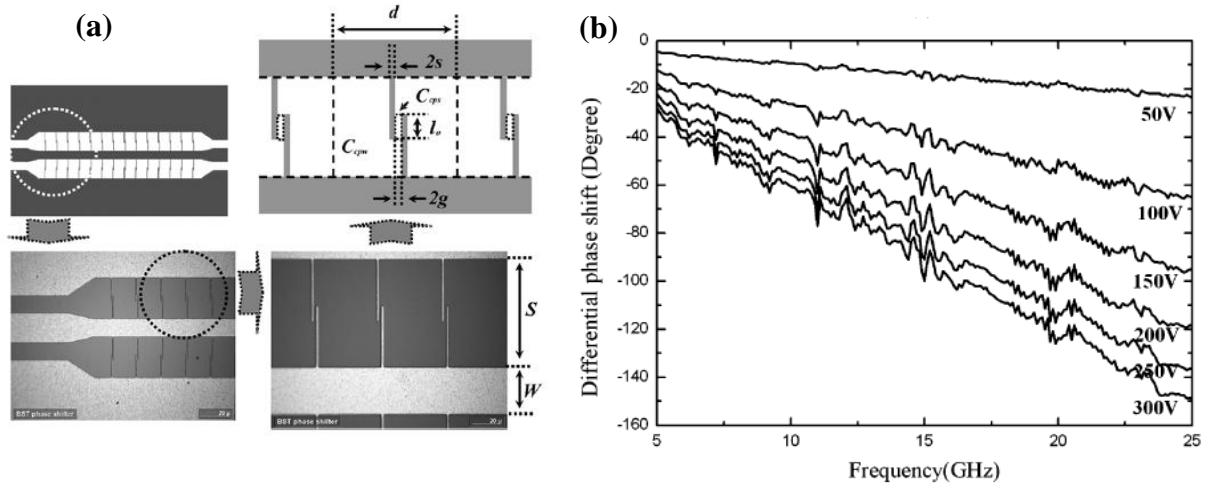
Figure 2.9: (a) Schematic diagram and photographs of the BST phase shifter along with the schematic unit cell of the CPS-CPW structure and (b) the measured phase shifts [13].

Figure 2.9 (a) shows the bilateral CPW phase shifters employed in a power distribution network for Ku-band antenna array applications [13]. A 350 nm thick BST thin film was deposited on a surface-treated high resistivity silicon substrate by the sputtering method. The

maximum insertion loss achieved was 2.6 dB at 15 GHz. Continuous phase shifts from 0 to 90º with a figure of merit of 36º/dB at 15 GHz are shown in Figure 2.9 (b).

Several other works based on BST phase shifters have also been developed. A CPW line periodically loaded with BST IDCs where a few matching networks were connected in series to form a new phase shifter structure [126], a phase shifter with large phase shifts at low tuning voltage and BST/YIG bilayer for phase shifting applications [127, 128] and a digital reflection-type phase shifter was built [129].

In addition to many potential applications of BST varactors in filters and phase shifters, they can also be implemented as part of matching networks and switches. In [14], a quad-band tunable matching network loaded with off-the-shelf doped BST capacitors for cellular power amplifier applications was developed. This is presented in Figure 2.10 (a). The input impedance varied from 3.44 – j1.87 to 3.55 – j0.02 Ω and 4.28 – j0.06 to 4.31 + j0.97 Ω with a power gain variation of -1.35 to -1.62 dB and -2.05 to -1.79 dB when operated for GSM850/900 and DCS/PCS frequency bands respectively as shown in Figure 2.10 (b). BST thin film parallel-plate capacitors were also used as tuning elements in an impedance tuner, which consisted of a phase shifter and a variable transformer for adaptive matching applications [130].

A switching mechanism based on the dielectric tunability of a shunted BST thin film varactor between two CPW ground lines is depicted in Figure 2.11 (a); the device was fabricated on a multilayer substrate [15]. The OFF- and ON-states mechanism were determined by the biasing voltage of the varactors, where the capacitance will be the highest at 0 V resulting in isolation between the output and input ports and lowest at 10 V due to the signal passing through between the ports. Figure 2.11 (b) shows the scattering parameters for the OFF- and ON- states. The resistive switching performance of BST thin films with tungsten and platinum electrodes were also investigated in [131], in which the application of tungsten electrodes revealed a performance that was superior to platinum electrodes.
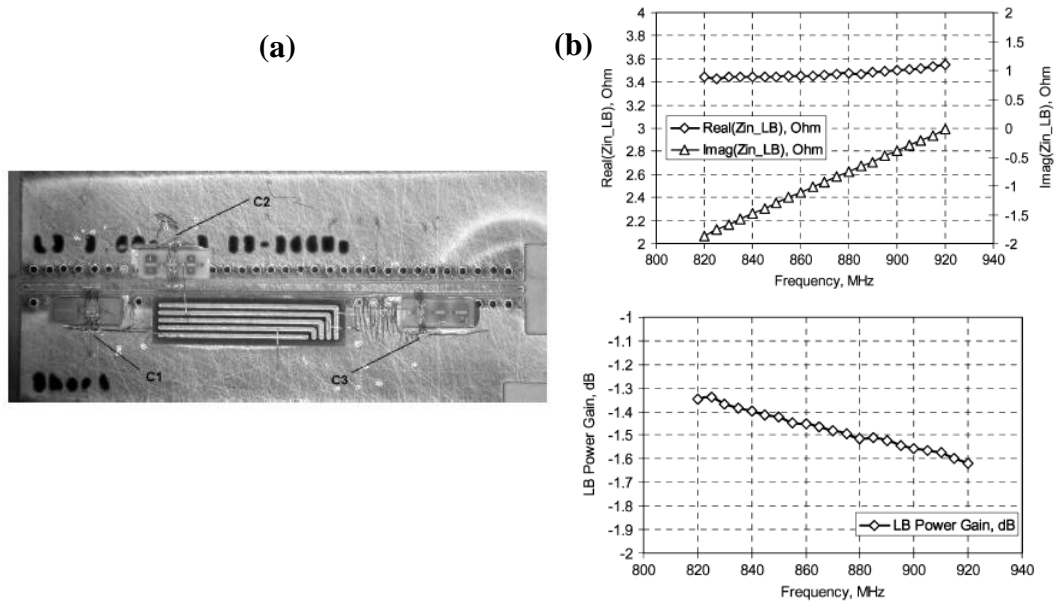
Figure 2.10: (a) Fabricated tunable matching network loaded with doped BST capacitors (C1, C2 and C3) and (b) the input impedance (top) and power gain variation (bottom) for GSM850/900 frequency band [14].
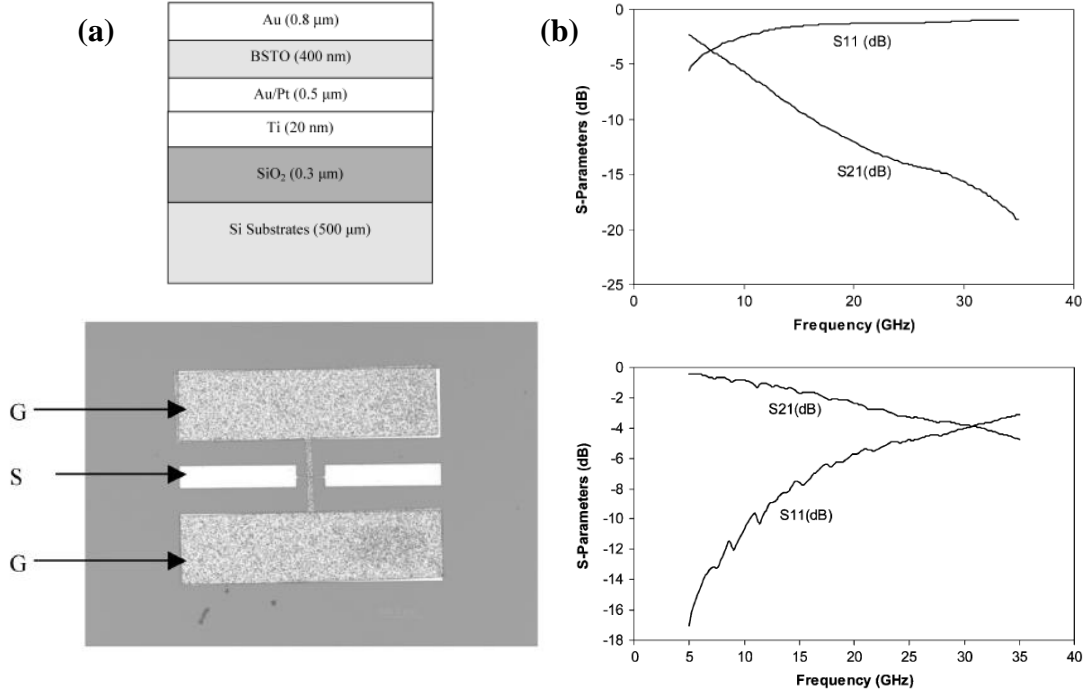
Figure 2.11: (a) Cross-sectional view of the multilayer substrate and the fabricated BST varactor shunt switch and (b) scattering parameters for the OFF-(top) and ON-(bottom) states [15].

2.5 Intermodulation Distortion in Microwave Varactors

BST is a high-permittivity material which exhibits a nonlinear *C-V* characteristic [132]. When an RF signal is applied across the BST varactor increases, the capacitance of the device tends to deviate from the value determined by the DC voltage, leading to signal compression [19]. If a single tone is applied, it will cause harmonics of the fundamental frequency that could easily be removed by proper filtering. However, when two or more tones are applied, intermodulation distortion will occur. In Figure 2.12, in the case of two-tone applied, the third-order intermodulation products $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ occur very close to the fundamental frequencies (ω_1 and ω_2) and are difficult to remove by filtering [21]. This results in linearity degradation of the microwave devices and hence lowers the dynamic range. Therefore, it is important to analyse the intermodulation distortion in nonlinear devices and to develop promising techniques to suppress or - even better - to eliminate it completely.
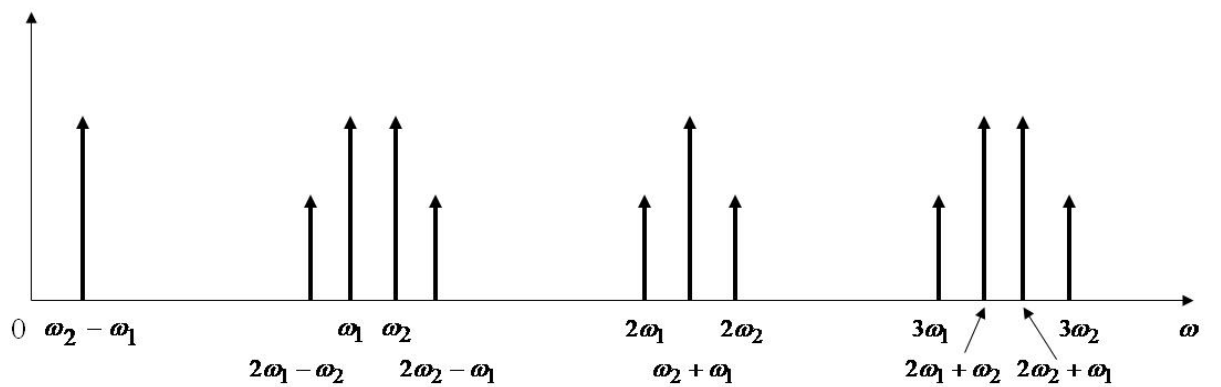
Figure 2.12: Output spectrum of second- and third-order two-tone intermodulation products, in which $\omega_1 < \omega_2$.

2.5.1 Intermodulation Distortion in Varactor Diodes

Several research works related to intermodulation distortion in nonlinear microwave varactors have been demonstrated. The intermodulation distortion in varactor diodes were analysed using Volterra series approach and closed-form expressions for the intermodulation distortion were successfully derived [133]. Figure 2.13 shows the two main topologies, anti-series and anti-parallel varactor diode circuits which were proposed and experimentally verified for achieving minimum distortions. Based on Figure 2.13 (a), the capacitance of each diode in the anti-parallel topology can be represented by a power series as a function of the incremental voltage, v.

$$C(v) = A_0 + A_1 v + A_2 v^2 + ... \tag{2.1}$$

$$C(v) = B_0 - B_1 v + B_2 v^2 + ... \tag{2.2}$$

The equation in (2.2) represents the diode operating in reversed-biased voltage. When both diodes are equal, the total capacitance yields

$$C(v) = 2C_0 + 2C_2 v^2 + ... \tag{2.3}$$

Here, it can be observed that the new second-order coefficient, C_1 is totally eliminated but the new first- and third-order coefficients, C_0 and C_2 are doubled.
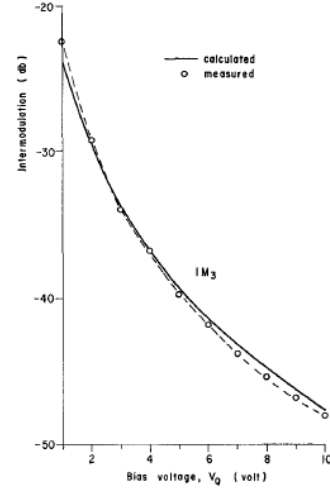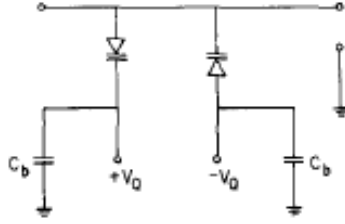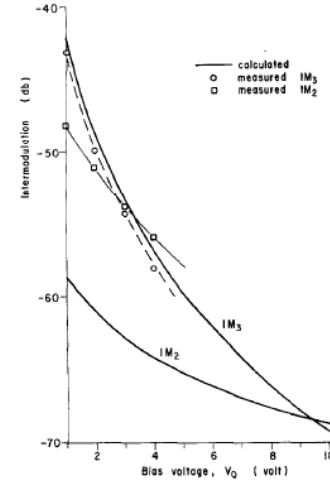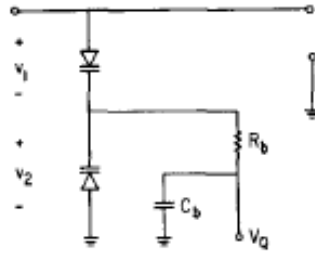
Figure 2.13: (a) Anti-parallel and (b) back-to-back (anti-series) varactor diode topologies with their calculated and measured intermodulation distortions [133].

For the back-to-back (anti-series) topology in Figure 2.13 (b), the resulting total capacitance for matched diodes yields

$$C(v) = \frac{M_0}{2} + \frac{M_2}{8}\left[1 - \frac{1.5M_1^2}{M_0 M_2}\right]v^2 \qquad (2.4)$$

where the new $C_0 = \frac{M_0}{2}$, $C_1 = 0$ and $C_2 = \frac{M_2}{8}\left[1 - \frac{1.5M_1^2}{M_0 M_2}\right]v^2$ are determined. It can be observed that the first-, second- and third-order coefficients are halved, eliminated and 1/8 of the single diode, leading to a much reduced intermodulation distortion. The term in the

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parentheses shows the second-order interaction term and the possibility of eliminating this coefficient if the doping profile, n = 0.5 [133].

Since this breakthrough, several research groups working in the varactor diode technology have implemented this idea. A research group from Delft University of Technology have conducted intensive research in developing various varactor diode topologies using highly Q silicon-on-glass (SOG) technology for semiconductor microwave devices. The anti-series and anti-parallel varactor topologies were first introduced in [134]. Figure 2.14 (a) shows the anti-series topology which has a condition of n ≥ 0.5 for setting both C_1 and C_2 to zero. However, if n > 0.5, C_2 will be zero but not C_1. This can be resolved by placing an identical stack in anti-parallel topology as shown in Figure 2.14 (b). The anti-series varactor diode topologies were employed in a tunable matching network [135], multi-band multi-mode class-AB power amplifier [136], bandpass filter [137] and a phase-shifter [138], all integrated on SOG technology.
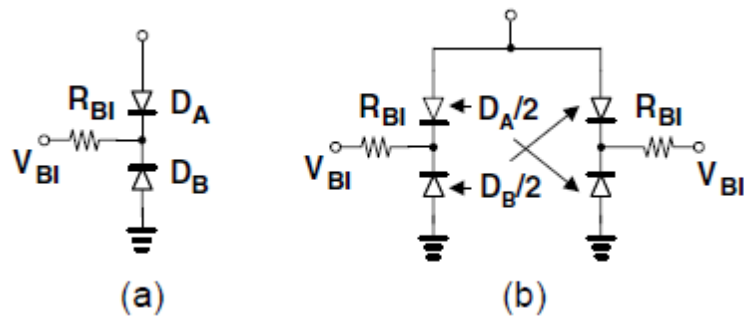
Figure 2.14: (a) Anti-series and (b) Anti-series/anti-parallel topologies for varactor diodes [134].

2.5.2 Intermodulation Distortion in BST Thin Film Varactors

A research group from the University of Michigan, Ann Arbor was among the first research groups to employ the anti-series topology concept in BST thin film varactors. In Figure 2.15

(a), the device architecture was modified by connecting several BST parallel-plate capacitors in an anti-series configuration [19]. The BST capacitors in Figure 2.15 (b) were fabricated on a sapphire substrate. Silicon chromium (SiCr) which served as thin film resistors that linked the top and bottom electrodes were sputtered to ensure equal biasing on each capacitor. As mentioned earlier, the capacitance values tend to deviate from the value set by the DC voltage when increasingly RF signal is applied. However, by connecting several parallel-plate capacitors in series, this effectively reduces the RF swing across each capacitor and thus improves the linearity of the overall device. An improvement of 16 dB of the third-order intercept point at input (IIP3) was achieved compared to the single capacitor. The drawback of this technique is the area of the device increased by N^2 to the number of N capacitors being stacked together in order to maintain the same capacitance value as the single capacitor.

(a)

(b)
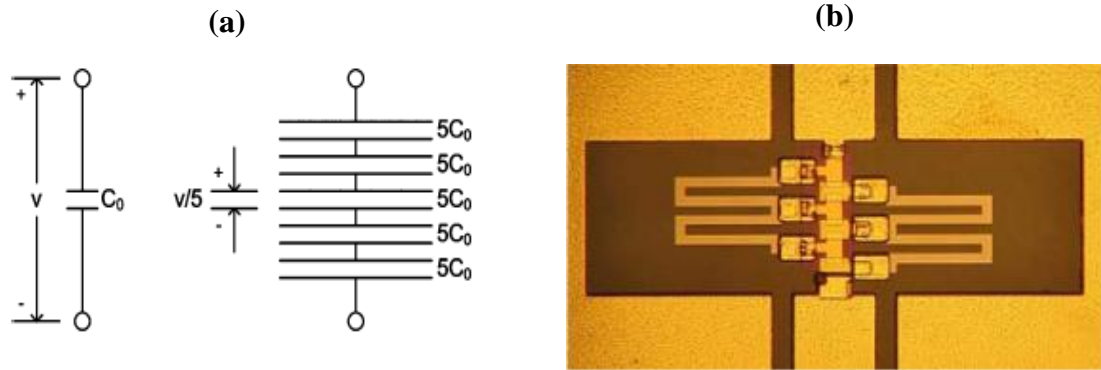
Figure 2.15: (a) Illustration of a basic concept of a five-stacked capacitor and (b) Fabrication of five-stacked capacitor [19].

A group from Georgia Institute of Technology had proposed a technique using separate RF and DC electrodes in their device architecture [20]. In Figure 2.16, the BST tunable capacitors were fabricated on sapphire substrates. The DC electrodes with a smaller gap were placed in between the wider gap of the RF electrodes. The two types of structure that produced a 6 dB

improvement of IIP3 compared to the conventional structure are the attached-bias-electrodes (ABE) and isolated-bias-electrodes (IBE) schemes as illustrated in Figures 2.16 (a) and (b) respectively. The DC electrodes were made from high resistivity materials of indium tin oxide (ITO) or lanthanum strontium cobalt oxide (LSCO) which decoupled the DC bias from the RF signals to ensure low intermodulation distortion. However, the tunability and Q-factor achieved were quite low.
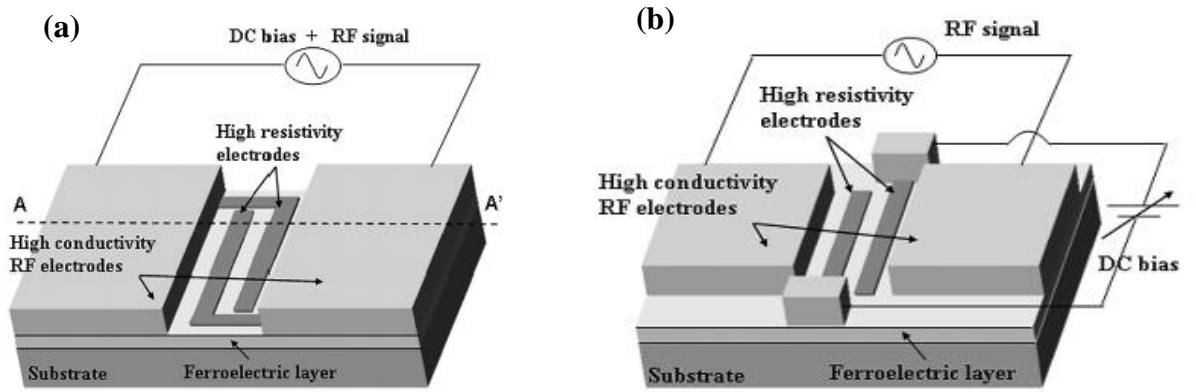
Figure 2.16: (a) Attached-bias-electrodes (ABE) and (b) Isolated-bias-electrodes (IBE) [20].

Apart from potential techniques to improve the linearity of BST thin film varactors, the temperature and voltage impact on the third-order intermodulation distortion (IM$_3$) in BST thin film varactors had also been experimentally demonstrated as shown in Figure 2.17 [139]. A dip/sweet spot occurred near 20 dBm of input RF power was observed, indicating interference from the higher-order IM$_3$ (5th and 7th). This dip was shifted to higher voltages as bias voltage increased. Also, as the temperature increased with the bias voltage fixed at 0 V, the power level of the third-order IM$_3$ decreased, which correlated to the overall compression of the *C-V* curve with increased temperature.
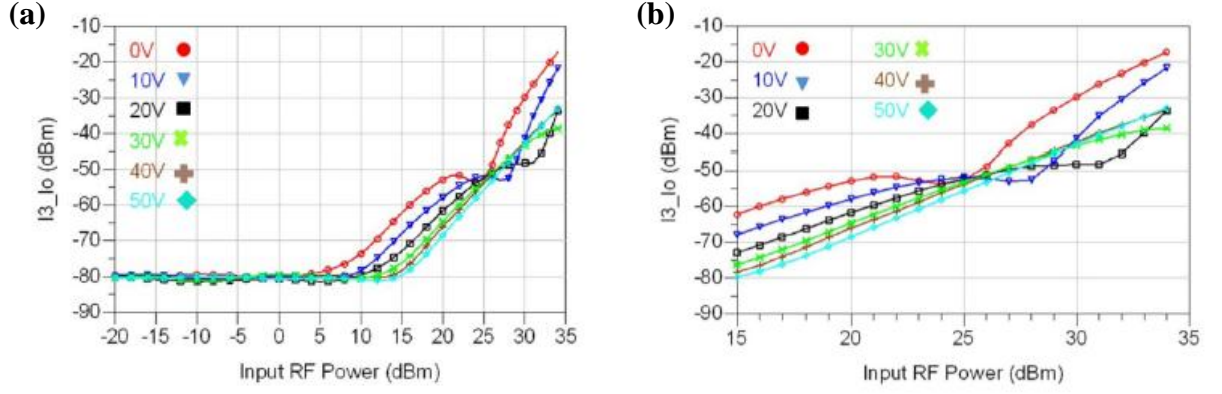
Figure 2.17: (a) The third-order intermodulation distortion, $2f_1 - 2f_2$ (0.99 GHz) with increasing input RF power at different bias voltages and (b) the shifts in the dip at 25 ºC [139].

2.6 Power Handling Capability in BST Varactors

Ideally, when an input RF/microwave signal is increasingly applied to nonlinear microwave components such as varactor diodes and transistors, gain compression would eventually occur and this led to increased microwave losses and signal distortions at the output terminal. This is an undesirable trait, particularly in the transmitter circuit where large output signal is expected. In order to quantify the linear operating range of the device, 1 dB compression point is defined where it is the power level in which the output power has reduced by 1 dB from its ideal characteristic [21]. This power level is important in observing how much power a certain microwave component could handle and still function properly. There is limited research discussing the importance of power handling capability (PHC) of BST varactors.

In Figure 2.18 (a), BST thin film parallel-plate capacitors were fabricated on silicon wafers and single-tone RF signal amplitudes were increasingly applied to observe the effect on their tunability [22]. It is observed that in Figure 2.18 (b), the tunability decreases as RF signal amplitude increases from 0.69 to 2.58 V_{rms}. A similar method was demonstrated in [23],

where a 1.95 GHz single-tone excitation with increasingly input power levels was applied to a BST filter. The large signal, S_{21} of the BST filter, however, became distorted at certain input power levels due to the nonlinear behaviour of the BST varactor element.

(a)   **(b)**
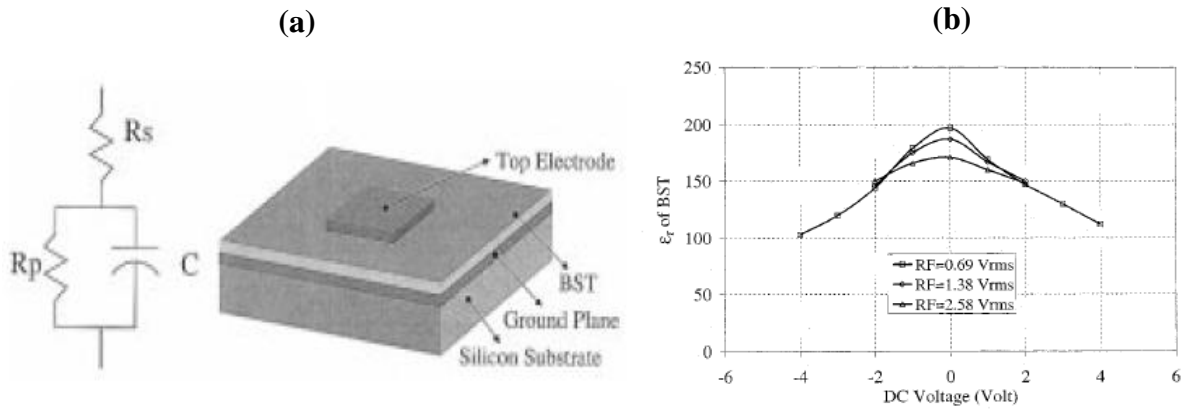
Figure 2.18: (a) BST parallel-plate capacitor and its equivalent circuit model and (b) Relative permittivity of BST for high RF voltages at frequency of 50 MHz and BST thickness of 700 Å [22].

A more detailed research of the PHC of BST thick film capacitors was demonstrated by a research group from the State Electrotechnical University. Microstrip resonators loaded with planar and parallel-plate BST varactors were investigated based on their nonlinear responses to the elevated microwave power [24, 25]. Figure 2.19 (a) shows the BST planar capacitor and experimental setup. One of the methods used was the measurement of the anharmonic response of the varactors to a pulsed microwave signal at 10 GHz where thermal and electric field effects that contribute to the nonlinearity of the varactors can be analysed separately. Figure 2.19 (b) shows that by increasing the microwave power, the peak of the resonance curve, S_{21} is shifted towards higher frequencies and becomes asymmetrical. This is obvious in the trailing front due to the thermal effect on the dielectric properties of BST film. Complex formulas of PHCs in terms of thermal and E-field effects were subsequently derived. It was

concluded that the PHC of the planar and parallel-plate varactors were limited by the thermal and electric field effects respectively. Therefore, parallel-plate varactors are useful in low power microwave systems.
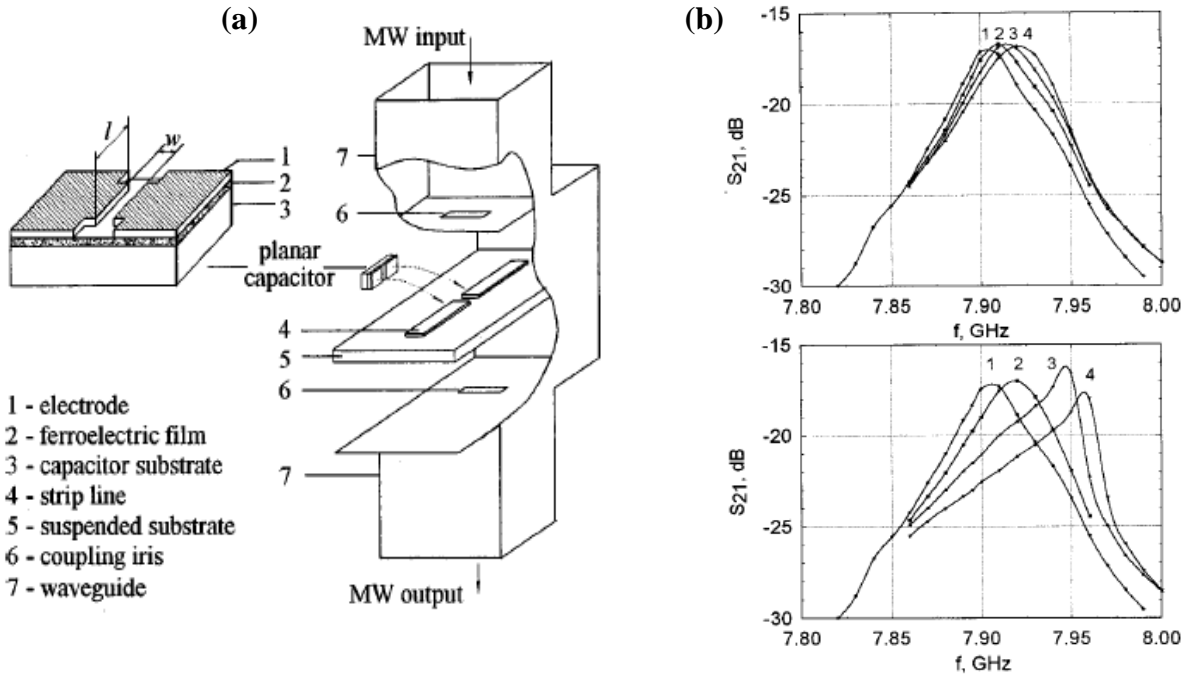
Figure 2.19: (a) The BST planar capacitor and experimental setup and (b) Frequency response of BST film capacitor-loaded resonator to pulsed microwave power of various levels measured at leading (top) and trailing (bottom) fronts. Incident power levels P_{inc} : (1) +6 dBm, (2) +26 dBm, (3) +32 dBm, and (4) +35 dBm [25].

2.7 Conclusions

The potential of barium strontium titanate in agile microwave devices was known about 50 years ago but intensive research has only been made in the past 20 years due to the development of thick and thin film technologies. In the 'varactor gap' region, BST thin film varactors have significantly higher Q-factor, power handling and tuning speed compared to the varactor diode technology. In comparison to its bulk material, BST thin film has a lower dielectric constant and higher dielectric loss. However, a low bias voltage is required to tune the capacitance of the BST thin film varactor, making it attractive to integrate it into semiconductor microwave circuits.

The two most common deposition techniques are sputtering and PLD due to the availability in most research labs. Sputtering has a large-area deposition capability and precise thickness control. However, the stoichiometry of the sputtered thin films is usually difficult to control. In the research community, PLD is considered one of the cheapest deposition technique as the laser may be shared among several deposition systems. Sol-gel deposition technique has the advantage of a non-existent vacuum system which reduces cost. However, problems with surface roughness, non-uniform thickness, existence of cracks and voids limit its usage in thin film applications [3]. MOCVD technique offers composition control and high conformality but the system is rather expensive. It requires a high temperature furnace, thus limiting the choice of substrates. The CCVD technique is cost-effective; it requires no vacuum chambers or reaction furnace but it has been demonstrated that the synthesis of thin films is mostly oxide thin films [140].

BST varactors usually have two basic structures, co-planar and parallel-plate configurations. Both structures require a DC voltage to tune the dielectric permittivity of the BST material which correlates to the change of its capacitance values. A co-planar varactor is easier to fabricate since the metal electrodes are built directly on top of the BST/substrate

structure but at the expense of a high tuning voltage due to the non-tunable partial capacitances [141]. On the other hand, a parallel-plate varactor provides low tuning voltage which compensates the complexity of its fabrication process.

Several research groups have demonstrated the employment of BST thin film varactors in agile microwave devices. The most often-reported in literature are the tunable BST-based filters and phase shifters in which they have the potential to be implemented in wireless transceivers and phase array antennas respectively. Tunable matching networks and switches have also been reported for cellular power amplifier and wireless sensor applications.

Intermodulation distortion in BST varactors has a significant effect within the passband if two or more RF signals are applied. This will lead to linearity degradation of the varactors. Anti-parallel and anti-series topologies were introduced for varactor diodes back in the 1970s. Since then, several research groups have demonstrated the effectiveness of implementing this idea in their respective fields to enhance linearity of the devices. BST-stacked parallel-plate varactors have been demonstrated by connecting several varactors in series which improved the overall linearity of the device structure. Apart from that, the introduction of new bias electrode schemes placed between the wider gaps of the RF electrodes has improved the IIP3 of the device. However, the analysis of the intermodulation distortion in BST varactors is currently deficient. Although voltage and temperature impacts on the IM_3 had been experimentally demonstrated in [139], a further effort to improve the theoretical model of predicting the IM_3 was emphasized. Since no research group has yet to develop it, hence this research work will focus on creating a reliable theoretical model for the analysis of IM_3 in BST varactors and solutions to improve the linearity of the devices will be addressed.

The information of power handling capability in BST varactors is also limited, especially in research relating to the 1 dB compression point. A few research groups have shown the compression of the BST tunability and the distortion of the S_{21} curve as increasingly single-tone input power was applied. A more in-depth research relating to microstrip resonators

loaded with planar and parallel-plate BST thick varactors was experimentally demonstrated, using a pulsed microwave signal. Complex power handling capability formulas in terms of electric and thermal field effects were theoretically derived. However, no method has been reported to increase the 1 dB compression points of BST varactors and this will be another focus of this research work.

The major objective of this research is to develop a novel method for the theoretical analysis of the third-order intermodulation distortion in BST thin film interdigital capacitors (IDCs). BST thin films are grown directly on r-plane sapphire substrates, which have the potential to be integrated with existing semiconductor microwave technologies. Two BST varactor circuit topologies are proposed to validate the theoretical analysis in comparison with the circuit simulation results. In both topologies, the third-order intermodulation distortion is also experimentally verified. The details of this work are thoroughly discussed in Chapter 4.

Another objective of this research is to develop BST varactors with high 1 dB compression points. These varactors have the potential to be implemented in tunable filters of a high power transceiver system. The geometry of the IDC in terms of the finger gap, width, length and number of fingers is varied and its influences on the shape of the nonlinear BST C-V curves are analysed. From the parametric analysis, three distinct C-V curves are defined and the relationship between their tunabilities and 1 dB compression points are determined by circuit simulations and measurements. The details of this work are thoroughly discussed in Chapter 5.

Chapter 3

Part I: Material Deposition and Characterisation of BST Thin Films

Part II: Fabrication and Microwave Characterisation of BST Thin Film Varactors

3.1 Introduction

As reported in Chapter 2, many research groups have found applications of BST thin film varactors in agile microwave devices. Epitaxially-grown BST thin films on c- and r-plane

sapphire substrates have also been successfully employed as tuning elements [11, 12, 63, 65]. In this research, both orientations were used as the host substrates to fabricate the BST interdigital capacitors (IDCs). Sapphire is well-known to have excellent microwave properties; low loss at high frequencies (*tan δ = 1x10⁻⁴*) and a reasonably high dielectric constant. More importantly, it has a close lattice match to BST thin film which enables epitaxial growth [3]. The r-plane sapphire substrates were used for the BST varactor circuit topologies introduced in Chapter 4 and c-plane sapphire substrates were used for the BST varactors with fine geometries introduced in Chapter 5. The deposited BST on r-plane sapphire substrates were realised using Pulse Laser Deposition (PLD) [9, 142] in collaboration with Dr. Ernest Fardin and will not be discussed in this thesis.

This chapter has two parts. Part I investigates the material deposition and characterisation of the BST thin films on c-plane sapphire substrates. BST thin films were initially deposited using the RF magnetron sputtering machine at RMIT University. The materials properties of these films were then characterised in terms of their physical and chemical properties by different analytical techniques such as X-Ray Diffraction (XRD), X-Ray Photoelectron Spectroscopy (XPS), and Scanning Electron Microscopy (SEM). Part II involves the fabrication and microwave characterisation of the BST IDCs. The multistep fabrication process was executed in the clean room facility and the performances of the IDCs produced were measured on a probe station connected to a Vector Network Analyser (VNA) at RMIT University.

3.2 BST Thin Film Deposition using RF Magnetron Sputtering System

As mentioned in Chapter 2, sputtering is one of the most common PVD techniques for depositing perovskite ferroelectric thin films. It offers high uniformity, scalability, low thermal budget and compatibility with standard IC processing [2]. There are different types of sputtering methods, which includes DC sputtering, RF sputtering and DC/RF sputtering. RF sputtering is used to deposit highly insulating oxide or nitride films and magnetic fields (magnetron) can be applied to improve the sputtering performance [143].

A schematic of a typical RF magnetron sputtering system is depicted in Figure 3.1. The sputtering system consists of a source/cathode and the substrate on which the film is to be deposited inside a vacuum chamber, two inlets for the inert (Ar) and reactive (O_2) gases and vacuum pumps. Initially, the chamber is evacuated to a high vacuum, achieving the base pressure range of 10^{-3} to 10^{-5} Torr and Ar/O_2 gas mixture is then flowed into the vacuum chamber. A few hundred Watts of RF power are applied to the sputtering target, creating a plasma discharge. This results in the positively charged Ar ions bombarding the target surface, which sputter off atoms from the surface into the gas phase. These atoms are then directed towards the substrate to form a thin film. Some electrons, known as secondary electrons, are also emitted from the target surface. The plasma discharge is sustained through the collisions of these secondary electrons with the gas atoms to form more ions. A magnetron, which is an array of magnets employed behind the sputtering target, generates a static magnetic field at the cathode. This magnetic field causes the secondary electrons to move in a current loop "parallel" to the cathode surface. Trapping these electrons close to the target leads to enhanced ionisation of sputtering gas and thus increases the deposition rate.

For sputtering of an insulating target material such as oxide ferroelectrics (e.g. BST), a high frequency plasma discharge must be applied to avoid the accumulation of electric load. This power supply operates at 13.56 MHz and an impedance matching network which consists of inductors and capacitors is also required. The material properties of the sputtered thin films depend on the parameters of the deposition runs. These include substrate temperature, substrate to target distance, process gas pressure, process gas mixture and the RF power applied [142].
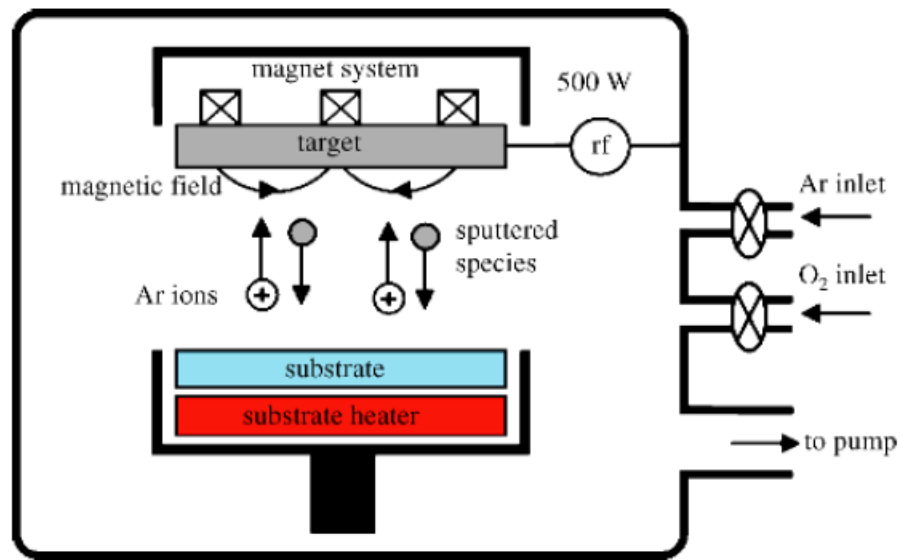
Figure 3.1: Schematic of a typical RF magnetron sputtering system [2].

BST thin films were deposited for the first time using the *Kurt J. Lesker* RF magnetron sputterer at the Microelectronics and Materials Technology Centre (MMTC), RMIT University (Figure 3.2). A few deposition runs were completed using a stoichiometric 100 mm diameter $Ba_{0.6}Sr_{0.4}TiO_3$ target (purchased from *William Advanced Materials*). The deposition conditions were held constant as tabulated in Table 3.1. The deposition conditions of the previous deposition runs [6, 9, 142] and also from other research groups [4, 5] were also used as references. After setting the deposition conditions, the BST thin films were

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sputtered on diced 10 x 10 mm^2 single c-plane sapphire substrates (purchased from *M.M.R.C Pty Ltd*). These samples were initially cleaned with acetone, IPA or methanol and DI water. The details of sample preparation and the fabrication process are discussed in Section 3.5. The low process gas pressure was set to achieve maximum growth rate and very smooth thin film surface which indicated high density of BST thin films. Further, utilising low gas pressure could avoid the decrease in the A-to-B site ratio [5], which would consequently decrease the tunability of the BST varactors. 100% argon was used in the initial deposition of the samples and then post-annealed to improve the crystallinity of the films.

Figure 3.2: *Kurt J. Lesker* RF magnetron sputterer.

Table 3.1: The deposition conditions of the sputtered BST thin films.

Parameter	Value
RF power (W)	200
Substrate temperature (℃)	700
Substrate to target distance (mm)	150
Process gas pressure (mTorr)	5
Process gas mixture (%)	100 % Argon
Deposition duration (hours)	8

3.3 Material Characterisation of BST Thin Films

Several different analytical techniques were employed to determine the physical and chemical properties of the BST thin films. The sputtered BST thin films were annealed in a vacuum oven and air at different temperatures and duration in order to investigate the influence on the crystal structure of the thin films via XRD. XPS provided the chemical composition of the BST thin films and correlated with the XRD data for the unannealed and annealed samples. SEM was implemented to analyse the thickness and provided information about the BST surface morphology.

3.3.1 X-Ray Diffraction (XRD)

XRD is a well-known crystallographic technique for identifying and quantifying various crystalline phases present in solid materials and powders [143]. When a solid material with repeating atoms that form a series of parallel planes separated by a distance, d is illuminated by an x-ray beam, λ at an angle, θ, diffraction occurs. This diffraction pattern represents the

crystal structure of the material and the crystal phases can be determined from internationally known databases. In Figure 3.3, constructive interference occurs only when the distance travelled by the reflected beams, 1' and 2' differs by an integer number, n of wavelengths. This condition, known as Braggs Law, is expressed as

$$n\lambda = 2d \sin \theta \qquad (3.1)$$

The crystalline phases of the BST thin film samples were analysed using a *Bruker AXS D8 Discover* powder diffractometer located at the RMIT Chemistry Department, School of Applied Sciences, and is shown in Figure 3.4. In the paths of the incident beam from the CuK_α ($\lambda = 0.15406$ nm) source and reflected beam from the sample, Soller slits are fixed which collimate both beams in one dimension. A fixed 1 mm slit in the incident beam limits the divergence of x-rays normal to the plane of the Soller slits and a Ni filter is used to attenuate the CuK_β radiation, and the background continuum, from the x-ray source [142].
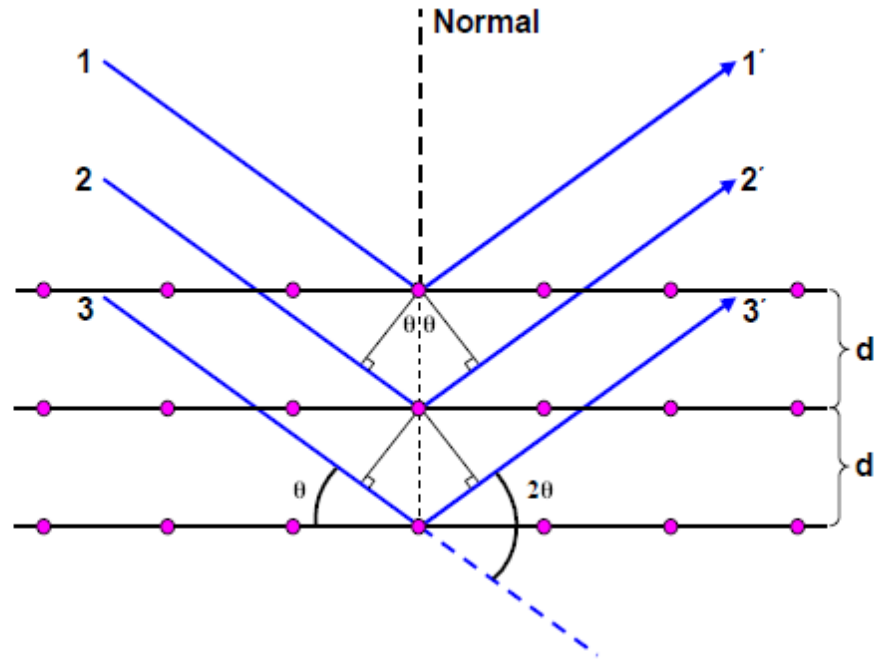
Figure 3.3: XRD from a solid material [142].

Figure 3.4: *Bruker AXS D8 Discover* powder diffractometer with GADDS (General Area Detector Diffraction System).

The XRD results for the first batch of BST thin film samples are shown in Figure 3.5. The BST thin films were deposited on three 10 x 10 mm^2 diced c-plane sapphire substrates (BST1, BST2 and BST3) with deposition temperature of 700 ℃ at 5 mTorr for 8 hours. The major peaks were observed at (100), (110) and (111) in all films, corresponding to the cubic perovskite BST phase with no indication of secondary phase formation. An initial decision was made to post-anneal two samples, BST1 and BST3 in a vacuum oven at 700 ℃. It was observed that the BST1 peak intensities at (100) and (200) increased after post-annealing for 10 minutes.

However, the BST3 peak intensities at (110) and (111) decreased after post-annealing for an hour. This implied a loss of crystallinity had occurred on annealing, most probably due to the presence of oxygen vacancies in the film. This condition was also in agreement with the XPS results of the sample, which is discussed in the next subsection. It was also observed that the baseline/background in the annealed sample was reduced and the peaks were more

resolved, more symmetrical and also not as broad. This provided evidence of an overall decrease of amorphous content in the bulk sample, and therefore a general improvement in the degree of crystallinity over the bulk sample. The narrower peaks also implied that the grain size was slightly larger than prior to post-annealing.

The second batch of BST thin film samples was deposited with the similar deposition conditions as before and one sample was post-annealed in air at 900 ℃ for 2 hours in a ceramic tube furnace. The results are shown in Figure 3.6. A stronger (110) orientation was observed in the annealed sample, indicating an improved crystallinity and preferred orientation for this film.
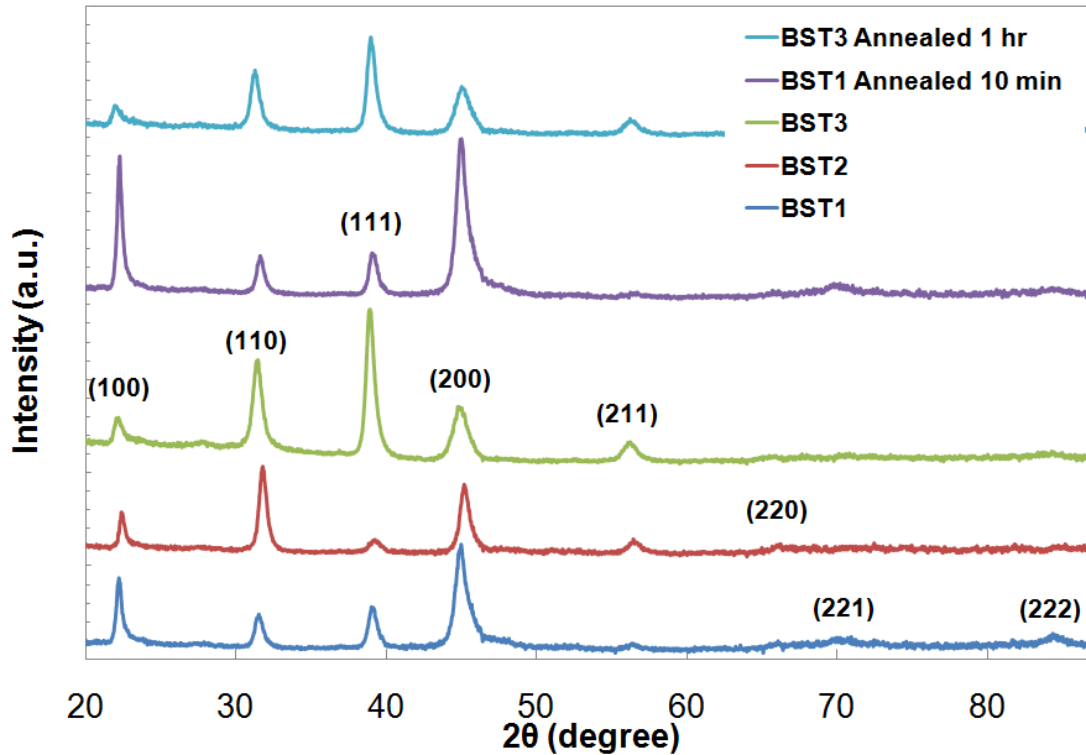
Figure 3.5: XRD patterns for the first batch of deposited BST thin film on c-plane sapphire substrates.
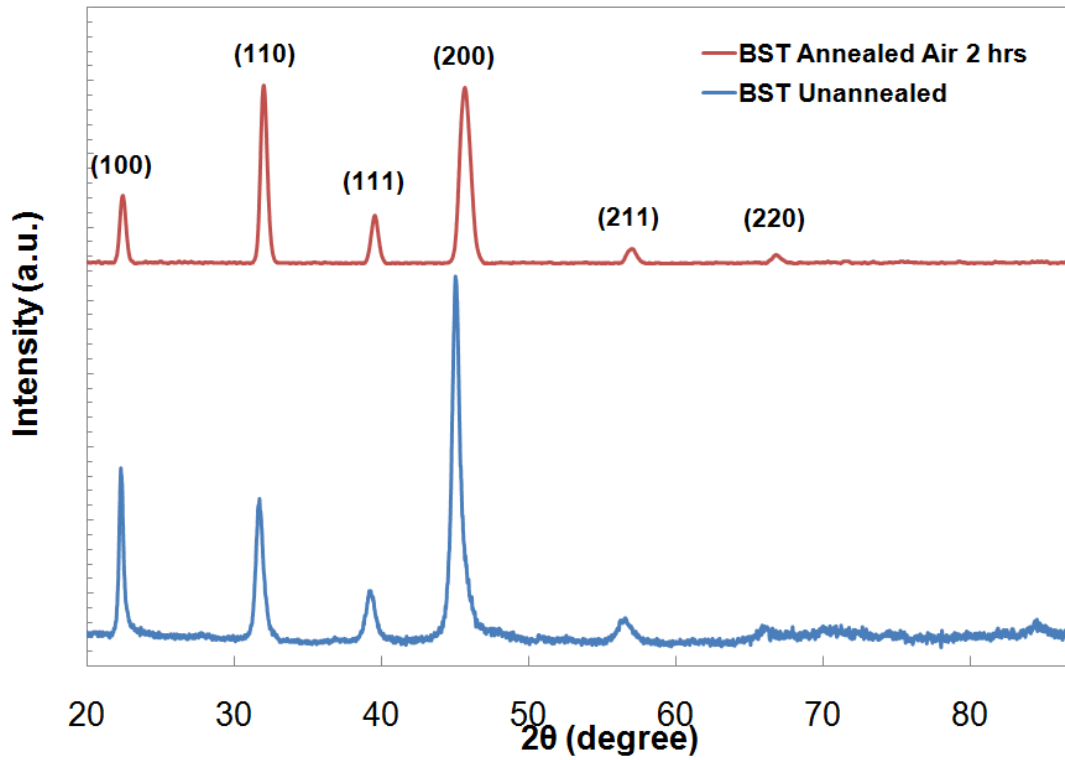
Figure 3.6: XRD patterns for the second batch of deposited BST thin film on c-plane sapphire substrates.

3.3.2 X-Ray Photoelectron Spectroscopy (XPS)

XPS is useful for identifying elements of a material, their chemical composition and empirical formulae within the first few atomic layers [143]. Based on the photoelectric effect in Figure 3.7, the sample is bombarded with an X-ray beam which causes photoelectrons to be ejected from the surface. The x-rays interact with the atomic electrons of the sample, primarily through photon absorption. The ejected photoelectrons escape (≤ 10 nm) from the very top of the surface and the kinetic energy is detected and analysed as a spectrum of their binding energies. This spectrum is compared with internationally known databases and the elements of the material exhibit their own unique characteristic peaks. The BST thin film samples were analysed using the *Thermo K-Alpha* spectrometer at the RMIT Microscopy and Microanalysis Facility (RMMF) (Figure 3.8).
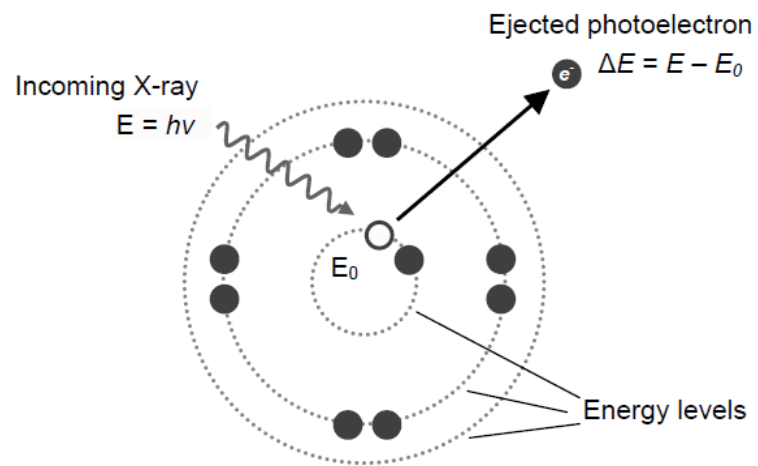
Figure 3.7: Electron orbits showing the ejection of a photoelectron after absorption of a photon [143].

Figure 3.8: *Thermo K-Alpha* spectrometer.

The XPS results for the first batch of BST thin film samples are shown in Table 3.2. As highlighted in Chapter 2, BST has a chemical composition of $Ba_xSr_{1-x}TiO_3$. The ideal atomic concentration (at. %) of the BST thin film is 10 at. % Ba, 10 at. % Sr, 20 at. % Ti and 60 at. % O [142]. As observed in Table 3.2, the first batch of the unannealed BST1 and BST3 samples had a close characteristic to the ideal composition. However, when both samples were post-annealed in vacuum oven, the at. % of O increased but at. % of Ba and Ti decreased. The significant reduction in at. % of Ba and Ti and the sudden increase in at. % of O suggested the presence of defects or deformations in the crystal structure of the films which implied the existence of oxygen vacancies in both annealed samples.

As highlighted in Chapter 2, BST is naturally perovskite with the ABO_3 structure and the A-to-B site ratio is an important predictor of the defect density and quality of the film structure [5]. From calculations based on Table 3.2, the A-to-B site ratio for BST1 had reduced from 1.1 to 1.07, before and after annealing it for 10 minutes in a vacuum oven respectively. However, with the BST3 sample this ratio had increased from 1.06 to 1.12, before and after annealing the sample for an hour in a vacuum oven. The slightly decreasing trend of the A-to-B site ratio in BST1 indicated that the annealed sample had lower dielectric constant and hence lower tunability along with lower loss and higher breakdown field strength [144] compared to its unannealed form. The slightly increasing trend of the ratio in BST3 suggested that the annealed sample had higher dielectric constant (higher tunability) but with higher loss and lower breakdown field strength compared to its unannealed form.

Figure 3.9 shows the O1s core level spectra for both BST1 and BST3 samples before and after annealing them at 700 ℃ for 10 minutes and an hour respectively in a vacuum oven. As observed, the OI peak in both annealed samples corresponded to the oxygen atom in the perovskite structure of BST [77]. The shoulder-like OII peak existed in both annealed samples and corresponded to the non-perovskite structure of BST, which implied the existence of oxygen vacancies in the films. Oxygen vacancies act as charged defects and contribute to

additional extrinsic microwave losses [145]. They also cause internal strains which are associated with the lattice mismatch and thermal expansion coefficient mismatch between the ferroelectric film and substrate [36, 37, 146]. In Section 3.6, it is shown that the strain-induced BST films significantly influence the performance of the fabricated BST varactors.

XPS analysis of the second batch of the BST thin film is tabulated in Table 3.3. The sample was post-annealed in air at 900 ºC for 2 hours. In this case, both the at. % of Ba and O increased but the at. % of Sr and Ti decreased. The increase in at. % of Ba and O suggested an improved crystallinity on annealing due to the incorporation of oxygen in the films. The A-to-B site ratio increased significantly from 1.39 to 1.88 before and after annealing the sample. Apart from the increased ratio attribute, this condition also indicated that the stress was vastly relaxed in this film.

Table 3.2: The elements of the first batch of BST thin film samples tabulated in atomic concentration (at. %).

Element	Unannealed BST1 (at. %)	Annealed BST1 10 min (at. %)	Unannealed BST3 (at. %)	Annealed BST3 1 hr (at. %)
Ba3d	10.46	6.98	10.45	6.39
Sr3d	9.7	9.99	9.63	9.18
Ti2p	18.28	15.85	18.89	13.84
O1s	61.57	67.18	61.03	70.58
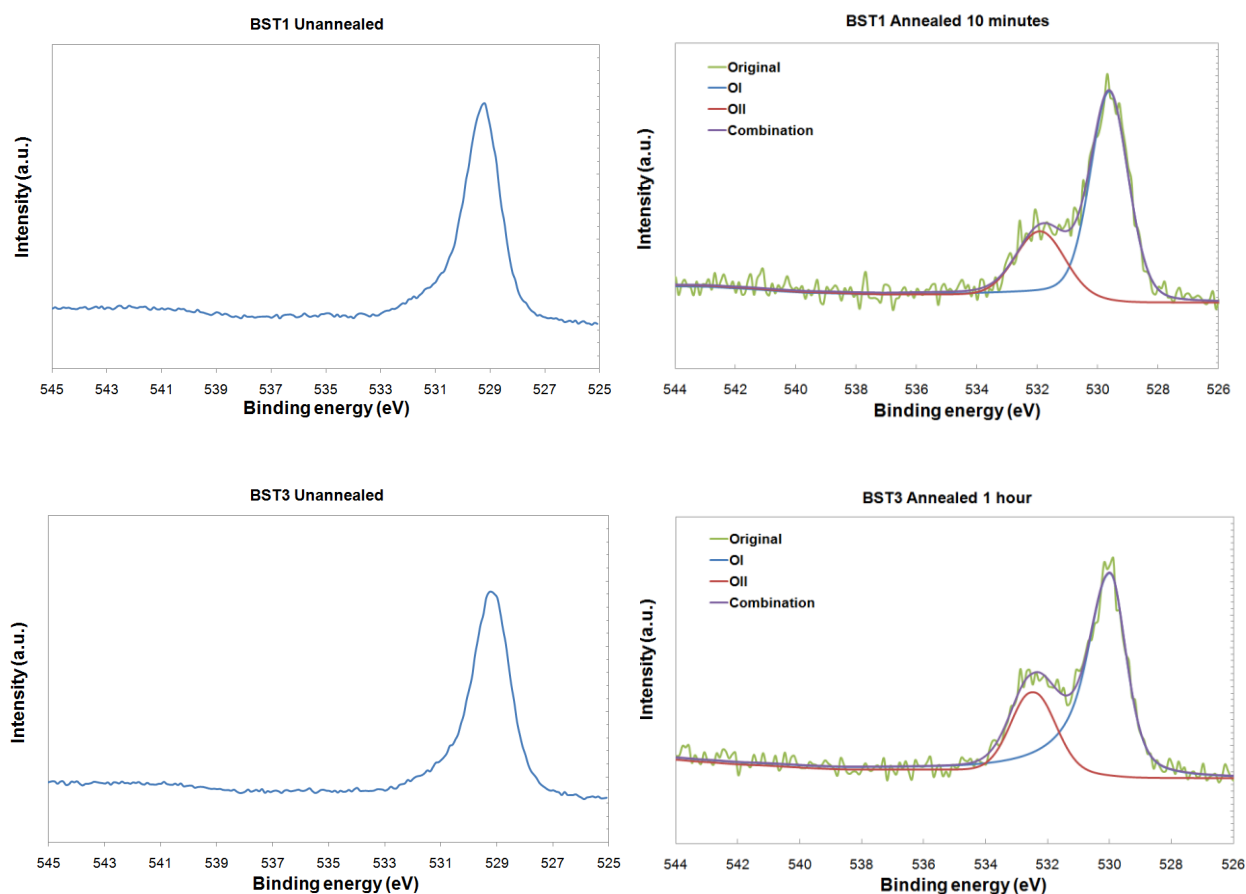
Figure 3.9: The O1s core level XPS spectra of the BST1 and BST3 samples before and after annealing at 700 ºC for 10 minutes and an hour respectively.

Table 3.3: The elements of the second batch of BST thin film samples tabulated in atomic concentration (at. %).

Element	Unannealed BST (at. %)	Annealed BST 2 hrs (at. %)
Ba3d	8.86	13.6
Sr3d	14.75	11.12
Ti2p	16.97	13.08
O1s	59.42	62.2

3.3.3 Scanning Electron Microscope (SEM)

SEM is a common technique to characterise micro/nanomaterials by providing information about the material's surface morphology, topography and composition. The surface of the material is scanned with an electron beam that interacts with the atoms of the material and emits secondary electrons which are detected and monitored. A schematic diagram of a SEM is depicted in Figure 3.10. The electron beam is emitted from a heated filament by applying an electrical potential and the electrons are accelerated towards the sample. The condenser lens focuses the electron beam and projects an image of the source onto the condenser aperture. The image is then focused by an objective lens and the sample is raster scanned by scanning coils. The secondary electrons are emitted as soon as the electron beam hits the sample and collected by the detector, which then converts them into voltage, amplifies and constructs an image. In order to avoid electric charging, the sample must be either conductive or coated with a thin metal layer.

The BST thin films were analysed using the *FEI NovaNano* SEM at the RMIT Microscopy & Microanalysis Facility (RMMF) (Figure 3.11). This equipment was utilised to determine the thickness of the BST thin films. A thickness of around ~400 nm was achieved in all samples as shown in the cross-section Figure 3.12. This thickness was expected for the sputtering conditions in Table 3.1. The surface of the BST thin film was very smooth, indicating high density of the film. Note that in the early work of producing the BST samples of ~200 nm thickness deposited for 4 hours with the other deposition conditions held constant as in Table 3.1, the film was measured using the *Ambios Technology XP-2 Surface Profiler*, confirming the thickness.
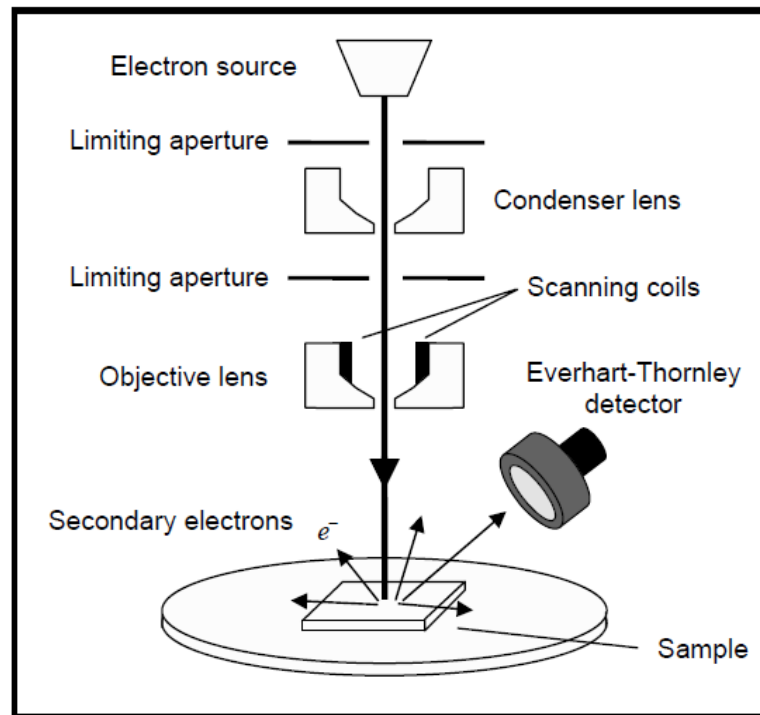
Figure 3.10: Schematic diagram of a SEM setup [143].
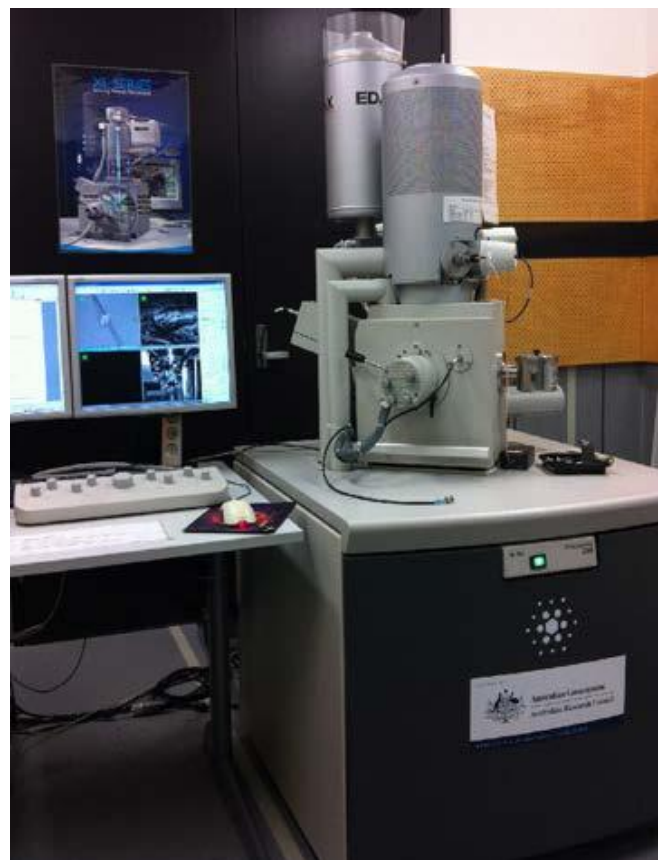
Figure 3.11: FEI NovaNano SEM.
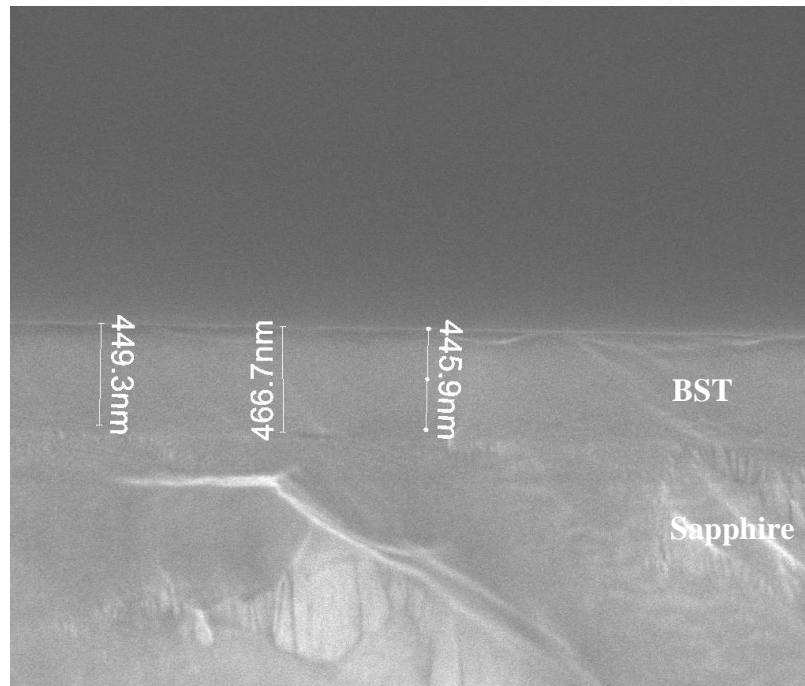
Figure 3.12: SEM image of the deposited BST layer on c-plane sapphire substrates.

3.4 Design of BST Interdigital Capacitors (IDCs)

One photomask plate, with several mask patterns, was used for the major parts of the IDCs fabrication process. It consisted of an array of IDCs pattern which were designed using Advanced Design System (ADS) 2009 software. An array of IDCs pattern with different sets of geometry in terms of the finger gap, finger length, finger width and numbers of fingers were designed as shown in Figure 3.13. The finger gap ranged from 2 to 8 μm and finger length from 90 to 130 μm. The finger width and number of fingers were fixed at 5 μm and 8 respectively. Open and short-circuit calibration standards patterns adjacent to the IDCs were also included. These were designed to de-embed the parasitic elements associated with the IDCs from the measured data and accurately determine the final capacitance and Q-factor values of the varactors [120, 142]. The IDCs were designed with two sets of electrodes to enable ground-signal-ground (GSG) configuration.

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The "seed layer mask" in Figure 3.13 was initially designed by the author's collaborator, Dr. Ernest A. Fardin who was also a former RMIT student. For this research, the mask had to be refined by adding up the necessary markers which were crucial in the alignment process stage. In order to fabricate the IDCs, a total of four masks were used. Figure 3.14 shows the design for the other three masks, "edge bead removal", "electroplating" and "seed layer removal". Each of the four masks was actually made to fit the 10 x 10 mm^2 diced sapphire substrate and designed on a single 4 x 4 in^2 soda lime mask. Another soda lime mask with an array of IDCs with fine geometries was also designed by the author for the fabricated varactors in Chapter 5.
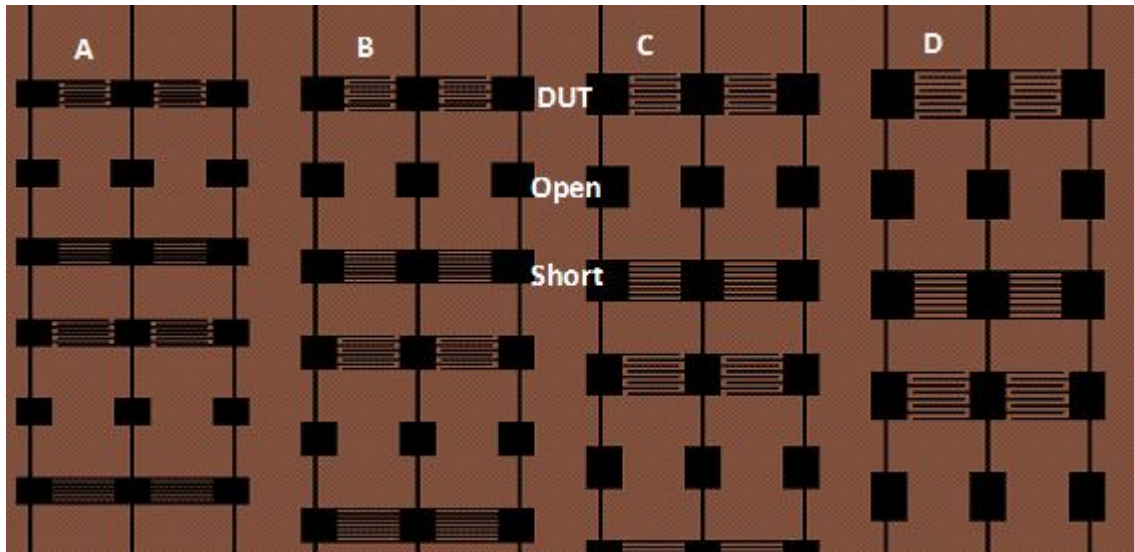
Figure 3.13: Design of an array of IDCs for the seed layer mask with adjacent open and short-calibration standards patterned on a 4 x 4 in^2 chrome soda lime mask. The IDC patterns were distinguished by the finger gap of A: 2 µm, B: 4 µm, C: 6 µm, and D: 8 µm. All the IDCs have finger lengths from 90 µm, 110 µm and 130 µm consecutively. The IDCs are electrically connected to one another in each column (A, B, C, and D) for the preparation of the electroplating process.

(a)

(b)

(c)
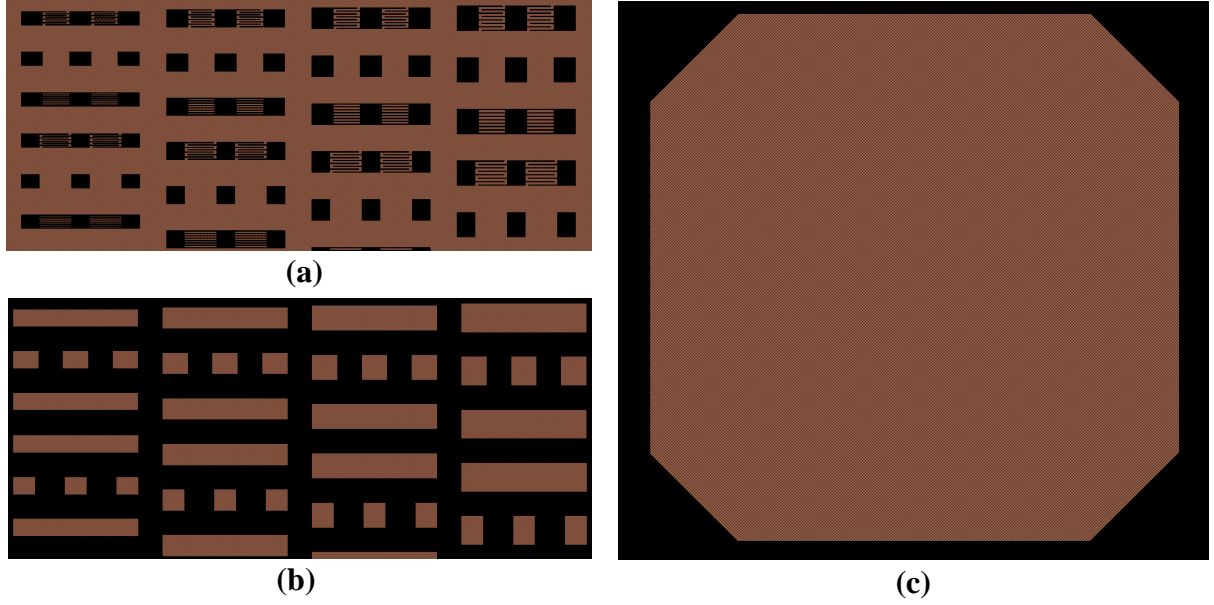
Figure 3.14: (a) Electroplating, (b) Seed layer removal and (c) Edge bead removal masks. The electroplating mask was designed for electroplating process. The seed layer removal mask was designed to remove the interconnect lines during etching process. The edge bead removal mask was designed to remove the "hillock" formation around the edges of the sample.

3.5 Fabrication of BST Interdigital Capacitors (IDCs)

As discussed in Chapter 2, there are two methods used to fabricate IDCs: (1) Lift-off and (2) Wet/Dry etching. For this research, the former method was used as it lowered the risk of damaging the BST layer during the fabrication process. The IDCs were fabricated on BST thin films which were epitaxially grown on 10 x 10 mm^2 c-plane sapphire substrates. The fabrication process was fully conducted in the class-100 clean room facility at the MMTC, RMIT University.

3.5.1 Sample preparation

A BST thin film grown on diced c-plane sapphire substrate was prepared by rinsing it thoroughly with acetone, IPA or methanol and DI water, and a nitrogen gun was used to blow-dry the sample. The sample was checked under a high magnification microscope to ensure all unwanted particles and residues were removed. Next, the sample was baked on a hotplate at 130 °C for 3 minutes to dehydrate it. The sample was then rested for 5 minutes to cool it to room temperature.

3.5.2 Photolithography

The photolithography or fabrication process of IDCs for this research was separated into three major stages. The first stage involved the electron-beam evaporation of the seed layer which consisted of composition metals of Ti/Ni/Au. The second stage involved electroplating defined region of the seed layer with Au. The final stage was to chemically wet etch the non-plated region of the seed layer.

3.5.2.1 First stage - Seed layer

First, hexamethyldisilazane (HMDS) was spun-coated on the sample using a spinner machine (*Karl Süss* RC8) with a spin speed of 3000 rpm and an acceleration of 300 rpm/s for 30 seconds. HMDS was used as an adhesion promoter between the photoresist and the substrate. Next, the photoresist AZ1512 was spun-coated on top of the thin HMDS layer at a similar spin speed. The sample was then baked at 95 °C for 2 minutes on a hotplate to allow the solvents to evaporate. Figure 3.15 (A) shows the cross-section of the profiled layer (utilising a profilometry) of ~1.5 μm thick AZ1512 on BST/sapphire.

For patterning the seed layer, the sample was exposed under an ultraviolet (UV) light of the mask aligner for 4 seconds as shown in Figure 3.15 (B). The "seed layer mask" as

described in Section 3.4 was used in the mask aligner (*Karl Süss* MA6). The sample was then immersed in a chlorobenzene solution for 1 minute to create undercuts of the photoresist for assisting the lift-off process. The sample was thoroughly rinsed in DI water and blow-dried with N_2. The sample was subsequently developed in an AZ400K 1:4 developer for 8 seconds (Figure 3.15 (C)) and the desired pattern was achieved as illustrated in Figure 3.15 (D) after the sample was being rinsed and blow-dried.

Note that prior to patterning the seed layer, an edge bead removal exposure for 4 seconds using an "edge bead removal mask" was performed to remove the "hillocks" formation by developing the sample in AZ400K 1:4 for 10 seconds. This mask is depicted in Figure 3.14 (c). The hillocks are part of the photoresist which tend to build up around the edges of the sample during spinning. Removing them ensures that there is a good contact between the mask and the photoresist during the pattern exposure. If the sample is the size of a standard wafer, the edge bead removal can be easily executed at the spinner machine immediately after spinning it with photoresist.

The metal composition of 10 nm Ti / 10 nm Ni / 50 nm Au were deposited on the sample using *Balzers* e-beam evaporator as depicted in Figure 3.15 (E). The sample was then submerged in a small beaker filled with sufficient acetone which was placed in an ultrasonic bath. The lift-off process was effected using the ultrasonic agitation for at least 5 minutes, simultaneously washing away the unwanted photoresist along with the metal layers on top of it. Eventually, the Ti/Ni/Au seed layer was obtained, as shown in Figure 3.15 (F), after the sample was being rinsed and blow-dried.
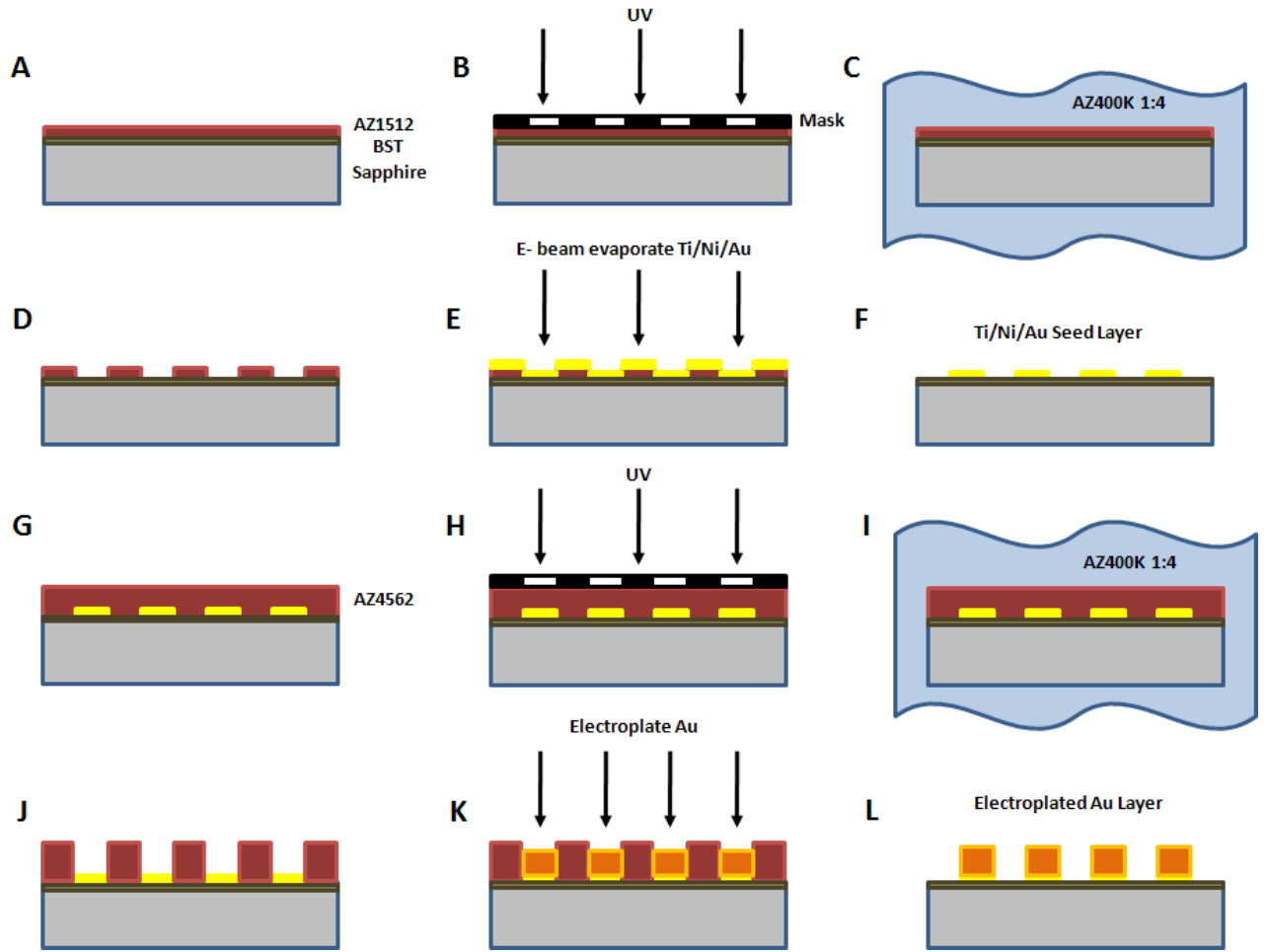
Figure 3.15: The cross-sections of the multistep fabrication process of BST interdigital capacitors on c-plane sapphire substrate.

3.5.2.2 Second stage - Electroplating

The next step was to spin-coat the HMDS followed by AZ4562 thick photoresist on top of the seed layer as shown in Figure 3.15 (G). The HMDS spin conditions remained the same as in the first stage. The closed-lid spin speed for AZ4562 was 6000 rpm with 2000 rpm/s acceleration for 30 seconds. The profiled thickness of ~3 µm for this photoresist was important to protect the non-plated seed layer region during the electroplating process. The sample was then rested for 15 minutes to allow most of the solvent to evaporate prior to softbaking it on a hotplate at 100 °C for 50 seconds. This resting time is important because

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otherwise the photoresist surface would dry quickly and the remaining trapped solvent may form bubbles, lifting the resist layer and eventually leading to adhesion failure. Edge bead removal exposure was then performed on the sample for 12 seconds and developed for 1 minute.

Next, the challenging part of this step was the alignment process. An "electroplating mask" was used with a similar pattern as the "seed layer mask" but without the interconnect lines connecting the IDCs pads as depicted in Figure 3.14 (a). This step was indeed crucial and careful alignment was needed. After properly aligning the mask pattern to the seed layer, the sample was exposed under UV light for 8 seconds and developed for 50 seconds as illustrated in Figure 3.15 (H) and (I) respectively. Eventually, the desired pattern was achieved in Figure 3.15 (J).

The electroplating process was conducted with the assistance of a licensed technical officer according to all cyanide handling procedures. Prior to this, the sample in Figure 3.15 (J) was post-baked at 115 °C for 50 seconds. Post-baking is recommended as this will ensure the hardening of the AZ4562 thick photoresist which could sustain the electroplating solution. The electroplating setup is shown in Figure 3.16. The top of the beaker with the plating solution was initially covered with plastic to avoid evaporation and the plating solution was heated to 40 °C. Electrical connections were then made and the diced sample was attached to the sample holder of the anode clamp assembly before submerging it in the solution. The current was set to the required value for electroplating the submerged seed layer pattern area, knowing the optimised current density of 3.4 mA/cm^2. During this process, it is important to ensure that no bubbles form on the surface of the sample. A ~2.7 µm Au layer was finally achieved for the duration of 10 minutes of electroplating as depicted in Figure 3.15 (K) and (L) after the standard cleaning and blow-drying of the sample.
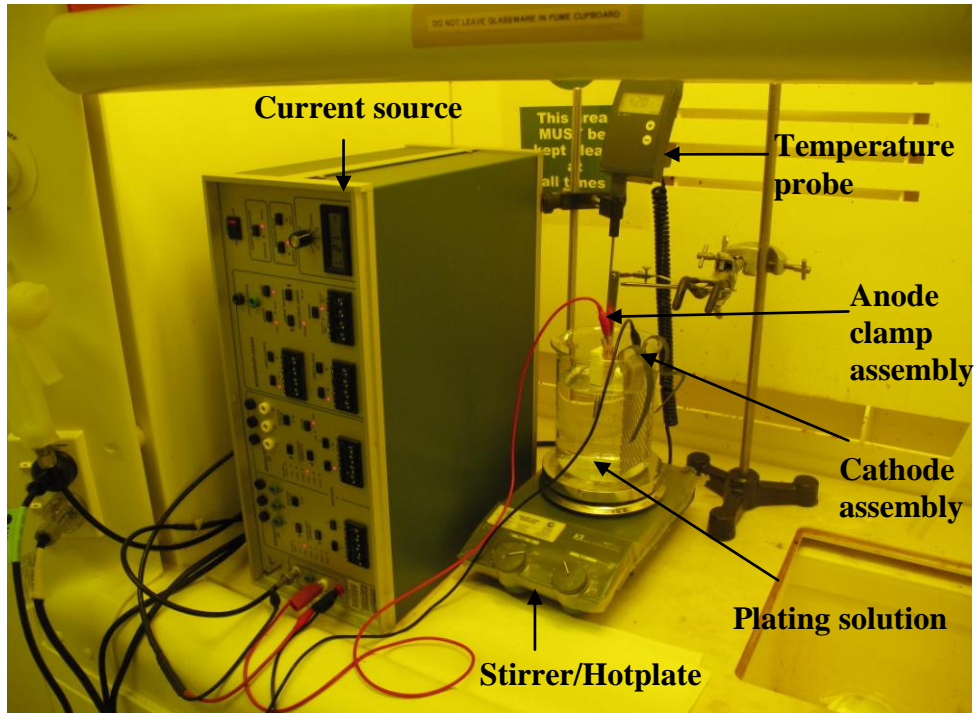
Figure 3.16: The electroplating process setup for electroplating the BST sample.

3.5.2.3 Final stage - Wet etching

The final stage of this photolithography process was to spin-coat the HMDS followed by AZ4562 on the electroplated Au layer. The HMDS spin conditions remained the same as in the first stage and, the closed-lid spin speed for AZ4562 was 6000 rpm with 1000 rpm/s acceleration for 5 seconds. The profiled thickness of ~4.5 μm for this photoresist was important to protect the plated Au region during wet etching as illustrated in Figure 3.17 (M). The sample was then rested for 15 minutes to allow most of the solvent to evaporate prior to softbaking it on a hotplate at 100 °C for 50 seconds. Edge bead pattern exposure was performed on the sample for 25 seconds and developed for 1 minute.

The "seed layer removal mask" was used with square-shaped patterns that protected the plated Au region as depicted in Figure 3.14 (b). After carefully aligning the squares to the

plated region, the sample was exposed under UV light for 25 seconds and developed for 40 seconds as illustrated in Figure 3.17 (N) and (O) respectively.

The sample in Figure 3.17 (P) was immersed in proper etchant solutions to etch the non-plated interconnect lines of metal layers, Ti/Ni/Au as shown in Figure 3.17 (Q). For etching the Au layer, a cyanide solution was used for 30 seconds. Ni-etchant and HF solutions were then used to etch Ni and Ti for 30 seconds and 15 seconds respectively. In this stage, it was crucial to etch the BST layer in the non-plated region entirely using HF solution to further reduce microwave losses [19]. Finally, the BST IDCs were produced as in Figure 3.17 (R). The top views of the before and after etching the interconnect lines are depicted in Figure 3.18. An example of the fabricated array of BST IDCs with fine geometries for the microwave applications in Chapter 5 is shown in Figure 3.19.
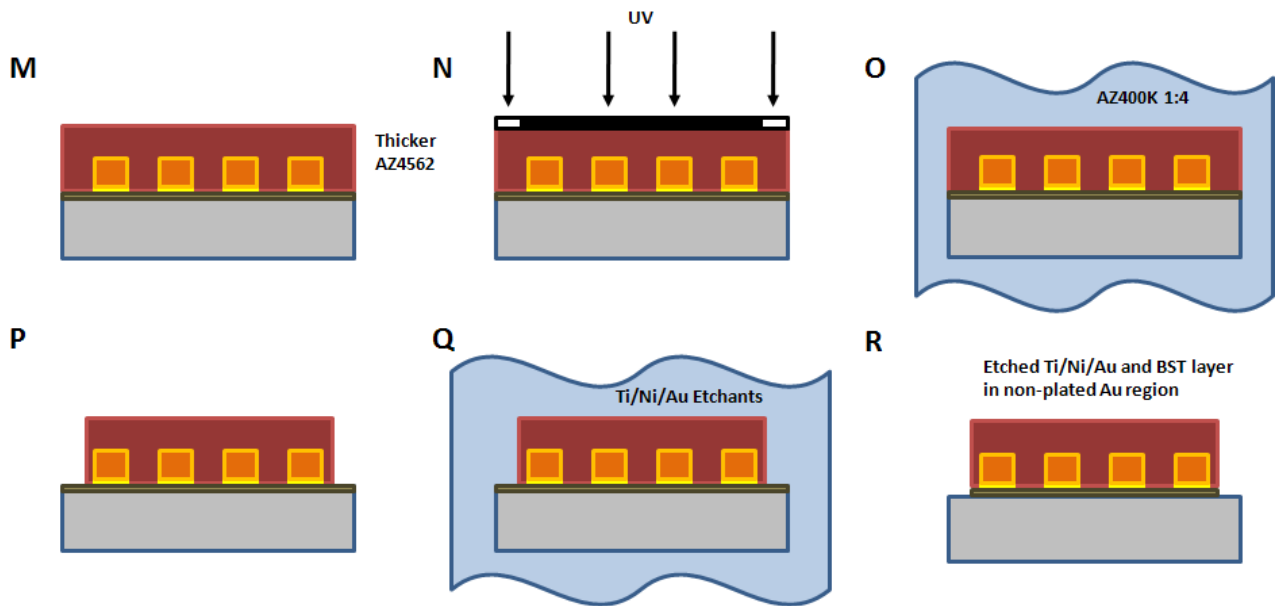
Figure 3.17: The continuation cross-sections of the multistep fabrication process of BST interdigital capacitors on c-plane sapphire substrate.
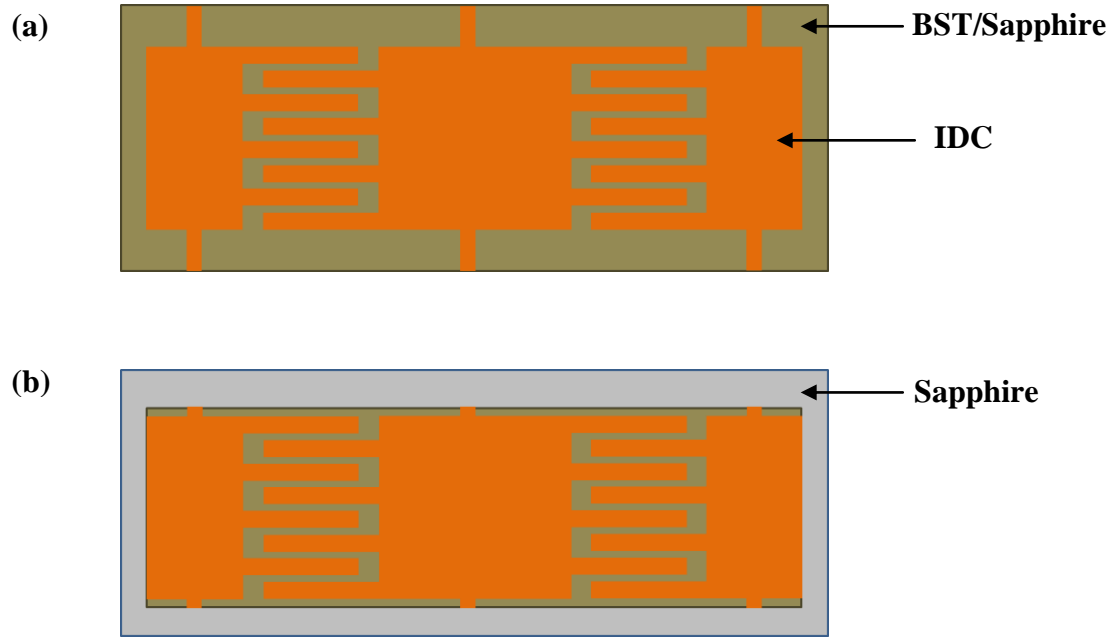
Figure 3.18: The top view of the BST interdigital capacitors on a c-plane sapphire substrate with a) non-plated interconnects and b) etched interconnects and BST layer in the non-plated region.
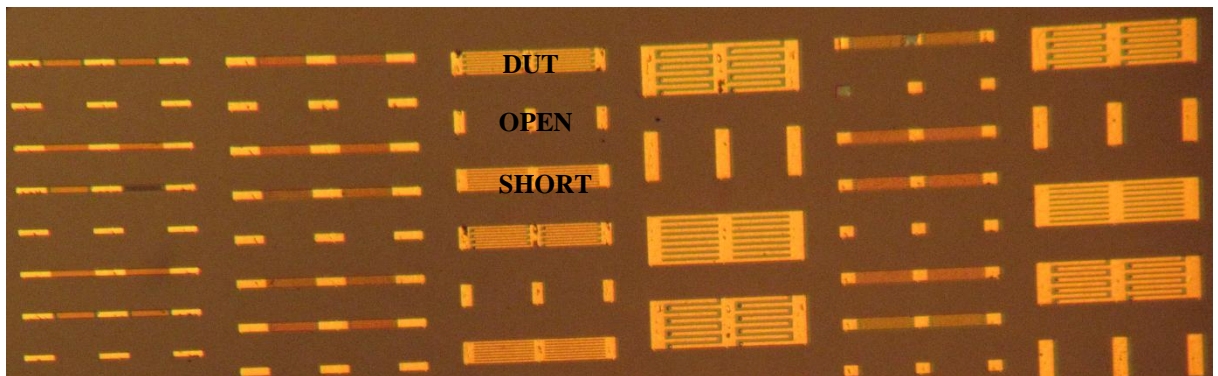
Figure 3.19: An array of the fabricated BST interdigital capacitors with adjacent open and short-circuit calibration standards. The varactors with fine geometries of 1 μm gap are indicated at the far left column.

3.6 Microwave Characterisation of BST Varactors

Microwave characterisations of the BST IDCs were performed on a probe station connected to the Vector Network Analyser (VNA) as shown in Figure 3.20. A video imaging system which consists of a camera (*Panasonic*), microscope, light source and a monitor is used to view the image of the sample for manual adjustments. The microwave probes (*GGB Industries*) were initially mounted on the micropositioners (*Newport ULTRAlign*) and tightened with screws. Before calibrating the VNA, an Au electroplated dummy sample was placed on the mounting stage and the three probe tips (GSG probe) were carefully levelled down to slowly touch the surface of the electroplated Au. The 'roll' adjustment was utilised to achieve equal impression for all the three probe tips on the Au sample.
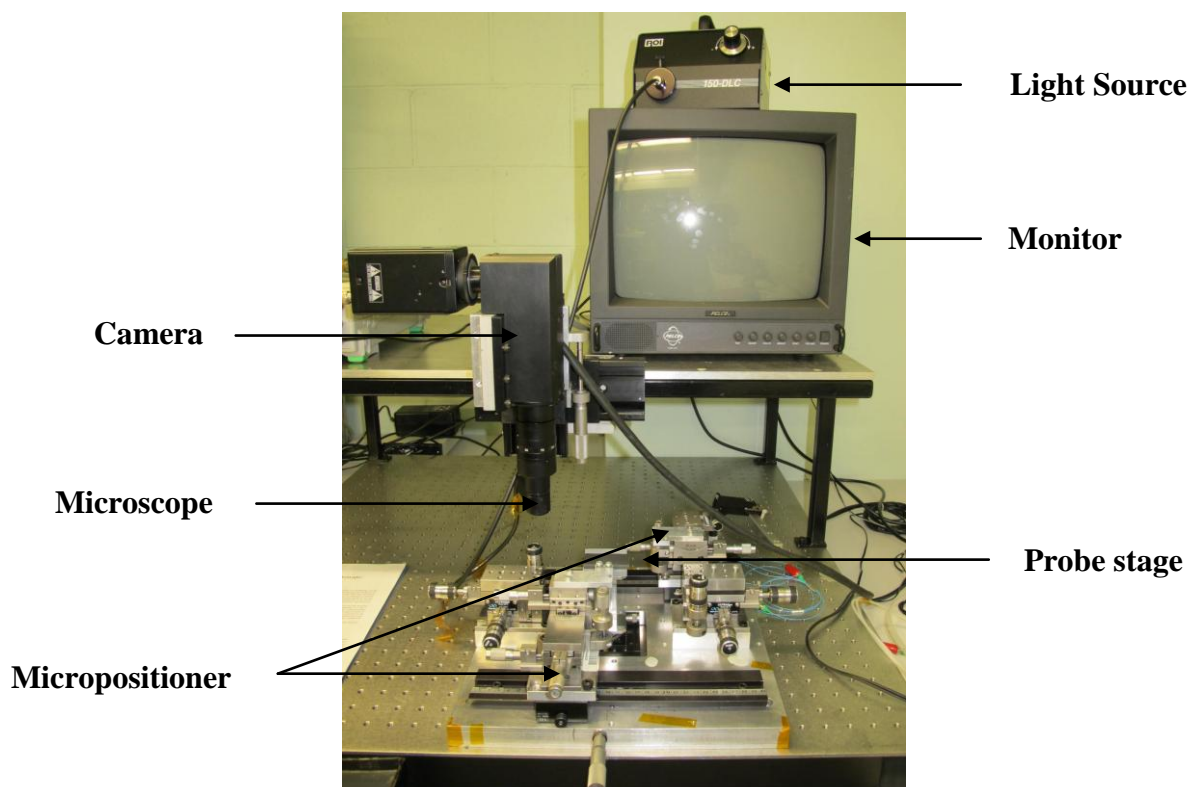
Figure 3.20: The probe station for the microwave characterisation of BST varactors.

Once the probe tips were levelled, calibration of the VNA was performed using a CS-5 calibration substrate (*GGB Industries*) for the 200 μm pitch probes. Open, short and 50 Ω matched calibration standards were used and a SOLT calibration technique was performed in the frequency range from 1 to 20 GHz. The S-parameter results were achieved as expected for this type of calibration technique. The BST IDCs were then measured and the S_{11} data were recorded and stored in data storage. The biasing was performed by connecting a power supply externally to the VNA, which is limited up to ±40 V.

As described in Section 3.4, the purpose of the open and short-circuit calibration standards patterned adjacent to the IDCs was to de-embed the parasitic elements related to the interdigital electrodes from the measured data. The fabricated calibration standards can be observed in Figure 3.19. Microwave measurements of the BST IDCs can be performed more accurately by taking into account all these parasitic elements [120, 142, 147]. Further, a significant variation in the extracted capacitance from 1 to 20 GHz is produced if the parasitic elements were not modelled [142]. The equivalent circuit BST varactor model is depicted in Figure 3.21 including the parasitic elements (C_p , L_p and R_p) related to the contact pads. The first step was to measure the S_{11} parameter of the open-circuit calibration standard, which is a device structure that omits the device under test (DUT), leaving the pads open. The short-circuit calibration standard is a device structure that omits the DUT and short-circuited the signal and ground planes and then S_{11} was measured. Finally, the measured S_{11} values for all elements in the model were substituted in a MATLAB algorithm (Appendix A) for computing the final capacitance and Q-factor values.

The measured results of the thin film BST varactors are tabulated in Table 3.4. From the SEM analysis in Subsection 3.3.3, the thickness for all of the BST thin films was ~400 nm. The early batch indicates the very first attempt to fabricate varactors on such thickness. All of the measured BST varactors had a 2 μm finger gap except for the second batch which was 1 μm finger gap varactors. The second batch varactors were produced using the new mask with
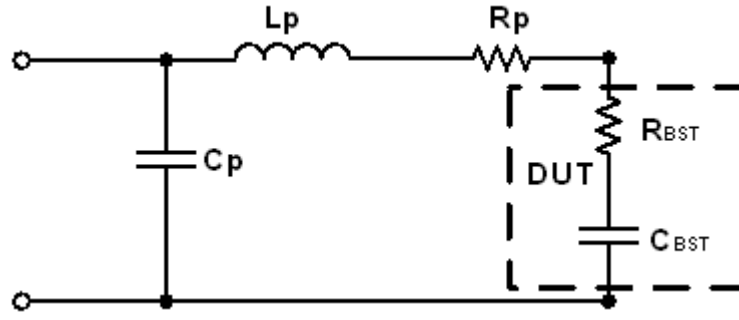
Figure 3.21: The equivalent BST thin film varactor circuit model including the parasitic elements.

Table 3.4: The performance of BST thin film varactors between unannealed and annealed samples measured at 10 GHz.

Parameter	BST early batch		First Batch				Second Batch	
			BST1		BST3		BST	
	Unannealed		Annealed 10 minutes in vacuum oven		Annealed 1 hour in vacuum oven		Annealed 2 hours in air	
	0 V	40 V	0 V	40 V	0 V	40 V	0 V	40 V
Capacitance (pF)	0.8406	0.6854	0.5353	0.4367	0.8827	0.7161	1.4805	0.7365
Q-factor	Invalid	Invalid	16.4	26.15	22	32.6	8.74	20.8
Tunability (%)	18.46		18.42		18.87		50.25	

fine geometries. As observed, the early batch varactors experienced large fluctuations in their Q-factor values which were caused by significant microwave losses. Consequently, the values were invalid. The non-etching of the remaining BST layer in the non-plated Au region was identified as the main cause as highlighted in Subsection 3.5.2.3.

No significant change was observed in the tunability of the early batch of varactors compared to the first batch of annealed varactors, indicating that annealing samples in a vacuum oven for this case did not improve the crystallinity of the BST films. This was well in agreement with the XRD and XPS data where the presence of oxygen vacancies as charge defects induced strain in the films, leading to the degradation or no improvement in the tunability of the BST varactors.

However, when annealed in air, the tunability improved significantly although the gap was reduced to 1 μm for the microwave applications - presented in Chapter 5. This indicated an improved crystallinity due to the increased grain size and significantly reduced strain in the film, well in agreement with the XRD and XPS data. Based on Table 2.1 in Chapter 2, BST tunability of at least 50 % with Q-factor of minimum 20 can readily compete with the other established silicon and MEMS technologies, and this was achieved with the second batch BST varactors.

Figure 3.22 shows the capacitance and Q-factor values for the second batch of BST varactors in the frequency range from 1 to 20 GHz. Fewer variations in the capacitance values were observed throughout the entire frequency range which was expected by taking into account all the parasitic elements. However, in the lower frequencies of less than 5 GHz, a large dispersion of the Q-factor values occurred due to the slightly reduced thickness of the electroplated electrodes, which contributed to conductor losses. At 10 GHz, the varactors achieved ~50 % tunability and Q_{min} of ~ 9 as plotted in Figure 3.23.
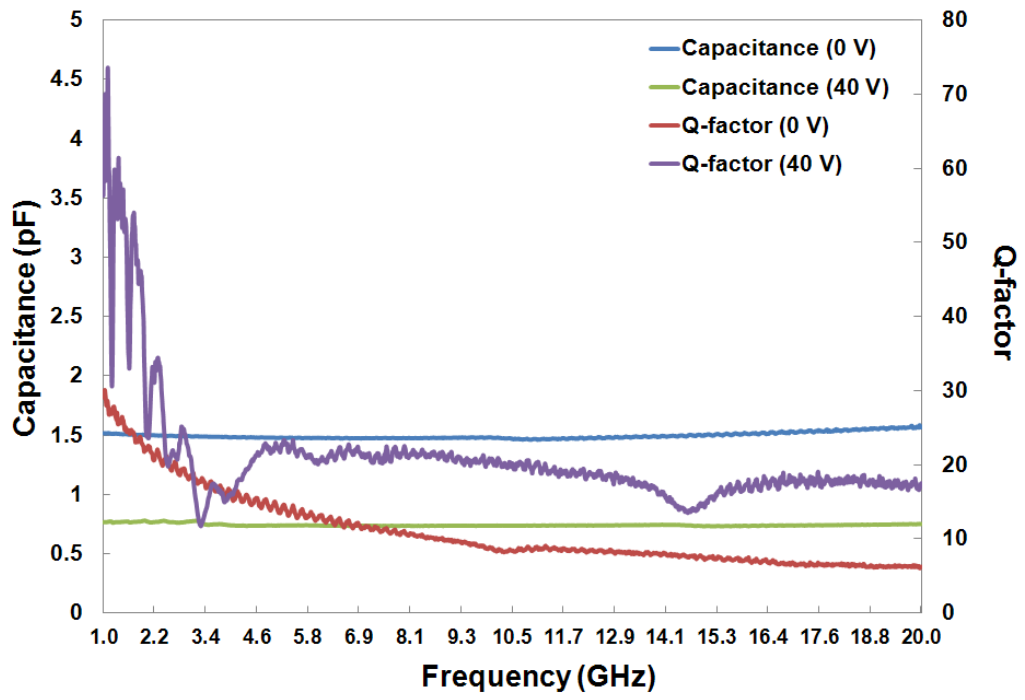
Figure 3.22: The extracted capacitance and Q-factor values of the second batch of BST thin

film varactors for a broad frequency range from 1 to 20 GHz.
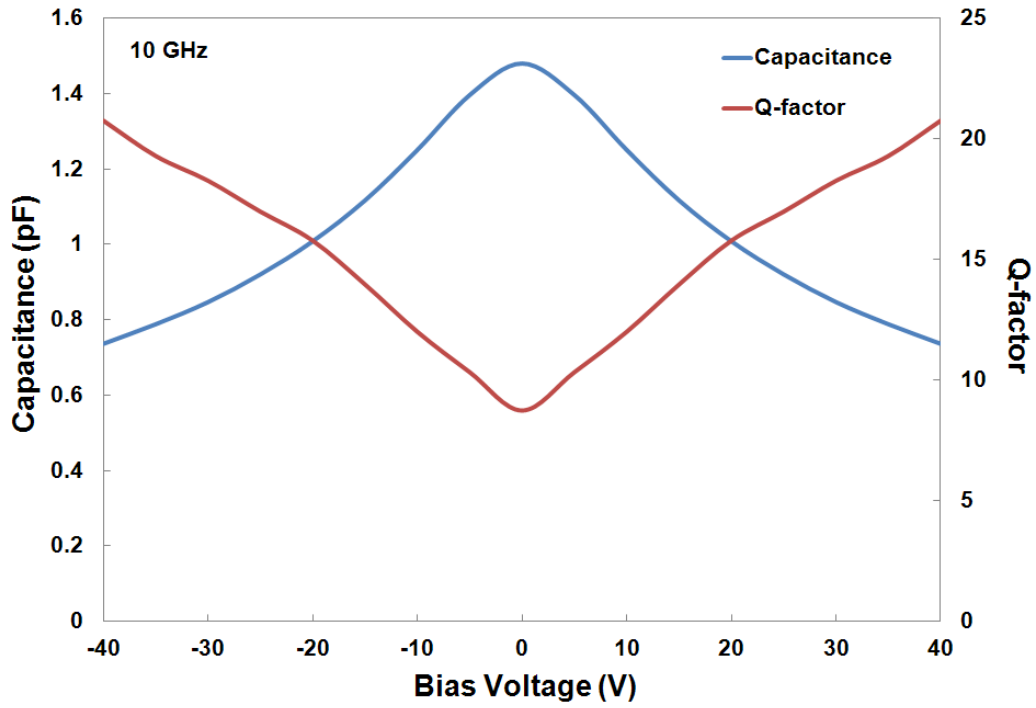
Figure 3.23: The extracted capacitance and Q-factor values of the second batch of BST thin

film varactors at 10 GHz.

3.7 Conclusions

This chapter has presented the material deposition and characterisation of the sputtered BST thin films used in this research. A BST thickness of ~400 nm was consistently achieved with the sputtering conditions held constant for every deposition run. XRD analysis for all samples revealed peaks which corresponded to the cubic perovskite BST phase with no indication of secondary phase formation. Post-annealing in vacuum oven and air were employed and crystal phases and chemical compositions of the BST thin films were investigated.

It was found that the BST samples annealed in the vacuum oven experienced a loss of crystallinity, which suggested the presence of oxygen vacancies in the films. XPS results were also in agreement with the XRD data that showed an increase of atomic concentration of the O elements and the loss of atomic concentration of the Ba and Ti elements in the chemical composition of BST. However, the BST sample annealed in air using a conventional tube furnace experienced an increase of atomic concentrations in both the O and the Ba elements. It was suggested that improved crystallinity in the film had occurred due to the incorporation of oxygen in the film. The A-to-B site ratio also suggested the poor film quality of the annealed samples in vacuum oven.

BST interdigital capacitors were fabricated on both annealed and unannealed samples and microwave measurements were performed. The final capacitance and Q-factor values were extracted from a MATLAB algorithm by taking into account all the parasitic elements associated with the interdigital electrodes using the equivalent BST thin film varactor circuit model. The annealed samples in the vacuum oven revealed no significant change compared to the unannealed samples, with tunability of ~18 %. However, tunability of ~50 % was achieved in the sample annealed in air. This indicated that strain-induced films due to the presence of oxygen vacancies affected the performance of the BST thin film varactors.

In the next chapter, the third-order intermodulation distortion in BST thin film varactors is investigated. A novel theoretical method for this analysis was developed and two BST varactor circuit topologies were simulated and measured for validation. As mentioned earlier, the BST thin films used were deposited on r-plane sapphire substrates which would have the potential to be integrated with silicon technology.

Chapter 4

Low Third-Order Intermodulation Distortion in Ba$_{0.6}$Sr$_{0.4}$TiO$_3$ Thin Film Interdigital Capacitors

4.1 Introduction

As described in Chapter 2, barium strontium titanate (BST) thin film varactors have found many applications in frequency agile microwave devices mainly due to their performance in the frequency region above 10 GHz. In this frequency region, which is known as the "varactor gap" region, BST varactors have significantly higher tuning speed, Q-factor and power handling compared to well-established silicon varactor technology [2]. Also, the high dielectric permittivity contributes to the size reduction of the microwave components and

compact, small-scaled microwave devices can be realised.

Integration of BST with the existing semiconductor technologies has long been of interest and silicon-on-sapphire (SoS) technology presents one of the possible solutions due to its many advantages. One of the main advantages over traditional bulk silicon integrated circuits is the high isolation between devices. This offers lower power dissipation, higher operating speed and minimum parasitic semiconductor junctions due to the highly effective insulating sapphire substrate. This technology uses a very thin layer of silicon deposited on an r-plane sapphire substrate, which provides a suitable orientation for the growth of silicon [148]. By depositing the BST film early in the SoS process, the high deposition temperature can be tolerated without affecting the silicon epilayer [9]. Some frequency agile microwave devices with the potential to be incorporated in this technology have been developed with epitaxial BST thin films on r-plane sapphire substrates at 10 GHz and above, such as interdigital capacitors (IDCs) [9], bandpass filters [66] and phase shifters [12].

Intermodulation distortion in nonlinear semiconductor and BST varactors is another issue that has gained interest over the past few years. Meyer *et al.* had previously analysed the intermodulation distortion in varactor diodes using the Volterra series approach in which closed-form expressions for intermodulation distortion in parallel- and series-tuned circuits were successfully derived. Anti-parallel and back-to-back circuit topologies were introduced and experimentally verified for achieving minimum distortions [133]. Since then, several research groups have demonstrated the effectiveness of implementing this idea in BST, MEMS and varactor diode technologies to enhance linearity of the devices [19, 134, 149, 150]. A linearity improvement technique based on BST-stacked parallel-plate capacitors has been analysed by connecting several capacitors in series, which reduced the RF swing across each capacitor [19, 151]. RF MEMS varactors in antibiased topology showed enhanced linearity and reduced bias noise [149]. Anti-series and anti-series/anti-parallel varactor diode

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topologies were presented in [134], in which the doping profile and area ratio parameters influenced the design to achieve minimum distortion.

In this chapter, a novel method for the theoretical analysis of the IM_3 in BST thin film IDCs on r-plane sapphire substrates is presented. Two circuit topologies - the "dual" and "series dual" BST varactor circuits - are proposed and their theoretical models along with simulated and measured results are presented. Low IM_3 is demonstrated and experimentally verified. By proper selective biasing, very low nulls are observed in both dual and series dual BST varactor circuit topologies which indicate minimum distortion. The measured first nulls are achieved at ± 13 V and ± 20 V for the dual and series dual topologies respectively. These results demonstrate the potential for incorporating these highly linear BST varactors in SoS applications.

4.2 BST Interdigital Capacitor Fabrication

In this work, IDCs were fabricated on 50 nm thick $Ba_{0.6}Sr_{0.4}TiO_3$ thin films grown on 10 x 10 mm^2 diced *r*-plane sapphire substrates. The BST thin films were initially deposited on the 500 µm thick sapphire substrates by pulsed laser deposition (PLD). The details of the BST thin film deposition and material characterisation can be found in [9, 142].

The fabrication of IDCs was realised in a multistep process described in Chapter 3. First, a seed layer composition of Ti/Ni/Au was deposited using e-beam evaporation. Next, the IDCs with adjacent open and short-circuit calibration standard patterns were achieved by lift-off. A 2.5 µm Au layer was then electroplated within a defined plated seed layer region. Finally, the non-plated seed layer region was removed by chemical wet etching. The purpose of the open and short-circuit calibration standards patterned adjacent to the IDCs was to de-embed the
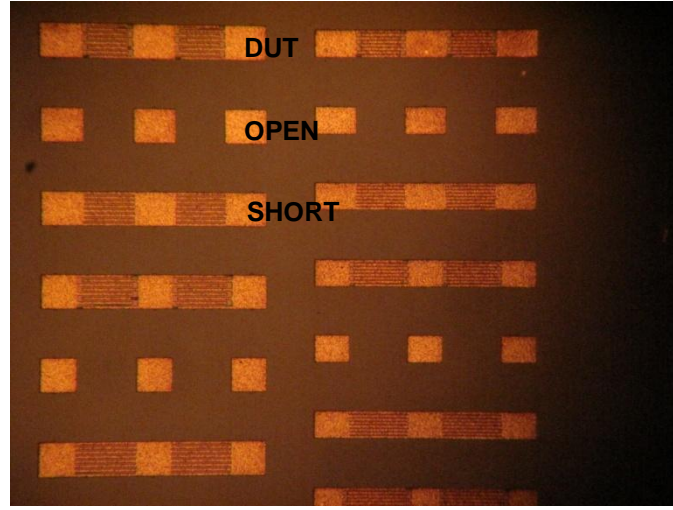
Figure 4.1: An array of the fabricated BST interdigital capacitors with adjacent open and short-circuit calibration standards on a 10 x 10 mm^2 diced r-plane sapphire substrate.

parasitic elements related to the interdigital electrodes from the measured data to accurately determine the final capacitance and Q-factor values of the varactors [6, 120].

An array of IDCs with different sets of geometry in terms of the finger gap, finger length, fingerwidth and number of fingers was realised. The finger gap ranged from 2 to 8 μm and finger length from 90 to 130 μm. The finger width and number of fingers were fixed at 5 μm and 8 respectively. The IDCs were designed with two sets of electrodes to enable ground-signal-ground (GSG) configuration. The IDCs are shown in Figure 4.1.

The BST varactors were selected based on the measured performances in which they had reasonably good tunability of ~43 % and Q-factor values in the range of ~13.4 to 78.3 from 0 to 40 V at 10 GHz. Note that the highest tunability of 64 % was recorded with the 200 nm BST films but compensated by the lowest Q-factor in the range of ~7.8 to 32.2 [9]. The reduction in the tunability of the measured 50 nm BST film was caused by the tensile strain. However, the permittivity remained quite high, ~800 at 0 V. The capacitance and Q-factor

values were computed using an RC equivalent circuit model, taking into account all the parasitic elements associated with the pad metallization [120, 142].

4.3 Theoretical Analyses and Simulations

4.3.1 Theoretical Analysis of Dual BST Varactor Circuit Topology

In order to analyse the nonlinear behaviour of the BST varactor, a curve fitting method is initially applied to the measured nonlinear capacitance-voltage (*C-V*) data of a BST thin film interdigital capacitor on r-plane sapphire substrate. Consequently, a 16th degree polynomial equation which perfectly fit the measured data is given by

$$C(V) = K_0 + K_2(V_{dc} + v)^2 + K_4(V_{dc} + v)^4 + ... + K_{16}(V_{dc} + v)^{16} \tag{1}$$

where K_o, K_2 … K_{16} are the coefficients of the polynomial and V is the sum of bias voltage, V_{dc} and RF voltage, v. Since a BST varactor has a symmetrical *C-V* curve [132], the odd-order terms ($K_1(V_{dc} + v)$, $K_3(V_{dc} + v)^3$, $K_5(V_{dc} + v)^5$, …..) in (1) are neglected. The expression in (1) is further verified by providing an excellent agreement to the nonlinear *C-V* BST varactor model proposed in [132], where the fringing capacitance, C_f is taken into account. The comparison between the polynomial equation in (1) and the measured data is shown in Figure 4.2 and the polynomial coefficients in Table 4.1.

Generally, the capacitance of a varactor is expanded by a power series as a function of the incremental voltage v and can be expressed as

$$C(v) = C_0 + C_1 v + C_2 v^2 + ... \tag{2}$$

The polynomial expression in (1) is then converted into the form of (2) and the value of each coefficient (C_0, C_1 and C_2) is extracted with respect to its incremental voltage, v. These coefficients are subsequently substituted into the well-established closed-form IM$_3$ expression

of a varactor diode [133], where it is found that this expression is also ideal for the analysis of

a BST varactor.
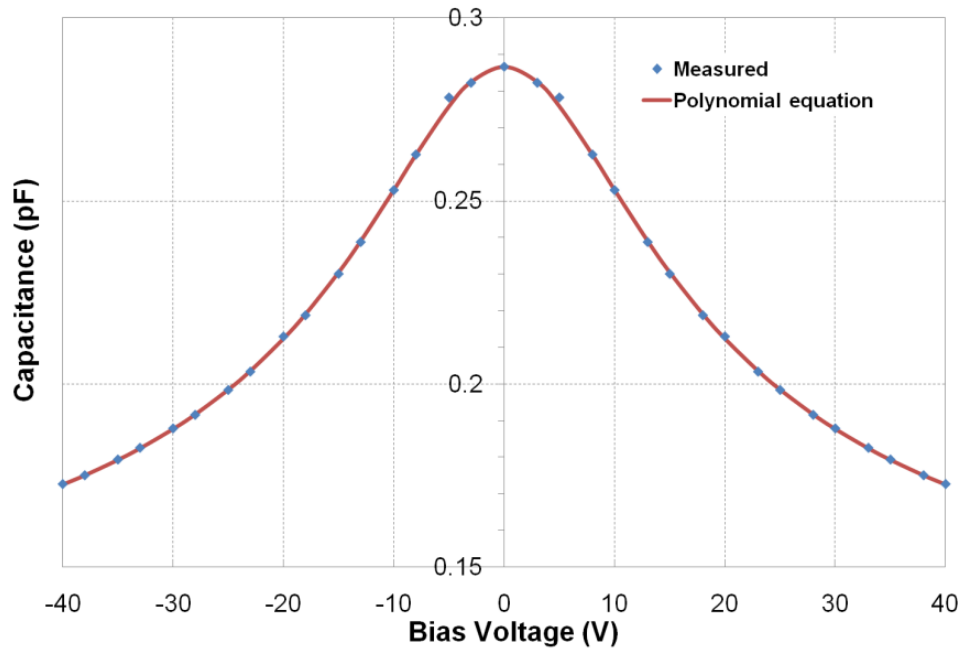
Figure 4.2: Polynomial expression in comparison with the measured data of the interdigital

BST capacitor.

Table 4.1: Polynomial coefficients and their corresponding capacitance values.

Coefficient	Capacitance Value (pF)
K_0	0.2867
K_2	-4.59806×10^{-4}
K_4	1.56378×10^{-6}
K_6	-3.9907×10^{-9}
K_8	6.67387×10^{-12}
K_{10}	-6.98047×10^{-15}
K_{12}	4.37173×10^{-18}
K_{14}	-1.49413×10^{-21}
K_{16}	2.13837×10^{-25}

IM$_3$ is defined as the ratio of the magnitude of the third-order distortion component to the fundamental signal. Recently, this IM$_3$ expression has been slightly modified from [133] to perfectly fit the simulated data and is given by

$$IM_3 = \frac{3}{8}V_o^2 \frac{|A_3(j\omega_1, j\omega_1, -j\omega_2)|}{|A_1(j\omega_1)|^2 |A_1(j\omega_2)|} \tag{3}$$

where V_o is the peak value of each fundamental output voltage and, $A_1(j\omega_1)$ or $A_1(j\omega_2)$ and $A_3(j\omega_1, j\omega_1, -j\omega_2)$ are the first-order and third-order Volterra coefficients. These Volterra coefficients are derived as

$$A_1(j\omega) = \frac{1}{\frac{1}{R} + j\omega C_0} \tag{4}$$

$$A_3(j\omega_1, j\omega_1, -j\omega_2) = -\frac{(2j\omega_1 - j\omega_2)\left[C_1\hat{A} + \frac{C_2}{3}A_1(j\omega_1)^2 A_1(-j\omega_2)\right]}{\frac{1}{R} + (2j\omega_1 - j\omega_2)C_0} \tag{5}$$

where

$$\hat{A} = \frac{1}{3}\left[2A_1(j\omega_1)A_2(j\omega_1, -j\omega_2) + A_1(-j\omega_2)A_2(j\omega_1, j\omega_1)\right] \tag{6}$$

and the second-order Volterra coefficient, $A_2(j\omega_1, -j\omega_2)$ or $A_2(j\omega_1, j\omega_1)$ is derived as

$$A_2(j\omega_a, j\omega_b) = -\frac{\frac{C_1}{2}(j\omega_a + j\omega_b)A_1(j\omega_a)A_1(j\omega_b)}{\frac{1}{R} + (j\omega_a + j\omega_b)C_0} \tag{7}$$

The simplifications in the above equations are a slight modification in (3) for redefining the IM$_3$ in terms of the average output power, P_{av} to match the simulated data. Also, the exclusion of the inductance, L as observed in (4) to (7) from the original equations in [133] are needed to implement the two circuit topologies proposed: the "dual" and "series dual" BST varactor circuits. The ideal single BST varactor circuit topology is illustrated in Figure 4.3 and its coefficients are tabulated in Table 4.2.

Figure 4.3: Ideal schematic of the single BST varactor circuit topology.

Table 4.2: Coefficients of ideal single BST varactor circuit topology.

Coefficient	Polynomial Expression
C_0	$K_0 + K_2(V_{dc})^2 + K_4(V_{dc})^4 + K_6(V_{dc})^6 + K_8(V_{dc})^8 + K_{10}(V_{dc})^{10} + K_{12}(V_{dc})^{12} + K_{14}(V_{dc})^{14} + K_{16}(V_{dc})^{16}$
C_1	$2K_2(V_{dc}) + 4K_4(V_{dc})^3 + 6K_6(V_{dc})^5 + 8K_8(V_{dc})^7 + 10K_{10}(V_{dc})^9 + 12K_{12}(V_{dc})^{11} + 14K_{14}(V_{dc})^{13} + 16K_{16}(V_{dc})^{15}$
C_2	$K_2 + 6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6 + 45K_{10}(V_{dc})^8 + 66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12} + 120K_{16}(V_{dc})^{14}$

In an ideal case, the values of the second- and third-order coefficients, C_1 and C_2 in (5) should be zero in order to eliminate the IM_3 in (3). In reality, this is difficult to achieve especially when dealing with the nonlinear behaviour of BST and the fabrication tolerances must be considered. However, by implementing the dual and series dual BST varactor circuit topologies, the IM_3 for each topology can be significantly reduced.

In order to reduce the second-order coefficient, C_1, the ideal dual BST varactor circuit topology is introduced as shown in Figure 4.4. The concept of this topology is to integrate two identical BST varactors in a parallel mode with opposite bias voltages applied (anti-parallel topology). Since the nonlinear C-V curve of the BST is symmetrical, either varactor can be forward or reverse biased, yielding the term "dual" topology. The DC blocking capacitor decoupled the varactors for individual biasing. Theoretically, by applying opposite bias voltages, the nonlinearity of one varactor will cancel the other and this will lead to the perfect cancellation of C_1.

The ideal dual BST varactor circuit topology coefficients in Table 4.3 have subscripts "left" and "right" indicating the position of the varactors in the topology and the capacitance of each is half of the single varactor for comparison. Also, the negative voltage, $-V_{dc}$ is applied to the right varactor. Here, it can be observed that C_1 is perfectly cancelled out due to the sum of C_{1left} and C_{1right}. The sums of "left" and "right" of similar coefficients are then substituted into (3) to (7) to compute the IM_3.

MAPLE and ADS software were utilised to compute the IM_3 equations and simulate the dual topology respectively. The MAPLE code for this procedure can be found in Appendix B. Two – tone signals, 1.80 GHz and 1.81 GHz were used. Here, the measured BST varactors with capacitance values of ~0.3 pF at 0 V were defined and the varactors were swept from -40 V to 40 V.
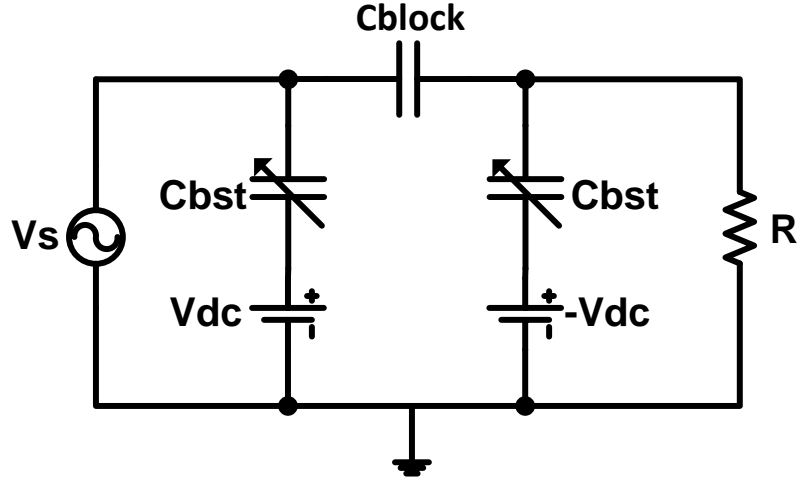
Figure 4.4: Ideal schematic of the dual BST varactor circuit topology.

Table 4.3: Coefficients of ideal dual BST varactor circuit topology.

Coefficient	Polynomial expression
C_{0left}	$[K_0 + K_2(V_{dc})^2 + K_4(V_{dc})^4 + K_6(V_{dc})^6 + K_8(V_{dc})^8 + K_{10}(V_{dc})^{10} + K_{12}(V_{dc})^{12} + K_{14}(V_{dc})^{14} + K_{16}(V_{dc})^{16}] / 2$
C_{0right}	$[K_0 + K_2(-V_{dc})^2 + K_4(-V_{dc})^4 + K_6(-V_{dc})^6 + K_8(-V_{dc})^8 + K_{10}(-V_{dc})^{10} + K_{12}(-V_{dc})^{12} + K_{14}(-V_{dc})^{14} + K_{16}(-V_{dc})^{16}] / 2$
C_{1left}	$[2K_2(V_{dc}) + 4K_4(V_{dc})^3 + 6K_6(V_{dc})^5 + 8K_8(V_{dc})^7 + 10K_{10}(V_{dc})^9 + 12K_{12}(V_{dc})^{11} +14K_{14}(V_{dc})^{13} + 16K_{16}(V_{dc})^{15}] / 2$
C_{1right}	$[2K_2(-V_{dc}) + 4K_4(-V_{dc})^3 + 6K_6(-V_{dc})^5 + 8K_8(-V_{dc})^7 + 10K_{10}(-V_{dc})^9 + 12K_{12}(-V_{dc})^{11} +14K_{14}(-V_{dc})^{13} + 16K_{16}(-V_{dc})^{15}] / 2$
C_{2left}	$[K_2 + 6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6 + 45K_{10}(V_{dc})^8 + 66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12} + 120K_{16}(V_{dc})^{14}] / 2$
C_{2right}	$[K_2 + 6K_4(-V_{dc})^2 + 15K_6(-V_{dc})^4 + 28K_8 (-V_{dc})^6 + 45K_{10}(-V_{dc})^8 + 66K_{12}(-V_{dc})^{10} + 91K_{14}(-V_{dc})^{12} +120K_{16}(-V_{dc})^{14}] / 2$

The IM$_3$ theoretical model and simulated results show excellent agreement. For the dual topology in Figure 4.5, it can be observed that the nulls are lower compared to the single topology at specific bias voltages, indicating minimum C_1. The first null can be achieved at ±9 V with an average of 10 dB linearity improvement. The second null can be observed at ±36 V with 13 dB linearity improvement. Hence, by proper tuning at a low voltage of ±9 V, a significantly low theoretical IM$_3$ can be achieved.

For further theoretical analysis, Figure 4.6 depicts an ideal case with matched varactors. As C_1 of the single topology increases, the corresponding C_1 of the dual topology maintains zero when biased from 0 to 10 V. This contribution of C_1 clearly degrades the IM$_3$ level of the single compared to the dual topology where the null occurs at 9 V.

In the next section, with the introduction of a new topology, an improved IM$_3$ is expected over all bias voltages.
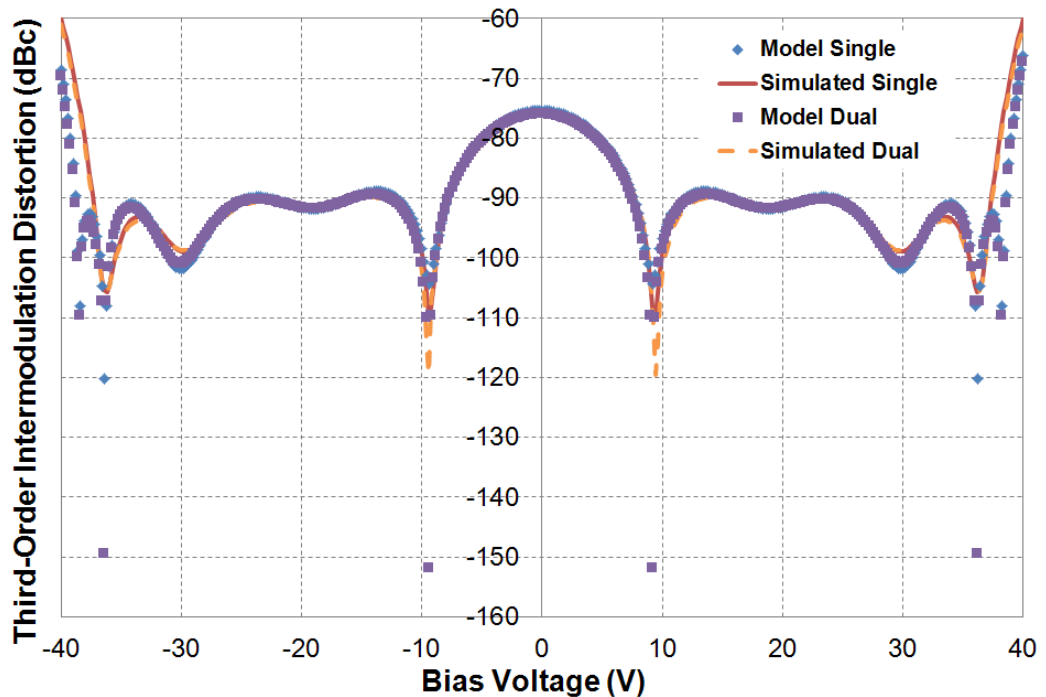
Figure 4.5: The third-order intermodulation distortion of model and simulated results for the dual BST varactor circuit topology.
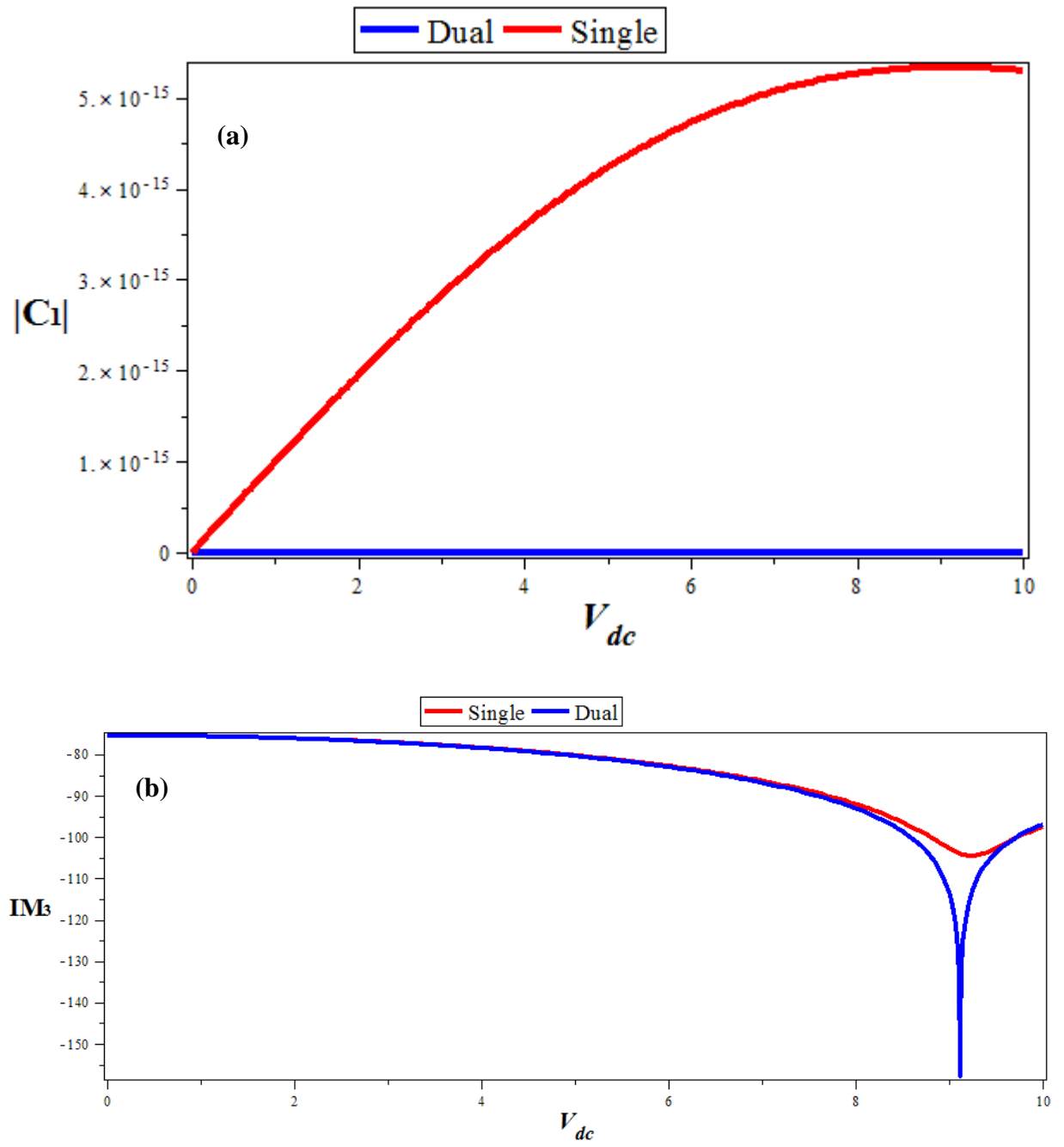
Figure 4.6: (a) The numerical simulation of C_1 and (b) closer view of the IM_3 from 0 to 10 V

for single and dual BST varactor circuit topologies.

4.3.2 Theoretical Analysis of Series Dual BST Varactor Circuit

Topology

In order to reduce both the second- and third-order coefficients, C_1 and C_2, the ideal series dual BST varactor circuit topology is implemented as shown in Figure 4.7. This topology is proposed to further reduce the nonlinearity in the dual topology. It has two identical BST varactors in series with opposite bias voltages applied (anti-series topology) and, in parallel with another identical set, yielding the term "series dual" topology.

In Table 4.4, the coefficients are summed up for the anti-series connections. Here, it can be observed that C_1 is perfectly cancelled out and C_2 is reduced significantly. For matched BST varactors in anti-series connections, the total capacitance equation is derived as [133]

$$C(v) = \frac{M_0}{2} + \frac{M_2}{8}\left[1 - \frac{1.5M_1^2}{M_0 M_2}\right]v^2 \tag{8}$$

where the anti-series connections coefficients are: $C_0 = \dfrac{M_0}{2}, C_1 = 0$ and $C_2 = \dfrac{M_2}{8}\left[1 - \dfrac{1.5M_1^2}{M_0 M_2}\right]$.
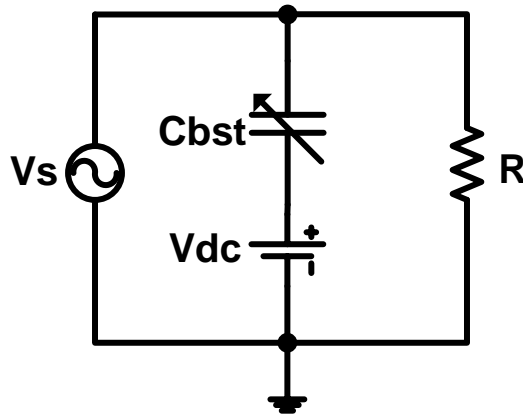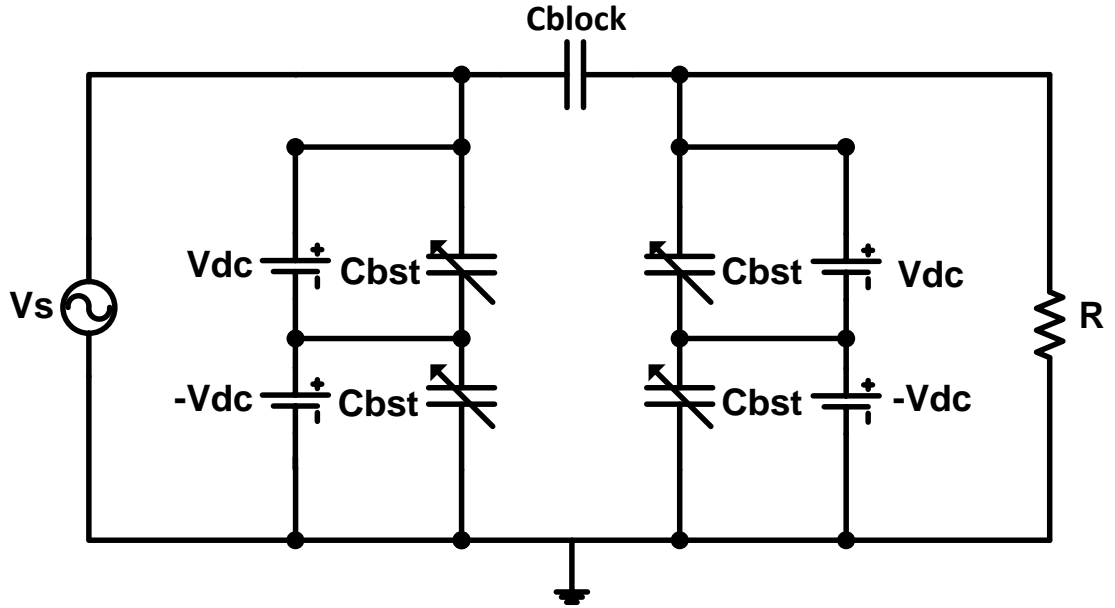

Figure 4.7: Ideal schematic of the series dual BST varactor circuit topology.

Table 4.4: Coefficients of ideal series dual BST varactor circuit topology.

Coefficient	Polynomial Expression
C_{0left_sum}	$[K_0 + K_2(V_{dc})^2 + K_4(V_{dc})^4 + K_6(V_{dc})^6 + K_8(V_{dc})^8 + K_{10}(V_{dc})^{10} + K_{12}(V_{dc})^{12} + K_{14}(V_{dc})^{14} + K_{16}(V_{dc})^{16}] / 2$
C_{0right_sum}	$[K_0 + K_2(V_{dc})^2 + K_4(V_{dc})^4 + K_6(V_{dc})^6 + K_8(V_{dc})^8 + K_{10}(V_{dc})^{10} + K_{12}(V_{dc})^{12} + K_{14}(V_{dc})^{14} + K_{16}(V_{dc})^{16}] / 2$
C_{1left_sum}	0
C_{1right_sum}	0
C_{2left_sum}	$1/8[K_2 + 6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6 + 45K_{10}(V_{dc})^8 + 66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12} + 120K_{16}(V_{dc})^{14}][1 - [1.5[2K_2V_{dc} + 4K_4(V_{dc})^3 + 6K_6(V_{dc})^5 + 8K_8(V_{dc})^7 + 10K_{10}(V_{dc})^9 + 12K_{12}(V_{dc})^{11} + 14K_{14}(V_{dc})^{13} + 16K_{16}(V_{dc})^{15}]^2 / [K_0 + K_2(V_{dc})^2 + K_4(V_{dc})^4 + K_6(V_{dc})^6 + K_8(V_{dc})^8 + K_{10}(V_{dc})^{10} + K_{12}(V_{dc})^{12} + K_{14}(V_{dc})^{14} + K_{16}(V_{dc})^{16}][K_2 + 6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6 + 45K_{10}(V_{dc})^8 + 66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12} + 120K_{16}(V_{dc})^{14}]]]$
C_{2right_sum}	$1/8[K_2 + 6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6 + 45K_{10}(V_{dc})^8 + 66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12} + 120K_{16}(V_{dc})^{14}][1 - [1.5[2K_2V_{dc} + 4K_4(V_{dc})^3 + 6K_6(V_{dc})^5 + 8K_8(V_{dc})^7 + 10K_{10}(V_{dc})^9 + 12K_{12}(V_{dc})^{11} + 14K_{14}(V_{dc})^{13} + 16K_{16}(V_{dc})^{15}]^2 / [K_0 + K_2(V_{dc})^2 + K_4(V_{dc})^4 + K_6(V_{dc})^6 + K_8(V_{dc})^8 + K_{10}(V_{dc})^{10} + K_{12}(V_{dc})^{12} + K_{14}(V_{dc})^{14} + K_{16}(V_{dc})^{16}][K_2 + 6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6 + 45K_{10}(V_{dc})^8 + 66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12} + 120K_{16}(V_{dc})^{14}]]]$

Figure 4.8 depicts the numerical simulation of C_2 which clearly indicates a significant reduction for the series dual compared to the single topology when biased from -40 to 40 V.

For the series dual topology in Figure 4.9, it can be observed that the entire IM_3 level has dropped significantly compared to the single topology. A 13 dB improvement can be achieved at 0 V and at higher bias voltages, an average of more than 40 dB improvement, starting from the first null at 20 V. The lower IM_3 achieved in this topology is due to C_1 and C_2 being minimized.

Since measured BST capacitance values with slight tolerances between them were implemented in both dual and series dual topologies, the perfect cancellation of the second-

order term or much lower third-order term could not be achieved. However, linearity improvements can still be realised.
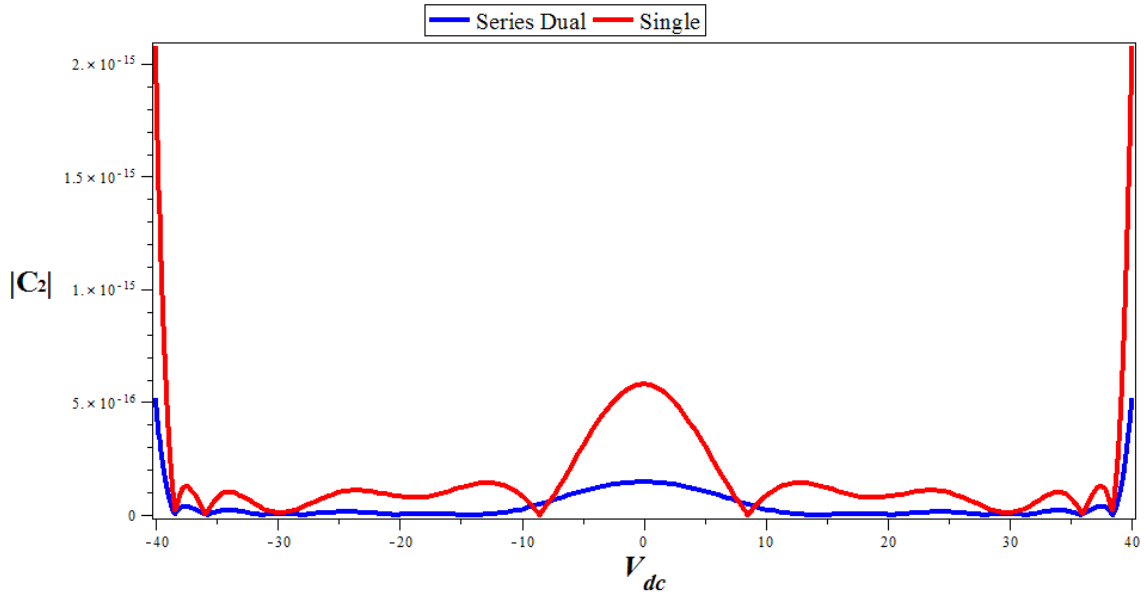
Figure 4.8: The numerical simulation of C_2 from -40 to 40 V for single and series dual BST varactor circuit topologies.
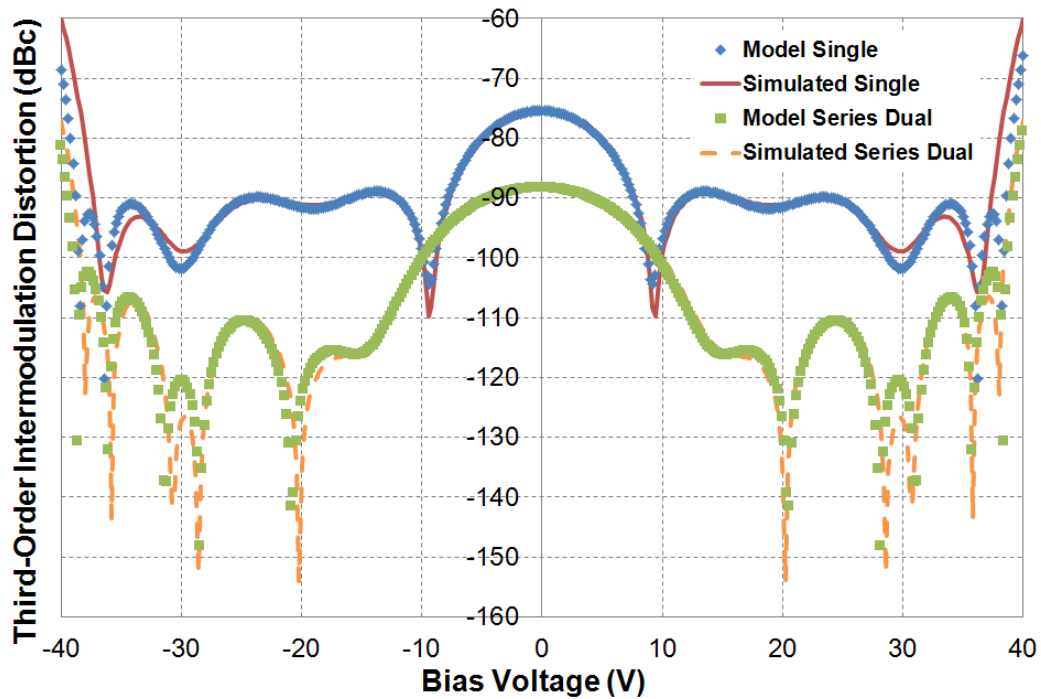
Figure 4.9: The third-order intermodulation distortion of model and simulated results for the series dual BST varactor circuit topology.

4.4 Measurements and Analyses

The selected IDCs discussed in Section 4.2 were mounted on a 20 x 32 mm^2 Rogers RO4003C board with a dielectric constant, ε_r of 3.38. Two diced chip varactors were positioned between the 50 Ω microstrip signal lines and ground planes, and integrated in a dual BST varactor circuit topology. On another board, four diced chip varactors were integrated in a series dual BST varactor circuit topology. Each diced chip had three varactors in array (two varactors as spares) with a footprint of 1.5 x 2 mm^2. On both boards, a 22 pF surface-mount technology (SMT) capacitor decoupled the left-hand and right-hand sides of the chip varactors for biasing purposes. These varactors were wirebonded to the external 50 Ω signal and ground Au-plated Cu microstrip lines. The circuit board was mounted on an aluminium block for mechanical stability. The Device Under Tests (DUTs) for both topologies are shown in Figure 4.10.
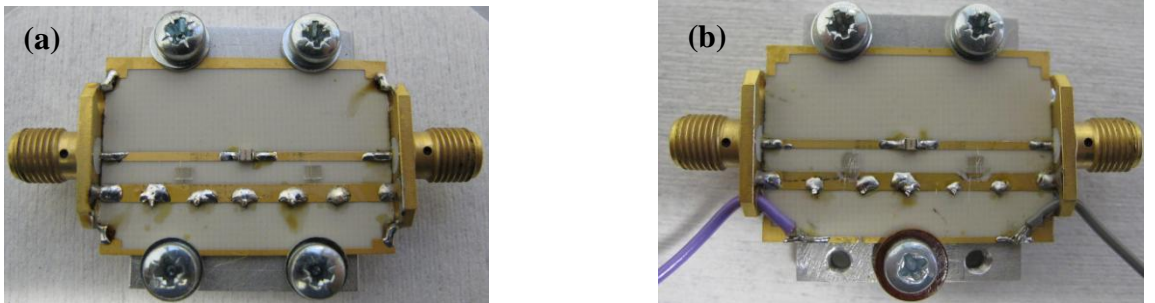
Figure 4.10: Device under tests of the (a) dual and (b) series dual BST varactor circuit topologies.

The DUTs for both topologies were initially designed in ADS software, including the microstrip lines, bondwires and SMT capacitors and simulations were performed. Figure 4.11 shows the board design of the dual BST varactor circuit topology. The IM$_3$ was then measured by applying two-tone input signals at 1.80 GHz and 1.81 GHz and input power of

16 dBm. The frequencies were chosen to accommodate the measurement setup which operated within the frequency range of interest. The schematic of the measurement setup is illustrated in Figure 4.12: it consisted of signal generators, amplifiers, bandpass filters, isolators, a power combiner, bias tees, power supplies, an attenuator and a spectrum analyser. Power amplifiers were used to generate sufficiently high input power levels to enable the BST varactors to produce IM_3 peaks above the noise floor. Each power amplifier had a built-in isolator to prevent the signals from reflecting back to it and the signal generators. Also, the isolator helped to avoid possible leak-through from one signal generator to another [151]. Insertion losses between 0.5 dB to 1 dB were achieved when the DUTs were connected between the bias tees. The whole measurement setup is shown in Figure 4.13. The setup parameters for the *Agilent E4405B* spectrum analyser are shown in Table 4.5.

Figure 4.11: The board design of the dual BST varactor circuit topology.

Figure 4.12: The schematic of the third-order intermodulation distortion measurement setup.

Figure 4.13: The measurement setup.

Table 4.5 : The setup parameters for the *Agilent E4405B* spectrum analyser.

Parameter	Value
Resolution Bandwidth (RBW)	1 kHz
Video Bandwidth (VBW)	300 Hz
Frequency span	10 MHz
Noise floor	110 dBm

For the dual topology, the IM_3 simulated and measured results are shown in Figure 4.14 with the BST varactors biased up to ±25 V. The measured first null is achieved at ±13 V, a ±4 V shift from the ideal value. However, good agreement is observed where the general trend of reduced distortion is realised. A 5 dB deviation at higher voltages starting from 20 V between the simulated and measured data is also observed.

In Figure 4.15, the entire IM_3 level has dropped about 5 dB for the series dual topology compared to the dual topology at 0 V. The measured first null was achieved at ±20 V with a ±8 V shift from the ideal value, although good agreement is observed. The general trend of much-reduced distortion compared to the dual topology is realised. In comparison with Figure 4.9, the first null of this simulated result becomes significant at ±13 V due to the extra "islands" introduced in the circuit. These islands are small area of microstrip lines which serve as negative nodes for opposite biasing of the varactors.

The voltage shifts in both topologies were caused by the degradation in the tunability of the BST varactors due to the compression of the *C-V* curves resulting from the high input power levels [22]. As shown in Figure 4.16, the compression of the *C-V* curves for the single BST varactor due to a continuous increase in input power levels, results in the degradation of its tunability. It can be observed that as the input power increases from 0 to 30 dBm, the peak capacitance (C_{max}) at 0 V starts to compress. In Figure 4.17, the nulls shift to higher voltages as the input power increases. As observed, the first nulls are shifted to 9, 11 and 15 V for 20,

25 and 30 dBm respectively. An alternative to reduce this degradation is to increase the stacking of the BST varactors, similar to [19].
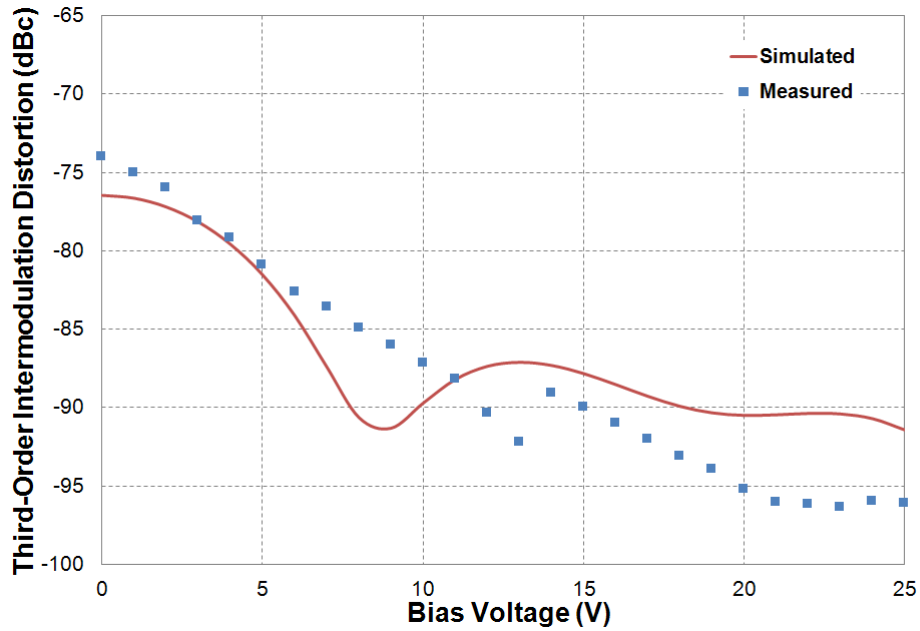
Figure 4.14: The third-order intermodulation distortion of simulated and measured results for the device under test of dual BST varactor circuit topology.
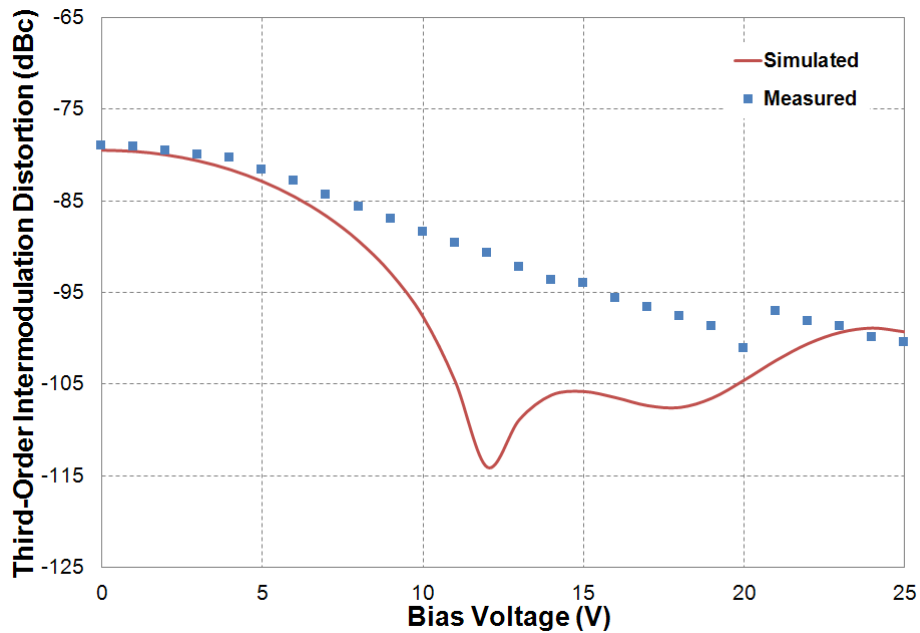
Figure 4.15: The third-order intermodulation distortion of simulated and measured results for the device under test of series dual BST varactor circuit topology.
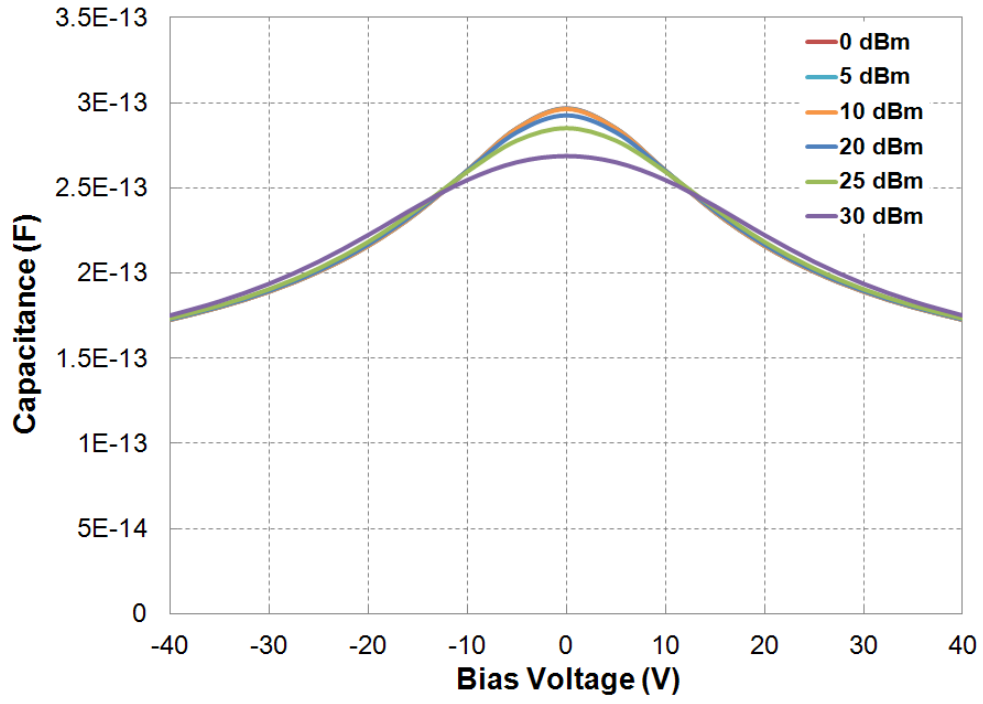
Figure 4.16: Compression of the *C-V* curves for the single BST varactor due to increasing
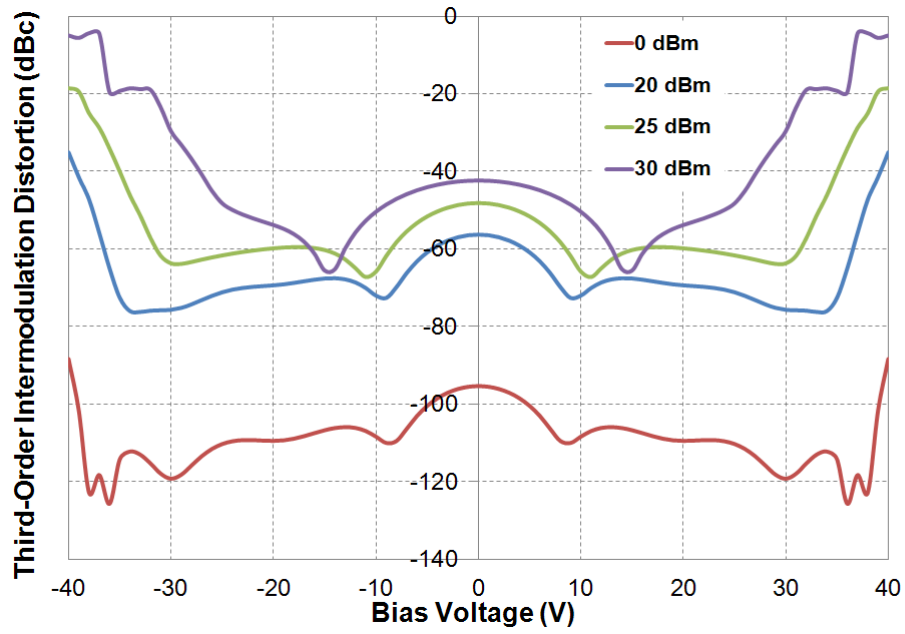
input power.

Figure 4.17: Shifting of the nulls in the dual BST varactor circuit topology due to increasing

input power.

The dual topology *C-V* curve is compressed further, compared to the series dual topology due to the larger RF swing across the varactors, resulting in a broader *C-V* curve. A broader *C-V* curve tends to have better IM_3 which contributes to a higher third-order intercept point (IP_3). This justified the slight deviation between the simulated and measured data at higher voltages in Figure 4.14.

Several single bondwires were also used on the DUTs, mainly in the series dual topology, which contributed to the parasitic inductances and degraded the IM_3 level. Figure 4.18 shows the simulation which confirmed the effects of these inductances that degraded the IM_3 level by 6 dB at 0 V.

Further, the simulation results are often affected by finite convergence limits especially at high input power and may limit their accuracy.
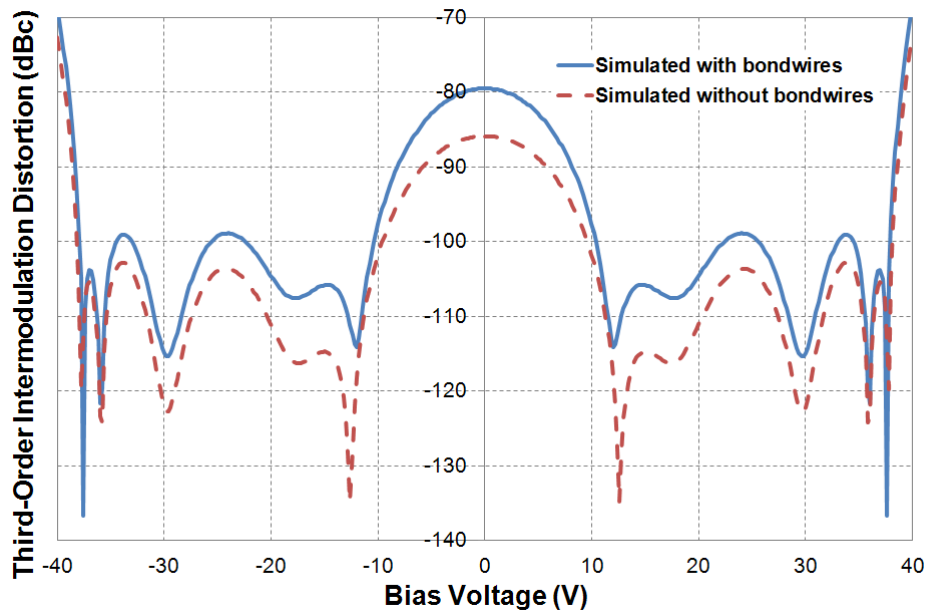
Figure 4.18: Bondwire effects which degraded the linearity.

4.5 Conclusions

This chapter has presented a novel method for the theoretical analysis of the IM_3 in BST thin film IDCs on r-plane sapphire substrates. A polynomial equation was initially derived from the measured BST varactor *C-V* curve data and all the relevant coefficients (*C_0, C_1 and C_2*) were extracted and substituted in a slightly modified IM_3 equation, which is ideal for the analysis of a BST varactor.

The comparison between the IM_3 theoretical model and simulated results showed excellent agreement for both dual and series dual BST varactor circuit topologies. Significantly low nulls were achieved in both topologies compared to the single BST topology as the varactors were carefully biased up to ±40 V. A significant improvement of IM_3 at all bias voltages was also achieved in the series dual topology compared to the single and dual topologies, with a 13 dB improvement at 0 V.

Low IM_3 was experimentally demonstrated in both dual and series dual BST varactor circuit topologies. The measured first nulls were achieved at ±13 V and $\pm$ 20 V for the dual and series dual topologies respectively with ±4 V and ±8 V shift from their ideal values. The voltage shifts were caused by the degradation in the tunability of the BST varactors, due to the compression of the *C-V* curves as confirmed through simulation. The *C-V* curve of the dual topology, however, was compressed further due to larger RF swing across the varactors. The performance degradation due to several bondwires especially in the series dual topology was also confirmed through simulation, which explained the reason for only a 5 dB improvement compared to the dual topology at 0 V.

However, the high linearity achieved in these BST circuit topologies has the potential to be implemented into SoS technology. The r-plane sapphire is found to be a suitable orientation for the growth of a very thin silicon layer. The integration of BST and silicon technologies

can be realised by depositing the BST early in the process before any metallization is done; hence it is unlikely to affect the SoS process.

In the next chapter, the 1 dB compression point of BST varactors is investigated. Parametric analysis of the BST varactor geometry in terms of its finger gap, width, length and number of fingers was performed. The relationships between the optimised *C-V* curves and their 1 dB compression points were then analysed via circuit simulations and measurements.

Chapter 5

Barium Strontium Titanate Thin Film Varactors with High 1 dB Compression Points

5.1 Introduction

As highlighted in Chapter 2, the body of literature relating to the investigation of power handling capability (PHC) of BST varactors is currently limited [22-25]. These studies, however, did not emphasize the importance of the 1 dB compression point of BST varactors. More importantly, the relationship between the tunability and the 1 dB compression point of BST thin film varactor has not been studied in detail. The 1 dB compression point is defined as the power level at which the output power of a nonlinear device reduces by 1 dB from its

ideal linear response. At this point, the gain response of the device is reduced by a specific amount.

This chapter aims to develop BST thin film varactors with high 1 dB compression points fabricated on c-plane sapphire substrates. The research objective is to analyse the effect of varying the geometry of the BST interdigital capacitor (IDC) in terms of its finger gap, finger width, finger length and also the number of fingers on the shape of the nonlinear *C-V* curves. The shape of the *C-V* curves will certainly become narrower or broader, depending on the geometry selections. The relationships between the optimised *C-V* curves and their 1 dB compression points are subsequently shown by simulations and measurements.

5.2 The 3D Modelling of BST Interdigital Capacitor

The BST IDC was initially modelled in Computer Simulation Technology (CST) software with the parameter specifications given in Table 5.1. The IDC with the same specifications for 700 nm BST layer was previously fabricated on c-plane sapphire substrates, achieving ~56 % tunability [6]. The measured capacitance values were then used to accurately determine the corresponding dielectric constants from 0 to 40 V for the simulation setup which will be discussed in the next subsection.

In this research, for the first time the BST thin films were deposited on c-plane sapphire substrates using the *Kurt J. Lesker* RF magnetron sputterer at RMIT University. As reported in Chapter 3, a thickness of ~400 nm was consistently achieved in all samples. Note that this is the maximum BST thickness that the sputterer could deposit. The samples were then post-annealed in vacuum oven and air and IDCs were fabricated on the samples using the mask with fine geometries as mentioned in Chapter 3.

Table 5.1: The parameter values of the modelled BST interdigital capacitor.

Parameter	Value
Finger gap: f_G (μm)	2
Finger width: f_W (μm)	5
Finger length: f_L (μm)	130
Number of fingers: f_N	8
BST film thickness: h_{bst} (μm)	0.7
Sapphire thickness: h_{sub} (μm)	1.4
Electrode thickness: h_{elec} (μm)	2.5
Sapphire dielectric constant: ε_r	10.2

5.2.1 Modelled Structure of 700 nm BST Layer Varactor

The initial model of the BST varactor on sapphire substrate is shown in Figure 5.1. The BST interdigital capacitor geometry which consisted of finger gap (f_G), finger width (f_W), finger length (f_L) and number of fingers (f_N) was designed on top of a BST layer on sapphire substrate. The values of these parameters are tabulated in Table 5.1. In the CST Microwave Studio, the IDC was designed with perfect electric conductor (PEC) electrodes and pads in an enclosed shielded structure. Two *full plane* ports were defined and boundary conditions of perfectly electric conducting walls were assigned at each side of the structure as depicted in Figure 5.2. The size of the waveguide port should be reasonably large enough to incorporate a significant part of the varactor fields. A port size that is too large may cause higher order waveguide modes to propagate in the port which results in very slow energy decays in the transient and sharp spikes in the frequency domain simulations respectively. However, a port size which is too small may cause degradation of the S-parameter's accuracy or even
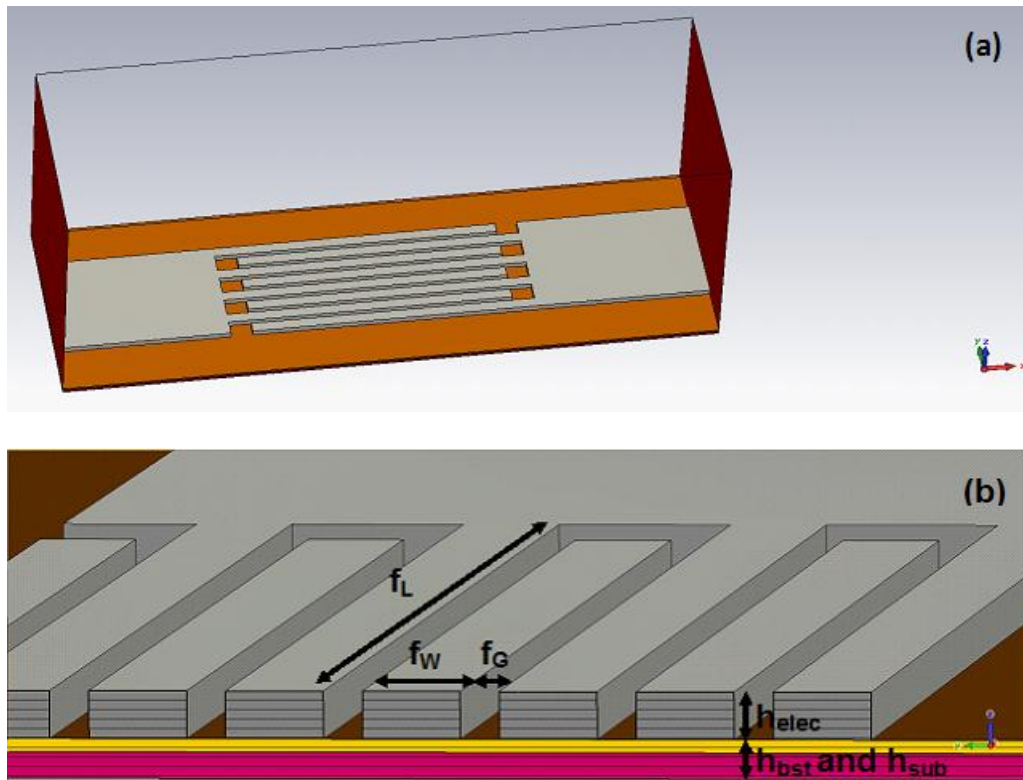
Figure 5.1: (a) Side view and (b) cross section of the modelled BST interdigital capacitor geometry.
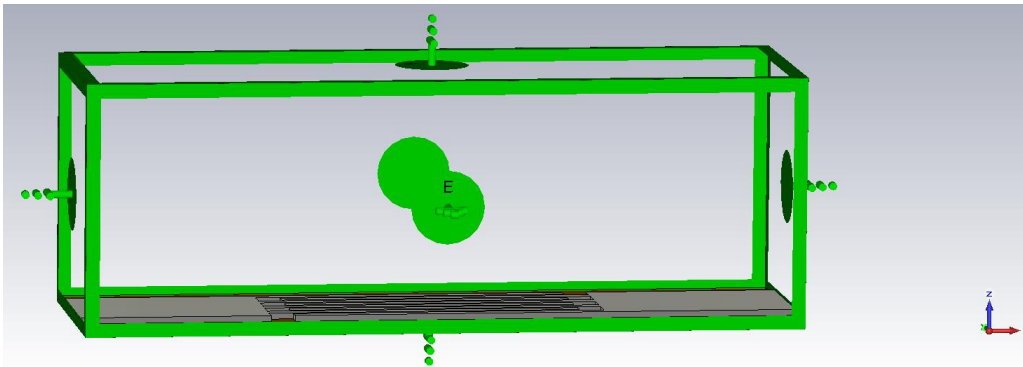
Figure 5.2: The boundary conditions with perfect electric conducting walls at each side of the modelled device structure.

instabilities of the transient solver [152]. Therefore, the easiest method of defining the ports which covers the entire boundary face of the device structure is to use the *Full Plane* option.

Depending on the type of structure to be simulated, the *transient (time domain) solver* and *frequency domain solver* are typically chosen to calculate the S-parameters. A *transient solver* is more suitable to simulate any kind of S-parameter or antenna problem and with the broadband simulation, the S-parameters for the entire desired frequency range could be achieved. The *frequency domain solver* is the fastest tool when it comes to calculating a small number of frequency samples and, to reduce simulation time, a broadband S-parameter simulation with adaptively chosen frequency samples is performed [152]. Since the device structure is a nonlinear frequency dependent BST varactor, the *frequency domain solver* was chosen for this type of simulation.

Before simulating the structure, the type of mesh must be considered due to its strong influence on the accuracy and speed of the simulation. The types of meshes which are typically selected are hexahedral mesh and tetrahedral mesh. In this case, tetrahedral mesh was implemented across the structure with local mesh refinements around the area of the electrodes as depicted in Figure 5.3. If hexahedral mesh is implemented, it may produce a large overhead in the number of elements for that part of the computational domain that does not require a fine mesh. For a small-scaled geometry such as the interdigital capacitor, tetrahedral mesh is more suitable as it does not include many mesh cells and can resolve the thin structure locally [152]. A total of ~27000 mesh elements were applied across the entire structure. The simulation was subsequently performed by sweeping the dielectric constant of the defined BST thin film from 560 to 115 which correlated to the bias voltage from 0 to 40 V of the measured BST varactor. The simulated and measured *C-V* curves at 10 GHz are shown in Figure 5.4 where excellent agreement is achieved.
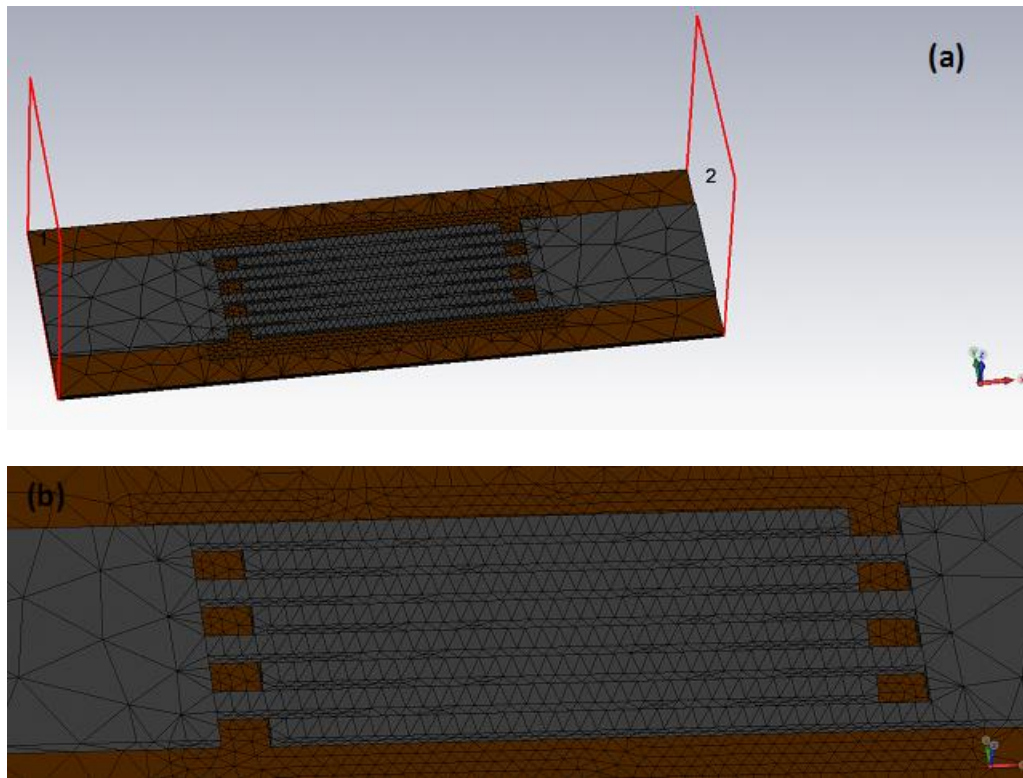
Figure 5.3: Tetrahedral meshing with mesh refinements across the area of the modelled interdigital electrodes (a) Side view and (b) enlarge view of the tetrahedral meshing across the electrodes.
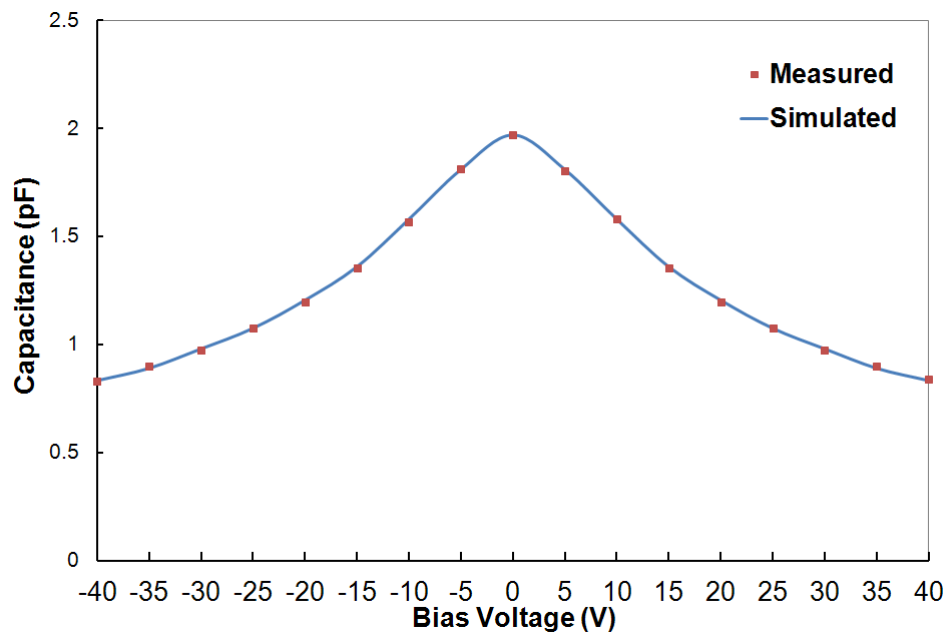
Figure 5.4: Simulated and measured *C-V* curves of the BST varactor at 10 GHz.

5.2.2 Parametric Analysis of the Modelled Structure

In this subsection, parametric analysis was performed by varying the IDC geometry and the changes in the shape of the nonlinear *C-V* curves were analysed. The aim of this analysis was to optimise the IDC parameter values for defining three distinct *C-V* curves: narrow, broad and intermediate curves.

In Figure 5.5, the finger gap (f_G) is varied from 1 to 10 μm while the other parameters are held constant at $f_W = 5$ μm, $f_L = 130$ μm and $f_N = 8$. As observed, f_G becomes insignificant above 8 μm and the smallest value of 1 μm is considered due to the fabrication limitation of the lithography equipment in RMIT University. It is observed that as f_G increases, the *C-V* curve becomes broader and the capacitance value drops over the entire tuning voltage range. This indicates a significant reduction in the tunability when f_G increases with the peak capacitance (C_{max}) drops from 2.77 to 1.3 pF. Also as observed, there is a significant drop in C_{max} when f_G increases from 1 to 2 μm with a 0.8 pF difference. The significant difference could be attributed to the higher confinement of DC and microwave fields [2] in the BST film of the 1 μm which resulted in a much higher tunability than the 2 μm.

Figure 5.6 shows that as the finger width (f_W) varies from 1 to 10 μm while the other parameters are held constant at $f_G = 2$ μm, $f_L = 130$ μm and $f_N = 8$, the *C-V* curve becomes broader. However, the capacitance value increases uniformly over the entire tuning voltage range with C_{max} increases from 1.63 to 2.3 pF. This also indicates that by increasing f_W, it causes a much lower tunability.
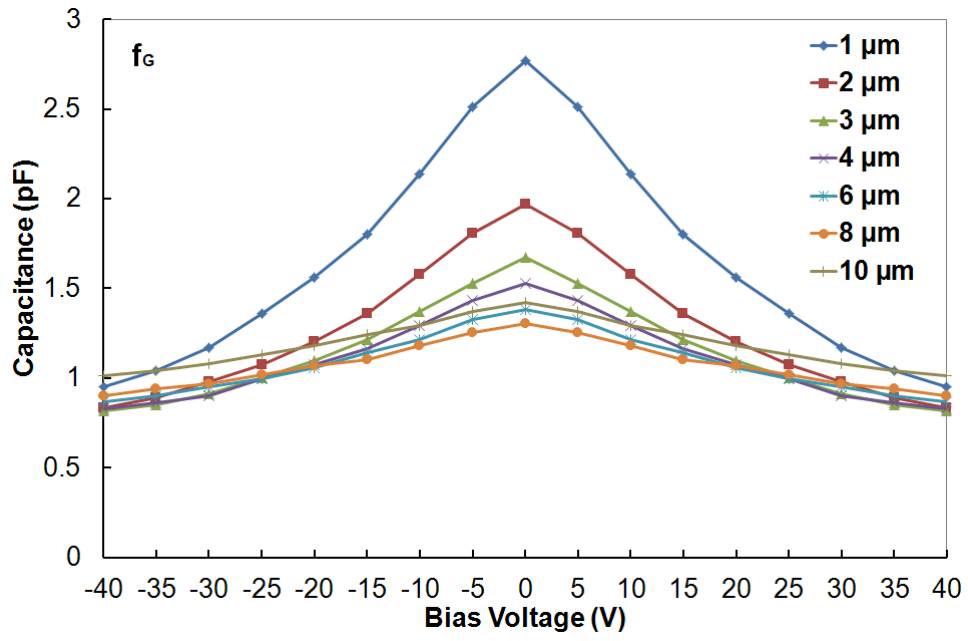
Figure 5.5: The nonlinear *C-V* curves by varying the finger gap from 1 to 10 µm.
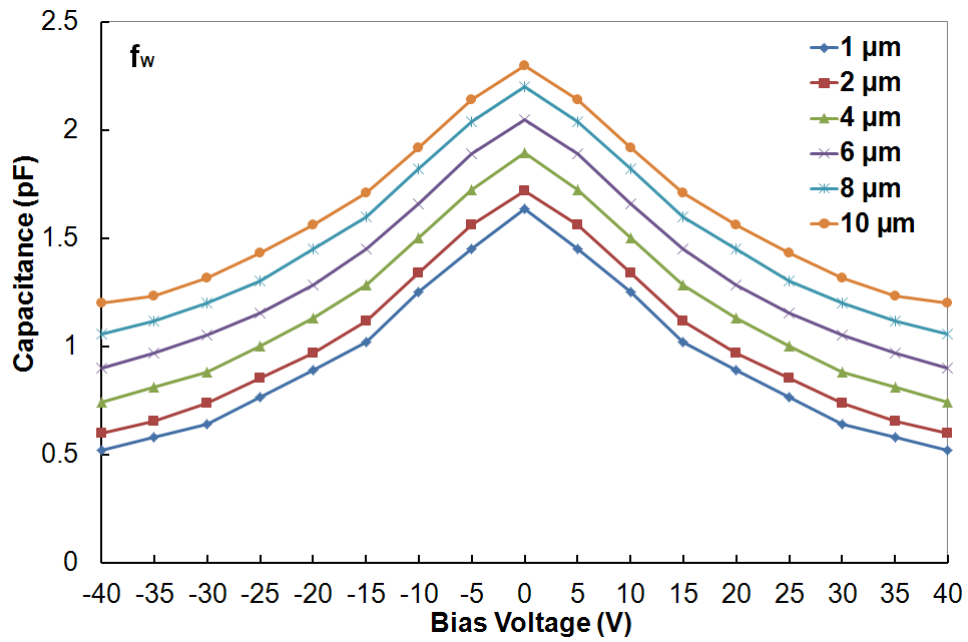
Figure 5.6: The nonlinear *C-V* curves by varying the finger width from 1 to 10 µm.

In Figure 5.7, a similar increasing capacitance value trend is shown. When finger length (f_L) varies from 90 to 150 μm with constant parameters at f_G = 2 μm, f_W = 5 μm and f_N = 8, C_{max} increases from 1.45 to 2.2 pF. In contrast to Figure 5.6, the *C-V* curve becomes narrower although this behaviour has a slight impact on the tunability, which is about 4 % rise from 90 to 150 μm.

Figure 5.8 also indicates that by varying f_N from 4 to 12 with constant parameters at f_G = 2 μm, f_W = 5 μm and f_L = 130 μm, C_{max} increases from 0.95 to 2.97 pF and the *C-V* curve becomes narrower. However, this trend has a slight impact on the tunability, which is about 2% rise from 4 to 12.
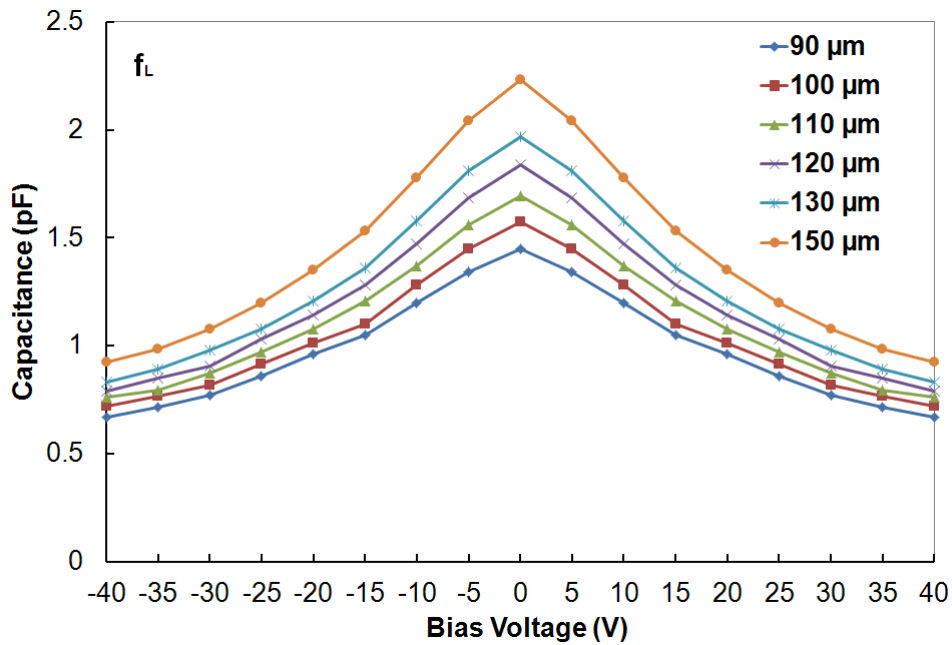
Figure 5.7: The nonlinear *C-V* curves by varying the finger length from 90 to 150 μm.
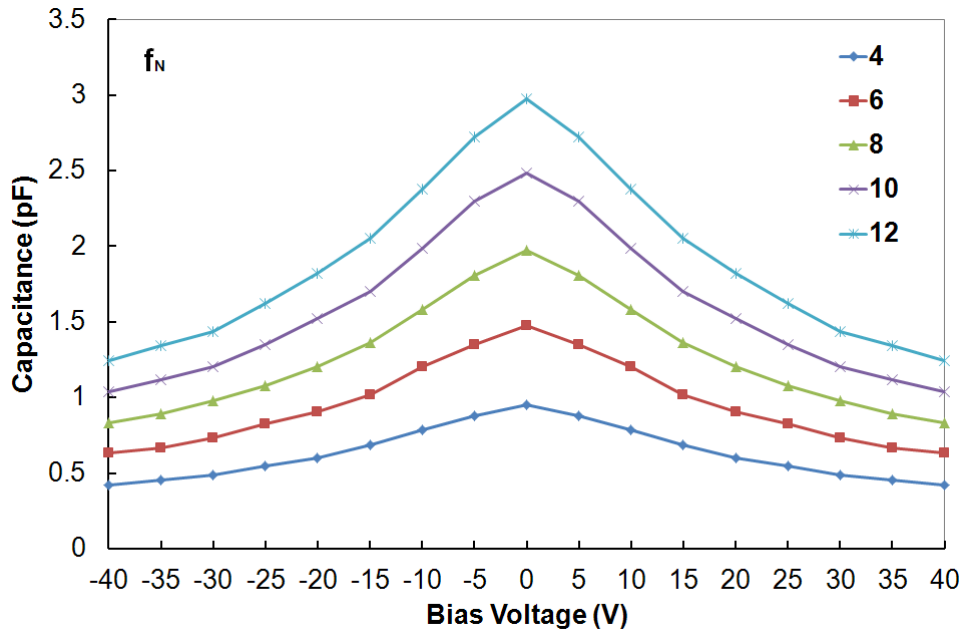
Figure 5.8: The nonlinear *C-V* curves by varying the number of fingers from 4 to 12.

5.3 The 1 dB Compression Point of BST Varactor

From the parametric analysis shown in the previous section, the narrow, broad and intermediate *C-V* curves were considered and the 1 dB compression point for each curve was determined. The IDC geometry for each case was optimised with C_{max} value preserved at ~2 pF as depicted in Figure 5.4.

Table 5.2 shows the optimised parameter values for each case. For the narrow curve, the IDC geometry was chosen to achieve the highest tunability of 73 %. This was well in agreement with [2] where the highest degree of confinement of DC and microwave fields in the BST film can be realised due to $f_g \approx f_w$ with the smallest values. The IDC geometry for the broad curve was chosen to achieve the lowest tunability at 28 %. In this case, the lowest confinement of DC and microwave fields in the BST film was realised due to the largest values of f_g and f_w. Figure 5.9 shows the electric field distributions between the gaps of the electrodes for the narrow and broad varactors. As observed, high intensity of E-fields

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Table 5.2: Parameter values for the narrow, broad and intermediate *C-V* curves.

Parameter		Narrow	Broad	Intermediate
Finger gap: f_G (µm)		1	8	3
Finger width: f_W (µm)		1	10	5
Finger length: f_L (µm)		110	150	160
Number of fingers: f_N		8	8	8
Simulated capacitance (pF)	0 V	1.96	1.95	1.99
	40 V	0.534	1.4	0.9146
Simulated tunability (%)		72.76	28.2	54
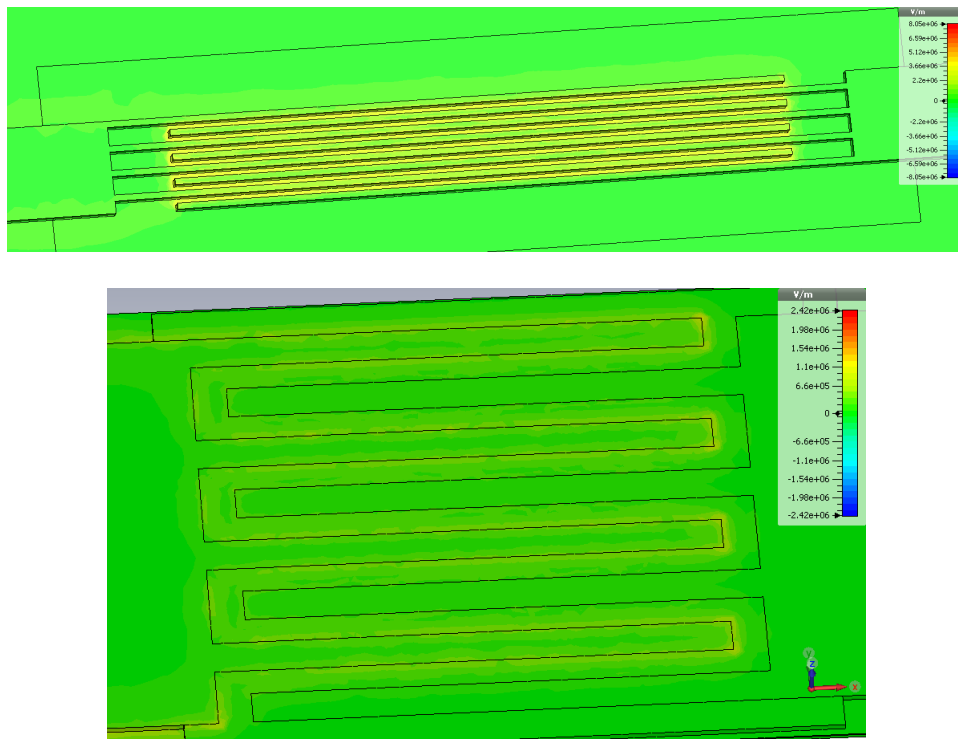
Figure 5.9: Electric field distributions between the 1 µm and 8 µm gap varactors.
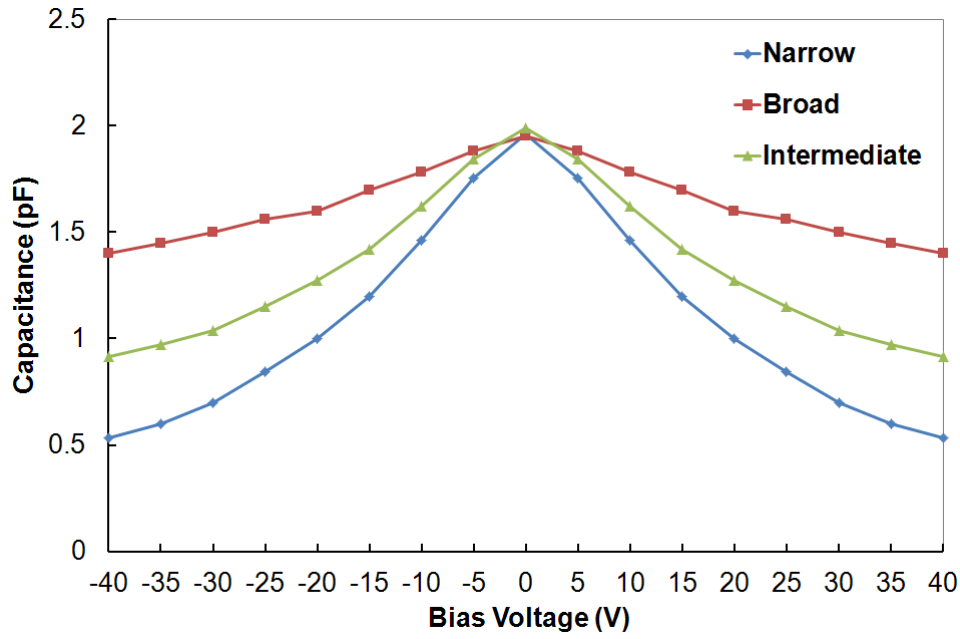
Figure 5.10: Narrow, broad and intermediate nonlinear *C-V* curves.

(indicated with dark orange colour) occurs between the 1 µm gaps while considerably less E-fields intensity is expected between the 8 µm gaps. The IDC geometry for the intermediate curve achieved a tunability of 54 %. All the curves are depicted in Figure 5.10.

The data in Figure 5.10 was subsequently compared to the established nonlinear *C-V* BST varactor model [132] via a curve-fitting function in MATLAB. A very good fit was achieved and important parameter values of the fringing capacitance (C_f) and the "2:1" voltage (V_2) were extracted. Using Agilent Advanced Design System (ADS) software, this nonlinear model along with the extracted parameter values were substituted into a nonlinear equation-based capacitor of a simple two-port series network as designed in Figure 5.11. The simulation was then performed by varying the input power from -10 to 50 dBm and the 1 dB compression point for each *C-V* curve was determined.

Figure 5.12 shows the 1 dB compression points for the narrow, broad and intermediate *C-V* curves. As observed, the broad curve achieves the highest 1 dB compression point at 41 dBm compared to the narrow and intermediate curves at 29 and 32 dBm respectively. Even though
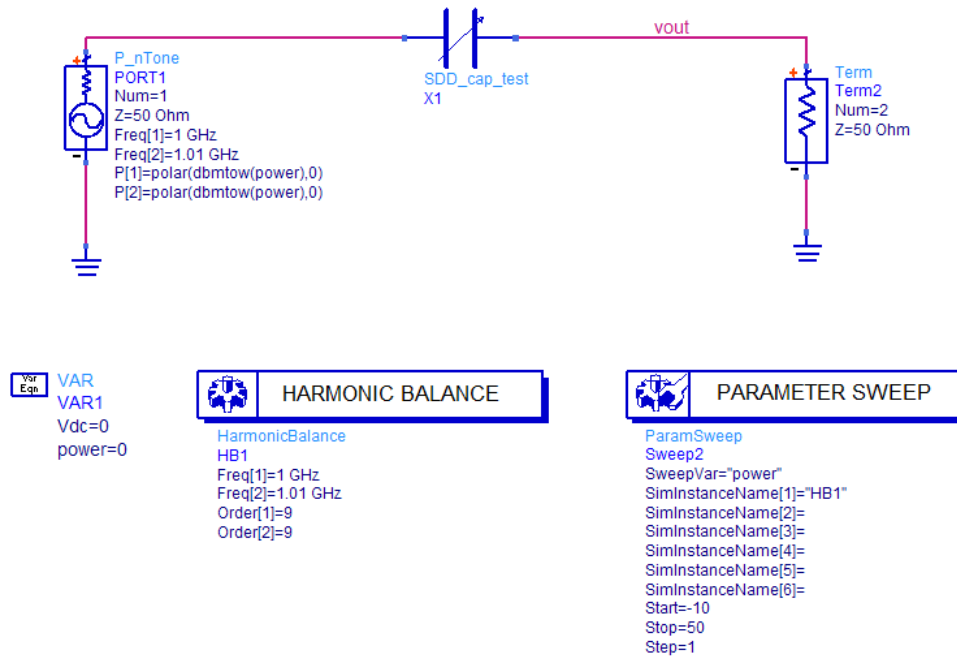
Figure 5.11: The nonlinear equation-based capacitor in a two-port series network for determining the 1 dB compression point.
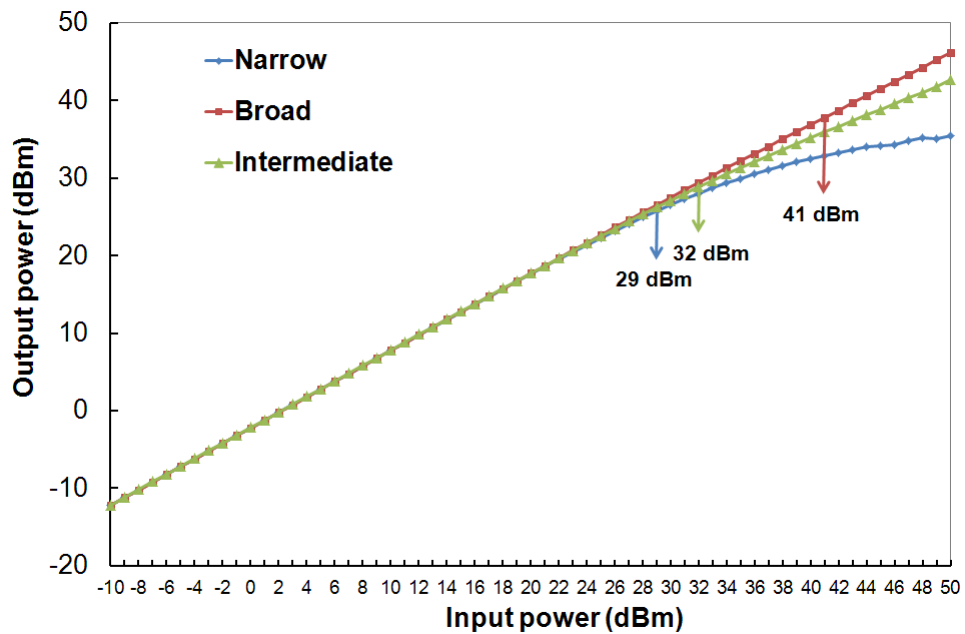
Figure 5.12: The 1 dB compression point of the narrow, broad and intermediate *C-V* curves.

the broad curve could withstand higher input power levels, it is compensated by having the lowest tunability. In contrast, the narrow curve compresses at lower input power levels but achieves the highest tunability. However, a BST varactor with reasonably high tunability and 1 dB compression point could be realised with the intermediate curve.

5.4 Measurements of 400 nm BST Layer Varactors

All the optimised *C-V* curves were realised in the physical form of varactors. The narrow, broad and intermediate varactors were fabricated on the deposited 400 nm BST layer grown on c-plane sapphire substrate. The details of the material deposition and fabrication process were comprehensively discussed in Chapter 3. Figure 5.13 shows the fabricated BST thin film varactors. Microwave measurements were performed and the results for all three varactors are tabulated in Table 5.3. As mentioned in Section 5.2, there was a limitation with depositing the BST thickness using the sputterer machine; hence, all the varactors were fabricated on the deposited 400 nm BST layer.

Figure 5.14 shows the measured and simulated *C-V* curves for all three varactors. As observed, the measured C_{max} (0 V) for all varactors were lower than ~2 pF of the equivalent simulated results and the tunabilities were also degraded due to the broader shape of the curves. The major constraints identified were the constraint of the deposited BST thickness and, strain-induced film due to the existence of oxygen vacancies which contributed to the lower tunability of the varactors. The deposition of different BST thickness would definitely change the varactors' performances. In this case, thinner film usually has a higher tensile strain and reduced grain size, which contributes to the lower dielectric constant. However, it was reported that the BST thickness could be optimised to achieve strain-relieved film with the highest tunability [9]. Post-annealing the film in air as conducted in Chapter 3 assisted in

improving the quality of the film, making it more crystalline and significantly reducing strain in the film.

(a)

(b)   **(c)**
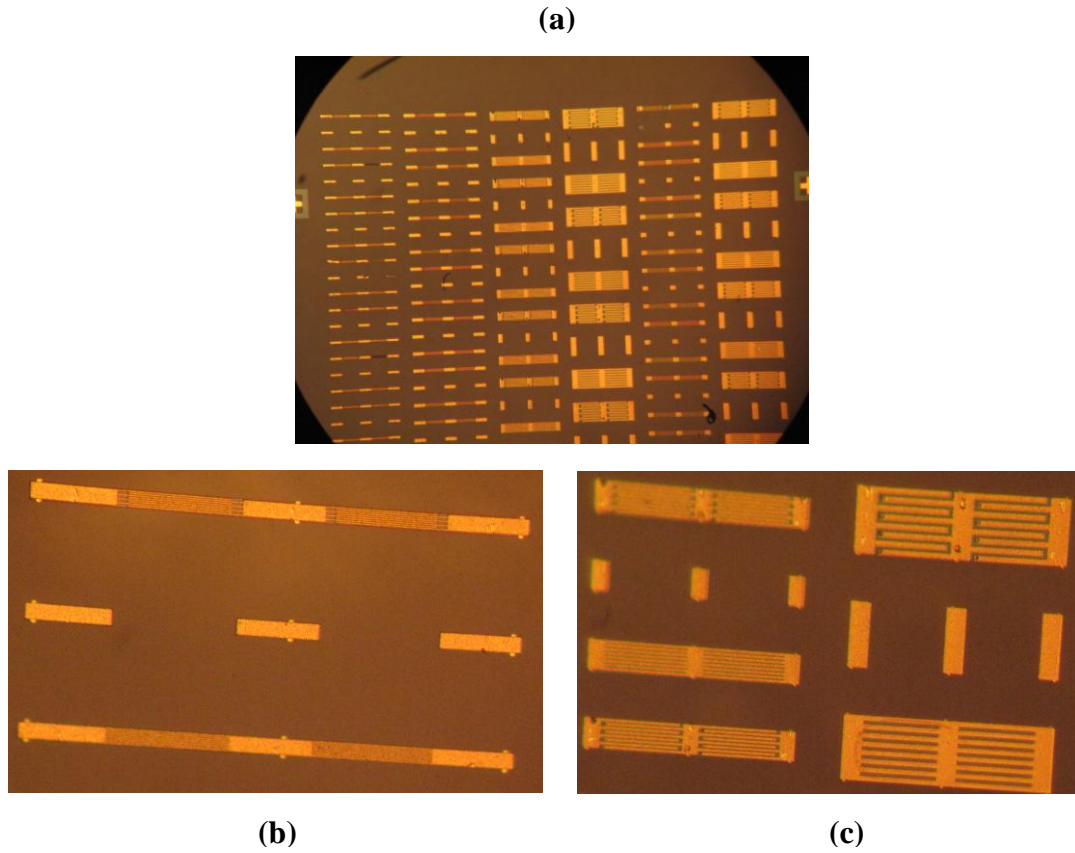
Figure 5.13: (a) The whole fabricated BST thin film varactors with different geometries on c-plane substrate, (b) the narrow varactor and (c) the intermediate and broad varactors.

Table 5.3: The performance of the measured narrow, broad and intermediate varactors at 10 GHz.

Type of varactor	Narrow		Broad		Intermediate	
Bias Voltage (V)	0	40	0	40	0	40
Capacitance (pF)	1.4805	0.7365	0.4927	0.463	1.0876	0.8219
Q-factor	8.74	20.76	16.3	24.6	12.6	22.23
Tunability (%)	50.25		6.04		24.4	
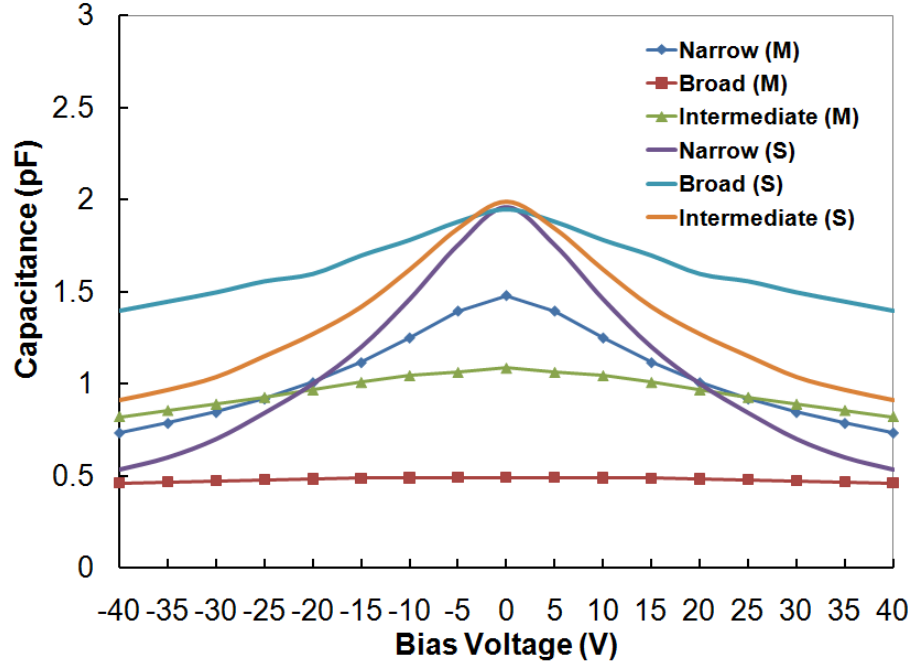
Figure 5.14: The comparison between the nonlinear *C-V* curves of the measured (M) and
simulated (S) narrow, broad and intermediate varactors.

The measured data for all varactors from Figure 5.14 were compared to the established
nonlinear BST model and substituted in the network similar to Figure 5.11. Simulation was
performed and the 1 dB compression point for each varactor was extracted as depicted in
Figure 5.15.

Table 5.4 shows the relationships between tunabilities and 1 dB compression points for all
measured and simulated varactors. As observed, the tunabilites of the measured varactors had
dropped by 20 to 30 % compared to their respective simulated varactors. It is evident that
C_{max} along with the tunability for each varactor had changed due to the 400 nm BST layer.
However, the extracted 1 dB compression points for the measured varactor results were
comparable to the simulated results. These results revealed that the slight thickness difference
did not have a significant impact on the 1 dB compression points. Although the intermediate
varactors had a 4.6 dB difference between them, this could be attributed to the much broader
curve of the measured intermediate varactor and a slight fabrication issue. The relationship

between the tunability and the 1 dB compression point is still valid; the varactor with the highest tunability produces the lowest 1 dB compression point while varactor with the lowest tunability produces the highest 1 dB compression point.
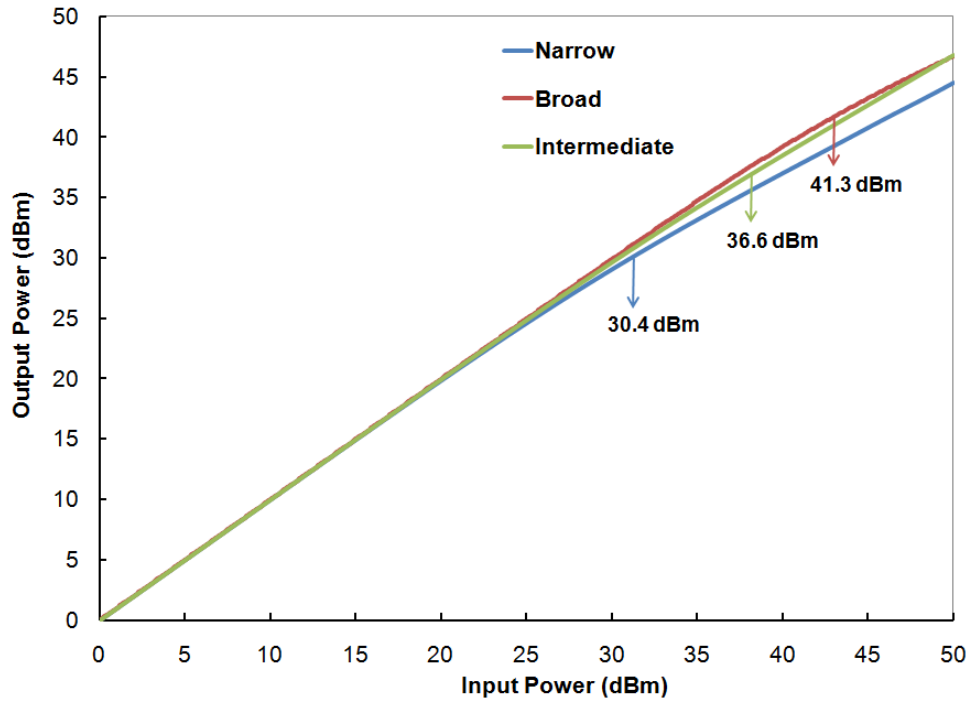
Figure 5.15: The 1 dB compression point of the measured narrow, broad and intermediate varactors.

Table 5.4: The relationships between tunabilities and 1 dB compression points of the varactors.

Type of varactor	Narrow		Broad		Intermediate	
Comparison	Simulated	Measured	Simulated	Measured	Simulated	Measured
Tunability (%)	72.76	50.25	28.2	6.04	54	24.4
1 dB compression point (dBm)	29	30.4	41	41.3	32	36.6

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5.5 Conclusions

This chapter has presented the relationship between the tunability and the 1 dB compression point of a BST varactor. The interdigital capacitor was modelled using CST software and a parametric analysis was made of its geometry by varying the finger gap, finger width, finger length and number of fingers in the specified design range. The effects on the shape of the nonlinear *C-V* curves were analysed for each parameter variation and three distinct *C-V* curves of narrow, broad and intermediate curves were subsequently produced. The 1 dB compression points for the optimised *C-V* curves were finally extracted from simulation.

For the equivalent varactors fabricated on the 400 nm BST layer, the measured tunability for each varactor was much lower than the simulated results due to deposition limitation and strain-induced film. However, the 1 dB compression points extracted for all three measured varactors were still comparable with the simulated results. These BST varactors have the potential to be implemented in high power microwave systems, possibly by integrating them with standard semiconductor chips and form hybrid modules such as system-on-chip (SoC).

Chapter 6

Conclusions and Future Work

During the course of this research, the author has investigated the large signal performance of nonlinear BST thin film varactors for agile microwave device applications. The focus was primarily on two important device parameters for large signal microwave applications: linearity and power handling capability. Most existing research work has concentrated on enhancing the tunability and lowering the microwave loss of BST thin film varactors to be implemented in many microwave devices, but only a few reports have discussed the large signal performance of these varactors.

In this research, the BST thin film varactors were fabricated on both r-plane and c-plane sapphire substrates since these materials exhibit very low loss at microwave frequencies, present close lattice match to BST thin film which enables epitaxial growth and have a relatively low cost. The r-plane orientation is also being implemented in silicon-on-sapphire (SoS) technology and this opens up the possibility of integrating BST thin film with the existing semiconductor technologies.

In this final chapter, summaries of the results established throughout this thesis are presented and the major findings of this research are highlighted. Also, potential future works are discussed.

6.1 BST thin films on c-plane sapphire substrates

A few deposition runs of BST thin films on c-plane sapphire substrates were established for the first time using the *Kurt J. Lesker* RF magnetron sputterer at RMIT University. The deposited BST thin films were from a stoichiometric $Ba_{0.6}Sr_{0.4}TiO_3$ target and through SEM analysis, BST thickness of ~400 nm was consistently achieved in all samples with the sputtering conditions held constant for every deposition run.

X-ray diffraction (XRD) analysis revealed peaks which corresponded to the cubic perovskite BST phase with no indication of secondary phase formation. The BST samples experienced a loss of crystallinity when post-annealed in vacuum oven for 10 minutes and an hour due to the existence of oxygen vacancies in the films. X-ray photoelectron spectroscopy (XPS) analysis confirmed the presence of defects or deformations in the crystal structure of the BST thin films with decreased at. % of Ba and Ti and increased at. % of O in both annealed samples. However, the BST sample post-annealed in air for 2 hours resulted in an improved crystallinity of the film with preferred (110) orientation and increased at. % of Ba and O due to the incorporation of oxygen in the film.

Interdigital capacitors were fabricated on both unannealed and annealed samples and microwave measurements of S_{11} were performed. For the annealed samples in a vacuum oven, their tunabilities were achieved at ~18 % which was similar to the unannealed samples, indicating no improvement in the crystallinity of the films. These results revealed that strain-induced films due to the presence of oxygen vacancies affected the performance of the BST

varactors. However, tunability of ~50 % was obtained in the sample annealed in air. For practicality, tunability of at least 50 % and Q-factor of minimum 20 can readily compete with other established silicon and MEMS technologies and this was achieved with the BST varactor of strain-relaxed films.

6.2 Low Third-Order Intermodulation Distortion in BST Thin Film Varactors

The author has investigated the first important device parameter which was linearity of the BST thin film varactors. A novel method for the theoretical analysis of the IM_3 in BST thin film IDCs fabricated on an r-plane sapphire substrate was established. The BST thin films on r-plane sapphire substrates were initially deposited using pulse laser deposition (PLD) technique and tunability of ~43 % and Q_{min} of 13.4 were achieved.

A polynomial equation was derived from this measured *C-V* curve and converted into the general nonlinear capacitor equation. The important coefficient values obtained were then substituted into the well-known IM_3 theoretical model for varactor diodes, which was found to be ideal for the BST varactor analysis. The IM_3 equation, however, was slightly modified by redefining it in terms of the average power, P_{av} to perfectly match the simulated data. The exclusion of the inductance values from the mathematical expansions of this equation were also necessary to implement the two circuit topologies proposed, the "dual" and "series dual" BST varactor circuits for linearity improvement.

For both circuit topologies, the IM_3 theoretical model and simulated results showed excellent agreement. Significant low nulls were achieved compared to the single BST varactor circuit topology when biased up to ±40 V. In the series dual topology, the entire IM_3

level dropped significantly with 13 dB linearity improvements at 0 V compared to the single and dual topologies. Low IM_3 were also experimentally demonstrated where the measured first nulls were achieved at ±13 V and ±20 V for the dual and series dual topologies respectively. The voltage shifts were caused by the degradation of their tunabilities due to the compression of their *C-V* curves. The IM_3 levels in both topologies were also degraded due to the parasitic inductances caused by the bondwires. However, these results demonstrated the potential for incorporating these highly linear BST varactors in SoS technology.

6.3 BST Thin Film Varactors with High 1 dB compression points

The author has investigated the second important device parameter which was power handling capability of the BST thin film varactors. The relationship between the tunability and the 1 dB compression point of the BST varactor was established. The BST IDC was initially modelled using CST software with specified parameter values based on the measured devices fabricated on a c-plane sapphire substrate. Parametric analysis was demonstrated by analysing the effects of varying the IDC geometry (which includes finger gap, finger width, finger length and number of fingers) on the shape of the *C-V* curves.

The optimised *C-V* curves were determined with the narrow, broad and intermediate curves producing tunabilities of 73 %, 28 % and 54 % respectively. All the *C-V* curves data were compared to the established nonlinear BST model using the curve-fitting function in MATLAB and important parameter values were extracted. The model along with the parameter values were subsequently implemented in a nonlinear equation-based capacitor of a two-port series network designed in ADS software. Simulations were performed and the 1 dB

compression points at input power for the narrow, broad and intermediate were determined at 29 dBm, 32 dBm and 41 dBm respectively. The relationship was established: the varactor with the highest tunability was compensated by having the lowest 1 dB compression point and varactor with the lowest tunability produced the highest 1 dB compression point.

The optimised *C-V* curves were realised in the physical form of varactors. The narrow, broad and intermediate varactors were fabricated on BST grown on c-plane sapphire substrate. The 1 dB compression points achieved were comparable to the simulated results even though a slight reduced thickness was identified as one of the major constraints.

6.4 Future work

There are several opportunities for potential future work identified by the author as summarised below.

- It is possible to reduce the effect of parasitic inductances resulting from the multiple bondwires used in the dual and series dual BST varactor circuit topologies through a microfabrication process. The whole device structure of both topologies could be fabricated and integrated on a single chip. This would not only downscale the size of the device but also save space and cost.

- The highly linear BST thin film varactors achieved could be integrated with tunable microwave devices such as a bandpass filter. The linearity performance of the filter could be improved at the desired frequency range by properly tuning the biasing voltages of the varactors. This filter could potentially replace several fixed microwave devices in the RF front-end where highly linear reconfigurable circuits are crucial in both transmit and receive applications.

- The uniformity of the BST thin film plays a significant role in the performance of varactors. Non-uniform thin film would result in different tunability and Q-factor for varactors fabricated on the same wafer. Some confidence can be achieved from the sputtered BST layer on c-plane sapphire substrates as demonstrated by the author, which consistently produced ~400 nm thickness in all samples for several deposition runs. A feasible deposition process that could reproduce high quality BST thin films, i.e. smooth and dense with minimal defects, is needed to obtain enhanced dielectric properties that are consistent across a single wafer and between wafer lots [1].

- The integration of BST thin films with semiconductor technologies via the SoS process is an interesting topic which requires extensive investigation. The successful deposition of BST thin films on a very thin layer of Si (~100 nm) grown on r-plane sapphire substrate [153] could pave the way for the integration of reconfigurable BST microwave devices with SoS technology in the near future.

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Appendix A

MATLAB Code for Capacitance and Q-factor Extraction from Measured S-parameter Data

```
% Extract frequency dependent R,C from S-parameter data
 C_i = 0.1; % capacitance guesstimate in pF

L_i = 0.1; % inductance guesstimate in nH

R_i = 0.1; % 1 Ohm guesstimate

Z_o = 50;


% Parasitic values

C_p = 0.0022; % pad parasitic capacitance in pF

L_p = 0.0317; % pad parasitic inductance in nH

R_p = 0.1650; % pad equivalent resistance in Ohms
```

```matlab
 NumPoints = 1601; % number of points in s2p file


%Read input file

fid=fopen('A1UM140V.txt','r');

[freq,s11_m,s11_a,s12_m,s12_a,s21_m,s21_a,s22_m,s22_a]=textread('A1UM140V.txt','%f%

f%f%f%f%f%f%f%f',-1);

fclose(fid);


%s11_dB=10*log10(1./((s11_m).^2));

%s11_cplx=s11_m.*exp(j.*(pi/180)*s11_a); %port 1

s11_dB=10*log10(1./((s22_m).^2));

s11_cplx=s22_m.*exp(j.*(pi/180)*s22_a); %port 2


R_vec=zeros(1,1601);

C_vec=zeros(1,1601);

Q_vec=zeros(1,1601);


for(index=1:NumPoints)

r=real(s11_cplx(index,1));

i=imag(s11_cplx(index,1));

z_r=real( Z_o*(1+s11_cplx(index,1))/(1-s11_cplx(index,1)) );

z_i=imag( Z_o*(1+s11_cplx(index,1))/(1-s11_cplx(index,1)) );

y_r=real( (1/Z_o)*(1-s11_cplx(index,1))/(1+s11_cplx(index,1)) );

y_i=imag( (1/Z_o)*(1-s11_cplx(index,1))/(1+s11_cplx(index,1)) );

omega=2*pi*freq(index,1)*1E+9;

'V=[R;C]'; % Open, DUT
```

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```
%'V=[R;L]'; % Short


% Open Standard

%F=inline('[((1+(((V(2)/1E+12).^2)*(omega.^2)*((V(1).^2)-

(Z_o.^2))))/(1+(omega.*(V(2)/1E+12)*(V(1)+Z_o)).^2))-r;(((-

2*omega.*(V(2)/1E+12).*Z_o)./(1+(omega.*(V(2)/1E+12).*(V(1)+Z_o)).^2)))-

i]','V','omega','Z_o','r','i');

%InitialGuess=[R_i;C_i];

%Options = optimset('TolX',1E-10,'TolFun',1E-8);

%XY=fsolve(F, InitialGuess, Options, omega,Z_o,r,i);


%Short Standard

%F=inline('[((V(1))/( (1-

(omega.^2)*(V(2)/1E+9)*C_p/1E+12).^2+(omega*V(1)*C_p/1E+12).^2 ))-z_r;((

omega*(V(2)/1E+9) - omega*(V(1).^2)*(C_p/1E+12)-

(omega.^3)*((V(2)/1E+9).^2)*C_p/1E+12 )./( (1-(omega.^2)*(V(2)/1E+9)*C_p/1E+12).^2 +

(omega*V(1)*C_p/1E+12).^2 ) )-z_i]','V','omega','C_p','z_r','z_i');

%F=inline('[((V(1))/( (V(1)).^2 +(omega*V(2)/1E+9).^2 ))-y_r;((omega*C_p/1E+12)+(( -

omega*(V(2)/1E+9) )./( (V(1)).^2 + (omega*V(2)/1E+9).^2 )) )-

y_i]','V','omega','C_p','y_r','y_i');

%InitialGuess=[R_i;L_i];

%Options = optimset('TolX',1E-10,'TolFun',1E-8);

%XY=fsolve(F, InitialGuess, Options, omega,C_p,y_r,y_i);

 % DUT

F=inline('[(((omega.^2)*(R_p+V(1))*((V(2)/1E+12).^2))/((1-

(omega.^2)*(L_p/1E+9)*(V(2)/1E+12)).^2+(omega*(R_p+V(1))*(V(2)/1E+12)).^2))-
```

```matlab
y_r;((omega*(C_p/1E+12))+((omega*(V(2)/1E+12)-

(omega.^3)*(L_p/1E+9)*(V(2)/1E+12).^2 )/((1-

(omega.^2)*(L_p/1E+9)*(V(2)/1E+12)).^2+(omega*(R_p+V(1))*(V(2)/1E+12)).^2)))-

y_i]','V','omega','R_p','L_p','C_p','y_r','y_i');

InitialGuess=[R_i;L_i];

Options=optimset('TolX',1E-10,'TolFun',1E-12);

XY=fsolve(F,InitialGuess,Options,omega,R_p,L_p,C_p,y_r,y_i);


R_vec(1,index)=XY(1,1);

C_vec(1,index)=XY(2,1);

Q_vec(1,index)=1/(omega*XY(1,1)*(XY(2,1)/1E12));

Z_vec(index,1)=(1/Z_o)*((XY(1,1)+1/(j*omega*(XY(2,1)/1E12))));

end
```

Appendix B

MAPLE code

B.1 Single and Dual BST Varactor Circuit Topologies

#Compute IM$_3$ **for** *IDEAL single*

    and *dual BST varactor circuit topologies with matched varactors*

#From curve-fitting method, the polynomial equation which is fitted well to the previous C-V

    data is given by $M{=}K_o + K_2 \cdot \left(V_{dc} + v_{ac}\right)^2 + K_4 \cdot \left(V_{dc} + v_{ac}\right)^4 + K_6 \cdot \left(V_{dc} + v_{ac}\right)^6 + K_8$

    $\cdot \left(V_{dc} + v_{ac}\right)^8 + K_{10} \cdot \left(V_{dc} + v_{ac}\right)^{10} + K_{12} \cdot \left(V_{dc} + v_{ac}\right)^{12} + K_{14} \cdot \left(V_{dc} + v_{ac}\right)^{14} + K_{16}$

    $\cdot \left(V_{dc} + v_{ac}\right)^{16}$

#SINGLE TOPOLOGY

#Thus, substituting $K_0 = 0.2967 \cdot 10^{-12}, K_2 = -0.0500736 \cdot 10^{-2} \cdot 10^{-12}, K_4 = 0.017041 \cdot 10^{-4}$

    $\cdot 10^{-12}, K_6 = -0.0043504 \cdot 10^{-6} \cdot 10^{-12}, K_8 = 0.000727689 \cdot 10^{-8} \cdot 10^{-12}, K_{10} = -7.6121 \cdot 10^{-5}$

    $\cdot 10^{-10} \cdot 10^{-12}, K_{12} = 4.76768 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12}, K_{14} = -1.62953 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12} \& K_{16}$

    $= 2.33225 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12}$ **in** *equation* M_1 *yields* :

$$M := 0.2967 \cdot 10^{-12} - 0.0500736 \cdot 10^{-2} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^2 + 0.017041 \cdot 10^{-4} \cdot 10^{-12} \cdot \left(V_{dc}\right.$$
$$\left.+ v_{ac}\right)^4 - 0.0043504 \cdot 10^{-6} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^6 + 0.000727689 \cdot 10^{-8} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^8$$
$$- 7.6121 \cdot 10^{-5} \cdot 10^{-10} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^{10} + 4.76768 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^{12}$$
$$- 1.62953 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^{14} + 2.33225 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^{16}$$

$$2.967000000\,10^{-13} - 5.007360000\,10^{-16} \left(V_{dc} + v_{ac}\right)^2 + 1.704100000\,10^{-18} \left(V_{dc} + v_{ac}\right)^4$$
$$- 4.350400000\,10^{-21} \left(V_{dc} + v_{ac}\right)^6 + 7.276890000\,10^{-24} \left(V_{dc} + v_{ac}\right)^8$$
$$- 7.612100000\,10^{-27} \left(V_{dc} + v_{ac}\right)^{10} + 4.767680000\,10^{-30} \left(V_{dc} + v_{ac}\right)^{12}$$
$$- 1.629530000\,10^{-33} \left(V_{dc} + v_{ac}\right)^{14} + 2.332250000\,10^{-37} \left(V_{dc} + v_{ac}\right)^{16}$$

#From M, we could extract the coefficients, C_0 **to** *C_4*
to *satisfy the term which represents the capacitance C of a varactor, $C(v) = C_0 + C_1 v_{ac}$*
$+ C_2 v_{ac}^2 + C_3 v_{ac}^3 + C_4 v_{ac}^4 + \ldots\ldots$

#Hence, the extracted coefficients, C_0 **to** *C_4 which are dependent of V_{dc} are given* **by:**

$C_0 := coeff\left(M, v[ac], 0\right)$
$$2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18}\,V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6$$
$$+ 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10} + 4.767680000\,10^{-30}\,V_{dc}^{12}$$
$$- 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16}$$

$C_1 := coeff\left(M, v[ac], 1\right)$
$$- 1.001472000\,10^{-15}\,V_{dc} + 6.816400000\,10^{-18}\,V_{dc}^3 - 2.610240000\,10^{-20}\,V_{dc}^5$$
$$+ 5.821512000\,10^{-23}\,V_{dc}^7 - 7.612100000\,10^{-26}\,V_{dc}^9 + 5.721216000\,10^{-29}\,V_{dc}^{11}$$
$$- 2.281342000\,10^{-32}\,V_{dc}^{13} + 3.731600000\,10^{-36}\,V_{dc}^{15}$$

$C_2 := coeff\left(M, v[ac], 2\right)$
$$- 5.007360000\,10^{-16} + 1.022460000\,10^{-17}\,V_{dc}^2 - 6.525600000\,10^{-20}\,V_{dc}^4 + 2.037529200\,10^{-22}$$
$$V_{dc}^6 - 3.425445000\,10^{-25}\,V_{dc}^8 + 3.146668800\,10^{-28}\,V_{dc}^{10} - 1.482872300\,10^{-31}\,V_{dc}^{12}$$
$$+ 2.798700000\,10^{-35}\,V_{dc}^{14}$$

$C_3 := coeff\left(M, v[ac], 3\right)$
$$6.816400000\,10^{-18}\,V_{dc} - 8.700800000\,10^{-20}\,V_{dc}^3 + 4.075058400\,10^{-22}\,V_{dc}^5 - 9.134520000\,10^{-25}$$
$$V_{dc}^7 + 1.048889600\,10^{-27}\,V_{dc}^9 - 5.931489200\,10^{-31}\,V_{dc}^{11} + 1.306060000\,10^{-34}\,V_{dc}^{13}$$

$C_4 := coeff\left(M, v[ac], 4\right)$

$$1.704100000\,10^{-18} - 6.525600000\,10^{-20}\,V_{dc}^2 + 5.093823000\,10^{-22}\,V_{dc}^4 - 1.598541000\,10^{-24}\,V_{dc}^6$$
$$+ 2.360001600\,10^{-27}\,V_{dc}^8 - 1.631159530\,10^{-30}\,V_{dc}^{10} + 4.244695000\,10^{-34}\,V_{dc}^{12}$$

#**DUAL TOPOLOGY**

#*Thus, substituting* $K_0 = 0.2967 \cdot 10^{-12}, K_2 = -0.0500736 \cdot 10^{-2} \cdot 10^{-12}, K_4 = 0.017041 \cdot 10^{-4}$
$\cdot 10^{-12}, K_6 = -0.0043504 \cdot 10^{-6} \cdot 10^{-12}, K_8 = 0.000727689 \cdot 10^{-8} \cdot 10^{-12}, K_{10} = -7.6121 \cdot 10^{-5}$
$\cdot 10^{-10} \cdot 10^{-12}, K_{12} = 4.76768 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12}, K_{14} = -1.62953 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12}\, \& \, K_{16}$
$= 2.33225 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12}$ **in** *equation* M_1 *yields* :

$$M_1 := \frac{0.2967 \cdot 10^{-12}}{2} - \frac{0.0500736 \cdot 10^{-2} \cdot 10^{-12}}{2} \cdot \left(V_{dc} + v_{ac}\right)^2 + \frac{0.017041 \cdot 10^{-4} \cdot 10^{-12}}{2} \cdot \left(V_{dc}\right.$$
$$+ v_{ac})^4 - \frac{0.0043504 \cdot 10^{-6} \cdot 10^{-12}}{2} \cdot \left(V_{dc} + v_{ac}\right)^6 + \frac{0.000727689 \cdot 10^{-8} \cdot 10^{-12}}{2} \cdot \left(V_{dc}\right.$$
$$+ v_{ac})^8 - \frac{7.6121 \cdot 10^{-5} \cdot 10^{-10} \cdot 10^{-12}}{2} \cdot \left(V_{dc} + v_{ac}\right)^{10} + \frac{4.76768 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12}}{2}$$
$$\cdot \left(V_{dc} + v_{ac}\right)^{12} - \frac{1.62953 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12}}{2} \cdot \left(V_{dc} + v_{ac}\right)^{14}$$
$$+ \frac{2.33225 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12}}{2} \cdot \left(V_{dc} + v_{ac}\right)^{16}$$

$$1.483500000\,10^{-13} - 2.503680000\,10^{-16}\left(V_{dc} + v_{ac}\right)^2 + 8.520500000\,10^{-19}\left(V_{dc} + v_{ac}\right)^4$$
$$- 2.175200000\,10^{-21}\left(V_{dc} + v_{ac}\right)^6 + 3.638445000\,10^{-24}\left(V_{dc} + v_{ac}\right)^8$$
$$- 3.806050000\,10^{-27}\left(V_{dc} + v_{ac}\right)^{10} + 2.383840000\,10^{-30}\left(V_{dc} + v_{ac}\right)^{12}$$
$$- 8.147650000\,10^{-34}\left(V_{dc} + v_{ac}\right)^{14} + 1.166125000\,10^{-37}\left(V_{dc} + v_{ac}\right)^{16}$$

#*Thus, substituting* $K_0 = 0.2967 \cdot 10^{-12}, K_2 = -0.0500736 \cdot 10^{-2} \cdot 10^{-12}, K_4 = 0.017041 \cdot 10^{-4}$
$\cdot 10^{-12}, K_6 = -0.0043504 \cdot 10^{-6} \cdot 10^{-12}, K_8 = 0.000727689 \cdot 10^{-8} \cdot 10^{-12}, K_{10} = -7.6121 \cdot 10^{-5}$
$\cdot 10^{-10} \cdot 10^{-12}, K_{12} = 4.76768 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12}, K_{14} = -1.62953 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12}\, \& \, K_{16}$
$= 2.33225 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12}$ **in** *equation* M_2 *yields* :

$$M_2 := \frac{0.2967 \cdot 10^{-12}}{2} - \frac{0.0500736 \cdot 10^{-2} \cdot 10^{-12}}{2} \cdot \left(-V_{dc} + v_{ac}\right)^2 + \frac{0.017041 \cdot 10^{-4} \cdot 10^{-12}}{2} \cdot \big($$
$$-V_{dc} + v_{ac})^4 - \frac{0.0043504 \cdot 10^{-6} \cdot 10^{-12}}{2} \cdot \left(-V_{dc} + v_{ac}\right)^6 + \frac{0.000727689 \cdot 10^{-8} \cdot 10^{-12}}{2}$$
$$\cdot \left(-V_{dc} + v_{ac}\right)^8 - \frac{7.6121 \cdot 10^{-5} \cdot 10^{-10} \cdot 10^{-12}}{2} \cdot \left(-V_{dc} + v_{ac}\right)^{10}$$
$$+ \frac{4.76768 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12}}{2} \cdot \left(-V_{dc} + v_{ac}\right)^{12} - \frac{1.62953 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12}}{2} \cdot \big($$
$$-V_{dc} + v_{ac})^{14} + \frac{2.33225 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12}}{2} \cdot \left(-V_{dc} + v_{ac}\right)^{16}$$

$$1.483500000\ 10^{-13} - 2.503680000\ 10^{-16}\left(-V_{dc} + v_{ac}\right)^2 + 8.520500000\ 10^{-19}\left(-V_{dc} + v_{ac}\right)^4$$
$$- 2.175200000\ 10^{-21}\left(-V_{dc} + v_{ac}\right)^6 + 3.638445000\ 10^{-24}\left(-V_{dc} + v_{ac}\right)^8$$
$$- 3.806050000\ 10^{-27}\left(-V_{dc} + v_{ac}\right)^{10} + 2.383840000\ 10^{-30}\left(-V_{dc} + v_{ac}\right)^{12}$$
$$- 8.147650000\ 10^{-34}\left(-V_{dc} + v_{ac}\right)^{14} + 1.166125000\ 10^{-37}\left(-V_{dc} + v_{ac}\right)^{16}$$

$M_3 := M_1 + M_2$

$$2.967000000\ 10^{-13} - 2.503680000\ 10^{-16}\left(V_{dc} + v_{ac}\right)^2 + 8.520500000\ 10^{-19}\left(V_{dc} + v_{ac}\right)^4$$
$$- 2.175200000\ 10^{-21}\left(V_{dc} + v_{ac}\right)^6 + 3.638445000\ 10^{-24}\left(V_{dc} + v_{ac}\right)^8$$
$$- 3.806050000\ 10^{-27}\left(V_{dc} + v_{ac}\right)^{10} + 2.383840000\ 10^{-30}\left(V_{dc} + v_{ac}\right)^{12}$$
$$- 8.147650000\ 10^{-34}\left(V_{dc} + v_{ac}\right)^{14} + 1.166125000\ 10^{-37}\left(V_{dc} + v_{ac}\right)^{16}$$
$$- 2.503680000\ 10^{-16}\left(-V_{dc} + v_{ac}\right)^2 + 8.520500000\ 10^{-19}\left(-V_{dc} + v_{ac}\right)^4$$
$$- 2.175200000\ 10^{-21}\left(-V_{dc} + v_{ac}\right)^6 + 3.638445000\ 10^{-24}\left(-V_{dc} + v_{ac}\right)^8$$
$$- 3.806050000\ 10^{-27}\left(-V_{dc} + v_{ac}\right)^{10} + 2.383840000\ 10^{-30}\left(-V_{dc} + v_{ac}\right)^{12}$$
$$- 8.147650000\ 10^{-34}\left(-V_{dc} + v_{ac}\right)^{14} + 1.166125000\ 10^{-37}\left(-V_{dc} + v_{ac}\right)^{16}$$

#From M_3, we could extract the coefficients, C_0 **to** C_4
   to satisfy the term which represents the capacitance C of dual BST varactors configuration,
   $$C(v) = C_0 + C_1 v_{ac} + C_2 v_{ac}^2 + C_3 v_{ac}^3 + C_4 v_{ac}^4 + \ldots\ldots$$

#Hence, the extracted coefficients, C_0 **to** C_4 which are dependent of V_{dc} are given **by**:

$C0 := coeff\left(M_3, v[ac], 0\right)$

$$2.967000000\ 10^{-13} - 5.007360000\ 10^{-16} V_{dc}^2 + 1.704100000\ 10^{-18} V_{dc}^4 - 4.350400000\ 10^{-21} V_{dc}^6$$
$$+ 7.276890000\ 10^{-24} V_{dc}^8 - 7.612100000\ 10^{-27} V_{dc}^{10} + 4.767680000\ 10^{-30} V_{dc}^{12}$$
$$- 1.629530000\ 10^{-33} V_{dc}^{14} + 2.332250000\ 10^{-37} V_{dc}^{16}$$

$C1 := coeff\left(M_3, v[ac], 1\right)$

$$0.$$

$C2 := coeff\left(M_3, v[ac], 2\right)$

$$-5.007360000\ 10^{-16} + 1.022460000\ 10^{-17} V_{dc}^2 - 6.525600000\ 10^{-20} V_{dc}^4 + 2.037529200\ 10^{-22}$$
$$V_{dc}^6 - 3.425445000\ 10^{-25} V_{dc}^8 + 3.146668800\ 10^{-28} V_{dc}^{10} - 1.482872300\ 10^{-31} V_{dc}^{12}$$
$$+ 2.798700000\ 10^{-35} V_{dc}^{14}$$

$C3 = coeff\left(M_3, v[ac], 3\right)$

$$C3 = 0.$$

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$$C4 = coeff\left(M_3, v[ac], 4\right)$$

$$C4 = 1.704100000\,10^{-18} - 6.525600000\,10^{-20}\,V_{dc}^2 + 5.093823000\,10^{-22}\,V_{dc}^4$$
$$- 1.598541000\,10^{-24}\,V_{dc}^6 + 2.360001600\,10^{-27}\,V_{dc}^8 - 1.631159530\,10^{-30}\,V_{dc}^{10}$$
$$+ 4.244695000\,10^{-34}\,V_{dc}^{12}$$

#*The modified first-order terms **without the value of L**, with two input frequencies, $\omega_a = 2\cdot\pi$
$\cdot 1.81\ GHz = 11.37404\ GHz$ & $\omega_b = 2\cdot\pi\cdot 1.8\ GHz = 11.3112\ GHz$ & $R = 50\ \Omega$ are given* **by**:

#**SINGLE TOPOLOGY**

$$A_1\left(j\omega_a\right) := \cfrac{1}{\cfrac{1}{50} + I\cdot 11.37404\cdot 10^9\cdot C_0}$$
$$1\Big/\left(\frac{1}{50} + 1.137404000\,10^{10}\,I\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2\right.\right.$$
$$+ 1.704100000\,10^{-18}\,V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8$$
$$- 7.612100000\,10^{-27}\,V_{dc}^{10} + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14}$$
$$\left.\left.+ 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)$$

$$A_1\left(-j\omega_b\right) := \cfrac{1}{\cfrac{1}{50} - I\cdot 11.3112\cdot 10^9\cdot C_0}$$
$$1\Big/\left(\frac{1}{50} - 1.131120000\,10^{10}\,I\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2\right.\right.$$
$$+ 1.704100000\,10^{-18}\,V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8$$
$$- 7.612100000\,10^{-27}\,V_{dc}^{10} + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14}$$
$$\left.\left.+ 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)$$

$$A_1\left(j\omega_b\right) := \cfrac{1}{\cfrac{1}{50} + I\cdot 11.3112\cdot 10^9\cdot C_0}$$
$$1\Big/\left(\frac{1}{50} + 1.131120000\,10^{10}\,I\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2\right.\right.$$
$$+ 1.704100000\,10^{-18}\,V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8$$
$$- 7.612100000\,10^{-27}\,V_{dc}^{10} + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14}$$
$$\left.\left.+ 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)$$

#*DUAL TOPOLOGY*

$$A1\left(j\omega_a\right) := \cfrac{1}{\dfrac{1}{50} + \text{I}\cdot 11.37404\cdot 10^9\cdot C0}$$

$$1\Big/\left(\frac{1}{50} + 1.137404000\,10^{10}\,\text{I}\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2\right.\right.$$
$$+ 1.704100000\,10^{-18}\,V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8$$
$$- 7.612100000\,10^{-27}\,V_{dc}^{10} + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14}$$
$$\left.\left. + 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)$$

$$A1\left(-j\omega_b\right) := \cfrac{1}{\dfrac{1}{50} - \text{I}\cdot 11.3112\cdot 10^9\cdot C0}$$

$$1\Big/\left(\frac{1}{50} - 1.131120000\,10^{10}\,\text{I}\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2\right.\right.$$
$$+ 1.704100000\,10^{-18}\,V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8$$
$$- 7.612100000\,10^{-27}\,V_{dc}^{10} + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14}$$
$$\left.\left. + 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)$$

$$A1\left(j\omega_b\right) := \cfrac{1}{\dfrac{1}{50} + \text{I}\cdot 11.3112\cdot 10^9\cdot C0}$$

$$1\Big/\left(\frac{1}{50} + 1.131120000\,10^{10}\,\text{I}\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2\right.\right.$$
$$+ 1.704100000\,10^{-18}\,V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8$$
$$- 7.612100000\,10^{-27}\,V_{dc}^{10} + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14}$$
$$\left.\left. + 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)$$

#*The modified second-order terms **without the value of L** :*

#*SINGLE TOPOLOGY*

$$A_2\left(j\omega_a, j\omega_a\right) := -\left(\cfrac{\dfrac{C_1}{2}\cdot 2\cdot\text{I}\cdot 11.37404\cdot 10^9\cdot A_1\left(j\omega_a\right)^2}{\dfrac{1}{50} + 2\cdot\text{I}\cdot 11.37404\cdot 10^9\cdot C_0}\right)$$

$$-\left(1.137404000\,10^{10}\,\mathrm{I}\left(-1.001472000\,10^{-15}\,V_{dc}+6.816400000\,10^{-18}\,V_{dc}^3-2.610240000\,10^{-20}\right.\right.$$

$$V_{dc}^5+5.821512000\,10^{-23}\,V_{dc}^7-7.612100000\,10^{-26}\,V_{dc}^9+5.721216000\,10^{-29}\,V_{dc}^{11}$$

$$\left.\left.-2.281342000\,10^{-32}\,V_{dc}^{13}+3.731600000\,10^{-36}\,V_{dc}^{15}\right)\right)\Big/\left(\left(\frac{1}{50}\right.\right.$$

$$+1.137404000\,10^{10}\,\mathrm{I}\left(2.967000000\,10^{-13}-5.007360000\,10^{-16}\,V_{dc}^2+1.704100000\,10^{-18}\right.$$

$$V_{dc}^4-4.350400000\,10^{-21}\,V_{dc}^6+7.276890000\,10^{-24}\,V_{dc}^8-7.612100000\,10^{-27}\,V_{dc}^{10}$$

$$\left.\left.+4.767680000\,10^{-30}\,V_{dc}^{12}-1.629530000\,10^{-33}\,V_{dc}^{14}+2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)^2\left(\frac{1}{50}\right.$$

$$+2.274808000\,10^{10}\,\mathrm{I}\left(2.967000000\,10^{-13}-5.007360000\,10^{-16}\,V_{dc}^2+1.704100000\,10^{-18}\right.$$

$$V_{dc}^4-4.350400000\,10^{-21}\,V_{dc}^6+7.276890000\,10^{-24}\,V_{dc}^8-7.612100000\,10^{-27}\,V_{dc}^{10}$$

$$\left.\left.\left.+4.767680000\,10^{-30}\,V_{dc}^{12}-1.629530000\,10^{-33}\,V_{dc}^{14}+2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)\right)$$

$$A_2\left(j\omega_a,-j\omega_b\right):=-\left(\frac{\dfrac{C_1}{2}\cdot\left(\mathrm{I}\cdot11.37404\cdot10^9-\mathrm{I}\cdot11.3112\cdot10^9\right)\cdot A_1\left(j\omega_a\right)\cdot A_1\left(-j\omega_b\right)}{\dfrac{1}{50}+\left(\mathrm{I}\cdot11.37404\cdot10^9-\mathrm{I}\cdot11.3112\cdot10^9\right)\cdot C_0}\right)$$

$$-\left(3.142000000\,10^{7}\,\mathrm{I}\left(-1.001472000\,10^{-15}\,V_{dc}+6.816400000\,10^{-18}\,V_{dc}^3-2.610240000\,10^{-20}\right.\right.$$

$$V_{dc}^5+5.821512000\,10^{-23}\,V_{dc}^7-7.612100000\,10^{-26}\,V_{dc}^9+5.721216000\,10^{-29}\,V_{dc}^{11}$$

$$\left.\left.-2.281342000\,10^{-32}\,V_{dc}^{13}+3.731600000\,10^{-36}\,V_{dc}^{15}\right)\right)\Big/\left(\left(\frac{1}{50}\right.\right.$$

$$+1.137404000\,10^{10}\,\mathrm{I}\left(2.967000000\,10^{-13}-5.007360000\,10^{-16}\,V_{dc}^2+1.704100000\,10^{-18}\right.$$

$$V_{dc}^4-4.350400000\,10^{-21}\,V_{dc}^6+7.276890000\,10^{-24}\,V_{dc}^8-7.612100000\,10^{-27}\,V_{dc}^{10}$$

$$\left.\left.+4.767680000\,10^{-30}\,V_{dc}^{12}-1.629530000\,10^{-33}\,V_{dc}^{14}+2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)\left(\frac{1}{50}\right.$$

$$-1.131120000\,10^{10}\,\mathrm{I}\left(2.967000000\,10^{-13}-5.007360000\,10^{-16}\,V_{dc}^2+1.704100000\,10^{-18}\right.$$

$$V_{dc}^4-4.350400000\,10^{-21}\,V_{dc}^6+7.276890000\,10^{-24}\,V_{dc}^8-7.612100000\,10^{-27}\,V_{dc}^{10}$$

$$\left.\left.+4.767680000\,10^{-30}\,V_{dc}^{12}-1.629530000\,10^{-33}\,V_{dc}^{14}+2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)\left(\frac{1}{50}\right.$$

$$+6.284000\,10^{7}\,\mathrm{I}\left(2.967000000\,10^{-13}-5.007360000\,10^{-16}\,V_{dc}^2+1.704100000\,10^{-18}\,V_{dc}^4\right.$$

$$-4.350400000\,10^{-21}\,V_{dc}^6+7.276890000\,10^{-24}\,V_{dc}^8-7.612100000\,10^{-27}\,V_{dc}^{10}$$

$$\left.\left.\left.+4.767680000\,10^{-30}\,V_{dc}^{12}-1.629530000\,10^{-33}\,V_{dc}^{14}+2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)\right)$$

#DUAL TOPOLOGY

$$A2\left(j\omega_a, j\omega_a\right) := -\left(\frac{\dfrac{C1}{2}\cdot 2\cdot I\cdot 11.37404\cdot 10^9\cdot A1\left(j\omega_a\right)^2}{\dfrac{1}{50} + 2\cdot I\cdot 11.37404\cdot 10^9\cdot C0}\right)$$

$$-0.\,I$$

$$A2\left(j\omega_a, -j\omega_b\right) := -\left(\frac{\dfrac{C1}{2}\cdot \left(I\cdot 11.37404\cdot 10^9 - I\cdot 11.3112\cdot 10^9\right)\cdot A1\left(j\omega_a\right)\cdot A1\left(-j\omega_b\right)}{\dfrac{1}{50} + \left(I\cdot 11.37404\cdot 10^9 - I\cdot 11.3112\cdot 10^9\right)\cdot C0}\right)$$

$$-0.\,I$$

#The modified third-order terms **without the value of L** at frequency $\left(2\omega_a - \omega_b\right)$:

#SINGLE TOPOLOGY

$$T := \frac{1}{3}\cdot\left(2\cdot A_1\left(j\omega_a\right)\cdot A_2\left(j\omega_a, -j\omega_b\right) + A_1\left(-j\omega_b\right)\cdot A_2\left(j\omega_a, j\omega_a\right)\right)$$

$$-\left(2.094666667\,10^7\,I\left(-1.001472000\,10^{-15}\,V_{dc} + 6.816400000\,10^{-18}\,V_{dc}^3 - 2.610240000\,10^{-20}\right.\right.$$
$$V_{dc}^5 + 5.821512000\,10^{-23}\,V_{dc}^7 - 7.612100000\,10^{-26}\,V_{dc}^9 + 5.721216000\,10^{-29}\,V_{dc}^{11}$$
$$\left.\left.- 2.281342000\,10^{-32}\,V_{dc}^{13} + 3.731600000\,10^{-36}\,V_{dc}^{15}\right)\right)\bigg/\left(\left(\left(\frac{1}{50}\right.\right.\right.$$
$$+ 1.137404000\,10^{10}\,I\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18}\right.$$
$$V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10}$$
$$\left.+ 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\bigg)^2\left(\frac{1}{50}\right.$$
$$- 1.131120000\,10^{10}\,I\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18}\right.$$
$$V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10}$$
$$\left.+ 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\bigg)\left(\frac{1}{50}\right.$$
$$+ 6.284000\,10^7\,I\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18}\,V_{dc}^4\right.$$
$$- 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10}$$
$$\left.\left.+ 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)$$
$$- \left(3.791346666\,10^9\,I\left(-1.001472000\,10^{-15}\,V_{dc} + 6.816400000\,10^{-18}\,V_{dc}^3 - 2.610240000\right.\right.$$
$$- 1.131120000\,10^{10}\,I\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18}\right.$$
$$V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10}$$
$$\left.+ 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\bigg)\left(\frac{1}{50}\right.$$
$$+ 1.137404000\,10^{10}\,I\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18}\right.$$
$$V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10}$$
$$\left.+ 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\bigg)^2\left(\frac{1}{50}\right.$$
$$+ 2.274808000\,10^{10}\,I\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18}\right.$$
$$V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10}$$
$$\left.\left.+ 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16}\right)\right)\bigg)$$

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$$A_3\left(j\omega_a, j\omega_a, -j\omega_b\right) :=$$

$$-\left(\frac{\left(2\cdot I\cdot 11.37404\cdot 10^9 - I\cdot 11.3112\cdot 10^9\right)\cdot\left(C_1\cdot T + \dfrac{C_2}{3}\cdot A_1\left(j\omega_a\right)^2\cdot A_1\left(-j\omega_b\right)\right)}{\dfrac{1}{50} + \left(2\cdot I\cdot 11.37404\cdot 10^9 - I\cdot 11.3112\cdot 10^9\right)\cdot C_0}\right)$$

#DUAL TOPOLOGY

$$U := \frac{1}{3}\cdot\left(2\cdot A1\left(j\omega_a\right)\cdot A2\left(j\omega_a, -j\omega_b\right) + A1\left(-j\omega_b\right)\cdot A2\left(j\omega_a, j\omega_a\right)\right)$$
$$-0.\,I$$

$$A3\left(j\omega_a, j\omega_a, -j\omega_b\right) :=$$

$$-\left(\frac{\left(2\cdot I\cdot 11.37404\cdot 10^9 - I\cdot 11.3112\cdot 10^9\right)\cdot\left(C1\cdot U + \dfrac{C2}{3}\cdot A1\left(j\omega_a\right)^2\cdot A1\left(-j\omega_b\right)\right)}{\dfrac{1}{50} + \left(2\cdot I\cdot 11.37404\cdot 10^9 - I\cdot 11.3112\cdot 10^9\right)\cdot C0}\right)$$

$$-\left(3.812293333\ 10^9\ I\left(-5.007360000\ 10^{-16} + 1.022460000\ 10^{-17}\ V_{dc}^2 - 6.525600000\ 10^{-20}\ V_{dc}^4\right.\right.$$
$$+ 2.037529200\ 10^{-22}\ V_{dc}^6 - 3.425445000\ 10^{-25}\ V_{dc}^8 + 3.146668800\ 10^{-28}\ V_{dc}^{10}$$
$$\left.- 1.482872300\ 10^{-31}\ V_{dc}^{12} + 2.798700000\ 10^{-35}\ V_{dc}^{14}\right)\Bigg/\left(\left(\frac{1}{50}\right.\right.$$
$$+ 1.137404000\ 10^{10}\ I\left(2.967000000\ 10^{-13} - 5.007360000\ 10^{-16}\ V_{dc}^2 + 1.704100000\ 10^{-18}\right.$$
$$V_{dc}^4 - 4.350400000\ 10^{-21}\ V_{dc}^6 + 7.276890000\ 10^{-24}\ V_{dc}^8 - 7.612100000\ 10^{-27}\ V_{dc}^{10}$$
$$\left.\left.+ 4.767680000\ 10^{-30}\ V_{dc}^{12} - 1.629530000\ 10^{-33}\ V_{dc}^{14} + 2.332250000\ 10^{-37}\ V_{dc}^{16}\right)\right)^2\left(\frac{1}{50}\right.$$
$$- 1.131120000\ 10^{10}\ I\left(2.967000000\ 10^{-13} - 5.007360000\ 10^{-16}\ V_{dc}^2 + 1.704100000\ 10^{-18}\right.$$
$$V_{dc}^4 - 4.350400000\ 10^{-21}\ V_{dc}^6 + 7.276890000\ 10^{-24}\ V_{dc}^8 - 7.612100000\ 10^{-27}\ V_{dc}^{10}$$
$$\left.+ 4.767680000\ 10^{-30}\ V_{dc}^{12} - 1.629530000\ 10^{-33}\ V_{dc}^{14} + 2.332250000\ 10^{-37}\ V_{dc}^{16}\right)\right)\left(\frac{1}{50}\right.$$
$$+ 1.143688000\ 10^{10}\ I\left(2.967000000\ 10^{-13} - 5.007360000\ 10^{-16}\ V_{dc}^2 + 1.704100000\ 10^{-18}\right.$$
$$V_{dc}^4 - 4.350400000\ 10^{-21}\ V_{dc}^6 + 7.276890000\ 10^{-24}\ V_{dc}^8 - 7.612100000\ 10^{-27}\ V_{dc}^{10}$$
$$\left.\left.\left.+ 4.767680000\ 10^{-30}\ V_{dc}^{12} - 1.629530000\ 10^{-33}\ V_{dc}^{14} + 2.332250000\ 10^{-37}\ V_{dc}^{16}\right)\right)\right)$$

*#Hence, the IM$_3$ equation **with V$_{peak}$** = **1.985** (**at 16 dBm**) is given* **by:**

#SINGLE TOPOLOGY

$$IM_3 := \frac{3}{4} \cdot \frac{1}{2} \cdot (1.985)^2 \cdot \left(\frac{\left| A_3\left(j\omega_a, j\omega_a, -j\omega_b\right) \right|}{\left| A_1\left(j\omega_a\right) \right|^2 \cdot \left| A_1\left(j\omega_b\right) \right|} \right)$$

#DUAL TOPOLOGY

$$IM3 := \frac{3}{4} \cdot \frac{1}{2} \cdot (1.985)^2 \cdot \left(\frac{\left| A3\left(j\omega_a, j\omega_a, -j\omega_b\right) \right|}{\left| A1\left(j\omega_a\right) \right|^2 \cdot \left| A1\left(j\omega_b\right) \right|} \right)$$

$5.632985062\ 10^9 \Big| \big(-5.007360000\ 10^{-16} + 1.022460000\ 10^{-17}\ V_{dc}^2 - 6.525600000\ 10^{-20}\ V_{dc}^4$

$\quad + 2.037529200\ 10^{-22}\ V_{dc}^6 - 3.425445000\ 10^{-25}\ V_{dc}^8 + 3.146668800\ 10^{-28}\ V_{dc}^{10}$

$\quad - 1.482872300\ 10^{-31}\ V_{dc}^{12} + 2.798700000\ 10^{-35}\ V_{dc}^{14} \big) \Big/ \Big(\big(\frac{1}{50}$

$\quad + 1.137404000\ 10^{10}\ \mathrm{I}\ \big(2.967000000\ 10^{-13} - 5.007360000\ 10^{-16}\ V_{dc}^2 + 1.704100000\ 10^{-18}$

$V_{dc}^4 - 4.350400000\ 10^{-21}\ V_{dc}^6 + 7.276890000\ 10^{-24}\ V_{dc}^8 - 7.612100000\ 10^{-27}\ V_{dc}^{10}$

$\quad + 4.767680000\ 10^{-30}\ V_{dc}^{12} - 1.629530000\ 10^{-33}\ V_{dc}^{14} + 2.332250000\ 10^{-37}\ V_{dc}^{16} \big) \big)^2 \big(\frac{1}{50}$

$\quad - 1.131120000\ 10^{10}\ \mathrm{I}\ \big(2.967000000\ 10^{-13} - 5.007360000\ 10^{-16}\ V_{dc}^2 + 1.704100000\ 10^{-18}$

$V_{dc}^4 - 4.350400000\ 10^{-21}\ V_{dc}^6 + 7.276890000\ 10^{-24}\ V_{dc}^8 - 7.612100000\ 10^{-27}\ V_{dc}^{10}$

$\quad + 4.767680000\ 10^{-30}\ V_{dc}^{12} - 1.629530000\ 10^{-33}\ V_{dc}^{14} + 2.332250000\ 10^{-37}\ V_{dc}^{16} \big) \big) \big(\frac{1}{50}$

$\quad + 1.143688000\ 10^{10}\ \mathrm{I}\ \big(2.967000000\ 10^{-13} - 5.007360000\ 10^{-16}\ V_{dc}^2 + 1.704100000\ 10^{-18}$

$V_{dc}^4 - 4.350400000\ 10^{-21}\ V_{dc}^6 + 7.276890000\ 10^{-24}\ V_{dc}^8 - 7.612100000\ 10^{-27}\ V_{dc}^{10}$

$\quad + 4.767680000\ 10^{-30}\ V_{dc}^{12} - 1.629530000\ 10^{-33}\ V_{dc}^{14} + 2.332250000\ 10^{-37}\ V_{dc}^{16} \big) \big) \big) \Big|$

$\Big| \frac{1}{50} + 1.137404000\ 10^{10}\ \mathrm{I}\ \big(2.967000000\ 10^{-13} - 5.007360000\ 10^{-16}\ V_{dc}^2$

$\quad + 1.704100000\ 10^{-18}\ V_{dc}^4 - 4.350400000\ 10^{-21}\ V_{dc}^6 + 7.276890000\ 10^{-24}\ V_{dc}^8$

$\quad - 7.612100000\ 10^{-27}\ V_{dc}^{10} + 4.767680000\ 10^{-30}\ V_{dc}^{12} - 1.629530000\ 10^{-33}\ V_{dc}^{14}$

$\quad + 2.332250000\ 10^{-37}\ V_{dc}^{16} \big) \Big|^2 \Big| \frac{1}{50} + 1.131120000\ 10^{10}\ \mathrm{I}\ \big(2.967000000\ 10^{-13}$

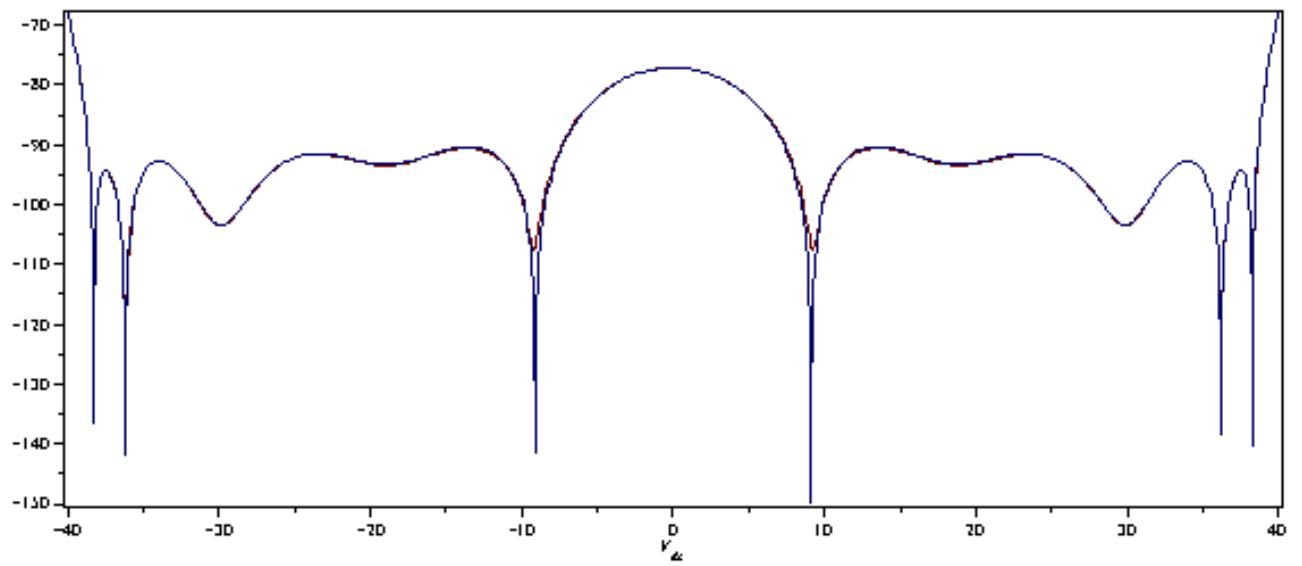$\quad - 5.007360000\ 10^{-16}\ V_{dc}^2 + 1.704100000\ 10^{-18}\ V_{dc}^4 - 4.350400000\ 10^{-21}\ V_{dc}^6$

$\quad + 7.276890000\ 10^{-24}\ V_{dc}^8 - 7.612100000\ 10^{-27}\ V_{dc}^{10} + 4.767680000\ 10^{-30}\ V_{dc}^{12}$

$\quad - 1.629530000\ 10^{-33}\ V_{dc}^{14} + 2.332250000\ 10^{-37}\ V_{dc}^{16} \big) \Big|$

$$5.632985062\,10^9 \left| \left(-5.007360000\,10^{-16} + 1.022460000\,10^{-17}\,V_{dc}^2 - 6.525600000\,10^{-20}\,V_{dc}^4 \right. \right.$$

$$+ 2.037529200\,10^{-22}\,V_{dc}^6 - 3.425445000\,10^{-25}\,V_{dc}^8 + 3.146668800\,10^{-28}\,V_{dc}^{10}$$

$$\left. - 1.482872300\,10^{-31}\,V_{dc}^{12} + 2.798700000\,10^{-35}\,V_{dc}^{14} \right) \Big/ \left(\left(\frac{1}{50} \right. \right.$$

$$+ 1.137404000\,10^{10}\,\mathrm{I}\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18} \right.$$

$$V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10}$$

$$\left.\left. + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16} \right) \right)^2 \left(\frac{1}{50} \right.$$

$$- 1.131120000\,10^{10}\,\mathrm{I}\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18} \right.$$

$$V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10}$$

$$\left.\left. + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16} \right) \right) \left(\frac{1}{50} \right.$$

$$+ 1.143688000\,10^{10}\,\mathrm{I}\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18} \right.$$

$$V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10}$$

$$\left.\left.\left.\left. + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16} \right) \right) \right) \right|$$

$$\left| \frac{1}{50} + 1.137404000\,10^{10}\,\mathrm{I}\left(2.967000000\,10^{-13} - 5.007360000\,10^{-16}\,V_{dc}^2 \right.\right.$$

$$+ 1.704100000\,10^{-18}\,V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6 + 7.276890000\,10^{-24}\,V_{dc}^8$$

$$- 7.612100000\,10^{-27}\,V_{dc}^{10} + 4.767680000\,10^{-30}\,V_{dc}^{12} - 1.629530000\,10^{-33}\,V_{dc}^{14}$$

$$\left.\left. + 2.332250000\,10^{-37}\,V_{dc}^{16} \right) \right|^2 \left| \frac{1}{50} + 1.131120000\,10^{10}\,\mathrm{I}\left(2.967000000\,10^{-13} \right.\right.$$

$$- 5.007360000\,10^{-16}\,V_{dc}^2 + 1.704100000\,10^{-18}\,V_{dc}^4 - 4.350400000\,10^{-21}\,V_{dc}^6$$

$$+ 7.276890000\,10^{-24}\,V_{dc}^8 - 7.612100000\,10^{-27}\,V_{dc}^{10} + 4.767680000\,10^{-30}\,V_{dc}^{12}$$

$$\left.\left. - 1.629530000\,10^{-33}\,V_{dc}^{14} + 2.332250000\,10^{-37}\,V_{dc}^{16} \right) \right|$$

$plot\left(\left\{20\log10\left(IM_3\right), 20\log10(IM3)\right\}, V_{dc} = -40..40\right)$

$plot\left(\left\{\left|C_1\right|, \left|C1\right|\right\}, V_{dc} = 0..10\right)$

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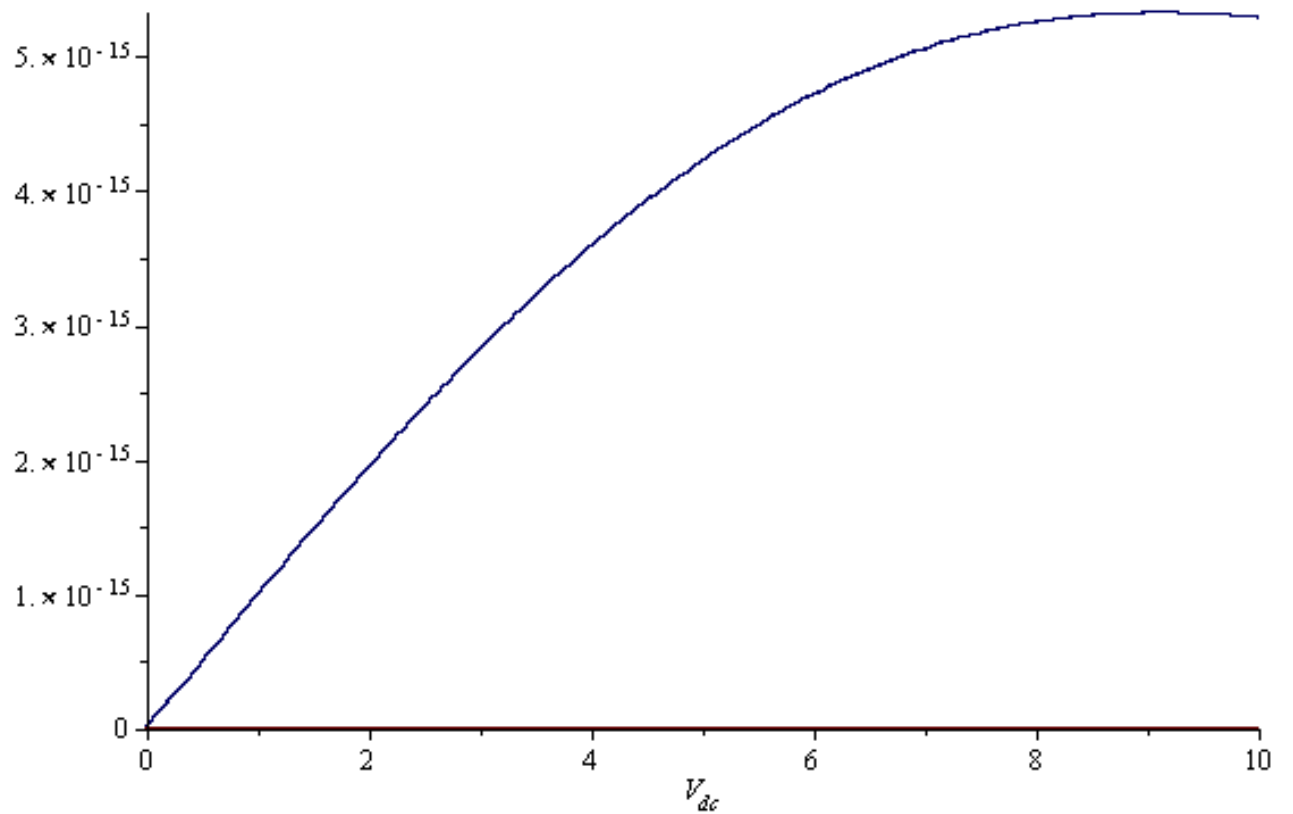
$vstart := 0; \ vend := 10;$

$$0$$
$$10$$

$vdiv := 51; \ vinc := \dfrac{(vend - vstart)}{vdiv};$

$$51$$
$$\dfrac{10}{51}$$

#Export IM$_3$ data of single topology

for i **from** 1 **by** 1 **to** $vdiv$ **do**
    $intmod := (i) \rightarrow \left(subs\left(V_{dc} = vstart + (vinc \cdot i), IM_3\right)\right);$
end do:
$inmod := Vector(vdiv, intmod);$

$$\begin{bmatrix} 1 .. 51 \ Vector_{column} \\ Data \ Type: anything \\ Storage: rectangular \\ Order: Fortran\_order \end{bmatrix}$$

#Export IM$_3$ data of dual topology

for i **from** 1 **by** 1 **to** $vdiv$ **do**
    $intmod := (i) \rightarrow \left(subs\left(V_{dc} = vstart + (vinc \cdot i), IM3\right)\right);$
end do:
$inmod2 := Vector(vdiv, intmod);$

$$\begin{bmatrix} 1 .. 51 \ Vector_{column} \\ Data \ Type: anything \\ Storage: rectangular \\ Order: Fortran\_order \end{bmatrix}$$

#Export C$_1$ data of the single bst varactor

for i **from** 1 **by** 1 **to** $vdiv$ **do**
    $intmod := (i) \rightarrow \left(subs\left(V_{dc} = vstart + (vinc \cdot i), |C_1|\right)\right);$
end do:
$inmod3 := Vector(vdiv, intmod);$

$$\begin{bmatrix} 1 .. 51 \ Vector_{column} \\ Data \ Type: anything \\ Storage: rectangular \\ Order: Fortran\_order \end{bmatrix}$$

B.2 Series Dual BST Varactor Circuit Topology

#Compute IM$_3$

    for *IDEAL series dual BST varactor circuit topology with matched varactors*

#From curve-fitting method, the polynomial equation which is fitted well to the previous C-V data is given by $M = K_o + K_2 \cdot (V_{dc} + v_{ac})^2 + K_4 \cdot (V_{dc} + v_{ac})^4 + K_6 \cdot (V_{dc} + v_{ac})^6 + K_8 \cdot (V_{dc} + v_{ac})^8 + K_{10} \cdot (V_{dc} + v_{ac})^{10} + K_{12} \cdot (V_{dc} + v_{ac})^{12} + K_{14} \cdot (V_{dc} + v_{ac})^{14} + K_{16} \cdot (V_{dc} + v_{ac})^{16}$

#ANTISERIES CONNECTION

#Thus, substituting $K_0 = 0.3018 \cdot 10^{-12}, K_2 = -0.0579888 \cdot 10^{-2} \cdot 10^{-12}, K_4 = 0.0217664 \cdot 10^{-4} \cdot 10^{-12}, K_6 = -0.00586324 \cdot 10^{-6} \cdot 10^{-12}, K_8 = 0.00101016 \cdot 10^{-8} \cdot 10^{-12}, K_{10} = -0.000107535 \cdot 10^{-10} \cdot 10^{-12}, K_{12} = 6.81098 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12}, K_{14} = -2.34574 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12}$ & $K_{16} = 3.37577 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12}$ **in** *equation M yields* :

$$M_1 := 0.3018 \cdot 10^{-12} - 0.0579888 \cdot 10^{-2} \cdot 10^{-12} \cdot (V_{dc} + v_{ac})^2 + 0.0217664 \cdot 10^{-4} \cdot 10^{-12} \cdot (V_{dc} + v_{ac})^4 - 0.00586324 \cdot 10^{-6} \cdot 10^{-12} \cdot (V_{dc} + v_{ac})^6 + 0.00101016 \cdot 10^{-8} \cdot 10^{-12} \cdot (V_{dc} + v_{ac})^8 - 0.000107535 \cdot 10^{-10} \cdot 10^{-12} \cdot (V_{dc} + v_{ac})^{10} + 6.81098 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12} \cdot (V_{dc} + v_{ac})^{12} - 2.34574 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12} \cdot (V_{dc} + v_{ac})^{14} + 3.37577 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12} \cdot (V_{dc} + v_{ac})^{16}$$

$$3.018000000\,10^{-13} - 5.798880000\,10^{-16} (V_{dc} + v_{ac})^2 + 2.176640000\,10^{-18} (V_{dc} + v_{ac})^4$$
$$- 5.863240000\,10^{-21} (V_{dc} + v_{ac})^6 + 1.010160000\,10^{-23} (V_{dc} + v_{ac})^8$$
$$- 1.075350000\,10^{-26} (V_{dc} + v_{ac})^{10} + 6.810980000\,10^{-30} (V_{dc} + v_{ac})^{12}$$
$$- 2.345740000\,10^{-33} (V_{dc} + v_{ac})^{14} + 3.375770000\,10^{-37} (V_{dc} + v_{ac})^{16}$$

#Substituting $K_0 = 0.3018 \cdot 10^{-12}, K_2 = -0.0579888 \cdot 10^{-2} \cdot 10^{-12}, K_4 = 0.0217664 \cdot 10^{-4} \cdot 10^{-12}, K_6 = -0.00586324 \cdot 10^{-6} \cdot 10^{-12}, K_8 = 0.00101016 \cdot 10^{-8} \cdot 10^{-12}, K_{10} = -0.000107535 \cdot 10^{-10} \cdot 10^{-12}, K_{12} = 6.81098 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12}, K_{14} = -2.34574 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12}$ & $K_{16} = 3.37577 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12}$ **in** *equation M yields* :

$M_2 := 0.3018 \cdot 10^{-12} - 0.0579888 \cdot 10^{-2} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^2 + 0.0217664 \cdot 10^{-4} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^4 - 0.00586324 \cdot 10^{-6} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^6 + 0.00101016 \cdot 10^{-8} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^8 - 0.000107535 \cdot 10^{-10} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^{10} + 6.81098 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^{12} - 2.34574 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^{14} + 3.37577 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^{16}$

$$3.018000000\,10^{-13} - 5.798880000\,10^{-16} \left(-V_{dc} + v_{ac}\right)^2 + 2.176640000\,10^{-18} \left(-V_{dc} + v_{ac}\right)^4$$
$$- 5.863240000\,10^{-21} \left(-V_{dc} + v_{ac}\right)^6 + 1.010160000\,10^{-23} \left(-V_{dc} + v_{ac}\right)^8$$
$$- 1.075350000\,10^{-26} \left(-V_{dc} + v_{ac}\right)^{10} + 6.810980000\,10^{-30} \left(-V_{dc} + v_{ac}\right)^{12}$$
$$- 2.345740000\,10^{-33} \left(-V_{dc} + v_{ac}\right)^{14} + 3.375770000\,10^{-37} \left(-V_{dc} + v_{ac}\right)^{16}$$

#Substituting $K_0 = 0.3018 \cdot 10^{-12}, K_2 = -0.0579888 \cdot 10^{-2} \cdot 10^{-12}, K_4 = 0.0217664 \cdot 10^{-4} \cdot 10^{-12}$, $K_6 = -0.00586324 \cdot 10^{-6} \cdot 10^{-12}, K_8 = 0.00101016 \cdot 10^{-8} \cdot 10^{-12}, K_{10} = -0.000107535 \cdot 10^{-10} \cdot 10^{-12}, K_{12} = 6.81098 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12}, K_{14} = -2.34574 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12}$ & $K_{16} = 3.37577 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12}$ **in** *equation M yields* :

$M_3 := 0.3018 \cdot 10^{-12} - 0.0579888 \cdot 10^{-2} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^2 + 0.0217664 \cdot 10^{-4} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^4 - 0.00586324 \cdot 10^{-6} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^6 + 0.00101016 \cdot 10^{-8} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^8 - 0.000107535 \cdot 10^{-10} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^{10} + 6.81098 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^{12} - 2.34574 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^{14} + 3.37577 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12} \cdot \left(V_{dc} + v_{ac}\right)^{16}$

$$3.018000000\,10^{-13} - 5.798880000\,10^{-16} \left(V_{dc} + v_{ac}\right)^2 + 2.176640000\,10^{-18} \left(V_{dc} + v_{ac}\right)^4$$
$$- 5.863240000\,10^{-21} \left(V_{dc} + v_{ac}\right)^6 + 1.010160000\,10^{-23} \left(V_{dc} + v_{ac}\right)^8$$
$$- 1.075350000\,10^{-26} \left(V_{dc} + v_{ac}\right)^{10} + 6.810980000\,10^{-30} \left(V_{dc} + v_{ac}\right)^{12}$$
$$- 2.345740000\,10^{-33} \left(V_{dc} + v_{ac}\right)^{14} + 3.375770000\,10^{-37} \left(V_{dc} + v_{ac}\right)^{16}$$

#Substituting $K_0 = 0.3018 \cdot 10^{-12}, K_2 = -0.0579888 \cdot 10^{-2} \cdot 10^{-12}, K_4 = 0.0217664 \cdot 10^{-4} \cdot 10^{-12}$, $K_6 = -0.00586324 \cdot 10^{-6} \cdot 10^{-12}, K_8 = 0.00101016 \cdot 10^{-8} \cdot 10^{-12}, K_{10} = -0.000107535 \cdot 10^{-10} \cdot 10^{-12}, K_{12} = 6.81098 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12}, K_{14} = -2.34574 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12}$ & $K_{16} = 3.37577 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12}$ **in** *equation M yields* :

$M_4 := 0.3018 \cdot 10^{-12} - 0.0579888 \cdot 10^{-2} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^2 + 0.0217664 \cdot 10^{-4} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^4 - 0.00586324 \cdot 10^{-6} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^6 + 0.00101016 \cdot 10^{-8} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^8 - 0.000107535 \cdot 10^{-10} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^{10} + 6.81098 \cdot 10^{-6} \cdot 10^{-12} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^{12} - 2.34574 \cdot 10^{-7} \cdot 10^{-14} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^{14} + 3.37577 \cdot 10^{-9} \cdot 10^{-16} \cdot 10^{-12} \cdot \left(-V_{dc} + v_{ac}\right)^{16}$

$$3.018000000\,10^{-13} - 5.798880000\,10^{-16}\left(-V_{dc} + v_{ac}\right)^2 + 2.176640000\,10^{-18}\left(-V_{dc} + v_{ac}\right)^4$$
$$- 5.863240000\,10^{-21}\left(-V_{dc} + v_{ac}\right)^6 + 1.010160000\,10^{-23}\left(-V_{dc} + v_{ac}\right)^8$$
$$- 1.075350000\,10^{-26}\left(-V_{dc} + v_{ac}\right)^{10} + 6.810980000\,10^{-30}\left(-V_{dc} + v_{ac}\right)^{12}$$
$$- 2.345740000\,10^{-33}\left(-V_{dc} + v_{ac}\right)^{14} + 3.375770000\,10^{-37}\left(-V_{dc} + v_{ac}\right)^{16}$$

#From M_1, M_2, M_3 & M_4, we could extract the coefficients, C_0 **to** C_2
   to satisfy the term which represents the capacitance C of a varactor, $C(v) = C_0 + C_1 v_{ac}$
   $+ C_2 v_{ac}^2$

#Hence, the extracted coefficients, C_0 **to** C_2 which are V_{dc} dependent are given **by:**

BST varactor C1 − Left

$CI_0 := coeff\left(M_1, v[ac], 0\right)$
$$3.018000000\,10^{-13} - 5.798880000\,10^{-16}\,V_{dc}^2 + 2.176640000\,10^{-18}\,V_{dc}^4 - 5.863240000\,10^{-21}\,V_{dc}^6$$
$$+ 1.010160000\,10^{-23}\,V_{dc}^8 - 1.075350000\,10^{-26}\,V_{dc}^{10} + 6.810980000\,10^{-30}\,V_{dc}^{12}$$
$$- 2.345740000\,10^{-33}\,V_{dc}^{14} + 3.375770000\,10^{-37}\,V_{dc}^{16}$$

$CI_1 := coeff\left(M_1, v[ac], 1\right)$
$$-1.159776000\,10^{-15}\,V_{dc} + 8.706560000\,10^{-18}\,V_{dc}^3 - 3.517944000\,10^{-20}\,V_{dc}^5$$
$$+ 8.081280000\,10^{-23}\,V_{dc}^7 - 1.075350000\,10^{-25}\,V_{dc}^9 + 8.173176000\,10^{-29}\,V_{dc}^{11}$$
$$- 3.284036000\,10^{-32}\,V_{dc}^{13} + 5.401232000\,10^{-36}\,V_{dc}^{15}$$

$CI_2 := coeff\left(M_1, v[ac], 2\right)$
$$-5.798880000\,10^{-16} + 1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4 + 2.828448000\,10^{-22}$$
$$V_{dc}^6 - 4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10} - 2.134623400\,10^{-31}\,V_{dc}^{12}$$
$$+ 4.050924000\,10^{-35}\,V_{dc}^{14}$$

BST varactor C2 − Left

$C2_0 := coeff\left(M_2, v[ac], 0\right)$
$$3.018000000\,10^{-13} - 5.798880000\,10^{-16}\,V_{dc}^2 + 2.176640000\,10^{-18}\,V_{dc}^4 - 5.863240000\,10^{-21}\,V_{dc}^6$$
$$+ 1.010160000\,10^{-23}\,V_{dc}^8 - 1.075350000\,10^{-26}\,V_{dc}^{10} + 6.810980000\,10^{-30}\,V_{dc}^{12}$$
$$- 2.345740000\,10^{-33}\,V_{dc}^{14} + 3.375770000\,10^{-37}\,V_{dc}^{16}$$

$C2_1 := coeff\left(M_2, v[ac], 1\right)$

$$1.159776000\,10^{-15}\,V_{dc} - 8.706560000\,10^{-18}\,V_{dc}^3 + 3.517944000\,10^{-20}\,V_{dc}^5 - 8.081280000\,10^{-23}$$
$$V_{dc}^7 + 1.075350000\,10^{-25}\,V_{dc}^9 - 8.173176000\,10^{-29}\,V_{dc}^{11} + 3.284036000\,10^{-32}\,V_{dc}^{13}$$
$$- 5.401232000\,10^{-36}\,V_{dc}^{15}$$

$C2_2 := coeff\left(M_2, v[ac], 2\right)$

$$-5.798880000\,10^{-16} + 1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4 + 2.828448000\,10^{-22}$$
$$V_{dc}^6 - 4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10} - 2.134623400\,10^{-31}\,V_{dc}^{12}$$
$$+ 4.050924000\,10^{-35}\,V_{dc}^{14}$$

BST varactor C3 − Right

$C3_0 := coeff\left(M_3, v[ac], 0\right)$

$$3.018000000\,10^{-13} - 5.798880000\,10^{-16}\,V_{dc}^2 + 2.176640000\,10^{-18}\,V_{dc}^4 - 5.863240000\,10^{-21}\,V_{dc}^6$$
$$+ 1.010160000\,10^{-23}\,V_{dc}^8 - 1.075350000\,10^{-26}\,V_{dc}^{10} + 6.810980000\,10^{-30}\,V_{dc}^{12}$$
$$- 2.345740000\,10^{-33}\,V_{dc}^{14} + 3.375770000\,10^{-37}\,V_{dc}^{16}$$

$C3_1 := coeff\left(M_3, v[ac], 1\right)$

$$-1.159776000\,10^{-15}\,V_{dc} + 8.706560000\,10^{-18}\,V_{dc}^3 - 3.517944000\,10^{-20}\,V_{dc}^5$$
$$+ 8.081280000\,10^{-23}\,V_{dc}^7 - 1.075350000\,10^{-25}\,V_{dc}^9 + 8.173176000\,10^{-29}\,V_{dc}^{11}$$
$$- 3.284036000\,10^{-32}\,V_{dc}^{13} + 5.401232000\,10^{-36}\,V_{dc}^{15}$$

$C3_2 := coeff\left(M_3, v[ac], 2\right)$

$$-5.798880000\,10^{-16} + 1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4 + 2.828448000\,10^{-22}$$
$$V_{dc}^6 - 4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10} - 2.134623400\,10^{-31}\,V_{dc}^{12}$$
$$+ 4.050924000\,10^{-35}\,V_{dc}^{14}$$

BST varactor C4 − Right

$C4_0 := coeff\left(M_4, v[ac], 0\right)$

$$3.018000000\,10^{-13} - 5.798880000\,10^{-16}\,V_{dc}^2 + 2.176640000\,10^{-18}\,V_{dc}^4 - 5.863240000\,10^{-21}\,V_{dc}^6$$
$$+ 1.010160000\,10^{-23}\,V_{dc}^8 - 1.075350000\,10^{-26}\,V_{dc}^{10} + 6.810980000\,10^{-30}\,V_{dc}^{12}$$
$$- 2.345740000\,10^{-33}\,V_{dc}^{14} + 3.375770000\,10^{-37}\,V_{dc}^{16}$$

$C4_1 := coeff\left(M_4, v[ac], 1\right)$

$$1.159776000\,10^{-15}\,V_{dc} - 8.706560000\,10^{-18}\,V_{dc}^3 + 3.517944000\,10^{-20}\,V_{dc}^5 - 8.081280000\,10^{-23}$$
$$V_{dc}^7 + 1.075350000\,10^{-25}\,V_{dc}^9 - 8.173176000\,10^{-29}\,V_{dc}^{11} + 3.284036000\,10^{-32}\,V_{dc}^{13}$$
$$- 5.401232000\,10^{-36}\,V_{dc}^{15}$$

$C4_2 := coeff\left(M_4, v[ac], 2\right)$

$$-5.798880000\,10^{-16} + 1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4 + 2.828448000\,10^{-22}$$
$$V_{dc}^6 - 4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10} - 2.134623400\,10^{-31}\,V_{dc}^{12}$$
$$+ 4.050924000\,10^{-35}\,V_{dc}^{14}$$

#C1 & C2 are in antiseries on the left hand side of the Series Dual BST toplogy

$$\#Cseriesleft := \frac{CI_0}{2} + \frac{CI_2}{8} \cdot \left(1 - \frac{1.5 \cdot CI_1^2}{CI_0 \cdot CI_2}\right) \cdot v_{ac}$$

$$C0left := \frac{CI_0}{2}$$

$$1.509000000\,10^{-13} - 2.899440000\,10^{-16}\,V_{dc}^2 + 1.088320000\,10^{-18}\,V_{dc}^4 - 2.931620000\,10^{-21}\,V_{dc}^6$$
$$+ 5.050800000\,10^{-24}\,V_{dc}^8 - 5.376750000\,10^{-27}\,V_{dc}^{10} + 3.405490000\,10^{-30}\,V_{dc}^{12}$$
$$- 1.172870000\,10^{-33}\,V_{dc}^{14} + 1.687885000\,10^{-37}\,V_{dc}^{16}$$

$$1.509000000\,10^{-13} - 2.899440000\,10^{-16}\,V_{dc}^2 + 1.088320000\,10^{-18}\,V_{dc}^4 - 2.931620000\,10^{-21}\,V_{dc}^6$$
$$+ 5.050800000\,10^{-24}\,V_{dc}^8 - 5.376750000\,10^{-27}\,V_{dc}^{10} + 3.405490000\,10^{-30}\,V_{dc}^{12}$$
$$- 1.172870000\,10^{-33}\,V_{dc}^{14} + 1.687885000\,10^{-37}\,V_{dc}^{16}$$

$$C1left := 0$$

$$0$$

$$C2left := \frac{CI_2}{8} \cdot \left(1 - \frac{1.5 \cdot CI_1^2}{CI_0 \cdot CI_2}\right)$$

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$$\frac{1}{8}\left(-5.798880000\,10^{-16} + 1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4\right.$$

$$+ 2.828448000\,10^{-22}\,V_{dc}^6 - 4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10}$$

$$\left.- 2.134623400\,10^{-31}\,V_{dc}^{12} + 4.050924000\,10^{-35}\,V_{dc}^{14}\right)\left(1 - \left(1.5\left(\vphantom{V_{dc}^2}\right.\right.\right.$$

$$-1.159776000\,10^{-15}\,V_{dc} + 8.706560000\,10^{-18}\,V_{dc}^3 - 3.517944000\,10^{-20}\,V_{dc}^5$$

$$+ 8.081280000\,10^{-23}\,V_{dc}^7 - 1.075350000\,10^{-25}\,V_{dc}^9 + 8.173176000\,10^{-29}\,V_{dc}^{11}$$

$$\left.\left.- 3.284036000\,10^{-32}\,V_{dc}^{13} + 5.401232000\,10^{-36}\,V_{dc}^{15}\right)^2\right)\Big/\left(\left(3.018000000\,10^{-13}\right.\right.$$

$$- 5.798880000\,10^{-16}\,V_{dc}^2 + 2.176640000\,10^{-18}\,V_{dc}^4 - 5.863240000\,10^{-21}\,V_{dc}^6$$

$$+ 1.010160000\,10^{-23}\,V_{dc}^8 - 1.075350000\,10^{-26}\,V_{dc}^{10} + 6.810980000\,10^{-30}\,V_{dc}^{12}$$

$$\left.- 2.345740000\,10^{-33}\,V_{dc}^{14} + 3.375770000\,10^{-37}\,V_{dc}^{16}\right)\left(-5.798880000\,10^{-16}\right.$$

$$+ 1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4 + 2.828448000\,10^{-22}\,V_{dc}^6$$

$$- 4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10} - 2.134623400\,10^{-31}\,V_{dc}^{12}$$

$$\left.\left.\left.+ 4.050924000\,10^{-35}\,V_{dc}^{14}\right)\right)\right)$$

#C3 & C4 are in antiseries on the right hand side of the BST Series Dual Topology

$$\#Cseriesright := \frac{C3_0}{2} + \frac{C3_2}{8}\cdot\left(1 - \frac{1.5\cdot C3_1^2}{C3_0\cdot C3_2}\right)\cdot v_{ac}$$

$$C0right := \frac{C3_0}{2}$$

$$1.509000000\,10^{-13} - 2.899440000\,10^{-16}\,V_{dc}^2 + 1.088320000\,10^{-18}\,V_{dc}^4 - 2.931620000\,10^{-21}\,V_{dc}^6$$

$$+ 5.050800000\,10^{-24}\,V_{dc}^8 - 5.376750000\,10^{-27}\,V_{dc}^{10} + 3.405490000\,10^{-30}\,V_{dc}^{12}$$

$$- 1.172870000\,10^{-33}\,V_{dc}^{14} + 1.687885000\,10^{-37}\,V_{dc}^{16}$$

$$C1right := 0$$

$$0$$

$$C2right := \frac{C3_2}{8}\cdot\left(1 - \frac{1.5\cdot C3_1^2}{C3_0\cdot C3_2}\right)$$

$$\frac{1}{8}\left(-5.798880000\,10^{-16} + 1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4\right.$$

$$+\,2.828448000\,10^{-22}\,V_{dc}^6 - 4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10}$$

$$-\,2.134623400\,10^{-31}\,V_{dc}^{12} + 4.050924000\,10^{-35}\,V_{dc}^{14}\right)\left(1 - \left(1.5\,\right(\right.$$

$$-1.159776000\,10^{-15}\,V_{dc} + 8.706560000\,10^{-18}\,V_{dc}^3 - 3.517944000\,10^{-20}\,V_{dc}^5$$

$$+\,8.081280000\,10^{-23}\,V_{dc}^7 - 1.075350000\,10^{-25}\,V_{dc}^9 + 8.173176000\,10^{-29}\,V_{dc}^{11}$$

$$\left.-\,3.284036000\,10^{-32}\,V_{dc}^{13} + 5.401232000\,10^{-36}\,V_{dc}^{15}\right)^2\right)\Big/\left(\left(3.018000000\,10^{-13}\right.\right.$$

$$-\,5.798880000\,10^{-16}\,V_{dc}^2 + 2.176640000\,10^{-18}\,V_{dc}^4 - 5.863240000\,10^{-21}\,V_{dc}^6$$

$$+\,1.010160000\,10^{-23}\,V_{dc}^8 - 1.075350000\,10^{-26}\,V_{dc}^{10} + 6.810980000\,10^{-30}\,V_{dc}^{12}$$

$$\left.-\,2.345740000\,10^{-33}\,V_{dc}^{14} + 3.375770000\,10^{-37}\,V_{dc}^{16}\right)\left(-5.798880000\,10^{-16}\right.$$

$$+\,1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4 + 2.828448000\,10^{-22}\,V_{dc}^6$$

$$-\,4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10} - 2.134623400\,10^{-31}\,V_{dc}^{12}$$

$$\left.\left.\left.+\,4.050924000\,10^{-35}\,V_{dc}^{14}\right)\right)\right)$$

#SERISDUAL TOPOLOGY

C0seriesdual := C0left + C0right

$$3.018000000\,10^{-13} - 5.798880000\,10^{-16}\,V_{dc}^2 + 2.176640000\,10^{-18}\,V_{dc}^4 - 5.863240000\,10^{-21}\,V_{dc}^6$$

$$+\,1.010160000\,10^{-23}\,V_{dc}^8 - 1.075350000\,10^{-26}\,V_{dc}^{10} + 6.810980000\,10^{-30}\,V_{dc}^{12}$$

$$-\,2.345740000\,10^{-33}\,V_{dc}^{14} + 3.375770000\,10^{-37}\,V_{dc}^{16}$$

C1seriesdual := C1left + C1right

$$0$$

C2seriesdual := C2left + C2right

$$\frac{1}{4}\Big(-5.798880000\,10^{-16} + 1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4$$

$$+\,2.828448000\,10^{-22}\,V_{dc}^6 - 4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10}$$

$$-\,2.134623400\,10^{-31}\,V_{dc}^{12} + 4.050924000\,10^{-35}\,V_{dc}^{14}\Big)\Big(1 - \Big(1.5\,\Big($$

$$-1.159776000\,10^{-15}\,V_{dc} + 8.706560000\,10^{-18}\,V_{dc}^3 - 3.517944000\,10^{-20}\,V_{dc}^5$$

$$+\,8.081280000\,10^{-23}\,V_{dc}^7 - 1.075350000\,10^{-25}\,V_{dc}^9 + 8.173176000\,10^{-29}\,V_{dc}^{11}$$

$$-\,3.284036000\,10^{-32}\,V_{dc}^{13} + 5.401232000\,10^{-36}\,V_{dc}^{15}\Big)^2\Big)\Big/\Big(\Big(3.018000000\,10^{-13}$$

$$-\,5.798880000\,10^{-16}\,V_{dc}^2 + 2.176640000\,10^{-18}\,V_{dc}^4 - 5.863240000\,10^{-21}\,V_{dc}^6$$

$$+\,1.010160000\,10^{-23}\,V_{dc}^8 - 1.075350000\,10^{-26}\,V_{dc}^{10} + 6.810980000\,10^{-30}\,V_{dc}^{12}$$

$$-\,2.345740000\,10^{-33}\,V_{dc}^{14} + 3.375770000\,10^{-37}\,V_{dc}^{16}\Big)\Big(-5.798880000\,10^{-16}$$

$$+\,1.305984000\,10^{-17}\,V_{dc}^2 - 8.794860000\,10^{-20}\,V_{dc}^4 + 2.828448000\,10^{-22}\,V_{dc}^6$$

$$-\,4.839075000\,10^{-25}\,V_{dc}^8 + 4.495246800\,10^{-28}\,V_{dc}^{10} - 2.134623400\,10^{-31}\,V_{dc}^{12}$$

$$+\,4.050924000\,10^{-35}\,V_{dc}^{14}\Big)\Big)\Big)$$

*#The modified first-order terms **without the value of L**, with two input frequencies, $\omega_a = 2\cdot\pi$*
$\cdot1.81\ GHz = 11.37404\ GHz$ & $\omega_b = 2\cdot\pi\cdot1.8\ GHz = 11.3112\ GHz$ & $R = 50\ \Omega$ & R
*$= 50\ \Omega$ are given **by**:*

$$A1\big(j\omega_a\big) := \frac{1}{\dfrac{1}{50} + \mathrm{I}\cdot11.37404\cdot10^9\cdot C0seriesdual}$$

$$1\Big/\Big(\frac{1}{50} + 1.137404000\,10^{10}\,\mathrm{I}\,\big(3.018000000\,10^{-13} - 5.798880000\,10^{-16}\,V_{dc}^2$$

$$+\,2.176640000\,10^{-18}\,V_{dc}^4 - 5.863240000\,10^{-21}\,V_{dc}^6 + 1.010160000\,10^{-23}\,V_{dc}^8$$

$$-\,1.075350000\,10^{-26}\,V_{dc}^{10} + 6.810980000\,10^{-30}\,V_{dc}^{12} - 2.345740000\,10^{-33}\,V_{dc}^{14}$$

$$+\,3.375770000\,10^{-37}\,V_{dc}^{16}\big)\Big)$$

$$A1\big(\text{-}j\omega_b\big) := \frac{1}{\dfrac{1}{50} - \mathrm{I}\cdot11.3112\cdot10^9\cdot C0seriesdual}$$

$$1 \bigg/ \bigg(\frac{1}{50} - 1.131120000 \ 10^{10} \ \mathrm{I} \big(3.018000000 \ 10^{-13} - 5.798880000 \ 10^{-16} \ V_{dc}^2$$
$$+ \ 2.176640000 \ 10^{-18} \ V_{dc}^4 - 5.863240000 \ 10^{-21} \ V_{dc}^6 + 1.010160000 \ 10^{-23} \ V_{dc}^8$$
$$- \ 1.075350000 \ 10^{-26} \ V_{dc}^{10} + 6.810980000 \ 10^{-30} \ V_{dc}^{12} - 2.345740000 \ 10^{-33} \ V_{dc}^{14}$$
$$+ \ 3.375770000 \ 10^{-37} \ V_{dc}^{16} \big) \bigg)$$

$$A1\big(j\omega_b\big) := \cfrac{1}{\cfrac{1}{50} + \mathrm{I} \cdot 11.3112 \cdot 10^9 \cdot C0seriesdual}$$

$$1 \bigg/ \bigg(\frac{1}{50} + 1.131120000 \ 10^{10} \ \mathrm{I} \big(3.018000000 \ 10^{-13} - 5.798880000 \ 10^{-16} \ V_{dc}^2$$
$$+ \ 2.176640000 \ 10^{-18} \ V_{dc}^4 - 5.863240000 \ 10^{-21} \ V_{dc}^6 + 1.010160000 \ 10^{-23} \ V_{dc}^8$$
$$- \ 1.075350000 \ 10^{-26} \ V_{dc}^{10} + 6.810980000 \ 10^{-30} \ V_{dc}^{12} - 2.345740000 \ 10^{-33} \ V_{dc}^{14}$$
$$+ \ 3.375770000 \ 10^{-37} \ V_{dc}^{16} \big) \bigg)$$

#*The modified second-order terms* **without the value of L** :

$$A2\big(j\omega_a, j\omega_a\big) := - \left(\cfrac{\cfrac{C1seriesdual}{2} \cdot 2 \cdot \mathrm{I} \cdot 11.37404 \cdot 10^9 \cdot A1\big(j\omega_a\big)^2}{\cfrac{1}{50} + 2 \cdot \mathrm{I} \cdot 11.37404 \cdot 10^9 \cdot C0seriesdual} \right)$$
$$-0. \, \mathrm{I}$$

$$A2\big(j\omega_a, -j\omega_b\big) :=$$
$$- \left(\cfrac{\cfrac{C1seriesdual}{2} \cdot \big(\mathrm{I} \cdot 11.37404 \cdot 10^9 - \mathrm{I} \cdot 11.3112 \cdot 10^9 \big) \cdot A1\big(j\omega_a\big) \cdot A1\big(-j\omega_b\big)}{\cfrac{1}{50} + \big(\mathrm{I} \cdot 11.37404 \cdot 10^9 - \mathrm{I} \cdot 11.3112 \cdot 10^9 \big) \cdot C0seriesdual} \right)$$
$$-0. \, \mathrm{I}$$

#*The modified third-order terms* **without the value of L** *at frequency* $(2\omega_a - \omega_b)$:
$$U := \frac{1}{3} \cdot \big(2 \cdot A1\big(j\omega_a\big) \cdot A2\big(j\omega_a, -j\omega_b\big) + A1\big(-j\omega_b\big) \cdot A2\big(j\omega_a, j\omega_a\big) \big)$$
$$-0. \, \mathrm{I}$$

$$A3\big(j\omega_a, j\omega_a, -j\omega_b\big) := - \bigg(\bigg(\big(2 \cdot \mathrm{I} \cdot 11.37404 \cdot 10^9 - \mathrm{I} \cdot 11.3112 \cdot 10^9 \big) \cdot \bigg(C1seriesdual \cdot U$$
$$+ \ \frac{C2seriesdual}{3} \cdot A1\big(j\omega_a\big)^2 \cdot A1\big(-j\omega_b\big) \bigg) \bigg) \bigg/ \bigg(\frac{1}{50} + \big(2 \cdot \mathrm{I} \cdot 11.37404 \cdot 10^9 - \mathrm{I} \cdot 11.3112$$
$$\cdot 10^9 \big) \cdot C0seriesdual \bigg) \bigg)$$

$$-\Bigg(9.530733333\ 10^8\ \mathrm{I}\Big(-5.798880000\ 10^{-16} + 1.305984000\ 10^{-17}\ V_{dc}^2 - 8.794860000\ 10^{-20}\ V_{dc}^4$$

$$+ 2.828448000\ 10^{-22}\ V_{dc}^6 - 4.839075000\ 10^{-25}\ V_{dc}^8 + 4.495246800\ 10^{-28}\ V_{dc}^{10}$$

$$- 2.134623400\ 10^{-31}\ V_{dc}^{12} + 4.050924000\ 10^{-35}\ V_{dc}^{14}\Big)\Big(1 - \Big(1.5\ \Big($$

$$-1.159776000\ 10^{-15}\ V_{dc} + 8.706560000\ 10^{-18}\ V_{dc}^3 - 3.517944000\ 10^{-20}\ V_{dc}^5$$

$$+ 8.081280000\ 10^{-23}\ V_{dc}^7 - 1.075350000\ 10^{-25}\ V_{dc}^9 + 8.173176000\ 10^{-29}\ V_{dc}^{11}$$

$$- 3.284036000\ 10^{-32}\ V_{dc}^{13} + 5.401232000\ 10^{-36}\ V_{dc}^{15}\Big)^2\Big) \Big/ \Big(\big(3.018000000\ 10^{-13}$$

$$- 5.798880000\ 10^{-16}\ V_{dc}^2 + 2.176640000\ 10^{-18}\ V_{dc}^4 - 5.863240000\ 10^{-21}\ V_{dc}^6$$

$$+ 1.010160000\ 10^{-23}\ V_{dc}^8 - 1.075350000\ 10^{-26}\ V_{dc}^{10} + 6.810980000\ 10^{-30}\ V_{dc}^{12}$$

$$- 2.345740000\ 10^{-33}\ V_{dc}^{14} + 3.375770000\ 10^{-37}\ V_{dc}^{16}\big) \big(-5.798880000\ 10^{-16}$$

$$+ 1.305984000\ 10^{-17}\ V_{dc}^2 - 8.794860000\ 10^{-20}\ V_{dc}^4 + 2.828448000\ 10^{-22}\ V_{dc}^6$$

$$- 4.839075000\ 10^{-25}\ V_{dc}^8 + 4.495246800\ 10^{-28}\ V_{dc}^{10} - 2.134623400\ 10^{-31}\ V_{dc}^{12}$$

$$+ 4.050924000\ 10^{-35}\ V_{dc}^{14}\big)\Big)\Big)\Big) \Big/ \Bigg(\Big(\Big(\frac{1}{50} + 1.137404000\ 10^{10}\ \mathrm{I}\ \big(3.018000000\ 10^{-13}$$

$$- 5.798880000\ 10^{-16}\ V_{dc}^2 + 2.176640000\ 10^{-18}\ V_{dc}^4 - 5.863240000\ 10^{-21}\ V_{dc}^6$$

$$+ 1.010160000\ 10^{-23}\ V_{dc}^8 - 1.075350000\ 10^{-26}\ V_{dc}^{10} + 6.810980000\ 10^{-30}\ V_{dc}^{12}$$

$$- 2.345740000\ 10^{-33}\ V_{dc}^{14} + 3.375770000\ 10^{-37}\ V_{dc}^{16}\big)\Big)^2 \Big(\frac{1}{50}$$

$$- 1.131120000\ 10^{10}\ \mathrm{I}\ \big(3.018000000\ 10^{-13} - 5.798880000\ 10^{-16}\ V_{dc}^2 + 2.176640000\ 10^{-18}$$

$$V_{dc}^4 - 5.863240000\ 10^{-21}\ V_{dc}^6 + 1.010160000\ 10^{-23}\ V_{dc}^8 - 1.075350000\ 10^{-26}\ V_{dc}^{10}$$

$$+ 6.810980000\ 10^{-30}\ V_{dc}^{12} - 2.345740000\ 10^{-33}\ V_{dc}^{14} + 3.375770000\ 10^{-37}\ V_{dc}^{16}\big)\Big) \Big(\frac{1}{50}$$

$$+ 1.143688000\ 10^{10}\ \mathrm{I}\ \big(3.018000000\ 10^{-13} - 5.798880000\ 10^{-16}\ V_{dc}^2 + 2.176640000\ 10^{-18}$$

$$V_{dc}^4 - 5.863240000\ 10^{-21}\ V_{dc}^6 + 1.010160000\ 10^{-23}\ V_{dc}^8 - 1.075350000\ 10^{-26}\ V_{dc}^{10}$$

$$+ 6.810980000\ 10^{-30}\ V_{dc}^{12} - 2.345740000\ 10^{-33}\ V_{dc}^{14} + 3.375770000\ 10^{-37}\ V_{dc}^{16}\big)\Big)\Big)$$

#Hence, the *IM$_3$* equation **with V_{peak} = 1.984** (*at* **16** *dBm*) *is given* **by**:

$$IM3 := \frac{3}{4}\cdot\frac{1}{2}\cdot(1.984)^2\cdot\left(\frac{\big| A3\big(j\omega_a, j\omega_a, -j\omega_b\big)\big|}{\big| A1\big(j\omega_a\big)\big|^2\cdot\big| A1\big(j\omega_b\big)\big|} \right)$$

$$1.406827735 \, 10^9 \left| \left| \left(\left(-5.798880000 \, 10^{-16} + 1.305984000 \, 10^{-17} V_{dc}^2 - 8.794860000 \, 10^{-20} V_{dc}^4 \right. \right. \right. \right.$$

$$+ 2.828448000 \, 10^{-22} V_{dc}^6 - 4.839075000 \, 10^{-25} V_{dc}^8 + 4.495246800 \, 10^{-28} V_{dc}^{10}$$

$$\left. - 2.134623400 \, 10^{-31} V_{dc}^{12} + 4.050924000 \, 10^{-35} V_{dc}^{14} \right) \left(1 - \left(1.5 \left(\vphantom{\frac{1}{1}} \right.\right.\right.$$

$$-1.159776000 \, 10^{-15} V_{dc} + 8.706560000 \, 10^{-18} V_{dc}^3 - 3.517944000 \, 10^{-20} V_{dc}^5$$

$$+ 8.081280000 \, 10^{-23} V_{dc}^7 - 1.075350000 \, 10^{-25} V_{dc}^9 + 8.173176000 \, 10^{-29} V_{dc}^{11}$$

$$\left. \left. - 3.284036000 \, 10^{-32} V_{dc}^{13} + 5.401232000 \, 10^{-36} V_{dc}^{15} \right)^2 \right) \Big/ \left(\left(3.018000000 \, 10^{-13} \right. \right.$$

$$- 5.798880000 \, 10^{-16} V_{dc}^2 + 2.176640000 \, 10^{-18} V_{dc}^4 - 5.863240000 \, 10^{-21} V_{dc}^6$$

$$+ 1.010160000 \, 10^{-23} V_{dc}^8 - 1.075350000 \, 10^{-26} V_{dc}^{10} + 6.810980000 \, 10^{-30} V_{dc}^{12}$$

$$\left. - 2.345740000 \, 10^{-33} V_{dc}^{14} + 3.375770000 \, 10^{-37} V_{dc}^{16} \right) \left(-5.798880000 \, 10^{-16} \right.$$

$$+ 1.305984000 \, 10^{-17} V_{dc}^2 - 8.794860000 \, 10^{-20} V_{dc}^4 + 2.828448000 \, 10^{-22} V_{dc}^6$$

$$- 4.839075000 \, 10^{-25} V_{dc}^8 + 4.495246800 \, 10^{-28} V_{dc}^{10} - 2.134623400 \, 10^{-31} V_{dc}^{12}$$

$$\left. \left. \left. \left. + 4.050924000 \, 10^{-35} V_{dc}^{14} \right) \right) \right) \right) \Big/ \left(\left(\left(\frac{1}{50} + 1.137404000 \, 10^{10} \, I \left(3.018000000 \, 10^{-13} \right. \right.\right.\right.$$

$$- 5.798880000 \, 10^{-16} V_{dc}^2 + 2.176640000 \, 10^{-18} V_{dc}^4 - 5.863240000 \, 10^{-21} V_{dc}^6$$

$$+ 1.010160000 \, 10^{-23} V_{dc}^8 - 1.075350000 \, 10^{-26} V_{dc}^{10} + 6.810980000 \, 10^{-30} V_{dc}^{12}$$

$$\left. \left. - 2.345740000 \, 10^{-33} V_{dc}^{14} + 3.375770000 \, 10^{-37} V_{dc}^{16} \right) \right)^2 \left(\frac{1}{50} \right.$$

$$- 1.131120000 \, 10^{10} \, I \left(3.018000000 \, 10^{-13} - 5.798880000 \, 10^{-16} V_{dc}^2 + 2.176640000 \, 10^{-18} \right.$$

$$V_{dc}^4 - 5.863240000 \, 10^{-21} V_{dc}^6 + 1.010160000 \, 10^{-23} V_{dc}^8 - 1.075350000 \, 10^{-26} V_{dc}^{10}$$

$$\left. + 6.810980000 \, 10^{-30} V_{dc}^{12} - 2.345740000 \, 10^{-33} V_{dc}^{14} + 3.375770000 \, 10^{-37} V_{dc}^{16} \right) \left(\frac{1}{50} \right.$$

$$+ 1.143688000 \, 10^{10} \, I \left(3.018000000 \, 10^{-13} - 5.798880000 \, 10^{-16} V_{dc}^2 + 2.176640000 \, 10^{-18} \right.$$

$$V_{dc}^4 - 5.863240000 \, 10^{-21} V_{dc}^6 + 1.010160000 \, 10^{-23} V_{dc}^8 - 1.075350000 \, 10^{-26} V_{dc}^{10}$$

$$\left. \left. \left. + 6.810980000 \, 10^{-30} V_{dc}^{12} - 2.345740000 \, 10^{-33} V_{dc}^{14} + 3.375770000 \, 10^{-37} V_{dc}^{16} \right) \right) \right) \right|$$

$$\left| \frac{1}{50} + 1.137404000 \, 10^{10} \, I \left(3.018000000 \, 10^{-13} - 5.798880000 \, 10^{-16} V_{dc}^2 \right.\right.$$

$$+ 2.176640000 \, 10^{-18} V_{dc}^4 - 5.863240000 \, 10^{-21} V_{dc}^6 + 1.010160000 \, 10^{-23} V_{dc}^8$$

$$- 1.075350000 \, 10^{-26} V_{dc}^{10} + 6.810980000 \, 10^{-30} V_{dc}^{12} - 2.345740000 \, 10^{-33} V_{dc}^{14}$$

$$\left. + 3.375770000 \, 10^{-37} V_{dc}^{16} \right) \Big|^2 \left| \frac{1}{50} + 1.131120000 \, 10^{10} \, I \left(3.018000000 \, 10^{-13} \right.\right.$$

$$- 5.798880000 \, 10^{-16} V_{dc}^2 + 2.176640000 \, 10^{-18} V_{dc}^4 - 5.863240000 \, 10^{-21} V_{dc}^6$$

$$+ 1.010160000 \, 10^{-23} V_{dc}^8 - 1.075350000 \, 10^{-26} V_{dc}^{10} + 6.810980000 \, 10^{-30} V_{dc}^{12}$$

$$\left. - 2.345740000 \, 10^{-33} V_{dc}^{14} + 3.375770000 \, 10^{-37} V_{dc}^{16} \right) \Big|$$

$plot\big(\{\,20\log10(IM3)\,\},\,V_{dc}=-40\,..40\big)$

$plot\big(\{\,|C1_2|,\,|C2seriesdual|\,\},\,V_{dc}=-40\,..40\big)$

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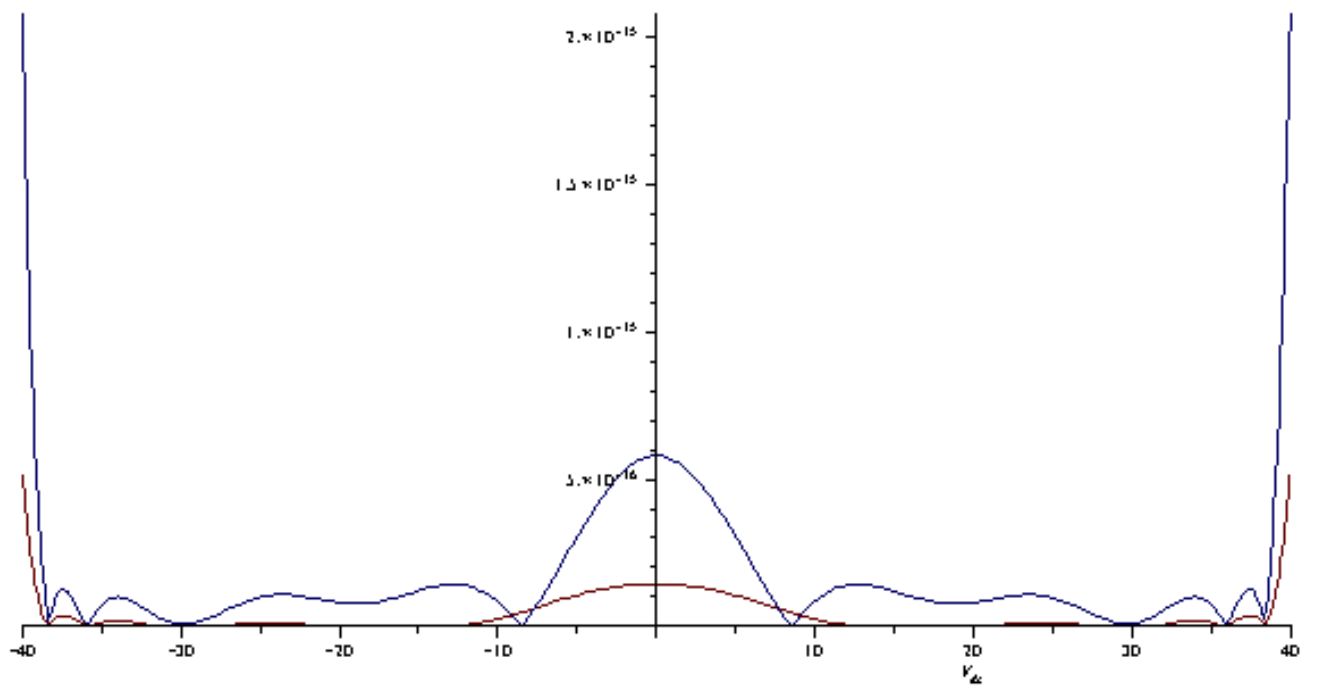
$vstart := -40; \ vend := 40;$

$$-40$$

$$40$$

$vdiv := 401; \ vinc := \dfrac{(vend - vstart)}{vdiv};$

$$401$$

$$\frac{80}{401}$$

#Export IM$_3$ data of series dual topology

for i **from** 1 **by** 1 **to** $vdiv$ **do**

$\qquad intmod := (i) \rightarrow \big(subs \big(V_{dc} = vstart + (vinc \cdot i), IM3 \big) \big);$

end do:

$inmod2 := Vector(vdiv, intmod);$

$$\begin{bmatrix} \textit{1 .. 401 Vector}_{column} \\ \textit{Data Type: anything} \\ \textit{Storage: rectangular} \\ \textit{Order: Fortran\_order} \end{bmatrix}$$

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