Introducing NFC for in-body and on-body medical sensors

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Abstract

In the last few decades, the number of people suffering from chronic diseases that require continuous treatment and monitoring has been on the rise. To achieve a more cost-efficient health care system, and to offer better treatment for patients, monitoring of the physiological parameters could be carried out by the patients themselves using mobile health services, known in short as "m-health". In this thesis, we focus on miniaturized battery-less implants and on-body sensors that use the near field communication (NFC) standard. This standard is now widely available on smart-phones/watches and is able to transfer energy and data to specific tags. Using this combination, the readings of the physiological parameters will be available on the phone and can thus be transferred to a health station for further processing.

The main goal of this work is to provide a toolset for designing, implementing and testing complete systems for implantable sensory NFC tags spanning aspects from the sensory implant to portable devices (smart-phone/watch) and health-stations servers. This will provide a huge step forward towards continuous monitoring of physiological parameters such as glucose level, among others. Two different ASICs have been developed in 90nm CMOS to demonstrate how to connect different types of sensors to a unique type 1 tag in a standardized fashion, as well as a mobile application to control, power up and communicate with the sensory tag and, finally, an algorithm to exchange the data between the smart-phone and a server.

We have demonstrated that multiple sensors monitoring different physiological parameters can be connected simultaneously to the same tag and provide continuous readings to a smart-phone/watch. This can supply invaluable data for doctors to analyse and discover any correlations between these parameters. An Android-based toolset has been developed to help reduce the effort required for hardware engineers to design new sensory tags by investigating which tag architectures match the requirements of throughput, complexity and energy consumption. On the functional blocks level, a few novel topologies have been researched, implemented and tested, including a particular amplitude shift keying (ASK) demodulator and sensor readout for specific nanowire (NW) biosensors using time to digital conversion (TDC).

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In the journey of pursuing my PhD studies, different people and institutions have made it enriching, enlightening and rewarding. I would like to take this chance to thank them all for making it possible and enjoyable. First and foremost, my deepest gratitude goes to my thesis advisor associate Prof. Philipp Häfliger for his supervision, patience, shared scientific knowledge, friendship and support in hard times. I am also grateful to my co-advisor Prof. Thomas Plagemann for his great expertise and for the unlimited hours of feedback and discussion he offered during this period.

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*Till **Ulrich***
*Till **Aline***
*Till **Miriam***

زرعوا فأكلنا ونزرع فيأكلون
The Earth is not a gift from our parents, it is a loan from our children

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List of Acronyms

1T1C	One Transistor One Capacitor
ADC	Analogue to Digital Converter
ASICs	Application Specific Integrated Circuit
ASK	Amplitude Shift Keying
BPSK	Binary Phase Shift Keying
CBRAM	Conductive Bridging Random Access Memory
CHI	Channel Hot electron Injection
CMOS	Complementary metal-oxide semiconductor
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
ECG/ EKG	Electrocardiography
EEG	Electroencephalogram
EM	ElectroMagnetic
ENOB	Effective Number Of Bits
FeRAM/FRAM	Ferro Electric Random Access Memory
FN	Fowler – Nordheim
FPGA	Field-programmable gate array
GPU	Graphics Processing Unit
HBP	High Blood Pressure
IR	InfraRed
IrDA	Infrared Data Association
LDO	Low Drop-Out
MIPS	Million Instructions Per Second
MLC	Multi Level Cell
MRAM	Magnetoresistive Random Access Memory
NFC	Near Field Communication
NRZ-L	Non-Return-to-Zero-Level
NVM	Non Volatile Memory
NW	NanoWire
PH	Potential Hydrogen
PRAM	Phase change Random Access Memory
ReRAM	Resistive Random Access Memory

RF	Radio Frequency
RFID	Radio Frequency IDentification
RTT	Round Trip Time
SAADC	Successive Approximation Analogue to Digital Converter
SAR	Specific Absorption Rate
SNR	Signal to Noise Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
SPI	Serial to Parallel Interface
SVC	Self Vth Cancellation
T1D	Type 1 Diabetes
TDC	Time to Digital Converter
TMR	Tunnel MagnetoResistance
UWB	Ultra Wide-Band
WBAN	Wireless Body Area Network
WHO	World Health Organization
WSN	Wireless Sensor Networks

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Chapter 1

Introduction

1.1 Motivation

Due to the big advancements made in medicine in the last few decades, more people are living longer. On one hand, this is good news since we have been searching for a longer life for millennia. However, knowing that chronic diseases are also increasing worldwide leads to the conclusion that more people are living longer but less healthily. The two major chronic diseases that are related to age are high blood pressure and diabetes, which we are going to discuss here to illustrate this issue.

Globally, the overall prevalence of raised blood pressure in adults aged 18 and over was around 22% in 2014 [1]. In the USA, 29% of the population had high blood pressure (HBP) in 2011[2]. There is a direct relationship between age and HBP. While in the USA, 37% and 35% of men and women respectively in the age group 45-54 have HBP, this ratio jumps to 67% and 78% of men and women respectively in the age group 75 and older, as shown in Figure 1.

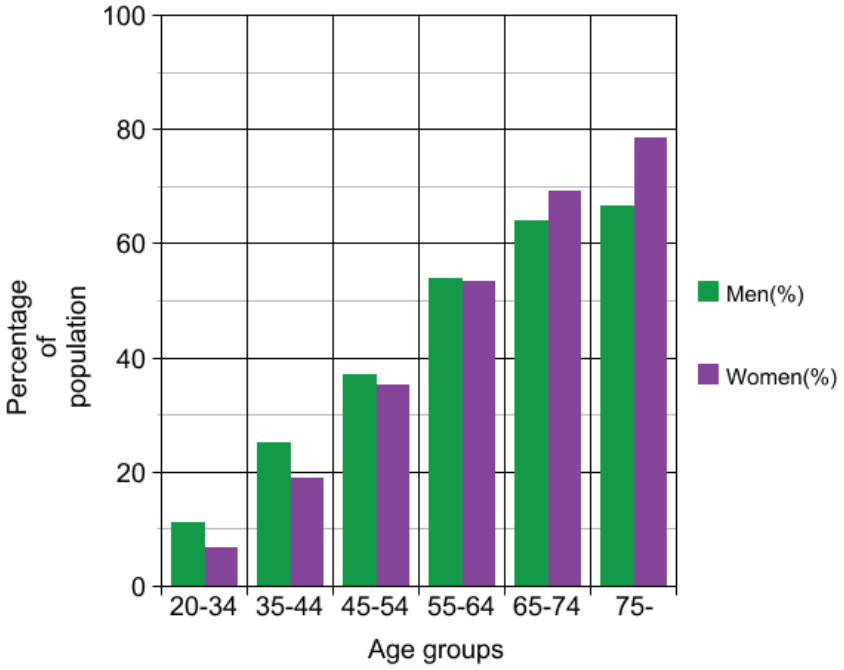

Figure 1 Age distribution of HBP patients in USA in 2011 as mentioned in [2]

The proportion of the world's population with HBP fell modestly between 1980 and 2008. However, because of population growth and ageing, the number of people with HBP rose from 600 million in 1980 to nearly 1 billion in 2008 [3]. From an economical perspective, in 2011 the cost related to HPB in the USA alone amounted to 46 billion USD [2] and worldwide it was around 1 trillion USD [4].

Diabetes is another chronic disease that is on the rise worldwide. While in 2011, 366 million adults, accounting for 8% of the adult population, had diabetes, the World Health Organization (WHO) is expecting this number to jump to 552 million adults, 10% of the adult population. This comes at a rate of 3 new cases every 10 seconds. Ten percent of diabetes patients have type 1 diabetes (T1D) which has much more serious consequences if the patients are not diagnosed quickly and if they do not receive insulin and skilled instructions on how to use it [5].

Children below the age of 14 years constitute a special group among T1D patients. Scandinavia scores the highest incidences in this group of T1D, as high as 35 cases per 100,000 people per year [6]. They need special guidance and attention to achieve good results while living with T1D. Monitoring the levels of glucose in the blood and adjusting the corresponding levels of insulin can be a challenging task for this group and a huge worry for their parents or care-takers. The health cost associated with diabetes varies from one country to another but, to get an idea, a diabetes patient's direct health cost goes up to 11,917 USD per patient per year [7]. On a worldwide scale, direct health cost of diabetes amounted to 376 billion USD in 2010 and it is expected to rise to 561 billion in 2030 [8]. Due to the huge cost associated with these services directed towards all the patients as a whole, many governmental funding agencies encourage research that uses the new portable technologies to realize what is referred to as e-health [9].

From another perspective, in recent years smart phones are becoming more popular and affordable for a wider segment of the global population. The majority of these smart phones offer different ways of connecting and communicating. Cellular communication (3G, 4G, …), WiFi, Bluetooth, IR and more recently NFC, are good examples of the type of communication facilities that can be available in one smart-phone. Recently, more and more mobile phone and smart-watch manufactures are focusing on adding extra features and communication channels to their devices. Thus, already there are a large number of smart-watches featuring Bluetooth and NFC communication links.

How can this huge advancement in communication technology be made use of to help give better health care for those needing it and at the same time reducing the cost as to meet the goals for different governments? Beneath e-health lies mobile health (m-health) that is growing at high speed. Even in developing countries, according to Vital Wave consulting [10], mobile phones reach further than other technologies and health infrastructures. Having mobile phones as a cornerstone in the efforts to improve health services at a reduced cost in developed countries has shown incredible results with patients. Monitoring, if automated, is one of the major operations that can be done on the patient's part with a flexibility that suits the patient. The results can be forwarded to a health station using Internet connections available in any smart phone, and can be analysed on the phone if needed and then forwarded as a different form of data to medical devices like insulin pumps, in the case of T1D. This can be represented as an implant monitoring different physiological parameters continuously or on demand, and communicating the results with a smart-phone.

The main goal of this work is to introduce a toolset that can be used to build complete electronic systems to monitor different physiological parameters from sensors using NFC technology as the means of interaction with them. The toolset includes, but is not limited to: analogue and digital sub-blocks forming an NFC tag; a unique standardized interface to facilitate the communication between multiple sensors and a tag; a benchmarking mechanism to define which NFC tag will fit the design requirements of the electronic system based on latency, data throughput and energy efficiency; an analogue to digital converter (ADC) using TDC to extract the zero crossing point in the I-V graphs of particular memristive nano-wire sensor; a mobile phone app to control different types of sensors with the ability to exchange custom-made commands between the phone and tag controlling the sensors; and, finally, an adaptive algorithm that runs on the mobile phone to check whether to process the sensed data before forwarding it to a server based on different criteria.

1.2 Methodology

We started from the question of how smart sensor nodes can and should be in a wireless sensor network (WSN). We defined how smart a sensor is, based on three criteria: communication, processing and storage. At the same time, there are other requirements that are specific for each node, itself based on its functionality that can be summarized by size, power consumption, range and,

finally, data throughput. Wireless technologies have different characteristics, as shown in Figure 2, which make some of them suitable for one scenario and not suitable for another.

WSN exists in different types with networks covering very small areas while others cover very large areas. For instance wireless body area networks (WBAN), which consist of a set of sensors, attached to the body or implanted, measuring the vital bio-parameters like heart rate, respiration, blood pressure, glucose level, temperature, electrocardiogram (ECG,EKG) and electroencephalogram (EEG), are characterized by:

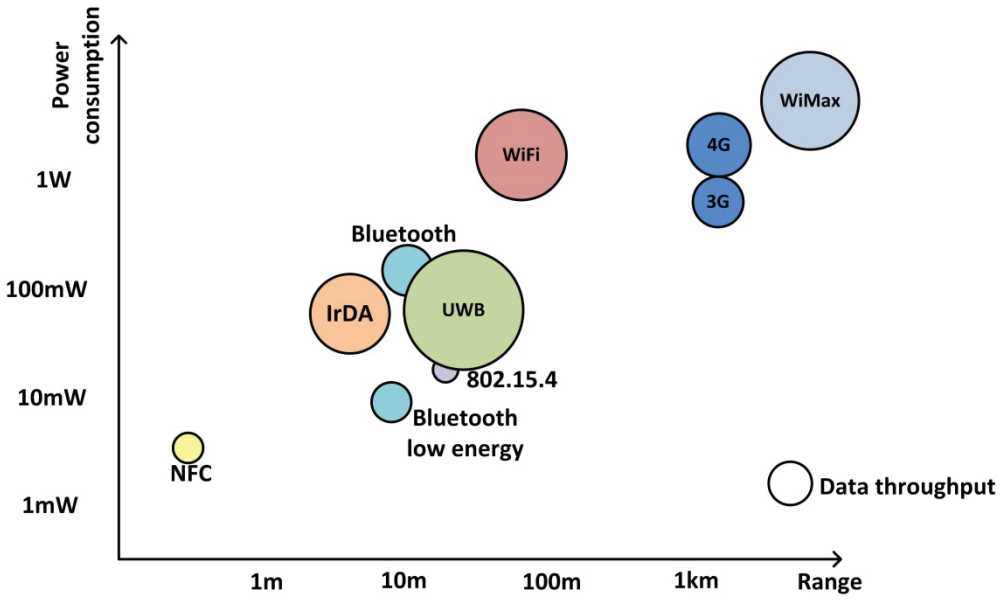

Figure 2 Wireless technologies plotted against range, power consumption and data throughput, modified from [11]

i. Energy and power limited.

ii. Low data rate (1kbps-100kbps in most case excluding ECG and EEG).

iii. Very low duty cycle in a sense that measured data does not change rapidly.

iv. Very short distance communication (less than 1m in most cases).

Environmental sensors, which can be spread around in nature to measure different readings like soil temperature, ground vibrations and fire weather index, share the same characteristics as WBANs except for the communication range. They need to be able to communicate over long distances, more than 100m in most cases. Radio transmission is the most energy-consuming activity when compared to data processing. According to [12], it takes on average 3J to transmit 1kb of data 100m at 1GHz, while you can use the same energy to execute 300 million instructions with a general purpose 100MIPS/watt processor[1]. Bearing this in mind, we developed an adaptive algorithm running on a mobile phone to decide the criteria for how to forward sensed data, if needed, to a server while being energy efficient.

WBANs composed of implants and/or on-body sensors, however, transmit only over a very short range. These sensors with their very small size can exist without a battery and they need to harvest energy from the surroundings. In such cases, NFC stands head and shoulders above the other

[1] A typical Intel I7 processor has around 5000MIPS/25watt, leading to around 200MIPS/watt [13]

communication protocols due to its inherit inductive coupling mechanism where data and energy are exchanged between the reader and the tag from a very close distance (less than 10cm). Eventually, NFC readers will power up the sensors while communicating with them to exchange information. Also, all NFC tags come with non-volatile memories of different sizes that can be used for data storage.

We started by investigating different alternatives for non-volatile memories, and the aim was to get a structure that is compatible with traditional CMOS technologies without the need to have extra masks. More specifically, different single poly non-volatile memory (NVM) structures were investigated by building an ASIC containing four different cells. Measurements in the lab were executed to characterize these cells.

The next step was to investigate which derivatives of the NFC tag structure suit our research. To do that, we developed a toolset to test and evaluate the performance of different NFC tags. The benchmarking objects included round-trip-time (RTT), data throughput and finally energy efficiency in cases of read/write and powering up only. The toolset is scalable to cover a wider range of tags than the ones tested. This toolset helped us in deciding which tag structure to design: tag type 1.

We developed a first ASIC that included the RF and the analogue parts of the tag, while we implemented the digital parts of the tag on an FPGA along with the sensor control block interfacing to the sensor front end. Since the interface between sensors and an NFC tag is not standardized, we worked on creating a protocol to connect multiple sensors with different characteristics running simultaneously to a tag. After extensive testing in the lab, with the help of an app on the mobile phone, another ASIC was developed to accommodate the complete tag structure and a sensor front unit. On a parallel track, a third ASIC containing a front end for a memristive nano-wire (NW) bio-sensor was developed as a cooperation project with EPFL. The fabricated ASIC was connected to the first ASIC and the FPGA, and with the help of the mobile app, we were able to run, control and read the results from a model of the memristive NW sensor. In all the developed NFC tag sensory systems, non-volatile memories were not introduced because the system will work only when the smart-phone is in proximity. In such a case, the sensed data can be stored on the smart-phone memory. By doing that, a lot of energy is saved because we no longer need to generate higher voltages to achieve tunnelling used while writing to Flash-memory. In addition, a smaller footprint tag will be achieved.

1.3 Dissertation Outline

This dissertation is a collection of papers published during the PhD period. The papers are meant to cover the whole system architecture from the transistor level to the application level on the smart-phone and later on a server. They are organized in chronological order in Part 2 where a short description of each paper precedes the papers.

Paper I presents an algorithm that works on the sensed data once available on the smart-phone and, based on different situations and criteria, a decision is made on how and when to transfer the sensed data forward to a server.

Paper II investigates different architectures for single poly non-volatile memory cells and introduces a new design aiming at achieving better performance and a smaller footprint compared to the others.

Paper III develops an ASIC hosting the front-end for memristive nano-wires sensors. It includes a control circuit, an ADC and, finally, a readout interface towards an NFC tag.

Paper IV works on creating a toolset that can help both software and hardware designers at an early stage to design NFC tag hardware and apps for specific application.

Paper V presents the first prototype we developed for a complete sensory NFC tag. It includes the power management system, along with the RF and analogue parts with the digital parts implemented on an FPGA. Simulation results and early measurements are presented.

Paper VI is an extended journal version of the Conference Paper V where the complete system is generalized to cover multiple different sensors running simultaneously. More weight is put on creating a unique and simple interface between the sensors and the NFC tag. Extensive measurements are done using the smart-phone app developed in Paper IV and the ASIC from Paper III. We present for the first time the control of the sensor from the smart-phone and receiving the result back on the smart-phone..

Here is the list of the papers:

I. Zaher, Ali, Ali Ahmad, Nicholas Dürr, and Nicolas Oliver Stamer. "Energy and latency impact of outsourcing decisions in mobile image processing." In *Computing, Networking and Communications (ICNC), 2013 International Conference on*, pp. 190-194. IEEE, 2013.

II. Zaher, Ali, and Philipp Häfliger. "Single poly non-volatile memory cells for miniaturized sensors in 90nm CMOS technology." In *NORCHIP, 2013*, pp. 1-4. IEEE, 2013.

III. Zaher, Ali, Philipp Häfliger, Francesca Puppo, Giovanni De Micheli, and Sandro Carrara. "Novel readout circuit for memristive biosensors in cancer detection." In *Biomedical Circuits and Systems Conference (BioCAS), 2014 IEEE*, pp. 448-451. IEEE, 2014.

IV. Dahl, Aage, Ali Zaher, and Thomas Peter Plagemann. "Android Based Toolset for NFC Tag Testing and Performance Evaluation." In *European Wireless 2015; 21th European Wireless Conference; Proceedings of*, pp. 1-8. VDE, 2015.

V. Zaher, Ali, Joar Særsten, Thanh Trung Nguyen, and Philipp Häfliger. "Integrated electronic system for implantable sensory NFC tag". In *Engineering in Medicine and Biology Society (EMBC), 2015 37th Annual International Conference of the IEEE* , pp. 7119 - 7122, 2015

VI. Zaher, Ali, Thomas Plagemann, and Philipp Häfliger. "Complete electronic system for implantable sensors using NFC technology". In *Circuits and Systems I, IEEE Transactions on*, under review, 2016

This dissertation is organized as follows: Chapter 2 presents the necessary background to put this current work in context. Chapter 3 presents a summary of the work as presented in the papers. Chapter 4 concludes this work and presents a roadmap for future research. The papers listed above are in Part 2.

Chapter 2

Background

This chapter is intended to give very brief background information necessary to understand the papers collectively and to see their individual contributions. It is a guideline for reading the papers and is not intended to act as an extensive review of the related work.

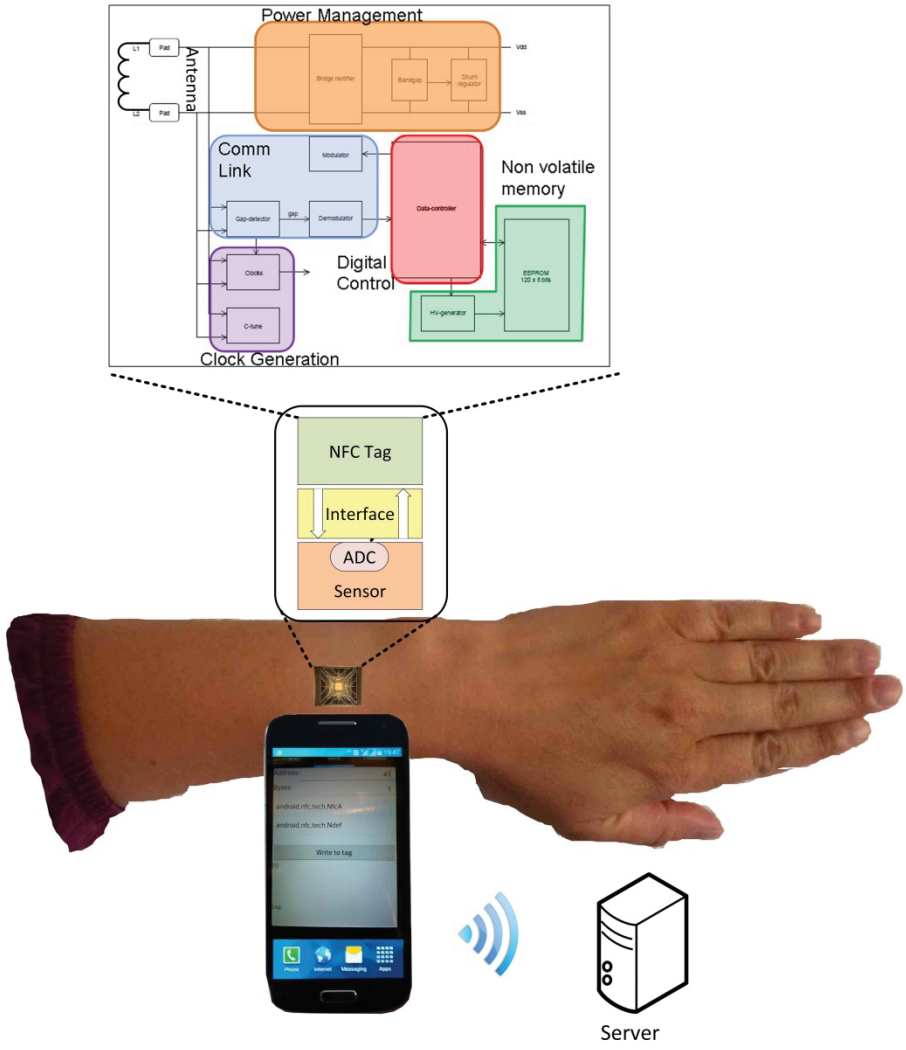

Figure 3 the complete monitoring system. It shows the implant, the mobile app and the server

Figure 3 shows how a complete system of monitoring vital parameters is structured. We have an implantable chip or an on-body chip, a smart-phone or a smart-watch, and a server. The smart-phone will function as a reader where it can power up, read and control the sensor on chip via an NFC link. It can store the data locally on the smart-phone memory, process it or run different algorithms on it, and can, under the command of the patient, be transferred to the doctor's server if needed. The chip contains one or more sensors, an NFC tag, and an interface which will allow the NFC tag to exchange data and control with the sensors. A central function of the sensor is to convert the sensor value to a

digital signal (analogue to digital conversion, ADC). This digital value can then be exchanged with the smart-phone. The following sections will cover the basic building blocks of the above architecture.

2.1 Sensor ADC

A significant power drain in the sensing subsystem is the ADC that converts an analogue sensor reading into a digital value. The power consumption of an ADC is related to the data conversion speed and the resolution of the ADC. It has been shown that there is a fundamental limit on the speed resolution product per unit power consumption of ADCs [14]. In what follows, I am going to discuss three main specifications of an ADC: number of bits, speed of conversion, and power consumption. The relationship between them is also discussed.

2.1.1 Number of bits (or Resolution): is the number of bits that an *ADC* uses to represent its analogue input [15]. Together with the dynamic range of the sensed parameter, it defines the smallest step we can detect, and consequently the resolution of the ADC. For example, if the glucose range to be measured varies between 20-500mg/dl, then a 10 bits ADC will give 2^{10}= 1024 levels where the difference between each level is $\frac{480}{1024} = 0.46875 mg/dl$. Then we can say that the resolution of this ADC is 0.46875mg/dl, which is equivalent to 1 LSB. If we need a smaller resolution, we can use more bits. On the other hand, if we know which resolution we are after, then we can calculate the number of bits needed to achieve that resolution based on the following equation:

$$n = \left\lceil \log_2 \left(\frac{Hlevel - Llevel}{Q} \right) \right\rceil \qquad \textbf{Equation 1}$$

Where n is the number of bits, $Hlevel$ is the highest level of the sensed signal, $Llevel$ is the lowest value of the sensed signal, and Q is the resolution we are after.

So, two factors affect how many bits we need for an ADC: How wide is the range we are sensing, and what is the needed resolution or accuracy?

There is another term used in relation to ADC and it is Effective number of bits (ENOB) which is smaller than the number of bits. It is defined as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \text{ (for an input sine wave)} \qquad \textbf{Equation 2}$$

Where SNDR stands for Signal-to-Noise-and-Distortion Ratio in dB. Since any electronic implementation of an ADC will introduce noise and distortion to the sampled signal, it is then worth looking at $ENOB$s of different ADCs to see which has the better implementation.

2.1.2 Speed of conversion: This is time the ADC needs to produce a new digital value reflecting the change at the input. This depends on the frequency of the input signal; how fast the change is occurring at the input, or which bandwidth the input signal has. It also depends on the sampling frequency; how fast the ADC is sampling the changing input signal. Usually to avoid aliasing, the sampling frequency should be higher than 2x the bandwidth of the input signal.

Thinking about physiological parameters, we can classify them based on how fast the changes occur in their values. Glucose level and body temperature are two parameters that do not change abruptly. Usually it is in the range of minutes before we notice a change of 1mg/dl [16]. However, heart beat and blood pressure values do vary at shorter intervals, within a few seconds. Moreover, since the heart beat varies between 30 to 200 beats per minute in an adult, the sampling frequency can theoretically be a few tens of Hz, so as to get the heart beat results within a few seconds. ECG and EEG signals have a wider bandwidth and contain more details in a milliseconds scale. The sampling frequency for ECG has a minimum recommended value of 128 Hz [17], where the prevailing sampling

frequency in many research sources varies between 500Hz to 8000Hz. Tsai and colleagues [18] use an 8 bit Successive Approximation ADC (SAADC) running at 10kHz to record the ECG.

For EEG the sampling rate varies between 250Hz and 2000Hz [19]. One thing to notice with EEG is the number of channels that are recording. Current numbers can go up to 64 or even 128 channels. If we are using 12bits ADCs, and we are sampling at 1024 Hz, with 32 channels, then we are recording data at the rate of 32x256x12 = 96kbps. One of the latest designs in neural recording is using 8 bits ADC to record on 32 channels with a frequency of 31.25kHz [20]. This can set a requirement on the communication channel that is used to transfer the data or on the memory where the data is stored.

Number of bits and the sampling frequency together can decide which ADC architecture to use to fulfil the requirements, as shown in Figure 4. This figure shows a typical case scenario, and of course different ADCs can be used in other areas too. Notice that our area of interest is the lower left corner of the graph where we have low sample rate and a lower resolution.

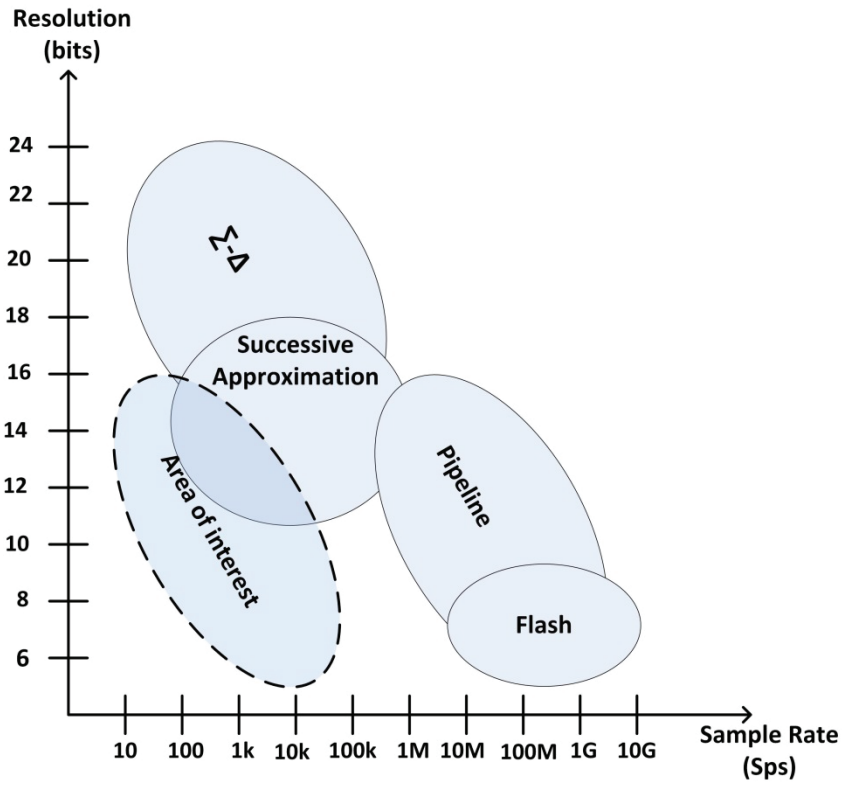

Figure 4 Typical areas where different ADC technolgies are used. Modified from Kester [21]

2.1.3 Power consumption: ADC topologies can use quite different ranges of power. It depends on the algorithm and the implementation behind. A theoretical lower limit on power consumption has been proposed to serve as a guideline for designers. One limit mentioned by Kenington and Astier[22] is based on the idea that, for an ADC to take full advantage of the resolution available to it, the quantization noise power must be lower than (or possibly equal to) the thermal noise power present at the converter input. This will lead to the following equation after some manipulation:

$$P = KT \times 10^{\frac{6n+1.76}{10}} \times Fs \qquad \textbf{Equation 3}$$

Where K is the Boltzmann constant, T is the temperature in Kelvin, n is the number of bits the ADC has, and Fs is the sampling frequency. Notice that the power consumption is independent from the range of the sensed parameter, in this equation. Needless to say, this equation is setting a lower limit

on the power consumption and, in practice, the power consumption will exceed the value obtained from this approach.

From the above equation, we can see how power consumption is affected by the resolution or the number of bits, and the sampling frequency at which the ADC is running. Increasing the number of bits linearly will increase the power consumption exponentially. As for sampling frequency, it is a linear relationship that governs its relationship to power consumption. Figure 5 shows the theoretical power consumption of ADCs with different number of bits and how it develops with an increasing sampling rate.

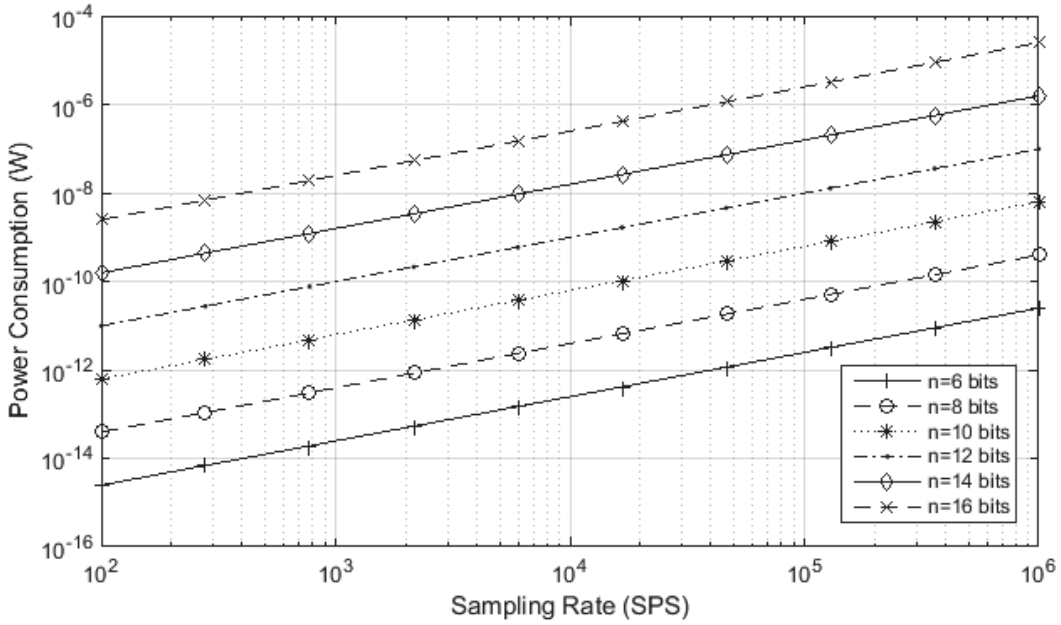

Figure 5 the relationship between power consumption, sampling rate and resolution, regenerated from Kenington and Astier [22].

To be able to compare power effectiveness of different ADCs having different number of bits, running at different sampling frequencies and of course having different topologies or architectures, a figure of merit is used to describe how many Joules are used to do one conversion. The basic figure of merit is defined as:

$$FoM = \frac{P_{total}}{2 \times BW \times 2^{ENOB}} \qquad \textbf{Equation 4}$$

Where P_{total} is the total power used, BW is the bandwidth of the sensed signal, and ENOB is the effective number of bits of the specific converter. An ADC with FoM smaller than 1pJ/conversion is considered an effective ADC.

2.2 NFC tag

The NFC protocol defines a communication protocol between two readers or between a reader and a tag. An example of a communication between two readers is when two mobile phones exchange files by touching each other. An example of a reader communicating with a tag is using a ticket card on a bus, or an access card in a building, where the ticket/card is the tag and needs to be held close to a reader terminal. The NFC tags can be classified into different categories. An NFC tag can be active or passive based on the availability of a power supply. A tag that has its own power supply is classified as an active tag, while tags that depend on the reader to power them up are passive tags. Among

passive tags, there are different types that can be categorized into five types based on data rate, memory size and which standard for communication they use, as shown in Table 1.

Other characteristics that differentiate between one tag type and another are hardware complexity, security and encryption. To know which tag to design to suit a specific application, we developed a benchmarking toolset where we define application requirements and add to the above criteria (memory size and data throughput) Read and Write energy efficiency and powering up energy efficiency to get a better picture about power consumption on the reader side. The result of this toolset will present how each tag meets the requirements set above. Once a tag is a chosen, the design process will start.

Tag	Standard	Android Protocol	Memory	Bit rate
Type 1	ISO 14443A	NFC-A	96B-2KB	106Kb/s
Type 2	ISO 14443A	NFC-A	48B-2KB	106Kb/s
Type 3	JIS 6319-4	NFC-F	2KB-1MB	212Kb/s
Type 4	ISO 14443A-B	NFC-A,B	32KB	106Kb/s-424Kb/s
Mifare	ISO 14443A-B	NFC-A,B	1KB-8KB	106Kb/s-424Kb/s

Table 1 Characteristics of different tag types

Tags have been used as means of sensing in different situations. Yeager et al. [23] use a 900MHz frequency compatible tag without a memory to sense bio-signals. [24] use an NFC tag to read glucose levels in the human body. [25] and Kassel et al. [26] use NFC compatible tags to connect different chemical and biological sensors in industry environments.

How suitable is NFC to deliver energy to the in-body and on body sensors? And in case of in-body sensors, do NFC electromagnetic waves exhibit any danger to the human tissues surrounding the implanted sensors? To answer these questions, we are going to present the reader-tag inductive power transmission where the system can be modelled as shown in Figure 6.

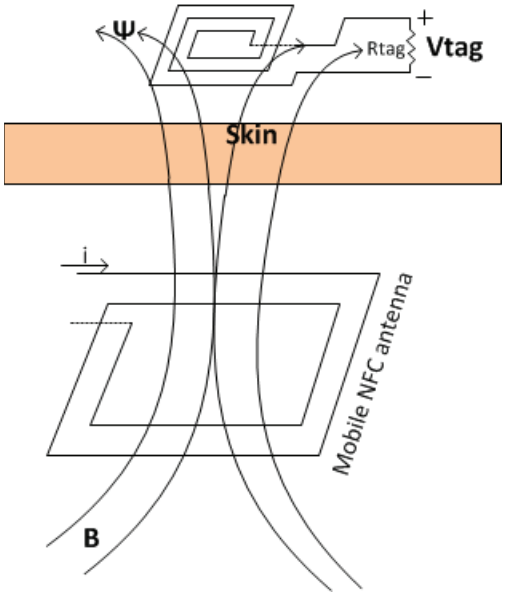

Figure 6 Inductive coupling between the NFC reader and the tag

Since the distance between the reader and the tag is very close and much smaller than $\frac{\lambda}{2\pi}$ (Where λ is the wavelength of the wave defined as the speed of light divided by the frequency of the signal, 13.56M in case of NFC), in this case around 22 meters, then it is mutual inductance between the NFC reader coil and the NFC tag coil that determines the amount of energy induced in the tag.

According to [27] the Magnetic flux density around the NFC reader coil is defined as in Equation 5:

$$B = \frac{\mu_0 I N a^2}{2r^3}\ Weber/m^2 \qquad \textbf{Equation 5}$$

where I is the current through the NFC reader coil, *N* is the number of windings in the NFC reader coil and a is its radius, μ_0 is the permeability of free space ($4\pi \times 10^{-7} H/m$) and finally *r* is the perpendicular distance from the NFC reader coil centre to the point of observation.

The NFC tag coil will try to capture as much as possible of this magnetic flux and transfer it in to current/voltage according to Equation 6:

$$V = -N\frac{d\Psi}{dt}$$

$$\Psi = \int B.dS \qquad \textbf{Equation 6}$$

$$V = 2\pi f.N_{tag}.Q.B.(S.cos\alpha)$$

where *S* is the area of the tag coil, N_{tag} is the number of windings in the NFC tag coil, f is the frequency of the wave, α is the alignment angle between the centres of the two coils, and *Q* is the quality factor of the resonant circuit and can be defined as:

$$Q = \frac{1}{\frac{R_{coil}}{2\pi f L_{tag}} + \frac{2\pi f L_{tag}}{R_{tag}}} \qquad \textbf{Equation 7}$$

where R_{tag} is the equivalent resistance of the whole tag, R_{coil} is the resistance of the NFC tag coil, and L_{tag} is the inductance of the NFC tag coil and it depends on the shape of the coil, radius of the coil, number of the windings, thickness of the windings, length of the coil. For a square shape coil, as the one shown in Figure 7, L is given by Equation 8:

$$L = K1 \times \mu_0 \times N^2 \times \frac{d}{1 + K2 \times p} \qquad \textbf{Equation 8}$$

where *d* is the mean coil diameter (dout+din)/2, p is (dout-din)/(dout+din), *N* is the number of windings, and *K1* and *K2* depends on the shape and in this specific case, they are 2.34 and 2.75 consecutively as presented in [28].

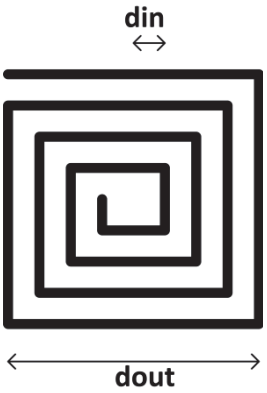

Figure 7 A layout of a rectangular NFC antenna

Absorption of EM waves by the tissue body, which consists of mostly saline water, accounts for a major portion of the propagation loss from the NFC reader to the implanted tag [29], and this is the reason why most studies uses saline solutions to emulate the effect of a human tissue as in [30]. Back to the absorptions of EM waves, they can become harmful since they can warm up the tissue and damage the cells around the implant. This depends on many factors including the frequency, size of the exposed tissue, duration of exposure among other factors. To quantify this process, a specific absorption rate (SAR) is defined as the incremental energy absorbed by an incremental mass contains in a volume element of a given density [31], and can be modeled as in Equation 9:

$$SAR = \frac{\sigma|E|^2}{p} W/kg \qquad \textbf{Equation 9}$$

Where σ is the conductivity of the tissue, p is the mass density of the tissue, and E is the RMS of the electric field strength. The EU R&TTE Directive 1999/5/EC covers NFC Devices where product standard EN 50364 is applied. In this standard, SAR higher limits are given over 10 grams of contiguous tissue over a period of 6 minutes, and for head and trunk it is 2W/Kg, and for the limbs it is 4W/Kg when the frequency is in the range of 10MHz-10GHz. In an experiment done by [30], it is shown that the maximum SAR measured with the tested mobile phones is 2 orders of magnitude lower than the EU recommendations. As a conclusion, personal exposure due to NFC devices causes SAR levels very far below the limits.

This leads us to the question about if NFC waves with the losses they face by reflection at the interface between the skin and the air, and the losses due to attenuation done by the skin itself, can penetrate the skin enough to power up electronic devices implanted inside. [32] has done some experiments where different tags with different sizes of antennas had been covered by different number of layers of beef fat, and with an NFC reader try to communicate with the tags. The tags were also packaged with a 12um thick plastic layer to protect them. Experiments showed that with 11mm thick fat, and an antenna with the size of 22x38mm, the reader was able to communicate with the tag from a distance of 7cm above the fat layer. This gives us a bigger margin to scale down the tag antenna to a limit where it is implantable and at the same time big enough to capture magnetic flux generated by the NFC reader at a distance of few millimeters from the skin.

In what follows I am going to present four major parts that exist in different NFC tags: Non-volatile memory, Power harvester, demodulator and, finally, the interface to a sensor. In addition, a short introduction to memristive sensors is presented.

2.2.1 Non-volatile memory (NVM):

The main use of the NVM is to store the unique ID of the tag, some configuration bits, and the data that is indented to be stored. As we see in Table 1, different tag types have different sizes of memories, varying from hundreds of bytes to few MBs. There are four major different technologies to design NVMs already used commercially today (and others that are under development): Flash memories, Ferroelectric memory, Magnetoresistive memory and finally Memristive memory.

Flash Memory:

Traditionally, a Flash memory makes use of charge stored on a floating gate to accomplish non-volatile data storage. This requires in general that the technology offers a two-poly option where there is an oxide layer separating one poly from another. To store this charge, two main methods can be used: Fowler – Nordheim (FN) tunnelling through thin oxides and Channel Hot electron Injection (CHI). In FN tunnelling, a high electric field of 10MV/cm (equivalent to 10V/10 nm thick oxide) is needed, as shown in Figure 8, where the figure to the left is tunnelling the electrons from the bulk/channel to the gate (programming), and the next figure is doing the opposite (erasing). The main effect of tunnelling on the transistor is the change to the threshold voltage of the transistor. Thus, a read voltage applied to the control gate may or may not open the transistor, dependent on the charge stored on the floating gate. Based on the sensed current, one case will match a stored '1' and the other will match a stored '0'.

Charge pumps are needed to achieve high enough voltages for FN-tunnelling with VDD at 1v and below in modern technologies. This will be another circuit that consumes energy. Also, as technology scales down, so does the oxide's thickness and VDD, as it appears in Table 2. On one hand, this is positive since lower voltages are required to achieve FN-tunnelling, but on the other hand, gate leakage occurs as the oxide thickness goes below 6nm, limiting the retention of stored charge.

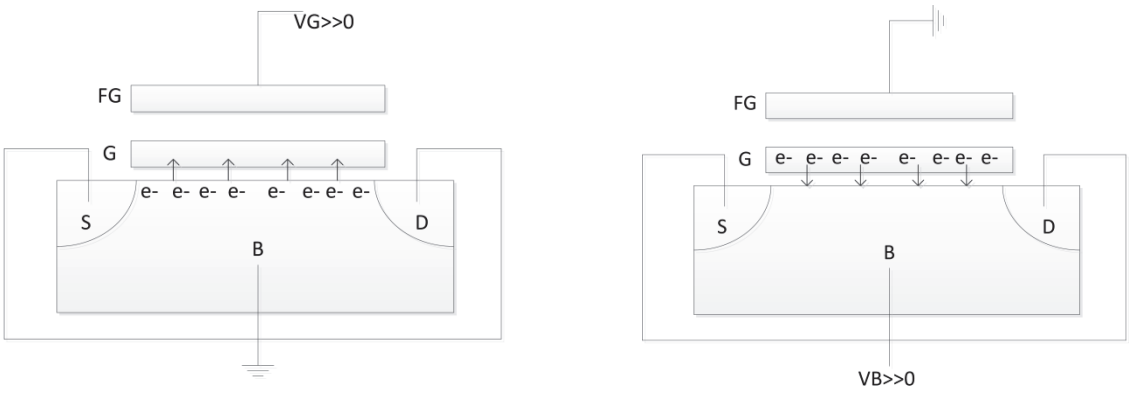

Figure 8 FN tunnelling to programme and erase a cell. High voltage is applied on the gate to trap the electrons in the floating gate while programming. A high voltage is applied to the bulk to release the electrons from the floating gate

Tech Node (nm)	tox(nm)	Vdd (V)
130	3	1.2
90	2.4	1.1
65	1.7	0.9
45	1.5	0.8
32	1.4	0.7
22	1.3	0.6

Table 2 Technology nodes with the corresponding oxide thickness and power supply value. Modified from [33]

Even with these difficulties, manufacturers were pushing the limit when they recently announced NAND structured Flash memory hosting 256Gb on 3-bit multi level [34]. Of course the target of these memories is hard disks and higher density memories. Another approach that appeared a few years ago is to use single poly technologies to create the cells where you can trap the charge. Instead of building vertically where the oxide is between the polys, single poly solutions focus on separating the two gates from each other horizontally, as it appears in [35] and [36]**.**

To achieve high voltages above VDD, charge pumps or voltage multipliers are used. They are a special type of DC-DC converters where the output voltage is bigger than the input voltage. A simple circuit presented in [37][Charge pumps: An overview.] showing a charge pump is presented in Figure 9:

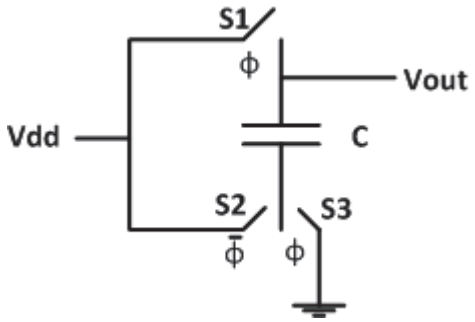

Figure 9 An illustration of a simple voltage doubling charge pump

Clock signals ϕ and $\overline{\varphi}$ are out of phase. When switches S1 and S3 are closed, the capacitor is charged to with Q= C x Vdd. When the S1 and S3 are opened and S2 is closed, the charge is still contained in the capacitor, generating a voltage of Vdd across the terminals of the capacitor. Since the bottom plate of C is still connected to Vdd via S2, then Vout will have a 2Vdd potential above ground. By doing so, double the supply voltage is presented at node Vout. Of course this analysis doesn't take into consideration the load connected to Vout, practical implementation of the switches, and other losses around the capacitor.

More complex designs like Dickson charge pump [38],switched capacitor techniques [39] and [40] use different approaches to counter act the effects mentioned above as well as to improve the efficiency of the charge pump.

Generally speaking, writing to a Flash memory is power consuming due to rather ineffective charge pumps to generate high voltages. So what about ultra-low power and sub-threshold CMOS circuits, where the power is harvested and not supplied via a battery or a main supply, like the work we have at hand here?

Ferro Electric RAM (FeRAM):

FeRAM stores the data by modulating the polarization of a ferroelectric capacitor and sensing the charge-versus-voltage response when it needs to read. The read operation is a destructive read. For this reason, a read state is always followed with a write state of the previous sensed value. FeRAM was first proposed by a master thesis from MIT in 1952 titled "Ferroelectrics for Digital Information Storage and Switching" [41]. A low Voltage 1 Mb 1T1C FRAM fabricated in 130 nm CMOS that operates from 1.5 V to 1.0 V with corresponding access energy from 19.2 pJ to 9.8 pJ per bit was presented in 2012 [42]. Before that, in 2007, an embedded 2 KB FeRAM has been introduced to work in Radio Frequency Identification (RFID) tag running at a 953-MHz carrier, implemented in 0.35um CMOS/FeRAM technology [43]. Between these two, in 2010, a 128Mb FeRAM chip was presented with the target of high speed and high density non-volatile memory applications using 130nm CMOS technology [44]. Texas Instruments has introduced their MSP430FRx FRAM microcontroller where the FeRAM has replaced the Flash Memory with sizes ranging from 4 KB to 128 KB. All of these designs share the advantage of FeRAM, which can be summarized in:

i. Low voltage requirements (1 volt switching).

ii. High speed write operations (<10ns).

iii. Low energy consumption (1000x lower than Floating gate NVM).

iv. Up to 10^16 access cycles.

Disadvantages are that FeRAM requires a high temperature during integration (>500 C), a larger cell size compared to Flash, and finally the destructive read nature. FeRAM density is still far below that of Flash memory.

Magnetoresistive RAM (MRAM):

An MRAM memory cell is made up of two ferromagnetic layers separated by a thin insulator layer. Each ferromagnetic layer has a polarization. MRAM stores the information by modulating the polarization of one of these layers. This leads to different resistance values based on the direction of the polarization. Reading out the value will be sensing the current through the cell. Different formats of MRAM do exist, like Anisotropic magnetoresistance (AMR), Giant magnetoresistance (GMR), Spin dependent tunnelling (SDT) and, finally, Magnetic Tunnel Junctions (MTJs).

If the magnetizations of the two layers are aligned, it is more likely that the electrons can tunnel leading to a low resistance (R_{low}). Alternatively, if they are opposed the resistance is higher (R_{high}). We define tunnel magnetoresistance (TMR) as:

$$TMR = \frac{R_{low} - R_{high}}{R_{low}} \qquad \textbf{Equation 10}$$

For reliable readout or even multilevel storage, TMR should be as high as possible. Currently, 200% TMR is achievable. MRAM has the advantage of high performance when it comes to write and read

speed[2] and it can work at a low voltage similar to the core voltage of modern CMOS. However, low TMR does not allow multi-level storage. Furthermore, a bigger cell pitch is required to avoid cross talk when writing to a cell. Therefore MRAM does not have high density compared to Flash memory[3]. On power consumption, MRAM requires high write currents in the range of hundreds of uAs. This does not make it attractive for ultra-low power designs.

Memristive RAM:

Memristors can be defined as all 2-terminal non-volatile memory devices based on resistance switching, regardless of the device material and physical operating mechanisms. This definition is mentioned in Leon Chua's paper from 1971 [45]. The idea is to achieve a very high difference between one resistance state and another. If the difference can be controlled gradually, then multi-level cells are possible too.

One type of Memristive RAM is Phase Change RAM (PRAM). It stores the information as the resistance change of a dielectric switching between amorphous (high resistance) and crystalline (low resistance). In 2012, Samsung announced a 1.8V 8Gb PRAM using 20nm technology [46]. PRAM has good characteristics, like its higher density compared to MRAM and FeRAM, its very high ratio between R_{high} and R_{low} (more than 100 times) and, finally, its fast write operation. On the other hand, it uses a high write current of hundreds of uAs and unfortunately this current does not scale down with technology scaling, leading to high current densities.

Another type of Memristive RAM is Conductive Bridging RAM (CBRAM). It stores the information by modulating the resistance of a dielectric via transport and reduction of ions. Typical materials contain silver, though other materials exist. Switching happens at low voltages with low currents, which makes it attractive for low power designs. On top of that, the ratio between R_{high} and R_{low} is extremely high (up to 10^8 times), which makes it perfect for multi-level cell implementations. Resistive RAM (ReRAM) is quite similar to CBRAM but instead of oxidization, applying higher voltage leads to defects or metal migration, creating a conductive path. In 2013, Toshiba announced a 32Gbit ReRAM chip in 24nm technology with multi-level cell (MLC) [47].

Both ReRAM and CBRAM work on low voltages and low currents, and have a fast switching read/write cycle below 50ns. They offer a low energy consumption compared to floating gate NVM, as well as high density and they are highly scalable below 20nm. Still, they face some challenges like noise immunity at sub-threshold voltages, and the low endurance they have (10^7 write cycles can be done before the material degrades, and the cells cannot be used).

As we can see from the above description of these different memory types, the technology decides a lot. Above 20nm, some NVMs are more suitable than others. Below 20nm, quite a few scale down. Another important factor that affects which memory to use is the application itself. Having ultra-low power applications where the energy is harvested from the surroundings will tend to favour NVMs that are quite energy efficient and do not require high voltages or currents for reading or writing.

2.2.2 Power Harvester:

The power harvester for an NFC tag consists of a rectifier, which translates an AC signal appearing across the terminals of the antenna into an unregulated DC signal. Before using this signal to supply power for the electronics, it needs to be regulated using a voltage regulator. If the electronic circuit contains different power domains or has mixed signal design where there are analogue parts and digital parts, it is important to separate the power supplies and this translates to multiple voltage

[2] Below 10ns, March 2011– PTB, Germany, announces having achieved a below 500ps (2GBit/s) write cycle on MRAM

[3] November 2012 - Chandler, AZ, USA, Everspin debuts 64Mb ST-MRAM.

regulators, to avoid noise appearing due to switching in the digital circuit on the analogue power lines.

There are two main types of rectifiers: passive and active. Passive rectifiers use, for instance, diode connected transistors as switches to enable the current to flow in one direction during one cycle. To achieve that, the input AC signal should be high enough to turn on this switch (i.e. exceed the diode threshold), basically higher than the Vth of this specific transistor. This will unfortunately lead to a dead zone where the rectifier is not passing any current when the input signal is below Vth. Knowing that Vth does not scale well with the scaling down of the technology and that harvesting energy for implants deals with small amplitude signal attenuated due to the penetration loss, this can become a real problem facing the design of a power supply for NFC tags meant for implants. Active rectifiers on the other hand try to solve this problem by using an additional power supply to bias the gate of the transistor, so effectively removing the dead zone created by Vth. Although this works quite well in many designs, it is not possible with the design targeting implants due to lack of any other power source. Another approach is to use self-cancellation Vth schemes (SVC) where we no longer need an extra power supply; instead the gates of the transistor are connected in a manner insuring that, as the output voltage increases, the Vth of the NMOS transistor decreases [48]. The early designs of SVC faced the dilemma of trading the ON resistance of the transistor for the cost of increasing the leakage current. Kotani and colleagues [49] proposed a solution for this problem known as a differential drive CMOS, as shown in Figure 10. Such a rectifier solves the problems mentioned before, plus it is scalable. If we want to achieve higher output voltage, then we can cascade a few of this structure side by side, and then the new structure will function as a voltage multiplier.

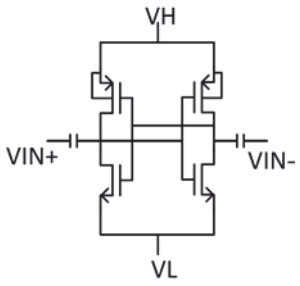

Figure 10 A differential drive CMOS rectifier unit

Voltage regulators work by first generating a stable reference voltage and then using this reference voltage in a feedback loop to create a proportional desired output voltage. First let us start by looking at a voltage divider taking as an input the unregulated output of the rectifier, as it appears in Figure 11:

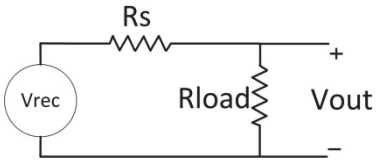

Figure 11 A simple voltage divider circuit where V_{out} needs to be regulated and V_{rec} is the unregulated input

$$V_{out} = V_{rec} \times \frac{R_{load}}{R_{load} + R_s} \quad \textbf{Equation 11}$$

$$V_{out} = I_{load} \times R_{load} \quad \textbf{Equation 12}$$

So, if I_{load} or V_{rec} change, so does V_{out}, and this is not good. If we can somehow change R_s in a manner that if I_{load} changes, then V_{out} stays constant:

$$R_s = R_{load} \times \frac{V_{rec} - V_{out}}{V_{out}} \quad \textbf{Equation 13}$$

And $V_{rec} - V_{out}$ is the drop voltage across R_s. From **Equation 11** and **Equation 12**, we are interested in controllable R_s that has a small value to create a low drop output, as it appears in **Equation 13**, and here, in the picture, comes a Low Drop Output (LDO) regulator. An LDO regulator needs to sense the output voltage and then use this sensed value to change R_s. R_s can be implemented as PMOS transistor as it appears in Figure 12:

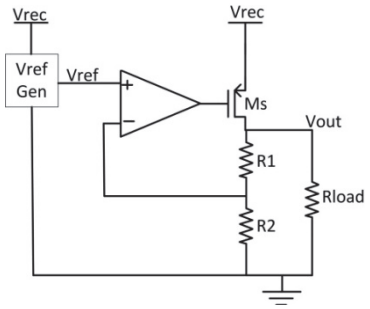

Figure 12 A simple circuit for a Low Drop Output regulator

The dropout through the PMOS transistor is $V_{DS(SAT),}$ which is a small value, and the sensing and the correction circuit can be both a voltage divider in parallel with the load and an error amplifier. The ratio of the resistors in the voltage divider decides the value of the output voltage in relation to V_{ref} based on Equation 14:

$$V_{out} = V_{ref} \times \frac{R_1 + R_2}{R_2} \quad \textbf{Equation 14}$$

The amplifier output will control the gate of the PMOS transistor to react to the change across the load. To make the negative feedback more stable, a capacitor can be added between the output and the negative input of the amplifier. In general V_{ref} will be generated using a bandgap circuit to be invariant to changes of temp and voltage. But since the aim is to use it at body temperature, a simpler design can be used where V_{ref} is invariant to changes of V_{rec} as it appears in Baker, Chapter 23 [50].

2.2.3 ASK Demodulator:

As it appears in Table 1, the NFC protocol exists in 3 main types: NFC-A, NFC-B and NFC-F. These protocols differ from each other on a multiple of different requirements when it comes to analogue and digital. But one thing in common is the modulation scheme they all use to communicate on the downlink channel between the reader and the tag. They all use ASK modulation with different modulation index as summarized in Table 3:

	Downlink (Reader to tag)	Uplink (Tag to reader)
NFC-A	Modified Miller coding with ASK 100% modulation	Manchester coding with load modulation (ASK)
NFC-B	NRZ-L coding with ASK 10% modulation	NRZ-L coding with load modulation (BPSK)
NFC-F	Manchester coding with ASK 10% modulation	Manchester coding with load modulation (ASK)

Table 3 Different modulation schemes are used in uplink and downlink across different NFC technologies

Where the modulation index defined as in **Equation 15**:

$$Modulatio\ index\ = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \times 100 \qquad \textbf{Equation 15}$$

And V_{max} and V_{min} as they appear in Figure 13.

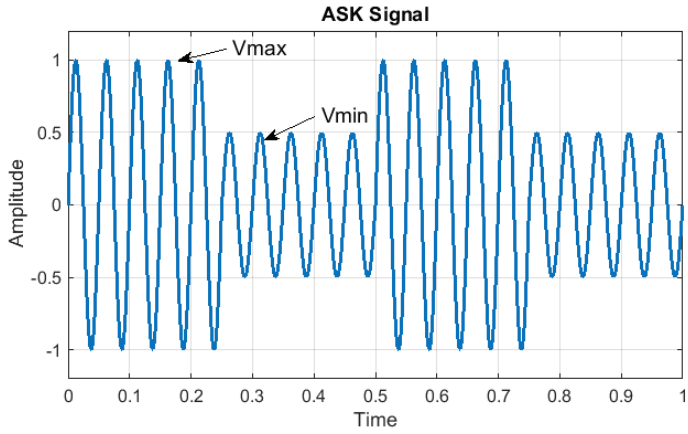

Figure 13 A typical ASK signal modulated across time. A similar signal appears across the antenna of the NFC tag when the reader is sending data to the tag

As we can see from the figure, the base-band data is the envelope of the ASK. Most of the available demodulator circuits use an envelope detector, and it is typically a low pass filter as it appears in [51], [52], [53], [54], [55] and [56] where all of them except Lee and Lee [56]use a capacitor to achieve this low-pass filter (LPF). Lee and Lee use, instead, a resistor in the design. Djemouai and Sawan [47] use a different approach from LPF where it focuses on building a current steering circuit to extract the demodulated signal[57], and, finally, Wang and colleagues[58] [48] use a Schmitt trigger to achieve the envelope detector. They use also a resistor in their design. For an implant that is very space limited, having a capacitor or a resistor is unfavourable because of the big space they occupy. A circuit as presented in [59] does not use any R or C and works with different modulation indexes, which is also preferable. When designing an ASK demodulator for NFC protocol intended for an implant, two criteria can be placed at the top: Low foot-print, and low power consumption. Having a general purpose ASK demodulator that can demodulate with a wider range of modulation indexes can be looked upon as an achievement as long as it meets the requirement of power and space.

The data on the uplink in NFC-A is exchanged with the NFC reader using Load Shift keying, known shortly as load modulation. This happens when the tag controls the load appearing across the tag

antenna. As the load changes, the reflected magnetic wave changes, and this change will be sensed by the NFC reader unit. Once sensed, any data embedded inside the load modulated signal will be retrieved by the reader. The data on the uplink is encoded using Manchester coding and it is modulated with a carrier frequency of 847 KHz generated by dividing the 13.56MHz extracted clock by 16. This generates two sidebands on both sides of the 13.56 MHz carrier separated from the main central frequency by 847 KHz each. In these two bands lies the uplink information. Figure 14 shows how a simple load modulator interacts with the tag antenna.

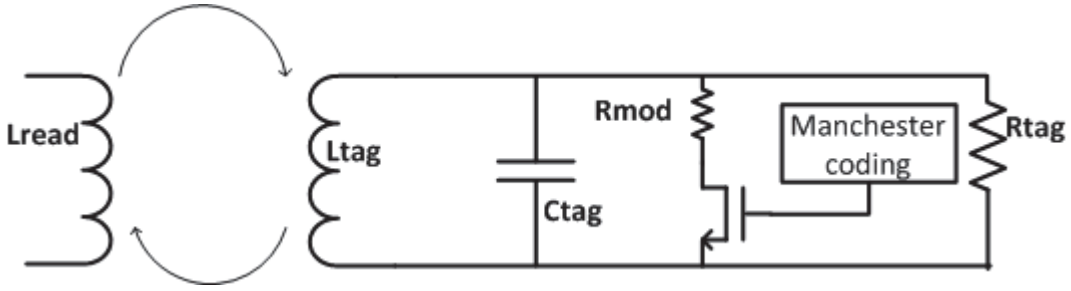

Figure 14 Load modulation used to send the data from the tag to the reader

2.2.4 Sensor interface:

To make the sensor accessible for the smart phone, the sensor needs to be connected to the NFC tag. The sensor should be able to receive a start signal to start sensing, a configuration word perhaps (in case the sensor runs in different modes), should be able to tell the tag when it has finished sensing, and should finally transfer the sensed data to the tag, so that the tag can send it up to the smart phone. Different standards exist to facilitate the communication between two devices like SPI, and I^2C. Both try to limit the number of lines of the interface to the minimum. To be able to send a configuration word to the sensor, the sensor needs to be memory mapped to a specific address in the tag's memory. Writing to that address is equivalent to writing the configuration register of that sensor. The same concept applies for the result. The tag writes the sensed data to a specific address assigned for the sensor in the memory. The memory in the tag will look like that in Figure 15.

To transfer the data between the sensor and the tag, the clock from the tag needs to be forwarded to the sensor even if the sensor runs on a different clock. This is needed so as to achieve a synchronous transfer of data. An interrupt can be used to notify the tag that a sensor has finished sensing and that there is available data to transfer, and an acknowledgment can be sent from the tag to sensor to initiate the transmission. The tag will act as master and the sensor will act as a slave during the transmission. Figure 16 shows a typical case where the tag starts the sensor, and reads the result afterwards.

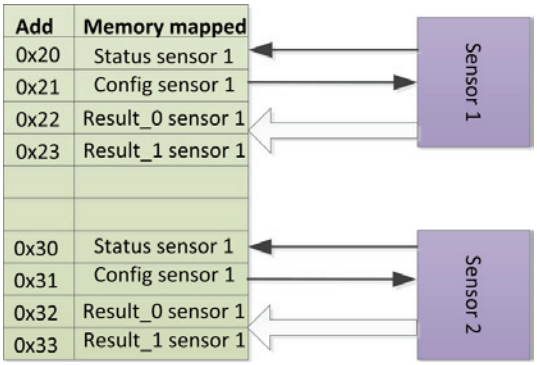

Figure 15 Typical memory-like distribution of sensors' registers. Each sensor is memory mapped to specific tag addresses so as to make the sensors accessible for the reader

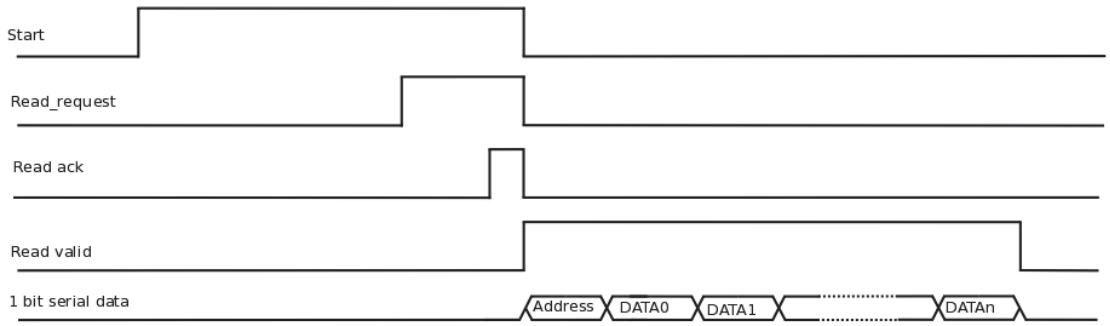

Figure 16 The interface protocol between the NFC tag control and the sensor.

2.2.5 Memristive Nanowires:

Nanowires that present a memristive effect where the I-V curve is a pinched hysteresis loop crossing (0,0), as shown in (C) in Figure 17, are considered as memristive devices and have been used as mentioned before in achieving resistive RAMs. Lately, they have been used in sensing biomarkers in the air [60] and in bio-sensing in general [61]. These nanowires after being fabricated with NiSi Schottky-barrier junctions, they are functionalized by bounding antibodies to them. Once they are functionalized, the I-V curve of the nanowire changes, and then the forward and the backword I-V curves cross zero at non-zero voltages. The voltage difference between these two crossings is what we refer to as a voltage gap, as shown in (D) in Figure 17. When the nanowire is dipped in the liquid to be sensed, the antigens are attached to the antibodies, and depending on the concentration of the antigens, the voltage gap will reduced accordingly. As can be seen in (E) of Figure 17, the concentration of the sensed material is directly proportional to the delta-change in the voltage gap.

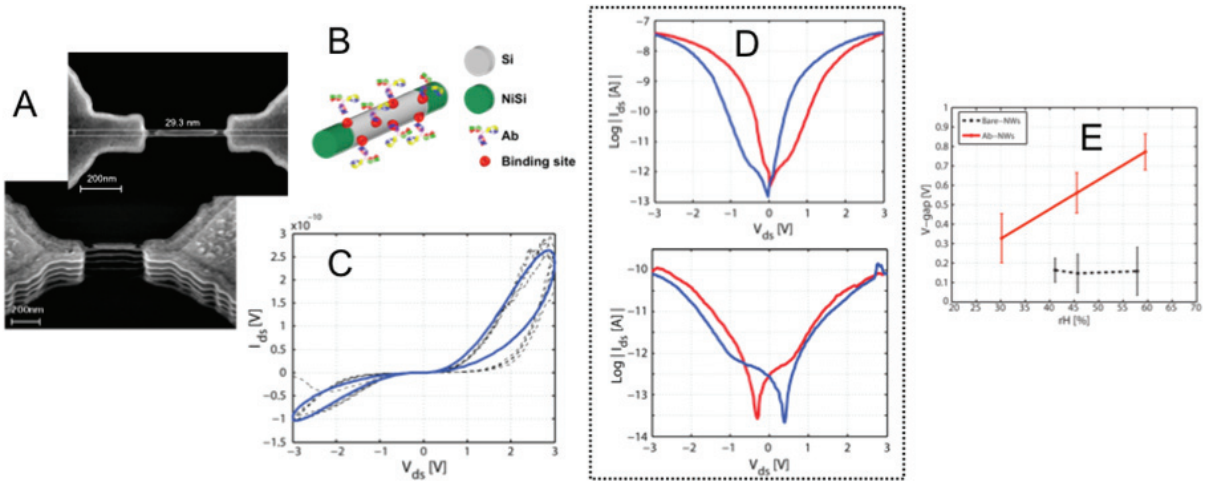

Figure 17 Memristor sensors from fabrication to measurements

Figure 17 shows A) SEM images of the fabricated memristive NWs; (B) schematic representation of the NW functionalization with antibodies (Ab) and antigen (Ag) uptake; (C) comparison between the simulated memristor theory (dashed curve) and the acquired characteristic from a fabricated wire (blue curve); (D) increasing voltage gap between forward and backward current minima after functionalization with biomolecules (lower image); (E) Mean voltage gap as function of the humidity calculated on 20 wires prior to (black line) and after (red line) functionalization. NW sensitivity to humidity if functionalized with biomolecules with respect to the constant and close to zero behavior of bare NWs.

2.3 Mobile Phone Software Interface

Smart-phone Interface:
The smart-phone is the tool the patient is going to use to access the sensor information on the implant. So it should be looked upon as the interface between the system and the user. At the same time it is the interface the software programmer needs to use to programme the NFC reader unit in the smart-phone to power up and communicate correctly with the implanted tag. Each of these interfaces sets a different requirement on the design as a whole, but one strict requirement is that the second interface should be seamless for the patient, and the whole mobile application should be patient friendly. What follows is a description of two related aspects that the mobile application should be able to satisfy while interfacing to the tag and to the patient.

Custom-made commands:
[62] defines 7 commands that can be exchanged between the NFC reader and the NFC tag, as it appears in Table 4.

Command	Hex	Comments
REQA	0x26	Request command, type A
WUPA	0x52	Wake-up, type A
RID	0x78	Read ID of the tag
RALL	0x00	Read all the bytes available in the memory
READ	0x01	Read a single byte from the memory
WRITE-E	0x53	Write with erase a single byte
WRITE-NE	0x1A	Write without erase a single byte

Table 4 Commands exchanged between the NFC reader and the NFC type 1 tag

The protocol defines 7 bits for the command and defines only the 7 commands above, leaving space for 120 combinations of bits not defined. At the same time, all the packets that follow the command are 8 bits wide, as shown in Table 5.

The NFC android development platform, [63], offers two types of interacting with the NFC reader hardware on the mobile phone:

- NFC basics: It gives a higher level of programming options for the programmer, where this method encapsulates some of the commands in Table 4, and the programmer can issue, for example, a read command that encapsulates a WUPA, RID, RALL and READ without the programmer needing to issue all these commands actively, and more importantly, it will build the frames for you, and sent it forward.

Command	Frame structure of the communication from the reader to the tag								
	7 bits	**8 bits each**							
REQA	0x26								
WUPA	0x52								
RID	0x78	0x00	0x00	0x00	0x00	0x00	0x00	CRC1	CRC2
RALL	0x00	0x00	0x00	UID0	UID1	UID2	UID3	CRC1	CRC2
READ	0x01	ADD	0x00	UID0	UID1	UID2	UID3	CRC1	CRC2
WRITE-E	0x53	ADD	DATA	UID0	UID1	UID2	UID3	CRC1	CRC2
WRITE-NE	0x1A	ADD	DATA	UID0	UID1	UID2	UID3	CRC1	CRC2

ADD: Stands for the address in the tag's memory.
DATA: The data sent from the reader to the tag, to be written at the specified address.
UID0…UID4: Unique Identification specific for each tag. It consists of 4 bytes.
CRC1, CRC2: Cyclic redundancy check over the previous 7 bytes. It consists of 16 bits.

Table 5 Frame structure of the commands sent from the NFC reader to NFC tag type 1

- Advanced NFC: Here Android grants the programmer access to the hardware, without any extra help (apart from calculating the CRC) in building up the frame structure. As the programmer is told by Android: "(you) have to manually read or write to the tag in raw bytes using your own protocol stack".

So, if the programmer has to write raw bytes to the tag in the case of advanced NFC, then it is possible to write any combination of bits in the command's 7 bits as long as the tag's hardware can decode it correctly. Only then can we think about the NFC commands as an instruction set sent to the tag, and the tag will be acting as a processor, decoding the instruction sent, and executing it directly. This opens the door for an important opportunity where the commands are no longer limited to a read and write to a memory position. It can take any form of command related to the specific characteristic of the sensor attached to the tag. In the case of many sensors attached, this will leads to different commands to different sensors.

Data outsourcing or forwarding:
This part deals with the sensed data gathered from the sensory tag and what to do with it afterwards. In a general case, the patient will have the current data presented on the smart-phone/watch, and the data will be saved on the mobile phone. The data can also be forwarded to a database at a hospital or clinic where the doctor responsible can access old and new data. How often the data should be forwarded and in which scenarios depends a lot on the patient status and the type of sensor and the sensed data. In some cases it is sufficient to send the sensed data once every 24 hours, and in other cases, where the patient is under supervision or the sensed result is beyond some boundaries (sugar level too high or too low, for example) it needs to be sent continually.
Another perspective to take into consideration is whether to process the data locally on the mobile phone before sending it forward, or just to send the raw data as it is without any processing. In this context, factors like power consumption of the mobile phone and latency can inform the decision on how to proceed with the data transmission. All these scenarios and decisions taken should be seamless for the patient. This requires an algorithm to run on the mobile phone to decide the most logical decision to take at any moment with the least interaction needed from the patient.

2.4 Privacy and Security

Privacy is one of the most important aspects in handling patient information. Patients would not like to have their health information get in the wrong hands. NFC acts a safe environment for acquiring data from the implantable sensor. This is due to the fact that NFC is revered as a "touching technology"; i.e. the two devices (the reader and the tag) are be in very close proximity for the communication to occur. Moreover, the reader needs to be aware of the existence of the tag that has a touch capability. According to Rukzio and colleagues [52][64], touching is seen as a natural activity because of what we do in our daily lives – touching objects to interact with them. Also,

among communication technologies – touching, pointing and scanning – touching was classified as very intuitive and was seen as the most secure and trustworthy approach, based on a survey carried out. In another experiment [64], where 8 users were asked what communication techniques they associate with the following features or attributes (Security, Intuitive, speed and least error prone), the answers were as follows:

- All users believe touching as the most secure technique. They prefer this technique if it interacts with some critical role in their lives.
- 4 users believe touching is intuitive, while 4 others believe pointing is intuitive.
- 5 users associate touching with speed of selection.
- All users believe touching is the least error prone technology.

Once the sensed data is available on the smart-phone, more security is required in different forms. The transfer of the data between the smart-phone and the server can be also secured, as well as data storage on the server. But how secure should the communication between the tag and the reader in this specific scenario be? Some tags come with an extra level of encryption which makes it harder for a "man in the middle" type of attack to be successful. This comes at the cost of more complicated and bigger hardware. This will also make it possible for authorized users only to access the content of the sensory tag. On the other hand, in a practical situation where the intruder would like to access the sensory tag, they would need to be very close to the patient and have the reader touching the exact place where the sensory tag is implanted without the patient noticing and reacting, which is quite unlikely. Even if the intruder succeeds, then the intruder will have access to just one reading, or one value of the sensed data. Though it is considered as a risk in the security analysis, the consequences of this risk are not vital, compared to an unauthorized access to the logs on the smart-phone or, more seriously, on the server.

Chapter 3

Research Summary

3.1 Paper I

This paper covers the part when the sensed data is available on the phone, and some kind of processing is required to run on the data – locally on the phone, or remotely on the server. It includes an adaptive outsourcing algorithm that transfers the sensed data (in this special case, we chose an image due to the size of the data, and the availability of algorithms to run on images of different levels of complexity) to the server. Once the data is on the server, one or many algorithms are run on the data, and the result is sent back to the mobile phone. The decision to send the data to the server is based on the following criteria: latency (defined as the sum of the execution time and the transaction time), power consumption as marked solely by the battery of the mobile phone, and finally the complexity of the problem. We ran different types of experiments in order to have strong foundations for the algorithm. These experiments can be categorized as running locally on the phone, and remotely on the server, while using wifi as a medium of communication in one case, and 3G in another. We also measure the signal strength for wifi and 3G whenever we transfer the data to the server.

Candidate's contribution:

Writing Abstract, Introduction, Measurements and results, Outsourcing decision making algorithm and editing Future work and Conclusion.

Results:

After finishing running the experiments in different environments, we arrived at the following:

- If the sensed data is big, and the algorithm run on the data is complex, outsourcing the job to the server can save up to 87% of the power consumption compared to locally executing it on the phone.
- If the sensed data is small, and the algorithm is trivial, outsourcing to the server using a 3G connection consumes most power. In such a case, executing locally is the option that saves most energy.
- In terms of latency, it is recommended to always outsource big data with complex algorithms using wifi. In such a scenario, the result will be available 65% faster compared to executing locally.
- Signal strength, especially in the case of 3G, can affect power consumption and latency incredibly.

This has led to designing an adaptive algorithm that runs in the background and has the following criteria, based on whether to execute locally or to outsource to the server: sensed data size, type of algorithm, signal strength, power level and state (charging or power-saving). Each execution is logged and used to better decide about the next execution.

3.2 Paper II

This paper studies the feasibility of having single poly non-volatile memory cells on the micro-implant. We chose single poly instead of the conventional double poly because of the cost and the compatibility with accessible 90nm CMOS technologies. We implemented 3 different cells, two of which are adopted from previous work done by other groups and not implemented in 90nm

technologies, and the last one is a novel structure. We are after cells that can be used in the NFC sensory tag type 1. NFC tag type 1 protocol defines latency between the command sent from the NFC reader and the reception of the response from the sensory tag. It can be summarized in Table 6.

Command	**Timing requirement**
READ, RALL*	~91us
WRITE-E**	~5.2ms
WRITE-NE ***	~2.6ms
*READ, RALL: read from one address vs reading the whole memory. ** WRITE-E: write to an address by erasing first the content. ***WRITE-NE: write to an address directly with no erase. In both case, the response contains a read of that address after the write command is executed to make sure it was successfully executed.	

Table 6 Timing requirement for delay noticed by the reader between command sent and responce received

These timing characteristics set a requirement on the read and write response of each tested cell. Read should be below 91us, a programme should be below 2.5ms, and finally the sum of erase, programme and read should be below 5.2 ms. In addition to latency, power consumption is also investigated since we are running on harvested energy from the reader.

Candidate's contribution:

Writing Abstract, Introduction, Related work, Cell structures and measurements, NFC tag 1 requirements, Results and Analysis, Conclusions.

Results:

We ran the testing on the 3 cells, and reached the following results:

- All cells meet the read operation requirement of below 91us.
- Cell I has the biggest footprint, while meeting the erase and programme requirements at lower voltages.
- Cell II has a smaller footprint compared to Cell II, but needs higher voltages to programme and erase to meet the timing requirements.
- Cell III lowers the voltages needed by Cell II by 2v, while meeting the timing requirements.
- There is an inverse relationship between the voltage amplitude applied and the duration of the pulse. With a longer pulse, a lower voltage is required to achieve erase or programme.
- All the cells needed less 10nA while erasing or programming. The main focus on power consumption then moves to the charge pump that needs to achieve the higher voltages.

During the measurements, we faced a problem with retention of all the 3 cells. All cells managed to hold the stored value for 5s-10s (varies if it is a 1 or a 0 stored). This corresponds to leakage currents of order of fAs. The thickness of the oxide of the transistors used with these cells can be a reason (earlier we implemented floating gate structures in 90nm but with another foundry, and there was no problem with the retention).

It is important to point out that the retention problem does not affect the analysis we have gone through or the results we reached to for the three cells.

3.3 Paper III

This research paper covers the analogue to digital conversion of the parameters that need to be sensed. In other words, it is a front end readout circuit for a sensor whose output needs to be digitized. This research was carried out during my research visit to EPFL, where the team there has been developing Nano Wire (NW) memristive sensors used for early detection of breast cancer, to measure humidity and PH levels, among other things. The sensing method for these memristive NWs work as follows: The voltage is swept across the terminals of the NW while sensing the current going through the NW. It is swept in both directions. We log the voltage value at every moment the current switches direction (zero crossing point). The difference between the two logged voltages is what we call the "voltage gap". Voltage gaps are directly proportional to the concentration of the material we are sensing.

The previous way of running the tests on the NW was done using a probe station, where the current is measured for every step increase/decrease in the voltage. This led to a case where the measurement of one NW lasted for hours. The new approach that this research paper proposes and designs cuts the testing time down to minutes and makes it tuneable, plus it can test multiple NWs at the same time. The last advantage can enable us to extract statistical results from an array of NWs instead of individual results from each NW. The implemented circuit is made up of a voltage ramp-up and -down controller, a current zero crossing sensing block and a time-to-digital converter to extract the voltage gap. It is also contains a fault detector for deformed NWs, as the fabrication process is very delicate.

Candidate's contribution:

Writing Abstract, Introduction, circuit requirements, circuit description, simulations and results, conclusion.

Results:

The circuit has been implemented in 0.35um CMOS technology to control an array of 4 NWs. The simulations were carried on where the NWs were replaced by a voltage-current lookup table extracted from the probe station in real-case scenarios. The following simulation results were achieved:

- The ramp-up and ramp-down voltage generator is tuneable in terms of the speed of ramping, and the voltage bounds it can bounce from and back to.
- The voltage ramp has achieved a linear increase and decrease with a deviation of 1.6% from the linear voltage expected.
- The duty cycle between ramp up and ramp down lies at 50%.
- A 600mv voltage gap has been detected with a 5mv error.

Post paper lab measurements:

After the paper was published, we got the ASIC back and we set up for measurements in the lab. The voltage ramp generator was tested and characterized. Two major characteristics were investigated: Does it ramp up and ramp down for the same time duration? During ramp up and ramp down, how linear is the voltage across time? The ramp duration is controlled by a bias voltage, as shown in Figure 18 where the period can be changed from 39 sec to 200 sec and more by increasing the bias voltage. The duty cycle, on the other hand, is not influenced that much and most of the time is around 49%–50%. Figure 19 shows how linear the voltage ramp signal is when we run the experiment with the bias voltage set to 3.6v. The real ramp is the measured voltage ramp on chip. Samples are taken every 10ms. The voltage varies between 100mv and 4.85v. The linear ramp represents how the measured voltage ramp should look if it is linear. Finally we plot the absolute

difference between both, to show how far we are from linearity. In the charging phase, we are off by maximum 40mv, but in the discharging phase, we approach 150mv offset.
To be able to use this ramp generator, we need definitely to calibrate the readings we get when a zero crossing is met, and then a post processing is done to get a more accurate value.

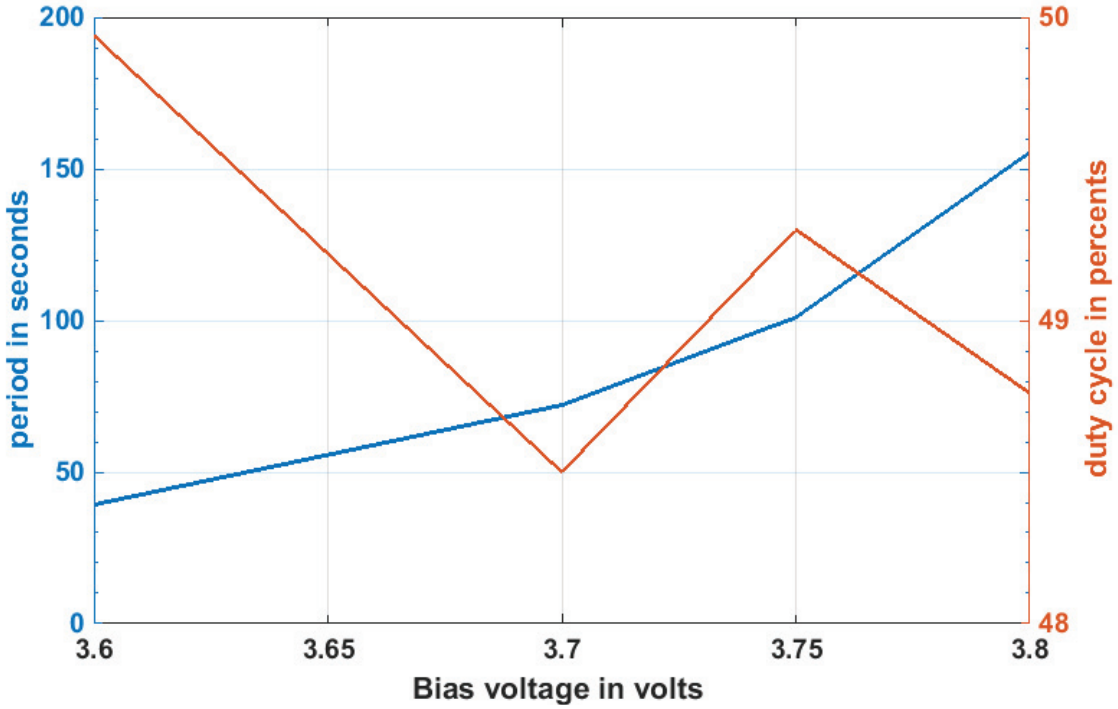

Figure 18 The voltage ramp signal's characterisctis as affeccted by bias voltage.

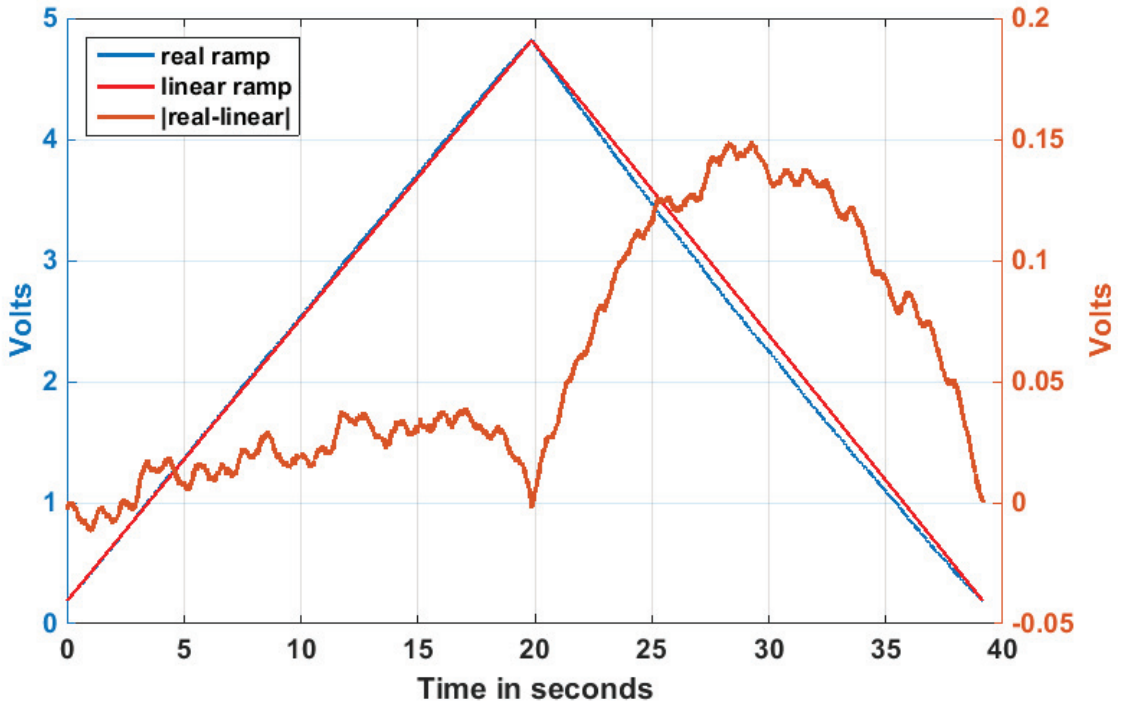

Figure 19 Voltage ramp is charging up and discharging down to complete a cycle of 39.27 seconds.

3.4 Paper IV

This paper deals with the application that should run on the smart-phone to communicate with the sensory tag. In looking to decide on which tag type we should build, we were not able to find published data about the performance and energy efficiency of different NFC tags. What we needed was a benchmarking routine to be able to decide which tags meet the requirements we set. We used the following commercially available tags in testing to cover the main five tag groups:

Topaz512: Type 1 from Broadcom, with 512B memory and 42mm in diameter [65].
NTAG203: Type 2 from NXP, with 144B memory and of size 80x50mm [66].
RC-S965 FeliCa Lite: Type 3 from Sony Corp, with 224B memory and of size 43x43mm [67].
Mifare DESFire: Type 4 from NXP, with 2kB memory and of size 80x50mm [68].
MF1 S50: Mifare Classic from NXP, with 1kB memory and of size 80x50mm [69].

The criteria of buying these tags were about having blank tags without extra application functionalities and they should be widely available. We were after smaller sizes when available and smaller memory in each category.

We defined the following benchmarking objects: Read and Write communication throughput, RALL communication throughput (Reading the whole memory), Read and Write energy efficiency (how much the smart-phone's battery drops for every read and write) and, finally, Powering up energy efficiency (when the smart-phone is powering up the sensory tag without communicating with it). Battery lifetime is, for smart-phone users, a very important property. Since the development of battery technology cannot keep track with the development of increasingly energy-hungry applications and increasingly powerful CPUs, GPUs and networks, it is important to make NFC applications more energy efficient.

We carried out two types of experiments: one with a saline solution between the tag and the smart-phone and one without. We also ran the experiments at different distances between the tag and the smart-phone. This has been done for all the five different tag structures available at that time. This toolset is designed in such a way that it is extensible with respect to supported tags and supported benchmarking routines. The architecture of the toolset comprises a basic library that provides a single interface for communication with a range of NFC tags, one app for benchmarking, and one app to test proprietary communications protocols.

In addition we extended the last mentioned app to communicate with tag type 1 using raw bytes and custom-made commands. This has been tested successfully in Paper VI, as will be shown later.

Candidate's contribution:

Copy editing the Abstract, writing related work and NFC Benchmarker app, Experiments design and parts of the results, parts of towards energy efficient NFC applications, and Conclusions.

Results:

- Read and write throughput is mainly influenced by the tag type, while displacement and embedding in saline solution have only a marginal impact.
- Energy efficiency for write and read varies strongly between the tags when measured in terms of energy consumption per byte, while the energy consumption per second is rather similar for the five tags.
- This insight leads us to the conclusion that increasing throughput could lead to increasing energy efficiency of NFC applications.

- We noticed that the energy consumption, while powering up the tag, is higher compared to when the smart-phone is reading or writing to the tag. This is 30% higher than writing energy consumption.

3.5 Papers V and VI

These two papers deal with the design, implementation, verification and simulation, and finally experimental results from the fabricated ASIC of an implantable NFC sensory tag with a sensor front end. The design has divided into three main blocks: the sensor front end, which may contain an ADC and interfaces to the sensor directly; the NFC physical layer module; and finally the NFC tag control module. In these two papers, the first block is implemented on a separate ASIC (the ASIC mentioned in Paper III), the second block is implemented on another ASIC, and finally the NFC tag control module holding the core of the NFC protocol and the interface to the first block is implemented on an FPGA as a first step and as a proof of concept. The aim is to move all the three modules into one ASIC (already developed and fabricated, and is under testing).

Paper V presents the early design of the 2nd and 3rd module, and the simulation results available before sending the ASIC to fabrication. Paper VI presents the full design of these two modules; extensive testing is carried on in the Lab with the help of the mobile app from Paper IV. The ASIC from Paper III is connected to the FPGA, and the mobile phone is powering up and communicating with the NFC physical layer module ASIC. So, these two papers present the first complete electronic system for implantable sensors using NFC technology.

The NFC physical layer module contains the power harvester, power regulators, demodulator, modulator, clock extractor and power-on reset sub-blocks. This module is responsible for supplying energy for itself and for the other two modules. It also receives the signals from the mobile, demodulates it and forwards it to the NFC tag-control module.

The NFC tag-control module implements the NFC-A protocol, without the implementation of a non-volatile memory. It also interfaces to the sensor front end ASIC to transfer control and data in between. Without this interface, the smart-phone will not gain access to the sensor, controlling it and gathering the sensed data. With the help of this interface, we are able to connect more than one sensor running simultaneously with the same smart-phone, without any collision occurring.

Candidate's contribution:

Paper V: Writing Abstract, Introduction, NFC background, Circuit design, Implementation, Simulations and results, conclusions and future work.

Paper VI: Writing Abstract, Introduction, NFC background, Circuit design, Implementation, Results, Conclusion and future work.

Results:

We implemented the NFC physical layer module in TSMC 90nm CMOS technology. It occupies $0.115mm^2$. It can harvest up to 400uW. It consumes 295uW by itself for power regulators, demodulator, load modulator, and clock extractor. A previously-published ADC and sensor front end [70], which will be integrated in the next ASIC, consumes 5.5uW. We are currently on the edge of meeting the power budget, while we have hopes of a more power efficient ASIC replacement of the FPGA.

We connected the ASIC from Paper III to the FPGA, and we were able to control the readout circuit from the smart-phone and at the same time read out sensed data of 88 bits long. We also tested the custom-made commands available in the mobile app developed in Paper IV. With the help of the

FPGA, we were able to decode any type of custom-made commands sent from the mobile phone, and carry out a corresponding dummy action.

Post update:

Early results appeared from the testing of the one chip solution containing the sensor front end, which contains an ADC and interfaces to the sensor directly; the NFC physical layer module; and finally the NFC tag control module. The digital part that was implemented in these two papers on an FPGA was tested and characterized to consume around 47uW@1V. Figure 20 shows the command REQA sent from the phone to the chip. With the current measurements, we are left with 53uA to power up other sensors.

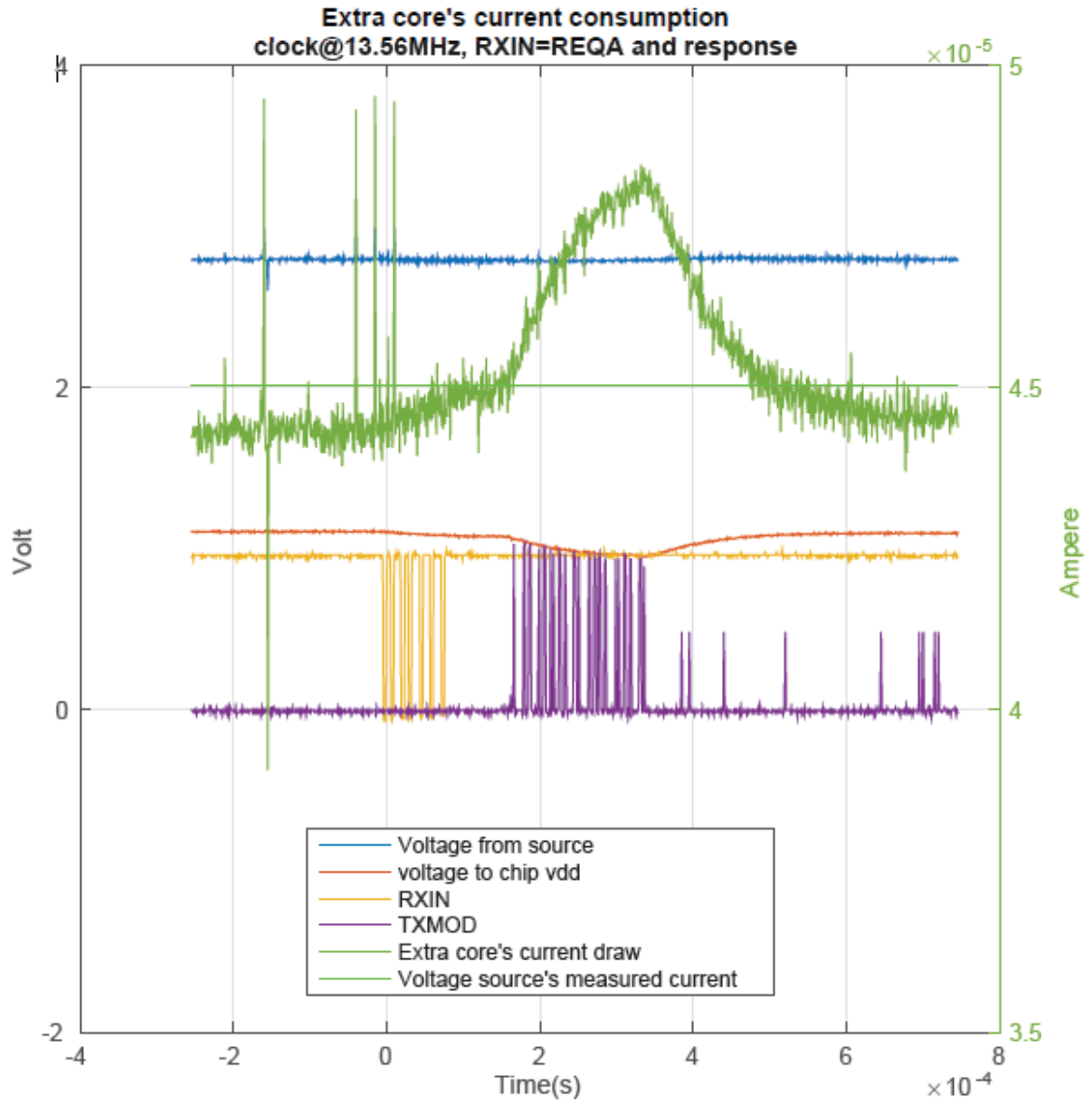

Figure 20 One chip solution replacing 2 ASICs and an FPGA

Chapter 4

Conclusion and future work

4.1 Summary

In this thesis we have introduced a complete electronic system for NFC implantable sensors. The system contains an NFC sensory tag made of a sensor front end and NFC tag control module harvesting power from the magnetic field generated by the reader. The reader in this case can be a smart-phone or a smart-watch. The system also contains a mobile application running on the smart-phone to control the sensory tag, thus the sensor, and to power up the electronics simultaneously. We have also implemented an algorithm to forward the data from the smart-phone to a server based on different criteria. Once the data is on the server, different algorithms can run on the current and previously stored data to extract relevant information, with the possibility that the results can be send back with the smart-phone.

4.2 Discussion

Designing a complete system compared to designing individual sub-blocks presents a different set of challenges and opportunities for the designer. One of these challenges is to design the individual blocks to meet requirements that are set on a local level (ADC's number of bits) while keeping in mind both the overall performance of the whole system and the tag's power consumption. The number of bits of an ADC, as we mentioned in section 2.1 Sensor ADC, is defined by the object we are monitoring, while the tag's power consumption will be dictated by the power budget of the whole system – the power we managed to harvest. On the other hand, new opportunities arise when following a top-down approach in designing the complete system, like cross layer optimization. If each sub-block is designed by itself without taking into consideration how it can be used in the whole system, we might end up with wasted resources. This can also be noticed when we answer the question of how smart can and should these sensors get? By smart, we refer to a system that has a memory, can process data, and can finally communicate. If we think about our system as a whole, it can become extremely smart, especially with the introduction of a smart-phone and a server. The phone is able to communicate, store and process data. If more memory space is needed or extra data processing is required, the server is available. By going in this direction, the electronics surrounding the sensor (NFC sensory tag) stay simple and fulfil the basic requirements of the sensing part (ADC) and the communication part (NFC) while being power efficient. A good example here is the NVM needed in NFC tag structure. Since the data can be stored on the phone, there is no need to store it on the tag and on the phone again. In this sense, the complete sensory system is a smart system and, if needed, can get smarter by adding extra features on the software running on the smart-phone and the server without adding more complexity to the design of the NFC sensory tag.

Extensive testing has been carried out to characterize the different implemented ASICs and sub-blocks contained inside, as well as the system as a whole unit. Results showed that, in case of a sensory system that runs only on the presence of the reader, there is no benefit in having a NVM to store sensed results on the implant, since the sensed data can be exchanged directly with the smart-phone and stored there, where there is unlimited space to use for a very low cost. Skipping the NVM in the sensory tag leads to two advantages: lower power consumption related to the absence of the high voltages needed while writing to the NVM, and smaller footprint of the sensory tag.

Moreover, the sensory tag can host multiple sensors of different characteristics running simultaneously. The size of the address word defined in the NFC protocol (8 bits in NFC-A protocol) and how many bytes each sensor is mapped to in the virtual memory are the major limitations on how many sensors can be connected to the sensory tag. Of course, before that comes the major limitation, which is the harvested power. To get around the harvested power limitation, the sensors

can run sequentially or on demand instead of running simultaneously. When the sensor is not running, the corresponding electronic unit can be power gated to save more power than can be used by the running sensor. With the current implementation, the harvested power is around 400uW, 295uW used by the NFC physical layer module and around 47uW used by the digital circuit running on a newer ASIC. A sensor front end designed earlier by our team consumes around 5.5uW. So with the current implementation we are able to power up and control multiple sensors.

4.3 Conclusion

After finishing designing and testing the different pieces of the current system, we conclude that we should have done a more systematic cross-layer optimization while still defining the requirements of system as a whole. In the case of tags with a power supply and don't depend on the reader to power them up, these sensory tags are able to run on their own even when the reader is not in proximity. In such a scenario, the system needs to consider having local storage (a NVM) on the sensory tag, so that the sensed values are saved and not lost until the next time the reader is nearby and the data can be exchanged with the reader. This will add an extra requirement as mentioned before on the hardware design of the sensory tag, but at the same time it will give more flexibility on the patient's side (e.g. continuous monitoring of some physiological parameters while the patient is asleep). For example, to ensure a storage for 8 hours of glucose level monitoring, assuming 8 bits per value, and the measurements are taken every 5 minutes, we end up with 8bits x 12readings/hr x 8hrs= 96 bytes. If we increase the monitoring period to 12 hrs, and we represent the results on 10 bits, then we need a NVM of 180 bytes. In both cases, tag-type 1 is a good solution. A FeRAM or a ReRAM will be good candidates to implement since we can make use of their advantages (working on low voltages and consuming low currents) while their major disadvantage (lower density) is not a concern since we have a very low number of bytes to use.

The first prototype we developed will not be suited for a micro-implant and cannot be as thoroughly power-optimized as a single ASIC SoC. In particular the FPGA, obviously, has more unused resources that can be removed for the SoC solution. Since the antenna size of the implant plays a major role in the amount of energy harvested by the ASIC, more focus will be directed towards reducing the power consumption of the NFC physical layer module. The system will profit more by reducing the tag power budget than by improving the efficiency of the inductive link. Different solutions can be investigated here, where the digital parts can be implemented in the subthreshold voltage region, for example, and, as another example, the power regulators can be redesigned so that we trade the area for the power consumption.

4.4 Future work

The next step that has already started is to implement a one ASIC solution in which we incorporate many of the different parts we designed separately in this thesis. More specifically one ASIC containing the previously-mentioned capacitive sensor front end, the NFC physical layer module, and the NFC higher layer protocol module developed before on an FPGA.

On the smart-phone front, the patient perspective is required as a major input in designing a user-friendly app running on the phone. This same input will also be used to shape the design of a smart-watch app. The smart-watch with its continuous presence over the implant will offer a means of continuous monitoring of the physiological parameters the NFC sensory tag is tracking.

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