A μ-Controller-Based System for Interfacing Selectorless RRAM Crossbar Arrays

Radu Berdan, *Student Member, IEEE*, Alexander Serb, *Member, IEEE*, Ali Khiat, *Member, IEEE*, Anna Regoutz, *Member, IEEE*, Christos Papavassiliou, *Senior Member, IEEE*, and Themis Prodromakis, *Senior Member, IEEE*

***Abstract*— Selectorless crossbar arrays of resistive random-access memory (RRAM), also known as memristors, conduct large sneak currents during operation, which can significantly corrupt the accuracy of cross-point analog resistance (M_t) measurements. In order to mitigate this issue, we have designed, built, and tested a memristor characterization and testing (mCAT) instrument that forces redistribution of sneak currents within the crossbar array, dramatically increasing M_t measurement accuracy. We calibrated the mCAT using a custom-made 32 × 32 discrete resistive crossbar array, and subsequently demonstrated its functionality on solid-state TiO_{2-x} RRAM arrays, on wafer and packaged, of the same size. Our platform can measure standalone M_t in the range of 1 kΩ to 1 MΩ with <1% error. For our custom resistive crossbar, 90% of devices of the same resistance range were measured with <10% error. The platform's limitations have been quantified using large-scale nonideal crossbar simulations.**

***Index Terms*— Crossbars, memristors, resistive random-access memory (RRAM), sneak paths.**

I. Introduction

MEMORY storage elements are the key components of many electronic systems ranging from data center servers to consumer electronics, and a great interest has been given to the development of reliable, low-power, massively scalable, information-compact memory cells. With current NAND-type flash memory quickly approaching its scalability limit, a shift toward ionic-based memories is ascertained with resistive random-access memory (RRAM) being the main candidate for a post-NAND market. RRAM cells, also known as memristors [1]–[3], have already been shown to excel in storage element size [4], write power [5], and information compactness, with the ability to store multiple bits per memory element [6], [7].

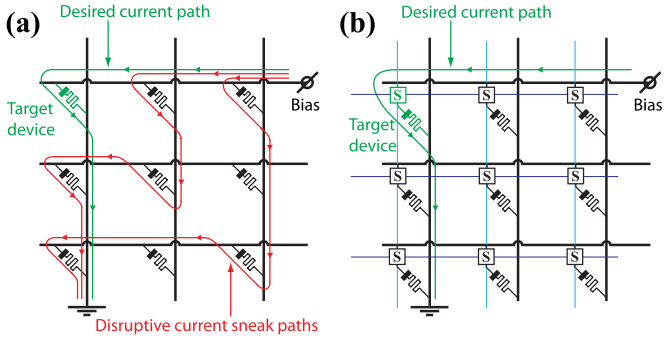

Fig. 1. (a) Sneak path/sneak current problem in crossbar arrays. Application of a bias reading voltage on active word and bitlines causes disruptive currents to flow in neighboring cells. (b) Low-density solution for sneak path limiting involving transistor-based selectors S.

Many of the benefits of RRAM technologies result from the small size of the storage nodes it utilizes, achieving densities of down to $4F^2$ [feature size (F)] per element for planar arrays and even below for 3-D arrays [8]. Achieving $4F^2$ density involves arranging the RRAM elements in a crossbar configuration. These can be either RRAM only [9] or postprocessed on top of a lower density CMOS in a CMOL configuration [10]–[12]. In both the cases, however, crossbar arrays suffer from the issue of sneak paths [13], whereby applying a voltage across the electrodes of a target device leads to the inadvertent application of voltage across all other elements in the array. This gives rise to sneak path currents that hinder the accurate reading of the active device's resistive state [Fig. 1(a)].

Sneak currents can be minimized by the implementation of nonlinear selector elements embedded into the storage node [14] (1D1R structure) or the utilization of CMOS transistor-based selectors [15], [16] [Fig. 1(b)—1T1R structure]. A special class of selector-based crossbar arrays is represented by complementary switches, where two RRAM elements are connected antiserially to form one cell which in turn exhibit a selector effect [13], [17]. Selector-based sneak current mitigation techniques suffer from their own shortcomings, such as loss of scalability (1T1R designs) and issues with reversibility of write process and manufacturing complications (1D1R designs). Complementary switches usually exhibit a destructive read process that requires an extra write-back step, which in turn severely limits reading throughput [17].

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R. Berdan and C. Papavassiliou are with the Circuits and Systems Group, Department of Electrical and Electronic Engineering, Imperial College London, London SW7 2AZ, U.K. (e-mail: radu.berdan11@imperial.ac.uk; c.papavas@imperial.ac.uk).

A. Serb, A. Khiat, and T. Prodromakis are with the Nano Group, Department of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, U.K. (e-mail: a.serb@soton.ac.uk; a.khiat@soton.ac.uk; t.prodromakis@soton.ac.uk).

A. Regoutz was with the Nano Group, Department of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, U.K. She is now with the Department of Material Science, Imperial College London, London SW7 2AZ, U.K. (e-mail: a.regoutz@imperial.ac.uk).

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Techniques for mitigating sneak paths in selectorless arrays have also been developed. One approach centers on multiport readout and subsequent mathematical cancellation of said sneak path currents [18]. Another, more conventional approach employs various schemes of active biasing of both active (leading to the target device) and inactive word and bitlines. Several such schemes have been developed in order to cater for read and write operations in large varieties of crossbar arrays with storage nodes showing highly diverse electrical behaviors. Some of the most popular such schemes are described in [20, Sec. 2.6] and [21].

In this paper, we focus our efforts toward this issue and present a multiport technique for reading accurate analog cross-point resistance values from devices within a planar, selectorless crossbar array—a markedly stricter criterion than achieving a good digital read margin. We implement the nonintrusive reading and writing techniques on a desktop PCB that facilitates quick acquisition of data of RRAM cells in a 32×32 crossbar array configuration via a user-friendly graphical user interface (GUI) on a local PC. In particular, in Section II, we introduce the theoretical background of our approach. Section III describes the practical implementation of our memristor characterization and testing (mCAT) system. The experimental results from a reference resistive crossbar array and an equal size solid-state RRAM array are presented in Section IV. Finally, Section V considers the benefits and limitations of the current system, as well as offering insights into the scaling up performance of the mCAT and direction of future efforts.

II. Theoretical Analysis

A. Read Operation

An illustration of the sneak path current issue is represented in Fig. 1. The selection of voltages applied to the inactive word and bitlines during operation (for multiport readout) and their relation to the voltages on the active word and bitlines affects the distribution of sneak currents within the array [Fig. 2(a)]. Furthermore, if all inactive word and bitlines are shorted together, the entire array is reduced to a three-node/three-lumped-component circuit, as shown in Fig. 2(b). External circuits can access any of the three nodes for either voltage or current sourcing/measurement, but any other currents flowing within the crossbar remain inaccessible.

Measuring the resistive state (memristance) of a target device M_t (read operation) requires accessing both the voltage drop across it [i.e., $V_{\text{bias}} - \text{GND}$ in Fig. 2(a)] and the current flowing through it during biasing. As shown in Fig. 2(b), the current through M_t can be obtained if M_w is bootstrapped by appropriately biasing node V_{inactive}. This is not the only way to gain access to the M_t current. For example, if the grounded node is connected instead to, e.g., a transimpedance amplifier virtual ground and M_b is bootstrapped, access to the current through M_t is gained.

In practice, such readout scheme may be implemented by a circuit, as shown in Fig. 2(c). V_{bias} and V_{read} are directly accessible by voltage measurement, and the current through M_t is indirectly computed via R_{sense}, thus allowing calculation

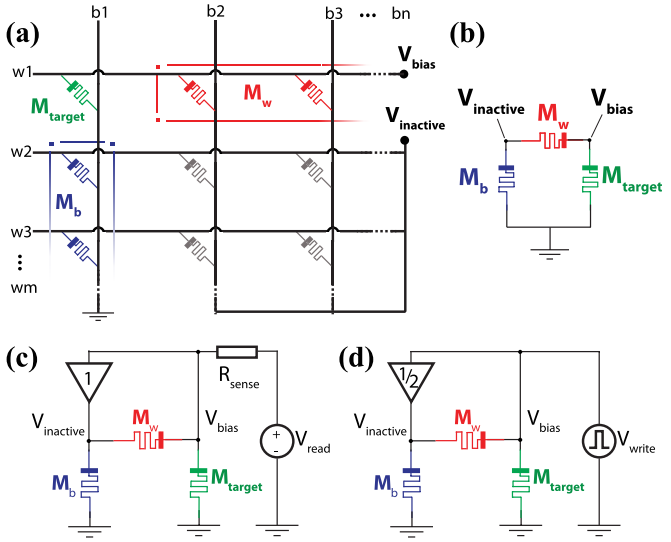

Fig. 2. (a) Illustration of a $m \times n$ (of which the first three wordlines and bitlines are shown) crossbar array with $M_{\text{target}} = M_t$—DUT located at the cross between active wordline (w1) and active bitline (b1), M_w—parallel combination of all inactive devices on the active wordline, M_b—parallel combination of all inactive devices on the active bitline. (b) Reduced three-node/three-lumped-component circuit. (c) Conceptual circuit for reading analog resistance values via (b). (d) Conceptual circuit for a write operation performed on same target device.

of the analog resistance value of M_t by solving the voltage divider network.

A crucial characteristic of the proposed readout scheme is the fact that V_{inactive} has to be derived from V_{bias} (e.g., by buffering) so as to allow separation between the currents flowing through M_t and the rest of the array and is accuracy-critical. The criticality occurs from the worst case scenario whereby the target is in a very high resistive state, and the lumped component M_w consists entirely of memory cells in very low resistive states, thereby forming a very low impedance path between V_{bias} and V_{inactive}. Even small offsets in the generation of V_{inactive} from V_{bias} can lead to significant amounts of current being diverted through M_w, hence corrupting the estimated target state.

B. Write Operation

RRAM cells are usually characterized by a voltage switching threshold (V_{thr}) under which no applied potential can disturb its resistive state [21]. We utilize this feature in our write scheme by applying half of the active device's write voltage (V_{write}) to all inactive lines, as shown in Fig. 2(d). Provided that $V_{\text{write}} > V_{\text{thr}}$ and $V_{\text{write}}/2 < V_{\text{thr}}$ then the risk of accidentally programming adjacent devices when writing only on M_t is minimized. We note that the write operation is not accuracy-critical, i.e., small variations in V_{inactive} do not significantly perturb the write operation.

III. System Implementation

To demonstrate these ideas and to facilitate practical RRAM characterization, a full system has been implemented on PCB. A photograph of the setup is shown in Fig. 3(a) with its corresponding simplified schematic

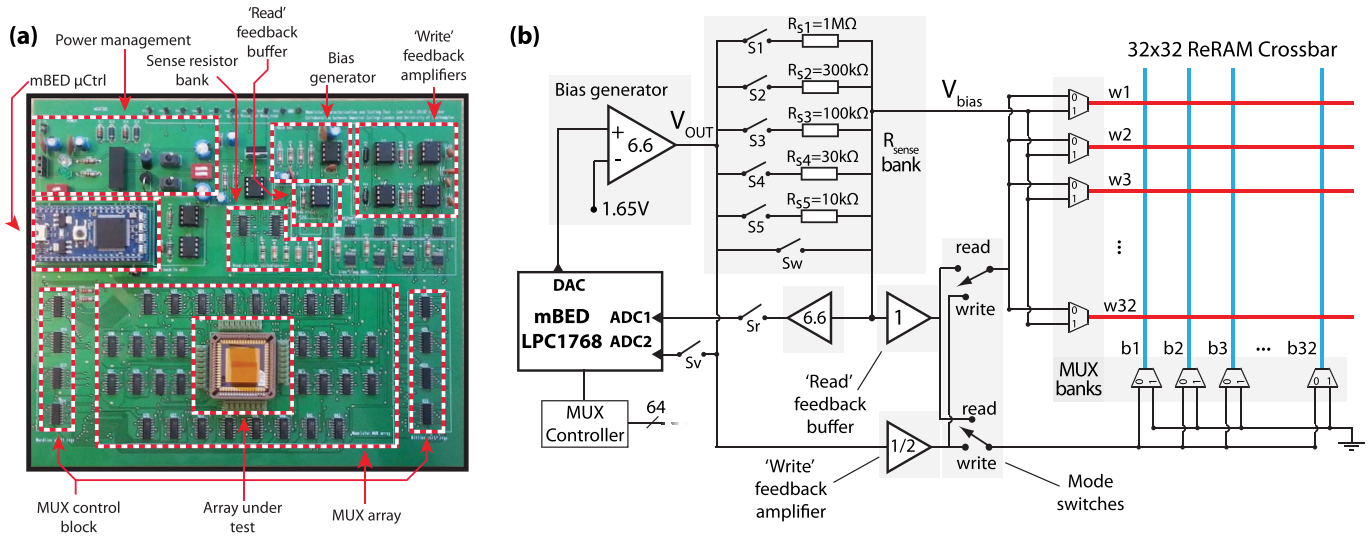

Fig. 3. (a) Photograph of the mCAT system on PCB. The array under test block contains a standard DIP PLCC68 holder in which a complementary package containing bonded 32 × 32 array cells can be introduced. The holder is surrounded by four 2 × 8 sockets used to interface to a probe card for on-wafer measurements. (b) Simplified mCAT schematic.

in Fig. 3(b). The key components of this platform are as follows.

1) An mBED LPC1768 microcontroller which features the following:
   a) serial communication with a local PC;
   b) 5-bit × 12-bit Analog to Digital Converters (ADCs) and one 10-bit Digital to Analog Converter (DAC) on board;
   c) twenty digital 10-ns transition i/o pins.
2) A bias generator subtractor op-amp that scales the mBED DAC from 0 −> 3.3 to ±9.2 V at $V_{\rm OUT}$.
3) A sense resistor bank allowing connection of the bias generator to the crossbar array via different sense resistors or a resistorless, bypass path.
4) A feedback buffer copying the voltage on the active wordline ($V_{\rm bias}$ to $V_{\rm inactive}$ during read operation).
5) A feedback amplifier block supplying $V_{\rm bias}/2$ on inactive wordlines and bitlines during write.
6) Wordline and bitline access multiplexer banks.
7) A variety of housekeeping systems (power management and multiplexer controllers).

A. Read Operation

Assuming that all switches are open in idle mode, and $V_{\rm OUT} = 0$ V, the operation proceeds as follows. First, the target device is selected by connecting the corresponding (active) wordline to the $V_{\rm bias}$ node and the respective bitline to GND. The inactive word and bitlines are shorted together and connected to the output of the read feedback buffer. Then, the mBED sets its DAC to facilitate $V_{\rm OUT} = 0.5$ V (default value but programmable) and subsequently switches the 1 MΩ sense resistor in (closes $S1$). This provides a dc bias to the bootstrapping feedback buffer input, which henceforth constantly performs its bootstrapping function on the inactive crossbar lines. The mBED then takes a reading of $V_{\rm OUT} = V_{\rm read}$ via ADC1 by closing switch Sr, and a reading of $V_{\rm bias}$ via ADC2 by closing the switch Sv. Typically, 50 measurements taken at full reading rate are averaged as a compromise between speed and noise rejection. The estimates of $V_{\rm bias}$ and $V_{\rm read}$ along with the value of the first sense resistor used yield enough information for a first calculation of the target memristance M_{S1}. Time delays are introduced to ensure that voltage readings are performed after all nodes have settled.

Next, the 1 MΩ is switched out, the 300-kΩ resistor is switched in ($S1$ open and $S2$ close), and the previous procedure of measuring $V_{\rm bias}$ and $V_{\rm read}$ is repeated yielding a new candidate value of memristance M_{S2}. This sequence is repeated for all sense resistors producing five different values $M_{S1->S5}$ for the resistance of the target device, each one corresponding to its respective sense resistor utilized $R_{S1->S5}$. These are recorded by the mBED.

Finally, from all calculated $M_{S1->S5}$, a single value M_{Si} is chosen in software as the final read value of memristance, where i is the index at which $|(M_{Si} - R_{Si}/R_{Si})|$ is minimized. This ensures that a reading is taken at the point where $\partial V_{\rm bias}/\partial M_t$ is maximized allowing for a minimal δM change that will produce a 1 LSB shift in voltage at the input of ADC1. To prove this, we note that from Fig. 2(c)

$$V_{\rm bias} = \frac{V_{\rm read} \cdot M_{\rm target}}{M_{\rm target} + R_{\rm sense}} \tag{1}$$

$$\frac{\partial V_{\rm bias}}{\partial M_{\rm target}} = \frac{V_{\rm read} \cdot R_{\rm sense}}{(M_{\rm target} + R_{\rm sense})^2} \tag{2}$$

$$\frac{\partial^2 V_{\rm bias}}{\partial M_{\rm target} \partial R_{\rm sense}} = \frac{V_{\rm read}(M_{\rm target} - R_{\rm sense})}{(M_{\rm target} + R_{\rm sense})^3} \tag{3}$$

where (2) expresses the sensitivity of our measurement node voltage $V_{\rm bias}$ to the differences in the value of $M_{\rm target}$ (measurement sensitivity) and (3) expresses the sensitivity of the measurement sensitivity on the value of the sensing resistor used. Hence, the maximum sensitivity for given $M_{\rm target}$ and $V_{\rm read}$ is reached when $M_{\rm target} = R_{\rm sense}$.

Under our current configuration, the read time for one cell is ≃20 ms, most of which is spent on the serial transfer of the corresponding float from the mCAT to the local PC.

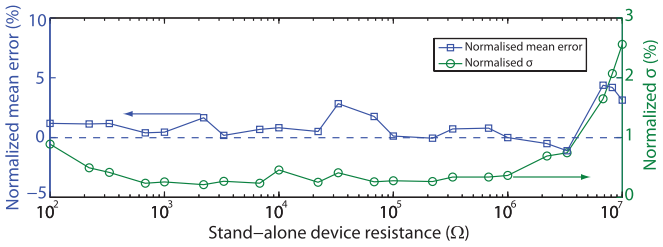

Fig. 4. Single device measurements showing low mean error and low variability between identical measurements (80 times) for a resistance dynamic range in between 100 Ω and 10 MΩ.

B. Write Operation

With initially all switches open, the write operation proceeds as follows: 1) the target device is selected and 2) the output voltage $V_{\text{OUT}} = V_{\text{write}}$ is set to the desired value. Mode switches are set to write. Subsequently, the bypass switch (S_w) is flash closed for the desired pulsewidth duration. While the active device is being subjected to the V_{write} voltage, all the inactive devices are fed $V_{\text{write}}/2$ via the bootstrap amplifier. Instead of using one feedback amplifier, the physical implementation of our system employs a bank of two pairs of amplifiers (one for wordline and one for bitlines) that facilitates the use of different gain settings for word and bitlines for testing purposes.

IV. Experimental Results

The mCAT is capable of self-calibration, which ensures that the effects of any hardware drifts and offsets are minimized in the C layer. Initially, the reading accuracy was assessed as a sanity check by measuring single discrete resistors, spanning five decades, connected across arbitrary inputs, and comparing the results with a high-end multimeter. Fig. 4 shows minimal mean read errors and excellent precision for standalone device measurement, without the intrusive effects of sneak paths.

A 32 × 32 resistor crossbar array with Surface Mount Devices (SMD) resistors was manufactured [Fig. 5(a)] in order to measure the accuracy of the read operation. A limited range of resistor was utilized (1 k, 5.6 k, 10 k, 56 k, 100 k, 560 k, and 1 MΩ), color mapped, and displayed in Fig. 5(b). The configuration was chosen such as to provide high stress conditions (high resistance elements sharing word or bitlines with many low resistance elements) that are more likely to disrupt the correct reading of the target resistor and such test the limitations of our system. Results of the full crossbar reading are shown in Fig. 5(c) and (d). The mCAT can thus measure 90% of the resistors on our standard testing crossbar with <10% reading error. It is clear from Fig. 5(d) that high resistance has larger reading errors than low resistance devices. This is due to the influence of M_w and the voltage offset of the read feedback buffer (V_{os}) used to isolate V_{inactive} from V_{bias}, as shown in Fig. 2(c). Other sources of error in the system will be caused by a complex combination of effects from V_{os}, M_w, M_b, R_{sense}, and the nonzero resistance of analog switches employed, bit and wordlines.

Several 32 × 32 TiO_{2-x} [$x = 0.06$ as measured by X-ray photoemission spectroscopy] solid-state RRAM crossbars were further measured by this setup. RRAM devices were fabricated as follows. The 200-nm SiO_2 was thermally

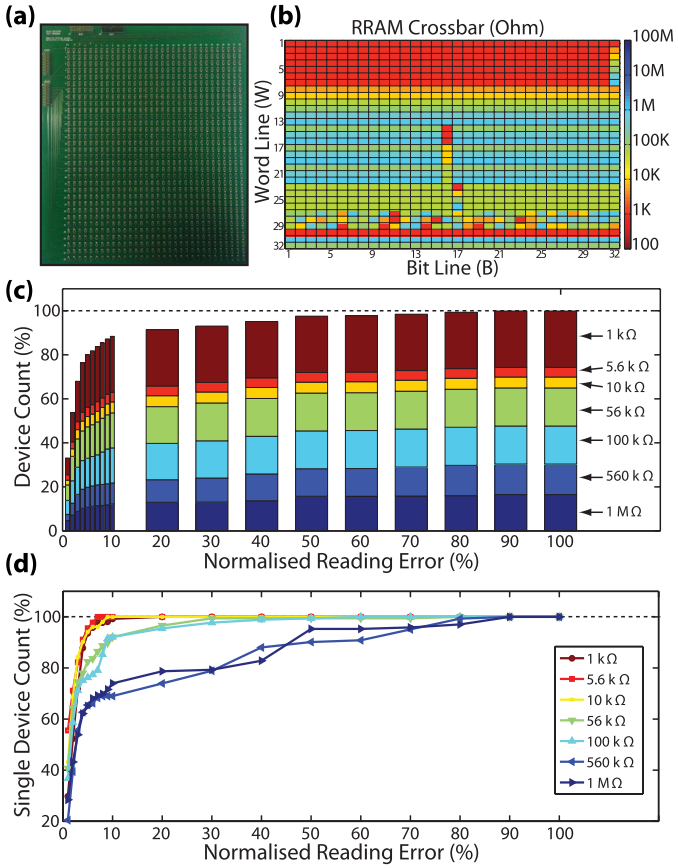

Fig. 5. (a) Manufactured 32 × 32 crossbar array of SMD resistors. (b) Real resistance of each wordline and bitline location on the crossbar shown in (a). (c) Normalized reading errors $|(R_{\text{measured}} - R_{\text{real}}/R_{\text{real}})|$ (%) of all resistors in the crossbar shown in (a). Each bin shows % of all devices that were read with an error of less than the corresponding bin value, color-coded stack for each type of resistor. (d) Normalized reading errors as in (c) per type of resistor.

grown on 6″ silicon wafer to serve as an insulating medium, followed by thin metal adhesive film (Ti or Cr) and Pt bottom electrode layer, both deposited with electron beam evaporation. Then, TiO_{2-x} active layer was deposited by plasma-assisted reactive magnetron sputtering. Finally, a metal top electrode layer was evaporated on top of the TiO_{2-x} film. Each layer was patterned by optical lithography, followed by a liftoff process to define the devices. Standalone and crossbar devices with various effective areas from 60 × 60 down to 1 × 1 μm^2 were fabricated. The following results shown in Fig. 6 were obtained from 2 × 2 μm^2 crossbar devices with the stack Ti/Pt/TiO_{2-x}/Pt (5/10/25/10 nm), diced in individual crossbars and packaged in standard DIP PLCC68 compatible with the mCAT setup [Fig. 6(f)]. Fig. 7 shows measurements attained from 30 × 30 μm^2 crossbar devices accessed directly on wafer, with the stack: Cr/Pt/TiO_{2-x}/Pt (3/5/25/4 nm).

A pulsing sequence recorded for one device is shown in Fig. 6(a) showing resistance modulation in between four different intermediate states. We have exploited the mCAT's capability to perform read operations at variable voltages (with a fixed sense resistor) in order to obtain a low-voltage I–V characteristic of the device under test (DUT). It is confirmed that the DUT is indeed a linear resistor [Fig. 6(c)]. The full 32 × 32 array was measured before and after

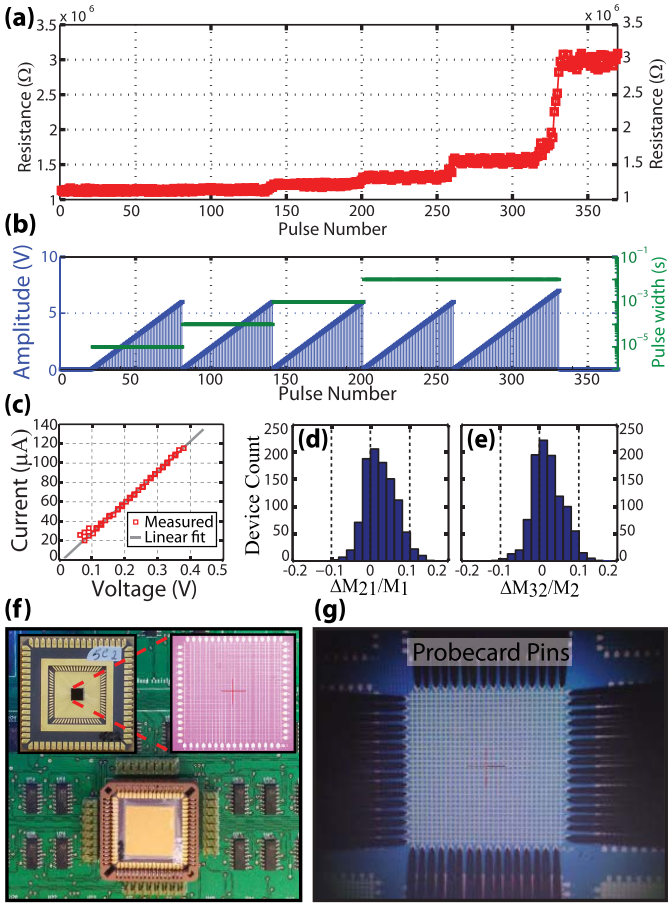

Fig. 6. (a) Modulation of resistance of a single solid-state TiO_{2-x} memristor cell (M_t located in a 32 × 32 crossbar array under (b) pulsing scheme. (c) I–V curve of target device in (a) under low potentials. Gray line: successful linear fit $y = 0.307\,\mu S \cdot x$. (d) Normalized readouts for all devices in the prototype array without the target device M_t: $\Delta M_{21} = M_2 - M_1$, where M_1 and M_2 represent the read resistances of all 1023 devices, before (M_1) and after (M_2) the application of the pulsing scheme of (b) to M_t. (e) Same normalized readout errors $\Delta M_{32} = M_3 - M_2$, where M_3 represents the read resistances immediately after the pulsing of M_t and the read sequence of M_2. The error distribution is similar. (f) Packaged 32×32 RRAM cells in standard PLCC68 package, connected to the mCAT. Inset: exposed memristor die. (g) Microscope photograph of a 32 × 32 TiO_{2-x} RRAM crossbar array on wafer interfaced by the mCAT via a 64-pin probe card.

the application of this pulsing scheme, and the distribution of the normalized resistance difference between the two iterations, excluding the target device, is plotted in Fig. 6(d) and (e). The resistance differences are within the noise floor and as such the inset shows minimal disturbance to inactive devices during programming of a single RRAM cell.

Furthermore, the mCAT can be linked via external connectors located around the package holder to an external 64-pin probe card, which facilitates interfacing on 32 × 32 crossbars directly on wafer [Fig. 6(g)]. A full read of one RRAM crossbar array on wafer (Cr/Pt/TiO_{2-x}/Pt stack of 30 × 30 μm^2 surface area) is shown in Fig. 7(a) with the distribution of read states in Fig. 7(b). Each device was then subjected to a positive pulse train of 10-ms width and amplitude 0–8 V in 0.25 V steps, with the goal of switching to a resistive state lower than $R_{ON} = 100\ k\Omega$ (electroforming). Full array reading after the programming run is illustrated via color-coding in Fig. 7(c) with its associated resistive

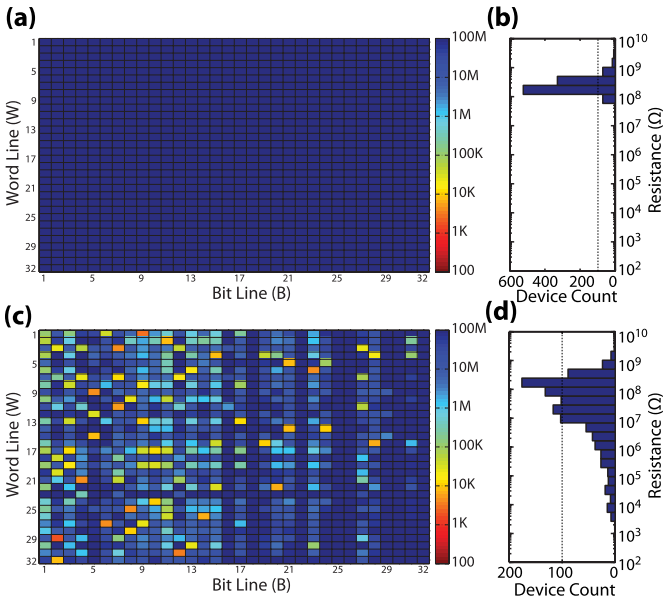

Fig. 7. Measurements from a TiO_{2-x} RRAM crossbar on wafer. (a) Full array measurement before programming. (b) Resistive state distribution for (a). (c) Full array measurement after programming. (d) Resistive state distribution for (c).

state distribution in Fig. 7(d), showing scattered successfully electroformed devices directly on wafer.

V. Discussion

There are a couple of aspects that limit the performance of a system similar to the mCAT. One is concerned with the reading errors that can be substantial in cases where the target resistance (M_t) is high and the inactive bit (M_b) and wordline (M_w) resistances are low. In order to mitigate the influence of M_w on M_t, a read feedback buffer with zero offset and a FET input stage must be utilized [Fig. 2(c)]. On the other hand, M_b provides current via the feedback buffer to the active bitline access MUX switch resistance, lifting the ground potential [Fig. 2(c)]. Another limitation is represented by the minimum programming pulse width, which is restricted by the speed of the bias generator op-amp [Fig. 3(b)], parasitic impedance on the active signal line, and the mBED clock. As such, the nonzero resistance of the analog switches, along with the finite offset of the read feedback buffer, plays a major role in the estimation of the target device resistance.

In order to quantify the behavior of our implemented reading method, the circuit during the read operation has been simulated in PSPICE for array sizes up to $N \times N = 128 \times 128$. Our employed devices consist of a $Pt/TiO_2/Pt$ stack, which based on their structure can boast a range of parasitic line resistance R_l and device capacitance Cp. Fabricated thin-film RRAM devices reported in the literature usually have an electrode size F (feature size) of 10 nm–10 μm with electrode thickness h of 10–100 nm and active core thickness d of 10–100 nm. In a $4F^2$ dense crossbar array configuration, these various device structures would yield a line resistance of $R_l = 2\rho_{Pt}/h$ (where ρ_{Pt} is the resistivity of Pt), which can vary in between 21.2 and 2.12 Ω. Concurrently, the range of parasitic capacitance Cp of these structures (calculated as: $Cp = \varepsilon_0 \varepsilon_{TiO_2} F^2/d$, where ε_0 is the permittivity of free

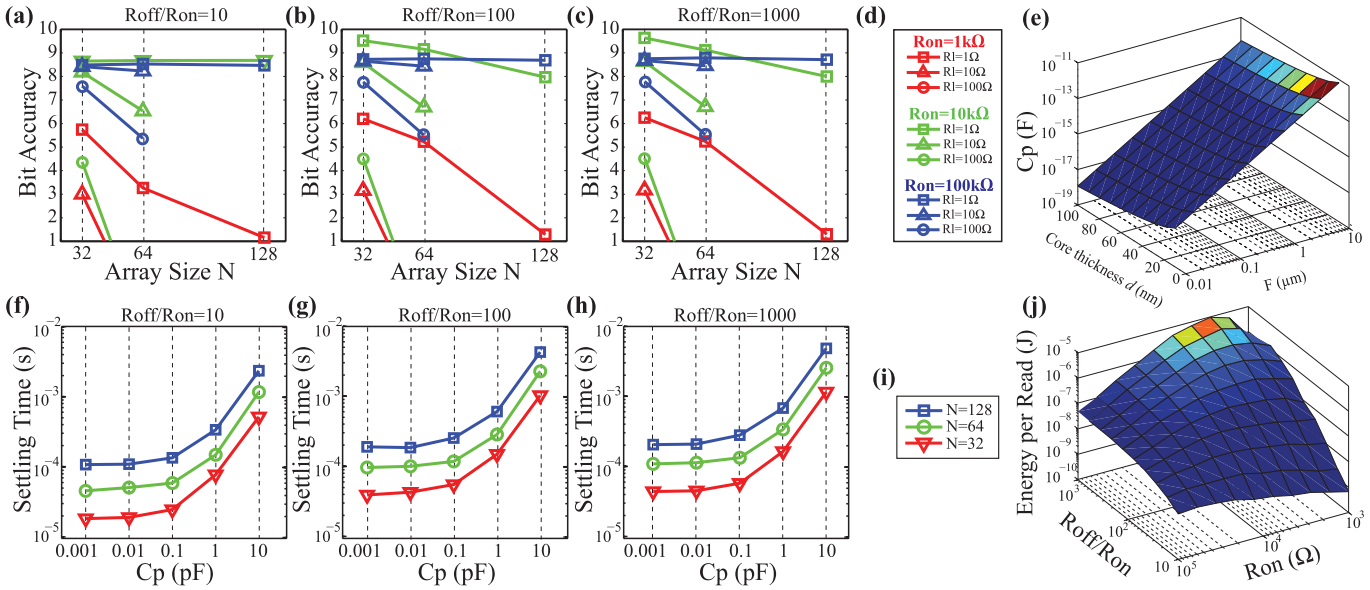

Fig. 8. Effect of parasitic line resistance R_l on the reading bit accuracy for $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ of (a) 10, (b) 100, and (c) 1000. (d) Legend for (a)–(c). (e) Parasitic capacitance Cp of $Pt/TiO_2/Pt$ devices with a range of possible structures. Effect of parasitic device capacitance C_p on speed of reading related to active wordline settling time for $R_{\mathrm{ON}} = 100$ kΩ and $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ of (f) 10, (g) 100, and (h) 1000. (i) Legend for (f)–(h). (j) Energy per read of one reading operation of a $M_t = R_{\mathrm{OFF}}$ using $R_{\mathrm{sense}} = 1$ MΩ for a range of $R_{\mathrm{OFF}}/R_{\mathrm{ON}} = (10, 1000)$ and $R_{\mathrm{ON}} = (1, 1000)$ kΩ, $C_p = 100$ fF and $N = 128$.

space and $\varepsilon_{TiO_2} = 100$ is the room temperature dc relative permittivity of TiO_2 [22]) is shown in Fig. 8(e) and can be contained in the range of 1 aF–10 pF. Due to some structures being impossible to fabricate and thus not representing realistic devices (e.g., $F = 10$ nm with $h = 100$ nm), the C_p parameter was constrained to 1 fF–10 pF in our subsequent simulations.

A line resistance range of $R_l = [1, 10, 100]$ Ω and access resistances $R_a = 9$ Ω (typical) have been introduced in the simulation run which involves probing an $N \times N$ array of devices with resistance R_{ON}, connected to the read buffer and the R_{sense} bank via R_a. A target resistor of M_t is placed at position $N \times N$, to simulate a worst case scenario. A read operation is performed and recorded by SPICE for $M_t = R_{\mathrm{ON}}$, and another one for $M_t = R_{\mathrm{OFF}} = R_{\mathrm{ratio}} * R_{\mathrm{ON}}$, where $R_{\mathrm{ratio}} = [10, 100, 1000]$. This process is repeated for $R_{\mathrm{ON}} = [1, 10, 100]$ kΩ and for all sets of N and R_l. Provided M_t can ideally vary in between R_{ON} and R_{OFF} then the voltage read by the mBED ADC1 when using $R_{\mathrm{sense1}} = 1$ MΩ (it was found that R_{sense1} boasts the largest voltage difference) will vary monotonically in between the two corresponding boundary cases. For any given array, we define bit accuracy as $\log_2(V_{\mathrm{bias}}|_{M_t=R_{\mathrm{OFF}}} - V_{\mathrm{bias}}|_{M_t=R_{\mathrm{ON}}}/\mathrm{ADCres})$, where V_{bias} is the voltage read from our sensing node while reading the worst corner device M_t at $N \times N$ and ADCres is the resolution of our on-board mBED ADC1 (1LSB ≈ 3.3 mV). We utilize this figure of merit to quantify the performance of our simulated mCAT for larger scale arrays [Fig. 8(a)–(d)].

For larger arrays, the line resistance degrades the reading accuracy significantly in the case when R_{ON} is small, while its influence is limited when R_{ON} is increased. Equally important is the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratio, which for the values of low R_{ON} (1 and 10 kΩ) is proportional to the bit accuracy. For large R_{ON}, the system performs similarly for the different values of $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ and R_l for array sizes up to 128×128. This may be due to the fact that the lumped components M_w and M_b are large enough not to interfere due to the offset voltage of the read feedback buffer, and R_l is minute compared with R_{ON} to play a measurable role.

We have further quantified the influence of C_p on the maximum throughput of the reading operation, which is inversely proportional to the active wordline settling time when probing one target device with V_{read} through R_{sense1} [Fig. 8(e)–(g)]. Due to the complexity of the problem and the large range of free parameters, the analysis of the influence of C_P and R_l was performed separately. The simplified circuit of Fig. 2(c) was expanded to include lumped parasitic $C_{P\mathrm{inactive}} = N(N-1) \cdot C_p$ and $C_{P\mathrm{bias}} = N \cdot C_p$ components at nodes V_{inactive} and V_{bias}, respectively. SPICE transient simulations of a reading operation, where $R_{\mathrm{ON}} = 100$ kΩ and $R_{\mathrm{sense}} = 1$ MΩ, have been performed for different states of the full $N \times N$ array: $N = [32, 64, 128]$, $R_{\mathrm{OFF}}/R_{\mathrm{ON}} = [10, 100, 1000]$ and $C_p = (0.001, 10)$ pF. It has been found that the worst case scenario representing the longest active wordline settling time occurs when $M_t = R_{\mathrm{OFF}}$, and all other elements of the array are R_{ON}. As shown in Fig. 8(f)–(h), the highest reading throughput using the mCAT circuitry can be achieved for a 32×32 array of low C_p and low $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratio. This value degrades with increasing array size and with increasing C_p. However, it has been proven [23] that RRAM devices exhibit capacitive switching, adding another level of variability when quantifying maximum possible throughput.

An example of the maximum energy dissipation during one read operation of a target device $M_t = R_{\mathrm{OFF}}$, when the rest of the array elements are R_{ON}, for an array of 128×128 size, $C_p = 100$ fF and a range of R_{ON} and $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratios is shown in Fig. 8(h). The maximum energy dissipation (only related to the crossbar array itself, neglecting amplifier power costs; calculated using energy dissipated in M_t and M_b during rise time and for 2.5 μs sample acquisition time)

in the array occurs when the employed devices have a large R_{OFF}/R_{ON} ratio and moderate R_{ON}. However, the same device feature boasts the largest possible bit accuracy, for any R_l, as shown in Fig. 8(c). Furthermore, the large R_{OFF}/R_{ON} ratio will also decrease the reading throughput. In the opposite case, the lowest power dissipation occurs for low R_{ON} and low R_{OFF}/R_{ON} which would, however, infer a low bit accuracy [Fig. 8(a)] and such the difficulty to distinguish in between more than two states, provided $R_l < 1\ \Omega$. Nevertheless, Fig. 8 shows the complex interplay in between all crossbar parameters and suggests that future RRAM implementations will require devices tailored to specific applications in order to achieve the necessary performance.

In the case where the system should only distinguish bistable (1-bit accuracy) RRAM cells which toggle between R_{ON} and R_{OFF}, the reading limitations relax dramatically. Depending on the R_{OFF}/R_{ON} ratio and R_{ON}, the mCAT can measure binary RRAM chips of up to 128×128 crossbar size, provided the associated line resistance is equal or below 1 Ω. Compared with the ADC method described herein for bistable crossbars, the traditional current sensing schemes are more suitable for such large scale applications, as the one described in [16]. However, as the mCAT is a research tool first, and not hindered by speed requirements or energy efficiency, the ADC-based reading method is essential for acquiring absolute values of cell resistance which accelerates mass testing of an infant technology such as RRAM. Nonetheless, the successful implementation of selectorless RRAM equally depends on the reading/writing method and on the characteristics of the devices employed.

VI. Conclusion

The mCAT is a low-cost, versatile platform for measuring and programming of RRAM cells as single devices, or in a 32×32 crossbar array configuration. The reading and programming schemes ensure that each cross-point resistance can be isolated from adjacent devices by active sneak path current redistribution. For reading analog values of resistance, our platform is capable of measuring standalone resistive cells in the range of 100 Ω–10 MΩ with <5% error and excellent precision ($\sigma < 3\%$). In our custom discrete resistor crossbar array, under high stress conditions (low impedance sneak paths), 90% of devices in 1 kΩ to 1 MΩ range were measured with <10% error. While interfacing with solid-state RRAM cells, applying programming pulses exerts halved interference on remaining inactive devices, minimizing the risk of accidentally modulating their resistive states.

Large-scale arrays have been simulated, and the effect of parasitic capacitance and line resistance has been examined. The limitations of the mCAT have thus been quantified and related to active device characteristics.

The platform's versatility is promoted by the use of a NXP mBED microcontroller that controls the adjacent mixed-signal circuitry. The mCAT is controlled via a MATLAB GUI which allows seamless interaction with 32×32 RRAM crossbar arrays, packaged or directly on wafer via a custom probe card. The latter method speeds up the process of mass testing of RRAM crossbars by discarding the packaging step.

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Authors' photographs and biographies not available at the time of publication.