UNIVERSITÄT BONN
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Counting and Integrating Microelectronics Development for Direct Conversion X-ray Imaging

von
Edgar Kraft

A novel signal processing concept for X-ray imaging with directly converting pixelated semiconductor sensors is presented. The novelty of this approach compared to existing concepts is the combination of charge integration and photon counting in every single pixel. Simultaneous operation of both signal processing chains extends the dynamic range beyond the limits of the individual schemes and allows determination of the mean photon energy. Medical applications such as X-ray computed tomography can benefit from this additional spectral information through improved contrast and the ability to determine the hardening of the tube spectrum due to attenuation by the scanned object. A prototype chip in 0.35-micrometer technology has been successfully tested. The pixel electronics are designed using a low-swing differential current mode logic. Key element is a configurable feedback circuit for the charge sensitive amplifier which provides continuous reset, leakage current compensation and replicates the input signal for the integrator. The electronic characterization of a second generation prototype chip is described and a detailed discussion of the circuit design is given.

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Abstract

A novel signal processing concept for X-ray imaging with directly converting pixelated semiconductor sensors is presented. The novelty of this approach compared to existing concepts is the combination of charge integration and photon counting in every single pixel. Simultaneous operation of both signal processing chains extends the dynamic range beyond the limits of the individual schemes and allows determination of the mean photon energy. Medical applications such as X-ray computed tomography can benefit from this additional spectral information through improved contrast and the ability to determine the hardening of the tube spectrum due to attenuation by the scanned object. A prototype chip in 0.35-micrometer technology has been successfully tested. The pixel electronics are designed using a low-swing differential current mode logic. Key element is a configurable feedback circuit for the charge sensitive amplifier which provides continuous reset, leakage current compensation and replicates the input signal for the integrator. The thesis focusses on the electronic characterization of a second generation prototype chip and gives a detailed discussion of the circuit design.

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1. Introduction

This thesis discusses the implementation and characterization of a new signal processing concept for semiconductor X-ray sensors for the use in computed tomography (CT) and medical imaging in general. The research was conducted as part of an activity which is pursued jointly by the Universities of Bonn and Mannheim and the Philips Research Laboratories Aachen.
The principal idea of the new signal processing concept is to include single photon counting and charge integrating signal processing channels into every picture element (pixel) of the detector system. If the circuit is designed in such a way that both channels can operate simultaneously on the same input signal, the dynamic range of the system can be extended beyond the limits of the individual channels. Furthermore, additional spectral information is obtained in the region where the dynamic ranges of both channels overlap. This essentially adds a new dimension to the acquired data by not only measuring the signal intensity but also the average energy of the photons constituting the signal. The additional information is obtained without the need to increase the radiation dose.
These properties of the new signal processing concept should allow to build X-ray detector systems which deliver 'colored' X-ray images[1] with a high contrast, high dynamic range and an electronic noise performance which is better than the expected quantum noise due to photon number fluctuations in the X-ray signal. The intended application in a CT system imposes two additional requirements: a high image acquisition rate of several kHz and the possibility of a dead-time free operation.
The signal processing chip itself does not actually detect X-ray photons, it analyzes the signal created in a pixelated sensor whose electrodes are connected to the inputs of the picture elements on the chip. This is the reason why the chip is often referred to as a *readout chip*. In the course of this thesis, two generations of prototype chips were developed and characterized. The main focus of this thesis is the discussion of the results obtained with the second prototype chip. Even though the prototype chip features input pads for the connection to a sensor, the measurements discussed here will only deal with the electronic characterization of the chip with test signals produced by circuits on the chip. The evaluation of the imaging performance with actual X-ray signals and different sensor materials lies beyond the scope

[1] The term 'colored' refers to the obtained spectral information.

of this work and will be covered elsewhere[2]. The extensive set of test circuits on the prototype chip, however, allows an exhaustive investigation of all aspects of the prototype and the signal processing concept itself.
The following discussion is structured as follows:

2. Fundamentals This chapter briefly discusses the basic physical processes underlying medical X-ray imaging.

3. X-ray Imaging reviews the technologies underlying the detector systems commonly used in medical imaging, starting with conventional film-based systems and covering computed radiography, digital radiography and fluoroscopy systems up to the direct-converting hybrid pixel systems which are currently under development.

4. Counting and Integrating Readout Concept contains the detailed explanation of the concepts and circuits involved in the implementation of the new signal processing scheme. It starts with a brief explanation of the motivation for the new concept and gives an introduction to the prototype chips involved. The subsequent sections explain the photon counter and the integrator, followed by a detailed discussion of the feedback circuit, which is the central (and arguably most complicated) element of the signal processing concept. Sections reviewing the charge injection circuits, the digital logic and the data acquisition system conclude the chapter. The research of the underlying transistor-level concepts necessary for the implementation of the signal processing scheme was conducted as part of the doctoral thesis of I. Peric and is documented in [1].

5. Experimental Results This chapter provides experimental evidence for the claims made in this introduction. It contains measurements investigating the performance of photon counter and integrator separately, followed by a characterization of the feedback circuit and the behavior in simultaneous counting and integration mode. After a discussion of the power consumption and a demonstration of the dead-time free image acquisition mode, the section finishes with a summary of the obtained results.

6. Conclusions and Outlook summarizes the findings of this thesis and gives an overview over potential improvements to the prototype.

Appendix The appendix contains descriptions covering some subcircuits in more technical detail. They are provided rather for matters of completeness and are not fundamentally relevant for the understanding of the signal processing concept.

[2] At the time of writing, measurements on such an X-ray imaging system are being carried out by Johannes Fink, a colleague of the author, as part of his doctoral thesis.

Some of the results obtained during the research for this thesis have already been published in [2], [3] and [4]. The signal processing concept and the integrator design have been patented by Philips [5] [6].

2. Fundamentals

Any form of X-ray imaging utilizes the interaction of electromagnetic radiation with the imaged object and the sensor material. In the energy range relevant for medical imaging (i.e. about 1 keV to 150 keV), this interaction is either caused by the photo effect or by Compton scattering. At higher energies, photons can also interact through pair production ($\mathrm{E}_\gamma > 2\mathrm{m}_e \approx 1.022$ MeV) and nuclear photo effect.

2.1 Photo Effect

The photo effect is the absorption of a photon by an electron in the atomic shell. Since the energy of the photon is completely transferred to the electron, the electron is emitted from its atom with a remaining kinetic energy of $E_\gamma - E_b$, with E_γ being the photon energy and E_b the binding energy of the electron.
The cross section of the photo effect σ_{photo} cannot be described in a single analytic expression over the full energy range. In the range between the K-edge and the rest energy of the electron $m_e = 511$ keV, the cross section of the photo effect can be expressed as [7]:

$$\sigma_{photo} = \frac{32}{3}\alpha^4\sqrt{2}\pi r_e^2 \left(\frac{m_e c^2}{E_\gamma}\right)^{\frac{7}{2}} Z^5. \tag{2.1}$$

Here, α is the fine-structure constant, $r_e = 2.82$ fm is the classical electron radius, c is the velocity of light and Z is the atomic number of the absorber material. The key point is that the cross section scales with the fifth power of the atomic number, which makes high-Z substances the most promising sensor material.
The vacancy left in the atomic shell after the emission of the primary electron is quickly filled by an electron captured from the medium or from a higher shell. This electron emits its surplus energy either through a photon in a process called fluorescence or by transferring the energy to another electron in the atomic shell, which is then ejected from the atom (Auger process). The absorption length (explained below) of the fluorescent photon depends on the sensor material and the shell from which the primary electron is ejected. Even for the most energetic fluorescent photons, which arise from transitions to the K-shell, the absorption length lies usually in the range

of a few ten micrometers, so that its deposited energy is detected together with the energy of the primary electron. If however, the photon escapes the sensor material, its energy is lost and the detected energy is reduced. This appears in X-ray spectra of a mono-energetic source as a second line which is shifted by the energy of the K-edge, an artefact known as *escape peak*.

2.2 Compton Effect

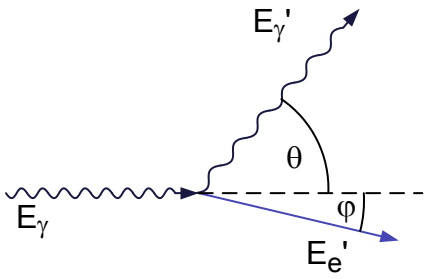

Fig. 2.1: Illustration of the Compton scattering process of an incident photon with energy E_γ at an electron. The interaction transfers energy and momentum from the photon to the electron, giving it a final energy of $E'_e = E_\gamma - E'_\gamma$ [8].

The Compton effect is the inelastic scattering process between an X-ray photon and a free electron. Electrons bound in an atom can be considered free for photon energies much larger than the binding energy. The amount of energy transferred from the photon to the electron E'_e is given given by

$$E'_e = E_\gamma - E'_\gamma \tag{2.2}$$

where E_γ and E'_γ are the photon energies before and after the interaction. The energy transfer depends on the angle θ between the incident and the scattered photon (see Fig. 2.1):

$$E'_\gamma(\theta) = \frac{E_\gamma}{1 + \frac{E_\gamma}{m_e c^2}(1 - \cos\theta)} \tag{2.3}$$

It becomes maximal if the photon is scattered back to the direction it came from (at θ=180°):

$$E'_e(\text{max}) = \frac{2\epsilon}{1+2\epsilon}\, E_\gamma \qquad \text{with} \tag{2.4}$$

$$\epsilon = \frac{E_\gamma}{m_e c^2} \tag{2.5}$$

$E'_e(\text{max})$ is also known as the *Compton edge*. The energy distribution of the scattered electrons takes a characteristic form, as depicted in Fig. 2.2. The

underlying cross section $\sigma_{compton}$ can be computed using the Klein-Nishina formula, a detailed derivation is given in [7]:

$$\sigma_{compton} = 2\pi r_e^2 \left(\frac{1+\epsilon}{\epsilon^2} \left(\frac{2(1+\epsilon)}{1+2\epsilon} - \frac{1}{\epsilon} \ln(1+2\epsilon) \right) + \frac{1}{2\epsilon} \ln(1+2\epsilon) - \frac{1+3\epsilon}{(1+2\epsilon)^2} \right) \tag{2.6}$$

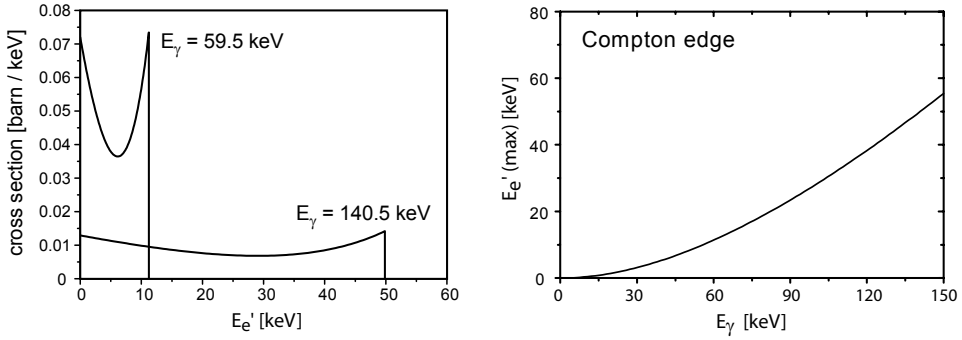

Fig. 2.2: Left: Energy distribution of the Compton electrons $\mathrm{d}\sigma/\mathrm{d}E'_e$ as a function of the energy of the scattered electron for two different photon energies. Right: Position of the Compton Edge as a function of the photon energy [8] [9].

2.3 Absorption Coefficient

The number of photons N which are transmitted through a material layer decreases exponentially with the thickness x, as is described by the Lambert-Beer law:

$$N = N_0 \cdot e^{-\mu x} \tag{2.7}$$

with N_0 being the number of incident photons and μ being the (total) absorption coefficient. The absorption coefficient has the unit $[\mathrm{m}^{-1}]$, its reciprocal value is also known as the *attenuation length*. The coefficient summarizes the probabilities for all types of interactions which can occur in the material and is thus related to their respective cross sections:

$$\mu_{total} = \mu_{photo} + \mu_{compton} \; (+\mu_{pair} + \mu_{nuclear}) \quad \text{with} \tag{2.8}$$

$$\mu_{photo} = \rho \, \frac{N_A}{A} \, \sigma_{photo} \tag{2.9}$$

$$\mu_{compton} = \rho \, \frac{N_A}{A} \, Z \cdot \sigma_{compton} \tag{2.10}$$

Here, ρ is the material density, N_A is the Avogadro constant and A is the nuclear number. The Compton term also contains the factor of the atomic number Z, which accounts for the fact that the Klein-Nishima formula describes the cross section for only a single electron. Fig. 2.3 compares the

contributions of photo effect and Compton effect in two common sensor materials. In cadmium telluride (one of the favored high-Z sensor materials), the photo effect is dominant at all energies $\leq$ 150 keV. Silicon has a much smaller photo effect and total absorption coefficient due to its small atomic number (i.e. 14, compared to an average of 50 in CdTe). This leads to a crossover between the two contributions so that Compton scattering is the dominant mechanism at energies above 60 keV (compared to 260 keV in CdTe).

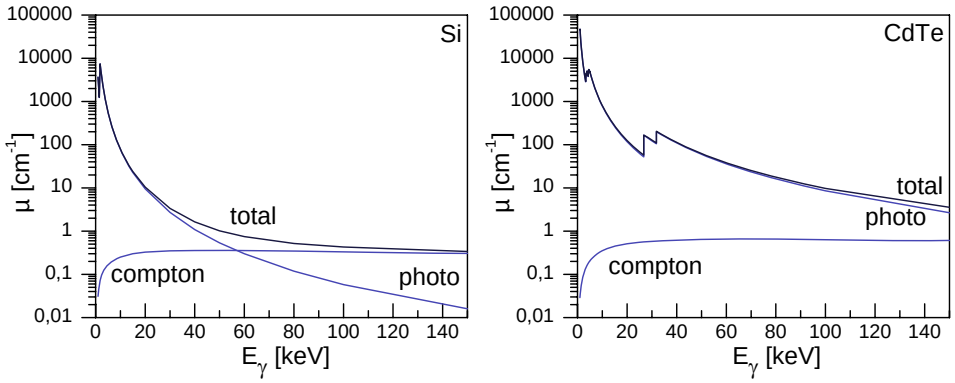

Fig. 2.3: Comparison of the contributions of photo effect and Compton effect to the absorption coefficient in silicon (left) and cadmium telluride (right) over the energy range relevant for medical imaging [10].

3. X-ray Imaging

The usefulness of X-rays for medical imaging was recognized immediately after their discovery by Wilhelm Conrad Röntgen in 1895. Fig. 3.1 shows the famous X-ray image of his wife's hand.

Fig. 3.1: X-ray image of Anna Bertha Röntgen's hand, December 28, 1895.

3.1 Photographic Film

The recording of X-ray images with photographic film (or photographic plates) was not only the earliest method, it still remains in use today, even though gradually being replaced by the newer, digital methods covered below. Photographic film is basically a sheet of plastic which is covered with a photosensitive emulsion containing silver halide salts. The grain size of these crystals determines the sensitivity and resolution of the film. After exposure, the film needs to be developed in order to obtain a visible image.
The reasons for the continuing popularity of this method are the small initial cost of a film-based imaging system, the high achievable spatial resolution of a few micrometers, the flexibility of the medium and the availability of film sheets in many sizes. The major drawback of photographic film is the low quantum detection efficiency of only 1-2%. This can be addressed by coating the film with sensitive layers on both sides and by covering the photosensitive emulsion with phosphor layers which convert incident X-ray radiation into visible light. Common phosphor materials are fluorescent salts like $CaWO_4$ and rare earth compounds such as $YTaO_4$:Nb and Gadolinium

oxysulfide (Gd_2O_2S:Tb) [11]. Even though photographic films with such coatings achieve detection efficiencies between 20% and 60%, the higher efficiency is paid for by a reduced spatial resolution [12].
Another drawback is the limited dynamic range of the film, which can lead to over- and/or underexposure of the image. This problem can be worsened during developing, which introduces an additional source for errors. The developing itself is a drawback on its own right, since it not only introduces a delay of several minutes, but also involves chemicals which are both hazardous and relatively expensive in the long term.

3.2 Photostimulable Phosphor Plate

Computed Radiography (CR) uses the same equipment as film-based systems with the only difference that the film cassette is replaced by a photostimulable phosphor plate. These plates, also known as *storage phosphors*, capture the X-ray image in a phosphor layer which traps electrons excited by the incident radiation in so called 'color centers'. Suitable phosphors are commonly found in the barium fluorohalide family, with BaFBr:Eu^{2+} being a typical example [13]. The trapped charges remain stored in their metastable states

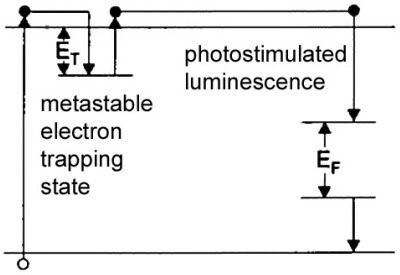

Fig. 3.2: Energy level diagram for photostimulable phosphor imaging. The electrons excited in initial exposure with X-rays are trapped in a metastable state. A second irradiation with a red laser beam raises the electrons into the conduction band, from which they decay emitting blue light [14].

until they are raised to the conduction band by irradiation with a scanning red laser beam. Subsequent recombination at one of the activator atoms (in this case Eu^{2+}) causes the emission of light at a shorter wavelength (blue), a process known as photostimulated luminescence (see Fig. 3.2). The emitted photons are detected by a photomultiplier and converted into an electronic signal, which is then digitized and stored as a 2D image (using the position of the scanning laser beam). Exposing the plate to room-level illumination erases the image and prepares the plate for the recording of a new X-ray image. Depending on the care taken during handling, plates can be reused up to a thousand times. A schematic view of such a CR system is shown in Fig. 3.3. The spatial resolution of a phosphor plate imaging system depends

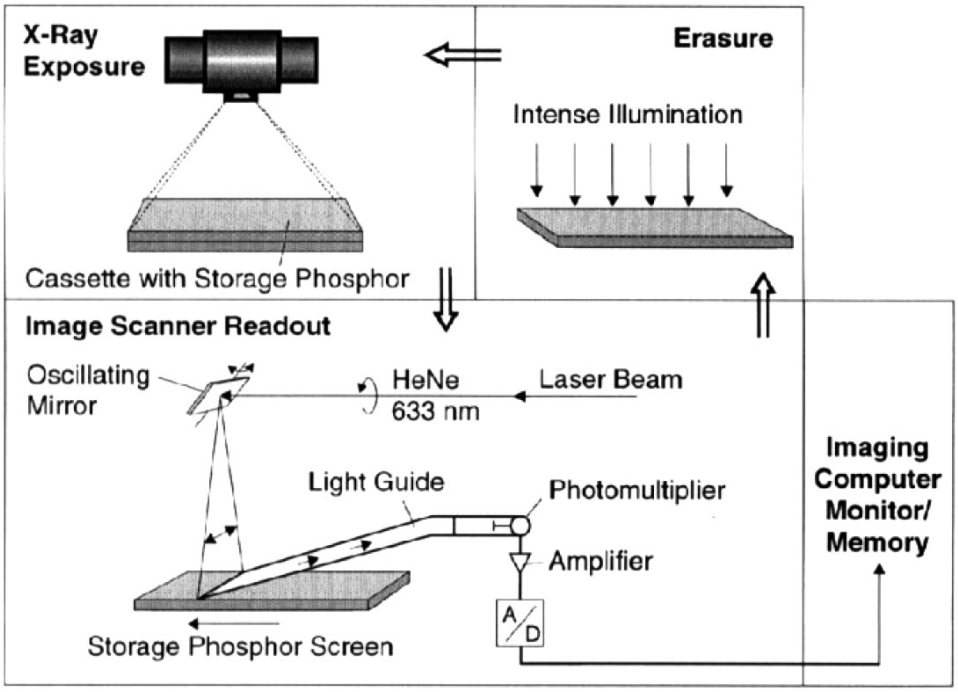

Fig. 3.3: Schematic representation of a photostimulable phosphor radiography system [14].

mostly on the size of the laser spot and lies typically at about 100 µm [15]. An additional factor for the image quality is the amount of light scatting in the phosphor layer. Photostimulable phosphor plate systems were quite successful in replacing film-based systems, because they offer several key benefits while still allowing to reuse existing equipment:

- The larger dynamic range of phosphor plates, about 10^4 to 10^5 compared to about 10^2 in photographic film [15], helps to avoid faulty exposures. A comparison is shown in Fig. 3.4. Combined with the possibilities of contrast and brightness adjustments provided by digital image processing, this allows to examine a wide range of thicknesses with a single measurement.
- Faster acquisition speeds. The scanning process takes about one minute compared to about 5-7 minutes for the developing of an conventional photographic film.
- The image is already present in a digital format and is easily stored, copied or transmitted for off-site review.

The major drawback of a CR system compared to a film-based system is the cost. Compared to other, fully digital systems, the main disadvantage is the laborious scanning of the plates, which makes real-time imaging impossible.

Fig. 3.4: Comparison of the imaging results at different exposure settings obtained with a film based system (left) to those obtained with a photostimulable phosphor plate (right). The dynamic range of the phosphor plate is superior to the film even under optimal conditions [12].

3.3 Image Intensification

X-ray image intensifiers (XRII) are vacuum tubes in which an X-ray image is transformed into a visible light output image with high luminosity. Incident X-ray radiation enters the intensifier through a thin input window and is converted to visible light in a phosphor screen (Fig. 3.5). The input window is typically fairly large with diameters of up to 57 cm. A common material for the input phosphor is Caesium iodide (CsI), which has not only a high effective atomic number, but also the benefit that it can be evaporated in such a way that it effectively forms optical wave guides (Fig. 3.6). The light is absorbed by a photocathode which is evaporated directly onto the phosphor surface. The electrons liberated during absorption are accelerated towards the anode by an electric field of about 25-35 keV. Electrostatic beam optics focus the electrons onto the comparably small output phosphor, which converts the electrons back to visible light. One electron produces between 1,000 and 10,000 photons [15], thus increasing the total yield significantly. The gain factor achieved by the acceleration of the electrons and through the demagnification is sufficiently large for the image quality to be determined by the quantum noise due to the limited number of incident X-ray photons. The light emitted by the output phosphor screen is usually converted into a digital image using a CCD camera[1]. This allows not only the acquisition

[1]CCD = *charge coupled device*, described for example in [16].

of static images by integrating the light over a certain time, but also the recording of video signals.

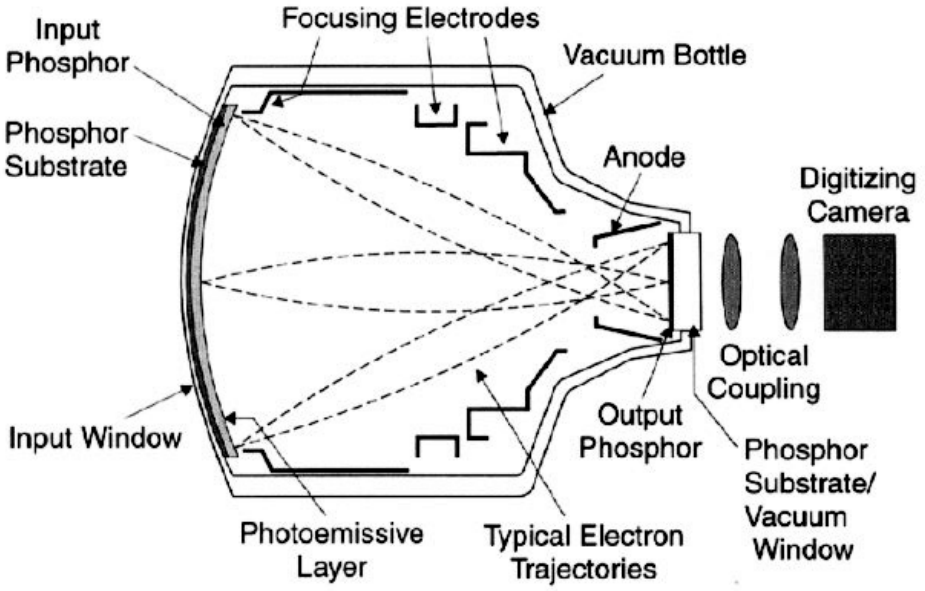

Fig. 3.5: Schematic illustration of an X-ray image intensifier tube [14].

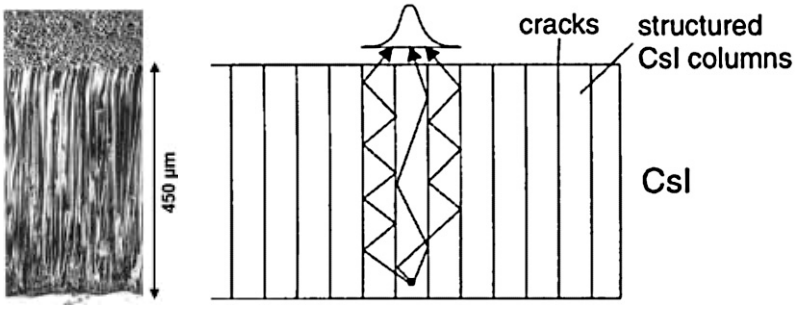

Fig. 3.6: Caesium iodide can be evaporated in a such a way that it produces a columnar structure (left, 10 µm columns) [9]. The segments of this structure effectively act as wave guides, which reduces the lateral light diffusion and improves the spatial resolution (right) [14].

Real-time X-ray imaging, also known as fluoroscopy, is required in applications such as angiography, vascular imaging, cardiac catheterization and for the implantation of cardiac rhythm management devices such as pacemakers. X-ray image intensifiers are gradually being replaced by flat-panel detectors, which are covered below. The spatial resolutions achieved with X-ray imaging intensifiers lie usually below those achieved by film based systems and are

on the order of 2-3 line pairs per mm. Besides their real-time capability, the major advantage of XRIIs is the achieved dose reduction.

3.4 Flat Panel Detectors

Flat Panel Detectors (FPDs) are the current state of the art in digital radiography. They owe their name to the form, which is considerably thinner than the bulky X-ray image intensifiers. There are generally two types of FPD: indirect conversion and direct conversion detectors. Indirect conversion detectors convert the incident X-ray radiation first into visible light photons and then to electronic charge. Direct conversion detectors convert the absorbed radiation directly to a charge signal. The XRII discussed above is thus an example of an indirect detector. This section will first explain the structure of indirect flat panel detectors.

Indirect Flat Panel Detectors

Such detectors consist of a layer of scintillator material (such as gadolinium oxysulphide or cesium iodide) which is coupled to a large-scale array of active picture elements (Fig. 3.7). Each pixel comprises a switching transistor and a photo diode which produces a charge proportional to the intensity of the light generated in the scintillator. Image acquisition is performed row-wise by connecting the respective picture elements to the readout lines and measuring the signal with charge sensitive amplifiers. The active pixel matrix is usually produced on a glass substrate which is covered with a layer of amorphous silicon and imprinted with thin-film-transistors (TFTs) and photodiodes. Besides the detector matrix, the imaging system also contains peripheral circuitry that amplifies, digitizes and synchronizes the readout of the image. Once transferred to a computer, the image can be stored, manipulated and printed as necessary.
The introduction of flat panel detectors has led to a replacement of image intensifiers in fluoroscopy applications (FPDs are also often used in radiology). Similar to XRIIs, flat panel detectors are available with large areas of up to 43 x 43 cm, allow real-time imaging and have a comparable spatial resolution with pixel pitches between 100 µm and 200 µm [11]. Besides the reduced form, their benefits lie in an improved sensitivity to X-rays, improved contrast and dynamic range, immunity to stray magnetic fields and a better temporal resolution, which helps to prevent blurring in moving images. They are, however, considerably more expensive to purchase and repair.

Direct Flat Panel Detectors

The concept of direct conversion flat panel detectors is very similar to that of the indirect type. Instead of a phosphor, direct detectors use a photo-

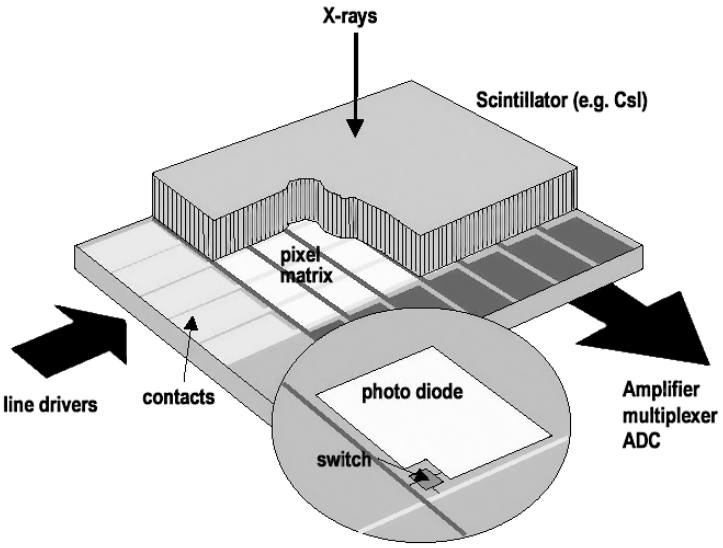

Fig. 3.7: Schematic illustration of an indirect flat panel detector [17].

conductor, commonly amorphous selenium (a-Se), which converts incoming X-ray photons directly to electron-hole pairs. In each pixel, the sensing instrument is a simple charge storage capacitor and a collection electrode, which replace the photodiode of the indirect approach. The backside of the selenium layer is coated with a continuous electrode, which is used to apply the bias voltage (typically several kilovolts) necessary for the collection of the produced electron-hole pairs. Readout of the pixel array is performed in an identical way in both detector types. An image of a commercially available direct FPD is shown in Fig. 3.8.

Fig. 3.8: Flat-panel active-matrix direct-conversion X-ray imager using an amorphous selenium conversion layer with an imaging area of 36 x 43 cm (courtesy of Hologic Inc.) [13].

Both types of flat panel systems share the benefits of high dynamic range and the availability of large-scale processing techniques. Amorphous Selenium panels are devoid of problems due to limited fill factors and lateral light diffusion in the scintillator of indirect converters. On the other hand, new problems arise from the inhomogeneity and from the *afterglow* in the conversion layer (a fraction of the produced signal arrives delayed over a prolonged interval of time).
In a more general sense, the main appeal of direct converting systems compared to the indirect approach lies in the high intrinsic spatial resolution [18] and in the larger number of produced electron-hole pairs per X-ray photon. Both advantages are achieved through the avoidance of an additional conversion step. These benefits are, however, only present to a limited extent for amorphous selenium as a conversion material: Compared to other direct conversion materials like cadmium telluride (CdTe), the number of electrons produced by an X-ray photon is smaller by a factor of 5 to 10, depending on the applied electric field. While the range of the primary electron produced during absorption ranges between 1-3 µm at 10-30 keV and 10-30 µm at 50-100 keV, an additional broadening occurs at energies above the K-edge of selenium (i.e. 12.6 keV). Above this energy, K-flourescent X-rays may be released if the absorbed photon interacts with the K-shell of an atom. Another problem is caused by the large attenuation depth at high photon energies (>1 mm above 60 keV), which requires the usage of a fairly thick conversion layer. This has a severe impact on the achievable spatial resolution if incident X-rays arrive at large angles, since it can reduce the spatial resolution to 250 µm for a-Se photoconductor of 1 mm thickness when illuminated at an incident angle of 15° [19]. In summary, the a-Se based detector panels seem best suited for applications at a low X-ray energy, such as for mammography.

3.5 Direct Conversion Hybrid Pixel Detectors

Hybrid pixel detectors consist of two separate parts, the direct conversion sensor and the *readout chip*. In every pixel, the sensor electrode is connected to the input of its corresponding channel on the readout chip with a bump-bond connection[2] as illustrated in Fig. 3.9. In contrast to the flat panel technology discussed above, the readout chip is usually fabricated from crystalline silicon. This permits to use industry standard processing technologies which provide a high level of electronics integration and allow more advanced signal processing circuits inside the pixels. The separation of both parts removes the necessity to choose a sensor material in which active elements such as switches and amplifiers can be implemented. Instead, the sensor can be made from a wide range of materials and the same readout

[2]The bump-bonding technologies will not be covered here, since the sensor connection lies beyond the scope of this work. A detailed description can be found in [9].

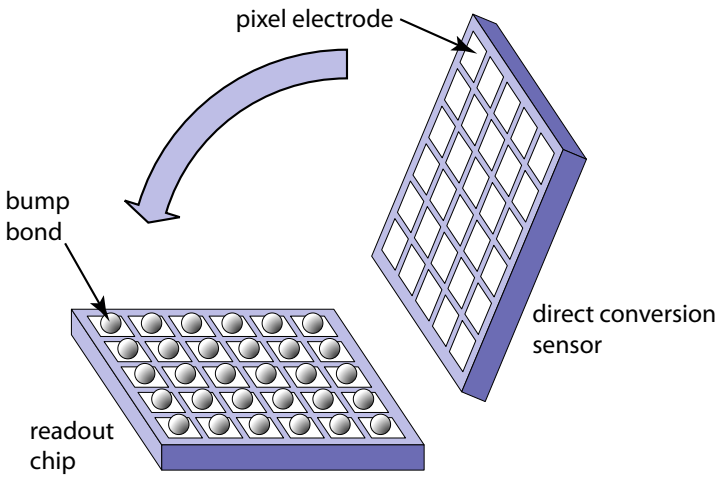

Fig. 3.9: Illustration of a hybrid pixel detector. The pixels of sensor and readout chip are connected in a process known as *flip-chip bump bonding* [8].

chip can be used with different sensor types. Sensor types used successfully in hybrid pixel detectors include Si, GaAs, CdTe, CdZnTe, diamond and 3D-silicon detectors [20] [21] [22] [23] [24] [25]. Readout chips for hybrid pixel detectors used in medical imaging can usually be categorized as either integrating or photon counting systems.

3.5.1 Integrating Pixel Detectors

Integrating systems accumulate the X-ray signal over a certain time interval and provide a measurement which is usually proportional to the total amount of energy deposited by the incident radiation. In this sense, all systems previously discussed in this chapter are integrating systems.
An integrating pixel usually comprises at least a capacitor or integrating amplifier on which the signal charge is integrated and a switch which selects the pixel for readout (similar to the design of an FPD). Small integration capacitances allow a small pixel pitch but often also restrict the dynamic range [9]. An example of a more elaborate design is the *Pixel Array Detector (PAD)* of Cornell University [26], which features an array of 92 x 100 pixels at a pitch of 150 µm x 150 µm and allows high-speed imaging with frame rates of up to 100 kHz [27]. Charge integrating systems are inherently confronted with the problem of sensor gain variations and leakage currents, which produce an input signal even if no X-ray source is present. This often requires the application of gain and offset corrections to the measured signal [28]. A detailed description of a charge integrating readout channel will be given in section 4.3.

3.5.2 Photon Counting Pixel Detectors

Photon counting detectors differ from all previously discussed systems in that they do not measure the total intensity of the incident radiation, but the number of individual photons (with an energy above a certain threshold) constituting the X-ray signal. The pixel cells usually comprise a charge sensitive amplifier, (optionally) a pulse shaper, a discriminator and a digital counter. Section 4.2 contains a detailed description of these circuits.
Since the concept was first introduced in 1997 [29], a number of research activities have developed:

MPEC is the name of the photon counting X-ray activity at Bonn University. The chip design has undergone several iterations. Its current version (2.3) features an array of 32 x 32 pixels at a pitch of 200 µm x 200 µm [9]. Each pixel contains a pair of discriminators, two 18-bit counter cells and a dedicated window logic which allows the counters to record only photons within a definable energy region, a feature used for contrast improvements [30]. The chip was tested with a wide range of sensor materials such as Si and GaAs [21]. It was also the first photon counting pixel detector system featuring CdTe sensors and multichip modules [20]. The MPEC2.3 chip provides pixel count rates up to 1 MHz [8].

Medipix has been developed in a collaboration comprising fifteen European institutes as part of a CERN[3] research project [31]. The chip is currently in its third generation. A prototype chip with a 8 x 8 pixel matrix and a pitch of 55 µm x 55 µm has been produced and tested [32]. Its predecessor, Medipix2, possessed a larger matrix with 256 x 256 pixel with 13-bit counter cells at the same pitch [33] [34]. The small pitch, however, not only provides a good spatial resolution but also confronts the pixel electronics with the problem of significant charge sharing between adjacent pixels. Charge sharing is caused by the diffusion of the produced charge cloud during the collection process. A second source is the emission and re-absorption of K-fluorescent X-ray photons, whose absorption length also lies in the order of the pixel pitch. The problem of charge sharing is especially critical for counting systems since it leads to the omission of events and to a corresponding distortion in the energy spectrum as seen by the pixel. This distortion limits the potential energy resolution of the system. Similar to MPEC, Medipix achieves a maximum count rate of about 1 MHz [35].

PILATUS, the *PIxeL ApparaTUS* for the Swiss-Light-Source, is a large-area silicon detector developed especially for crystallography studies at the synchrotron facility of the Paul-Scherer-Institute (PSI) in Villingen,

[3] CERN = Conseil Européen pour la Recherche Nucléaire

Switzerland [36]. The detector covers a total area of 40 x 40 cm^2 with over four million pixels, each with a size of 217 x 217 μm^2. It is build from modules with a silicon sensor of 300 µm thickness which is connected to 16 readout chips. The whole array can be read out in only 6.7 ms.

XPAD is also a multi-module assembly that was developed for synchrotron radiation crystallography experiments [37]. Each chip contains 24 x 25 pixels at a pitch of 330 µm. The complete detector covers a total area of 7 x 7 cm^2 with 200 x 192 pixels. A speciality of this detector are the maximum photon count rate of 10 MHz and the relatively small dead time between subsequent measurements of 2 ms.

DIXI is a 31 x 32 pixel readout chip with a pitch of 270 µm developed at Uppsala University, Sweden, in collaboration with Ideas ASA, Hovik, Norway [38]. The readout chip is connected to a 500 µm silicon sensor. A speciality of this chip are the two counters which are implemented with digital logic but with capacitors that are discharged step wise. The counted number of photons is obtained by measuring the potential on the capacitors externally.

All photon counting X-ray imaging systems share a number common advantages. The energy threshold setting, if chosen large enough, allows to conduct measurements which are not impaired by the sensor leakage current or noise events. Photon counters are also inherently linear as long as the average photon rate is low enough so that no pile-up of subsequent pulses occurs. This makes these systems especially well suited for measurements at a small photon flux. The signal-to-noise ratio of a measurement is typically only limited by the quantum noise due to fluctuations in the number of absorbed photons. If a mono-energetic radiation source is used, the threshold setting can be chosen in such a way that only photons are counted which have not been scattered in the absorber. This suppression of Compton-scattered photons can greatly improve the image quality.

3.6 Computed Tomography

The basic idea of all computed tomography (CT) scanners is to measure the X-ray absorption along many different lines through the object of interest and to use reconstruction algorithms to compute the three-dimensional absorption profile from the set of projections. The complexity of the reconstruction algorithms depends strongly on the specific set of recorded absorption lines. In the simplest algorithm, *filtered backprojection*, the volume inside the scanner is divided into an three dimensional array of volume elements (voxels). All measurements are projected back along their respective line (which, of course has to be known), adding the recorded intensity to all voxels intersecting the line. Provided enough measurements are taken, so that each voxel is intersected by a sufficient number of lines with a sufficiently different angle, the normalized sum accumulated in each voxel is a measure of its absorption coefficient. Two dimensional images of arbitrary slices through the object in question can then be obtained by plotting the voxels which intersect the image plane.

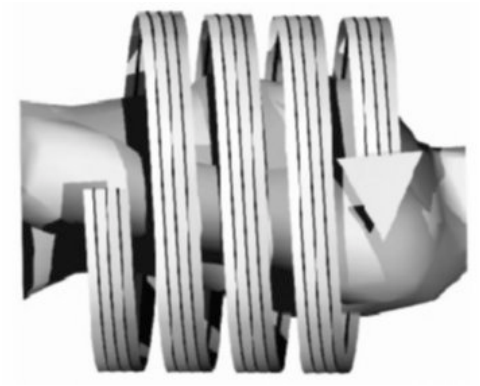

Fig. 3.10: Illustration of the detector movement in a Spiral-CT [17].

Inside the imaged object, areas with a higher absorption coefficient (e.g. a gold filling inside a tooth) cause measurements with a correspondingly low signal intensity. This information is distributed along the projected paths, which can lead to an overestimation of the absorption coefficient in the affected voxels. These artifacts become especially intense in voxels close to the strong absorber and pose a problem for the reconstruction algorithm. State-of-the-art reconstruction algorithms address this problem by introducing *beam hardening corrections* which aim at producing an absorption coefficient profile which is consistent with the obtained measurements. Since the presence of strong absorbers is revealed by the hardening of the transmitted beam spectrum, a detector which is able to detect such beam hardening (such as the system discussed in this thesis) promises to be helpful in improving the quality of the reconstructed image. Measurements demonstrating the

detection of beam hardening are presented in section 5.5.3.
The CT systems differ by the number of detector elements, the shape of the X-ray beam and the motion of the patient table. During a measurement, the setup of detector and X-ray tube (gantry) usually rotates continuously around the patient at rotation rates of up to 3 revolutions per second. The detector itself is usually ring-shaped (similar to a banana). The number of parallel ring elements (slices) is commonly used to classify the CT system[4]. A higher number of slices also corresponds to a faster acquisition speed, which is a surprisingly important factor for the image quality. The reason for this is that motion artifacts due to breathing and heard-beating can be minimized if the total acquisition time interval is short enough.

Implications for Detectors in a CT Application

The fast acquisition times and high rotation rates can only be achieved if the detector is able to handle the short exposure time and reciprocally larger signal intensities (the dose per pixel per measurement must usually be kept constant to retain the same image quality). Typical measurement frame durations range from 50 µs to 300 µs, typical X-ray fluxes can reach up to 10^9 photons /(s mm^2). In the example of an imaging sensor made from CdTe (which has an average electron-hole-pair creation energy of 4.61 eV), an average photon energy of 60 keV and a pixel pitch of 300 µm, the typical input signal of a single pixel computes to:

property	value per pixel
max. photon rate	90 MHz
typical photon pulse size	13,000 e^-(2.1 fC)
max. input current	190 nA

These values will often be used in chapter 5 as typical input signals.

[4]State-of-the-art at the time of writing is the 256-slice scanner manufactured by Toshiba which was installed at the Johns Hopkins University School of Medicine in the beginning of 2007 and which is not yet available commercially.

Dual Source CT

In 2005, Siemens introduced a CT model (Somatom) which uses two separate X-ray tubes and a dual array of 64-slice detectors. The tubes can operate at two different acceleration voltages (e.g. 80 kV and 140 kV [39]), which allows not only to measure the absorption coefficient, but also to estimate the average atomic number in a voxel by separating the contributions of photo-effect and Compton-effect. This is made possible by using the two independent measurements as proposed in [40]. The additional information allows for example the differentiation of calcium (bone material) and iodine (contrast medium). The new pixel concept described in the subsequent

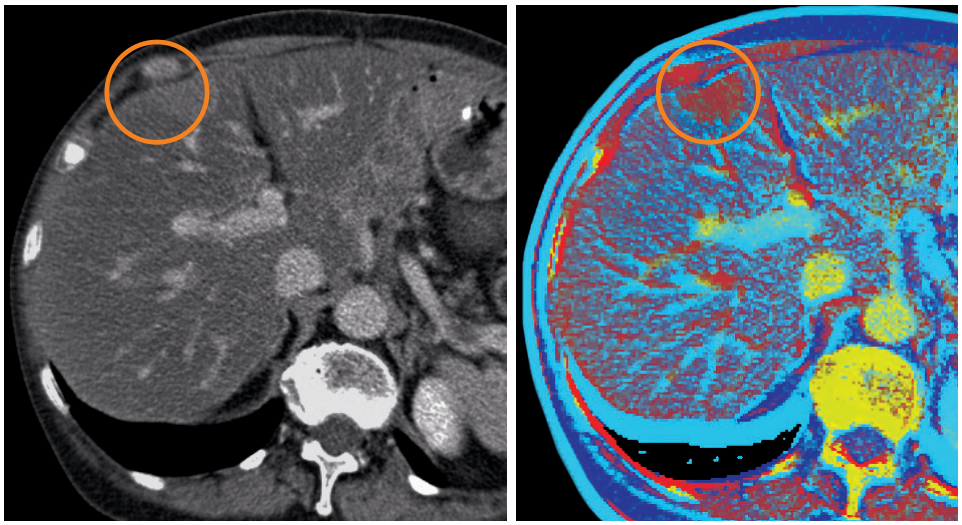

Fig. 3.11: Two measurements illustrating the benefit of the spectral information in a dual-energy CT. The lesion marked in the top left can be identified as a lipid degeneration in the right image whereas it is hardly visible in the left image (courtesy of Siemens AG, Medical Solutions) [39].

chapters also obtains two separate measurements, which allows to determine the spectral hardening of a beam spectrum. Similarly, the measurements should also allow to distinguish between the contributions of photo- and Compton-effect, and obtain similar results without the need for a second X-ray tube or an increased dose. At the time of writing, however, this possibility has not been explored yet.

4. Counting and Integrating Readout Concept

The signal of X-ray imaging sensors is often processed using one of two distinct schemes: photon counting or signal current integration.

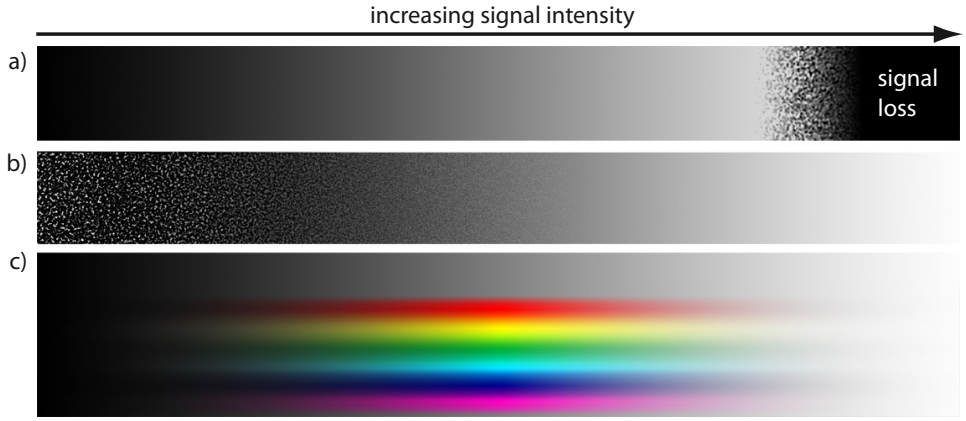

Fig. 4.1: Motivation for simultaneous photon counting and integration. The images show the typical responses of a) photon counter b) integrator and c) a counting and integrating pixel as a function of increasing signal intensities. Brightness and granularity in the images denote signal intensity and noise in the measurements. The counting and integrating scheme can measure signals throughout the combined dynamic range and yields additional spectral information in the overlap region of photon counter and integrator (bottom, denoted by the color gradient).

Counting schemes measure the number of absorbed photons whose deposited energy exceeds a certain threshold [20], [41], [38]. The lowest measurable flux is therefore a single photon per measurement interval. With rising photon flux, it becomes increasingly difficult to distinguish individual charge pulses and the number of unregistered events increases up to the point where no counts are registered at all (Fig. 4.1, a). Unless multiple energy thresholds are used, measurements of the photon count rate do not yield any spectral information besides the minimal energy determined by the threshold.
Schemes measuring the integrated signal current, on the other hand, give information on the total deposited energy [13]. The designs are well suited for large rates and signal currents, but measuring small signals can be difficult

due to electronic noise (Fig. 4.1, center). Furthermore, the integrating technique does not yield spectral information either.

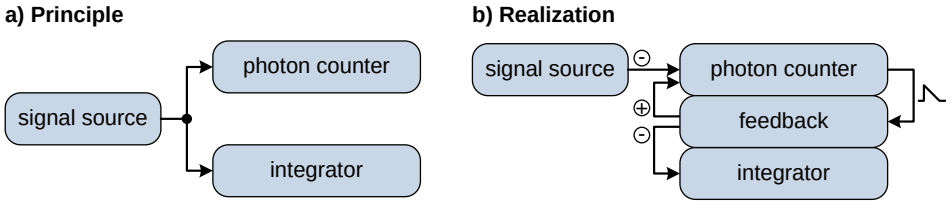

Fig. 4.2: Comparison of the basic idea and the actual realization of a pixel cell allowing simultaneous counting of individual photons and integration of the total signal current. The key element which links both schemes is the circuit providing feedback for the photon counter and signal replication to the integrator.

The concept of simultaneous counting and integrating overcomes the limitations of the individual schemes by measuring both the absorbed photon flux and the deposited energy. This combination does not only extend the dynamic range beyond the limits of the respective concepts, it also yields additional spectral information in terms of mean photon energy in the region where the operating ranges of counter and integrator overlap (Fig. 4.1, c). The mean photon energy is computed by multiplying the measured average pulse size (i.e. the ratio between the measured current and the measured pulse rate) with the electron-hole-pair creation energy of the sensor material. Medical X-ray imaging applications can benefit from this information through improved contrast and through the ability to determine the hardening of the tube spectrum due to attenuation in the imaged object.
In the case of the *counting and integrating X-ray imaging* chip, each pixel contains three basic elements (Fig. 4.2): a photon counter, an integrator and a special feedback circuit which provides both signal shaping for the photon counter and signal replication for the integrator [1]. Detailed schematics of photon counter, integrator and feedback can be found in figures 4.5, 4.7 and 4.12, respectively.

4.1 Prototype ASICs

The concepts and circuits for a counting and integrating X-ray chip were explored by four prototype ASICs named Silab01A, CIX0.1, CIX0.19 and CIX0.2.

Silab01A (TSMC 0.25 µm, design: P. Fischer)

Silab01A explored the properties and feasibility of the *low swing differential current logic* (DCL). Despite the chip itself is not linked directly to the CIX activities, the characterization results [2] which were obtained in the beginning of this thesis confirmed the suitability of this logic concept for mixed signal applications such as CIX.

CIX0.1 (AMS 0.35 µm, design: I. Peric)

CIX0.1 was the first prototype chip with counting and integrating pixels. The chip contained seventeen channels with a layout area of 100 µm × 550 µm. Since the pixel cells did not have connection pads for an external X-ray sensor, the input signal was simulated with internal charge injection circuits. These circuits allowed the generation of input signals equivalent to variable photon energies, signal intensities, charge collection times, capacitive loads and and leakage currents. The characterization results were published in [3] and [4] and will only be used in this thesis for comparison to later results with CIX0.2.

CIX0.19 (AMS 0.35 µm, design: M. Koch)

This ASIC contained prototype structures of the digital counter designs intended for the second generation CIX chip (CIX0.2). Test circuits similar to Silab01A allowed a detailed analysis of the AMS 0.35 µm version of the DCL cells. Besides these logic cells, it also featured an alternative design of the integrator charge pump (*three transistor charge pump*). Characterization results are discussed in [42].

CIX0.2 (AMS 0.35 µm, design: Peric, Koch, Kraft, Harter)

CIX0.2 implemented the counting and integrating signal processing scheme in a 8x8 pixel matrix, which can be connected to an actual X-ray sensor via bump bond pads. The pixel pitch is 250 µm × 500 µm. The ASIC covers an area of 5680 µm by 4110 µm, contains about 295,000 gates and features 137 wire bond pads for external connections. Eighty of these bond pads are arranged in staggered rows at the bottom of the chip and are vital for operation. The remaining pads are optional, as they are connected to calibration circuits, allow measurement and control of the chip DAC voltages

and provide additional connection paths to the supply and ground lines. Compared to CIX0.1, the major changes in CIX0.2 are (details will be given in the following discussion):

- Pixelated layout of the CIX cells (500µm × 250µm, arranged in a 8x8 pixel matrix).
- Bump bond pads in every pixel for the connection to a direct conversion semiconductor sensor (e.g. Si, CdZnTe, CdTe).
- Redesign of the feedback circuit, including the introduction of a third feedback mode (*controlled redirection*).
- Additional charge injection circuits (*photo diode, net charge delivering capacitive chopper, external pad*).
- Threshold tuning DACs (6-bit) in every pixel.
- Redesign of the pump control logic.
- Redesign of the integrator charge pumps, introduction of a third pump type (*three-transistor charge pump*).
- Redesign of the slow control logic, now using an I^2C-interface[1].
- Redesign of the readout logic, now allowing dead-time free operation of the chip due to simultaneous readout during an ongoing measurement. LVDS[2] output signals.
- Access to the analog outputs of preamplifier and integrator in every pixel.

The characterization of the CIX0.2 prototype chip is the main focus of this work.

[1] I^2C is an acronym for the *Inter-Integrated Circuit* serial bus, a two wire bus designed by Philips Semiconductors (now NXP) for the connection of components on the same printed circuit board. Currently effective is specification 2.1 [43].

[2] *low voltage differential signaling*, ANSI/TIA/EIA-644-1995

CIX0.2 Overview

Since the remaining sections of this chapter will discuss the different elements of CIX0.2, this section is intended as a brief overview. Fig. 4.3 shows a top

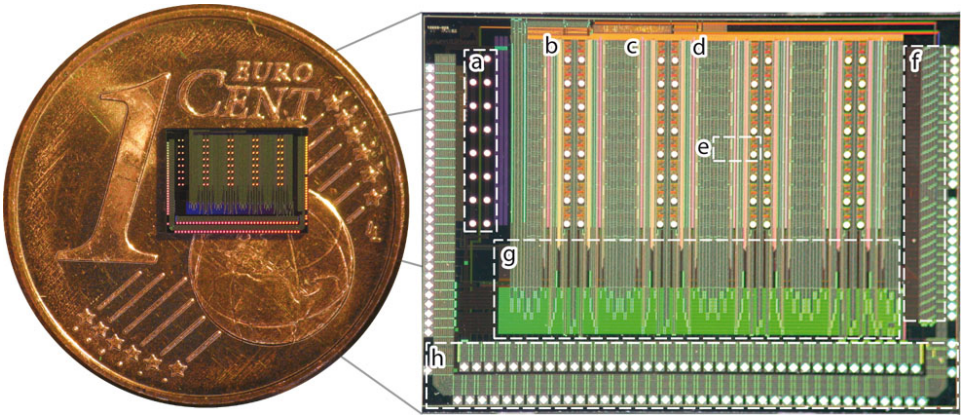

Fig. 4.3: Photographs of the CIX0.2 prototype ASIC. Structures marked in the top level overview: a) one pixel of the 8×8 pixel matrix, white dots are sensor connection pads b) chip register and I^2C interface. Readout chain: c) address sequencer, d) row select elements, e) bus receivers and LVDS output drivers. Other structures: f) 28 on-chip DACs and bias cells, g) 80 vital connection pads, h) routing matrix, i) guard ring connectors.

view of the ASIC. The main element is the 8×8 pixel matrix, of which a single pixel element is highlighted (a). The static pixel configuration is controlled via the I^2C interface and the chip register (b). All dynamic configuration signals are provided externally. Elements (c-e) mark the circuits responsible for the readout, i.e.the address sequencer (c), the row select elements (d) and the bus receiver and LVDS output driver units (e). For a detailed description refer to sect. 4.7 and appendix A.2. Biasing of the chip circuits is controlled by 28 on-chip DACs and bias cells (f). The 80 vital wire bond pads (g) are situated at the bottom of CIX0.2. Other structures visible on the photograph are the main routing matrix (h) and the bump bond pads for the connection to the sensor guard ring (i).
Fig. 4.4 shows an overview of the pixel layout. The preamplifier and feedback of the photon counter (a) are the most sensitive parts of the analog electronics and were therefore placed farthest away from the digital circuits. They will be discussed in sections 4.2 and 4.4. The charge injection circuits, which are used to simulate the sensor signal, are also situated near the input node, in area (a) and will be explained in sect. 4.5. Area (b) contains the pixel register and the 6-bit DAC for threshold tuning. The integrator and its charge pumps are found in area (c) (sect. 4.3). The pump control logic for the integrator is found in (d), together with the logic functions providing signals for the counters and latches. These are arranged in sixteen identical one-bit

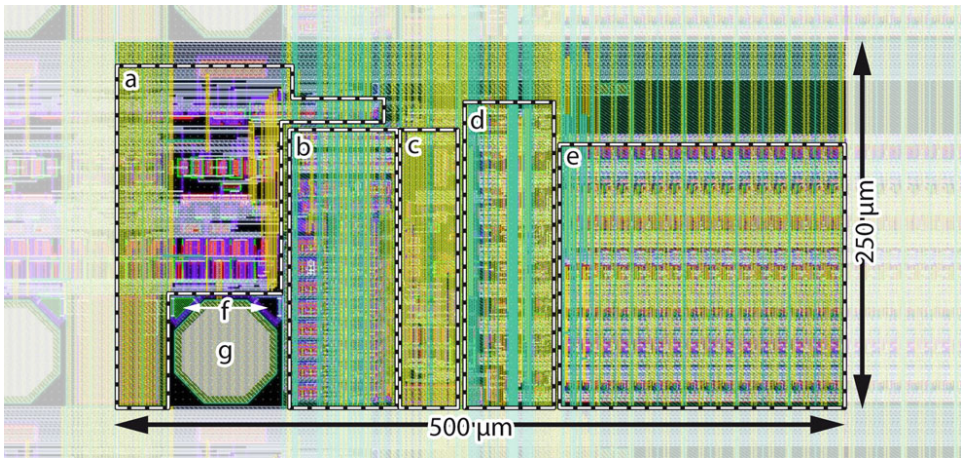

Fig. 4.4: CIX0.2 pixel cell layout. Structures marked: a) preamplifier, feedback and charge injection, b) pixel register, threshold tune DAC, c) integrator and charge pumps d) pump and control logic e) counters, latches output multiplexers and bus drivers (16-bit), f) photo diodes, g) sensor connection pad.

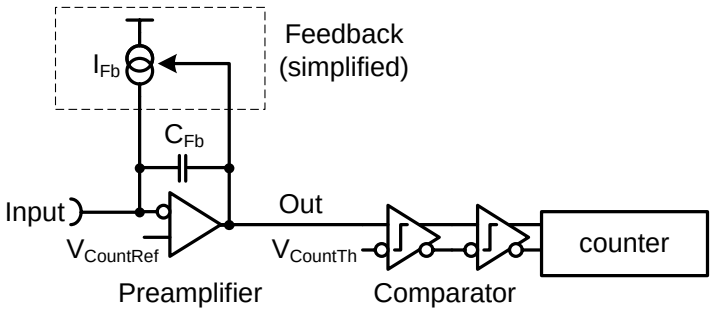

Fig. 4.5: Schematic of the photon counter. Absorption of a photon in the conversion layer causes a negative charge pulse at the input node. The electrons accumulate on the feedback capacitor C_{Fb} until they are removed by the feedback circuit (continuous reset). A two stage comparator triggers if the rise in the preamplifier output potential exceeds the threshold $V_{CountTh}$, thereby incrementing the 16-bit ripple counter.

units (e), each with the necessary counters, latches and output elements. Details of these logic circuits are discussed in A.3. In addition to this, the pixels contain two photo diodes (f) and a bump bond pad for the sensor connection (g). Every odd pixel column is mirrored, so that the sensitive analog circuits are maximumly separated from digital elements and digital to analog crosstalk is minimized.

4.2 Photon Counter

The signal processing chain of the photon counting channel (Fig. 4.5) consists of a charge sensitive amplifier (*preamplifier*) with a 10 fF feedback capacitor, a two-stage comparator with differential output and a 16-bit ripple counter. Incoming charge accumulates on the feedback capacitor until it is removed by the feedback circuit, which is basically a differential pair acting as a voltage controlled current source. This circuit provides a *continuous reset* of the amplifier. In the absence of an input signal, the output voltage of the preamplifier settles to $V_{CountBaseline}$[3]. A negative signal of charge Q on the input node raises the output voltage by ΔV (ignoring effects of finite charge collection time and ballistic deficit for now):

$$\Delta V = \frac{Q}{C_{Fb}}$$

The increased output voltage activates the feedback current source, which delivers a current I_{Fb} to the input node. This current compensates the signal charge, thereby decreasing the output voltage. Full compensation of the signal charge is achieved when the output voltage reaches $V_{CountBaseline}$, thereby also turning off the feedback current source. In this simple model, the time needed for the return to baseline t_{rtb} is given by the time the constant feedback current needs to deliver the given charge (compare Fig. 4.6, right)

$$t_{rtb} = \frac{Q}{I_{Fb}} \tag{4.1}$$

Contrary to the behavior of a CR-RC shaper, the return-to-baseline time of this feedback circuit scheme is not independent of the pulse size, but approximately proportional to it (Fig. 4.6, left). Since the differential pair in the feedback circuit delivers smaller currents when the output voltage approaches the baseline, the actual time interval is somewhat longer (see Fig. 4.17). The comparator stage switches to a logical high state while the preamplifier output exceeds the threshold voltage $V_{CountTh}$. Each positive transition triggers a single count event in the connected photon counter. If the time spacing between subsequent photons is long enough for the preamplifier output to return to its baseline ($t > t_{rtb}$), a photon is counted if its deposited energy exceeds the threshold E_{Th}:

$$E_{Th} = \frac{w_i}{e} \cdot C_{Fb} \cdot (V_{CountTh} - V_{CountBaseline}) \tag{4.2}$$

The intrinsic pair-creation energy w_i is a material property which describes the average energy necessary to produce one electron-hole-pair in the conversion layer. In $CdTe$, a typical value is $w_i = 4.64$ eV [44]. A photon of 60 keV photon will hence deposit about 2 fC. This value is thus often used as an input pulse size for the characterization.

[3] An explanation of why the baseline voltage is different from $V_{CountRef}$ requires a more detailed view of the feedback circuit, as will be given in section 4.4 (Fig. 4.12).

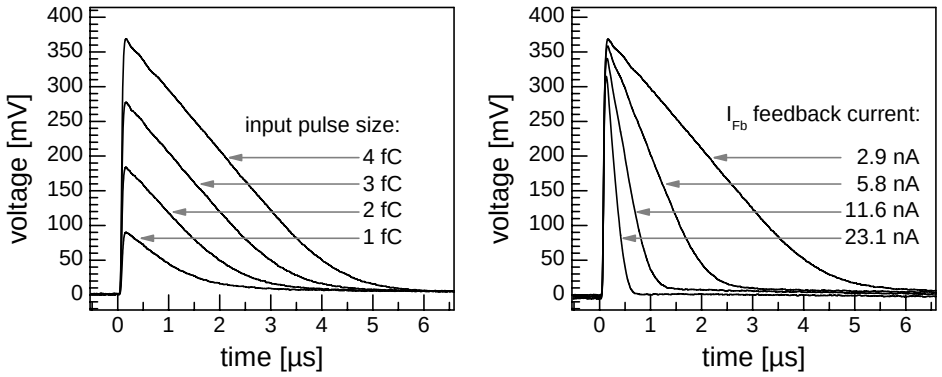

Fig. 4.6: Oscillograms of the preamplifier output response to an input pulse. Left: Response to different pulse sizes at a feedback current $I_{Fb} = 2.9$ nA. Right: Variation of the feedback current, 4 fC input pulse size.

Pileup

Large photon fluxes correspond to an increased probability for pulse spacings shorter that t_{rtb}. If this occurs, the previous signal charge is not yet fully compensated, so that the charge of the new pulse is added to the remainder of the previous. This effect is known as *pile up*. Given enough remaining charge, the new pulse can cross the energy threshold even if its corresponding energy deposit is below the nominal threshold E_{Th}. If the time interval is short enough such that the preamplifier output has not returned below the threshold voltage, there will be no transition in the comparator state. Thus, the subsequent photon is not counted, irrespective of its deposited energy. Even worse, the time until the output reaches its baseline increases by the t_{rtb} of the second photon. The chosen implementation of the photon counter is hence called a *paralyzable* photon counter.

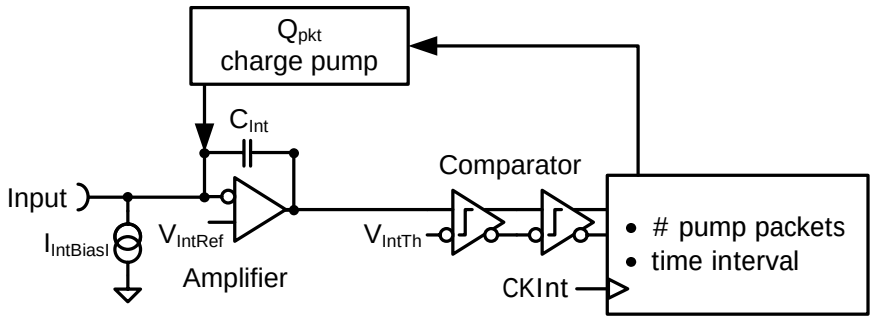

Fig. 4.7: Simplified schematic of the integrator circuit. The input signal is integrated on the C_{Int} capacitor until the amplifier output voltage exceeds a certain threshold V_{IntTh}. This triggers the clock synchronous operation of the charge pump, which removes a charge packet of defined size Q_{pkt} from the integrator input. Counters record the number of charge packets and the time interval between first and last pump event. The injection of an additional bias current $I_{IntBiasI}$ allows measuring smaller input signals.

4.3 Integrator

The integrator implementation shown in Fig. 4.7 is similar to the *sigma-delta converter* concept which is often used in high precision, low frequency measurement applications [45]. Recent results with a chip based on a similar implementation are discussed in [46]. The first stage of the integrator signal processing chain is an amplifier-comparator stage similar to the one found in the single photon counter. One difference to the photon counter is the clock-synchronized operation of the feedback circuit. It uses a charge pump to remove a charge packet of defined size Q_{pkt} from the integrator input each time the accumulated charge on the feedback capacitor exceeds a threshold given by V_{IntTh}. In a somewhat simplified sense, this type of feedback converts a continuous input current to a frequency of pump actions (see Fig. 4.8). Two counters record the number of charge packets N_{pkt} and the elapsed time Δt, which is derived from the number of clock cycles N_t between the first and the last pump action in the measurement cycle. The measurement of the current I_{Signal} is then given by:

$$I_{Signal} = \frac{N_{pkt} \cdot Q_{pkt}}{\Delta t} = \frac{N_{pkt} \cdot Q_{pkt} \cdot f_{CK}}{N_t}. \tag{4.3}$$

Here, f_{CK} is the integrator clock frequency. As will be explained below, a convenient property of this method of current measurement is that the *absolute* discretization error decreases as the input signal gets smaller, giving rise to a nearly constant relative resolution throughout the full dynamic range. Common analog to digital converters with a constant bin size do not possess this property due to the inherently large *relative* discretization errors at small values.

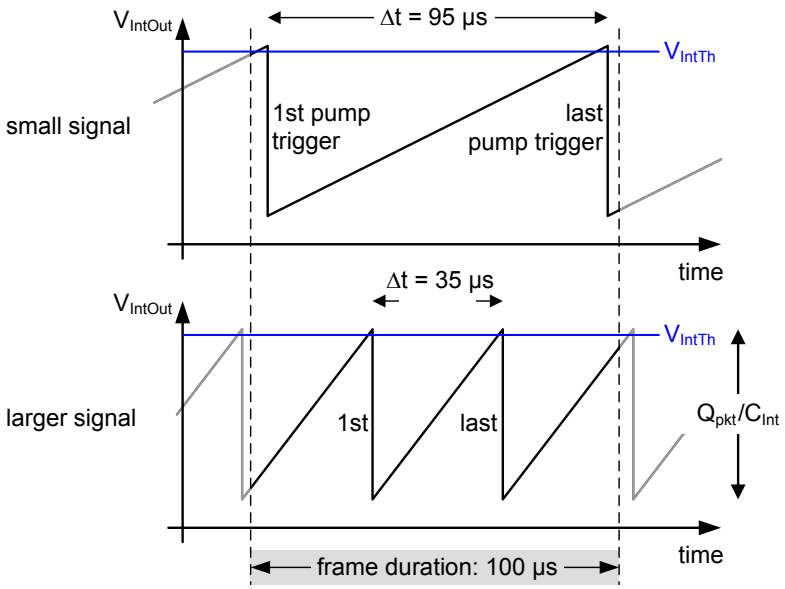

Fig. 4.8: Illustration of the integrator operation for two different input currents: The signal charge is accumulated on the integration capacitor C_{Int} until the output voltage V_{IntOut} exceeds a certain threshold V_{IntTh}. Larger input signals cause steeper inclines. The crossing of the threshold triggers a charge pump which removes a charge packet of defined size Q_{pkt} on the next clock cycle. Even though both input currents happen to produce only a single packet within the frame duration (here: 100 μs), they can be distinguished by the difference in the recorded time intervals Δt between first and last pump trigger.

Fig. 4.9 illustrates this property. It shows the relative measurement precision (i.e. the relative discretization bin size) as a function of the number of charge packets for different measurement durations at a clock frequency of 20 MHz. Since the charge on the feedback capacitor at the start of the measurement is generally not fixed, the same number of charge packets can occur at different currents. Large currents, however, will trigger the charge pump in shorter time intervals (as seen in Fig. 4.8). Hence, the simulation examined all possible N_t values at a given N_{pkt} and computed the minimal current increase that would change either value.
The dynamic range of the integrator is determined by the charge packet size, the clock frequency and the measurement duration t_{meas}. Small signals can be measured if they produce at least one charge packet (i.e. two pump events) within the measurement interval.

$$I_{min} = \frac{Q_{pkt}}{t_{meas}} \tag{4.4}$$

Smaller currents are certain to fail producing a valid measurement. However, *twice* this minimal current is needed to ensure a proper result under all

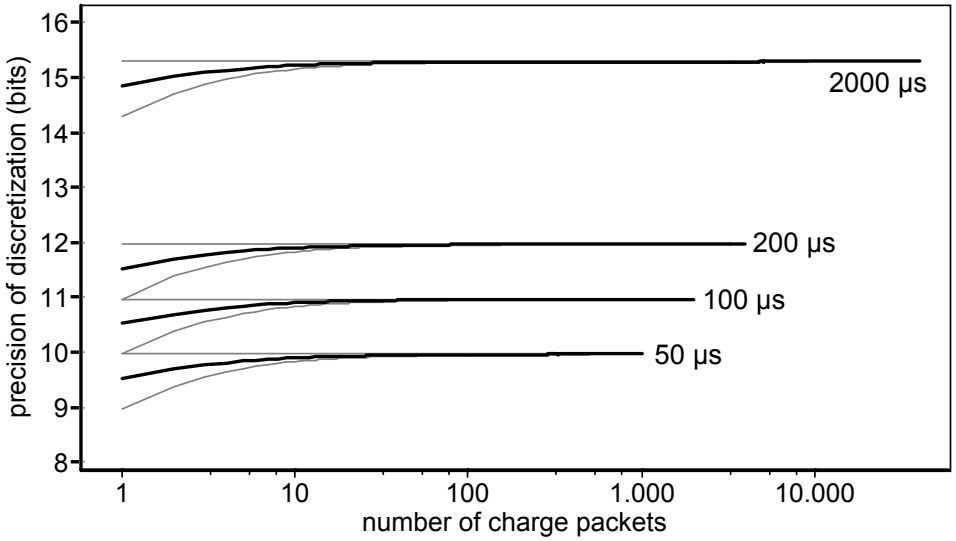

Fig. 4.9: Simulation of the expected discretization precision as a function of the signal intensity. Integrator clock rate is 20 MHz, measurement durations as noted. The precision of the integrator ist almost constant throughout the whole dynamic range. A given number of pumped charge packets can occur in a range of different input currents, depending on the initial charge on the feedback capacitor at the start of the measurement. This translates into a range of expected discretization precisions, whose minimal and maximum limits are marked by the grey lines. Black denotes the average precision.

circumstances. The reason for this is that the initial charge on the integration capacitor at the commencement of the measurement is only defined to within one pump packet. If a pump event happens shortly before the start of the measurement, I_{min} will cause only one pump event and will thus not be measured. A twice as large current, on the other hand, will cause the first event before half the measurement duration and the second event before the end, thus meeting the minimal requirements.
The largest measurable current causes a pump action on every clock cycle. It is therefore approximately the N_{max}-fold multiple of the minimal current (without bias source), with N_{max} being the number of clock cycles within the measurement interval:

$$I_{max} = \frac{t_{meas} \cdot f_{CK} \cdot Q_{pkt}}{t_{meas}} = \frac{N_{max} \cdot Q_{pkt}}{t_{meas}} = N_{max} \cdot I_{min} \tag{4.5}$$

Note that the discretization precision is determined by N_{max}, as well. At a clock rate of 20 MHz and a measurement duration of 100 μs, the discretization precision computes to :

$$\frac{1}{N_{max}} = \frac{1}{2000} = 0.0005 \mathrel{\hat{=}} 10.97 \text{ bits.} \tag{4.6}$$

This means that a current is measured with a relative precision of about 0.05%. This does not, however, imply a statement about the *accuracy* of the measurement. In this example, the dynamic range extends over approximately $\log(2000) = 3.3$ decades. The absolute values of I_{min} and I_{max} are determined by the choice of the packet size $Q_{pkt.}$. Fig. 4.9 shows the maximum packet counts and the corresponding precisions for different measurement durations. A two milliseconds long measurement yields a discretization precision of about 15.3 bits and a theoretical dynamic range covering 4.6 orders of magnitude.

Certain charge pump types (switched capacitor, three-transistor type, see 4.3.1) need to be reseted before they are ready to deliver another charge packet. This restriction limits the maximum pump rate to one packet on every second integrator clock cycle, thus reducing the maximum measurable current by one half. If however the required maximum input current is fixed, it can be met by using charge packets twice as large. This, of course, comes at the price of limiting the minimal current (without bias source).

A common means to extend the lower limit to even smaller currents is the introduction of an additional bias current $I_{IntBiasI}$. This small current is fed directly into the integrator input and is ideally just large enough to ensure two pump actions even when no additional signal current is present. Offline calibration subtracts the bias current from the integrator measurement in order to yield the correct signal current. While the first prototype chip lacked such a dedicated bias current source, it has been introduced with CIX0.2. As a result of the usage of this bias source, the minimal current is in principle only limited by the discretization precision of the bias current measurement. The electronic noise inherent to real measurements, however, becomes increasingly dominant for such small input currents. A meaningful number for the minimal measurable current can thus only be given if the desired signal-to-noise-ratio is supplied.

4.3.1 Integrator Charge Pumps

There are three different types of integrator charge pumps in CIX0.2, i.e. the*switched current source*, the *switched capacitor* and the *three-transistor-type*. All of these operate synchronous to the integrator clock and remove a charge packet of a defined size Q_{pkt} from the integrator input when triggered. Since the chip is designed for a signal consisting of electrons, the charge pumps have to deliver positive charge packets. Even though all three types are present in every pixel, only one type can be active at a given time. The choice is made chip wide and usually not changed during measurements.

Switched-current-source type

When triggered, the switched current source delivers an adjustable, constant current during the high-phase of the integrator clock. In this simple model, Q_{pkt} equals the product of half the integrator clock period and the pump current I_{Pump}. The maximum current to the integrator on the other hand is always equal to half the pump current, independent of the integrator clock rate. Unless, of course, the clock speed is chosen so low that the nominal packet size exceeds the dynamic range of the amplifier. Since it has no need for a reset between triggers, this pump type can be activated on every integrator clock cycle. The variation of pump current and clock frequency allows highly tunable packet sizes, which makes this charge pump suitable for very small signals. The absence of capacitors allows smaller footprints in the chip layout (about half the area). Main disadvantages of this type are the comparably large dispersion of current intensities and hence packet sizes between different pixels and the additional noise contribution from the current source. The dispersion seen in CIX0.2 could be improved with a dedicated, mismatch tolerant layout of the current sources (at the cost of increased layout area). During counting and integrating operation however, the noise contribution of the pump type is negligible compared to the noise introduced by the feedback circuit.

Switched-capacitor type

The circuit used in the switched capacitor charge pump is shown in Fig. 4.10. Charge is pumped from the $V_{PumpMean}$ supply to the integrator input in packets whose size is determined by the voltage difference between V_{PumpHi} and V_{PumpLo}:

$$Q_{pkt} = C_{pump} \cdot (V_{PumpHi} - V_{PumpLo}). \tag{4.7}$$

The $V_{PumpMean}$ voltage is usually matched to the integrator input (V_{IntRef}) so that the left side of the pump capacitor is always connected to the same potential, minimizing unwanted additional charge injection during the switching process. Before the pump is ready to deliver another packet, it

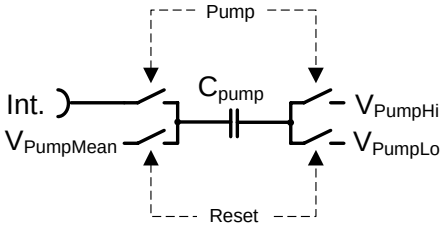

Fig. 4.10: Schematic of the capacitive charge pump. The packet size is controlled by the voltage difference between V_{PumpHi} and V_{PumpLo}. $V_{PumpMean}$ is usually adjusted to match the voltage on the integrator input (V_{IntRef}). The switches, controlled by the non-overlapping signals *Pump* and *Reset*, discharge/recharge the pump capacitor ($C_{pump} \approx 25.0$ fF).

needs to be recharged by closing the switches connected to the *Reset* signal. Enabling the *Pump* signal injects the charge packet into the integrator. Both signals are gated by the integrator clock, thus ensuring the non-overlapping operation of the switches.
The major advantages of this type of charge pump are the good reproducibility and the comparably low variation in packet sizes throughout the chip, thus providing a good anchor point for further calibration. In AMS 0.35 µm-technology, the expected dispersion of the pump capacitance is less than 0.2 percent and the temperature influence is smaller than 0.05 percent at typical lab temperatures. Less favorable properties are the need for a reset cycle between subsequent pump actions, the corresponding increase in the complexity of the control logic and the somewhat larger layout area occupied by the pump capacitor.

Three-transistor type

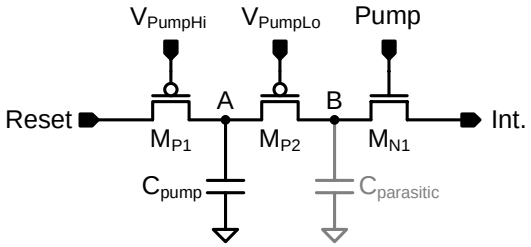

Fig. 4.11: Schematic of the three-transistor charge pump type.

The three-transistor charge pump (Fig. 4.11) is quite similar to the switched capacitor type in the sense that it is driven by the same *Pump* and *Reset* signals, and that its packet size is determined by the size of the pump capacitor

and the difference in V_{PumpHi} and V_{PumpLo}. Its principle of operation, however, is quite different and discussed in some detail in appendix A.1.

4.3.2 Integrator Logic

The integrator logic serves two main purposes: control of the charge pumps and control of the counters and time latches. The pump control must not only produce trigger signals when the threshold is exceeded, it also has to provide reset signals for the capacitive and three-transistor charge pumps if they are selected. These reset cycles must be enforced even under overload conditions, when the threshold is exceeded continuously. The counter logic manages the latch-, count- and reset signals for pump and time counter. This is complicated by two alternative operation modes for the integrator:

1. The time counter operates continuously and is only restarted from zero when a measurement series commences. TimeFirst records the time stamp of the first pump action, TimeLast latches on every pump event. If one measurement follows immediately after another, one can deduce the initial charge at the beginning of the frame. It is computed by interpolation between the TimeLast value of the previous frame and the TimeFirst value of the current frame at the time value at frame start. This allows measurements with only a single pump event per frame, provided the difference between the current in two subsequent measurements is not too severe.

2. The time counter starts from zero at the first pump event. This removes the need for the TimeFirst latch, only TimeLast needs to be read out. In this case, no information on the initial charge at frame start can be obtained. This mode has the advantages of increased readout speed, smaller layout area, circuit complexity and lower power consumption.

A logic block which provides the demanded flexibility was successfully implemented in *differential current steering logic*, which will be explained in section 4.6. A detailed description of the implementation of the control logic is not provided here, since the details are not relevant to the evaluation of the signal procession concept.

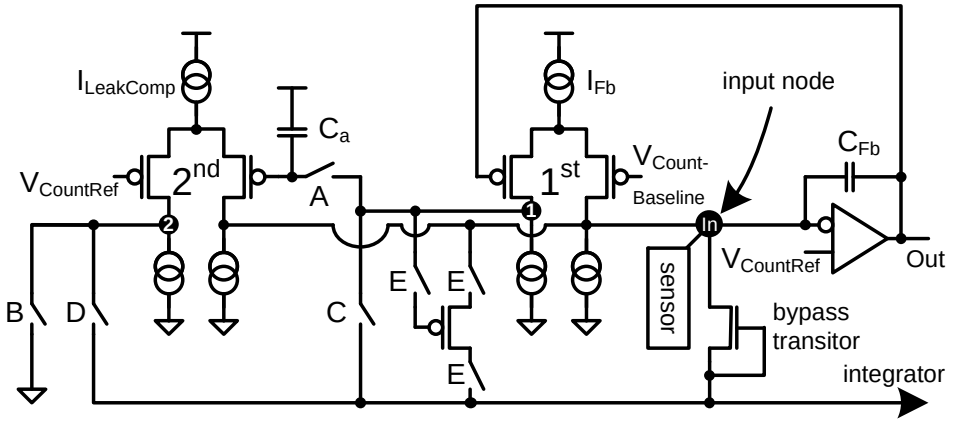

Fig. 4.12: Simplified schematic of the feedback circuit. Two differential pairs provide feedback for the charge sensitive amplifier of the photon counter (right) and signal replication to the integrator. The switches A-E are used to enable one out of four different feedback configurations. Simplified schematics of the individual configurations are given in the following discussions.

4.4 Feedback

A simplified diagram of the feedback circuit is shown in Fig. 4.12. The circuits main purposes are signal shaping for the photon counter, signal replication for the integrator and leakage current compensation. The key elements of the feedback circuit are the two differential pairs. Pair 1 provides the feedback for the photon counting amplifier and signal replication for the integrator. Pair 2 is responsible for leakage current compensation. Both differential pairs share the same basic behavior: the two current drains at the bottom of each branch drain precisely half the current entering from the current source above. If the gate potentials of both PMOS transistors match, the pair is balanced and no current will flow into or out of the nodes between the transistors and the current drains. A mismatch between the gate voltages, however, shifts the current from one branch into the other, causing some additional current in one branch and missing current in the other. This additional/missing current must leave/enter the branch through the node above the respective current drain.

4.4.1 Feedback and Signal Duplication

The operation of the feedback circuit can be understood by following the chain of events caused by a negative charge pulse Q arriving at the input node (In, Fig. 4.12) from the sensor. Let us assume that both differential pairs are balanced in the beginning. This implies that the preamplifier output voltage (Out) equals $V_{CountBaseline}$ and there is no current entering or leaving through the nodes above the current drains. Upon arrival of the

signal charge Q, the amplifier output voltage increases by Q/C_{Fb}, because the input node is connected to the inverting input of the amplifier so that its voltage remains constant (equal to $V_{CountRef}$). This voltage increase is seen on the left branch of the first differential pair and shifts some feedback current from the left branch into the right. The additional current in the right branch flows into the input node, thereby canceling the original charge pulse. During the cancelation process, the output voltage of the amplifier decreases until it reaches $V_{CountBaseline}$. At this point, the first differential pair is balanced again and no further current flows into the input node. This is how the first differential pair provides the feedback (*continuous reset*) for the photon counting amplifier.

Note that the imbalance in the differential pair causes not only a current flowing out of the right branch into the amplifier input node, but also an identical current *entering* the left branch from node 1. The integral over both current pulses is identical in size (both matching the original input pulse), but of opposite sign. Hence, if the integrator is connected to node 1 (switch C closed), it receives a charge pulse of equal size and sign as the input pulse. This is how the first differential pair provides signal duplication.

Between the input nodes of the preamplifier and the integrator, there is also a diode connected NMOS transistor (*bypass*), seen in the bottom right of Fig. 4.12. This transistor becomes conductive if the input node potential drops more than a threshold voltage below the integrator input voltage (about 1.2 V) - a situation which can occur only if the sensor signal becomes too large to be compensated by the feedback current. Hence any current exceeding the limits of the feedback bypasses the feedback via the diode connected transistor, allowing the integrator a proper measurement of the input signal.

4.4.2 Static Leakage Current Compensation

Biased semiconductor sensors usually exhibit some degree of leakage current flowing into the readout electronics even when no real signal is present. This current can cause shifts in the output voltage baseline of the amplifier and decrease the dynamic range. It is therefore desirable to compensate the leakage current *prior* to the signal processing. In our feedback design, this is done by the second differential pair (Fig. 4.13). Note that the right output node of this pair is connected to the preamplifier input node. The current delivered to the input node corresponds to an imbalance in the second pair. The magnitude of this current is determined by the voltage on the *sampling capacitor* C_a. Since switch A is open, the voltage will remain constant, thereby freezing the current to the input node to a constant value (which is the reason why this mode is called *static* leakage current compensation). During a separate sampling phase, this voltage is adjusted so that the current

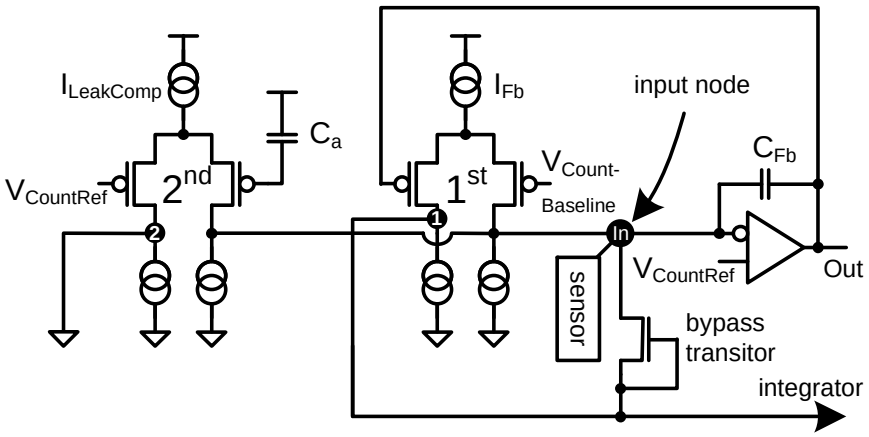

Fig. 4.13: Simplified schematic of the feedback circuit in static leakage current compensation mode. The first differential pair provides feedback for the photon counting amplifier and signal duplication for the integrator, the second pair delivers a static current, thereby compensating the sensor leakage current. Static l.c. switch configuration (compare Fig. 4.12):
A open, B closed, C closed, D open, E open.

compensates the leakage current. In this configuration, all current in the left branch of the second differential pair is simply drained to ground.

4.4.3 Sampling

The sampling of the feedback current is performed in the absence of real signals, when there is only leakage current flowing to the sensor (Fig. 4.14). Closing the sampling switch A and disconnecting the integrator leaves node 1 connected only to the right gate of the second differential pair and the sampling capacitor C_a. There can thus be no DC current flowing into or out of the first differential pair. This implies that the leakage current can only be compensated by the current from the right branch of the second differential pair (which is connected to the input node). Through this mechanism, sampling adjusts the voltage on C_a until the leakage current is matched by the current leaving the right output node of the second differential pair. The current on the left branch of the second differential pair (node 2) is again ignored and simply drained to ground.
For illustration purposes, one can follow the chain of events triggered by a sudden increase in the sensor leakage current. At first, this increase would be compensated by the first differential pair, shifting current from the left branch to the right. This current decreases the potential on the sampling capacitor C_a. As a result, the second pair delivers more current to the input node. The first pair reacts by delivering slightly less current. This slows down the voltage decrease on C_a until it reaches an equilibrium. At that

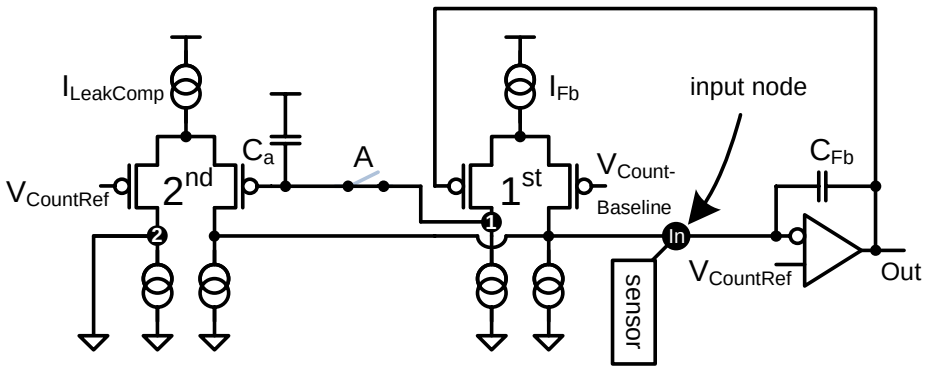

Fig. 4.14: Simplified schematic of the feedback circuit during leakage current sampling. When engaged in the absence of a real signal, this mode adjusts the voltage on C_a while the sampling switch A is closed until the compensation current (from the second differential pair) matches the leakage current to the input node. Sampling phase switch configuration:
A closed, B closed, C open, D open, E open.

point, the first differential pair is balanced again and the second pair has adjusted to the new leakage current following the adjustment of the voltage on C_a. Once stable conditions are reached, the sampling switch A can be opened, thus storing the voltage on the sampling capacitor and consequently settings the compensation current delivered to the input node to a constant value. For stability reasons, I_{Fb} is much smaller than $I_{LeakComp}$ and the sampling capacitor C_a is large compared to C_{Fb}. The first differential pair reacts quickly but with limited current, while the second pair reacts slower but can handle significantly larger currents. If the integrator is reconnected to node 1, there will be no current flow to the integrator unless a signal arrives at the input node. Since the leakage current is already compensated at the input node, there will also be no baseline shift in the amplifier output. Note that the design of switch A requires special attention, because any current leaking through that switch and any charge injection during switching will corrupt the current delivered to the input node. Unfortunately however, the design precautions taken in CIX0.2 turned out to be insufficient for long term measurements without regular sampling intervals.

4.4.4 Continuous Leakage Current Compensation

This feedback mode differs from the previously discussed *static* leakage current compensation in that it adjusts the compensation current of the second differential pair *continuously* to the incoming DC current - regardless of whether it is actual leakage current or signal current. The motivation for the continuous leakage current compensation lies in the behavior of the photon counter for very large signals: Large photon flux causes pile-up of

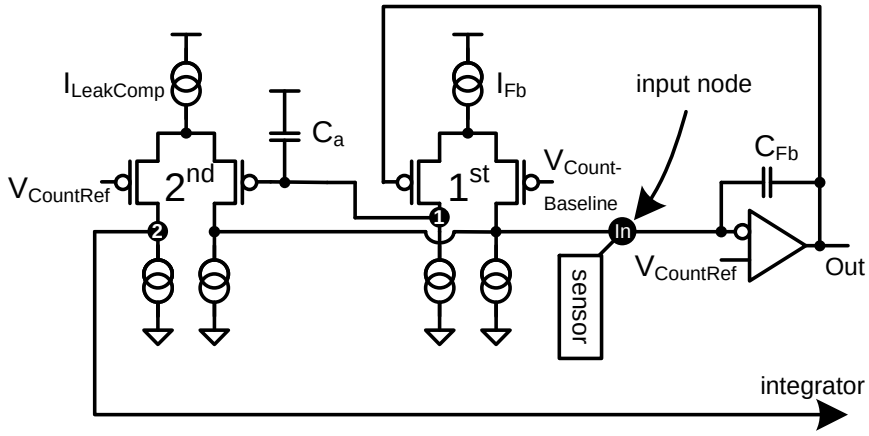

Fig. 4.15: Simplified schematic of the feedback circuit in continuous leakage compensation mode. The first pair reacts quickly to the input signal, but delivers no net current. The DC component is removed by the (slowly responding) second differential pair, which also delivers a low-pass filtered copy of the input signal to the integrator. Continuous leakage current compensation switch configuration:
A closed, B open, C open, D closed, E open.

subsequent events, leading to a quick breakdown of the count efficiency. Additionally, the effective threshold voltage shifts since even smaller pulses can cross the threshold while the previous pulse is not yet fully compensated. Continuous leakage current compensation allows operation of the photon counter at significantly higher fluxes at the expense of a baseline shift in the high signal regime. The basic idea is to use the strong second differential pair to keep the preamplifier within operation limits at all times by removing the DC component of the input signal. Since the second differential pair is slow, the effect of this is only noticeable at high pulse rates.
From a schematic point of view, the continuous leakage compensation mode is very similar to the sampling configuration. The only difference lies in the current leaving node 2. In sampling mode, it is simply discarded to ground via the closed switch B (Fig. 4.12). In the continuous leakage compensation mode, however, it is fed to the integrator through switch D. The resulting schematic is shown in Fig. 4.15. Using the same line of argument as above, the current leaving node 2 has to be equal in size and sign to the current entering the input node from the sensor. Differential pair one does not deliver any net current, because its left output (node 1) is connected to capacitive loads only. All input current must hence be compensated via the right output of the second pair - thereby producing a mirrored signal on the left output for the integrator. While the net charge of the input signal is in principle replicated exactly, its temporal behavior is not. The reason is that the imbalance of the second differential pair is controlled by the gate voltage of

the right PMOS transistor, which is connected to the sampling capacitor C_a. The large size of this capacitor causes a long response time constant, thereby imposing a noticeable low-pass filter on the signal fed to the integrator. This behavior is considered not to be an issue for the integrator measurement, since the integration interval is usually much longer than this time constant. Note that the signal delivered to the integrator consists of both signal current and leakage current. The term *continuous leakage compensation* therefore only refers to the input of the photon counting amplifier, not to the integrator. This is opposed to the case of static leakage compensation, where the leakage current is compensated in both photon counter and integrator. An additional contribution to the integrator input current arises from threshold voltage mismatches of the transistors used for the current drains in the branches of the differential pairs. The size (and sign) of this contribution varies from pixel to pixel and scales with the general bias current ($I_{LeakComp}$) flowing through the differential pair. Since the output nodes of the differential pair are connected to the inputs of integrator and photon counter, respectively, $V_{CountRef}$ and V_{IntRef} (the integrator input potential, see Fig. 4.7) should generally be chosen equal. Otherwise, the different drain-source voltages of the current drains would introduce an additional offset. All remaining non-signal contributions in the integrator can be taken care of using a second offset compensation circuit in the integrator. Similar to the function of the second pair in case of the static leakage compensation mode, any input current to the integrator can be sampled and subsequently removed.

4.4.5 Controlled Redirection

The controlled redirection feedback mode differs from the two other modes by not using any of the differential pairs to compensate the input current signal. In fact, the second differential pair is not used at all. Instead, a PMOS transistor $\mathrm{P_X}$ of dynamically controlled resistivity is used to redirect the sensor current from the photon counter input directly to the integrator. Since both leakage and signal current are redirected, this mode does not suffer from the saturation of the feedback circuit at large input signals as seen in the static leakage compensation mode. Instead, it behaves quite similar to the continuous leakage compensation mode, introducing an input current dependent baseline shift in the amplifier output voltage. The main benefit of this configuration compared to the continuous leakage compensation mode is the avoidance of the large sampling capacitor C_a and the second differential pair, thereby reducing power consumption, circuit complexity, noise sources and layout area.
The basic principle of operation of this feedback scheme can be explained by following the circuits response to a change in the input signal. Lets assume the system starts off in a balanced state, so that the gate potential on $\mathrm{P_X}$ is in equilibrium and allows all incoming (leakage) current to pass to the

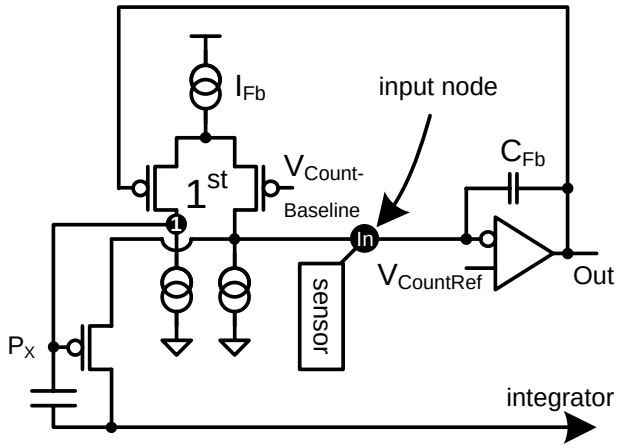

Fig. 4.16: Simplified schematic of the feedback circuit in controlled redirection mode. Differential pair 1 does not deliver any net current. Instead, it controls the gate voltage of the transistor P_X redirecting the signal current to the integrator. Controlled redirection switch configuration:
A open, B closed, C open, D open, E closed.

integrator. A negative charge pulse arriving on the input node will, again, cause an increase in the preamplifier output voltage. This voltage increase shifts some current in the differential pair from the left branch to the right branch, thereby delivering (positive) charge to the input node and negative charge to gate of the redirection transistor. Both charges help to compensate the original charge pulse. The positive charge cancels some of the input signal directly whereas the negative charge lowers the gate potential, thus redirecting more input current to the integrator. This negative feedback compensates the charge pulse. At some point, the preamplifier output will reach its baseline voltage, resulting in a balanced state in the differential pair. But the compensation does not stop yet, because net charge has been delivered to the gate of P_X. Instead, the redirection transistor allows a maximum current flow between integrator and input node, inevitably leading to an undershoot (Fig. 4.17, bottom left). Through the same feedback mechanism as discussed above, this leads to an imbalance of opposite sign in the differential pair and thus to an increasing gate potential.
The feedback response ends when the net charge delivered by the differential pair amounts to zero so that the initial gate voltage on P_X is restored. Such an equilibrium can only be reached if the time constants in the feedback circuit have to be chosen properly so that oscillations in the output voltage are avoided. As explained in [1], there are two time constants involved: the response time of the differential pair (determined by C_{Fb} and the transconductance of the differential pair) and the response time of the redirection transistor (controlled by the gate capacitance and transconductance of P_X). Oscillations are avoided if the second time constant is much larger than the

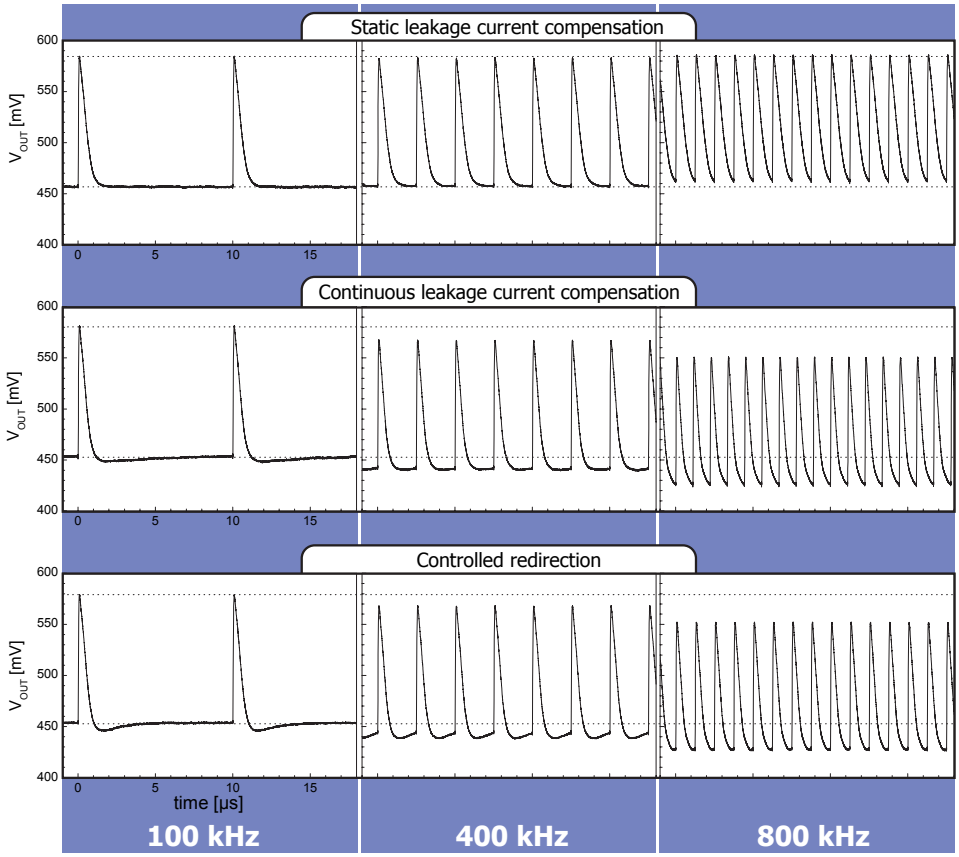

Fig. 4.17: Oscillograms comparing the signal shaping properties of the different feedback configurations. Waveforms at the preamplifier output for pulse streams (2.3 fC) of different frequencies (left: 100 kHz, center: 400 kHz, right: 800 kHz). Static leakage current compensation does not exhibit a baseline shift whereas both other configurations do (dashed lines mark the original peak and base lines). In the 800 kHz waveform, the signal does not fully return to the baseline because of a slight pileup of subsequent pulses.

first. This condition can be met by choosing a large enough gate capacitance of P_X and a small enough current in the differential pair (I_{Fb}). This is the reason for the additional MOS capacitor on the gate of the redirection transistor. Note that the transconductance of P_X depends on its drain-source current, namely the current flowing between input node and integrator. Large signal- or leakage currents can thus influence the settling behavior of the feedback response. Typical leakage currents less than a few nA do, however, not pose a problem.

property	static L.C.	continuous L.C.	contr. redir.
integrator connection	1st diff. pair	2nd diff. pair	via P_X
leakage reaches integrator	no	yes	yes
second diff. pair	static	dynamic	obsolete
baseline shift	no	yes	yes
overload count rate loss	abrupt	gradually	gradually
bypass diode used	yes	no	no
sampling phase necessary	yes	no	no
feedback undershoot	no	yes	yes

Tab. 4.1: Comparison of the CIX feedback modes. L.C. = leakage current compensation.

4.4.6 Comparison of the Feedback Modes

The waveforms in Fig. 4.17 show the signal at the output of the charge sensitive amplifier, measured using an analog buffer situated on the chip. Fast continuous streams of charge pulses (Q = 2.3 fC) have been injected into the input of the amplifier using a fast switched current source. In the top row oscillograms, the feedback circuit was configured to provide static leakage compensation. Increasing signal frequencies (from left to right) illustrate the feedback behavior at larger signal currents. Static leakage compensation does not have a shift in the baseline, the pulse maxima remain at the same voltage, independent of the pulse frequency (dashed lines). At 800 kHz, however, a slight pile up of subsequent pulses occurs, so that the signal does not reach the baseline voltage in between. As seen on the left side, the typical pulse shape at the preamplifier output has a triangular shape without any undershoot. This form corresponds to the feedback operating as a constant current source at output voltages larger than 10-20 mV above the baseline. The nonlinear feedback behavior below that voltage is also the reason why the minor pileup visible in the top right graph does not add up quickly so that the amplifier saturates. Remaining charge from the previous pulse causes a slightly higher than normal peak voltage in the subsequent pulse and the pulse retains this elevated voltage throughout the shaping process. This results in a less throttled feedback current when the output voltage would have normally become too low. A small amount of remaining charge will thus cause a slight decrease in shaping time, thereby postponing the point of saturating pileup.
Continuous leakage compensation removes the mean DC component of the signal current right at the input node. As seen in the middle row, this leads to a baseline shift that increases with signal intensity. The benefit of the baseline shift is that signal fluxes which cause severe pileups can be measured by the photon counter. This increase in maximum count rate is paid for by

the loss of a proper energy discrimination, since a lower base line voltage translates into to a higher charge on the feedback capacitor that is necessary to cross the discriminator threshold voltage. Note however, that the energy discrimination under such conditions is far from being perfect even if no baseline shift occurs. In an actual measurement with a X-ray source, the incoming photon pulses have Poisson-distributed spacing. This statistics leads not only to a large probability of charge remaining on the feedback capacitor when a new photon arrives, it also causes a large uncertainty in the amount of remaining charge. Since the effective threshold voltage is only as well defined as the voltage from which the pulses start, the problem of ill-defined energy discrimination remains. The presence of a baseline shift at large signal intensities is thus not a strong argument against continuous leakage current compensation. This line of arguments also applies to the controlled redirection mode, which behaves quite similar to the continuous leakage current compensation mode, as can be seen in the bottom row.

4.4.7 Integrator Offset Correction

The integrator features an additional compensation circuit for the correction of offset currents originating in the feedback circuit. It also provides leakage current compensation for the integrator when the feedback circuit is operated in continuous leakage current compensation mode or controlled redirection mode. As can be seen in Fig. 4.18, the circuit schematic is almost identical to the second differential pair in the feedback circuit (Fig. 4.14). The difference

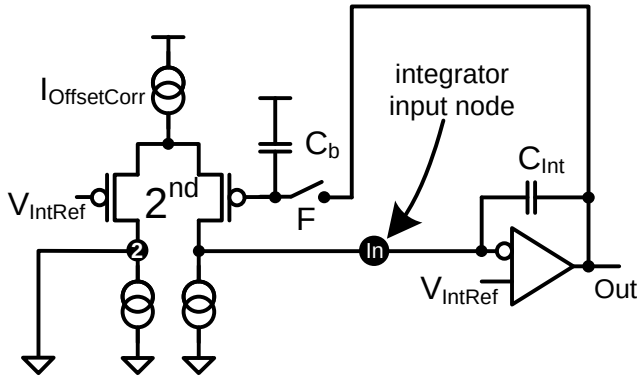

Fig. 4.18: Simplified schematic of the integrator offset correction circuit.

to the feedback circuit lies in the connection of the sampling capacitor C_b, which in this case is connected to the amplifier output of the integrator. Switch F serves the same purpose as switch A in the feedback schematics. It is used to sample the (offset) current entering the integrator input node. While F is closed, the voltage on the sampling capacitor C_b is adjusted until the current delivered by the differential pair matches the input current. Once

stable conditions are reached, switch F can be disconnected, thereby storing the voltage on the sampling capacitor. A subsequent measurement with the integrator will only record the additional (signal) current whereas the sampled offset current is compensated at the integrator input node.
While this circuit basically works as intended, there is unfortunately a design flaw which prevents the usage of this circuit in combination with the injection of an integrator bias current through the $I_{IntBiasI}$ source (Fig. 4.7). Since this current source does not possess a switch to disconnect it from the integrator input during the sampling phase, its current is also compensated by the offset correction circuit (thus voiding the intended effect of the bias current). Such a switch, connected to the complement of the signal controlling switch F, should hence be introduced in subsequent chip iterations.

4.5 Charge Injection and Signal Generation

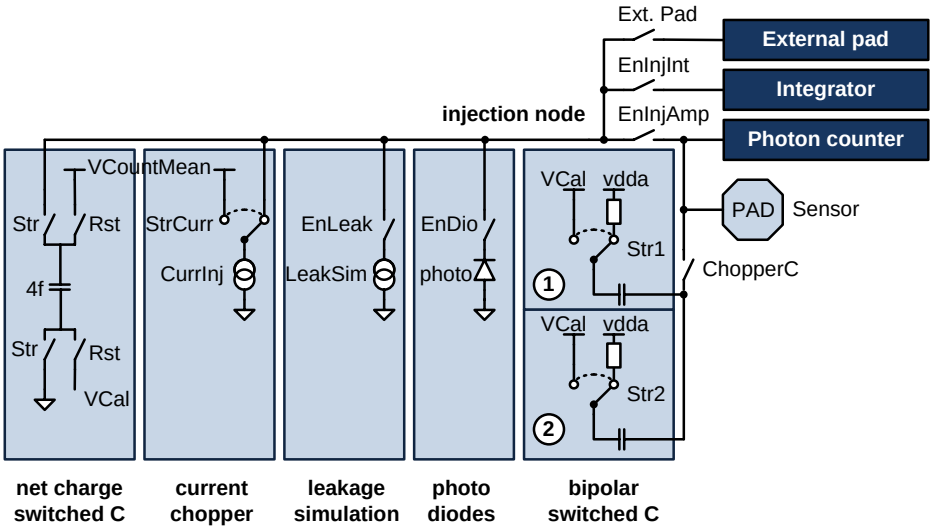

Fig. 4.19: Schematic of the charge injection circuits. The sensor pad and the two bipolar capacitive choppers are connected directly to the preamplifier input. All other, net charge delivering, injection circuits are connected to the injection node, which can be routed to the photon counter or directly to the integrator. There is also the possibility to connect the external pad. Switch states are non-exclusive and defined in the pixel register.

The characterization results discussed in this thesis were obtained without an actual imaging sensor connected to the pixel input pads. Instead, all signals were produced by the internal charge injection circuits, illustrated in Fig. 4.19. Two switched-capacitor chopper circuits are connected to the preamplifier input via the *ChopperC* switch. Since the delay between the strobe signals *Str1* and *Str2* can be chosen arbitrarily small, these choppers

allow measurement of the photon counter's double pulse resolution. Their second application is the tuning procedure of the photon counter thresholds. Despite their charge pulses being inherently bipolar with a resulting integral of zero, the choice of the strobe signals allows an arbitrary delay between positive and negative flank. Due to the strong difference in the time constants of injection phase (fast) and recharge phase (slow), their maximum frequency is limited to about 10-50 kHz.
All net charge delivering injection circuits are connected to the *injection node*. The *net charge delivering switched capacitor* uses the same circuit as the capacitive charge pump, even though with a much smaller injection capacitance of only $4fF$ compared to $25fF$. Like its twin in the integrator, it needs a reset phase before another charge pulse can be produced. The *switched current source* is the injection circuit most commonly employed in the characterization of CIX0.2. It is very flexible with respect to the possible pulse sizes (controlled by the *ICurrInj* bias DAC and the *StrCurr* pulse duration) and can cope with small pulse spacings. A drawback, however, is the high dispersion between currents delivered in the different pixels. The *leakage simulation current source* does not only serve the obvious purpose of simulating leakage current, due to the large current range covered by the *ILeakSim* bias DAC, it can also be used to characterize the saturation currents of preamplifier and feedback circuit and their overload behavior. In addition to the injection circuits mentioned above, each pixel features two photo diodes. These deliver a current caused by electron-hole-pairs created by visible light absorbed in the depletion region of the p-n junction. One photo diode consists of a n-well to p-bulk diode, the other one has a second depletion region caused by an additional p+ implantation within the n-well. With pulses from an external laser, the photo diodes allow charge injection without the need for external strobe signals. In CIX0.1, these strobe signals were found to induce a noticeable signal in the analog electronics even if the injection circuits were deactivated. To reduces this issue, all strobe signals in CIX0.2 were routed as differential signals. Full voltage swings are unfortunately still required to achieve the switching speeds desirable for the chopper circuits.
Three non-exclusive switches (*EnInjAmp, EnInjInt, Ext.Pad*) allow connection of the injection node to the photon counter input, to the integrator (directly, bypassing feedback), or to an external connection pad. All switch configurations are stored in each pixel register so that a very high flexibility is achieved. A somewhat extreme example illustrating the extent of this flexibility might be a configuration in which all sensor pads are connected to a single integrator. Typically, however, all pixels share an identical configuration and are not interconnected.

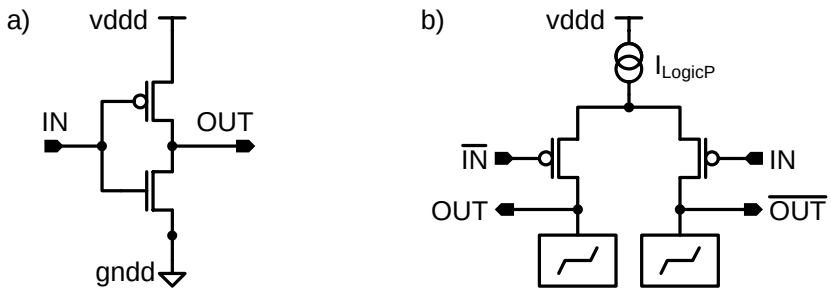

Fig. 4.20: Inverter gate schematics: a) standard CMOS logic implementation, b) differential current steering logic (DCL). The symbols in the bottom of the right schematic denote the load circuits (see Fig. 4.21). Vddd and gndd refer to the digital supply and ground rails.

4.6 Differential Current Steering Logic

Digital circuitry on a chip can be implemented with a choice of design schemes, so called logic families. *Complementary Metal-Oxide-Semiconductor* (CMOS) logic is the most common concept. This family owes its name to the use of complementary pairs of p-type and n-type MOSFETs for the logic functions. A typical example of a CMOS inverter gate is shown in Fig. 4.20 a). CMOS logic has a number of advantages, such as relatively simple and space efficient circuit design, high noise immunity and a very low static power drain (at least in technologies with feature sizes larger than 180 nm, where gate leakage currents are still negligible). Ideally, a CMOS logic cell will only consume any significant power while switching from one logic state to the other.
From a designer's point of view, another important aspect is the availability of proven design libraries containing all important logic elements. These do not only simplify the implementation of digital circuits significantly, they are also a key prerequisite for the use of design synthesis tools. Despite these strong arguments in favor of CMOS logic, there is also the major drawback of large crosstalk between digital and analog circuits in mixed signal applications. This crosstalk occurs when digital elements switch between their logical states. There are two main contributions: inter-signal crosstalk and crosstalk via the power supplies. Digital and analog signals are coupled not only through the capacitance and inductance between adjacent wires, but also via their capacitance and resistivity with respect to the chip substrate. The fluctuations induced in a certain node by the voltage swing on nearby digital signal wires are proportional to the amplitude and slew rate. In CMOS logic, switching involves not only large and fast voltage changes on the signal lines, but also a sudden increase in power consumption. Due to the resistivity and inductance of the supply lines, the sudden increase in power consumption translates into a local drop in the power supply voltage and a rise in the local ground potential (*ground bounce*). These effects are

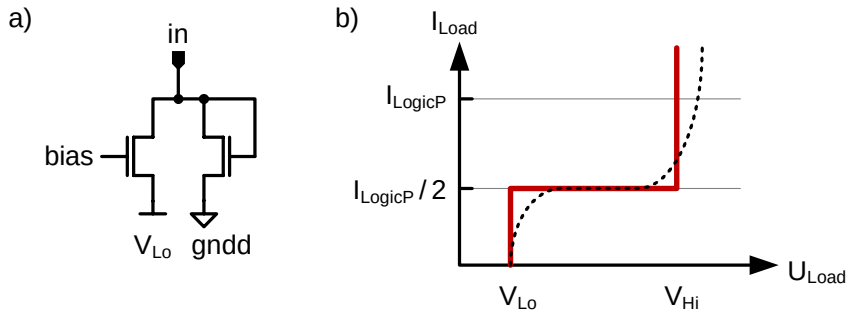

Fig. 4.21: a) The load circuit is formed by parallel connection of a diode-connected NMOS transistor and a NMOS transistor operated as a current source to the V_{Lo} supply voltage. The bias voltage is chosen to produce a current of $I_{LogicP}/2$. b) Illustration of the resulting characteristics of this load circuit (dashed line) in comparison to the behavior of an 'ideal' load circuit. See Fig. 4.22 for actual measurements.

usually counteracted with local capacitors decoupling the supply voltage, by providing low impedance supply and ground nets and by using separate power supplies for digital and analog circuitry. Other common countermeasures are:

- Shielding of the digital (or analog) lines with low impedance metal barriers (*guard traces*) and n-well implantations with externally controlled potential underneath the signal lines.
- Enclosure of sensitive and noisy circuits in diffusion barriers (*guard rings*) implanted into the chip surface.
- Maximum spacial separation of analog and digital circuits/wires.
- Minimal length of parallel routing of digital and analog signals.
- Reduction of the switching slew rate at the cost of achievable speed.

While these measures help to reduce the digital crosstalk, their application in a pixel cell is restricted by the pixel area and the number of metal layers available for local routing. The densely interwoven structure of digital and analog circuits in a CIX pixel also limits the possible degree of separation. It is thus desirable to reduce the amount of switching noise right at its origin. The *low-swing differential current steering logic* (DCL) [47] [48] approaches this problem with differential logic gates operated at a constant bias current I_{LogicP} [2]. Fig. 4.20 b) shows the topology of such a logic gate. A constant bias current is steered with a differential switching network into load circuits that transform the current into a voltage. The voltage levels must be suited to drive other, identical, logic stages. The benefits of this approach are

small crosscoupling due to small swings, cancelation of injections due to the differential nature of the logic and the absence of voltage spikes on the supply voltage even during signal transients. There are however also a number of drawbacks, namely the static power consumption, the increased number of transistors and necessary IO-pads and the increase in layout area and routing complexity. As discussed in [2], these disadvantages turn out not to be severe at least in applications which require high switching speeds, radiation hard layout or complex logic functions .
The key element which distinguishes this approach from others like [47] and [48] is the design of the load circuit (Fig. 4.21). It consists of a parallel connection of two NMOS transistors. One is operated in saturation as a current source to the supply voltage V_{Lo}. Drain and Gate of the second transistor are connected (*diode-connected*), resulting in a steep I-V characteristic. This allows the adjustment of the switching speed through the bias current, since the voltage swing depends only weakly on the bias current (proportional to the square root). Furthermore, the bias current can be adjusted for individual groups of cells, allowing a stronger bias current in cells which need a higher switching speed (e.g. the least significant bits in a ripple counter). The offset produced by V_{Lo} controls the logical low-level. Even though the logic elements were designed for a V_{Lo} value of 200 mV, tests on the prototype chip showed that lower voltages provide a better stability. V_{Lo} was therefore usually set to 0 V. The resulting characteristics for these two choices of V_{Lo} and four different bias currents is shown in Fig. 4.22.
This load implementation mimics the behavior of an 'ideal' load circuit. In order to obtain well defined voltage levels, the load circuit must sink a very large current as soon as the output reaches the high level (0.7 V in Fig. 4.22). Below the low voltage level, the current must fall to zero. An ideal circuit should also ensure that both signal edges have an identical slew rate so that both output signals are truly complimentary. The load circuit should therefore drain a constant current of $I_{LogicN} = I_{LogicP}/2$ so that the current available for charging up/down the capacitive load on the output equals $\pm I_{LogicP}/2$. This can be achieved with a bias cell which provides the appropriate translation ratios for both the PMOS current source and the NMOS current drains in the load circuits. In the CIX0.2 implementation, however, we provided two separate Bias-DACs (I_{LogicP} and I_{LogicN}) so that the currents can be chosen independently. Simulations suggested that the switching speed increases if I_{LogicN} is chosen slightly larger than $I_{LogicP}/2$. Furthermore, measurements on the prototype confirmed that this can also enhance the reliability of switching.
An interesting consequence of the usage of differential signals is the reduction of the number of unique elementary logic elements. For example, the inverter gate shown in 4.20 turns into a buffer element if the input polarities are swapped. Similarly, there are only two elements with two input signals: AND (equals NAND, OR, NOR) and XOR.

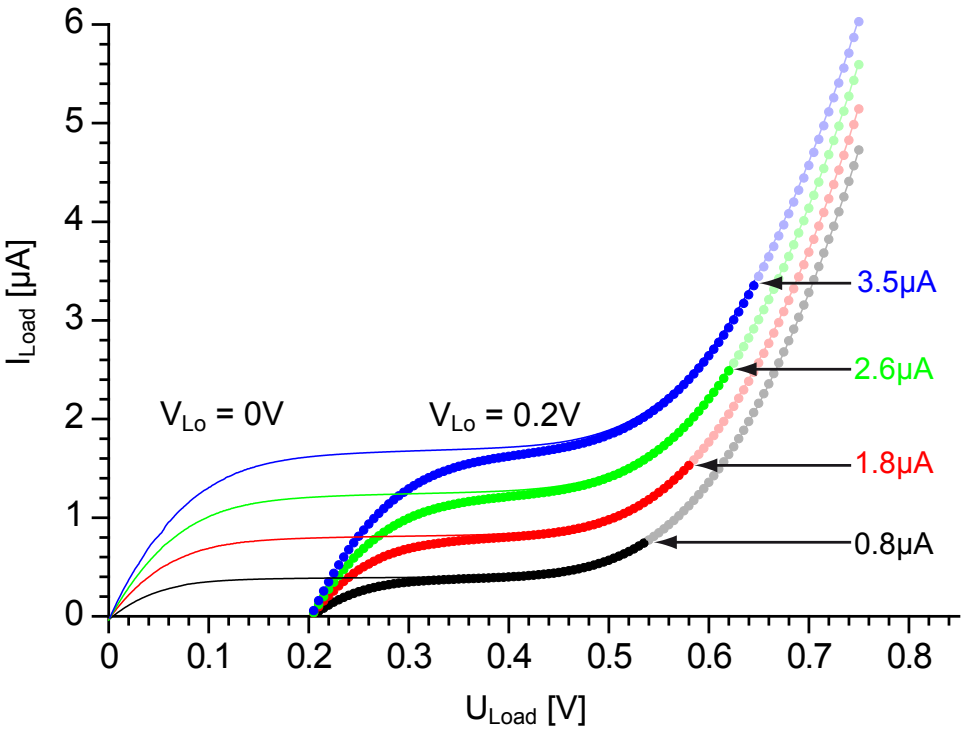

Fig. 4.22: The characteristic of the load circuit is a superposition of the characteristics of the diode-connected NMOS transistor and a NMOS transistor operated as a current source. Shown are the measured characteristics for different bias currents at $V_{Lo} = 0\ V$ and $V_{Lo} = 0.2\ V$. Measurements not reached during normal operation are grayed out. Graph adapted from [42].

4.7 Digital Readout Scheme

In medical imaging applications, the patient dose has to be kept to an absolute minimum. It is thus necessary to transfer the measurement data while the next measurement is underway. This is made possible by saving all measurement results to four *readout latches* at the end of a measurement. Since the readout process must not interfere with the measurement process, special care must be taken to minimize the digital to analog crosstalk of all circuits involved. Applications in computed tomography demand short frame durations in order to achieve high frame rates up to 10.000 images per second. On the other hand the imaging system should also be able to conduct measurements with comparably long frame durations without counter overflow. It is thus desirable to be able to match the bit depth to which the counters are read out to the measurement duration, thereby keeping the data volume to the necessary minimum. For a CIX chip, it might be desirable to read out only a subset of data, such as the photon counter or

the integrator. The readout system implemented in CIX0.2 satisfies all these demands. The basic scheme is shown in Fig. 4.23. The address sequencer

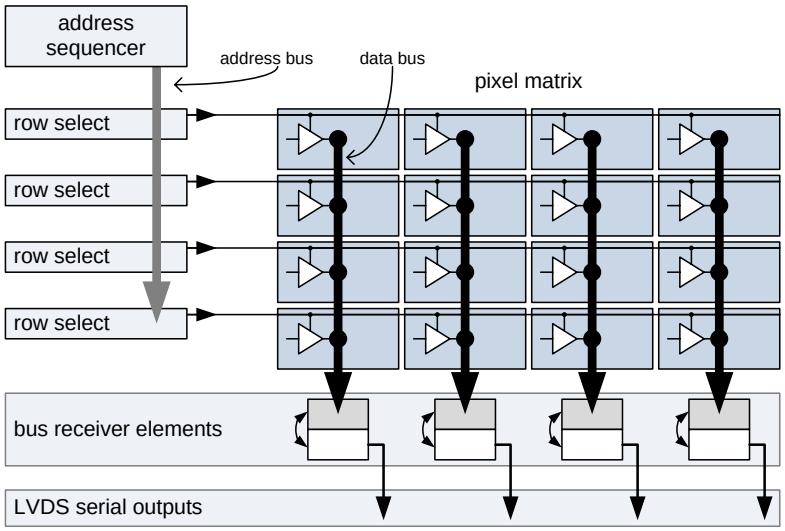

Fig. 4.23: Simplified schematic of the readout chain.

selects a row of pixels and the data channel to be read out, row select elements enable the output buffers in the corresponding row. Each pixel in this row writes its data to the column's data bus. The bus receiver at the end of each bus has two banks, one receives the new data, while the other shifts the previous data to the serial output LVDS drivers. Flexibility with respect to the counter bit depth is achieved through the choice of frequency ratio between address clock and serial output clock. The address sequencer can be configured to select only the desired data channels. All logic was designed with differential current steering logic, more details on the implementation are provided in appendix A.2.

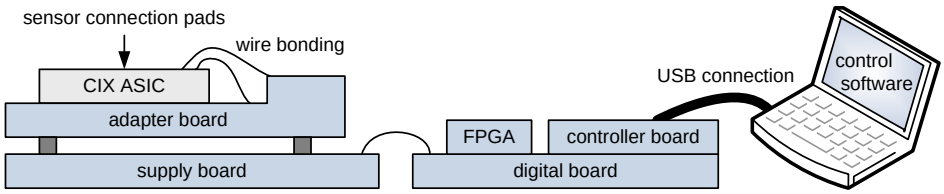

Fig. 4.24: Illustration of the data acquisition and control chain of the imaging system. The design of most components is customized to the requirements of CIX0.2.

4.8 Data Acquisition and Analysis

A fully operational imaging system requires a number of additional components besides the bare readout ASIC (Fig. 4.24) and the imaging sensor. Even though the design effort for each of these is comparable to the original chip design, the details involved are somewhat less relevant to the scientific evaluation of the signal processing concept. They will thus be discussed only briefly. Moving away from the signal source, the components involved in the readout and control of the CIX system are:

- CIX0.2 features 138 IO-pads which need to be connected to the system. Eighty of these are arranged at the bottom of the chip in a double row with an effective pitch of 65 µm. This pad count and density can not be handled with a normal multi purpose chip carrier. Neither is it possible to produce such a fine pitch on conventional printed circuit boards (PCB), even considering the relaxed spacing due to the fan-out structure of the wire bond connections. The solution to this problem was a three-layer printed circuit board with only partial top layer coverage. Areas not covered by the top layer afford access to the middle layer. This structure allows a double arc wire bonding scheme in which the bottom row of pads is connected to the middle layer while the top row is connected to the top layer (Fig. 4.25). This doubling of the effective pitch and a fan-out structure in the wire bond connections allow a design with wire widths and inter-wire spacings compatible with available PCB processing technology (both 100 µm, bond pads slightly wider).

  Each ASIC is bonded to its individual adapter board. Interchange of the adapter board mounted onto the supply board provides an easy way to examine different chips. While the main purpose of the adapter board is the routing of the chip connections to connector pads on the bottom side, it also fulfills a few additional functions: (optional) connection of digital and analog chip ground lines (*gnda, gndd, gnd*), decoupling of supply and reference voltages, high-voltage connection for

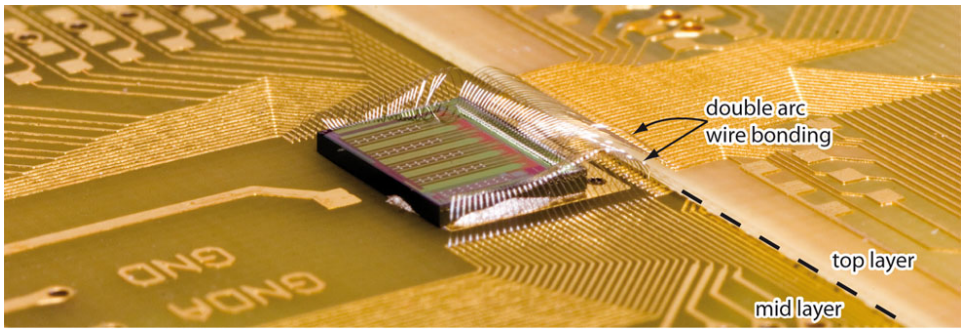

Fig. 4.25: The adapter PCB has only a partial top layer and prepreg coverage, allowing access to the middle layer so that a double-arc bonding scheme is possible. In addition to a fan-out structure of the wire bonds, this helps to relax the effective pitch of the 80 pads at the bottom of CIX0.2 (right side in picture) from 65 µm to 200 µm.

the sensor backplane, thermally and electrically conducting connection to the chip substrate, termination of signal lines.

- The supply board (Fig. 4.26) generates all reference voltages and power supplies needed by CIX0.2. All voltages are controlled by a 32-channel, 14-bit DAC and monitored with a dual channel, 16-bit ADC. In total, the board contains eight *source-monitoring units* (SMUs, configurable voltage or current sources which allow monitoring of the current and voltage at their output), twelve voltage references (voltage measurement only) and four power supplies (*vddd, vdda, vddo,* V_{Lo}). All elements on the supply board are accessed via the *Serial Peripheral Interface*(SPI)-bus provided by the micro controller board. The high-voltage for sensor depletion is generated by an external supply connected to a socket on the supply board. Digital and analog supply lines are also separated on the supply board. The chip grounds can be connected to the analog ground of the analog board either on the supply board or, closer to the chip, on the adapter board.
  Besides the supply function, the board also provides connectors for external measurements, namely the external pad connection and the fast and slow analog busses of photon counter and integrator (left side in Fig. 4.26). Test pins connected to the bias cells of the on-chip DAC elements allow to measure the DAC current/voltage or to override the DAC with an external source. The digital output signals of the chip are simply routed via a 68-pin connector to the digital board. In the opposite direction, control signals generated by the FPGA (see below) are transformed to differential signals of definable voltage levels by single-pole-dual-throw (SPDT) analog switches acting as CMOS-to-DCL converters.

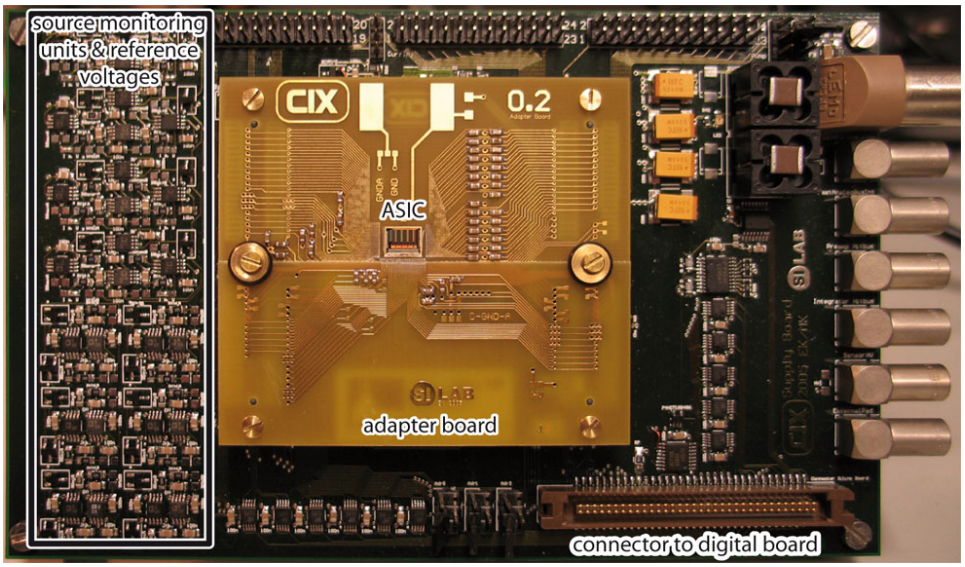

Fig. 4.26: The supply board generates the reference and supply voltages for CIX0.2. It also contains CMOS-to-DCL converters, temperature measurement equipment, test pins, I^2C address configuration jumpers and connection sockets for the high voltage supply, the analog busses and the external pad. All digital signals are routed via the connector to the digital board.

- The key component of the digital board is the FPGA, a configurable IC which can implement almost arbitrary logical functions on its 173 IO-pins. This devices generates all signals and signal sequences necessary to operate CIX0.2. It is also responsible for the acquisition of the digital data from the chip and its storage in memory elements (256 KB) on the digital board. The FPGA is controlled by the micro controller and represents the main interface between PC and chip. Besides the state-machines realizing the acquisition and measurement control logic, it also contains modules which are able to generate pulse sequences with equidistant or Poisson-distributed pulse spacings.
  The digital board itself and the micro controller board which provides the USB interface to the PC are slightly adapted from a different research activity in the work group.

- The control software running on the PC connected to the test system provides the user interface, covering all tasks from low-level control of chip, test system and external devices over diagnosis tools, basic data acquisition and calibration to high level functions like automatic threshold tuning, multi-parameter measurements, stability testing and basic data analysis and graphing. All modules were written in C++.

5. Experimental Results

The counting and integrating channels in each pixel were tested both separately and simultaneously. All measurements took place at room temperature in an environment without special electromagnetic shielding, except for a small cover box enclosing the prototype chip to prevent the illumination with ambient light.

5.1 Calibration

The reference for the chip-wide calibration is the value of the charge pump capacitor C_{Pump}. Since this capacitor is fairly large (25 fF), its size is expected to have a low deviation between the different pixels: in AMS 0.35 µm-technology, the expected tolerance of the pump capacitance is less than 0.2 percent and the temperature influence is typically below 0.05 percent at lab temperatures. The knowledge of C_{Pump} allows the calibration of the integrator, which in return allows the calibration of the injection circuits and the photon counter.

Pump capacitor

The value of C_{Pump} that is actually relevant for further calibration is its *effective* value, which includes the parasitic coupling capacitance of the capacitor with respect to its environment and its connections. This value is best measured in situ, under normal operating conditions[1]. The calibration scheme infers the pump capacitance from measurements of a known current with charge pump packets of varying size. Given the constant, known input current I_c and an unknown pump packet size Q_{pkt} the measured pump frequency f_{Pump} is given by:

$$f_{Pump} = \frac{N_{Pkt}}{\Delta t} = \frac{I_c}{Q_{pkt}} \tag{5.1}$$

[1] CIX0.2 also features a number of dedicated test structures for the calibration of the chip's capacitances. The capacitance measurements obtained with these structures, however, turned out inconclusive. Hence, the calibration scheme described above was devised instead.

N_{Pkt} and Δt are the number of charge packets and the time interval as defined in eqn. 4.3. In the case of the capacitive charge pump, the packet size is given by:

$$Q_{pkt} = C_{Pump} \cdot (V_{PumpHi} - V_{PumpLo}) \tag{5.2}$$

Multiple measurements of f_{Pump} at different values of V_{PumpLo} allow to measure the pump capacitance as a derivative of the packet size:

$$C_{Pump} \quad = \quad -\frac{\mathrm{d}Q_{pkt}}{\mathrm{d}V_{PumpLo}} \quad = \quad -\frac{\mathrm{d}(\frac{I_c}{f_{Pump}})}{\mathrm{d}V_{PumpLo}} \tag{5.3}$$

The result of such a measurement with an input current of about 180 nA is shown in Fig. 5.1. The current, produced by the $I_{LeakSim}$ current source (Fig. 4.19), was routed to the external connection pad and measured with a pico-amperemeter.

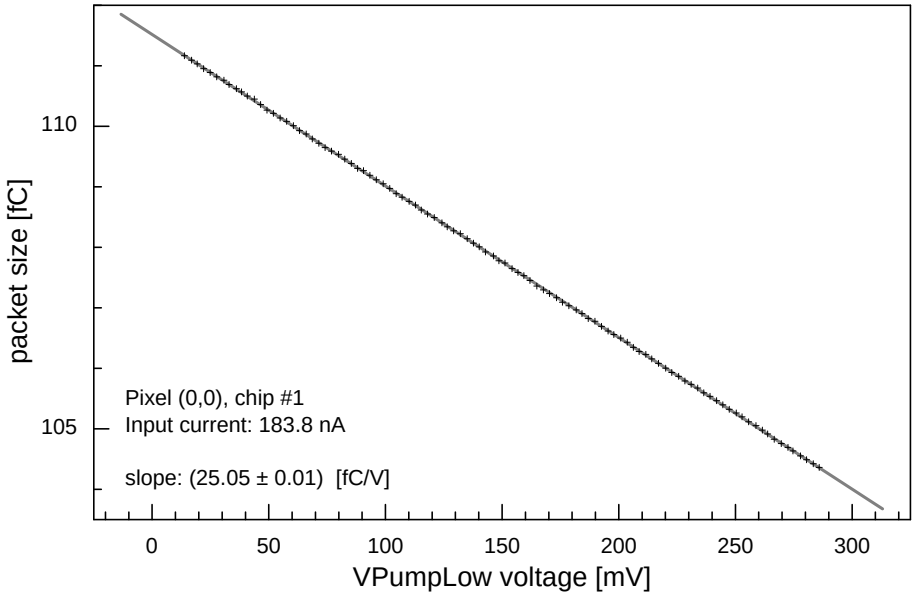

Fig. 5.1: Calibration of the capacitive charge pump capacitor C_{Pump} from the derivative of the pump packet size with respect to the voltage swing. The packet size is computed from the pump frequency and the known size of the input current.

This procedure was executed for multiple pixels on the chip, yielding a mean result of $C_{Pump} = (25.0 \pm 0.5)$ fF. The accuracy of about 2% is a rather conservative estimate, based on the variations found between pixels and the reproducibility of the current measurement with the external pico-amperemeter. Note that since this value is the anchor point for all further calibrations, its accuracy is inherited by all measurements. Any offset in

the actual value will, however, remain static and thus translate only into a systematic scale factor which is identical for all measurements. The achievable measurement *precision* can thus be significantly higher than the *accuracy* of the calibration.

A key assumption implied in the calibration scheme is that the charge pump is fully recharged/discharged during pump events. This, however, is only true if the integrator clock period is long compared to the RC-time constant of the charge pump. Fig. 5.2 shows that this assumption holds for clock frequencies up to about 13 MHz. Higher frequencies can be used as well, but demand individual calibration. All calibrations were carried out at a clock frequency of 10 MHz.

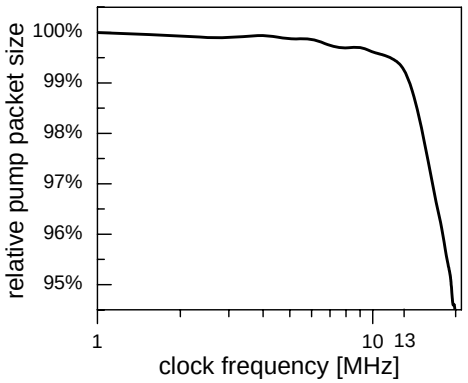

Fig. 5.2: Integrator clock frequency dependence of the capacitive charge pump size. The influence of the RC-time constant of the recharge/discharge process is negligible for frequencies below ≈13 MHz.

Integrator charge packet size

Since the other charge pump types demand individual calibration as well, an automatic pump calibration function was implemented in the control software. This allows a fresh integrator calibration before every measurement series. It bases on two assumptions: a) the value of C_{Pump} is known, constant and identical throughout the chip and b) a change in the $V_{PumpLow}$ voltage will cause an identical change in the voltage swing on the capacitor. Other parameters, such as the input current, threshold and reference voltages, mismatches between pixels, absolute voltage swing and the value of the other voltages on C_{Pump} can change at will.

The pump calibration algorithm first determines the size of a constant, internal current I_c (generated by the $IntBiasI$ current source, Fig. 4.7) from two pump rate measurements (f_1, f_2) at different $V_{PumpLow}$ voltages. Since

both the voltage difference $\Delta V = (V_{PumpLo,1} - V_{PumpLo,2})$ and the pump capacitance are known, the absolute current computes to:

$$I_c = C_{pump} \cdot \Delta V \; \frac{f_1 \cdot f_2}{(f_1 - f_2)} \tag{5.4}$$

Once I_c is known, pump type, pump parameters and integrator clock rate can be changed. The resulting packet size is determined from a new pump rate measurement, using eqn. 5.1.

Charge injection and feedback capacitor

The size of the charge pulses generated with the switched current source (*StrCurr*, Fig. 4.19) can be determined by measuring the current produced by a pulse stream of known frequency with the integrator. Once the pulse charge Q_{inj} has been measured for a number of different injection source DAC settings $I_{CurrInj}$, they can be compared to corresponding peak voltages in the preamplifier output (V_{peak} as visible in the waveforms in Fig. 4.17). The difference quotient between pulse charge and peak voltage gives an absolute calibration of the feedback capacitance C_{Fb}:

$$C_{Fb} = \frac{\Delta Q_{Inj}}{\Delta V_{peak}} \tag{5.5}$$

Note that a benefit of using the derivative instead of the absolute value is that no prior knowledge of the individual pixel's threshold mismatch is necessary. This measurement is, however, only accurate if the feedback is operated at the smallest current possible, so that the ballistic deficit is kept minimal. The chip average of the calibration measurements yielded $C_{Fb} = (10.35 \pm 0.28)$ fF, in which the error accounts for the accuracy of the current measurement (2%) and the standard deviation of the calibration measurements (0.19 fF). The capacitance C_{Inj} of the capacitive chopper circuits is calibrated by comparing the preamplifier output peak voltage to the voltage swing ($vdda - V_{Cal}$) on the injection capacitor:

$$\frac{\mathrm{d}V_{peak}}{\mathrm{d}Q_{Inj}} = \frac{1}{C_{Fb}} \tag{5.6}$$

$$Q_{Inj} = C_{Inj} \cdot (vdda - V_{Cal}) \tag{5.7}$$

$$\Rightarrow \frac{\mathrm{d}V_{peak}}{\mathrm{d}V_{Cal}} = -\frac{C_{Inj}}{C_{Fb}} \tag{5.8}$$

Combined with the value obtained for C_{Fb}, the measured injection capacitance is $C_{Inj} = (3.35 \pm 0.26)$ fF. The accuracy arises from the C_{Fb} calibration and the fit accuracy of $\mathrm{d}V_{peak}/\mathrm{d}V_{Cal}$ ($\approx$7.1%). Table 5.1 summarizes the calibrated effective capacitances an their design values:

capacitor	design	measured
C_{Pump}	25.06 fF	25.0 fF
C_{Fb}	9.32 fF	10.35 fF
C_{Inj}	4.13 fF	3.35 fF

Tab. 5.1: Comparison of the design capacitances to those measured on the prototype ASIC.

5.2 Photon Counter

The discussion of the photon counter characterization requires a brief description of the *threshold scan*, one of the key tools used in the upcoming chapter.

Threshold Scan

A *threshold scan* is the measurement of count efficiency as a function of the comparator threshold voltage (see Fig. 4.5). At each voltage setting, the photon counter is fed with a fixed number of identical input pulses. As the threshold voltage sweeps across the peak voltage U_{Peak} of the preamplifier output signal, the count efficiency shows a transition from 100% to 0% (see Fig. 5.3). The resulting measurement can be fitted by the *cumulative*

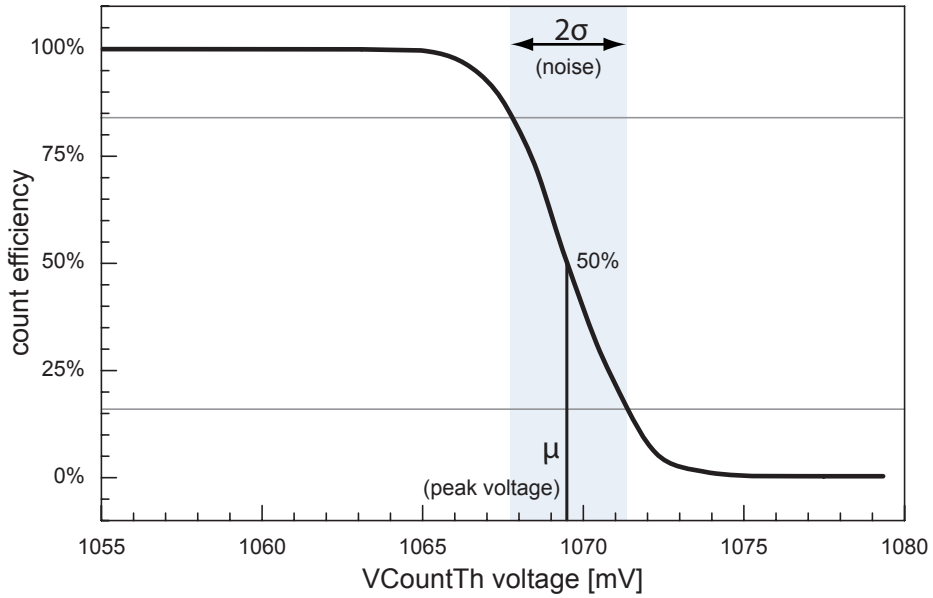

Fig. 5.3: Typical result of a threshold scan. Peaking voltage and electronic noise can be extracted from the fit parameters μ and σ of a cumulative distribution function as described in the text.

distribution function (*CDF*) of the normal distribution[2]:

$$CDF(x;\mu,\sigma) = \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{x} \exp\left(-\frac{(u-\mu)^2}{2\sigma^2}\right) du \quad (5.9)$$

$$= \frac{1}{2}\left[1 + \mathrm{erf}\left(\frac{x-\mu}{\sigma\sqrt{2}}\right)\right] \quad (5.10)$$

Here, erf(x) is the error function, also named *s-curve* due to its shape. In terms of the threshold scan, x denotes the tested threshold voltage, $\mu = U_{Peak}$ is the average peak voltage and σ describes the width of the transition. The value σ is a measure of the electronic noise of the photon counter, its value (a voltage) is often converted into the amount of charge on the input node which would produce a corresponding voltage on the output. This charge is named *equivalent noise charge* (ENC) and expressed in electrons [e$^-$]. In our case, the ENC can be computed by a multiplication of σ with the effective feedback capacitance C_{Fb} as derived from the calibration. In summary, the threshold scan is a measurement of the peak output voltage (i.e. pulse height) and the electronic noise.
There is also an alternative approach to the threshold scan, in which the threshold voltage is kept constant while the size of the input pulses is varied. In the case of the capacitive chopper, this corresponds to a scan in the V_{Cal} voltage. Both approaches can be fitted by eqn. 5.9, and if the proper capacitance is used for the conversion of σ from voltage to electrons (C_{Inj} instead of C_{Fb}), both yield the same ENC within their error limits.

5.2.1 Threshold Dispersion and Tuning

The comparator response of the photon counting channels to a given input signal shows a certain variation between the pixels, a phenomenon known as *threshold dispersion*. Fig. 5.4 (left) shows a histogram of such a measurement with 2 fC input pulses (about 12,000 e$^-$). Such a large dispersion translates to a very inhomogeneous energy discrimination. If the average threshold is chosen so that only photon pulses in excess of 12,000 e$^-$ are counted, one pixel will only count pulses with more than 15,000 e$^-$ while a pixel on the other extreme will also count pulses with 10,000 e$^-$. This problem is addressed with the 6-bit tuning DACs in every pixel. These DACs tune the currents in the comparator stages so that the comparator threshold voltage is shifted by an amount proportional to the DAC setting. The gain factor of this shift is controlled by a global bias DAC I_{Trim}. Sufficient gain settings are usually in the order of 1.4 mV per step.
An automated tuning algorithm implemented in the control software tries to determine a set of tune values so that the remaining threshold dispersion is minimized. The algorithm involves the following steps:

[2]Since the CDF as given produces a 0 to 1 transition, 1−CDF(x) is the function actually used in the case shown in Fig. 5.3.

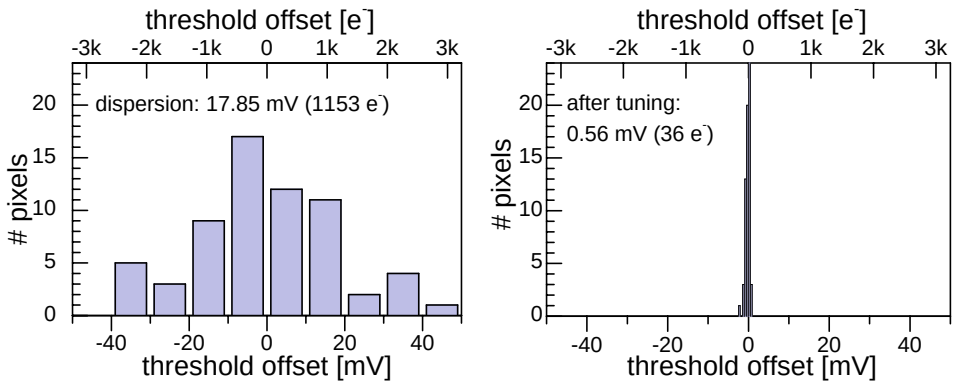

Fig. 5.4: Comparison of the threshold dispersion before (left) and after automatic threshold tuning (right). A detailed view of the threshold distribution underlying the histogram in the right graph is shown in Fig. 5.5. The standard deviation decreased from 17.85 mV (1153 e⁻) to 0.56 mV (36 e⁻).

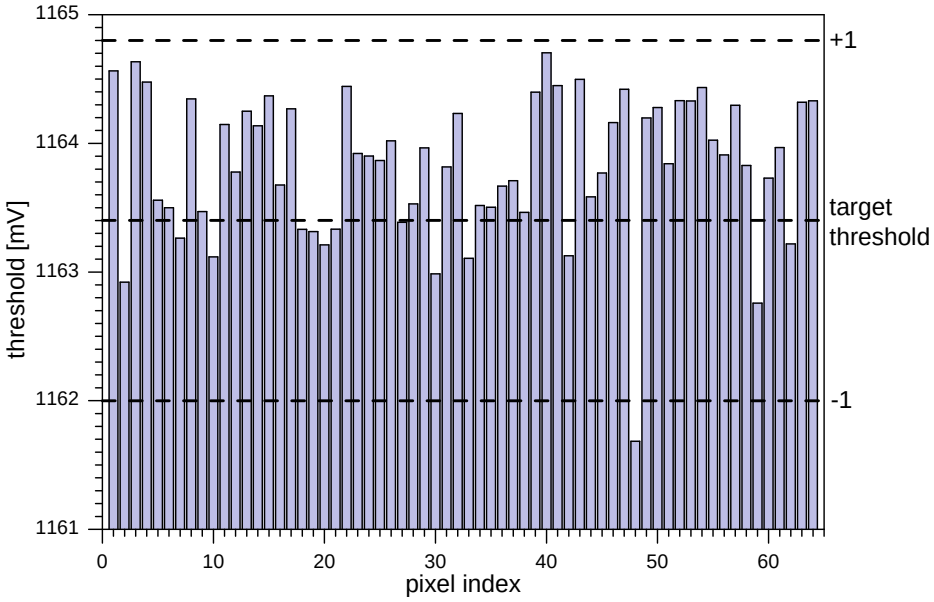

Fig. 5.5: Distribution of peak voltages measured by a threshold scan after the automatic threshold tuning. Dashed lines mark the threshold voltage aimed for by the tuning algorithm and the interval of ± one tune DAC step. All but one pixel fall in the expected interval.

1. Two threshold scans determine the extend of voltage range covered by the tune DACs and measure the extend of the threshold dispersion.

2. The algorithm tries to find a threshold voltage achievable in all pixels (or, alternatively, the voltage with the minimal remaining dispersion) and computes a set of the expected corresponding DAC values $\{t_i\}$.

3. Five threshold scans are conducted with tune settings in the vicinity of the computed value $t_i + \Delta$ with $\Delta \in \{-2, -1, 0, 1, 2\}$.

4. The value whose resulting threshold scan came closest to the desired threshold voltage is accepted. A new threshold scan with the set of final tuning values measures the resulting threshold dispersion achieved by the tuning process.

The outcome of this tuning process is shown in Fig. 5.4 on the right hand side. Here, the standard deviation decreased from 17.85 mV (1153 e^-) to 0.56 mV (36 e^-). A closeup of the peak voltages determined by the final threshold scan is given in Fig. 5.5.
The precision of the tuning outcome can be enhanced by increasing the number of sample points in the threshold scan, increasing the search interval around the expected tuning value and by minimizing the gain setting, so that almost the full range of possible tune DAC values is covered. As can be seen in Fig. 5.6, the tune DAC values obtained by the tuning algorithm show a strong correlation to the offset voltages of the respective pixels before the tuning.

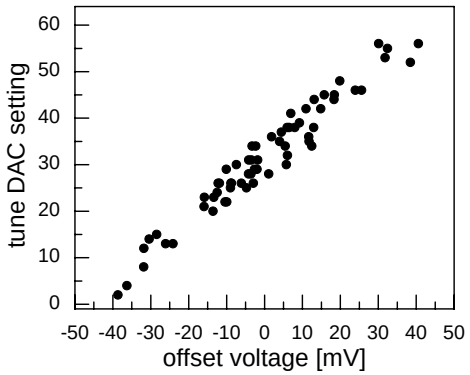

Fig. 5.6: Correlation between the settings obtained by the tuning algorithm and the offset voltages measured beforehand.

Threshold Definition Procedure

For a normal measurement, it is desirable to set the threshold in such a way that all pixels will count pulses which are larger than a certain, well defined size. This is achieved by performing an automatic threshold tuning with input pulses whose size matches the desired threshold. These pulses are generated by the capacitive chopper circuits, their size is controlled by V_{Cal}. The threshold voltage on the comparator $V_{CountTh}$ is then set to the resulting tuning value. Note that the threshold setting is thus determined by the choice of V_{Cal}, whereas the value of $V_{CountTh}$ is just a result of this choice. This procedure removes all offsets due to comparator mismatches, dispersion in the feedback current and gain variations. As a result, the threshold is both well defined and uniform.

5.2.2 Dynamic Range

The dynamic range of a photon counter starts with a single photon during the measurement interval and reaches up to photon fluxes at which the pileup of subsequent pulses becomes dominant, leading to a corresponding decline in counting efficiency.

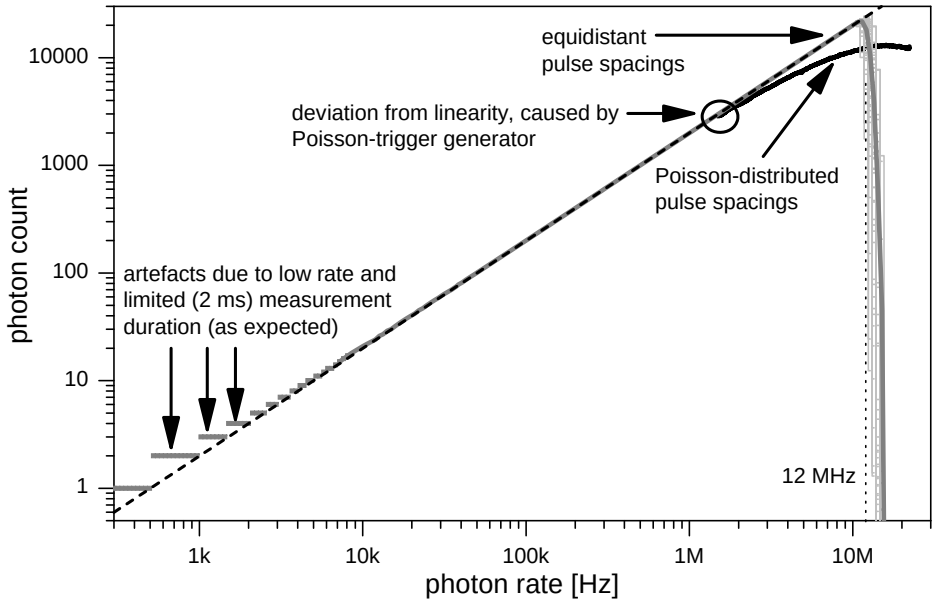

Fig. 5.7: Dynamic range of the photon counter, tested with 2.1 fC input pulses. Gray lines: response to pulses of equidistant spacings (superposition of the all measurements in all pixels), full count efficiency is achieved up to the steep decline which marks the maximum the count rate at about 12 MHz. Black: Poisson-distributed pulse spacings cause a more gradual decline, with a maximum photon count at a similar frequency. The dashed line denotes 100% count efficiency.

In the case of artificially generated, equidistant test pulses, this decline is very steep, because any remaining charge of the previous pulse quickly adds up and saturates the preamplifier. The maximum count rate is thus well defined and depends only on the shaping duration, which is determined by the feedback strength and pulse height, but not the threshold setting.
In the more realistic case of Poisson-distributed pulse spacings, the decline depends on the threshold settings. If large threshold voltages are chosen, the decline is more gradual than in the case of equidistant pulse spacings. The maximum number of recorded counts per frame matches roughly with the frequency of the steep decline measured with equidistant pulse spacings. Fig. 5.7 shows a comparison of both behaviors with 2.1 fC input pulses, a threshold setting of about half the pulse size and a feedback current of 91 nA (static leakage compensation mode). The measurement duration was 2 ms.

The maximum count rate of equidistant 2.0 fC input pulse achieved under optimal conditions was 18.6 MHz on average with a chip-wide dispersion of about 1 MHz. Optimal conditions are:

- Maximum feedback currents ($I_{Fb} = 91$ nA). A smaller feedback current (14.5 nA) limits the frequency to 2.8 MHz.
- Small input pulse durations of 10 ns. Measurements with longer pulses (30 ns), which were tuned to achieve the same peak voltage, showed a decrease in the maximum rate to 11.0 MHz. This is decrease is stronger than expected, which is most likely due to a larger total signal charge. The longer pulse duration will also cause a larger ballistic deficit, so that more charge is needed for the same peak voltage.
- Maximum comparator bias currents while maintaining reliable operation in all pixels. In a limited number of pixels, larger comparator settings allow count rates up to an average (in this subset) of 20.9 MHz. Individual pixels can cope with count rates rates up to 24 MHz.
- 2 fC input pulses. Since the return-to-baseline interval is approximately proportional to the pulse size, the product of maximum count rate and pulse size is about constant.
- Maximum preamplifier bias currents. These are, however, only of comparably small influence. If the biasing is reduced to one quarter, the photon counter still operates up to 16.6 MHz.
- Static leakage compensation. Dynamic leakage compensation and controlled redirection often allow higher count rates than static compensation, yet they are much more difficult to adjust to measurements of the absolute maximum rate. The signal dependent baseline shift would require careful tuning of the threshold voltage to the other operation parameters involved. In result, a number for the maximum count rate in these modes would not be meaningful.

Note that the operation parameters achieving the maximum count rates are often not desirable for normal operation due to large power consumption, higher noise and a large ballistic deficit.

5.2.3 Electronic noise

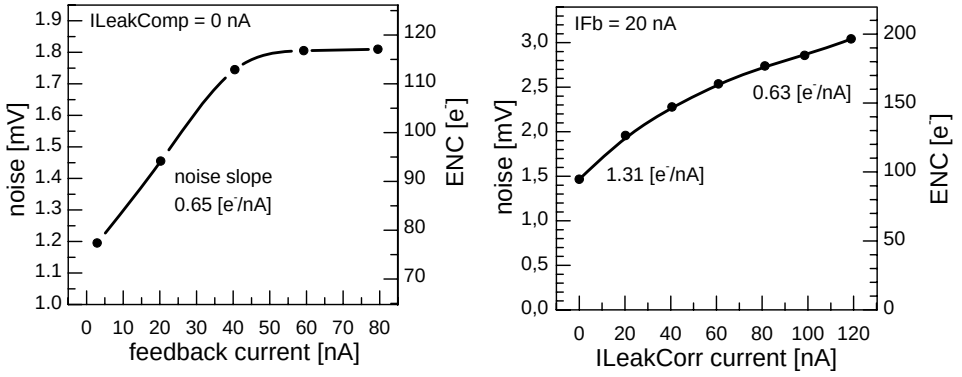

Fig. 5.8: Photon counter noise performance of CIX0.2 under variation of the feedback bias currents. The equivalent noise charge was obtained from threshold scans with equidistant 2 fC input pulses at 10 kHz. Left: increasing feedback currents add 0.65 e^-/nA to the minimal noise of 78 e^-. The noise saturates at 117 e^- for large feedback currents. Right: The leakage compensation bias current increases the noise by 0.6 to 1.3 e^-/nA.

The measurements in Fig. 5.8 show an investigation of the photon counter noise performance with 2 fC charge pulses produced by the switched capacitor injection method (*Str1*). Threshold scans yield an electronic noise equivalent to approximately 78 e^- at minimal feedback settings. Larger I_{Fb} feedback bias currents cause an additional noise of about 0.65 electrons per nA (Fig. 5.8, left). The $I_{LeakComp}$ bias current in the second differential pair increases this value with a slope between about 0.6 and 1.3 electrons per nA (Fig. 5.8, right, measured at $I_{Fb} = 20$ nA).
Investigations on the CIX0.1 prototype chip measured the dependence on the capacitive load at the preamplifier input node [4]. This was made possible by five 100 fF capacitors which could be connected to the input node – a feature not included in CIX0.2 due to area constraints. Starting from an ENC of 119 e^- without additional load, the noise increases by approximately 0.375 electrons per fF. Typical noise slopes respective to I_{Fb} and $I_{LeakComp}$ were 0.72 e^-/nA and 1.00 e^-/nA, similar to the values obtained for CIX0.2.

5.2.4 Noise Count Rate

The noise count rate of the photon counter is measured by sweeping the comparator threshold voltage $V_{CountTh}$ around the baseline voltage at the preamplifier output ($V_{CountBaseline}$). If no additional input signal is present, all recorded counts can be attributed to noise. The result of such a measurement is shown in Fig. 5.10. The noise count rate reaches its maximum when the comparator threshold matches the baseline. Its absolute value is a

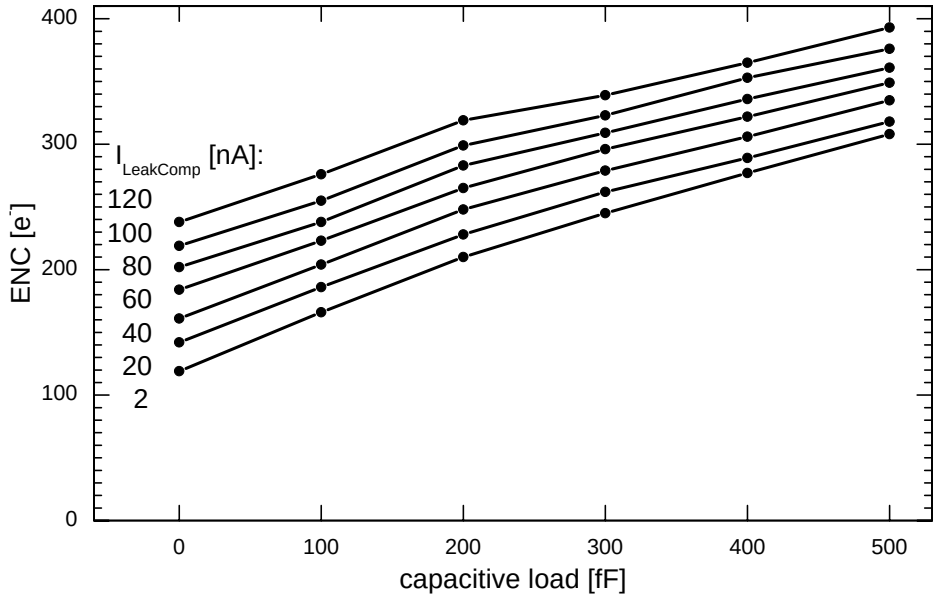

Fig. 5.9: Photon counter noise performance of CIX0.1 under variation of the capacitive load on the amplifier input node and the leakage compensation bias current $I_{LeakComp}$. The equivalent noise charge was measured using threshold scans with equidistant 2 fC charge pulses at 12.7 kHz pulse rate and a feedback current bias setting of 19 nA. The photon counter noise increases from 119 e^- by about 0.375 e^- per fF additional capacitive load and by 1.00 e^- for each nA of leakage compensation bias current.

influenced by the speed of comparator and preamplifier and the magnitude of the feedback current. The noise count rate distribution is symmetrical in the voltage difference, which is expected since a count event requires both a positive and a negative transition in the comparator output. It is, however, a remarkable sign of small digital to analog crosstalk that CIX0.2 can measure this function at all. In designs with a larger crosstalk, the digital activity caused by a noise hit can trigger additional comparator transitions. This counting only stops if the threshold voltage is increased beyond the level of crosstalk (hysteresis). No such effect was encountered in CIX0.2. The shape of the noise count rate can be fitted by a gaussian distribution [49], as can be seen in Fig. 5.10. Its standard deviation is comparable to the ENC obtained from threshold scans. The noise count rate adheres to the gaussian shape even at threshold voltages further away from the baseline, as can be seen from the inverse-parabolic shape in the logarithmic plot of the same data set in Fig. 5.11. This plot allows an accurate prediction of the noise count rate at a chosen threshold voltage. For example a threshold voltage of 6 mV (400 e^-) above the baseline will yield an expectation value of less than one noise hit during a 1 ms measurement. If the threshold voltage is

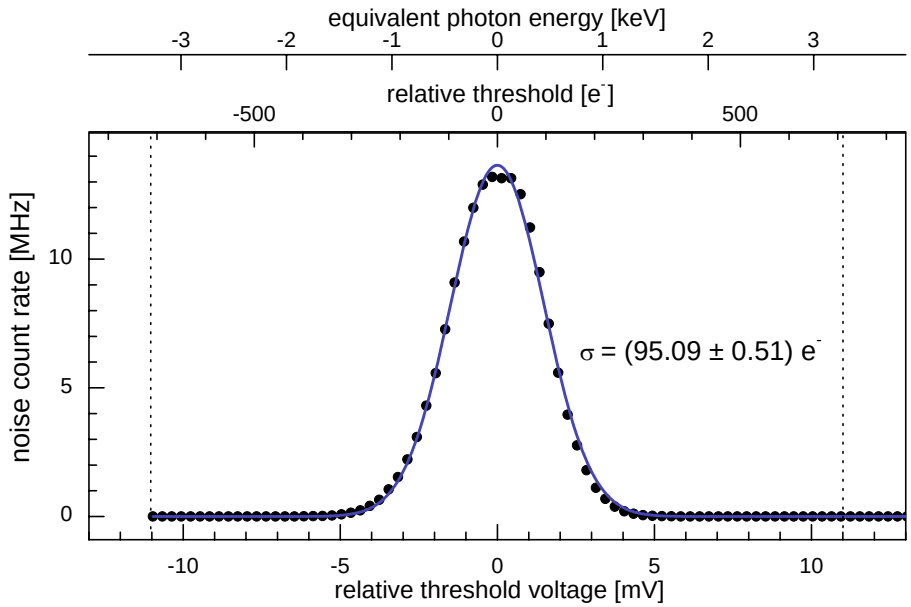

Fig. 5.10: Noise count rate of the photon counter, measured in the absence of input signals by sweeping the comparator threshold voltage around the preamplifier output baseline voltage (compare Fig. 4.5 and Fig. 4.12). All counts are caused by the inevitable electronic noise. Low digital-to-analog crosstalk is a key requirement for this measurement.

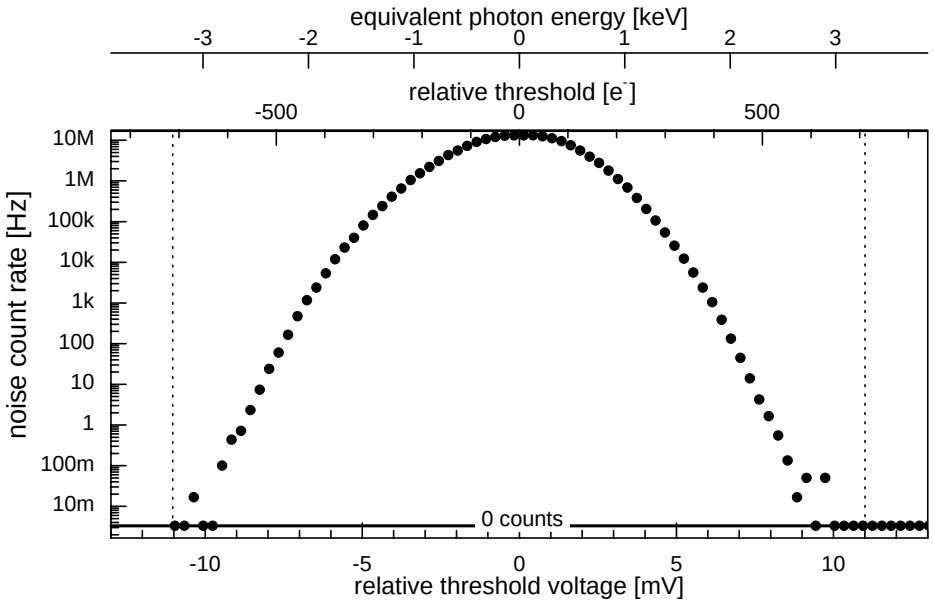

Fig. 5.11: Logarithmic plot of the noise count rate measurement. Noise count rates below one per millisecond are obtained for thresholds above 6 mV. Less than one noise count per minute is achieved above 9 mV.

chosen larger than 9 mV, the noise count rate drops below a single hit per minute. Fig. 5.12 shows the influence of the feedback current on the noise

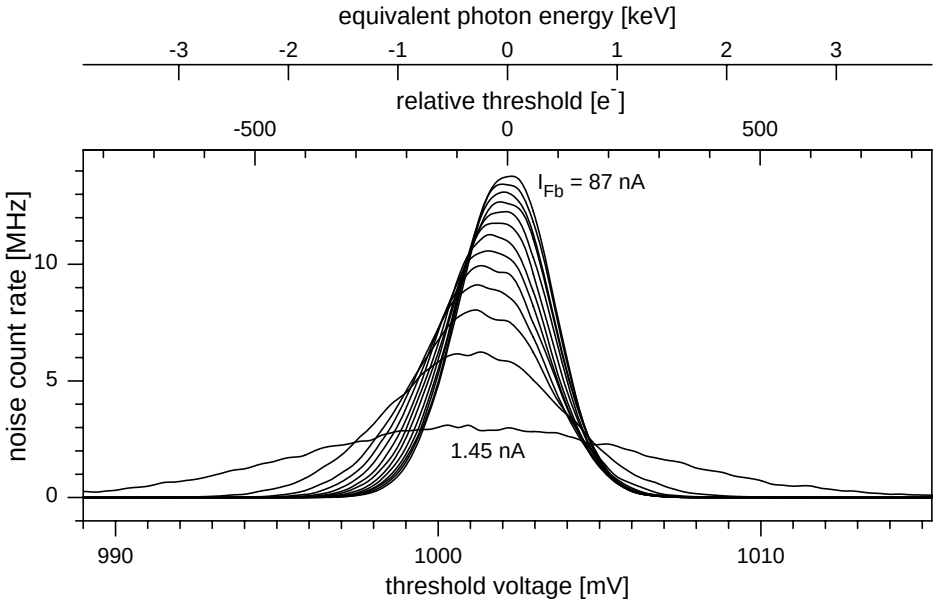

Fig. 5.12: The feedback current I_{Fb} controls both the maximum noise count rate and the width of the distribution. Higher settings cause a higher maximum noise count rate and a slight shift in the baseline, but can also lead to a decreased number of noise counts if the threshold voltage is further away from the baseline.

count rate. Both the maximum count rate and the width of the distribution depend on the feedback current. Larger currents produce more noise hits at the maximum, but less noise hits in the distance. It is thus possible to use a lower threshold setting at the same noise count rate. Higher feedback bias currents also cause a slight shift in the baseline, which is caused by mismatches in the first differential pair. Section 5.4.1 discusses the influence of the feedback bias setting on the offset currents due to this mismatch.

5.2.5 Charge Injection

The photon counter noise is also influenced by the method of charge injection. Capacitive charge injection ($Str1$, $Str2$) shows typically both less noise and a smaller dispersion of the noise among the pixels than the switched current source charge injection ($StrCurr$). Fig. 5.13 compares both injection types in a measurement of the photon counter noise with 2 fC input pulses at 10 kHz (I_{Fb} = 91 nA, $I_{LeakComp}$ = 0 nA). Capacitive charge injection with $Str1$ showed a noise of (111.7 ± 7.8) e$^-$ compared to (144.8 ± 15.2) e$^-$ in the case of the current chopper. Note that the dispersion between the pixels has almost doubled. The noise of the current chopper is related to its transconductance g_m. Pixels whose charge chopper has a large g_m will thus not only show a higher peaking voltage due to the increased current, but also a larger noise.

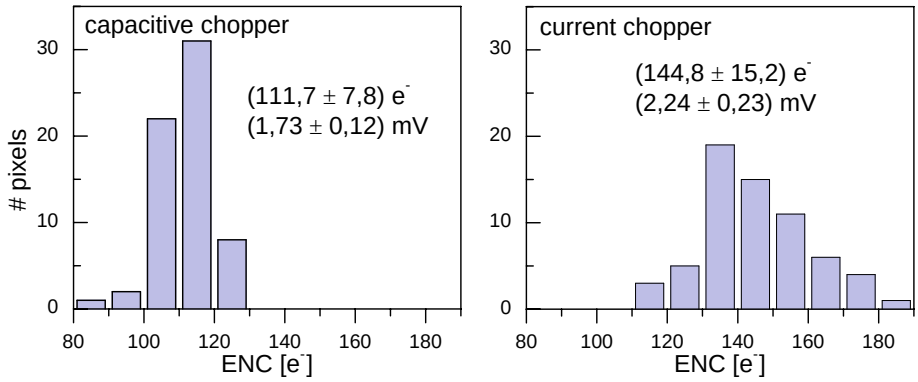

Fig. 5.13: Comparison of the noise performance of capacitive and switched current source charge injection circuits. The current chopper shows both a 30% higher noise and a twice as large dispersion along the pixels.

5.2.6 Ballistic Deficit

The ballistic deficit is the amount of charge which is removed from an input pulse before the preamplifier output reaches its peak voltage. Its size depends on the feedback current and the output rise time. In a simple model, it is the product of both.

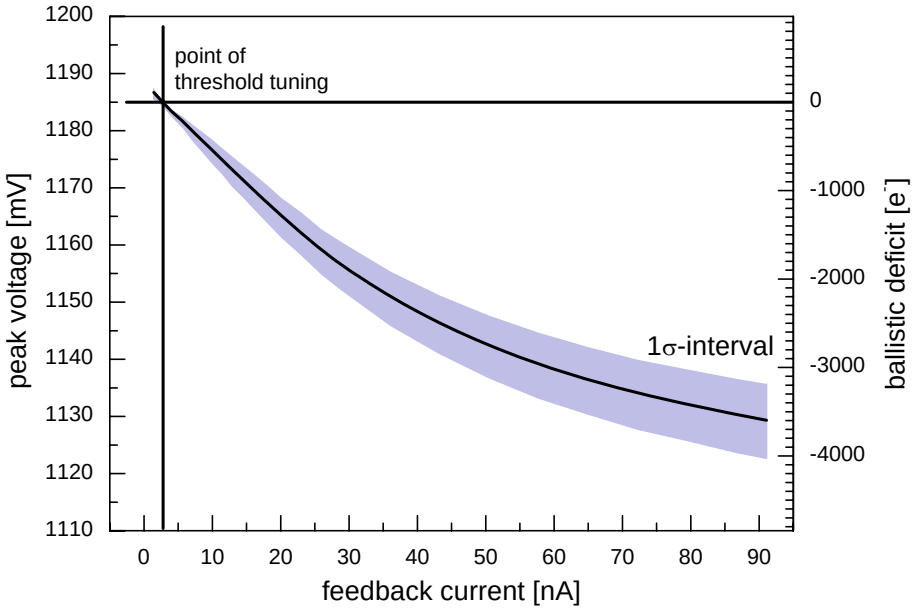

Fig. 5.14: Ballistic deficit of the photon counter as a function of the feedback current. Measured from 2 fC (12,000 e⁻) input pulses after a threshold tuning at $I_{Fb} = 2.8$ nA. The deficit corresponds to a signal rise time of 12.5 ns.

Fig. 5.14 shows a measurement of the ballistic deficit with 2 fC (12,000 e⁻) input pulses. The automatic threshold tuning was performed at a very small feedback current of about 2.8 nA. Subsequent threshold scans measured the peaking voltage in every pixel as a function of the feedback bias setting. As expected, larger feedback currents cause a deficit in the achieved peak voltage, which can be expressed in terms of electrons using the known size of C_{Fb}. The dispersion between the pixels seen in Fig. 5.14 is caused by mismatches in the actual feedback current and by differences in the signal rise time. At large feedback settings, the ballistic deficit can amount to a significant fraction of the total signal charge, for example 21% to 37% at $I_{Fb} = 91$ nA. The resulting charge loss of about 3,500 e⁻ corresponds to the charge delivered by the feedback circuit (here: $I_{Fb}/2 = 45$ nA) within 12.5 ns, a number compatible with the typical signal rise times.

5.2.7 Double Pulse Resolution

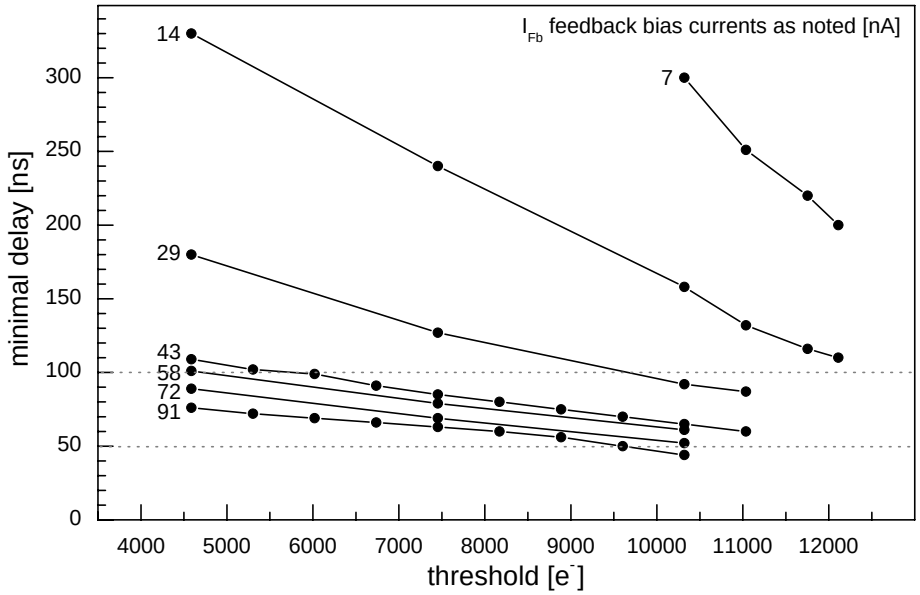

Fig. 5.15: Double pulse resolution: Minimal delay between two consecutive charge pulses allowing a reliable distinction of both. This delay depends on the comparator threshold voltage and the feedback current. The minimal delay (43 ns) for this pulse size was achieved using a threshold voltage of 10,300 e^- and a feedback current setting of 91 nA.

An investigation showed that the analog signal processing allows distinction of two typical photon signals (using optimized feedback and threshold settings) if the time difference of their occurrence exceeds approximately (43 ± 5) ns. This was tested using a series of one thousand 2 fC double pulses with a tuneable delay between the two pulses. The distinction was assumed to be reliable if all 2,000 pulses (=1,000 double pulses) were counted successfully. Since each pixel on the chip showed a slightly different minimal separation, each measurement noted the minimal delay at which a) all pixels, b) half the pixels and c) only the last pixel work reliably. The results in Fig. 5.15 show the chip median (measurement b) of the minimal delay under variation of the comparator threshold and the feedback current settings. The minimal delays of the 'slowest' and the 'fastest' pixels (measurements (a) and (c)) lay typically about 11% above and 13% below the chip average, respectively. A continuous stream of equidistant 2 fC pulses is measured correctly up to a maximum rate of approximately 18 MHz using static leakage current compensation and optimized settings. This rate corresponds to an input current of about 36 nA (pulse charge frequency product). Higher rates can be achieved with continuous leakage current compensation.

5.2.8 Poisson-distributed Pulse Spacings

Electronic testing of a signal processing circuit is often done with test pulses triggered by an external pulse generator. These devices can usually produce pulse sequences of arbitrary pulse count, width and frequency. The spacing between subsequent pulses, however, is identical for all pulses.
Actual sensor signals, on the other hand, consist of charge pulses caused by the absorption of photons in the sensor material. Their temporal distribution is random and can be described by a Poisson-distribution. In a photon stream of average flux ϕ, the mean rate λ of photons passing through an area A is given by $\lambda = \phi \cdot A$, so that the mean time interval τ between subsequent pulses computes to $\tau = 1/\lambda$. The probability to observe n photons during a time interval t is then given by

$$P_n(t) = \frac{\mathrm{e}^{-\lambda t}(\lambda t)^n}{n!}. \tag{5.11}$$

The probability for a certain pulse spacing or in other words the probability to observe *no* photon ($N = 0$) is simply

$$P_0(t) = \mathrm{e}^{-\lambda t} = \mathrm{e}^{-\frac{t}{\tau}}. \tag{5.12}$$

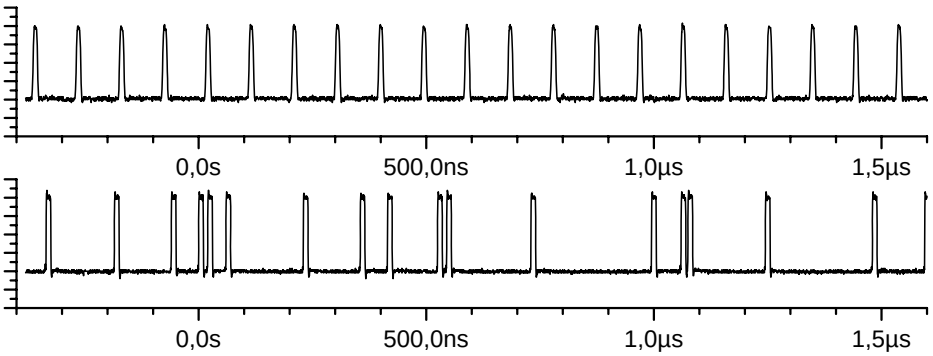

Fig. 5.16: Comparison of two trigger sequences of similar mean frequency, but a different distribution of pulse spacings. Top: equidistant pulse spacings, bottom: Poisson-distributed pulse spacings.

A pulse sequence with spacings fulfilling this distribution can be produced electronically with a fast external pulse generator which is able to output a programmable bit sequence. The bit sequence is generated from random numbers $\{q_i \mid 0 < q_i < 1\}$ by mapping them to a set of time intervals $\{t_i\}$:

$$t_i = -\tau \cdot \ln(q_i) \tag{5.13}$$

The sequence is filled with trigger pulses whose time intervals are drawn from $\{t_i\}$. A slight deviation from the ideal distribution is introduced by

the time discretization imposed by the pulse generator's output bit rate, the necessary pulse duration and the minimal spacing between two subsequent trigger pulses. A comparison of such a sequence to equidistant trigger signals is shown in Fig. 5.46.

Polychromatic Signals

The generation of trigger pulses with such a bit sequence has the additional benefit that it is also able to produce polychromatic test signals. This feature arises from the pulse size of the current chopper (*StrCurr*), which depends both on the bias current $I_{CurrInj}$ and the pulse duration. While the bias setting cannot be changed quickly, the pulse duration is flexible down to the bin size imposed by the pulse generator's output bit rate. Provided this bit rate is high enough (in the order of 1 Gbps), polychromatic signals can be produced by varying the pulse width of the trigger pulses in the bit sequence. This allows the generation of artificial input signals which mimic the spectrum of a real X-ray spectrum.

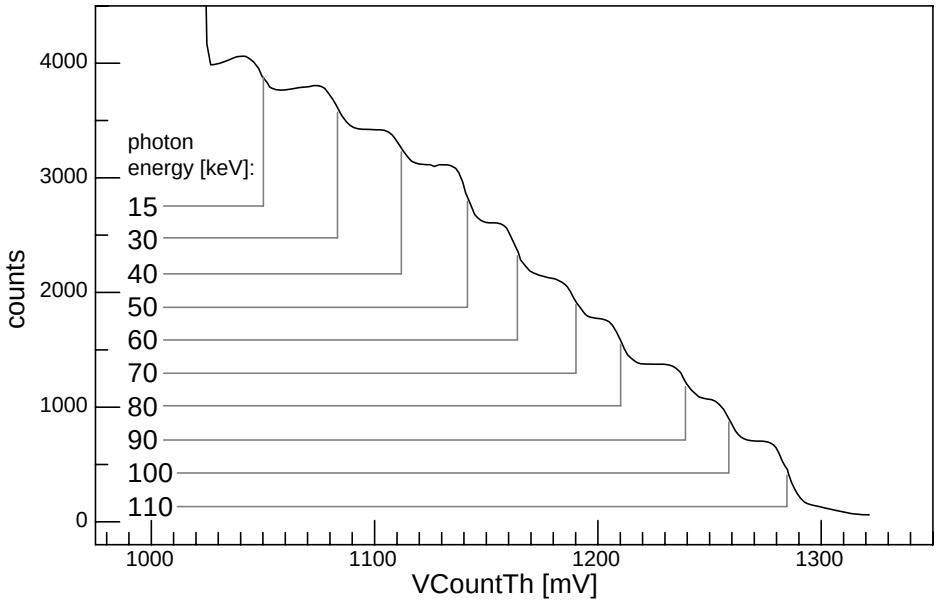

Fig. 5.17: Threshold scan of a polychromatic input signal with Poisson-distributed pulse spacings. Each energy present in the input signal contributes its own step. The numbers denote the photon energy [keV] corresponding to each energy bin. The input spectrum had similar pulse rates at all energies.

The first step is the calibration of the pulse size E_w in every pixel for the desired range of pulse durations w (typically between 5 and 30 ns), from current measurements with the integrator. A simulated X-ray spectrum can then be mapped to a set of pulse rates $\{\lambda_w\}$ at each energy bin. The

generation of the bit sequence works similar to the scheme discussed above. Time intervals are computed for the τ-value corresponding to the cumulative pulse rate. At each trigger, a random pulse duration is chosen according to the fractional contribution derived from the set $\{\lambda_w\}$:

$$P(w) = \frac{\lambda_w}{\sum_i \lambda_i}$$

A threshold scan of such a polychromatic input signal is displayed in Fig. 5.17. Since the input signal consists of photons with a number of different energies (as marked on the left side), the resulting threshold scan is a superposition of the respective s-curves. The step positions and step heights correspond to the energy and flux of the different input signal constituents.

5.2.9 Measurements with Poisson-distributed Pulses

The response of the preamplifier to a (monochromatic) input signal with Poisson-distributed pulse spacings is displayed in Fig. 5.18. Due to the fluctuations in the pulse intervals, there are both phases with pileup and phases in which the signal returns to its baseline. This is the reason why a threshold scan on such a signal will show omitted counts at low thresholds as well as count events at threshold voltages above the typical peaking voltage of this pulse size. Neither of them occur in a threshold scan at the same frequency with equidistant pulses. The deviation from an 'ideal' threshold scan (as seen in Fig. 5.3) will become more severe as the pulse rate increases.

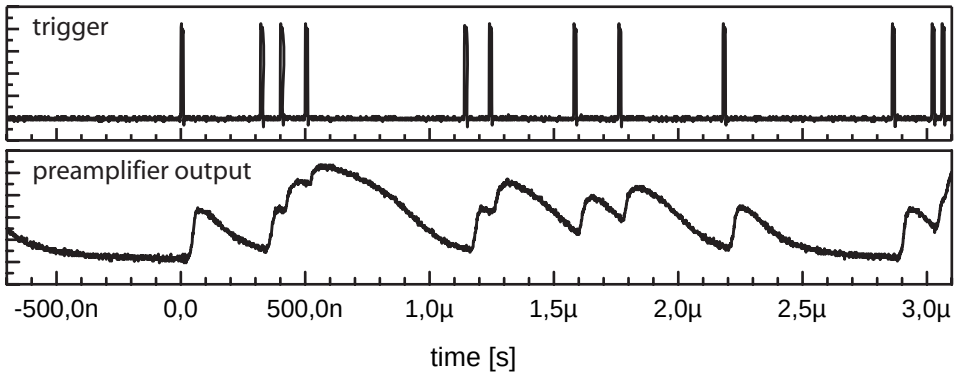

Fig. 5.18: Poisson distributed trigger signals (top) and the corresponding output of the preamplifier (bottom). The waveform contains events with multiple pileup as well as phases in which the signal returns to its baseline. The distortion seen at high output voltages is an artifact from the limited dynamic range of the analog output buffer.

This can be seen in the threshold scans shown in Fig. 5.19. Input pulses of 2 fC were injected at different average pulse rates (noted in [MHz]). The feedback

was configured for static leakage compensation, $I_{Fb} = 91$ nA, $I_{LeakComp}$ was turned off. Hence there is no baseline shift at larger pulse frequencies as would be present with dynamic leakage compensation or controlled redirection feedback mode. The threshold scans retain an resemblance to an error function for pulse rates up to about 1 MHz, even though at a decreased count efficiency of only 80%. At larger pulse rates, the threshold becomes increasingly ill-defined.

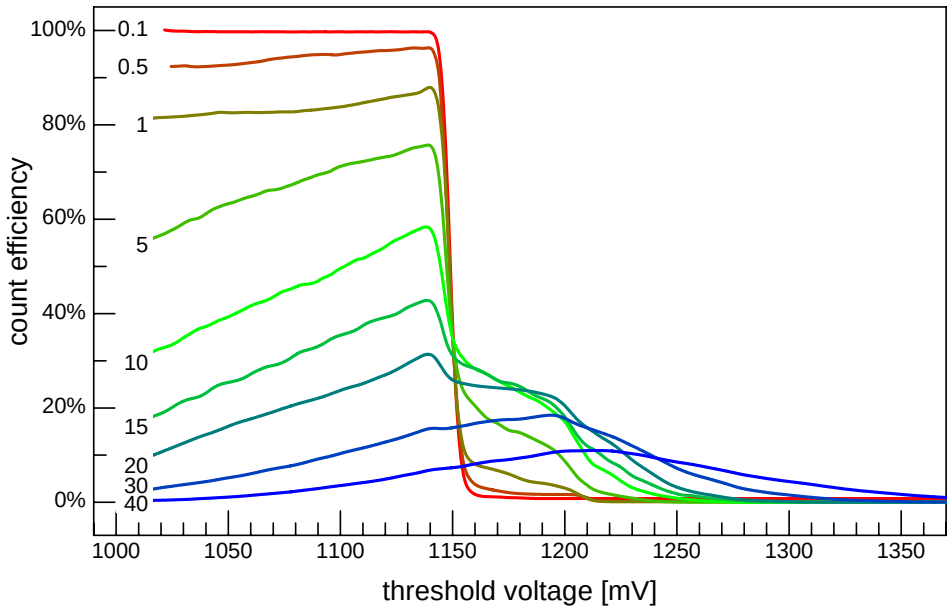

Fig. 5.19: The shape of threshold scans with Poisson-distributed pulse spacings has a strong dependence on the average pulse rate (noted in MHz). For rates up to about 1 MHz, the result still bears some resemblance to an error function, even though at a decreased count efficiency of 80%. The increased pileup at higher frequencies leads to a loss of counts at small thresholds and to additional counts at thresholds beyond the normal peak voltage. Feedback was in static leakage compensation mode, hence no shift occurred at high frequencies.

5.2.10 Photon Counter Breakdown Behavior

The breakdown behavior of the photon counter has a large dependence on the distribution of the pulse spacings. Equidistant pulses cause a very steep decline in count efficiency once a substantial pileup of subsequent pulses occurs. Poisson-distributed pulse spacings, on the other hand, show a more gradual decline, as can be seen in Fig. 5.20.

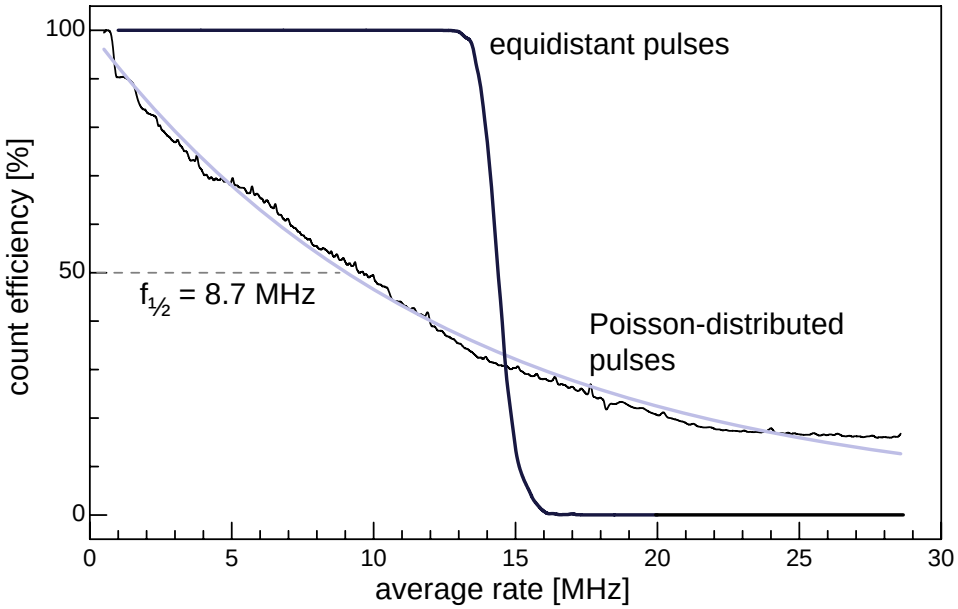

Fig. 5.20: Comparison of the photon counter breakdown behavior with equidistant and Poisson-distributed pulse spacings. Equidistant pulses cause a steep decline in count efficiency above 14 MHz, whereas Poisson-distributed spacings lead to an approximately exponential decrease with $f_{1/2} = 8.7$ MHz.

In this example, the input signal consisted of 2 fC pulses generated by the *StrCurr* current chopper with 10 ns trigger signals. Both measurements used a threshold setting of half the pulse size and feedback currents of 91 nA. In case of the equidistant pulses, the maximum count rate in the measurement was about $f_{max} = 14$ MHz, which corresponds to an effective return-to-baseline time of $t_0 = 1/f_{max} = 71.4$ ns. Shorter pulse spacings lead to pileup which quickly saturates the preamplifier.
The shape of the gradual decline of the Poisson-distributed input pulses can be fitted by the model of the count efficiency η of a paralyzable photon counter, as described in [50]:

$$\eta(f) = \mathrm{e}^{-f\tau} \tag{5.14}$$

Here, τ denotes the system dead time, i.e. the time interval after a trigger event during which no subsequent pulses are counted. The fit to the measured

data yielded the value $\tau = 79.4$ ns, corresponding to a frequency of $f_d = 12.6$ MHz. This value lies close to the maximum count rate found with equidistant input pulses, which is to be expected for a paralyzable counter with the given dead-time. The model used in [50] is, however, only a simplified description of the photon counter. It assumes that the dead-time is independent of the residual charge on the feedback capacitor at the occurrence of a new event. In the CIX photon counter, this is not the case, since the return-to-baseline time will increase proportional to the additional pulse charge. This difference becomes even more relevant when multiple pileup occurs. The model also neglects the influence of the threshold setting (here at half the pulse height). Large threshold settings allows to count new pulses before the output has returned to its baseline. There is also the experimental limitation that two subsequent pulses must have a minimal spacing (here: 15 ns). This constraint causes a deviation of the generated pulse spacings from a real Poisson-distribution, which becomes increasingly significant as the average frequency increases.
Keeping this in mind, the breakdown behavior of the photon counter can be summarized as follows: The count efficiency of equidistant pulses is 100% up to about 14 MHz and drops to zero at 15 MHz. The count efficiency of input pulses with Poisson-distributed pulse spacings decreases by one half with each increase in pulse rate of about 8.7 MHz ($= f_d \cdot \ln 2$).

5.3 Integrator

The measurements presented in this section characterize the integrator on its own, without the influence of the feedback circuit. Most measurements were done by injecting the charge directly into the integrator, bypassing the feedback. Two charge injection methods were used:

- *Pulsed* current injection with the *StrCurr* current chopper, which is connected to the injection node and can be routed directly into the integrator (Fig. 4.19). If pulse width and pulse spacing are sufficiently large (larger than a few ns), the pulse size is determined by pulse duration and the strength of the $ICurrInj$ current source.

- *Continuous* current injection with the $IntBiasI$ current source, situated on the integrator input node (Fig. 4.7), or with the $ILeakSim$ current source, connected to the input node like the current chopper. The magnitude of the current delivered by both sources can be controlled either by their respective on-chip DAC or by an external source (Keithley 2400). Both on-chip DAC and external source are connected to the input of current mirror circuits which scale down the current. The designed mirror ratios are 4,000:1 for the $IntBiasI$ source and 400:1 for $ILeakSim$.

5.3.1 Dynamic Range

The dynamic range of the integrator was found to be in good agreement with the theoretically expected value determined by measurement duration, integrator clock frequency and pump packet size as explained in section 4.3. Fig. 5.21 shows the typical dynamic range of the integrator, measured with

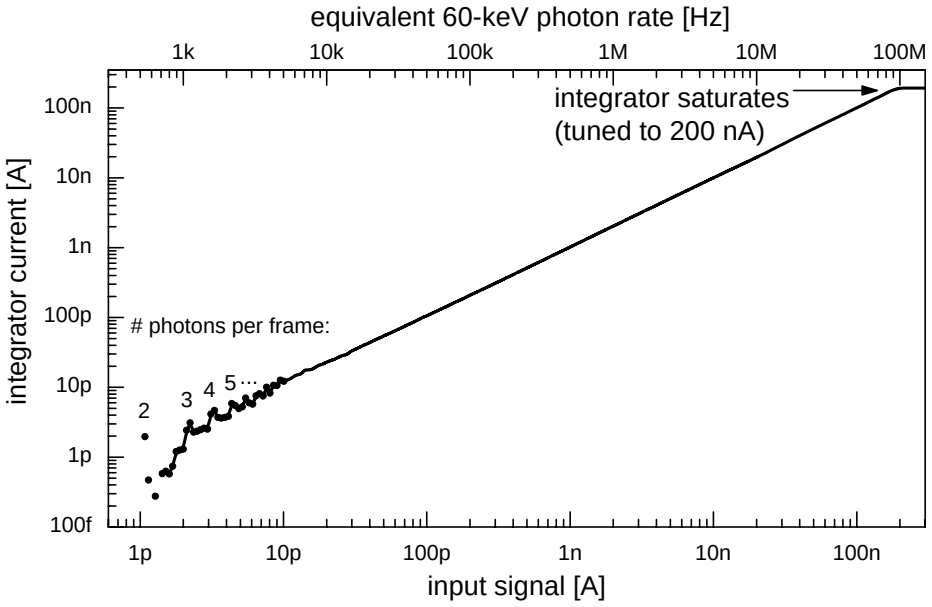

Fig. 5.21: The dynamic range of the integrator covers currents from 2 pA to 200 nA. Measured with equidistant 2.1 fC input pulses and, above 30 nA, with a continuous input current. Note that the artifacts at low input current arise from the quantized nature of the input signal.

pulsed current injection (2.1 fC, equidistant) in the lower current region and with a continuous input current in the range above 30 nA. The upper current limit of 200 nA is given by the integrator clock rate of 20 MHz and the pump size 10 fC of the switched current source charge pump. A frame duration of 2 ms sets the lower integrator current limit to 10 pA (as explained on pg. 32). This limit was, however, removed by a 200 pA offset current introduced by the $IntBiasI$ current source, so that the minimal current is only limited by the signal-to-noise ratio. Note that the wavy pattern visible in the region below 10 pA is an artefact caused by the quantized nature of the input current. In this region, the current consisted of only one to ten charge pulses throughout the frame duration (as noted in Fig. 5.40). A detailed analysis of the integrator noise is given in section 5.3.2.

Adjustability of the Dynamic Range

The upper and lower boundaries of the dynamic range can be shifted by adjustments of the pump size, clock frequency and frame duration. The measurement discussed above is just a typical example. Larger pump packet sizes can shift the upper limit to maximum currents of 1 µA. The lower limit, however, follows accordingly, so that the ratio between maximum and minimal current remains the same. On the other hand, smaller pump sizes allow the measurement of currents down to a few pA, as seen in the measurements presented in Fig. 5.26.

5.3.2 Noise Performance

The noise of the integrator current measurement was determined from the standard deviation of one hundred subsequent measurements of the same input current. Fig. 5.22 shows a measurement of the absolute noise value

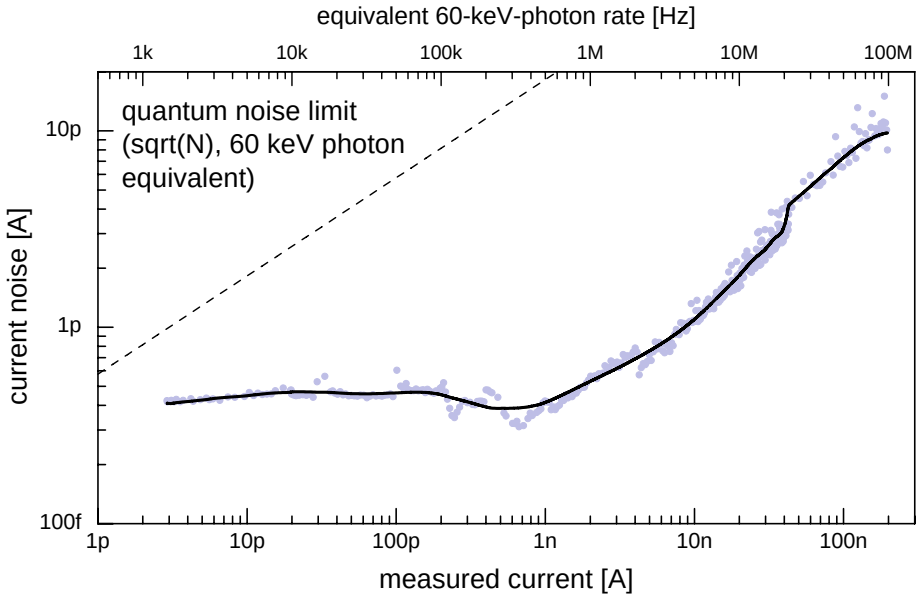

Fig. 5.22: Absolute integrator noise. The input signal is produced by the *ILeakSim* current source, controlled via an external voltage supply and fed directly to the integrator, bypassing the feedback. An additional offset current of 770 pA extends the dynamic range to lower currents and causes the noise floor at 0.4 pA (compare to Fig. 5.25). The dashed line marks the quantum noise limit in a corresponding signal produced by 60 keV X-ray photons.

as a function of the input current, here produced by the *ILeakSim* current source, controlled by an external voltage supply. The current was injected into the integrator, bypassing the preamplifier and feedback circuit. An additional offset current of $IntBiasI = 770$ nA extended the dynamic range

to lower currents. As expected, the noise remains fairly constant (at about 0.4 pA) if the input signal is small compared to the offset current. Larger input current cause an noise increase up to about 10 pA, reached at input currents of 200 nA.
Note that this corresponds to a signal-to-noise ratio of 20,000:1 (see Fig. 5.23). In this example, the precision of discretization was about 1:60,000, given by the 6 ms frame duration and the clock rate of 10 MHz. As can be seen in both figures, the statistical contribution arising from the number fluctuations ($\sqrt{N}$, marked by the dashed line) exceeds the integrator noise by more than an order of magnitude. The integrator noise contribution can thus usually be neglected for X-ray generated input signals.

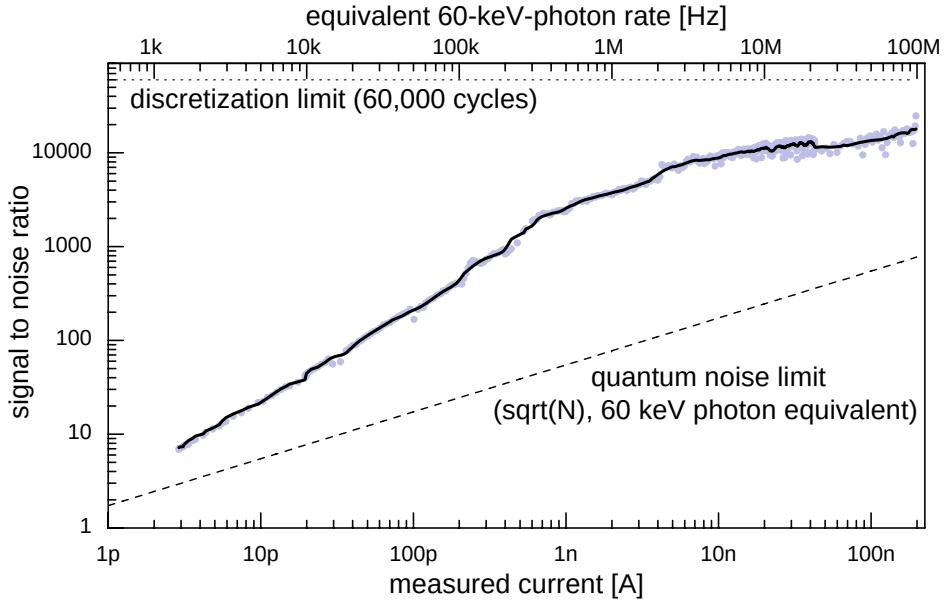

Fig. 5.23: Integrator signal-to-noise ratio as a function of the integrator current. The precision of discretization (dotted line, top) is about 1:60,000 due to the frame duration of 6 ms and the clock rate of 10 MHz. The signal-to-noise ratio is far better than the quantum noise limit for a signal produced by 60 keV photons (dashed line, bottom).

Dependence on Pump Type and Frame Duration

The measured integrator noise depends strongly on the frame duration, since the integration over a longer time interval will produce similar results as averaging several measurements with smaller durations. It also depends on the integrator clock frequency, since higher clock rates will yield a higher precision of discretization if the frame duration is kept constant. The measurements shown in Fig. 5.24 compares the noise performance with

respect to pump type, clock frequency and frame duration. A continuous input current of about 4.7 nA, produced by the *IntBiasI* offset current source, was measured with the different charge pump types at clock rates of 5, 10 and 20 MHz in frames whose duration was varied between 100 µs, 320 µs and 3 ms. For each clock frequency and pump type setting, the pump packet size was chosen for a maximum integrator current of 200 nA.

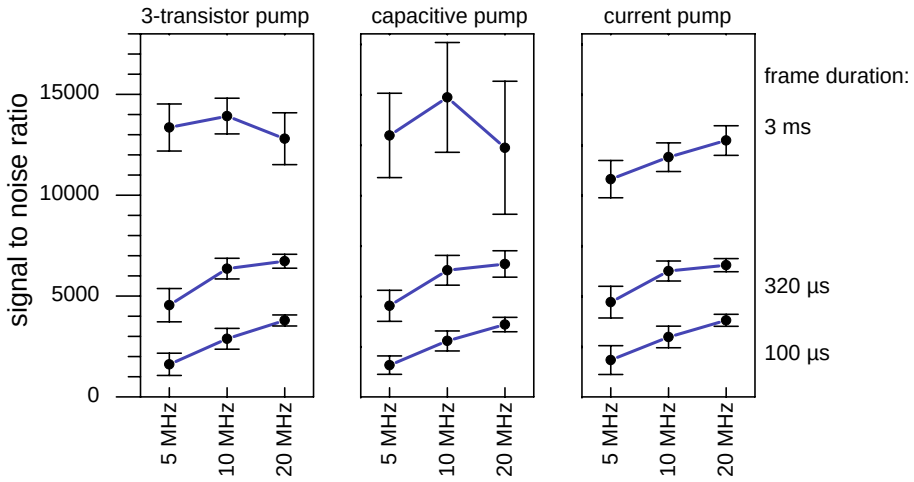

Fig. 5.24: Comparison of the integrator signal-to-noise ratio with respect to pump type, clock frequency and frame duration. The input signal was a 4.7 nA current produced by the *IntBiasI* current source on the integrator input node. The error bars denote the dispersion between the pixels.

The noise performance of the three charge pump types is very similar. In the characterization of the CIX0.1 prototype, it was found that the type of the charge pump influences the noise performance. This could not be confirmed with CIX0.2. A (slightly) better performance of the capacitive pump and the 3-transistor pump type is only seen in the measurements with 3 ms frame duration. However, since these measurements also exhibit a comparably larger dispersion between the pixels, the benefit is not considered significant. As expected, higher integrator clock rates yield better signal-to-noise ratios at the same measurement duration. This increase in system performance is most significant for small measurement durations and clock frequencies. The gain achieved with higher clock rates becomes smaller at higher frequencies. A clock rate of 20 MHz might thus not be worth the additional power consumption compared to a 10 MHz setting.
Note that even short measurements at low clock rates (100 µs, 5 MHz) yield signal-to-noise ratios above 1,500:1. This is far beyond the statistical noise contribution arising from the quantized nature of the input signal, if it was produced by the absorption of X-ray photons. For example, a 4.7 nA input signal produced by 60 keV photons (2 fC per pulse), consists of about

235 pulses within a 100 µs time frame. In this case, both the statistical fluctuation and the expected signal-to-noise ratio compute to $\sqrt{N} \approx 15$.

Minimal Current

The measurement discussed in this section tries to determine the minimal current which is measurable by the integrator. This is achieved by using a minimal pump packet sizes (2.8 fC), so that the $IntBiasI$ offset current necessary to produce two pump events per frame can also be kept to a minimum.

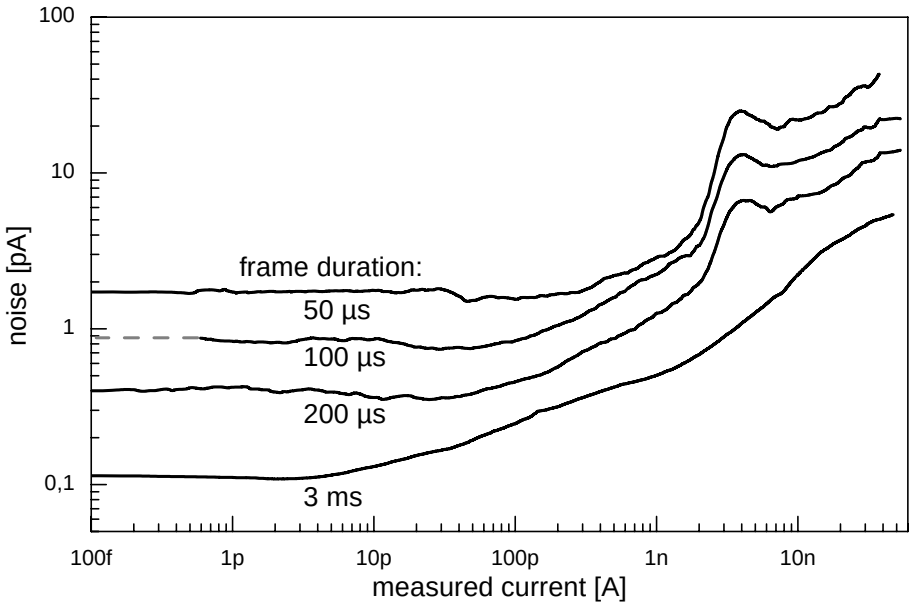

Fig. 5.25: Absolute noise of the integrator using settings aimed at small input signals. A pump packet size of only 2.8 fC allows to use small $IntBiasI$ offset currents. The noise peak in the three topmost measurements was caused by insufficient comparator bias settings.

As can be seen in Fig. 5.25, the absolute noise behaves very similar to the measurement at larger settings (Fig. 5.22). The noise level stays constant for signal currents smaller than the offset current. Different offset currents were chosen to suit the respective measurement durations (50 µs: 110 pA; 100 µs: 55 pA; 200 µs: 30 pA; 3 ms: 3 pA). At around 4 nA, there is a noise peak in the three measurements with small measurement duration. This peak is attributed to insufficient comparator settings, since the measurement with 3 ms duration and significantly larger bias settings does not show such behavior.
The constant absolute noise amplitude in the low current regime translates into a signal-to-noise ratio which is approximately proportional to the current.

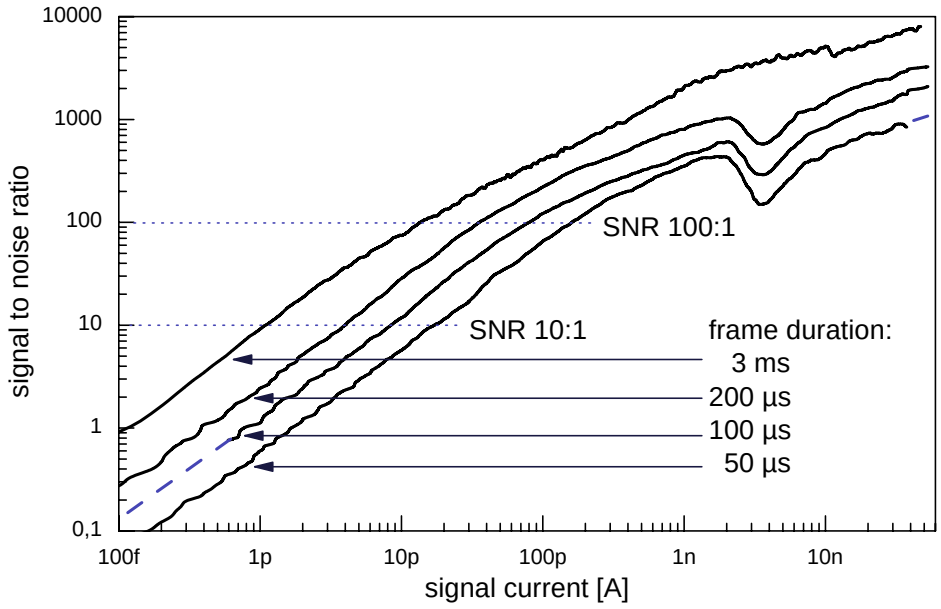

Fig. 5.26: Signal-to-noise ratio plot of the discussed measurement. The constant noise amplitude at small input currents causes the SNR to be proportional to the input current.

This can be seen in Fig. 5.26 and in table 5.2, which summarizes the minimal currents for signal-to-noise ratios of 10:1 and 100:1. The upper current limit at these settings was 56 nA, as would be expected from the product of pump size and the integrator clock frequency of 20 MHz. The minimal current measurable by the integrator at a signal to noise ratio above 10:1 is thus about one pA at 3 ms frame duration. Smaller currents can still be measured if multiple frames are averaged.

frame duration	SNR 10:1	SNR 100:1
50 µs	17 pA	160 pA
100 µs	8.6 pA	80 pA
200 µs	4.0 pA	35 pA
3 ms	1.1 pA	12.5 pA

Tab. 5.2: Minimal currents measurable at the given frame duration as a function of the demanded signal-to-noise ratio (SNR).

Comparison to the Noise Performance of CIX0.1

A comparison of the characterization results of the CIX0.1 prototype to measurements with CIX0.2 at the same clock rate (6 MHz) and frame duration (640 µs) is shown in Fig. 5.27. The new prototype performs similar or better than CIX0.1 throughout its dynamic range. At input currents above 10 nA, the signal-to-noise ratio approaches the discretization limit, denoted by the horizontal line. An additional offset current of 238 pA extends the integrator limit to smaller currents. The band around the CIX0.2 measurement denotes the dispersion of the signal-to-noise ration between the different pixels. The measurements with the CIX0.1 prototype show its performance with the two pump types and sizes. Since the CIX0.1 prototype contained only a very limited number of pixels, the dispersion between is hardly meaningful. Instead, it was chosen to display the standard deviation of a *single* pixel in the band around the measurement. Consequently, the intervals cannot be compared to each other. Both chips show a noise that is far better than the quantum noise which would arise if the input signal was produced by the absorption of X-ray photons.

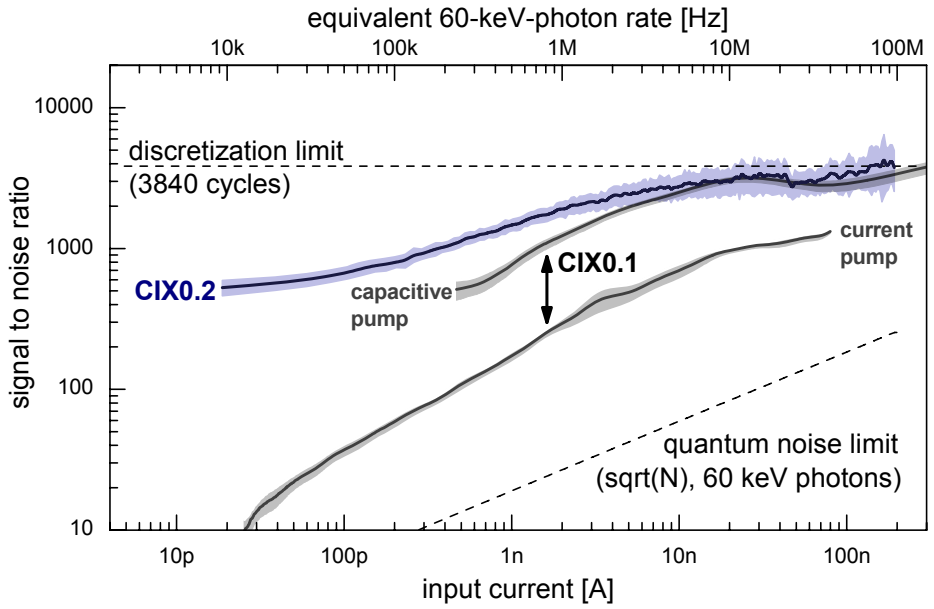

Fig. 5.27: Comparison of the noise performance of CIX0.1 and CIX0.2 at 640 µs measurement duration and 6 MHz integrator clock rate. Two lines illustrate the discretization limits of the integrator and the quantum noise limit for a signal produced by 60 keV photons. In CIX0.2, the noise is independent of the charge pump type.

The improved performance of the new prototype is explained by the separation of digital and analog supply lines in CIX0.2 and by improvements in the charge injection and charge pump circuit designs.

5.4 Feedback Circuit

This section investigates the behavior of the feedback circuit in terms of input signal reproduction, noise, dynamic range, overload behavior and leakage current compensation (l.c.c.).

5.4.1 Signal Reproduction

One of the main tasks of the feedback circuit is to provide a copy of the input signal to the integrator. The differences between original and reproduced signal were investigated by injecting a continuous current into the integrator both via a direct connection and via the feedback circuit. Comparison of both measurements allows to evaluate the reproduction in terms of offset current, noise increase and dynamic range.
Mismatches in the transistors of the differential pairs will generally cause an offset current into or out of the branches of the differential pair. The offset current varies in size and sign between pixels and scales with the bias settings, as can be seen in Fig. 5.28 in a measurement in the absence of input current.

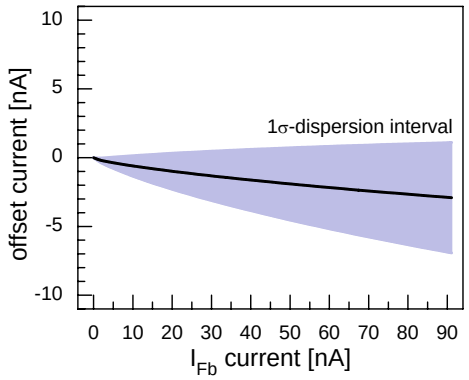

Fig. 5.28: Offset current due to mismatches in the first differential pair. Sign and size of the offset current vary between pixels and scale with the I_{Fb} bias current, as can be seen from the 1σ dispersion interval.

At large bias settings ($I_{Fb} = 91$ nA), the mismatch of the first differential pair alone amounts to -2.9 nA with a dispersion between the pixels of 4.0 nA. In order to allow measurements of the negative current values, the integrator was supplied with an additional current which was sufficiently large to accommodate even the pixel with most negative offset ($IntBiasI = 11.3$ nA). A comparison of the offset currents which arise in the different feedback modes is shown in Fig. 5.29. In order to measure these offsets, both leakage and offset compensation circuits had to be deactivated by setting their respective bias currents to zero. Normally, these offsets are either removed by activating the leakage and offset compensation circuits (discussed in section 5.4.3) or

handled by injecting a sufficient integrator bias current and subtracting the measured offset currents afterwards (*pedestal correction*).

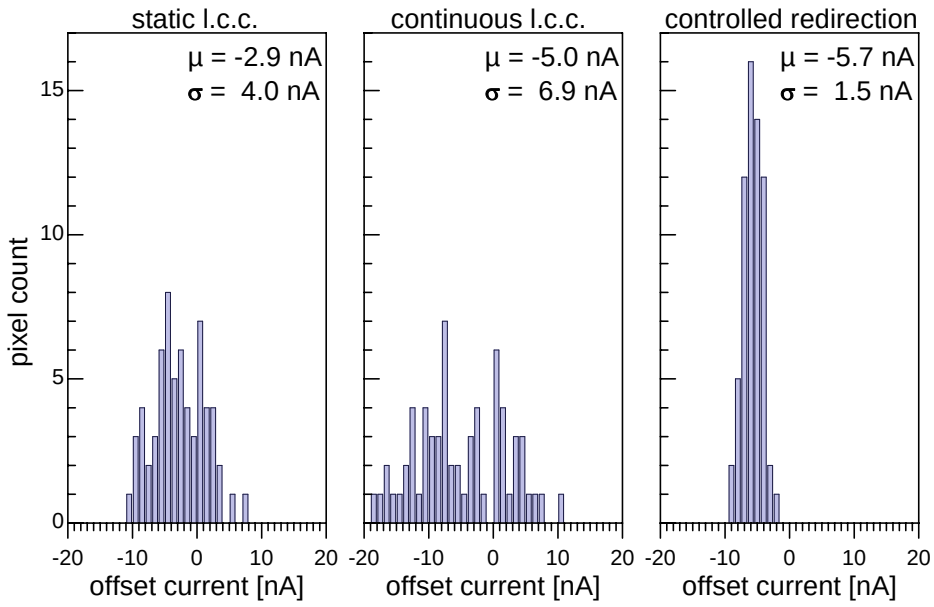

Fig. 5.29: Comparison of the distribution of the offset currents found in the different feedback modes. The mean and standard deviation of the distributions are denoted with μ and σ. No input signal was present in these measurements. The offsets are usually either removed by activating the leakage and offset compensation circuits or by performing an offline pedestal correction.

In all three modes, the offset currents are on average negative and have the same order of magnitude. Continuous leakage current compensation shows a larger dispersion of offset currents in comparison to the static leakage current compensation mode. This is expected since continuous leakage current compensation uses not only an additional differential pair (Fig. 4.15), but also a twice as large bias current in it (discussion of the operation settings follows below). The controlled redirection mode, on the other hand, shows the smallest dispersion, owed to the simplicity of the circuit (Fig. 4.16) and to a comparably small feedback current.
The accuracy of the current reproduction was measured with the leakage simulation current source ($I_{LeakSim}$), whose current is controlled by an external voltage source. Variation of the voltage allowed to generate input currents between a few pA and about 200 nA. For each feedback mode, a suitable set of operation parameters was chosen. Since the performance of the feedback circuit depends strongly on these parameters, the specific settings are briefly discussed:

Static leakage current compensation mode: In order to match the conditions used for high photon count rates, the feedback current was set to

its maximum, i.e. 91 nA. Both integrator and photon counter input potentials were set to 1 V. The actual compensation was deactivated by setting the bias current of the second differential pair to zero.

Continuous leakage current compensation: The largest possible input current is determined in this mode by the strength of the second differential pair. $I_{LeakComp}$ was hence set to its maximum of 180 nA. For better comparability to the similar *controlled redirection* feedback mode, an I_{Fb} current of 23 nA was chosen. Like before, both input potentials were set to 1 V. The large dispersion in the offset currents required a higher integrator bias current.

Controlled redirection: This mode requires a difference in the input potentials to function properly. V_{IntRef} was thus set to 1.4 V while $V_{CountRef}$ remained at 1.0 V. Furthermore, the redirection transistor (see Fig. 4.16) should be biased with some leakage current. This was accomplished by injecting about 2.7 nA with the $I_{CurrInj}$ current source, which is normally used for the current chopper. The second differential pair was turned off, the first pair was biased moderately ($I_{Fb} = 23$ nA).

The result of these measurements can be seen in Fig. 5.30, which shows the discrepancy between original current and its replication (pedestal-corrected). Fig. 5.31 shows a different view of the same data set by expressing the discrepancy in percents of the signal current. This allows a better investigation of the behavior at small signals.
The measurement with static leakage current compensation (left) allows to evaluate the impact of activation of bypass transistor. This occurs when the input signal exceeds the maximum current the feedback circuit can compensate (here: about 35 nA[3]). As can be seen in the left graph by comparison to the dashed lines, the mismatch caused by the activation amounts to less than 1% of the signal current or about 350 pA maximum on average. The implementation of the bypass transistor can therefore be considered a viable approach for directing the signal current to the integrator in case of a photon counter overload.
The current replicated by the continuous leakage current compensation mode shows a deviation from the original which remains fairly constant throughout its dynamic range at about one percent. At about 80 nA, the upper end of the dynamic range, a sharp signal loss can be seen in the middle graph of Fig. 5.31. At this point, the second differential pair (Fig. 4.15) is in a state of maximum imbalance. Additional current can still be compensated by the first feedback pair. It does, however, not show up in the integrator, because the second differential pair already delivers its maximum. The bypass transistor,

[3]The bias current of 91 nA allows the delivery of currents up to 45 nA. Up to 10 nA are lost due to in the pixels individual offset, leaving a remaining maximum compensatable current of 35 nA.

conceptually used exclusively in static leakage current compensation mode, will open up only if the signal current also exceeds the limit of the first differential pair. The I_{Fb} dependent signal loss due to the first differential pair is, however, also retained at larger currents. This is the reason why such signal intensities must be considered to lie outside the valid operation range for this feedback mode. A measurement demonstrating this behavior is shown in Fig. 5.32.

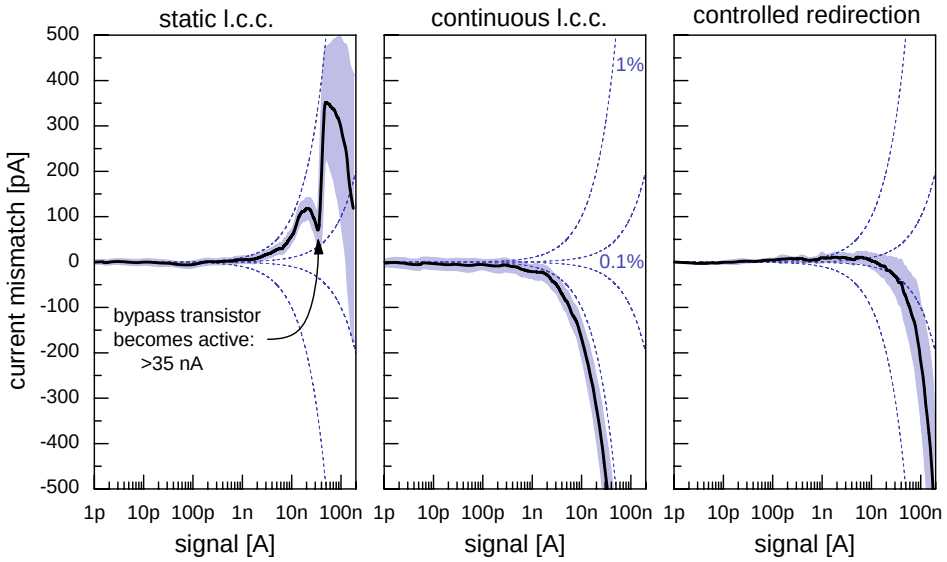

Fig. 5.30: Current mismatch between original current and its replication (pedestal-corrected) as a function of the input signal. The area around the black line shows the standard deviation of the dispersion between the pixels. Dashed lines mark a mismatch corresponding to 1% and 0.1% of the input signal. The measurement with static leakage current compensation (left) shows that the mismatch caused by the activation of the bypass transistor amounts to less than 1% of the signal current. The dynamic range of the continuous l.c.c. mode is limited to 80 nA. As the signal approaches this limit, the replicated current deviates from the original by about 1%. The controlled redirection mode shows the least deviation, especially at large signal currents, where the signal stays within a few tenths of a percent of the original.

The controlled redirection mode shows the least deviation, especially at large signal currents, where the signal stays within a few tenths of a percent of the original. Yet even at small signals, the deviations are smaller than those found in the other modes.

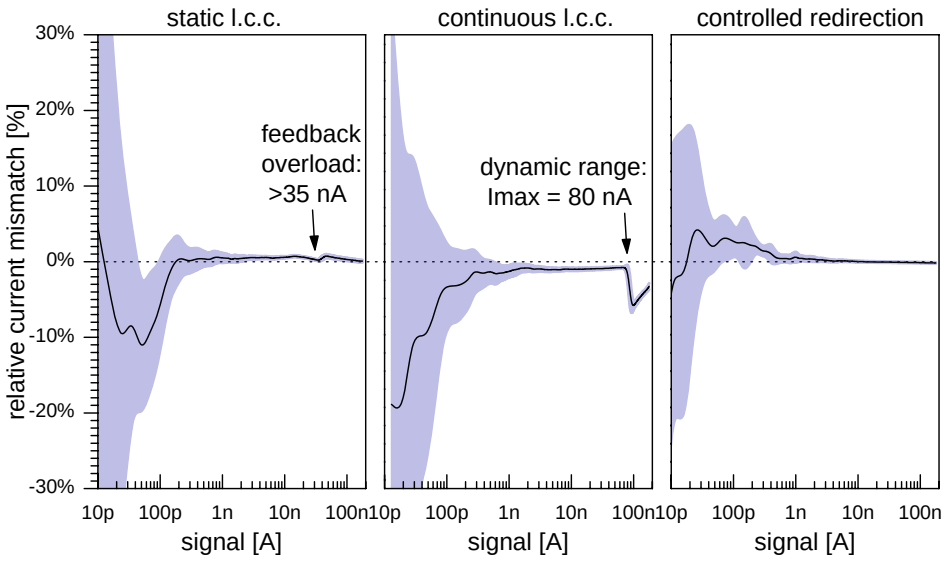

Fig. 5.31: Relative mismatch between the original current and its replication, expressed in percent of the signal current. The area around the measurement marks the 1σ dispersion interval. Visible features include: the (small) impact of the bypass transistor when it becomes active due to feedback overload in the static l.c.c. mode (left), the 1% mismatch of the current delivered by the continuous l.c.c. mode and the limit of this mode's dynamic range (middle). A consistently good current matching for signals larger than a few hundred pA is visible in the controlled redirection mode (right). The large deviations seen at small signals in all three measurements are attributed to fluctuations in the comparably large offset- and bias currents.

5.4.2 Feedback Noise Performance (Continuous Currents)

The measurements of the signal reproduction discussed in the previous section also allow to evaluate the impact of the different feedback modes on the integrator noise performance. Fig. 5.33 shows the noise in terms of absolute value and signal-to-noise ratio. All measurements used a frame duration of 6 ms at an integrator clock rate of 10 MHz. Since data acquisition was performed during the subsequent measurements, the noise measurements contain an additional contribution due to digital-to-analog crosstalk (see section 5.6.4). The measured noise values might thus improve slightly if the subsequent measurement is delayed until the data acquisition is complete.
At currents below 30 nA, the measured noise is almost constant. This is mostly due to the comparably large integrator bias currents which are necessary to accommodate the current offsets. As expected, the lowest noise level is found in the measurement with direct injection (1.6 pA, curve *d*). The controlled redirection configuration has the smallest noise of the feedback

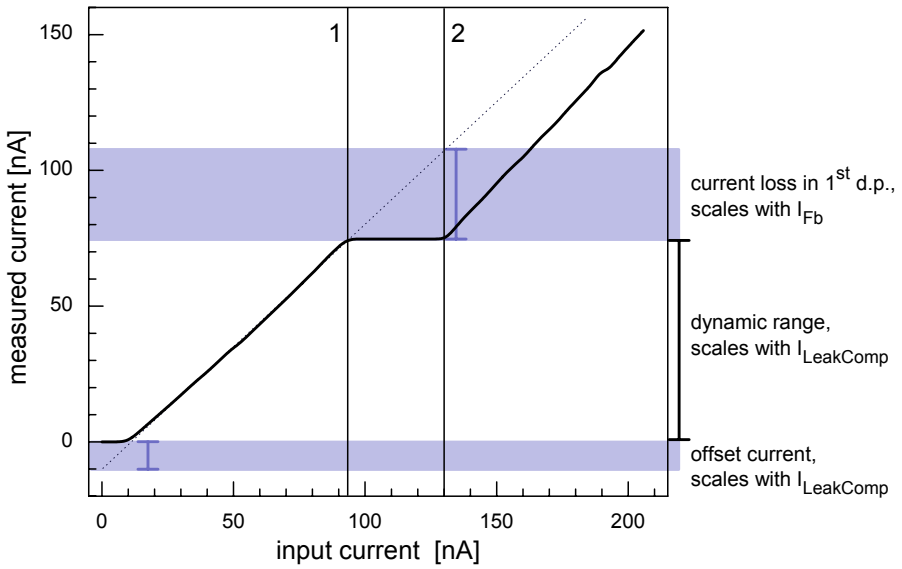

Fig. 5.32: Typical measurement of the current produced by the feedback circuit in continuous leakage current compensation mode as a function of the input current. The offset current and the dynamic range are visible on the left side. Both are determined by the bias current $I_{LeakComp}$ in the second differential pair (Fig. 4.15). Point 1 marks the maximum input current up to which the feedback operates correctly. It is followed by a region in which the first differential pair still compensates the input current, but no additional current is delivered to the integrator. This causes increasing current loss until the first differential pair also becomes insufficient (point 2), determined by I_{Fb}. Beyond this point, the bypass transistor becomes active so that the surplus current reaches the integrator. Since the current loss is retained, this feedback mode can only operate up to point 1.

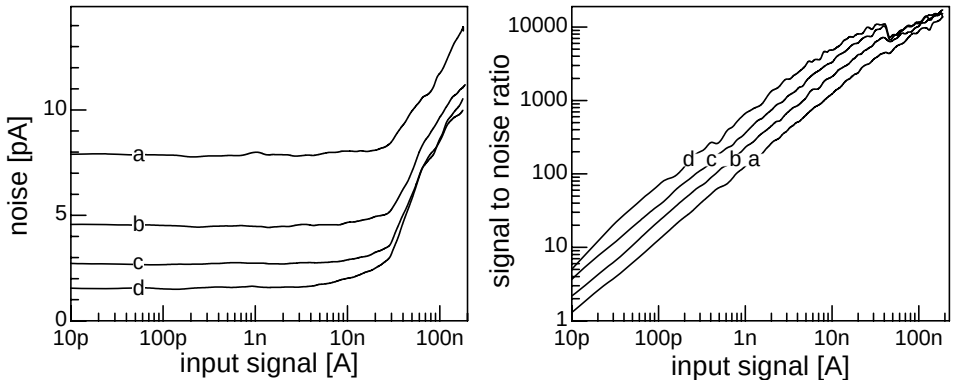

Fig. 5.33: Comparison of the integrator noise at the different feedback modes. a) Continuous leakage current compensation, b) static leakage current compensation c) controlled redirection d) direct injection (=reference).

modes (2.7 pA, curve *c*). At signals beyond 30 nA, its noise performance is almost identical to the original. The static leakage current compensation feedback mode exhibits a noise level of about 4.5 nA (curve *b*). The largest noise (7.8 pA, curve *a*) occurs in the continuous leakage current compensation mode. This is expected, since this feedback mode features both large bias currents and noise contributions from two differential pairs.
The plots of the signal-to-noise ratio in Fig. 5.33 also exhibit a negative dent in the top right corner. This dent corresponds to the steep noise increase which is also seen in the left plot, above 30 nA. Even though most pronounced in the direct injection measurement (d), the increase is visible in all four measurements. Noise measurements with pulse charge injection do not show such a behavior. The noise increase is thus suspected to arise from automatic range switching in the external voltage source controlling the input signal rather than from the chip itself.

5.4.3 Leakage Compensation

The measurements discussed in section 5.4.1 showed that the offset currents caused by the feedback circuit reach values of up to 10-20 nA. Even without electronic compensation mechanisms, these offsets can be handled by injecting a sufficiently large bias current into the integrator and performing an offline pedestal correction. Yet this method also has an adverse effect on the usable dynamic range of the integrator. In the continuous leakage current compensation mode, for example, the lowest offset current is -19 nA while the highest offset is +11 nA (see Fig. 5.29, center). Injecting an appropriate bias current of about 20 nA into the integrator will ensure valid measurements in all pixels. The integrator of the pixel with the highest offset, however, will see a current of 31 nA even in the absence of an actual input signal. This is a severe restriction of the dynamic range, as can be seen by comparing the dynamic range measurement shown in Fig. 5.21. Large currents also mean that the information recorded by the time counter is barely relevant. Its value will always be close to the frame duration. The additional layout area and power consumption compared to a simpler integrator counting only charge packets would thus be wasted in many pixels. In order to use the integrator in the way it is designed for, both leakage and offset currents must be removed electronically.
The effect of the leakage/offset compensation mechanism can be seen in Fig. 5.34. This measurement was performed in static leakage compensation mode. Opposed to the measurement discussed in section 5.4.1, the second differential pair was actually activated by supplying it with a bias current of 180 nA. As can be seen in the left plot, this reduced the average offset current by a factor of 500 from -2900 pA to -5.9 pA. The dispersion between the pixels also sank from 4000 pA to 31.5 pA.

The remaining average offset current depends on the voltage difference between the input nodes of photon counter and integrator, as can be seen in the right hand plot of Fig. 5.34. At an integrator input voltage of about 1,000 mV, the best matching is obtained at $V_{CountRef} = 986$ mV.

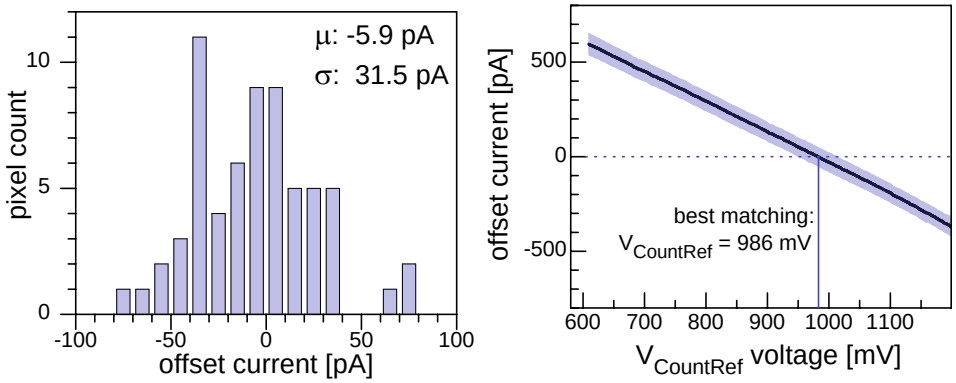

Fig. 5.34: Left: Offset currents of the feedback circuit with activated (static) leakage compensation. Compared to a measurement with deactivated compensation, the average offset is reduced by a factor of 500 and the dispersion sinks from 4,000 pA to 31.5 pA. Right: The average offset current depends on the input potentials of photon counter ($V_{CountRef}$) and integrator ($V_{IntRef} \approx 1$ V). Best matching is obtained at $V_{CountRef} = 986$ mV. The area around the measurement marks the 1σ dispersion interval.

The offset compensation in the other two feedback modes is provided by the offset current compensation circuit in the integrator. This circuit delivers results similar to those of the second differential pair in case of the static leakage current compensation. There is, however, a design flaw in CIX0.2 which often makes the usage of the offset correction unfeasible: the integrator bias current source does not feature a switch which would allow fast disconnection during the offset sampling. The offset compensation will thus also remove the bias current, so that the user can only choose either offset correction or extension of the dynamic range to smaller currents. A work-around for this limitation is to use the current chopper to inject an additional current during the measurement frame.

Range of Compensatable Leakage/Offset Currents

The maximum current which can be compensated (offset and/or leakage) is determined by the bias settings of the second differential pair and the offset correction circuit. It is thus identical to the dynamic range of the continuous leakage current compensation mode (i.e. 80 nA), since both are limited by the current in the second differential pair.

Accuracy of Compensation

Even within the range of compensatable currents, the amplitude of the current which remains after sampling is not exactly zero. Instead, there is a minor dependency on the bias setting of the compensation circuit and on the strength of the original current. The measurement in Fig. 5.35 shows the current remaining after compensation as a function of the original current. Up to currents of about 40 nA, the curve is approximately linear with a slope of (4.79 ± 0.01) pA/nA. In other words, the compensation circuit removes about 99.5% of the leakage current. Currents above 80 nA cannot be fully compensated. A similar measurement with a small leakage current and a variation of the compensation bias setting shows a negative slope of -0.4%.

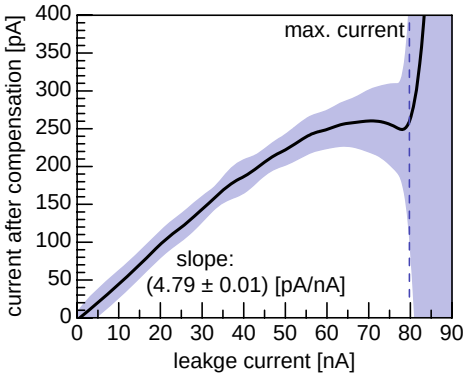

Fig. 5.35: The current remaining after leakage/offset compensation shows a minor dependence (note the different scales) on the original leakage current (+0.479 percent). A similar dependence exists with regard to the bias current of the compensation circuit (-0.4 percent). The area around the measurement denotes the 1σ dispersion interval, the dashed line marks the maximum current that can be compensated.

Sampling Noise

Each sampling phase consists of a settling interval for the voltage on the sampling capacitor, followed by a switching step which freezes the potential. Both steps introduce some noise, so that the current delivered by the compensation circuit is slightly different each time the leakage current is sampled. A measurement of this noise as a function of the leakage current is displayed in Fig. 5.36. In this measurement, the bias settings were chosen smaller (and more realistically) than in Fig. 5.35, which leads to a maximum compensatable current of about 24 nA. The noise varies between 100 pA and about 10 pA. Best values are achieved if the maximum compensatable current exceeds the leakage current only slightly. This result is also found at

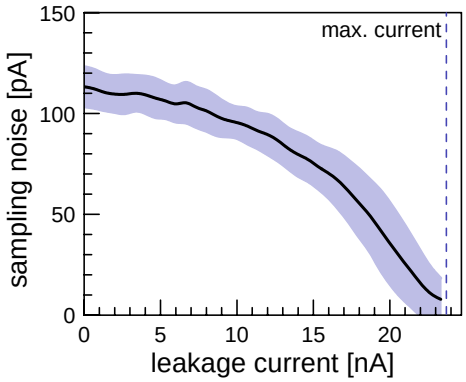

Fig. 5.36: The sampling step causes an additional noise contribution, which depends on the relative sizes of leakage current and compensation bias settings. Bias settings slightly above the leakage current produce least noise. The area around the measurement denotes the 1σ dispersion interval.

other bias currents. The bias settings for the compensation circuits should thus be chosen as small as possible.

Long-Term Stability of the Compensation Current

The intensity of the current delivered by the compensation circuit depends on the voltage stored on the sampling capacitor C_A (see Fig. 4.12). For long-term stability it is thus necessary that this voltage stays as constant as possible. Since the gate leakage current in the AMS 0.35 micron-technology is negligible, the major source for a decay of the sampled voltage is the switch disconnecting the sampling capacitor (switch A in Fig. 4.12). In CIX0.2, the precautions taken in the design of this switch turned out to be insufficient. The compensation current sinks typically by about 200 pA per second. In measurements lasting a few hundredths of a second, this change in current is usually irrelevant. On the other hand, measurement series over several seconds or minutes without the possibility of intertwined sampling phases are seriously impaired. Such conditions are typical for example in measurements with an actual X-ray tube.
A simplified diagram of the sampling switch is shown in Fig. 5.37 (a). It connects the input node 1 (right side), coming from the first differential pair, to the right gate of the second differential pair (on the left). On the left side, there is also the sampling capacitor C_A, which uses the gate capacitance of a large transistor. Switching is performed by the signal *Sampleb*[4]. The current leaking through the switch transistors has two contributions: current into the bulk of the transistor and current between source and drain. The circuit tries to minimize both. A 100 fC capacitor between the transistors buffers

[4] *Sampleb* is the inverted line of the differential *Sample* signal.

the voltage during the sampling step, so that the drain-source potential of the left transistor should ideally be zero. Since the transistors are p-type, their bulk leakage current can be controlled trough the voltage applied to their n-well. In CIX0.2, this potential can be controlled either externally using the V_{nwell} reference voltage, or internally with a buffer element which sets the bulk potential to the voltage stored on C_A. There is still, however, the leakage current in the right transistor, which has both a non-zero drain-source potential (node 1 is connected to V_{IntRef} during measurements) and a n-well potential which is significantly larger than the voltage on the buffering capacitor.

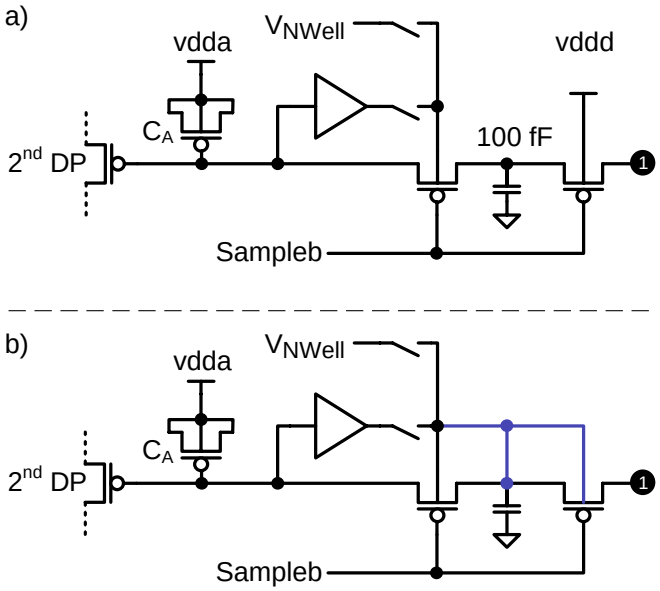

Fig. 5.37: Simplified circuit diagram of the sampling switch (i.e. switch A in Fig. 4.12), which connects the input (node 1, right) with the sampling capacitor and the right gate of the second differential pair (left). a) Design as implemented in CIX0.1. b) suggested design change.

On a next iteration of the CIX chip, the leakage-tightness of the sampling switch could be improved with a slight modification to the design, which already achieved good results on the *MPEC* X-ray imaging chip (a counting imaging chip previously designed in our working group) [9]. As can be seen in diagram (b) in Fig. 5.37, the only difference are the additional connections of the buffer element to the n-well of the right transistor and to the node between both transistors. This prevents the deterioration of the potential on the buffer capacitor. Note that since the n-well potential must always be higher than the source and drain potentials, it might be advisable to leave the n-well potential of the right hand transistor connected to *vddd*. Sampled voltages below V_{IntRef} might otherwise attract current from node 1.

5.5 Simultaneous Photon Counting and Integration

This section discusses the performance of the CIX chip in measurements with simultaneous photon counting and integration. The usage of pulsed input signals allows to investigate the correlation between photon counter and integrator measurements. It also allows to determine the energy resolution of the reconstructed average pulse size/mean photon energy. The section will conclude with a discussion of measurements with polychromatic input signals whose energy distribution approximates actual X-ray spectra.

5.5.1 Observability of Fluctuations in the Photon Flux

A prerequisite for the successful measurement of the average pulse height of an input signal is that fluctuations in the number of photons in the input signal produce correlated fluctuations in the photon count rate and in the current measurements. This requirement has been investigated in the measurement shown in Fig. 5.38. The input signal consisted of 2 fC input pulses with Poisson-distributed pulse spacings at different average frequencies.

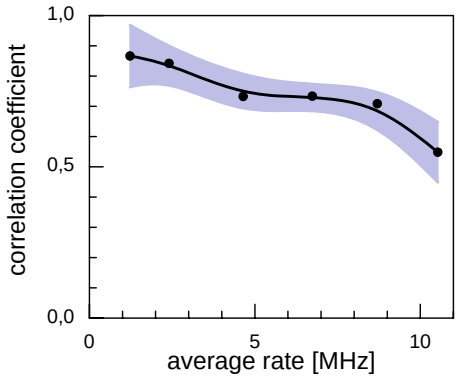

Fig. 5.38: The correlation between the fluctuations in photon counter and integrator measurements identifies quantum fluctuations in the input signal. Increased pile-up of the Poisson-distributed input pulses at higher photon rates decreases this correlation. The area around the measurement marks the 1σ dispersion interval.

The correlation coefficient decreases at higher photon rates, which is expected due to the increased pileup and the corresponding loss in count efficiency as discussed in section 5.2.9. A second effect of the pileup is that on average, pixels with a smaller individual pulse size show a stronger correlation. The original measurements of a typical pixel and the best performing pixel are shown in Fig. 5.39.

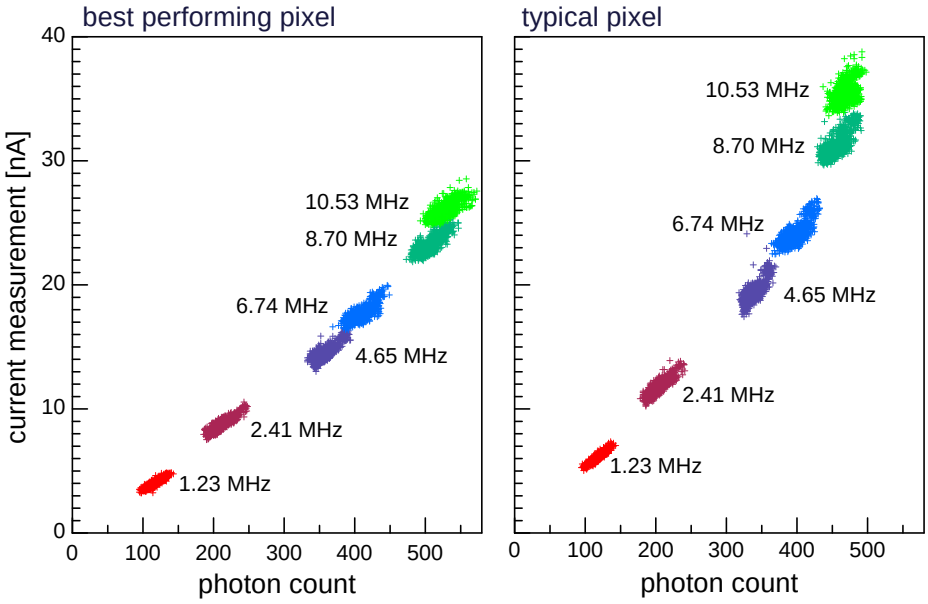

Fig. 5.39: Comparison of the correlation measurements in the best performing pixel and in a typical pixel. At each frequency, 100 measurements were recorded. The number fluctuations in the random input signal cause correlated fluctuation in the photon count and in the integrator measurements. The degree of correlation decreases with increasing photon rate. Pixels with a smaller individual pulse size show a stronger correlation due to a smaller chance for pileup. This can be seen in the measurement of the best performing pixel (smallest pulse size, higher correlation at larger pulse rates).

5.5.2 Dynamic Range and Energy Resolution

This section investigates the combined dynamic range and the energy resolution of a CIX pixel in simultaneous counting and integration mode. Both properties were determined from a measurement with an input signal consisting of equidistant 2.1 fC charge pulses whose frequency was varied from 500 Hz to 20 MHz. Signals beyond the count rate limit of the photon counter were generated with a constant current source. This allowed to deliver currents to the integrator up to and beyond its maximum current. Table 5.3 summarizes the used operation parameters.
With these settings, the CIX pixel covers a total dynamic range from about 1 pA to 200 nA, equivalent to rates of 60 keV photons between 500 Hz and 95 MHz. This can be seen in Fig. 5.40. The photon counter handles photon rates up to about 12 MHz, equivalent to a current of 25.2 nA. At smaller frequencies, all pixels achieve 100% count efficiency. The integrator can measure currents up to the chosen maximum of 200 nA (equivalent to a photon rate of about 95 MHz). In the low current regime, the current measurement becomes increasingly noise dominated, as can be seen from the 1σ noise

property	setting
input signal	2.1 fC (13,000 e$^-$, 60.4 keV photons)
	> 30 nA: constant current source
pulse spacing	equidistant
photon counter threshold	1.12 fC (7,000 e$^-$, 32.5 keV)
integrator clock	20 MHz
frame duration	2 ms (40,000 clock cycles)
pump type	switched current source
pump packet size	10 fC (62,400 e$^-$)
feedback mode	static leakage current compensation
feedback bias current	$I_{Fb} = 91$ nA
compensation bias current	$I_{LeakComp} = 29$ nA

Tab. 5.3: Operation parameters for the measurement of the combined dynamic range and the energy resolution in simultaneous counting and integration mode.

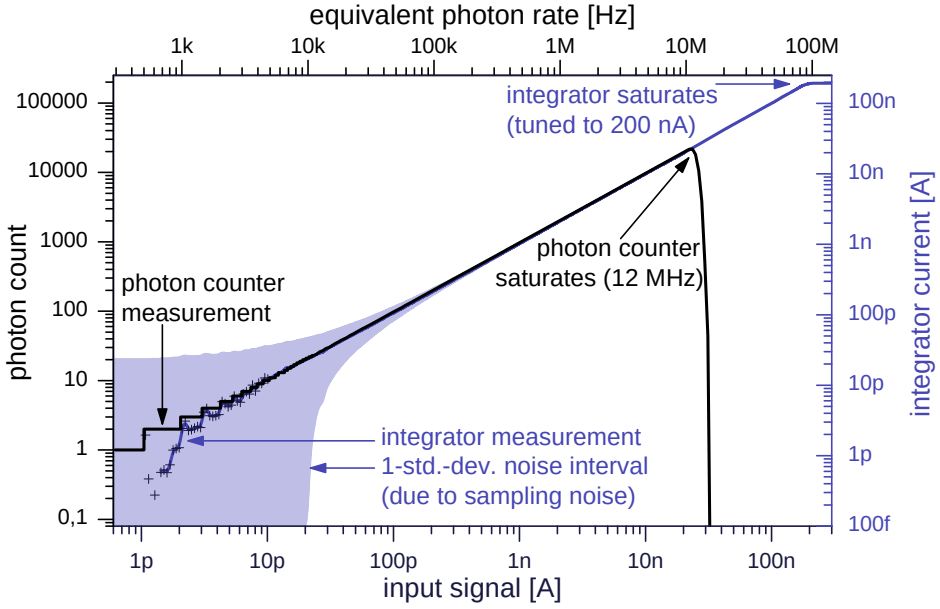

Fig. 5.40: The combined dynamic range of photon counter and integrator covers signals from about 1 pA up to 200 nA. In the high signal regime, the photon counter saturates at about 12 MHz, while the integrator measures currents up to the chosen value of 200 nA. At small input signals, the integrator noise, marked by the interval around the measurement, becomes dominant. The integrator noise is mainly caused by the sampling step before every measurement. It retains a constant value of (23.6 ± 3.4) pA throughout the dynamic range.

interval. Note that in this graph, the interval around the measurement does *not* denote the dispersion between the pixels but the average noise of their current measurements. The noise is dominated by the contribution from the sampling step and retains a constant amplitude of (23.6 ± 3.4) pA throughout the dynamic range. As was already mentioned in section 5.3.1, the wavy pattern visible in the integrator measurement at currents below 10 pA is an artefact caused by the quantized nature of the input current. The same measurement was already used there to demonstrate the dynamic range of the integrator itself.

Pulse Size Calibration

The pulse size was calibrated by measuring the current produced by a stream of equidistant input pulses injected directly into the integrator at a pulse rate of 1 MHz. This calibration can be compared to the pulse size reconstructed from the simultaneous photon counter and integrator measurements in response to the same input signal. As can be seen in Fig. 5.41, the reconstructed pulse size matches its calibration. This result is not unexpected, since the photon counter achieves 100% count efficiency and the feedback was already shown in section 5.4.1 to reproduce currents accurately when using leakage/offset compensation and pedestal correction.

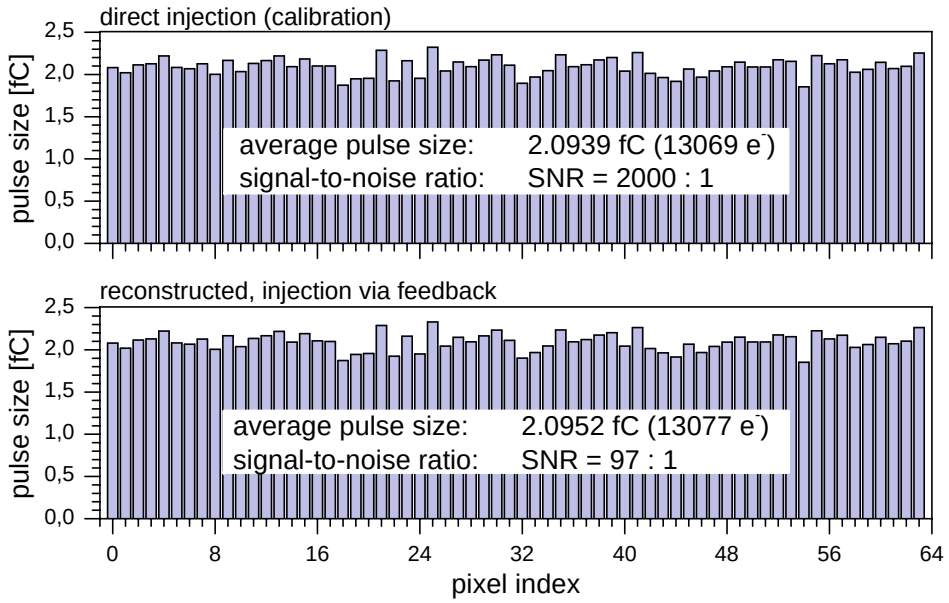

Fig. 5.41: Comparison of calibrated pulse size and the pulse size reconstructed from simultaneous photon counter and integrator measurements. Due to 100% count efficiency and accurate current reproduction, the pulse sizes match. The feedback, however, reduces the signal-to-noise ratio by a factor of 20.

The impact of the feedback circuit is, however, visible in the difference in the signal-to-noise ratio, which is reduced from 2,000:1 to 97:1. To set this value into perspective, note that a similar signal with Poisson-distributed pulse spacings will be limited by quantum fluctuations to a signal-to-noise ratio of $\sqrt{2000} \approx 44 : 1$.

Spectral Information: Pulse Size Reconstruction

Fig. 5.42 shows the average pulse size (i.e. the mean photon energy) which was reconstructed from the count rate and current measurements in Fig. 5.40 like explained in the introduction of chapter 4. As can be seen from the interval around the measurement, the average integrator noise (and thus the noise in the pulse size measurement) becomes dominant at signals below about 100 pA. Even though a single measurement in this range will not produce a reliable value, the average of multiple measurements does still yield sensible results down to currents of about 20 pA. At large input signals, the pulse size is overestimated due to the breakdown of the count efficiency caused by the saturation of the photon counter. As a function of the pulse rate, the measured pulse size shows slight deviations from the calibrated value (denoted by the dashed line). Independent pulse size measurements with threshold scans (noted by the crosses), however, confirm that this deviation is caused by variations in the input pulse size rather than by inaccuracies in the measurement.

Spectral Resolution

Two input signals with different average pulse sizes can be distinguished from each other if the difference in their pulse size measurements is large compared to the noise of the measurement. The width of the interval shown in Fig. 5.42 can thus be used as a measure for the spectral resolution of the CIX pixel. A plot of this width as a function of the input signal is shown in Fig. 5.43.
The pulse size can be measured with a signal-to-noise ratio better than 10:1 in the range between 250 pA and 25 nA, corresponding to 60 keV-photon rates between 120 kHz and 12 MHz. The form of the curve matches the expected shape for a measurement with signal independent noise in the current measurement, 100% count efficiency and a photon counter saturation frequency of 12 MHz.

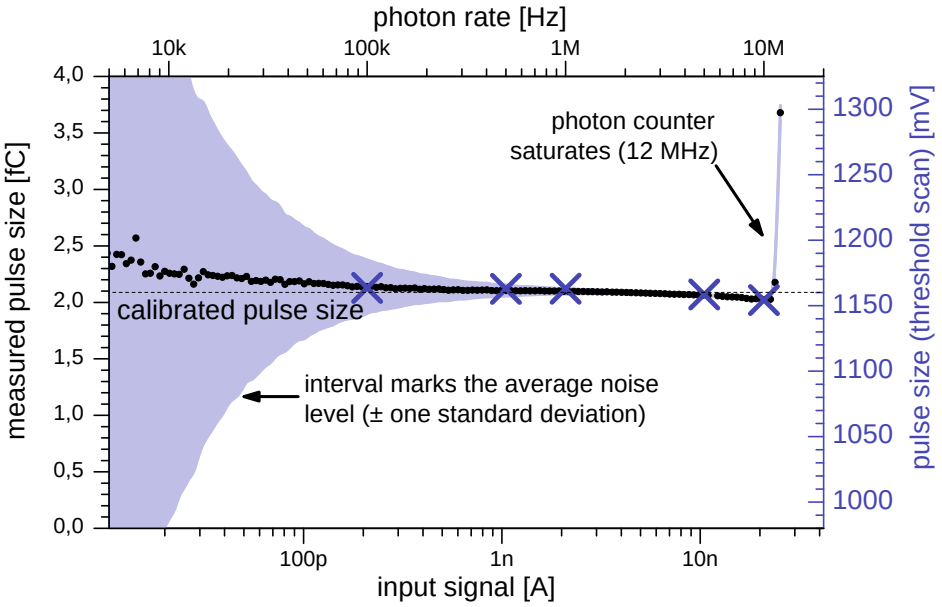

Fig. 5.42: Average pulse size, reconstructed from photon counter and integrator measurements. At low frequencies, the measurement becomes dominated by the noise in the current measurement. Sensible results can still be obtained by averaging multiple measurements. The deviations of the measured pulse size from the calibrated value (dashed line) are due to variations in the input pulse size, as is confirmed by independent threshold scans (cross marks, right scale).

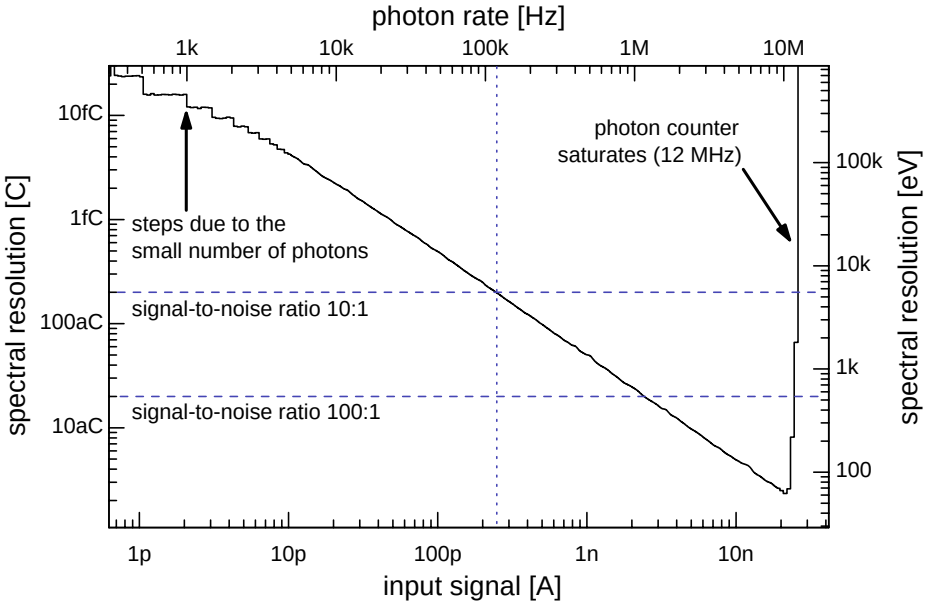

Fig. 5.43: Spectral resolution of the pulse size measurement as a function of input frequency. The noise in the pulse size measurement lies below 10% from 250 pA (120 kHz, marked by the dotted line) to 25 nA (12 MHz).

5.5.3 Spectral Hardening

One of the most interesting questions for the evaluation of the signal processing concept is, to what extend it will be able to provide information about spectral hardening in an actual X-ray spectrum. This was investigated with an input signal which simulates the transmission spectra of a 90 kVp X-ray tube after passing through different absorber materials (Fig. 5.44). In this case, the first absorber was a copper sheet of 0.5 mm thickness, while the second absorber was 11.6 mm aluminium. Due to its higher atomic number, the copper absorber transmits an X-ray beam with a more pronounced spectral hardening. The simulation also took into account the thickness and material of the conversion layer, which was 1 mm of CdZnTe. Both signals were normalized to a photon rate of 250 kHz, which corresponds to an initial incident flux of 7.3 million photons/(mm^2 s) for Cu and to 6.8 million photons/(mm^2 s) for Al. The threshold was set to a photon-energy-equivalent of about 12 keV.

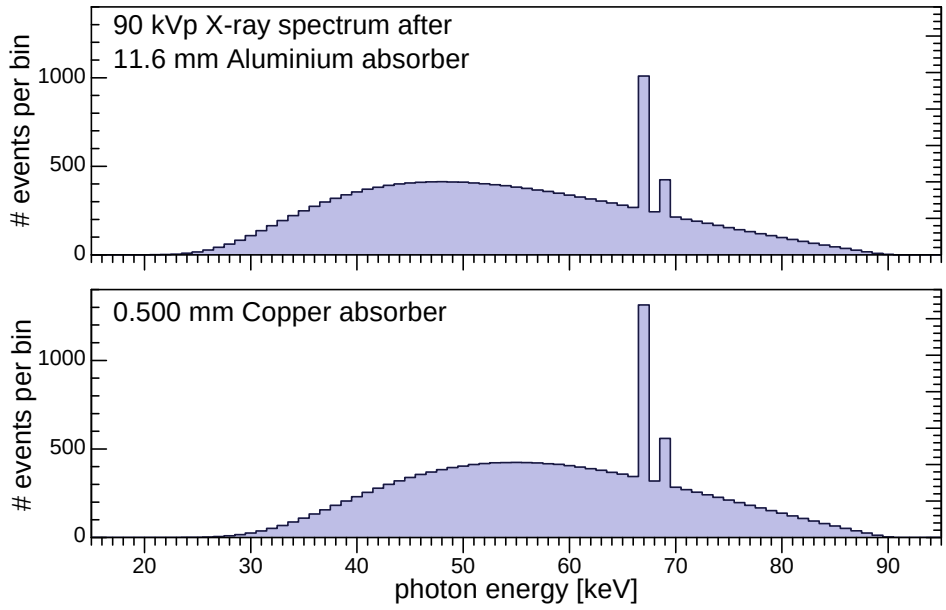

Fig. 5.44: Computed transmission spectra of a 90 kVp X-ray beam passing through 11.6 mm Al absorber (top) and 0.5 mm Cu absorber (bottom). The higher atomic number of copper causes a stronger spectral hardening of the transmitted X-ray beam. Both spectra are discretized into 1 keV bins and normalized to 16,250 events, corresponding to 250 kHz photon rate and a measurement duration of 65 ms.

Method

The input signal was produced by providing a sequence of digital strobe signals to the current chopper as described in section 5.2.8. Different photon energies were simulated by varying the duration of the strobe pulses. A calibration beforehand determined the corresponding photon energy for the set of available trigger durations between 1 and 30 ns (vertical lines in Fig. 5.45). The computed spectra behind the copper and aluminium absorbers were mapped to the set of producible photon energies by distributing the photon flux in each keV-bin to the two neighboring discretization points in a way which conserved both the total flux and the total energy. The resulting mapping is plotted in Fig. 5.45.

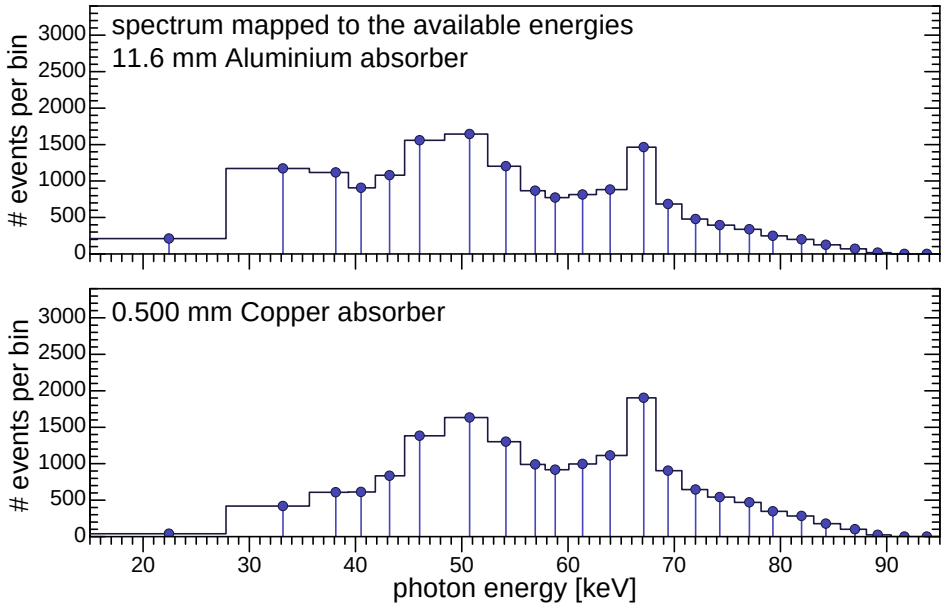

Fig. 5.45: The transmission spectra in Fig. 5.44 are mapped to the set of photon energies producible by the current chopper (vertical lines). The resulting spectrum conserves both the average flux and the average energy. Based on these spectra, a Monte-Carlo algorithm subsequently generated a 65 ms random pattern with Poisson-distributed pulse spacings. This bit pattern was used to trigger the current chopper, thereby producing input signals resembling those of an actual sensor.

Since the producible energies are not spaced evenly, the discretization points covering a larger energy range are assigned a higher flux. This ensures that the total flux in those energy regions matches the computed spectrum. A Monte-Carlo generator converted the discretized spectrum to a 65 ms random pattern with Poisson-distributed pulse spacings. Pulses of higher energy correspond to strobe signals of longer duration. The pulse count at each energy level matches the distribution of the mapped spectrum. This bit

pattern was used to trigger the current chopper, thereby producing input signals resembling those of an actual sensor. An illustration of such a strobe pattern is displayed in Fig. 5.46.

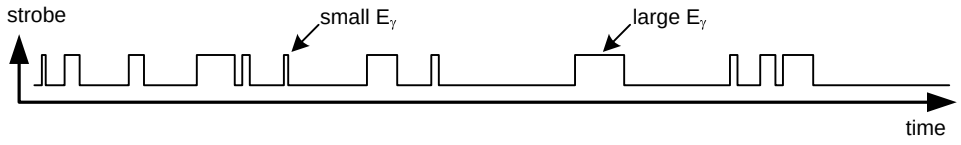

Fig. 5.46: Illustration of the random bit pattern generated based on the mapped transmission spectra. Longer strobe durations produce more energetic pulses. The resulting signals resemble true X-ray signals with respect to randomness, energy distribution and photon rate.

Since the pulse generator is only able to deliver non-repetitive sequences with a maximum pattern length of 65536 bits (and does so at a bit rate of 1 GHz), the total measurement had to be subdivided into one thousand 65 µs frames, each with a different random pattern.

Results

The results of this measurement are shown below and compared with the expectation values. A histogram of the distribution of the measurements which were obtained in the sub-frames is displayed in Fig. 5.47.

absorber	expected	measured	unit
Aluminium	54,215	$53,927 \pm 317$	eV
	1.884	1.874 ± 0.011	fC
	11,760	$11,698 \pm 69$	e^-
Copper	58,388	$58,416 \pm 317$	eV
	2.029	2.030 ± 0.011	fC
	12,665	$12,672 \pm 69$	e^-

Within the achieved precision of about 0.6%, both measurements agree with the expected values for the mean energy of the transmitted spectra. Furthermore, both spectra can clearly be distinguished, since their energy difference of 4.17 keV exceeds the achieved precision of 0.32 keV thirteen-fold. In order to obtain a 1-σ separation between both spectra, a measurement duration of 377 µs would have been sufficient (1.5 ms for a 2-σ separation). However, a single 65 µs frame does not allow the separation of both spectra. This is not surprising, since an average photon rate of 250 kHz yields an expectation value of only 16 photons within this frame duration.
Since the total measurement duration of 65 ms had to subdivided into 1,000 sub-frames, the uncertainty of the combined measurement can be computed

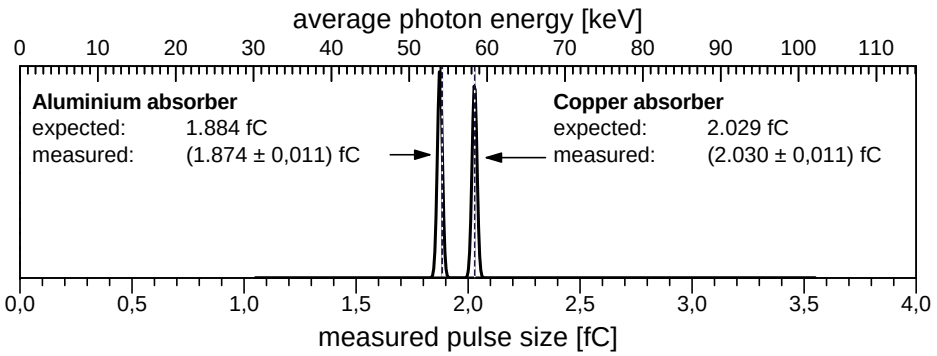

Fig. 5.47: The measured average photon energies agree with the expected value computed from the transmission spectra (dashed lines). The spectral hardening of both spectra is measured successfully, as indicated by the clear separation between the measured average photon energies (black curves).

from the standard deviation of the sub-measurements. Latter was found to be 0.35 fC in both cases, yielding an uncertainty in the combined measurement of 0.011 fC. This is depicted in the width of the Gaussian distributions (black lines) in Fig. 5.47. The measured average photon energies of both spectra are clearly separated, indicating that the spectral hardening is determined successfully.

5.6 Digital Circuitry

5.6.1 Power Consumption

The power consumption of the prototype chip was investigated by measuring the current delivered by the digital and analog supply lines (*vddd*, *vdda*) with respect to the various bias DAC settings. Fitting the respective slopes allowed the determination of each subcircuit's power consumption per DAC step. From these values, the total power consumption can be computed for every set of operation parameters. For example, the operation parameters used in the measurement shown in Fig. 5.40 cause a total power consumption of 236 mW, with each pixel dissipating about 3.7 mW (3.2 mW if corrected for the power consumption of the chip periphery). Almost all of the power (98%) is consumed by the digital circuitry. Among the analog circuits, most of the power (87%) is dissipated in the comparator stages.
The power consumption of the prototype pixels depends largely on the desired integrator clock speed. Higher clock rates impose stronger timing constraints on the combinatory logic circuit, which can only be met by increasing the logic bias settings. An important property of the logic circuits is thus the amount of time needed to switch between logic states. This can be examined by measuring the *propagation delay* of the counter cells (section 5.6.2). On the level of the whole photon counter and integrator subcircuits, the range of logic settings which allow reliable operation is investigated in section 5.6.3.

5.6.2 Propagation Delay and Power-Delay-Product

The propagation delay of a ripple counter describes the amount of time needed for a new value to propagate from the least significant bit to the most significant bit. For the counter cells of the photon counter, this delay can be measured by pre-loading the counter with the value 2^n-1, with n being the number of bits in the counter, $n = 16$ in this case. Following the next count event, one bit after another will undergo a high-to-low transition. The propagation of these transitions through the counter is observed with a latch which becomes opaque after a certain delay with respect to the trigger pulse. The number of zeros (starting from the LSB) marks the propagation progress for the chosen delay.
Four such measurements of the propagation progress as a function of the delay at different logic bias setting are shown in Fig. 5.48. As would be expected, larger logic bias currents cause a faster propagation of the signal through the ripple counter. The linear extrapolations of the four curves meet at a negative value. This offset is caused by combinatory logic in front of the least significant bit. Its delay is equivalent to 1.6 counter cells.
The slope of the propagation curves yields the propagation delay per bit. This value can be related to the respective power consumption by computing the power-delay-product. As can be seen in Fig. 5.49, the value increases at

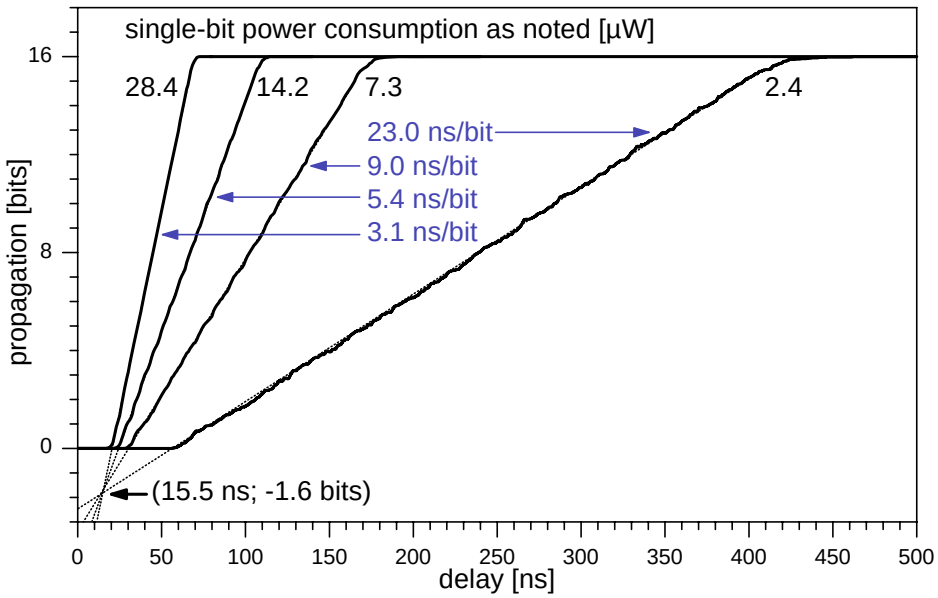

Fig. 5.48: Propagation of a new value through the cells of a ripple counter. Higher *ILogicP* bias currents (noted by the corresponding single-bit power consumption) increase the propagation speed. The delay caused by combinatory logic in front of the first bit is equivalent to 1.6 counter bits.

larger bias settings, which means that higher speeds demand a more than proportionally larger bias current. This effect is explained by the larger voltage swing caused by the increased logic high-level at larger bias current. If the measurement is corrected for this swing increase, the power-delay-product is almost constant at about 57 µW·ns (normalized to 600 mV voltage swing).

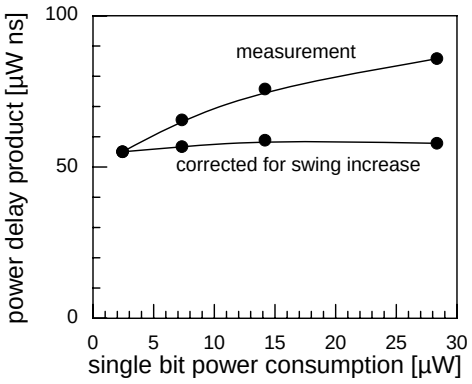

Fig. 5.49: Power-delay-product of the ripple counter. Higher speeds demand a more than proportionally larger bias current. If corrected for the voltage swing increase at higher bias currents, the power-delay-product is almost constant.

5.6.3 Power Optimization

Since the logic circuits are responsible for the majority of the chip's power consumption, an important factor for the power efficiency is the optimization of the logic settings. The switching speed of the differential current steering logic cells depends on three parameters:

- I_{LogicP} is the bias current flowing into the logic block (see Fig. 4.20). Each pixel contains 218 logic elements using the bias current (about 14,000 on the whole chip), resulting in a total increase in power consumption of 3.4 mW per DAC step. This is the largest individual contribution to the chips power consumption, which has a typical total value of 236 mW.

- I_{LogicN} controls the bias of the NMOS transistors in the two load circuits (Fig. 4.21). It is usually chosen to match $I_{LogicP}/2$, but can be adjusted individually. While not influencing the total power consumption, the value of I_{LogicN} with respect to I_{LogicP} controls the value of the current plateau in the load characteristic (Fig. 4.22). This determines the currents during the switching of the logic element's output state, thereby influencing both switching speed and reliability.

- V_{Lo} is the offset voltage of the current source in the load circuits (Fig. 4.21) and defines the logic low-level. Larger values decrease the voltage swing and reduce the power consumption, since about half the I_{LogicP} bias current flows from *vddd* to V_{Lo} (the other half is drained to *gndd*). All logic circuits were designed for a V_{Lo} setting of 200 mV.

A comprehensive scan of all combinations of the three variables is shown in Fig. 5.50. In this measurement, 65,000 pulses were injected into the photon counter. Comparator, feedback circuit and charge injection were chosen so that 100 percent count efficiency was achieved. At each setting of V_{Lo}, I_{LogicP} and I_{LogicN}, the number of pixels returning the correct result was determined and plotted. A white color corresponds to the proper result in all pixels, darker colors correspond to a smaller number of pixels counting correctly and black means that no pixel recorded the proper value. The white area thus marks the range of settings in which the digital circuits of the photon counter operate properly.
The range of valid (I_{LogicP}, I_{LogicN}) settings shrinks significantly as V_{Lo} is increased. At voltages above 125 mV, there is no bias setting at which the photon counter operates reliably in all pixels. If V_{Lo} is set to its design value of 200 mV, only a few pixels work even at optimal bias settings. This deviation from the simulated behavior is attributed to mismatches in the branches of the logic elements. It was also seen in the investigation of the preceding logic test chip [42]. Another possible source for the deviation could be a voltage gradient on the ground and V_{Lo} lines. This should, however, lead

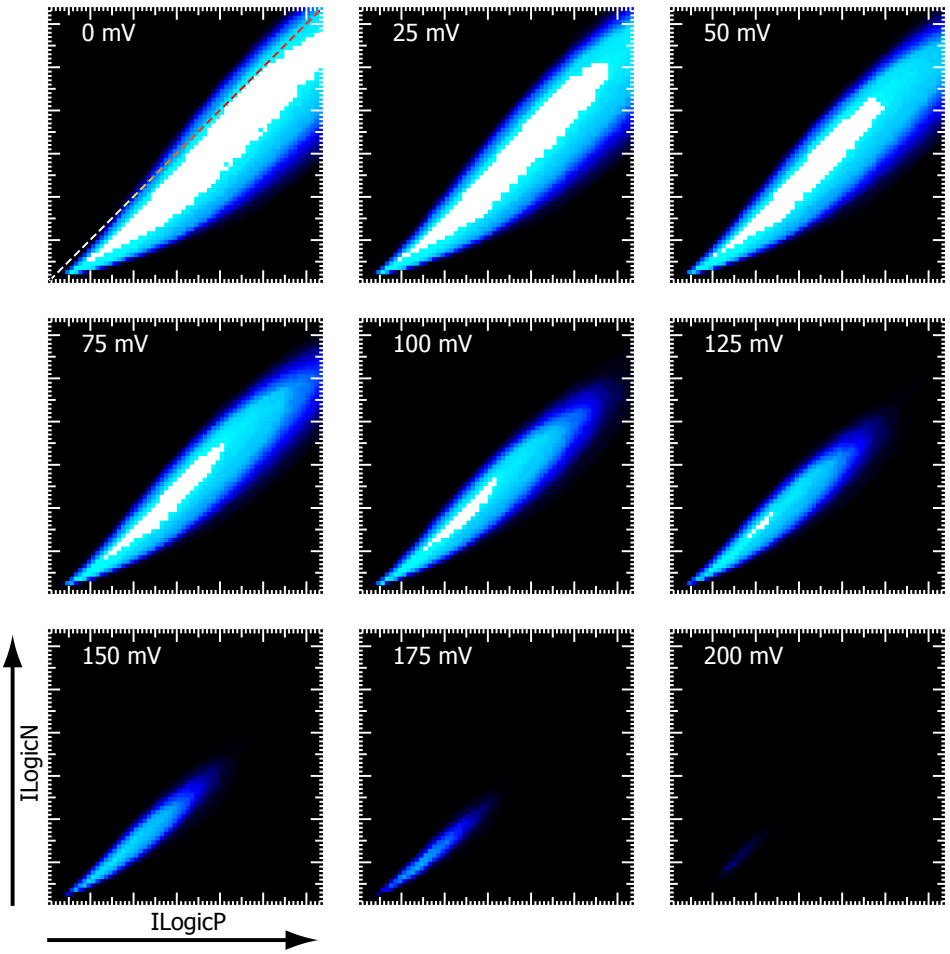

Fig. 5.50: Investigation of valid settings for V_{Lo}, I_{LogicP} and I_{LogicN}, measured using pulse injection into the photon counter. At each setting, the number of properly operating pixels was determined. The white area marks the range in which all pixels return the correct result. Large V_{Lo} voltages reduce the range of valid bias settings significantly. I_{LogicN} must be chosen smaller than I_{LogicP}, as can be seen by the dashed line in the top left graph.

to a gradient in the failing behavior along the chip, which was not observed. As a consequence of these findings, V_{Lo} was always set to 0 V in order to avoid restriction of the range of valid bias settings. V_{Lo} can thus not be used to decrease the power consumption.

The measurement shown in the top left of Fig. 5.50 reveals an additional deviation from the expected behavior. As can be seen from the dashed line, operational bias parameters are only found for I_{LogicN} settings smaller than I_{LogicP}. It is therefore not advisable to derive the NMOS bias voltage of the load circuits directly from the I_{LogicP} bias. The origin of the deviation is

attributed to the circuits which derive the bias voltages from the current delivered by the on-chip DAC.
The most severe timing constraints apply to the time counter of the integrator and the connected *TimeLast* latch. Not only does the value of the counter increase with every integrator clock cycle, its new value also has to be copied to the latch if a pump trigger occurred during the clock cycle. This implies that the sum of total ripple delay and latch setup time must be shorter than the interval between trigger signals for counter and latch. A switch in the chip allows to set the phase difference between both triggers to either a full or half an integrator clock cycle. Choosing a full clock cycle doubles the available time interval (thus reducing the necessary power by one half), but it also makes the circuit sensitive to racing conditions between the two trigger signals. If the counter trigger arrives before the latch signal, a new rippling process might begin before the latch closes, thus corrupting the least significant bit(s) of the latch value.
A detailed investigation of the timing behavior was performed under worst case conditions (frame time: 32768 cycles, pump events on every clock cycle due to maximum input current and current source pump type). This investigation showed that the integrator works reliably at 10 MHz with a delay setting of half a clock cycle between latch and counter trigger signals at bias DAC setting above 45. This corresponds to a power consumption in time counter and latch of 0.81 mW per pixel. As expected, setting the delay to a full clock cycle reduces the necessary power by about one half. In this case, however, some of the pixels show a corruption of the least significant bit of the time latch. This problem could easily be addressed on a potential successor to CIX0.2 by adding an additional delay element to the counter trigger path. In the practical application, however, the influence is usually not significant, since the introduced error is usually smaller than one tenth of a percent.
Note also, that the timing constraints depend strongly on the chosen frame duration. Frame durations exactly matching 2^n clock cycles are the worst choice possible. Slightly different durations allow reliable operation at significantly lower bias settings. Also will shorter frame durations reduce the used number of bits and thus the total ripple delay.

Optimization of the Logic Circuitry

In a new iteration of the CIX chip (*CIX1.0*), a reduction in the power consumption of the logic circuits could be achieved by streamlining the logic circuitry:

- Removing the *TimeFirst* latch will reduce the amount of acquired data by one quarter. This will not only speed up the readout process, save power and layout area, but will also allow an additional simplification of the counter control logic.
- Matching of the counter and latch bit depths to the actually required frame durations. If only 100 µs frame durations at 20 MHz clock rate are required, 11 bits will be sufficient. The first two items alone will reduce the required number of logic elements by about 38%.
- Simplification of the pump control logic by providing only one charge pump type, preferably the switched current source.
- Clustering of nearby pixels to reduce the number of bus drivers and multiplexers.

If power consumption is the primary issue, there is also the option to use a different logic family such as slew rate limited CMOS logic. The potential impact on digital-to-analog crosstalk would, of course, have to be taken into account.

5.6.4 Dead-time Free Readout

The dead time free readout allows the acquisition of previously measured data during the subsequent measurement frame. As mentioned before, this feature is important for medical imaging, where insensitive time intervals must be avoided so that the patient's exposure to radiation is kept to a minimum.

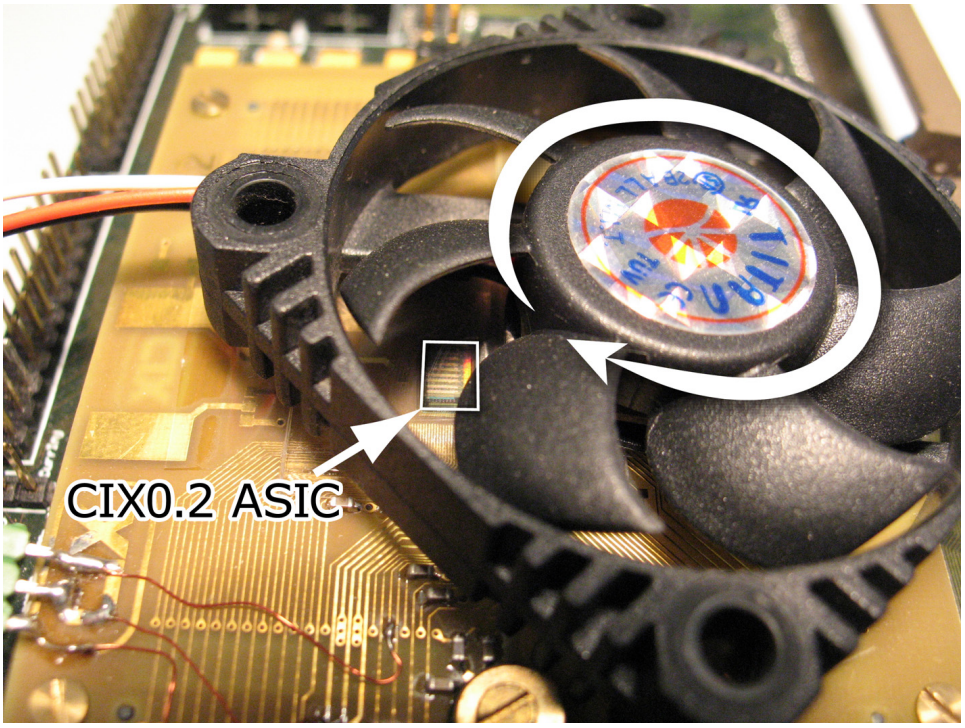

Fig. 5.51: Experimental setup for the demonstration of the dead-time free readout. A 7-blade CPU fan is placed between a light source and CIX0.2 ASIC. The shadow image of the rotating blades is recorded by the photo diodes in the pixel cells.

A demonstration of this readout mode was carried out with the setup shown in Fig. 5.51. A sequence of forty subsequent images from the measurement series is shown in Fig. 5.52. These images are part of a 1,000 frames sequence captured at a rate of 20,000 frames per second (50 µs frame duration). The depicted object is a 7-blade CPU cooling fan spinning at around 4,500 revolutions per minute. Following the images from the top left to the bottom right, one can see the shadow image of one blade passing over the prototype chip. The shadow image was recorded by measuring the current produced by visible light in the on-chip photo diodes. The signal was routed to the integrator directly, bypassing feedback and photon counter. As a side effect of the direct illumination of the pixel matrix, signal charge arises both in

the photo diodes and the exposed n-wells of the analog part. This is also the reason for the inhomogeneities visible in the top row of images. Note that no flat field correction was applied to these images.

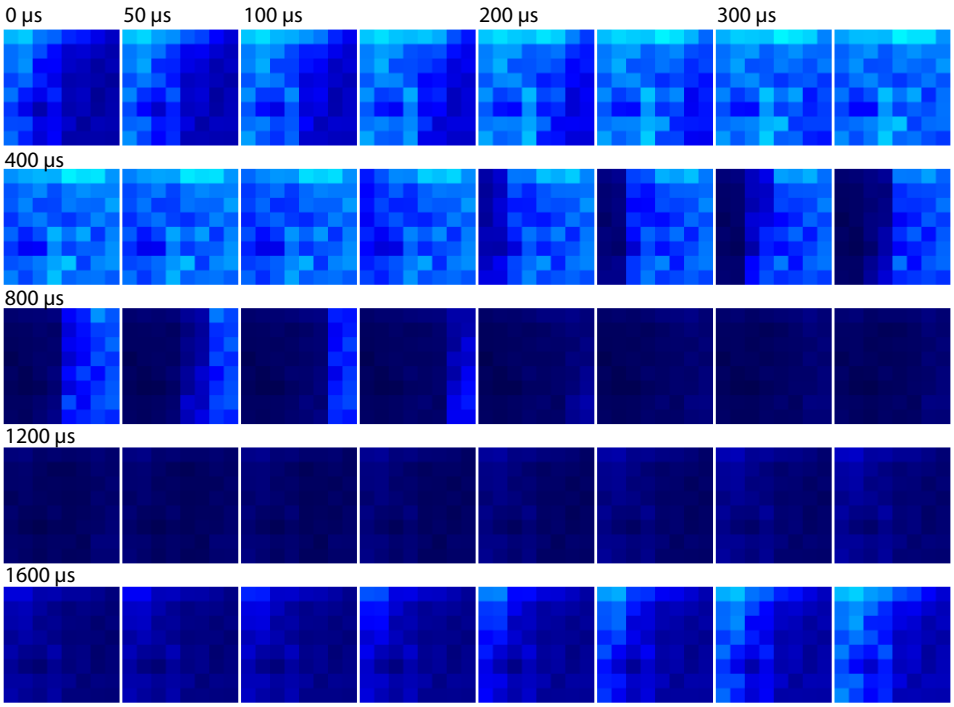

Fig. 5.52: Demonstration of the dead-time free readout using the shadow image of a 7-blade CPU fan spinning at 4,500 rpm. One blade can be seen entering the sensor area from the left at around 600 µs. The images are part of a sequence of one thousand 50 µs-frames recorded at a rate of 20,000 kHz.

The additional digital-to-analog crosstalk arising during the readout process can be investigated by comparing the noise hit rate of the photon counter in measurements with and without simultaneous readout. Fig. 5.53 shows the result of such an investigation. Like in the measurement presented in section 5.2.4, the noise count rate of the photon counter was measured at several threshold voltages relative to the baseline voltage. A difference between both readout modes is only seen at thresholds more than 4 mV above the baseline voltage, where the noise count rate lies below about 80 kHz.
In this area, the simultaneous readout mode reaches the same noise count rate at threshold settings which is slightly larger than those found in the case with interleaved readout. For example, a noise count rate below 10 Hz is achieved at thresholds of 13 mV (800 e^-) in simultaneous readout mode compared to 7 mV (450 e^-) in separate readout mode. Note that the digital-to-analog crosstalk might also contain contributions from interferences on

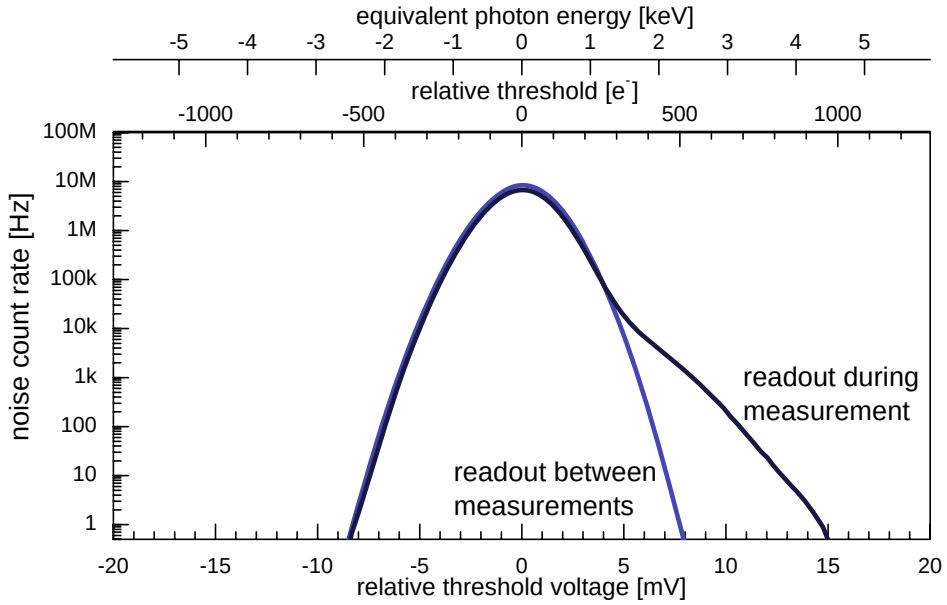

Fig. 5.53: Comparison of the noise count rate with interleaved digital readout in between measurements (left) and during the measurement (right). With simultaneous readout, noise count rates below 10 Hz are obtained with thresholds of 13 mV (800 e^-).

the external PCB. The measurements give thus only an upper limit on the chip's crosstalk.
The crosstalk was also investigated in integrator measurements. For maximum impact, the frame duration was chosen so short (80 µs) that the readout process occupied almost the entire frame duration. Using a 4.7 nA input current, the integrator noise rose from 4.3 pA to 5.1 pA (12 %). This corresponds to a decrease in the signal-to-noise ratio from 1,100:1 to 930:1 (at a discretization precision of 1:1,600).

5.7 Summary of the Experimental Results

This section gives a condensed summary of the most important findings made during the characterization of the prototype.

Photon Counter

The photon counter shows a minimal electronic noise of 78 e^-. The influence of larger feedback bias currents (Fig. 5.8) and capacitive loads were investigated (Fig. 5.9). Low digital-to-analog crosstalk allows precise measurements of the noise count rate (Fig. 5.11). Noise count rates of less than one hit per millisecond are obtained at threshold settings of 6 mV (400 e^-).

An investigation of the double-pulse resolution examined the influence of threshold and feedback settings (Fig. 5.15) and showed that two subsequent 2 fC pulses can be separated if the pulse spacing exceeds a minimal value of 43 ns. The maximum count rate of equidistant 2 fC input pulses lies at 18 MHz, with 12-14 MHz being achieved under typical operating conditions (Fig. 5.7). Input pulses with Poisson-distributed pulse spacings show the predicted exponential decline in the count efficiency at high count rates (Fig. 5.20). The impact of pile-up of subsequent pulses on the shape of threshold scans was investigated (Fig. 5.19). Automatic threshold tuning yields a threshold dispersion of 0.56 mV (36 e^-, Fig. 5.4).

Integrator

The integrator covers a dynamic range of about five orders of magnitude (Fig. 5.21) and is suited for currents between a few picoamperes (Fig. 5.26) and 200 nA. Depending on the logic bias settings, the integrator can be operated at clock rates up to 20 MHz. The noise performance is far better than the quantum noise limit for 60 keV photons throughout the dynamic range (Fig. 5.22 & 5.27). It is in good approximation independent of the charge pump type (Fig. 5.24) and scales with the total input current (signal plus bias current). A typical value for the noise magnitude is 0.4 pA (Fig. 5.22).

Feedback Circuit

The feedback circuits produce accurate reproductions of the input current (Fig. 5.41) with a typical mismatch (after pedestal correction) of less than 10 pA at currents below 1 nA (Fig. 5.30) and a matching of better than 1% at currents above 1 nA (Fig. 5.31). The same measurements also show that the feedback circuit does not hinder the dynamic range in controlled redirection and in static leakage compensation mode (the bypass transistor works as intended). Continuous leakage current compensation is possible for signal currents up to 80 nA. The total noise introduced into the current measurements by the feedback circuit depends on the chosen feedback mode. Typical total values are 2.7 pA for controlled redirection, 4.5 pA for static leakage current compensation and 7.8 pA for continuous leakage current compensation (Fig 5.33). In a comparison of the feedback modes, the controlled redirection mode delivers the most promising results in terms of induced offset currents, signal reproduction quality and the circuit complexity involved. Offset and leakage currents can be removed by the compensation circuits up to a maximum current of 80 nA with an accuracy of about 99.5% (Fig. 5.35). This reduces the remaining average feedback offset current by three orders of magnitude and reduces the dispersion between the pixels to 31.5 pA (Fig. 5.34). Multiple sampling of the same leakage current shows that the best sampling noise (about 10 to 20 pA) is achieved if the compensation

bias current is matched to the actual leakage current (Fig. 5.36). If the compensation circuits are used, sampling noise is usually the dominant noise source in current measurements. The long term stability of the sampled current was found to be insufficient for measurements in which interleaved sampling is impossible for an extended period of time (i.e. several seconds). This problem can be addressed with a small modification to the sampling switch (Fig. 5.37) and turned out to be insignificant for the measurements conducted in the electronic characterization of the prototype.

Simultaneous Photon Counting and Integration

The simultaneous operation of photon counter and integrator allows to identify quantum fluctuations in the input signal and demonstrates the expected correlation between both channels (Fig. 5.38 and 5.39). A combined photon counter and integrator measurement covers a dynamic range from 1 pA to 200 nA (Fig. 5.40). Precise measurements are obtained even in regions in which the photon counter is saturated by a high photon flux or in which the integrator is dominated by the sampling noise. The accuracy of the pulse size measurement was found to exceed the accuracy with which the input pulse size can be kept constant along different pulse frequencies (Fig. 5.42). Spectral information is obtained with a signal-to-noise ratio better than 10:1 in the range between 250 pA and 25 nA (Fig. 5.43). A spectral hardening of about 4 keV was successfully observed in 65 ms measurements with two input signals of similar intensities but slightly different spectral distributions, which matched the transmission spectra behind a copper and an aluminium absorber (Fig. 5.47).

Power Consumption and Dead-Time-Free Readout

A measurement of the power dissipation of the prototype chip determined a typical power consumption of 3.2 mW per pixel. Most of the power (98%) is drawn by the digital circuitry. Further investigation explored the range of valid operation parameters and their influence on the switching speed (Fig. 5.48 & 5.49) and on the reliability of the digital circuitry (Fig. 5.50). Potential options for power optimization were identified. Measurements of the noise count rate and the current noise quantified the cross-talk impact of simultaneous readout during ongoing measurements in comparison to the interleaved readout mode (Fig. 5.53). Even during simultaneous readout, less than one noise hit per millisecond can be achieved with a threshold setting of 530 e^-. The functionality of the dead-time free readout was demonstrated in a measurement that captured a series of 1,000 subsequent frames at a rate of 20 kHz (Fig. 5.52).

6. Conclusions and Outlook

This thesis discussed the implementation and characterization of a new readout scheme for direct conversion X-ray imaging with simultaneous photon counting and integration. These two channels are combined into a single pixel using a special feedback circuit which also provides leakage current compensation.
The investigation served two main purposes: to study the general feasibility and behavior of the new signal processing concept and to evaluate the different design alternatives in the implementation of the concept, so that substantiated design choices can be made in the development of a full-scale imaging chip.
The general feasibility of the concept was successfully demonstrated, showing that the combination of the two channels extends the dynamic range by about one order of magnitude beyond the limits of the individual channels. Spectral information is obtained in the overlap region, which covers about two orders of magnitude. This allows to determine the hardening of the tube spectrum due to attenuation by the imaged object. The feedback circuit is able to handle the sensor leakage currents and delivers accurate reproductions of the input signal. Its additional noise contribution to the current measurement is usually small compared to the quantum noise due to photon number fluctuations in the input signal. The crosstalk between the integrator circuit and the photon counter is small enough to allow simultaneous operation of both channels. Data acquisition can be performed at high frame rates, without interrupting or degrading the ongoing measurement. In summary, the signal processing concept fulfills the expectations and seems to be well suited for the intended applications in CT and radiography.
The comparison of the different feedback configurations identified the controlled redirection mode as a very promising candidate. Not only is the circuit very simple and power efficient, it also shows the best noise performance and current reproduction quality throughout the dynamic range. The circuit has the potential disadvantage of the baseline shift at large input signals. However, even the feedback mode without such a baseline shift is significantly impaired at high photon rates due to the increasing pile-up of subsequent pulses. Furthermore, the baseline shift will also allow to achieve higher count rates, which extends the overlap region during simultaneous operation.
The comparison of the different integrator charge pump types revealed no significant difference between the concepts. The switched current source

charge pump might be the favored candidate, since it does not need a reset cycle between pump actions, which simplifies the pump control logic. However, the large dispersion between the individual pump currents will require a dedicated calibration mechanism. This could, for example, involve a single integrator with a capacitive charge pump which is used to calibrate the other integrators on the chip.
The digital logic circuits, implemented in differential current steering logic, proved to be well suited for the simultaneous operation, since they exhibited only little digital-to-analog crosstalk. A disadvantage is the fairly large power consumption, which is partially owed to the demanded flexibility of the prototype chip. In a new iteration, the logic circuits should thus be kept as simple as possible. It might also be sensible to undertake detailed crosstalk studies comparing this logic family to other potentially more power efficient approaches.
The design of the sampling switches involved in leakage current compensation showed some potential for improvement and should be iterated with the changes discussed in the text. A reduction of the sampling noise would also lead to an improved overall performance, since this noise contribution is the limiting factor in the current measurement in the simultaneous operation mode.
Future applications of the prototype chip will lie in the investigation of different sensor materials and in the evaluation of the imaging properties of the signal processing concept when confronted with the behavior of an actual sensor. The unique combination of measurement possibilities on the prototype chip promises to provide some new and detailed insights. Whether or not there will be a full-scale pixel chip is still unclear at the time of writing. Since the prototype successfully demonstrated the properties which originally motivated its development, the transition to a larger imaging array seems quite sensible from a technical point of view.

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Appendix

A. Detailed Implementation Descriptions

A.1 Three-Transistor Charge Pump Type

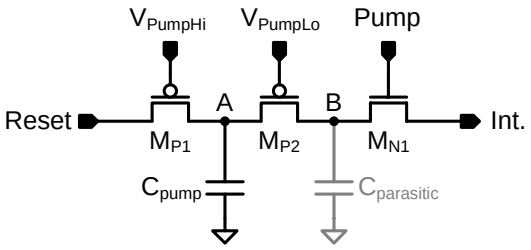

Fig. A.1: Schematic of the three-transistor charge pump type.

The three-transistor charge pump (Fig. A.1) is quite similar to the switched capacitor type in the sense that it is driven by the same *Pump* and *Reset* signals, and that its packet size is determined by the size of the pump capacitor and the difference in V_{PumpHi} and V_{PumpLo}. The circuit is a serial connection of two p-channel transistors (M_{P1}, M_{P2}) and one n-channel transistor (M_{N1}). Node A in between the p-channel transistors is also connected to the pump capacitor C_{pump}. The packet size is determined by the voltage swing on this node, controlled through the gate voltages on the two adjacent transistors (V_{PumpHi} and V_{PumpLo}). M_{N1} is only used as a switch that separates node B from the integrator input unless the *Pump* signal is triggered. For proper operation, some restrictions apply to the gate voltages of M_{P1} and M_{P2}: V_{PumpHi} is chosen smaller than at least one threshold voltage V_{Th} below the high-level V_{Hi} of the *Reset* signal. V_{PumpLo} has to be smaller than V_{PumpHi} but more than a threshold voltage larger than the integrator input potential:

$$(V_{Hi} - V_{Th}) > V_{PumpHi} > V_{PumpLo} > (V_{IntRef} + V_{Th}) \qquad \text{(A.1)}$$

The mechanism of charge transportation can be understood by following the chain of events occurring throughout a reload-discharge cycle (Fig. A.2). Recharging starts with a high-level on the *Reset* connection, which raises the potential on nodes A and B to V_{Hi}, typically around 2.4 V. A subsequent negative edge on *Reset* swaps the role of source and drain on M_{P1} and M_{P2}. Nodes A and B discharge rapidly until their potential reaches ($V_{PumpHi}+V_{Th}$) after which the gate-source voltage of M_{P1} drops below a threshold voltage

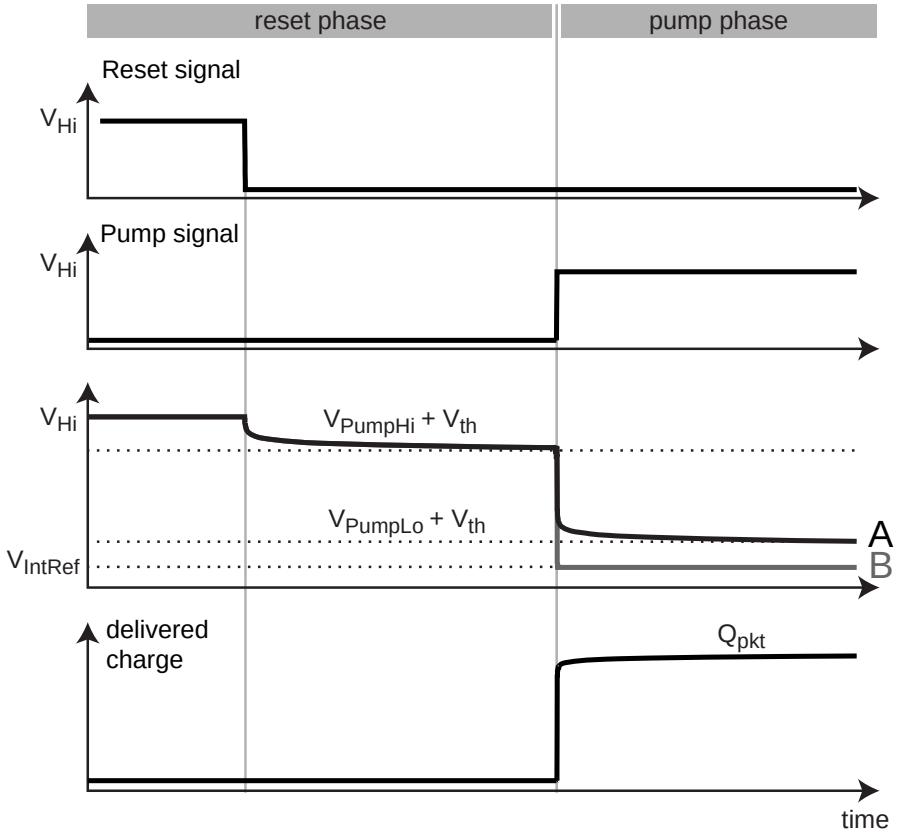

Fig. A.2: Simulation illustrating the pump process in the three-transistor charge pump. Graphs show (from top to bottom): Developing of the non-overlapping control signals *Reset* and *Pump*, the resulting voltages at nodes A and B of Fig. A.1 and the total charge delivered to the integrator input. The high-state of the *Reset* signal raises the potential on A and B to V_{Hi}. After the falling edge of *Reset*, both potentials relax to $(V_{PumpHi} + V_{th})$, thereby completing the recharge process. The rising edge of *Pump* triggers the discharge of nodes A and B, thus delivering the charge packet into the integrator. Neglecting the parasitic capacitance on node B, the packet charge is given by $Q_{pkt} = C_{pump} \cdot (V_{PumpHi} - V_{PumpLo})$.

and the resistance increases significantly. This concludes the recharge phase. A trigger of the *Pump* signal connects node B to the integrator input, thereby swapping source and drain of M_{P1} and M_{P2} once again. Node B discharges quickly to V_{IntRef}, delivering some unwanted additional charge to the integrator input due to the parasitic capacitance of this node. Node A discharges as well until the gate-source voltage of M_{P2} falls below the threshold voltage. This provides the main contribution to the packet size, because C_{pump} is usually much larger than $C_{parasitic}$. The voltage drop on node A dropped from $(V_{PumpHi} + V_{Th})$ to $(V_{PumpLo} + V_{Th})$ thus producing a charge packet of size:

$$Q_{pkt} = C_{pump} \cdot \left[(V_{PumpHi} + V_{Th}) - (V_{PumpLo} + V_{Th})\right] \quad (A.2)$$

$$= C_{pump} \cdot (V_{PumpHi} - V_{PumpLo}) \quad (A.3)$$

Even though this simplistic model gives a good understanding of the basic functionality, there are several effects that have to be taken into account. The following is a brief summary of the higher order effects, a more detailed analysis is presented in [42]. Firstly, the parasitic capacitance of node B causes an increase in packet size, approximately given by

$$Q_{parasitic} = C_{parasitic} \cdot (V_{PumpHi} + V_{Th} - V_{IntRef}). \quad (A.4)$$

The expected size of $C_{parasitic}$ as extracted from the chip layout of CIX0.2 is 9 fF, compared to the measured pump capacitance of about 25 fF. Clearly, the contribution cannot be neglected. Secondly, the threshold voltage of a transistor depends on the difference between source- and bulk potential, a phenomenon know as *bulk effect* or *body effect*. In this case, the source voltages of M_{P1} and M_{P2} are linked to the respective gate voltages, so that the two V_{Th}-terms in equation A.2 are not exactly equal and therefore no longer cancel out. Imperfections in the fabrication process also cause a dispersion of threshold voltages between the different pixels, leading to a non-uniform distribution of packet sizes. Thirdly, the finite resistivity of M_{P1} and M_{P2} in the sub-threshold region induces a dependency of the packet size on the integrator clock frequency. Lower frequencies correspond to longer relaxation periods, leading to a slightly different voltage on nodes A and B at the end of the recharge cycle. The same holds for the duration of the pump phase, where node A discharges to a slightly different voltage. In summary, the higher order effects present in a real-world implementation provide a strong motivation for the usage of an individual calibration of the pump packet size for each pixel and each set of operation parameters.

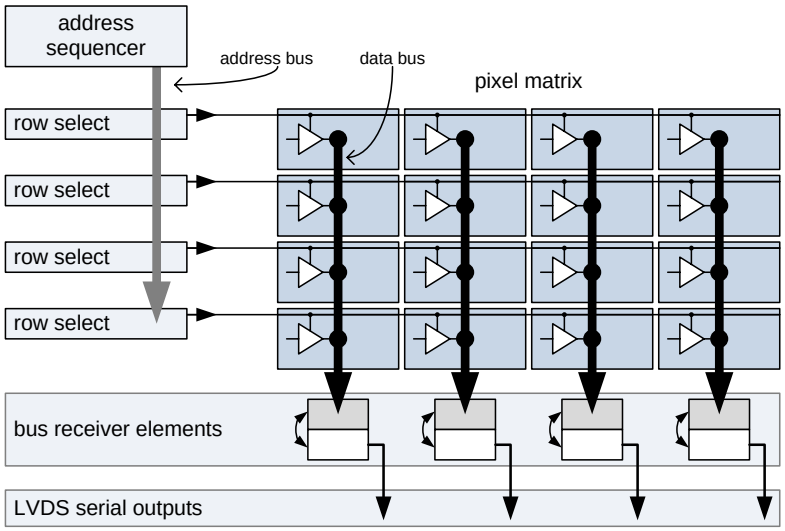

Fig. A.3: Simplified illustration of the readout scheme. The address sequencer selects a pixel row, the *row select* element of given row enables all corresponding bus drivers. These send the values measured in their pixel to their respective data bus. Bus receivers in each column store and serialize the received value. All signals are fully differential. The elements are designed for up to 256 rows and an arbitrary number of columns. Selection of the individual latches is not shown.

A.2 Implementation of the Readout Scheme

The readout scheme strives to be as simple as possible. Ideally, a single clock ($SerCK$) should be sufficient to read out the full chip. In the CIX0.2 prototype chip, however, flexibility and testability are enhanced by separating two clocks ($AdrCK$ and $Switch$) which would normally be derived from $SerCK$. More details are given below. Every pixel stores the information of the last measurement in four 16-bit *readout latches* (namely *PulseCnt, PumpCnt, TimeLast, TimeFirst*). The readout cycle of a single data value consists of the following steps (a simplified schematic and a timing diagram are given in Fig. A.3 and Fig. A.4, respectively):

1. Triggered by a rising edge on $AdrCK$, the *address sequencer* selects a pixel row and the number of the desired readout latch and writes the corresponding address to the 10-bit address bus (Point (a) in A.4).

2. On the falling edge of $AdrCK$, the *row select* modules compare the eight most significant bits on the address bus (Adr) with their respective row index. The selected decoder enables the tristate bus drivers of the pixels in its row. It also feeds the two least significant bits (encoding the index of the selected readout latch) to a 2-bit bus which is connected to every pixel's output multiplexer.

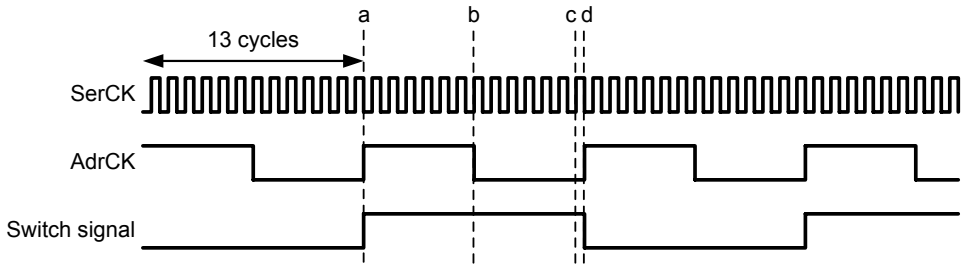

Fig. A.4: Time diagram illustrating the steps of a readout cycle: a) a new address becomes visible on the *Adr* bus, b) corresponding data is fed to the data bus, c) last latching into bus receiver, d) start of serial output (corresponds to point a) of the following data value).

3. The sixteen 4-to-1 output multiplexers in every pixel select the appropriate readout latch so that bus drivers can feed the recorded value to the column's data bus (Point (b) in A.4).

4. Each column's data bus terminates in a *bus receiver*, a unit which consists of DCL load circuits for the data bus and two banks of 23 flip-flops (more on the bank structure below). These flip-flops, operating on the rising edge of $SerCK$, feature a 2-to-1 input multiplexer which is controlled by $Switch$ in one bank and $\overline{Switch}$ in the other. The input multiplexer determines wether the flip-flop is loaded from the data bus or the output of the preceding flip-flop. $Switch$ thus swaps the operational mode of the banks between parallel loading and shift register mode.

5. When $Switch$ changes its state, the bank that previously monitored the data bus becomes a shift register whose output is connected to the column's *LVDS driver* (Point (d) in A.4). With the following pulses on $SerCK$, the recorded data is fed serially to the pair of output pads connected to the LVDS driver. This concludes the readout cycle. The data originally selected by the address sequencer has been written to the serial output pads. Meanwhile, the next readout latch or next pixel has already been selected so that new data is available when $Switch$ changes its state once again.

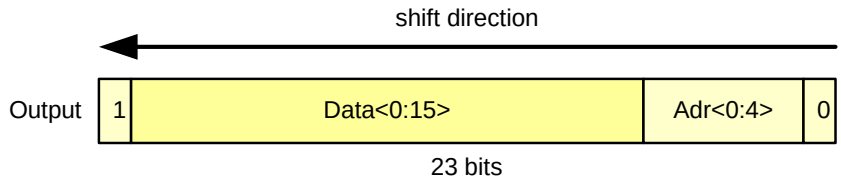

Fig. A.5: Structure of the bus receiver bank: the ratio between the frequencies of *AdrCK* and *SerCK* determines the number of bits that are actually read out. This allows the simulation of counters with a lower bit depth or the retrieval of additional address information for diagnosis purposes.

A.2.1 Bus Receiver

As mentioned above, the banks of the bus receiver consist of twentythree flip-flops (named FF<0:22>) instead of the sixteen that might be expected from the counter depth (see Fig. A.5). The actual data value is stored in FF<1:16>, with FF<1> holding the least significant bit. FF<0> is always loaded with a logical one, FF<17:21> contain the five least significant bits of the selected address, FF<22> is always loaded with zero. Note that the number of bits which are actually transferred to the serial output depends on the number of *SerCK* pulses during one *AdrCK* cycle. Given a desired counter depth of N bits, the relation between the clock frequencies is:

$$f_{SerCK} \quad = \quad (N+1) \cdot f_{AdrCK} \quad = \quad 2 \cdot f_{Switch}$$

This allows the simulation of counters with different depths. A value of 16 will produce 17 *SerCK* pulses between subsequent transitions in *Switch*, resulting in one header bit, followed by the 16-bit value on the serial output. The header bit is a precaution, its value might be corrupted depending on the phase between *SerCK* and *Switch*. This is also the reason why *Switch* is not simply derived from *AdrCK*, but provided externally with direct control of the phase relation between *Switch* and *SerCK*. A value of $N = 12$, as shown in Fig. A.4, yields the twelve least significant bits of the recorded value. On the other hand, it is possible to obtain additional information on the selected pixel and readout latch if N is chosen $\geqq 21$. This is helpful not only during the debugging phase, but also for readout stability testing and power optimization.

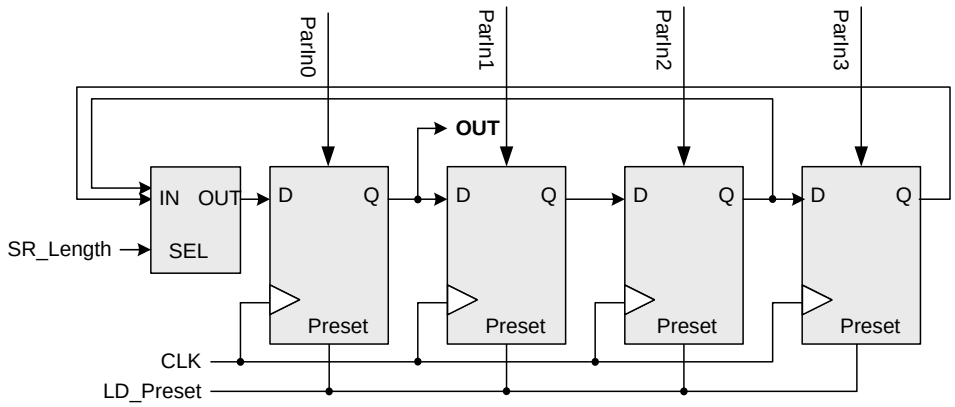

Fig. A.6: Schematic of the ring shift register with preset used in the address sequencer for the generation of arbitrary bit patterns with a length between one and four bits. *SR_Length* connects the output of the third flip-flop for a pattern length of 3 and the output of the last flip-flop in all other cases.

A.2.2 Address Sequencer

The previous discussion assumed that the address sequencer delivers the next address with every rising edge of $AdrCK$. In a configuration where all four latches are read out in every pixel, the address sequencer could therefore simply be a normal counter. Yet the different modes of operation which are desirable for a CIX pixel demand a higher degree of flexibility. For example, one might be interested only in photon counter measurements or only the integrator data. Latter can also be obtained in two different modes:

- Continuous operation of the time counter, recording the time stamps of the first and last pump event ($TimeFirst$, $TimeLast$).
- Restart of the time counter from zero when the first pump event occurs. This eliminates the need for the $TimeFirst$ latch, which is always zero.

The readout should, of course, always operate as fast as possible i.e. with the minimal number of $SerCK$ clock cycles. This flexibility and efficiency is achieved using three synchronous, configurable 4-bit ring shift registers of the type shown in Fig. A.6. Each register has a 4-bit preset *ParIn<0:3>*, stored in the I^2C chip register, which is loaded before every readout phase. Determined by the value of SR_Length, the periodicity is either 3 or 4 $AdrCK$ clock cycles. Combined with a proper preset, any period between one and four is possible (see examples a) and b) in Fig. A.7). Two of these ring shift registers produce the address which selects the readout latch type *Adr<1:0>*. The third register contains the count-enable bit $CntEn$ which controls the 8-bit counter element responsible for the pixel row address *Adr<9:2>*. The pixel address is increased every time a logic one appears

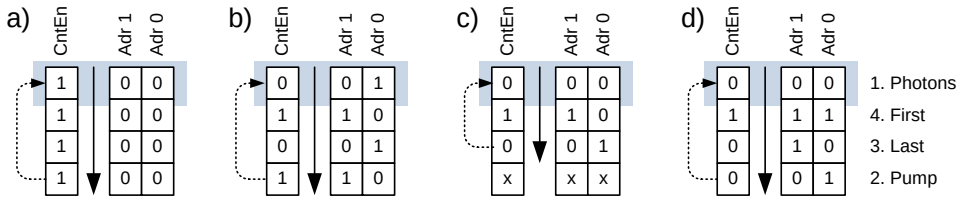

Fig. A.7: Example presets for the ring shift registers (vertical segments). The blue area marks the output flip-flops, the arrows show the shift direction and periodicity. Acquired measurement channels: a) Photon counter only, b) integrator only (no *TimeFirst* latch), c) photon counter and integrator, d) full data set. Note the order in which the indices appear at the output, shown for example d) on the right side.

on the register output. With presets like shown in Fig. A.7, all possible combinations of measurement channels can be read out with the minimal number of $SerCK$ pulses.
This concludes the description of the elements involved in the readout chain. It has been explained how the readout logic achieves full flexibility in counter depth and the number of measurement channels while maintaining maximum transfer rates and a simple, (almost) one-clock based readout scheme.

A.3 Counter Cells

The counter logic block is implemented in differential current logic and consists of sixteen identical one-bit units (see Fig. A.8), each with photon counter, pump counter, time counter, time-first latch, time-last latch, four additional readout latches (for photon and pump counter and both time latches), a 4-to-1 output multiplexer and a tristate buffer [42]. Additional readout latches are necessary for the simultaneous readout during the following measurement. They save the measured values from being overwritten by the ongoing measurement before they are read out. All three counters are designed as asynchronous ripple-counters which operate on the falling edge of the input signal. The most stringent timing constraints apply to the time counter, whose value must be transferred to the time last latch on every pump event. It is thus mandatory that the propagation of the new time value through the counter cells finishes before the time last latch freezes its recorded value. For this reason, the pump counter is provided with separate bias control DACs (I_{TimeP} and I_{TimeN}). The counter logic block is not only responsible for 40% of the pixel width (area: $200\mu m \cdot 180\mu m$), it also dissipates about two thirds of the total power consumption. A lower bit depth is thus the major candidate for potential power and area reduction.

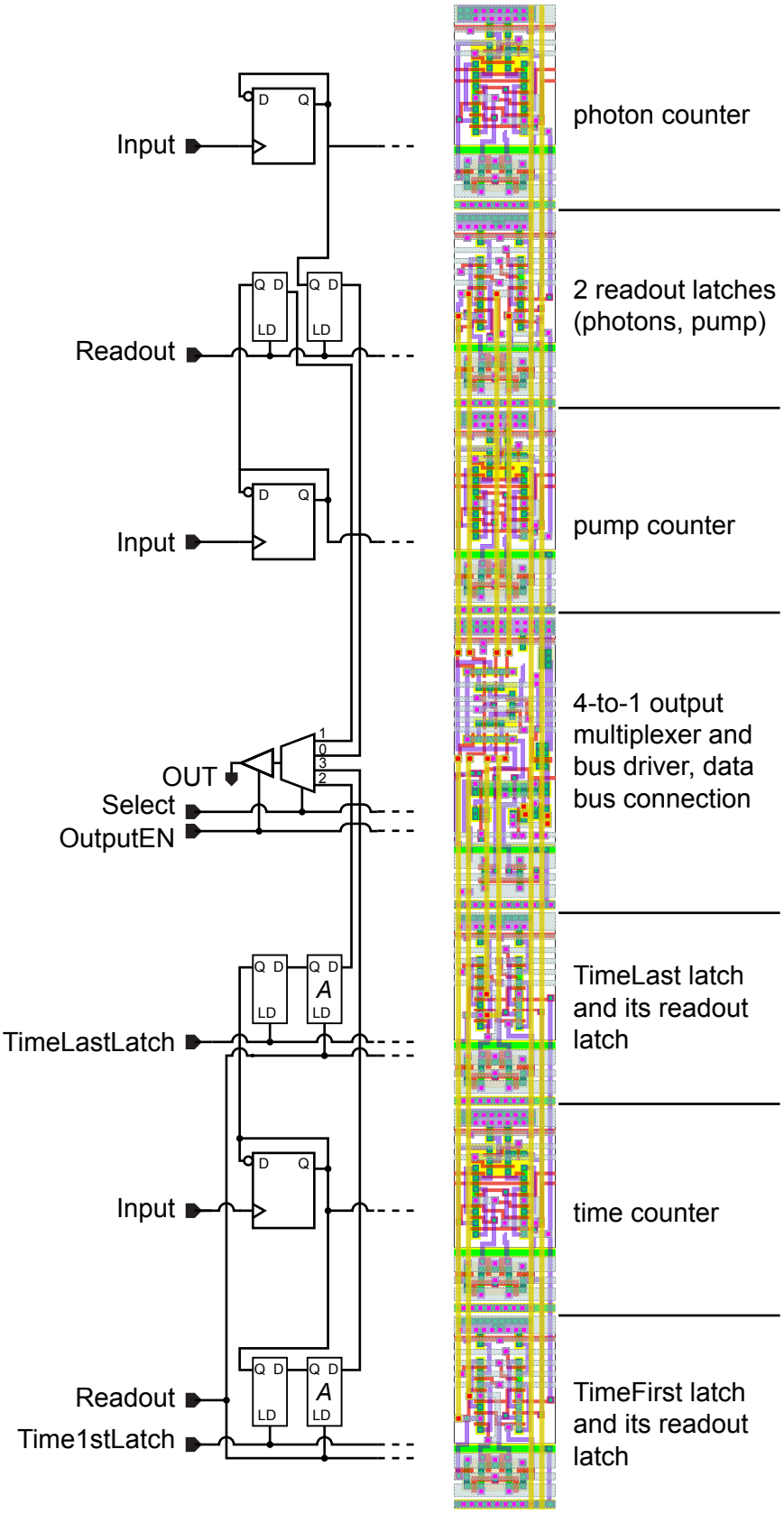

Fig. A.8: Schematic and layout view of a one-bit element of the CIX counter block. Sixteen of these elements are present in each pixel, covering a total area of $200\mu m \cdot 180\mu m$. Adapted from [42].