UNIVERSITÄT BONN
Physikalisches Institut

Design of a current based readout chip and development of a DEPFET pixel prototype system for the ILC vertex detector

by
Marcel Trimpl

Abstract: The future TeV-scale linear collider ILC (**I**nternational **L**inear **C**ollider) offers a large variety of precision measurements complementary to the discovery potential of the LHC (**L**arge **H**adron **C**ollider). To fully exploit its physics potential, a vertex detector with unprecedented performance is needed. One proposed technology for the ILC vertex detector is the DEPFET active pixel sensor. The DEPFET sensor offers particle detection with in-pixel amplification by incorporating a field effect transistor into a fully depleted high-ohmic silicon substrate. The device provides an excellent signal-to-noise ratio and a good spatial resolution at the same time. To establish a very fast readout of a DEPFET pixel matrix with row rates of 20 MHz and more, the 128 channel CURO II ASIC has been designed and fabricated. The architecture of the chip is completely based on current mode techniques (SI) perfectly adapted to the current signal of the sensor. For the ILC vertex detector a prototype system with a 64×128 DEPFET pixel matrix read out by the CURO II chip has been developed. The design issues and the standalone performance of the readout chip as well as first results with the prototype system will be presented.

Post address:
Nussallee 12
53115 Bonn
Germany

BONN-IR-2005-08
Bonn University
December 2005
ISSN-0172-8733

Design of a current based readout chip and development of a DEPFET pixel prototype system for the ILC vertex detector

Dissertation

zur

Erlangung des Doktorgrades (Dr. rer. nat.)

der

Mathematisch-Naturwissenschaftlichen Fakultät

der

Rheinischen Friedrich-Wilhelms-Universität

zu Bonn

vorgelegt von

Marcel Trimpl

aus

Kamen

Bonn 2005

Dieser Forschungsbericht wurde als Dissertation von der Mathematisch-Naturwissenschaftlichen Fakultät der Universität Bonn angenommen.

Die Dissertation ist auf dem Hochschulschriftenserver der ULB Bonn *http://hss.ulb.uni-bonn.de/diss_online* elektronisch publiziert.

Tag der Promotion: 20.12.2005
Referent: Prof. Dr. N. Wermes
Koreferent: Prof. Dr. I. C. Brock

Abstract: The future TeV-scale linear collider ILC (**I**nternational **L**inear **C**ollider) offers a large variety of precision measurements complementary to the discovery potential of the LHC (**L**arge **H**adron **C**ollider). To fully exploit its physics potential, a vertex detector with unprecedented performance is needed. One proposed technology for the ILC vertex detector is the DEPFET active pixel sensor. The DEPFET sensor offers particle detection with in-pixel amplification by incorporating a field effect transistor into a fully depleted high-ohmic silicon substrate. The device provides an excellent signal-to-noise ratio and a good spatial resolution at the same time. To establish a very fast readout of a DEPFET pixel matrix with row rates of 20 MHz and more, the 128 channel CURO II ASIC has been designed and fabricated. The architecture of the chip is completely based on current mode techniques (SI) perfectly adapted to the current signal of the sensor. For the ILC vertex detector a prototype system with a 64×128 DEPFET pixel matrix read out by the CURO II chip has been developed. The design issues and the standalone performance of the readout chip as well as first results with the prototype system will be presented.

Contents

Introduction **7**

1 The ILC project **10**

1.1 Linear collider concept 10
1.2 Superconducting accelerator technology at the ILC 13
1.3 Large Detector Concept 14
1.4 Design considerations of the vertex detector 19
1.4.1 Beam related pair production background at the ILC 19
1.4.2 Baseline design of the vertex detector 21

2 The DEPFET sensor **25**

2.1 Sidewards depletion 25
2.2 Principle of operation of the DEPFET detector 26
2.3 Clear operation of the device 29
2.4 Readout principles for DEPFET pixel 30
2.5 Operation of a DEPFET matrix 32
2.6 DEPFET production for the ILC 33

3 Design of the CURO readout chip **35**

3.1 Readout scheme at the ILC 35
3.2 Architecture of the CURO chip 36
3.3 Design of a fast and accurate current memory cell 38
3.3.1 Basic principle of operation 39
3.3.2 Cascode circuit 41
3.3.3 Settling behavior 42
3.3.4 Noise analysis of a basic current memory cell 44
3.3.5 Design flow 47
3.3.6 Double stage memory cell 50
3.3.7 Summary of the memory cell design 53
3.4 Input stage realized by a regulated cascode 54
3.5 Current comparator for hit discrimination 58
3.6 Hitscanner and digital part 59
3.7 Summary of the CURO design 62

4 Performance of the CURO II chip 64
4.1 Overview of the readout chip CURO II 64
4.2 Linearity of the analog part and performance of the pedestal subtraction 66
4.3 Noise contribution of the readout 70
4.4 Channel dispersion 71
4.5 Zero suppression and digital tests 71
4.6 Power consumption 73
4.7 Towards an ILC CURO generation 74
4.8 Summary of the CURO II performance 75

5 Design consideration of a DEPFET pixel based vertex detector 76
5.1 Module concept 76
5.2 Thinning concept of a DEPFET device 78
5.3 Material budget and power consumption 80
5.4 Radiation Tolerance 83
5.5 Estimated noise performance 85
5.6 Summary of the DEPFET pixel based vertex detector 89

6 The ILC DEPFET-System 91
6.1 Description of the system 91
6.2 Readout sequence 93
6.3 System calibration 94
6.4 Leakage current 95
6.5 Noise Performance 95
6.6 Measurements using X-rays 98
6.7 Summary of the ILC DEPFET-System 102

Summary and Outlook 103

A Correlated Double Sampling 105
A.1 Weighting function for correlated double sampling 105
A.2 Influence of CDS on the system noise 106

B Noise integrals 110
B.1 One pole 110
B.2 Two poles 111
B.3 Two poles and one zero 111

C CURO II reference 114
C.1 Command and Data Register 114
C.2 Analog Part 114

Bibliography 124

Acknowledgments 129

Introduction

Urged to unravel the mysteries of nature, researchers are never satisfied with the standard of knowledge of mankind. By performing a wide variety of extensive experiments, this knowledge has been vastly improved in the last decades.

One of the most significant achievements of modern elementary particle physics is the development of the Standard Model of particle physics [1], describing the fundamental particles and their interaction. The Standard Model considers quarks and leptons, i.e. the electron and its heavier partners as the basic constituents of matter. A concise theoretical framework (the Standard Model) for the forces between these fundamental particles has been developed which is based on the theoretical principle of gauge invariance [2]. The Standard Model includes the strong interactions due to the color charges of quarks and gluons and is described by the well established Quantum Chromodynamics (QCD). A combined theory of weak and electromagnetic interaction, known as electroweak theory, introducing W and Z bosons as the carrier particles of weak processes, and photons as mediators to electromagnetic interactions.

Despite the fact that the Standard Model is confirmed by many precision measurements, many fundamental questions are still open. For example, it is still unclear through which mechanism particles acquire their mass. At the moment, the inherent mechanism proposed to extend the Standard Model, to give particles a mass while preserving the gauge principles is the so-called Higgs mechanism. This mechanism involves the Higgs boson, which has not been observed yet. Therefore, one of the most pressing challenges of particle physics is to establish the Higgs mechanism, to find the Higgs particle, if it exists and to study its properties.

The missing explanation for the masses of particles is not the only deficiency of todays Standard Model. General arguments, such as the hierarchy problem [3] clearly point to the existence of a more fundamental theory. Supersymmetry is one favored idea and offers various extensions to the Standard Model. Most importantly, supersymmetry provides a framework for the unification of the electromagnetic, weak and strong forces at large energies. The discovery of supersymmetric particles and a precise measurement of their properties could provide a better understanding of the underlying fundamental theory.

To facilitate these studies, collider machines will be constructed in the next years accessing energies that are beyond the reach of present accelerators. These machines have a very good chance to discover the Higgs boson and supersymmetric particles. Besides

the challenge of constructing these collider machines, it is necessary to provide hermetic detector systems that are capable to reconstruct the particle tracks after collision and to identify the momentum, energy and charge of the produced particles. The tracking part of the detector system is placed as close as possible to the collision point. Especially, so called vertex detectors are used to reconstruct precisely the position where particles with life times of about 10^{-12} s and shorter have decayed and produced secondary particles. Here, highly granulated detectors with excellent spatial resolution in the order of a few micrometers are needed for an accurate reconstruction.

Semiconductor materials have made a significant contribution in building such high resolution devices. One important advantage of semiconductor devices is the small energy that is needed to produce charge carriers in the medium. Compared to other detector systems, such as gas based technologies, this leads to a large signal provided by impinging radiation. Thus, a high signal to noise ratio is obtained. Furthermore, the high mobility of the charge carriers in semiconductors offers a very fast detector response in the order of a few nanoseconds.

Due to the wide availability and the close link to microchip technology, silicon has become an outstanding material. Modern industrial processes can be used to produce large scale detectors and a fine segmentation of the material provides a very good spatial resolution. Other semiconductor materials with higher atomic numbers, like cadmium compounds are emerging for direct detection of high energetic X-rays due to their better absorption coefficient. These materials are interesting for medical imaging or for quality and security surveillance. For tracking applications in high energy physics, however, silicon is still the first choice material.

To satisfy the increasing requirements on tracking devices, existing detectors are improved and completely new concepts are explored. The DEPFET (**DEP**leted **F**ield **E**ffect **T**ransistor) is an advanced semiconductor detector. It integrates a first electronic amplifying stage in form of a Field Effect Transistor in a silicon detector. Due to the combination of radiation detection and amplification the device shows an excellent noise performance. Recent measurements on present DEPFET sensors demonstrated a noise performance of ENC $= 2.2\,e^-$ (**E**quivalent **N**oise **C**harge) at room temperature [4]. Together with an observed spatial resolution of $\sigma = (6.7 \pm 0.7)\mu$m using $50 \times 50\,\mu m^2$ large pixel cells [5], this is an outstanding overall performance.

Within the scope of this thesis, a concept for a vertex detector at the International Linear Collider (ILC) based on DEPFET pixels is described and first results achieved with a prototype system will be presented. The thesis is arranged in the following way:

In the first chapter the ILC project will be introduced. The linear accelerator concept will be discussed and the overall detector will be briefly described to place the development of the vertex detector in perspective to the whole project. Finally, the requirements on the vertex detector and the baseline design will be introduced.

The second chapter deals with the DEPFET detector itself. The principle of operation of the device and readout concepts for a DEPFET matrix will be discussed.

For the fast readout of a DEPFET pixel matrix a microchip has been fabricated in a

standard CMOS process. The readout chip uses novel current mode techniques for on-chip signal processing. The architecture and the design of the microchip will be discussed in chapter 3. Chapter 4 summarizes the standalone performance of the microchip.

In chapter 5 the design concept of a vertex detector for the ILC based on DEPFET pixels will be presented. The concept will be evaluated with respect to the crucial requirements.

In chapter 6 the ILC DEPFET-System will be described. First results with the prototype system using a 64×128 DEPFET pixel matrix will be presented.

Finally, the main subjects and results of the thesis will be summarized and an outlook into future developments of the project is given.

1 The ILC project

At present, the focus of interest of particle physicist is the Large Hadron Collider (LHC) at CERN. The LHC is a proton-proton collider currently under construction and is expected to be commissioned in 2007. Providing center-of-mass energies up to 14 TeV and a luminosity of up to $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, the LHC will probably discover new physics beyond the Standard Model. After the discoveries, more precise measurements are needed which can be provided by colliders that use leptons instead of hadrons. The advantage of lepton machines is the well defined initial state of the collision due to the structureless leptons that are used and the fact that all the center-of-mass energy is available in the primary collision. Furthermore, less competing background processes occur compared to hadron machines, leading to clean signatures in the detector system. Historically, the Fermilab proton anti-proton collider TeVatron and the Large Electron Positron collider (LEP) at CERN have already demonstrated how powerful the synergy of hadron and leptons machines can be. To fill the gap of a precision partner for the LHC, the International Linear Collider (ILC) is proposed where electrons will collide with positrons at a center-of-mass energy ranging from 90 GeV to 1 TeV. Studies have shown that the ILC can provide detailed information on newly discovered particles as well as exact measurements on already existing parameters of the Standard Model. For example, deviations from the tri-linear WWZ coupling $\Delta\mathcal{K}_{\mathcal{Z}}$ measured at the ILC will be three orders of magnitude more precise than those measured at the LHC or the TeVatron [6]. The complementary nature of the LHC and the ILC has convinced the international particle physics community that the ILC must be the next major particle physics project and that it should ideally operate in parallel with the LHC. However, it has neither been decided to build the ILC, nor exists a global agreement where to construct the facility. In this chapter the linear collider itself as well as one possible detector option for the ILC is described.

1.1 Linear collider concept

In principle, two main concepts for realizing the accelerating part of a collider machine exist, the circular concept and the linear one. In a circular collider, particles are accelerated in a ring until they reach a designated energy and are then brought to collision. In case of a linear collider, the particles start at two different locations and are accelerated in a straight line before they collide, as illustrated in Fig. 1.1. Since the ILC uses electrons and positrons for collisions and should provide a center-of-mass energy up to the TeV scale, the circular acceleration concept is no longer feasible due to en-

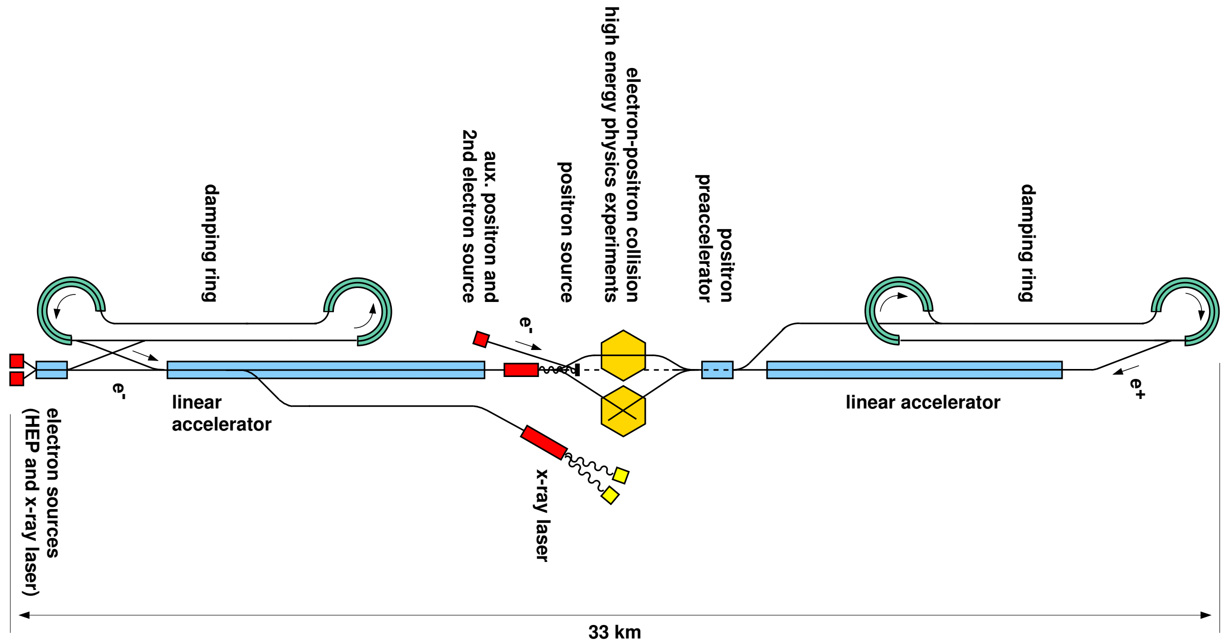

Figure 1.1: Principle overview of the proposed TESLA facility. The linear collider as well as the X-ray laser laboratory is shown.

ergy loss caused by synchrotron radiation. Synchrotron radiation emitted by a charged particle when forced on a circular path is proportional to $1/m^4$. Although the energy loss becomes negligible at high energies for heavy particles like protons, it is not for light particles like electrons. The energy loss ΔE due to synchrotron radiation for one circular revolution of a highly relativistic particle with rest mass m_0 and energy E is given by [7]

$$\Delta E = \frac{e^2}{3\,\epsilon_0\,(m_0 c^2)^4}\,\frac{E^4}{r} \tag{1.1}$$

where e is the elementary charge, ϵ_0 is the dielectric coefficient, c is the speed of light and r is the radius of the circular path. Table 1.1 illustrates the effect of synchrotron radiation of a circular accelerator when simply scaling the energy range and dimensions of the LEP collider at CERN that stopped operating at the end of 2000. At a center-of-mass energy in the TeV range, the energy loss reaches about 10 % per revolution for a typical radius of 1000 km, rendering the operation of a circular approach no longer economic. Hence, the next e^+e^- machine is supposed to be a linear one. When choosing the linear collider

	LEPII	Super-LEP	Hyper-LEP
E_{CM}[GeV]	180	500	2000
L[km]	27	200	3200
ΔE[GeV]	≈ 1.5	≈ 12	≈ 240

Table 1.1: Energy loss ΔE due to synchrotron radiation for different circular accelerator configurations.

concept, a few aspects have to be taken into account. First, the acceleration gradient has to be much more efficient compared to a circular one, since the final energy has to be reached in a single acceleration cycle. Consequently, high acceleration gradients are needed to keep the geometrical dimension of the facility within a realistic boundary.

Besides the center-of-mass energy, the luminosity $\mathcal{L}$ of the beam is another figure of merit of a collider machine. It determines the expected event rate, dN/dt of a specific process characterized by its cross section σ

$$\frac{dN}{dt} = \mathcal{L} \cdot \sigma \tag{1.2}$$

Figure 1.2 gives an overview of some theoretical cross sections for e^+e^- annihilation processes for center-of-mass energies $\sqrt{s}$ up to 1 TeV. Apart from known and still unknown

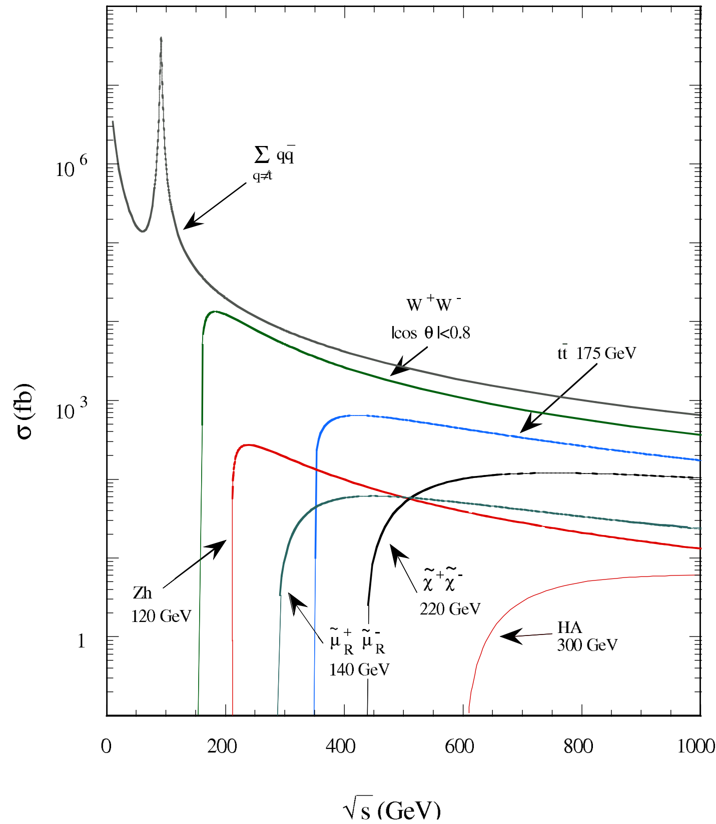

Figure 1.2: Expected cross sections for selected e^+e^- annihilation processes depending on the center-of-mass energy $\sqrt{s}$ of the collider [8].

resonances like the Z^0-resonance and threshold effects, the cross section shows a $1/s$ behavior. Thus, running at high energies means at the same time lower cross sections. In order to achieve a sufficient event rate the luminosity of the beam has to be increased. Achieving high luminosities with a linear collider machine is especially laborious since the particle bunches are used for one collision only and cannot be reinserted. To summarize, the required developments for the construction of the ILC machine are driven by the necessity of achieving high acceleration gradients and a high luminosity.

1.2 Superconducting accelerator technology at the ILC

An important step towards the realization of the ILC was taken in 2004, when the International Technology Review Panel recommended to use superconducting RF technology for the acceleration of the electrons and positrons [9], rather than the normal conducting alternative. The advantage of superconducting cavities is the significant reduction of surface resistance by a factor of 10^6 by using the superconducting material niobium instead of copper structures operated at room temperature. Thus, a better energy efficiency is achieved, even if elaborated cooling for the superconducting temperature is taken into account. Furthermore, the requirement on the alignment of the superconducting cavities is much lower due to much lower resonant frequency compared to normal conducting cavities. The technology recommendation was accepted by the American, Asian and European Particle Physics laboratories which are working together to construct the ILC.

Since the superconducting acceleration concept was initially proposed by the TESLA (**T**eV **E**nergy **S**uperconducting **L**inear **A**ccelerator) group at DESY, the ILC accelerator will probably be constructed in a similar way. In the following the TESLA accelerator will be briefly introduced. A comprehensive overview of the project can be found in the TESLA Technical-Design-Report [10]. The 33 km large TESLA facility is illustrated in Fig. 1.1. It consists of an electron and a positron source with associated damping rings and two 15 km long linear accelerators for electrons and positrons each. Besides of the main interaction region for the e^+e^- collisions, a second detector (e.g. for $\gamma\gamma$ interactions) is foreseen. An operation mode with polarized electrons (up to 80 %) and positrons (up to 60 %) has been considered. In the first stage of construction, a center-of-mass energy of 500 GeV is planned, which will be extended in a second stage to 800 GeV or even more depending on the acceleration gradients that can be achieved. At the moment, acceleration gradients in the order of 25 MV/m have been achieved using cavities from batch production, while post-worked cavities provide a much higher gradient. A theoretical limit on the acceleration gradient is set to 50 MV/m, when the magnetic field at the surface of the cavity reaches the critical magnetic field $B_c \approx 200\,\mathrm{mT}$ of the superconductor niobium.

The operation of the cavities also dictates the time structure of the collider. In case of the 500 GeV mode, 2820 bunches having an interval of 337 ns are combined into one train of 950 μs length. The repetition rate of the bunch train is 5 Hz leading to a long bunch gap of 199 ms. The beam itself has an elliptical shape with a size of $5 \times 553\,\mathrm{nm}^2$. Hence, a high luminosity of $\mathcal{L} = 3 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ is achieved while keeping the beam related background at a tolerable level. Some parameters of the TESLA collider for the two energy stages are summarized in table 1.2. For comparison, also the LEP parameters are listed.

The original TESLA proposal included a X-ray laser laboratory [12]. The laser is operated as a Free-Electron-Laser (FEL) and provides coherent X-rays. The peak brilliance of the laser will be more than a factor of 100 million times higher compared to todays best synchrotron radiation sources. In addition, the X-rays will be delivered in flashes

parameter	LEP	TESLA		unit
center-of-mass energy	209	500	800	GeV
luminosity	$\approx 10^{32}$	$3.4 \cdot 10^{34}$	$5.8 \cdot 10^{34}$	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
bunch train duration		950	850	μs
number of bunches / train		2820	4886	
bunch distance	$22 \cdot 10^3$	337	176	ns
train repetition rate		5	4	Hz
beam size σ_x	100	0.553	0.391	μm
beam size σ_y	10	0.005	0.0028	μm
beam length σ_z	10	0.3	0.3	mm
acceleration gradient	7	25	40	MV/m

Table 1.2: Baseline parameters of the TESLA collider for 500 GeV and 800 GeV center-of-mass energies [10] compared to the LEP collider [11].

of 100 femtoseconds duration or less, which will allow the observation of very fast processes in biology or chemistry. Due to its outstanding scientific potential, the X-FEL facility has been approved in 2003. It is currently under construction at DESY using the superconducting acceleration cavities developed for the TESLA collider. First light beams are scheduled for 2012.

1.3 Large Detector Concept

For the ILC, the detector development is not so much dominated by radiation hardness issues, like for the LHC. The detector design is driven by precision measurements to fully exploit the physics capabilities of the machine. Compared to the detectors at the LEP and SLC accelerators, detector performance has to be improved by an order of magnitude to fully exploit the physics potential at the ILC. The main requirements addressed to the detector system are summarized in the following, details can be found in [13]:

- An efficient track reconstruction, even for processes with high multiplicities of heavy quark jets.
- An excellent momentum resolution.
- An excellent impact parameter resolution for high b- and c-tagging capabilities.
- An almost complete hermiticity, as most SUSY (**SU**per**SY**mmetry) signatures are characterized by missing energy.
- A high resolution calorimeter with a sufficient three dimensional granularity.
- Compatibility with a triggerless operation for maximal efficiency.

Since the decision for the superconducting acceleration technique has been made, three main detector concepts emerged, the SiD (Silicon Detector), the LDC (Large Detector Concept) and the GLD (Global Large Detector). The development of the detector concepts is still in progress, a summarizing design report is expected to be published in 2007. The former TESLA detector proposal as presented in [13] is most closely related to the Large Detector Concept, and will be discussed in the following as the detector option for the ILC. A global overview of the TESLA detector is shown in Figure 1.3. A combined

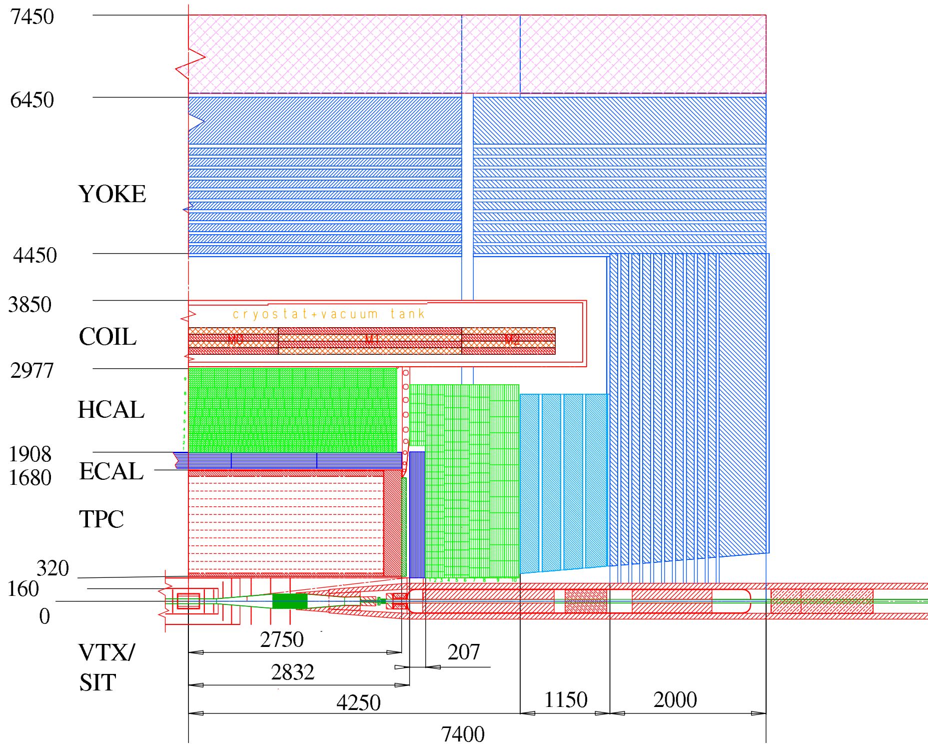

Figure 1.3: Schematic drawing of one quadrant of the TESLA detector. All dimensions are in mm. The magnetic flux return yoke is instrumented as a muon detector.

tracking system (VTX/SIT and TPC) forms the central part of the detector, enclosed by an electro magnetic (ECAL) and a hadronic calorimeter (HCAL). A strong magnetic field of 3-4 T is provided by a coil to measure the momentum of charged particles and to force the pair production background to small radii. Both calorimeters are placed inside the coil to reduce the amount of material in front of the detectors. The muon chambers are housed in the magnet flux return yoke. They are also used as a tail catcher for hadronic showers outside the HCAL. The first choice for their detector technology is based on resistive plate chambers (RPC) [14]. Special emphasis in the detector design has been made to establish the capability of independent track reconstruction for the different detector components. Although full information of all detector parts will be used for physics analysis, standalone track reconstruction is advantageous for the mutual alignment of the components and to reduce track ambiguity. The subsequent sections will give a brief overview of some detector components.

Tracking System

The different components of the tracking system are shown in Fig. 1.4. A pixel vertex

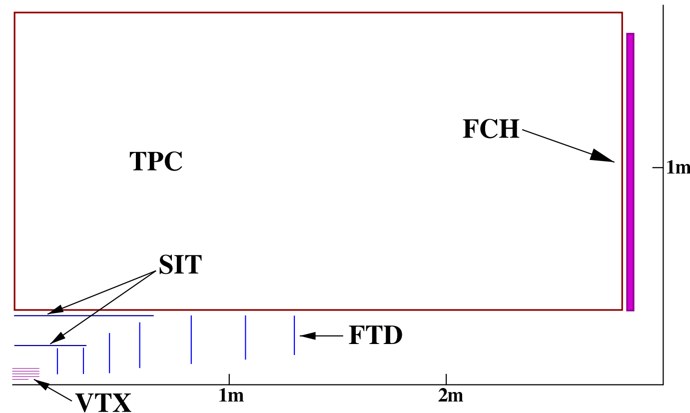

Figure 1.4: Schematic overview of the tracking system of the TESLA detector (see text).

detector (VTX), the innermost part of the tracking system is placed as close as possible to the interaction point to provide an excellent impact parameter resolution. The requirements on the vertex detector as well as the baseline design will be discussed in detail in section 1.4. Outside the vertex detector, a large time projection chamber (TPC) is foreseen. The TPC is a gaseous chamber which is read out at the side via a fine segmented endplate. The lateral drift time in the chamber is in the order of 50 μs. Hence, superimposing 150 bunch crossings for one readout causes no difficulties to disentangle single events. Even in a dense track environment, the TPC provides an efficient and robust track finding due to the large number of precise spatial coordinates measured along the track. Simultaneously, the TPC offers particle identification via the specific energy loss (dE/dx) in the gas volume with an energy resolution of about 5 %. For the readout of the TPC different options based on gas avalanche micro detectors are currently under investigation. So called gas electron multiplier foils (GEM) [15] or Micromegas [16] are discussed which offer various advantages compared to a conventional readout using wire chambers.

To compensate the degraded track reconstruction performance of the TPC in the forward direction additional forward chambers (FCH) in form of strawtubes are proposed. To further improve the momentum resolution of the tracking system, two layers of silicon strip detectors (SIT - Silicon Intermediate Tagger) are inserted in the gap between vertex detector and TPC. The layers are located at a radius of 36 cm and 64 cm respectively and have a strip pitch of 10 μm in rϕ and z direction. For low angular tracking seven forward discs (FTD) are laterally assembled along the beam pipe. The first three layers of this system are based on pixel sensors, whereas the outer discs consist of strip detectors. Altogether, the tracking system will provide a momentum resolution of $\delta(1/\mathrm{p_t}) = 5 \cdot 10^{-5}\,\mathrm{GeV}^{-1}$, which is a factor of ten better than achieved with the LEP detectors.

Calorimetry

The primary issue of the calorimeter system is to reconstruct the energies of single particles and particle jets as precise as possible. In a typical multi jet event approximately 65 % of the total energy consists of charged particles, about 25 % is composed of photons and about 10 % of neutral hadrons. The momenta of charged particles are measured in the tracking system. The energy of photons and electrons are measured in the ECAL and the energy of hadrons is measured using both the ECAL and the HCAL. Hence, an efficient jet reconstruction combines the information of the tracking system with the clusters found by the calorimeter. This method, known as energy flow algorithm, critically depends on the separation ability of different showers in the calorimeters. Thus, besides a good energy resolution, the granularity of the calorimeters becomes equally important.

For the electro-magnetic calorimeter two alternatives are discussed, a silicon tungsten (SiW) calorimeter and a lead-scintillator sandwich with a shashlik readout. The SiW calorimeter consists of 40 layers, each using tungsten as absorber material and silicon for detection of the electromagnetic showers. Due to the high density of tungsten, an overall absorption of 24 radiation lengths will be realized within only 20 cm detector thickness. The SiW layers are transversely segmented into $1 \times 1\,\mathrm{cm}^2$ readout cells well matched to the Molière radius of 9 mm in tungsten. Although this fine three dimensional segmentation of the calorimeter leads to an overall number of 32 million readout channels, the excellent granularity of the calorimeter makes it possible to track the direction of e.g. photons, which becomes important for processes where the photon does not originate from the interaction point. Simulation studies for photons between 3 and 30 GeV showed that an angular resolution of $68\,\mathrm{mrad}/\sqrt{\mathrm{E}} \oplus 8\,\mathrm{mrad}$ is achievable [17]. With the calorimeter being about 2 m away from the interaction point, this number translates into an impressive standalone impact parameter resolution for the SiW ECAL of a few centimeters.

The lead-scintillator option is a sandwich calorimeter consisting of 140 layers. Each layer being 1 mm thick, is constructed by alternating lead and scintillator plates. Although the absorber and scintillator tiles are approximately $20 \times 10\,\mathrm{cm}^2$ large, a transverse segmentation in the order of $3 \times 3\,\mathrm{cm}^2$ is achieved by confining the scintillation light within smaller sections of the plate. The light confinement is achieved by cutting grooves into the plates. The segments are connected by wavelength shifting (WLS) fibers and read out by photodetectors. Although all segments are connected to the same readout channel a longitudinal segmentation is possible by using scintillators with different decay times for the front and for the back parts of the calorimeter. For the first 30 layers, corresponding to $5\,\mathrm{X}_0$[1] scintillators with a decay time of 250 ns will be used, which is much larger than the decay time of 10 ns for the residual layers. The timing information of the response signal can then be used to disentangle the segments. For further signal processing fast photomultiplier and WLS-fibers are used, in order not to deteriorate the separation of the fast and the slow scintillator signal. To further increase the longitudinal

[1] X_0: radiation length in the material.

granularity of the calorimeter three silicon layers are proposed at certain depths to get additional information about the shower development.

Both ECAL options, the SiW as well as the shashlik one provide the required energy resolution in the order of

$$\frac{\sigma_{\mathrm{E}}}{E} = \frac{10\%}{\sqrt{E}} \oplus 1\%$$

The SiW calorimeter offers a much better spatial resolution. The shashlik sandwich calorimeter on the other hand, is supposed to be ten times cheaper.

For the hadronic part of the calorimeter two proposals are competing as well. The basic mechanical setup for both is equal, since they are constructed as a sampling calorimeter. 20 mm thick stainless steel plates offering a low magnetic permeability are used as absorbers. Overall, about 40 plates divided into 9 segments in longitudinal direction provide an absorption of $4.5\,\lambda$ in the barrel region. The main difference between the two discussed options is the detection of the hadronic showers.

In case of the first option, the tile calorimeter uses scintillator plates transversely segmented into $5 \times 5\,\mathrm{cm}^2$ units. The scintillation light is absorbed and converted by wavelength shifting (WLS) fibres and is read out by photodetectors. In case of the second option, the “digital HCAL”, the detection medium is made of resistive plate chambers or wire chambers operated in limited Geiger mode. They are read out in a binary mode without using pulseheight information. Due to the low occupancy an efficient zero suppression can be performed inside each cell and a serial readout mode can be realized. The basic idea of the digital HCAL is to have a very fine segmentation, so that a binary readout mode already leads to a spatial resolution comparable to an analog readout with coarser segmentation. Therefore, the digital version proposes a transversal segmentation of $1 \times 1\,\mathrm{cm}^2$. For both options an energy resolution in the order of

$$\frac{\sigma_{\mathrm{E}}}{E} = \frac{35\%}{\sqrt{E}} \oplus 3\%$$

can be achieved.

Forward Region

In the forward region, shown in Fig. 1.5, the mask shields the tracking components from backscattered particles that are produced in the quadrupole area by secondary processes of the beam background. The mask is made of tungsten and carbon due to their good absorption properties. To extend the hermeticity of the detector system to smaller angles, the mask is instrumented with additional calorimetrical elements. First, the luminosity calorimeter (LCAL) covering polar angles from 27.5 mrad down to 5 mrad, is a radiation hard tungsten sampling calorimeter primary intended to monitor the luminosity of the beam. It is located at both sides of the beam pipe and absorbs a large part of the incoming $\mathrm{e}^+\mathrm{e}^-$ pair production background. Since the number of pairs

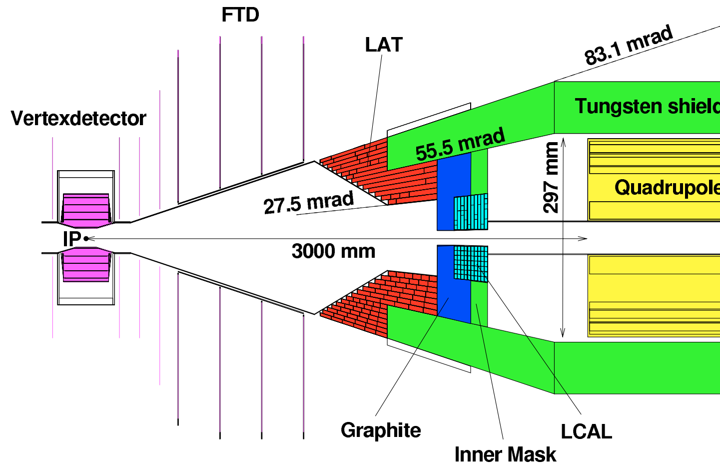

Figure 1.5: Detailed overview of the forward region of the TESLA detector. The LCAL, LAT and the forward disks (FTD) are shown. The vertical scale has been stretched [13].

and their energy is very sensitive to luminosity variations, the LCAL signal can be used as a feedback signal to tune the beam delivery system [18]. Second, the low angle tagger (LAT) covering polar angles from 83 mrad down to 27.5 mrad, is placed at the tips of the tungsten mask.

1.4 Design considerations of the vertex detector

In this section the vertex detector, the innermost part of the tracking system of the ILC detector will be discussed in more detail. The requirements on the vertex detector are leading to a baseline design, which is independent of the technological realization. In chapter 5, a proposal for the ILC vertex detector based on DEPFET pixels will be presented. Except for the different strength of the magnet fields having an impact on the pair production background, the baseline design is similar for all three ILC-detector options (LDC, SiD, GLD).

1.4.1 Beam related pair production background at the ILC

Electron-Positron colliders are often associated with low background rates and clean signatures in their detectors compared to hadron ones. However, the detector components at the ILC machine have to cope with a severely higher background environment than the previous ones at LEP or SLC due to the highly focused beam and the high particle density in the beam. By reducing the beam dimensions, the emission of beamstrahlung increases. The beamstrahlung occurs due to the focusing character of the two colliding bunches of complementary charge, known as pinch effect bending the beam to a smaller size. The dependence of the energy loss δ_{BS} caused by beamstrahlung on the beam di-

mension $\sigma_{\mathrm{x,y,z}}$, the number of particles per bunch N and the Lorentz factor $\gamma = \mathrm{E/mc^2}$ is given by [19]

$$\delta_{\mathrm{BS}} = \frac{\Delta E}{E} \propto \frac{\gamma}{\sigma_{\mathrm{z}}} \left(\frac{N}{\sigma_{\mathrm{x}} + \sigma_{\mathrm{y}}} \right)^2 \tag{1.3}$$

At the ILC, a beam size of $553 \times 5\,\mathrm{nm}^2$ is envisaged, compared to $130 \times 6\,\mu\mathrm{m}^2$ realized at LEP. One reason for the well focused beam and the high particle density in the beam is the requirement on the luminosity of $5.8 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at 800 GeV. The luminosity $\mathcal{L}$ can be expressed in terms of the machine and beam parameters

$$\mathcal{L} = \frac{n_{\mathrm{b}} N^2 \nu_{\mathrm{rep}}}{4\pi\sigma_{\mathrm{x}}\sigma_{\mathrm{y}}} \times H_{\mathrm{D}} \tag{1.4}$$

where n_{b} is the number of bunches per train, N is the number of particles per bunch, ν_{rep} is the train repetition rate and $\sigma_{\mathrm{x,y}}$ are the transverse dimensions of the beam in the plane at z=0. The focusing character of the pinch effect is considered by the factor H_{D}.

Hence, the luminosity is inversely proportional to the product of the beam dimensions, whereas the energy loss due to beamstrahlung is inversely proportional to the square sum of the beam dimensions only. Therefore, an elliptical beam shape is chosen to achieve a high luminosity at lowest possible beamstrahlung. Furthermore, the beamstrahlung photons are very well collimated around the beam axis and leave the detector inside the beam pipe. However, secondary particles are produced by the photons and have an impact on the detector components.

For the vertex detector the dominant background due to beamstrahlung is pair production. Pair production via the interaction of a photon with the collective field of the oncoming bunch is called coherent pair production [20] whereas the production via the interaction with the field of an individual particle is called incoherent pair production [21]. In case of the ILC machine, the contribution due to coherent pair production is negligible [22]. For incoherent pair production three processes, as shown in Fig. 1.6 contribute. The Breit-Wheeler process describes the interaction of two real photons, the

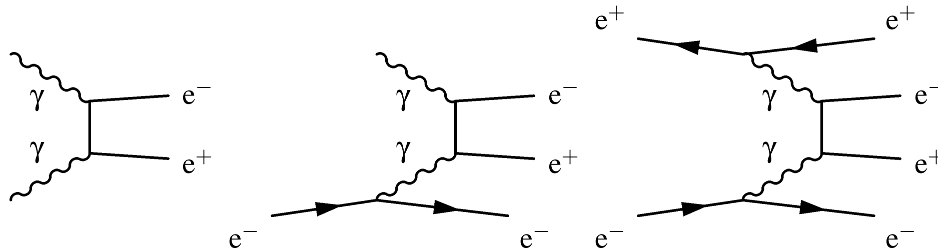

Figure 1.6: Feynman diagrams for incoherent pair production: Breit-Wheeler, Bethe-Heitler and Landau-Lifschitz process (from left to right).

Bethe-Heitler process describes the interaction of one real and one virtual photon and the Landau-Lifschitz process is the interaction of two virtual photons. The produced

e^+e^- pairs are less well collimated as the beamstrahlung photons and are partly deflected in the detector. However, due to their low energy they are constrained on a cone with small radius in the high magnetic field of 3-4 T. Consequently, the background rate strongly peaks close to the interaction point and falls rapidly beyond. Figure 1.7 shows the hit density due to the pair background for different distances from the interaction point [23]. The beam pipe of the collider machine is foreseen at a radius of r=15 mm,

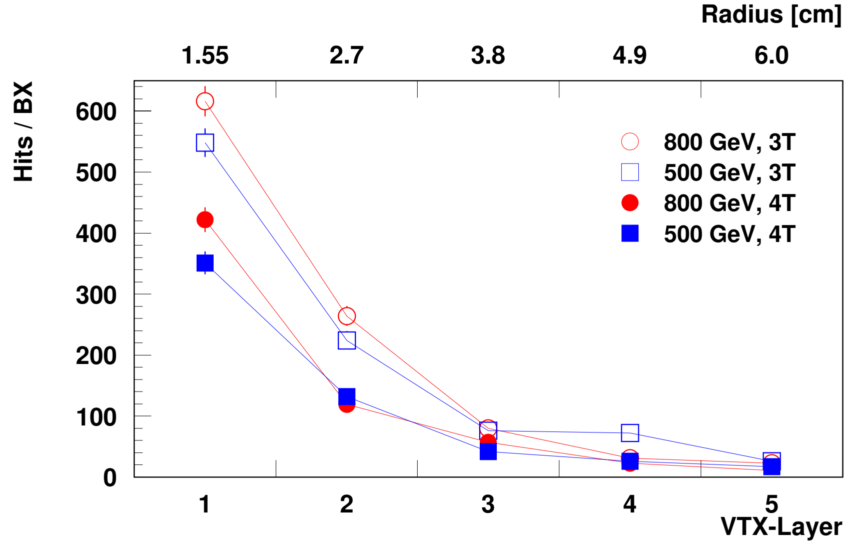

Figure 1.7: Number of hits per bunch crossing (BX) due to pair production at different distances from the interaction point for various center of mass energies and magnetic field strengths [23].

constituting a limit for the innermost layer of the vertex detector. The background rate at this point is approximately 500 hits per bunch crossing (BX) for 800 GeV resulting in a hit density of 0.05 hits per BX and mm^2. This particle flux, although low compared to hadron colliders like the LHC, has to be taken into account in the design of the vertex detector. In particular, the pair background has an impact on the readout speed and the radiation tolerance of the detector components.

1.4.2 Baseline design of the vertex detector

The ILC vertex detector will provide a major opportunity for flavor identification. B-quark and charm-tagging and even more sophisticated methods such as the separate identification of quark and anti-quark jets for both b- and charm-quarks using vertex charge technique will become possible. The baseline design of the vertex detector is driven by this physics motivation. Detailed studies to optimize the detector design are done by the LCFI[2]-Group. The proposed baseline design is shown in Fig. 1.8 and is almost independent of the detector technology used. It consists of a series of nested

[2]**L**inear **C**ollider **F**lavour **I**dentification

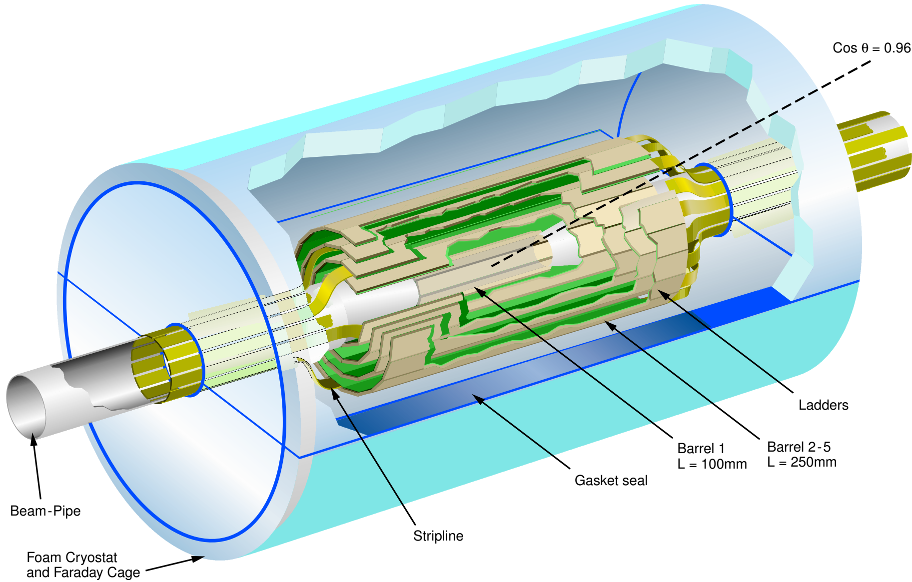

Figure 1.8: Baseline layout of the ILC vertex detector [24].

low mass spherical barrels at 5 different radii. The ladder extends in length to cover a polar angle range of $|\cos\theta| \leq 0.96$ for layer 1 and 2 and $|\cos\theta| \leq 0.90$ for layer 3-5. One key parameter that has been studied in detail is the impact parameter resolution of the detector. For a set of cylindrical detector layers, the impact parameter resolution $\sigma\left(d_0\right)$ can be expressed as

$$\sigma\left(d_0\right) = \sqrt{a^2 + \left(\frac{b}{p \cdot \sin^{\frac{3}{2}}\theta}\right)^2} \tag{1.5}$$

The constant a depends on the spatial resolution and geometrical stability of the detector and b represents the resolution degradation due to multiple scattering, which varies with the track momentum p and polar angle θ. Although the typical impact parameter of a b-hadron is approximately $300\,\mu$m, allowing a moderate detector performance, the typical impact parameter of a tau or charm particle are 3-4 times smaller. Furthermore, the detector should permit the correct assignment of nearly all tracks to the primary, secondary and tertiary vertices. Therefore, the innermost layer is placed as close as possible to the interaction point, right outside the beam pipe at r=15 mm and a pixel size of well below $50 \times 50\,\mu\text{m}^2$ is required to provide a spatial resolution in the order of $3-4\,\mu$m. Furthermore, the material budget of a detector layer should not exceed 0.1 % of a radiation length to reduce multiple scattering. Even in a TeV-scale collider machine the typical energy of particles in the jets (depending on the physics process) is in the region of 1-2 GeV. The reconstruction of tracks with low momentum is especially important for measuring the vertex charge where all tracks, including those with low momentum need to be assigned correctly. Figure 1.9 shows simulated impact parameter resolutions in rϕ-plane as a function of the particle momentum for different detector designs [25]. With a 5 layer design covering a radius from 15 mm to 60 mm and a material budget of $0.064\,\%\,\text{X}_0$ per layer a resolution of $\sigma\left(\text{d}_0\right) = (3.9 \oplus 7.8/\text{p} \cdot \sin^{\frac{3}{2}}\theta)\,\mu$m can be achieved.

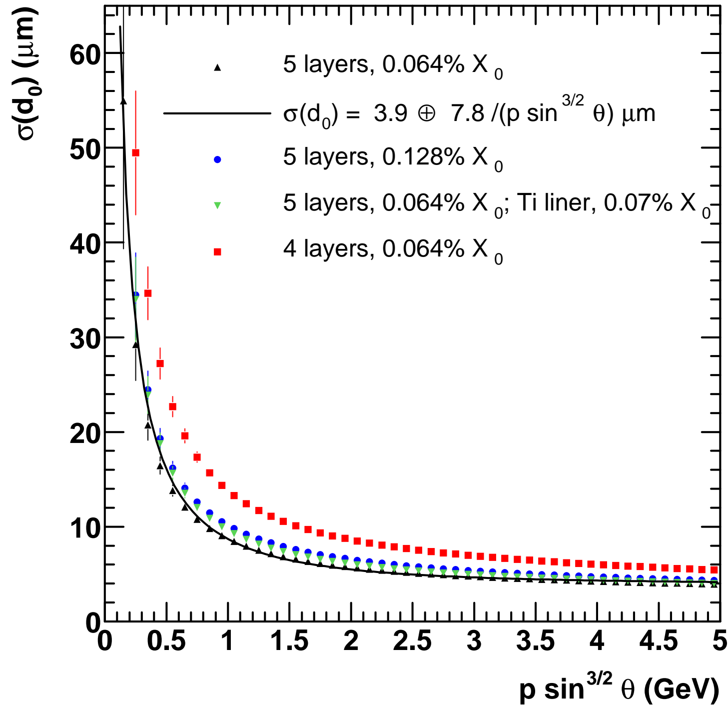

Figure 1.9: Impact parameter resolution $\sigma\,(\mathrm{d}_0)$ in rϕ-plane as a function of the particle momentum for different detector options [25].

The impact parameter resolution decreases slightly if the same detector geometry is used and the material budget is doubled. Leaving out the innermost layer, on the other hand, decreases the impact parameter resolution significantly. It has been shown in [26] that a much better resolution is required for an efficient c-tagging performance. Consequently, the required vertex detector at the ILC starts as close as possible to the beam pipe covering a radius up to 60 mm for robust track fitting. The material budget is of minor importance but should not exceed a level of $\approx 0.1\,\%$ per layer.

By placing the innermost layer at r=15 mm, the level of e^+e^- pair production background becomes high enough to affect the readout scheme of the detector. Since the accelerating technology of the ILC has been decided to be a superconducting one, it is very probable that the time structure of the bunch will be given by the one set by the TESLA accelerator [9]. As shown in Fig. 1.10 the bunches are divided into bunch trains of 950 μs length, containing 2820 bunch crossings with a bunch gap of 199 ms. Having a

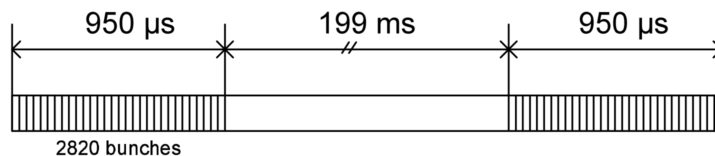

Figure 1.10: Bunch timing scheme of the ILC accelerator.

bunch spacing of only 337 ns it is not possible to adapt the readout rate of the detector

to each bunch crossing without introducing a hybrid sensor design processing every pixel in parallel. On the other hand, integrating over a whole bunch train leads to an occupancy that will compromise track finding. With a background density of 0.05 tracks per bunch crossing and mm^2 in the innermost layer, the integrated occupancy will be 26 %, assuming a pixel size of $25 \times 25\,\mu\mathrm{m}^2$ and a typical cluster multiplicity of 3 pixel per background track. To keep the occupancy at a reasonable level of about 1 % as required for robust track finding, the innermost layer has to be read out 20 times per bunch train implying a readout time of $50\,\mu$s. The outer four layers, where the background is much lower, are read out every $250\,\mu$s. Due to the negligible occupancy there, a standalone track reconstruction in the vertex detector is possible. This is advantageous for the internal alignment of the vertex detector itself and offers an efficiency monitoring of the other tracking components, notably the SIT and the TPC.

2 The DEPFET sensor

The DEPFET (**DEP**leted **F**ield **E**ffect **T**ransistor) detector is one of the technology options presently discussed for a vertex detector at the ILC. The DEPFET concept has been proposed in 1987 [27]. Apart from particle physics the detector is used in fields of biomedical imaging [5] and for spectroscopy applications in X-ray astronomy [28]. The DEPFET consists of a sidewards depleted silicon sensor with an integrated amplifier realized by a Field-Effect-Transistor (FET). To meet the requirements at the ILC, a dedicated DEPFET pixel sensor production has been fabricated in 2004 at the Semiconductor Laboratory of the MPI Munich. The basic principle of operation of the detector as well as possible readout options for a DEPFET pixel matrix with respect to the ILC requirements will be discussed in this chapter.

2.1 Sidewards depletion

The DEPFET substrate is depleted by means of sidewards depletion [29]. The principle of sidewards depletion is shown in Fig. 2.1. Here, the sensor is not just a single pn-junction (n-substrate, p-backside), but consists of a pnp-sandwich (p frontside-implantation, n-substrate, p-backside). The n-substrate in the middle is used as a common reference (often called bulk). By applying negative voltages to both p-implantations with respect to be substrate, the detector volume is depleted from both sides of the pn-junctions. After full depletion of the detector volume, a potential minimum for electrons occurs at a plane parallel to the front. Solving the one-dimensional Poisson equation with the given boundary conditions ($\varphi(0) = V_{\mathrm{u}}$, $\varphi(d) = V_{\mathrm{d}}$), yields the potential distribution φ as a function of the depth z in the detector substrate

$$\varphi(z) = \frac{qN_{\mathrm{D}}}{2\epsilon_{\mathrm{s}}} z\,(d-z) + \frac{z}{d}\,(V_{\mathrm{d}} - V_{\mathrm{u}}) + V_{\mathrm{u}} \tag{2.1}$$

where q is the elementary charge, N_{D} is the doping concentration of the substrate, d is the total wafer thickness, ϵ_{s} is the dielectric constant of the semiconductor and V_{d}, V_{u} are the voltages applied to the back and the front side, respectively. Thus, the depth of the potential minimum z_{min} is given by

$$z_{\mathrm{min}} = \frac{d}{2} + \frac{\epsilon_{\mathrm{s}}}{q\,N_{\mathrm{D}}\,d}\,(V_{\mathrm{d}} - V_{\mathrm{u}}) \tag{2.2}$$

If both voltages are chosen equally, the potential minimum is formed in the middle of the detector. By applying asymmetric voltages, the potential minimum can be shifted

in the depth arbitrarily. The principle of sidewards depletion is commonly used in semiconductor drift chambers [29]. In case of the DEPFET detector, sidewards depletion is used for the local accumulation of charge generated in the detector substrate.

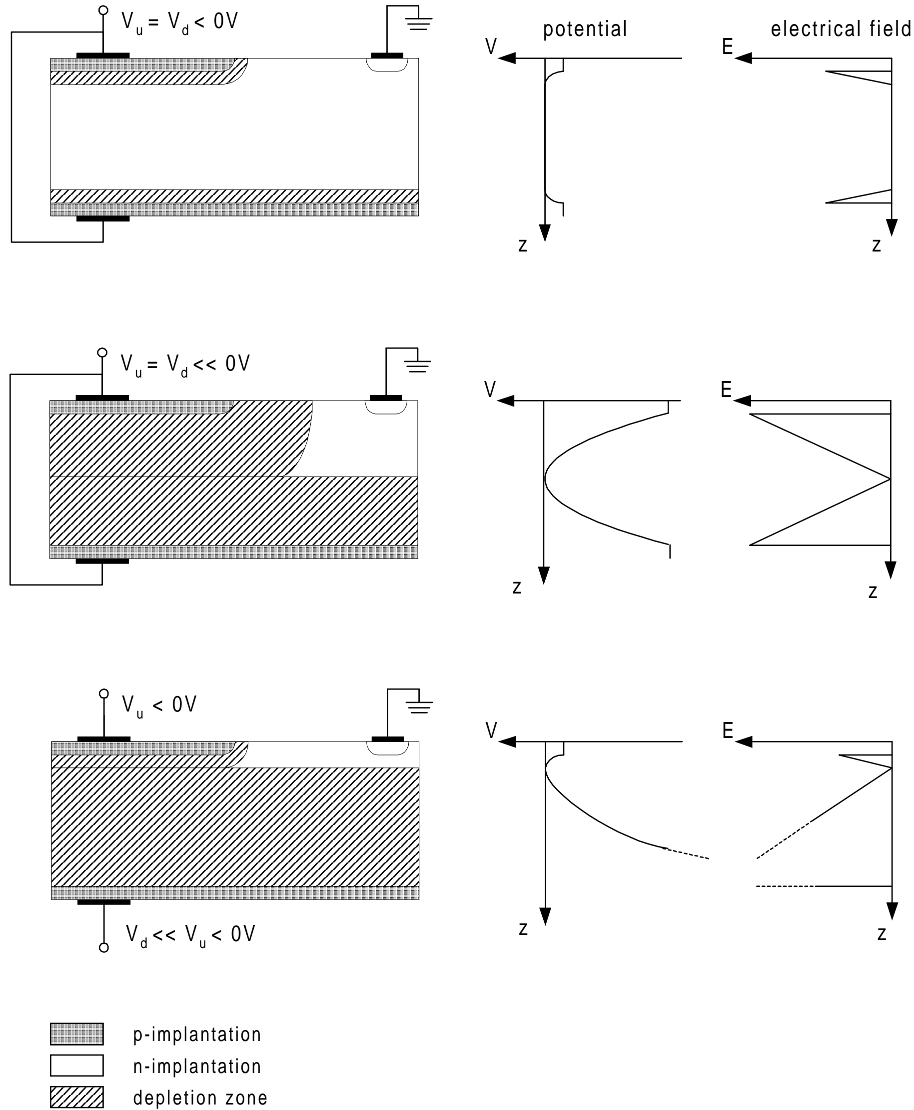

Figure 2.1: Principle of the sidewards depletion (left). Distribution of the resulting electrical field (right) and the potential (middle) in the detector substrate for different biasing conditions.

2.2 Principle of operation of the DEPFET detector

The DEPFET detector belongs to the family of active pixel devices. That means that the detector itself provides a first amplification stage for the generated charge. In case of the DEPFET, the amplification stage is realized by a FET that is embedded into the silicon

substrate. Figure 2.2 shows a cross section of a DEPFET pixel using a MOSFET[1] for amplification. The detector substrate is fully depleted by means of sidewards depletion.

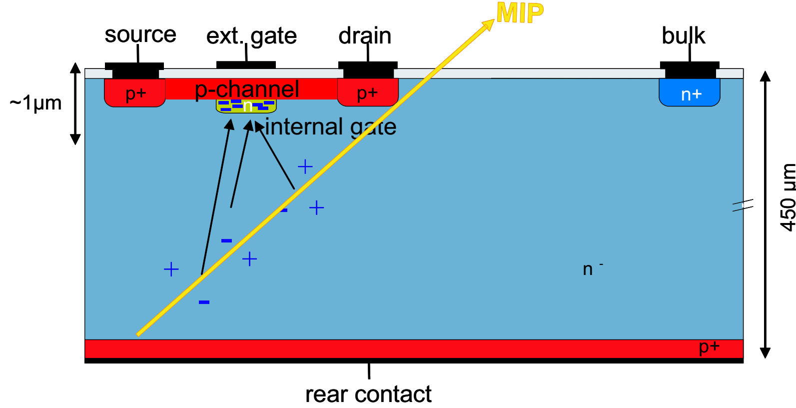

Figure 2.2: Cross section of a DEPFET pixel through the transistor channel, illustrating the principle of operation.

Due to asymmetric voltages at the transistor channel (≈ -5 V) and the detector backside (≈ -100 V), the potential minimum plane for electrons is shifted very close to the detector surface, where the embedded transistor is located. By additional n-implants below the transistor, the potential minimum is confined laterally. Hence, a local minimum is formed directly underneath the transistor channel, at a position where the external gate of the transistor is located. This potential minimum is considered as an internal gate of the transistor. If electron-hole pairs are generated in the depleted substrate by impinging radiation, the holes drift to the backside implantation and the electrons are accumulated in the internal gate. Since the collecting mechanism is based on an electric drift field, charge collection is intrinsically fast and complete. The collected charge changes the potential of the internal gate. Similar to the bulk-effect known for FET transistors, the potential of the internal gate modulates the transistor channel. For a fixed drain-source voltage, this leads to a variation of the transistor current. By probing the transistor current at two different times, the collected charge during the time period can be obtained by subtracting both currents. Another readout mode is to operate the device in a source-follower configuration. Both methods will be treated in section 2.4. The following will focus on the drain readout only, since it offers much faster operation being a crucial issue at the ILC.

The figure of merit of the DEPFET device read out in current mode, is the amplification of the charge in the internal gate. The amplification g_q is given by the change of the transistor current ∂I_D due to the collected charge ∂Q

$$g_\mathrm{q} = \left.\frac{\partial I_\mathrm{D}}{\partial Q}\right|_{V_\mathrm{GS},V_\mathrm{DS}} \tag{2.3}$$

for a given gate-source voltage V_GS and drain-source voltage V_DS. As shown in [30] the internal amplification can be expressed in terms of the hole mobility μ_h and of the

[1]**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor

transistor gate length L for a given saturation voltage of the transistor $V_{\mathrm{DS}}^{\mathrm{sat}}$

$$g_{\mathrm{q}} = -\frac{\mu_{\mathrm{h}}}{L^2} V_{\mathrm{DS}}^{\mathrm{sat}} \tag{2.4}$$

Like for the transconductance of MOS transistors, the internal amplification can be maximized by choosing a small gate length. Figure 2.3 shows the simulated internal amplification of a DEPFET sensor as a function of the effective gate length L_{eff} using the two dimensional simulation tool TeSCA [31]. For the present ILC-DEPFET production

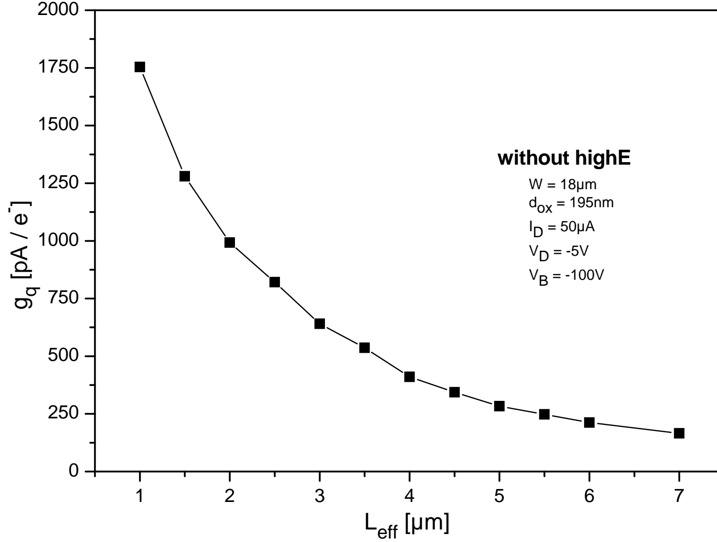

Figure 2.3: Simulation of the internal amplification g_q of a DEPFET device as a function the effective gate length using the TeSCA simulator [31].

which uses a conservative design with a gate length of $4\,\mu$m, an internal amplification of $400\,\mathrm{pA/e^-}$ is expected. By reducing the gate length to the present technological limit of $2\,\mu$m in future productions, an internal amplification up to $1\,\mathrm{nA/e^-}$ should be possible.

The simultaneous detection and amplification feature makes the DEPFET attractive for low noise applications, like biomedical imaging and spectroscopy in X-ray astronomy. For a vertex detector application at a particle collider the low noise can be exploited by fabricating thin devices. The low noise is obtained since the input capacitance of the amplifying transistor, given by the capacitance of the internal gate, is very small. Typical values are in the order of a few femtofarad. Furthermore, no external connection circuitry to the amplifier is needed, where electromagnetic interference (EMI) may deteriorate the signal. For individual pixel structures, the best noise figures achieved so far are ENC=$2.2\,\mathrm{e^-}$ at room temperature using signal shaping with a shaping time of $\tau_{\mathrm{s}} = 6\,\mu$s [4]. For the ILC, where high readout speed is required, a total noise of about $100\,\mathrm{e^-}$, including sensor and readout components is a realistic goal. Even with a $50\,\mu$m thin DEPFET device providing a MIP[2] signal of about $4000\,\mathrm{e^-}$, this noise figure yields an excellent signal to noise ratio of 40. The expected noise performance for a fast DEPFET readout operating at speed suited for the ILC will be discussed in detail in section 5.5.

[2]**M**inimum **I**onizing **P**article

2.3 Clear operation of the device

To remove the charge, accumulated in the internal gate, the DEPFET device is equipped with a reset mechanism. The removal of the charge from the internal gate is known as clearing. To illustrate the clear operation, a cross section of a DEPFET pixel perpendicular to the transistor channel is shown in Fig. 2.4. The clear process is performed

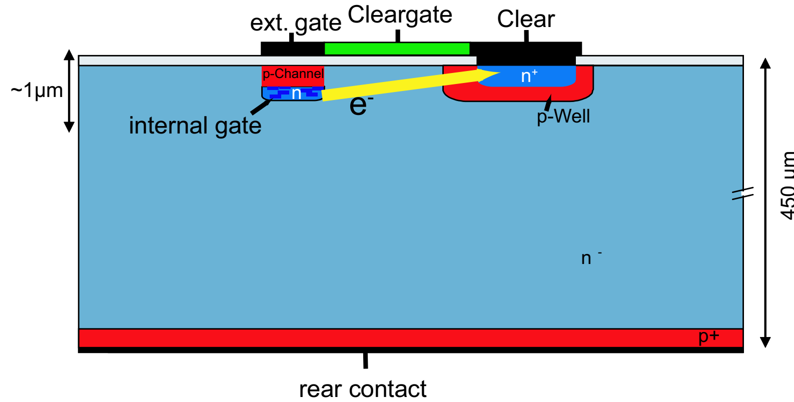

Figure 2.4: Cross section of a DEPFET pixel perpendicular to the transistor channel (view from drain to source) showing the clear principle of the device. Present devices are 450 μm thick, for the ILC a thickness of 50 μm is proposed.

by a clear contact, located at the side of the transistor channel. By applying a high positive voltage to the clear contact, the potential minimum moves from the internal gate to the clear contact. Hence, the electrons drift to the clear contact where they are removed. The implantation underneath the clear contact is highly n-doped (n^+) to make the region more attractive for electrons and to provide an ohmic contact to the clear electrode. The n^+-region is embedded in a p-well forming a reverse biased pn-junction. Due to the high voltage applied to the clear contact during clearing, the pn-barrier is overcome via the punch through effect [33] and the charge is removed from the internal gate. During charge collection though, when a low voltage is applied to the clear contact, the n^+-implantation is shielded by the p-well and charge loss via the clear contact is prevented.

To improve the clear process an additional cleargate, as shown in Fig. 2.4 is implemented. The cleargate is a MOS structure that controls the potential distribution in the substrate between the clear contact and the internal gate. In principle, the cleargate potential can be pulsed, as for the clear contact. That means that different voltages are possible during the clear process and during charge collection. For a fast operation at the ILC however, it would be desirable to hold the cleargate at a static potential, so that no additional steering strobe is necessary. Operating the device with a static cleargate is especially difficult since two very different requirements during charge collection and clear process have to be fulfilled by one cleargate potential. Choosing the cleargate potential too low leads to an inefficient clear process. If the cleargate potential is chosen too high, the substrate underneath the cleargate attracts electrons. Consequently, a potential pocket

is formed that competes with the internal gate regarding charge collection. This leads to an incomplete charge collection in the internal gate.

To optimize this delicate balance, part of the wafer production was doped by an unmasked deep high energy (highE) phosphorous implantation (not shown in Fig. 2.4). Due to this implantation, the sequence of the clear process is shifted deeper into the substrate (at around $1\,\mu$m depth), instead of taking place at the surface where the influence of the cleargate is dominant. On the one hand, a more efficient operation using a static cleargate and significantly lower clear voltages are expected by introducing the highE implantation. On the other hand, the highE implantation shifts the internal gate slightly away from the transistor channel. Due to the reduced capacitive coupling of the internal gate to the transistor channel, the internal amplification of a device with highE is expected to be lower compared to a device without highE. The issue of building devices with a fast and complete clearing ability offering a similar amplification to non-highE devices at the same time, will be addressed in the next DEPFET production.

The removal of all charge from the internal gate is known as complete clear. A complete clear is attractive since the device is hence always reset to the very same pedestal current and no additional reset-noise occurs. Furthermore, the pedestal current is stable and can be probed as a reference after any clear. This enables an efficient readout mode for the ILC, see section 3.1. For the operation at the ILC moreover, the clear process has to be performed very fast, in the order of 10 ns.

The efficiency of the clear process with respect to different clear and cleargate voltages for various design options with and without highE has been studied in detail and is reported in [34] and [32]. It has been shown that complete clearing is possible within a very short time interval of 10 ns using a static cleargate potential [34].

2.4 Readout principles for DEPFET pixel

In principle, there are two different readout modes for a DEPFET device, a current based readout at the drain and a voltage based readout at the source. Both principles are illustrated in Fig. 2.5 and will be discussed in the following.

Source-follower readout

In the case of a voltage based readout, the DEPFET device is operated through a source-follower stage, as shown in Fig. 2.5 (left). Here, a constant current $\mathrm{I_B}$ is applied to the transistor. Charge accumulated in the internal gate, dQ_{in}, is detected as a voltage swing dU at the source of the DEPFET. The amplification G of the source-follower configuration is approximately given by [35]

$$G = \frac{dU}{dQ_{\mathrm{in}}} = \frac{1}{C_{\mathrm{GD}}} \tag{2.5}$$

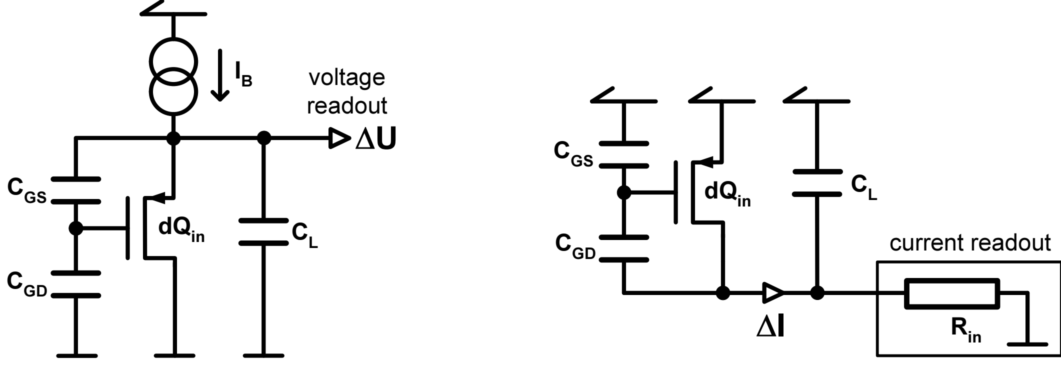

Figure 2.5: Two possible readout concepts for a DEPFET pixel: A voltage based readout using a source-follower configuration (left) and a current based readout at the drain of the transistor (right).

where C_{GD} is the gate-drain capacitance of the DEPFET detector. The gain is independent of the gate-source capacitance C_{GS} of the DEPFET, as V_{GS} remains constant due to the unity voltage gain of the source-follower. Thus, C_{GD} should preferably be small to obtain a large amplification. The settling time τ, the time in which the output signal reaches about 63 % of its peak value, is approximately given by [35]

$$\tau \approx \frac{C_{\mathrm{L}}\left(1+\frac{C_{\mathrm{GS}}}{C_{\mathrm{GD}}}\right)+C_{\mathrm{GS}}}{g_{\mathrm{m}}} \tag{2.6}$$

where g_{m} is the transconductance of the DEPFET and C_{L} is the load capacitance at the readout node. In a row wise operation mode of a DEPFET matrix as needed at the ILC, see section 2.5, the load capacitance given by the readout bus is in the range of a few picofarad and dominates the numerator in equation (2.6). For example, the expected capacitive load of a 64×128 pixel matrix is already 10 pF, whereas the gate capacitances are in the range of a few femtofarad. The transconductance g_{m} of the transistor is limited due to the feature sizes of the DEPFET technology process, where a transistor with a gate length of $\mathrm{L} = 2\,\mu\mathrm{m}$ is already at the present technological limit. Furthermore, g_{m} is preferably kept low to minimize the thermal noise contribution of the DEPFET transistor. For typical values of C_{L}=10 pF, C_{GD}=10 fF, C_{GS}= 100 fF and $g_{\mathrm{m}} = 40\,\mu\mathrm{S}$ the settling time is $\tau = 2.8\,\mu\mathrm{s}$, which is far-off the timing requirements needed to operate DEPFET matrices at a row rate of 20 MHz or more at the ILC, see section 5.1.

Current readout at the drain

In case of the drain readout, shown in Fig. 2.5 (right) the drain-source voltage of the device is kept constant. As described in section 2.2, the transistor current dI_{D} is then modulated by the accumulated charge dQ_{in} according to the amplification g_{q} of the internal gate

$$dI_{\mathrm{D}} = g_{\mathrm{q}} dQ_{\mathrm{in}} \tag{2.7}$$

The settling time of the output signal is hence given by

$$\tau = C_{\mathrm{L}} \cdot R_{\mathrm{in}} \tag{2.8}$$

for load capacitances C_{L} being much larger than the gate capacitances C_{GS} and C_{GD}. In this configuration, the readout speed is no longer limited by the transconductance g_{m} of the DEPFET transistor, as it was the case for the source-follower readout. For a given load capacitance, the settling time can be optimized by providing a low input impedance of the succeeding current readout. Since this circuitry is fabricated using standard CMOS technologies, the input impedance can be kept very small. According to equation (2.8), an input resistance of 100 Ω for a load capacitance of 10 pF yields a rise time of τ=1 ns, compared to about 2.8 μs for the source-follower stage. Thus, for a very fast operation as needed at the ILC, only a current readout at the drain is possible. The succeeding readout chip for such a configuration would be, in the ideal case, based on currents only, converting the signals into voltages only at the very end of the readout chain. For that reason, a completely current based readout architecture has been chosen for the ILC readout, as will be discussed in chapter 3.

2.5 Operation of a DEPFET matrix

In principle, several DEPFET pixels can be arranged in a matrix where each pixel is processed in parallel by attaching a readout chip to the sensor using bump bond techniques [36]. In such a hybrid design, as used e.g. for the ATLAS pixel detector [37], each pixel is read out by an individual channel in the electronic chip. For smaller matrices or in an environment where elaborate cooling can be used, this design may be viable and advantageous regarding the readout speed. However, with a total number of 510 MPixels at the ILC vertex detector, this readout mode leads to an unacceptable power consumption, see section 5.3. Furthermore, active cooling cannot be used in the sensitive area, as a minimum material budget is mandatory to reduce multiple scattering effects.

Since the transistor of the DEPFET pixel does not need to be enabled during the charge collection process in the internal gate, a row wise operation of the matrix is possible where a pixel is switched on only for readout. The principle of operating a DEPFET matrix in a row wise mode is illustrated in Fig. 2.6. The matrix is arranged in a way where all external gate and clear contacts are connected row wise. The drains of the pixel transistors are connected column wise. The rows can be selected one after each other by a steering chip attached at the side of the matrix and the transistor currents are probed column wise at the matrix bottom by the readout chip. The clearing of the internal gate is performed for a complete row at a time. Both steering functions, row selection and clear, can be integrated in one chip so that a single steering chip has to be placed on one matrix side only. By processing row after row, the whole matrix can be read out. A description of the steering chip, SWITCHER II can be found in [38]. The

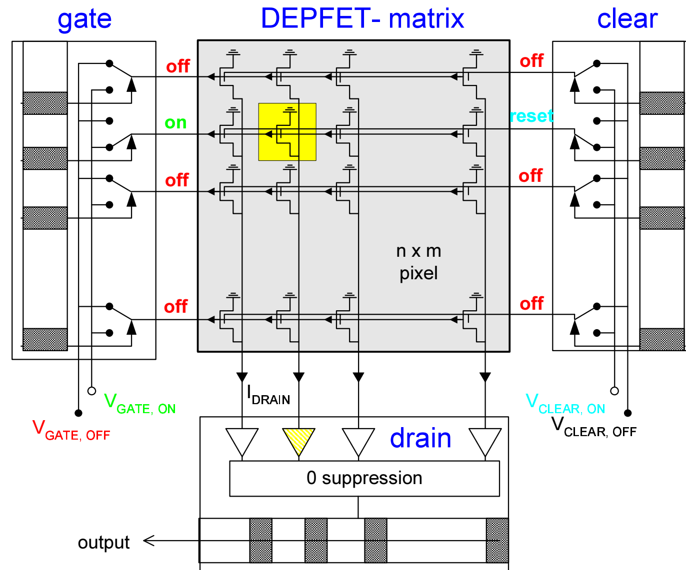

Figure 2.6: Readout principle of a DEPFET matrix in a row wise operation with steering chips at the side of the matrix and a readout chip at the bottom.

design and the performance of the readout chip, CURO II will be treated in chapters 3 and 4.

Since only a few transistors are activated for readout at the same time, the power consumption can be significantly reduced. Consequently, no intensive cooling is needed and the material in the sensitive area is given by the sensor and the steering chips only. To reach a minimum material budget, the sensor can even be thinned to a few ten microns thickness. On the other hand, this operation mode imposes a high row rate since the readout time of the whole module is given by the sum of the processing time for all rows. For the ILC vertex detector, the required readout time of 50 μs translates into a row rate of 20 MHz. A more detailed discussion of the concept of a DEPFET pixel based vertex detector and the power consumption will be presented in chapter 5.

2.6 DEPFET production for the ILC

Dedicated DEPFET pixel matrices with respect to the requirements for the ILC have been designed and fabricated at the MPI Semiconductor Laboratory in Munich in 2004. The requirements concerning the sensor production are mainly a small pixel size of $20 \times 20\,\mu\text{m}^2$ to $30 \times 30\,\mu\text{m}^2$ and the possibility of producing large matrices with up to 4000×500 pixels (for the innermost layer). To fulfill these requirements, the technology of the DEPFET production moved from the previous JFET to a MOSFET realization of the implanted transistor for several reasons. First, the pixel-to-pixel dispersion is smaller for MOS production than for JFET production due to the self-alignment properties of the process. This is an essential requirement for the production of large scale matrices with up to 2 MPixels. Second, the cleargate structure needed for a fast and efficient

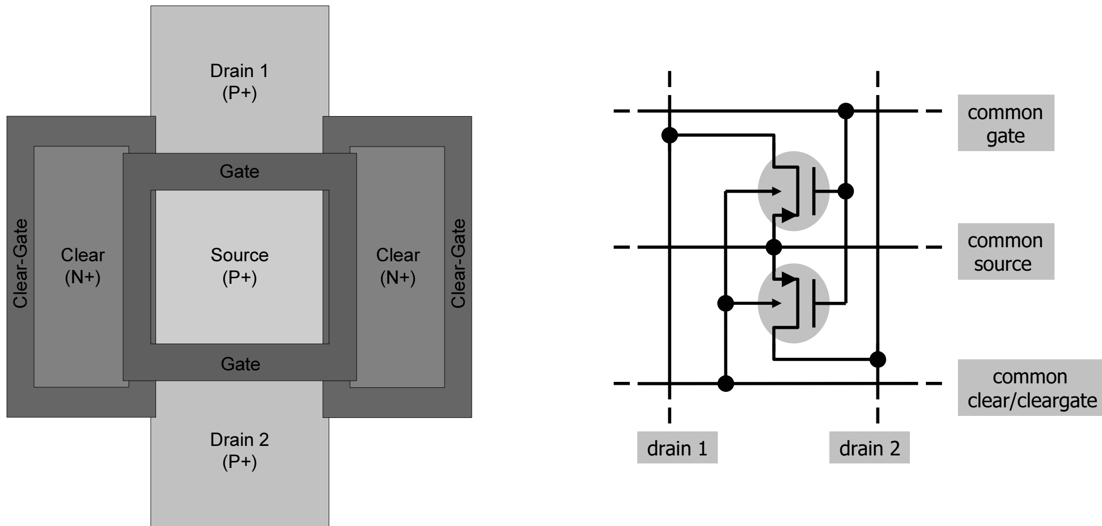

Figure 2.7: Simplified geometry of a DEPFET double-pixel structure (left). Circuit showing the control and readout lines of a double-pixel structure (right).

clear performance can only be implemented as a MOS structure. Furthermore, the MOS technology offers the possibility of fabricating rectangular pixel cells. Although the realization of circular transistors is much easier, rectangular structures offer higher integration capability. A schematic overview of a rectangular DEPFET structure is given in Fig. 2.7 (left). In order to achieve a maximum integration density, the matrices are arranged in double-pixel structures sharing a common source implantation. The source potential is common for all pixels in the matrix. The clear contacts, located at both sides of the pixel, are joined between neighboring pixels in a row. In a matrix also the drain regions are joined between pixels arranged upon each other in a column. Since only one row is activated at a time, the drain currents of both pixels do not interfere. Both transistors of the double structure are steered by common clear and gate lines, as illustrated in Fig. 2.7 (right). Depending on the design, the cleargate can be arranged row wise as for clear and gate, or all cleargates are connected for the whole matrix if the cleargate can be kept at a static potential. Every double-pixel provides two drain lines which are read out in parallel. Although the rectangular pixel design offers high integration density, a lateral channel isolation between neighboring pixels is needed. Commercial CMOS processes make use of a LOCOS (local oxidation) or a box channel isolation for this purpose. Since the cleargate structure controls the potential at the side of the transistor channel anyway, it can act as an isolating gate to prevent a parasitic drain to source current.

In the latest production, matrices with up to 64×128 pixels, more precisely 64 double-pixels leading to 128 readout channels, have been fabricated. Due to the very compact design of the double-pixel structure, pixel sizes down to $24 \times 33\,\mu\text{m}^2$ have been achieved. Yield measurements on test structures have shown that a pixel pitch of $25\,\mu$m in both dimensions is feasible in the next production [31]. Measurements using a 64×128 DEPFET pixel matrix from the present production will be presented in chapter 6.

3 Design of the CURO readout chip

The ILC vertex detector imposes several requirements on the readout of a DEPFET matrix. This above all comprises a row rate of 20 MHz and a noise performance in the order of ENC=100 e^-. These requirements need to be met also by the readout chip. Since the ILC detector will be operated without a first level trigger, hit detection and zero suppression is ideally made on chip. In this chapter, a new readout concept for a fast readout of a DEPFET pixel matrix facing these requirements is described, the CURO architecture. The architecture is completely current based and perfectly adapted to the signal output of the DEPFET device. The major building blocks of the architecture as well as their design aspects will be discussed in detail. These blocks are mainly: a current memory cell for temporal storage of a current, a regulated cascode providing a low impedance input stage, a current comparator for hit detection and a hitscanner for zero suppression.

3.1 Readout scheme at the ILC

The principle readout scheme of a DEPFET sensor matrix is shown in Fig. 3.1. The

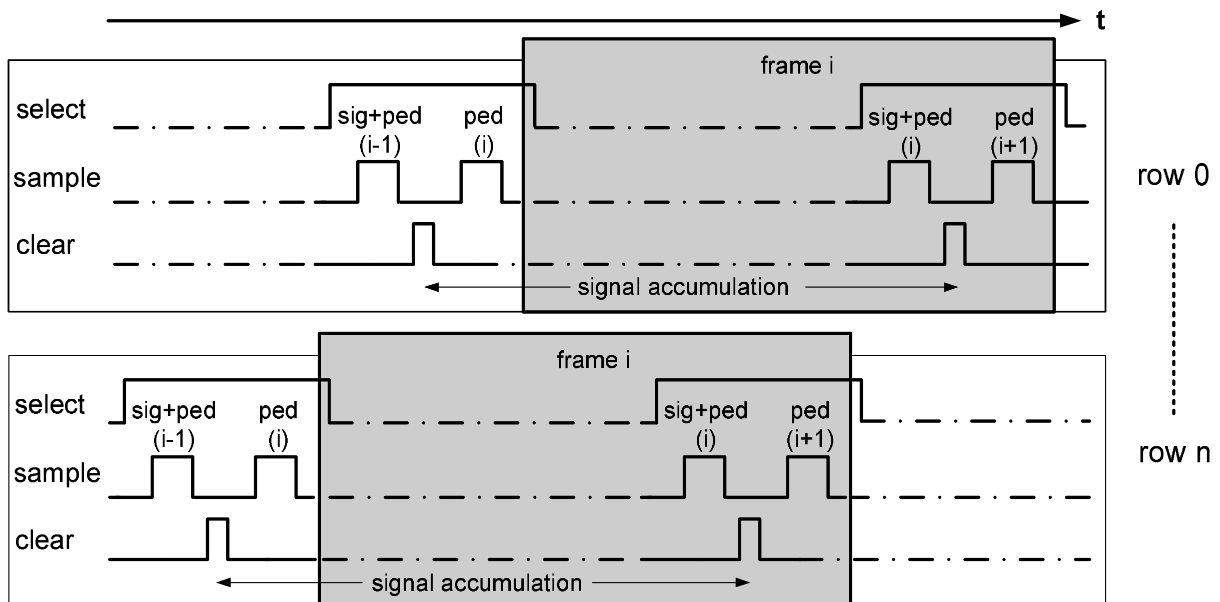

Figure 3.1: Principle readout scheme of a DEPFET sensor matrix operated row wise.

matrix is read out row wise, whereas the signal accumulation for one row comprises the following steps:

- The row is cleared and the pedestal current $I_{ped,i}$ is sampled.
- After an integration time in which the other rows of the matrix are processed (frame time), the row is selected again and the signal current superimposed on the pedestal current $I_{sig,i} + I_{ped,i}$ is sampled.
- By subtracting both values the signal current $I_{sig,i} = (I_{sig,i} + I_{ped,i}) - I_{ped,i}$ is obtained.

For most of the applications the subtraction of both samples can be done off-line. For the triggerless operation and the readout rates as required at the ILC however, zero suppression of the data is crucial. Hence, the pedestal subtraction has to be done on-chip. Unfortunately, the pedestal currents for all pixels of a matrix cannot be stored on the chip during the integration time. However, assuming a stable pedestal ($I_{ped,i} = I_{ped,i+1}$) due to a complete clear, the pedestal value of the next frame can be taken as a reference and the pedestal subtraction can be done during a single row cycle. The signal current of the current frame $I_{sig,i}$ is then given by

$$I_{sig,i} = (I_{sig,i} + I_{ped,i}) - I_{ped,i+1}$$

A further advantage of this readout scheme is that the performed correlated double sampling (CDS) is more powerful in suppressing 1/f noise of the sensor, see appendix A, because the time interval between both samples is much shorter.[1] On the other hand, this readout scheme requires a complete clear of the sensor to ensure that the pedestal level is stable. Otherwise, an additional noise contribution (generally known as reset noise) due to remaining charge in the internal gate after the clear, has to be considered. A complete clear has already been demonstrated for several matrix designs [34].

3.2 Architecture of the CURO chip

Since a fast readout is one of the crucial points at the ILC, a current-mode operation was chosen, the CURO (**CU**rrent **R**ead**O**ut) architecture. With the output of a DEPFET for a fast drain readout being a current, optimal further processing of the signal is achieved, if it is current based. Furthermore, a very convenient and accurate subtraction of two currents, needed for the pedestal subtraction, is very easily done.

The readout principle of the CURO architecture is illustrated in Fig. 3.2. It consists of three major parts. An analog part, a mixed-signal FIFO and a digital part. To keep the overview clearer, only one channel is shown for the analog part and for the mixed signal FIFO in Fig. 3.2. Switches for the routing of the various currents at the junctions are

[1]The row cycle is a factor of 1000 shorter than the frame cycle.

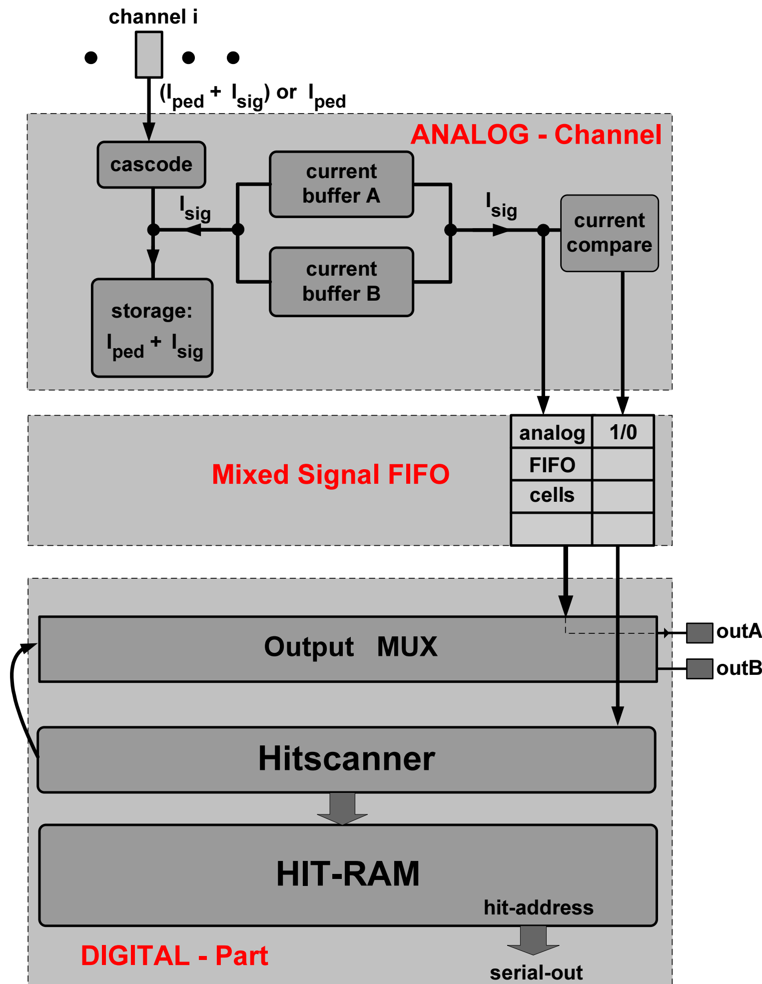

Figure 3.2: Schematic overview of the CURO-Architecture.

not shown for simplicity. During operation it is ensured that the currents are flowing only in one direction at the same time.

To provide a low input impedance for the DEPFET current the first stage of the analog part is realized by a regulated cascode. The readout of one matrix row is performed as follows:

- After one row in the sensor matrix has been selected for readout, the signal current superimposed on a pedestal current $I_{sig} + I_{ped}$ is provided by the matrix and is stored in a current memory cell located right behind the cascode.
- The row is then cleared and the input of the circuit is reduced to the pedestal current I_{ped}. Since the stored value of signal and pedestal current is still provided by the memory cell, the pedestal current is automatically subtracted at the input node of the memory cell.
- The resulting signal current I_{sig} is stored alternately in two current buffer cells.

The current memory cell will be discussed in detail in section 3.3. Due to the alternating storage of the signal current in the buffer cells, the succeeding signal processing of the signal current can take three storage cycles: storage in the pedestal subtracting cell, signal storage in the other buffer cell and again, storage in the pedestal subtracting cell. After the three storage cycles the buffer cell has to be ready again for the next signal current. The succeeding signal processing comprises of hit detection and analog storage of the signal current in a FIFO. One cycle is used for the hit detection, so that two cycles remain for the analog storage.

Hit detection is performed by comparing the signal current with a programmable threshold. Afterwards, the digital hit information is stored together with the analog value in a small mixed signal FIFO. The FIFO derandomizes the hit rate fluctuations to a constant rate. Simulations show that a FIFO depth of 4-8 rows is enough to cope with the occupancy expected at the ILC, see section 3.6. The currents in the FIFO below the threshold are not relevant and the digital pattern can be used to switch off the appropriate analog FIFO cells to save power. One can think of a more sophisticated clustering logic, keeping the neighbors of a seed pixel, as well for example. Note, that the whole front end is operated by one single clock, synchronous to the row clock of the matrix. All control signals for the complex analog part are derived from this clock inside the chip.

To empty the FIFO, a fast hitscanner arranged in parallel, analyzes the digital hit pattern and finds up to 2 hits per cycle. Their addresses are stored in a Hit-RAM and the analog values are multiplexed to 2 output nodes where they are digitized by two external ADCs. The ADCs can in principle, be integrated onto the chip as well. The Hit-RAM should be large enough to store all hits of a bunch train, so that it can be read out conveniently during the long pauses between the trains. After zero suppression the expected data volume of a whole bunch train for a 128 channel chip is below 100 kB for the innermost layer, see section 3.6. The integration of an adequate RAM is therefore easy to realize. For the outer layer the amount of data will be even smaller due to the lower background rate. After the RAM is read out, the hit coordinates can be associated with the values digitized by the ADCs.

3.3 Design of a fast and accurate current memory cell

The readout architecture presented above requires the temporary storage of a current. This cannot be performed using conventional techniques. In this section the principle of a current memory cell will be discussed.

The requirements on the current storage are very challenging. On the one hand, a high bandwidth of up to 40 MHz is required (20 MHz row rate including 2 samples) while, on the other hand, the noise level should not exceed $100\,e^-$. The required noise figure can be translated into a current noise using the internal amplification g_q of the DEPFET transistor. Present devices achieve a g_q of $\approx 283\,pA/e^-$, whereas a g_q of up to $1\,nA/e^-$ can be expected from more advanced sensors designs. Hence, the noise performance

of a single memory cell should be well below 100 nA. Both design goals, a high speed operation and a low noise are not only demanding, but also contradictory with respect to the design parameters of the cell. These parameters will be discussed in the next sections to optimize the overall performance of the cell.

3.3.1 Basic principle of operation

The basic schematic of a current memory cell, as proposed in [39] is shown in Fig. 3.3 (left). The circuit consists of a memory transistor M1, in this case a nMOS, with a

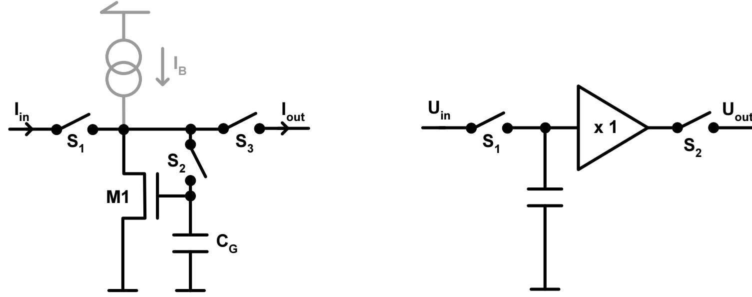

Figure 3.3: Basic principle of the current memory stage [39]. The current source I_B is not necessarily needed and therefore drawn gray (left). Conventional voltage sample and hold (right).

gate capacitance C_G, a bias current source I_B and several switches S1, S2 and S3. Note that for the current storage in general, the bias current source I_B is not needed and is therefore drawn gray. It is added mainly for two reasons. First, to allow negative input currents because a single nMOS is not able to source current. Second, to improve the linearity of the circuit by modulating a small input current on top of a larger bias.

The current sample and hold is divided into three phases:

1. In the initial state S1 and S2 are closed and S3 is open. The gate capacitance of transistor M1 is charged until the device provides the combined input and bias current ($I_{M1} = I_{in} + I_B$).

2. S2 is opened. The gate voltage and therefore the transistor current ideally remain unchanged.

3. Immediately after sampling, S1 is opened and S3 closed. As the current through M1 is still $I_{M1} = I_{in} + I_B$ and since I_B is still provided by the bias source, the remaining I_{in} must be delivered by the output node to satisfy Kirchhoff's current law.

Thus, in the ideal case the sampled output current is an inverted copy of the input current: $I_{out} = -I_{in}$. The non-ideal effects of the circuit leading to a sampled output current deviating from the input current will be treated later on.

Although the sampled value in the current memory cell is a voltage, given by the gate voltage at the storage transistor, the circuit offers several advantages compared to a conventional voltage sample and hold shown in Fig. 3.3 (right). First, the voltage sampled at the capacitance is not directly proportional to the input signal, as it is the case for the voltage sampler because the drain current I_{D} of a FET in strong inversion is to first order a function of the square of the effective gate source voltage $V_{\mathrm{G}} = V_{\mathrm{GS}} - V_{\mathrm{th}}$

$$I_{\mathrm{D}} = \frac{\beta}{2}(V_{\mathrm{GS}} - V_{\mathrm{th}})^2 \quad (3.1)$$

where β is the transistor gain and V_{th} is the threshold voltage. Due to the quadratic dependence, the occurring voltage swing is small. This is advantageous when going to submicron technologies with reduced supply voltages, where the current based circuit can potentially offer a larger dynamic range than the voltage sampler. Furthermore, a current mode sample stage does not need any driver to transfer the sampled value from one point to another. Since the requirements on the driver, which is required in the voltage mode, have to meet the ones of the sampling stage, such a design is not trivial, especially if good linearity at high speed is needed. In case of the current mode sample and hold such a driver is provided automatically. In addition, no quality requirement exists for the storage capacitance. For voltage sample and hold stages special analog processes are chosen that provide very linear capacities that are needed for high accuracy sampling. In case of the current sample circuit the sampling capacitance, inherently given by the gate capacitance of the MOS device needs no quality requirements. This allows the realization of analog circuitry with excellent performance within digital processes, which are cheaper to fabricate.

The main disadvantage of the current mode is that a current can flow only into one single node at the same time. If the current value is needed more than once, current mirrors are needed. The design of a dynamic current mirror, providing high bandwidth and high linearity, is as challenging as the design of the memory cell itself. In the voltage domain, a signal can be probed in parallel without any deteriorating effects.

The simple circuit shown in Fig. 3.3 (left) suffers from some non-ideal effects that have to be taken into account if the required performance should be achieved. The main effects are:

- A finite output conductance of the transistor M1 and the biasing current source.
- A finite settling behavior of the circuit.
- kT/C-sampling noise.
- Charge injection due to the sample switch S2.

In the following sections these effects and their minimization will be discussed.

3.3.2 Cascode circuit

Since the voltage at the drain node of the sampling transistor is not constant during the operation of the memory cell, the limited output conductance of the transistor cause non-linear errors in the transfer characteristic of the cell. During the charging phase of the circuit, see Fig. 3.3 (left) with S1, S2 closed and S3 open, the voltage at the drain node is given by the dioded transistor M1. After the sampling phase with S1, S2 opened and S3 closed, the drain voltage is equal to the voltage source the memory cell is switched to. Furthermore, the drain voltage of the dioded transistor in the charging phase is a function of the input current, see equation (3.1). Assuming a typical voltage swing of $\Delta V_D = 50\,\mathrm{mV}$ at the drain node and an output resistance in the order of $100\,\mathrm{k\Omega}$, a current variation of roughly $0.5\,\mu A$ is expected. For a dynamic range of $10\mu A$, this already translates into an uncertainty of 5 %.

The effect of the limited output conductance can be successfully reduced using cascode techniques [40]. Figure 3.4 shows the sampling part of the current memory cell with a simple (unregulated) cascode configuration. The sampling transistor is described by its

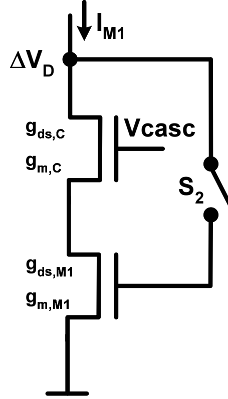

Figure 3.4: Sampling transistor M1 of the current memory cell with the sampling switch S_2. A cascode transistor is integrated to improve the output conductance.

transconductance $g_{\mathrm{m,M1}}$ and its output conductance $g_{\mathrm{ds,M1}}$. To lower the output conductance of the circuit a cascode transistor is added. The cascode transistor is described by its transconductance $g_{\mathrm{m,C}}$, its output conductance $g_{\mathrm{ds,C}}$ and is biased by V_{casc}. The voltage swing at the drain node is indicated by ΔV_D. By using the unregulated cascode, the output conductance of the circuit is lowered by the grounded source voltage gain of the cascode transistor. Hence, the low-frequency (DC) output conductance g_{ds} of the cascoded stage, neglecting the bulk effect is given by [40]

$$g_{\mathrm{ds}} = g_{\mathrm{ds,M1}} \left(\frac{g_{\mathrm{ds,C}}}{g_{\mathrm{ds,M1}} + g_{\mathrm{ds,C}} + g_{\mathrm{m,C}}} \right) \approx g_{\mathrm{ds,M1}} \left(\frac{g_{\mathrm{ds,C}}}{g_{\mathrm{m,C}}} \right) \tag{3.2}$$

It has been assumed that the transconductance of the memory transistor $g_{\mathrm{m,C}}$ is much larger than the output conductances of the memory and cascode transistor $g_{\mathrm{ds,C}}$, $g_{\mathrm{ds,M1}}$.

Due to the improved output conductance, the current variation caused by the voltage swing is reduced. Typical values for the ratio $g_{\mathrm{ds}}/g_{\mathrm{m}}$ of transistors can be as high as 100, reducing the former 5 % current variation to a negligible effect.

An even lower output conductance can be achieved using a regulated cascode circuit, see section 3.4. However, in the design an unregulated cascode has been used since its improvement is sufficient and the increased circuit complexity and the higher power consumption due to the active feedback of the regulated stage are not justified.

Unregulated cascode stages have been used for the memory transistor itself, as well as for the bias current source. The aspect ratio (W/L) of the cascode transistors has been chosen to achieve a maximum $g_{\mathrm{m,C}}$, while keeping the stack of transistors in saturation.

While improving the output conductance significantly by the cascode stage, the input impedance of the circuit remains unchanged and is still approximately given by $1/g_{\mathrm{m,M1}}$. Hence, the settling behavior of the circuit is not degraded by the cascode circuit. The cascode transistor can therefore be neglected when treating the settling behavior of the cell.

3.3.3 Settling behavior

The required bandwidth of 40 MHz of the current memory cell is very high. The settling behavior will be analyzed in the following to find an optimal dynamic performance of the cell. The influence of the finite output conductance of the storage transistor will be neglected since it is significantly improved by the cascode circuit, see section 3.3.2.

Figure 3.5 shows the small signal equivalent circuit of the memory cell in the charging phase and a simplified version, neglecting the switch resistance. When the switch resis-

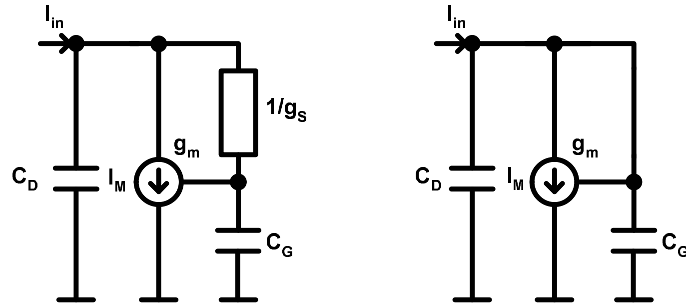

Figure 3.5: Small signal equivalent circuit of a current memory cell during the charging phase. With (left) and without (right) the sampling switch.

tance is neglected, the drain capacitance C_{D} and the gate capacitance C_{G} are lumped together. The settling behavior of this circuit, namely the settling of the gate voltage and therefore the transistor current, is given by a first order transfer function with the characteristic settling time

$$\tau = \frac{C_{\mathrm{D}} + C_{\mathrm{G}}}{g_{\mathrm{m}}} \tag{3.3}$$

Hence, fast settling is obtained by choosing a high transistor transconductance g_m and small gate and drain capacitances.

Taking into acccount the switch resistance $1/g_\mathrm{s}$ as well, leads to the small signal equivalent circuit shown in Fig. 3.5 (left). Hence, the system becomes of second order and the transfer function is given by [39]

$$H(s) = \frac{I_\mathrm{M}}{I_\mathrm{in}} = \frac{1}{1 + s\frac{C_\mathrm{D}+C_\mathrm{G}}{g_\mathrm{m}} + s^2\frac{C_\mathrm{G}C_\mathrm{D}}{g_\mathrm{m}g_\mathrm{s}}} \tag{3.4}$$

The transfer function is characterized by the frequency

$$\omega_0 = \sqrt{\frac{g_\mathrm{m}g_\mathrm{s}}{C_\mathrm{G}C_\mathrm{D}}} \tag{3.5}$$

and the pole quality factor

$$Q = \frac{\sqrt{\frac{g_\mathrm{m}}{g_\mathrm{s}}C_\mathrm{G}C_\mathrm{D}}}{C_\mathrm{G}+C_\mathrm{D}} \tag{3.6}$$

Depending on Q, the time response of the circuit can either be overdamped ($Q < 0.5$), underdamped ($Q > 0.5$) or critically damped ($Q = 0.5$). More details concerning the response of second order systems can be found in textbooks, e.g. in [41]. According to equation (3.6), the critical switch conductance g_crit, for which the response of the circuit is critically damped, is

$$g_\mathrm{crit} = \frac{4\,g_\mathrm{m}C_\mathrm{G}C_\mathrm{D}}{(C_\mathrm{G}+C_\mathrm{D})^2} \tag{3.7}$$

Figure 3.6 illustrates the response behavior of a second order system for the overdamped (left) and the underdamped (right) case. The settling error ε is defined as the difference

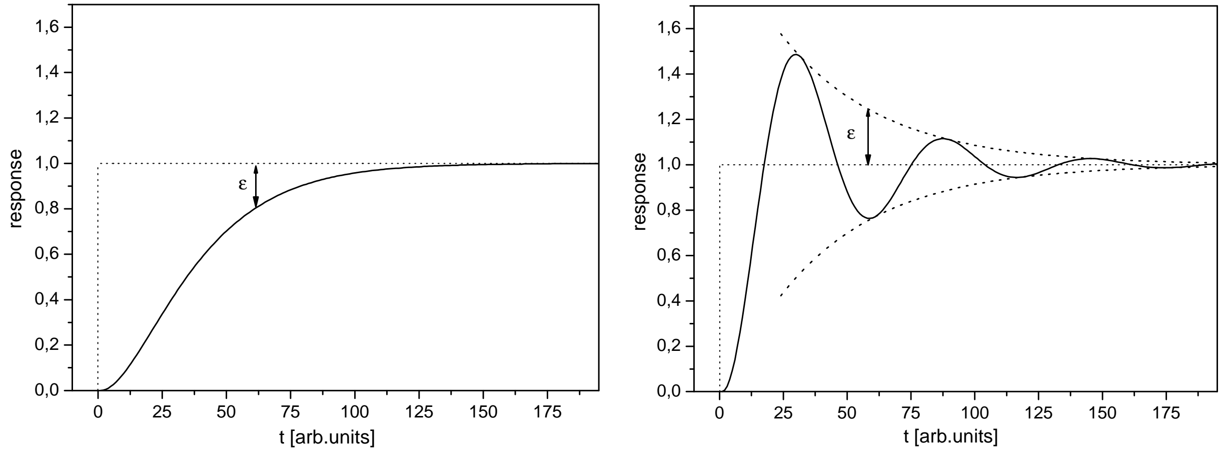

Figure 3.6: Response behavior of a second order system for the overdamped (left) and the underdamped (right) case illustrated the settling error.

between the ideal step response and the actual response at a time t. For the underdamped response, the envelope of the exponential decaying overshoot has been assumed

for the settling error, as shown in Fig. 3.6 (right). The settling error ε, normalized to the step height as a function of g_s/g_{crit} after a settling time of t=15 ns is shown in Fig. 3.7. For the system frequency $\omega_0 = 500 \cdot 10^6\,\mathrm{s}^{-1}$ has been used. The case of minimum switch

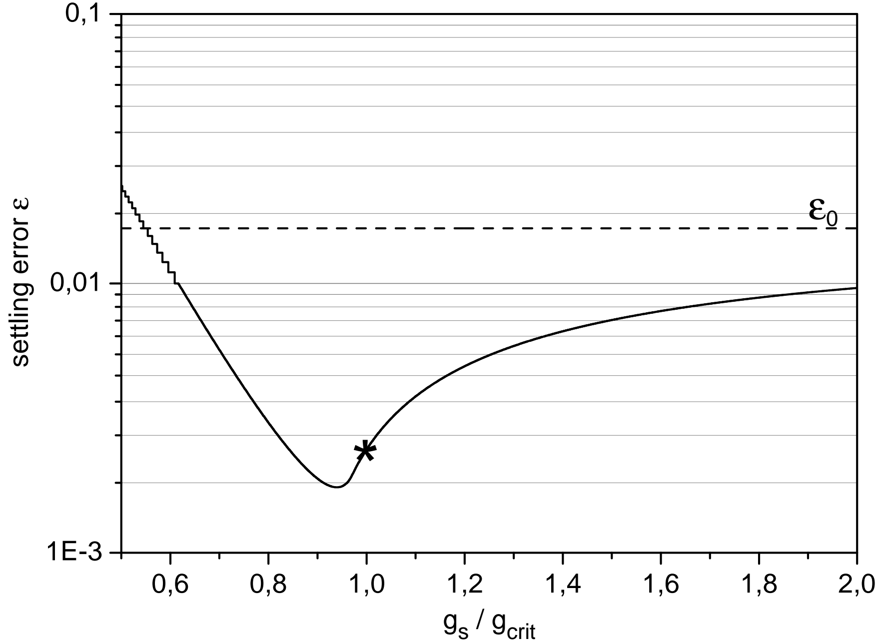

Figure 3.7: Normalized settling error ε of a second order system ($\omega_0 = 500 \cdot 10^6\,\mathrm{s}^{-1}$) after t=15 ns as a function of g_s/g_{crit}. ε_0 indicates the limit for $g_s/g_{crit} \rightarrow \infty$. The star indicates the settling error for the critical switch conductance.

resistance, which is the limit for $g_s/g_{crit} \rightarrow \infty$ is given by ε_0. From Fig. 3.7 it can be observed that $\varepsilon(g_s/g_{crit})$ is a lot smaller than ε_0 over a wide range of g_s/g_{crit}, demonstrating that minimum switch resistance is not the ideal case. This is due to the separation of both capacitances, C_D and C_G, by the switch and the active feedback by the transistor. Although a minimum settling error is obtained for the slightly underdamped response, the critically damped case is preferred in practice due to design uncertainties which have to be considered. Hence, the switch conductance should be chosen according to equation (3.7) to obtain critically damping (aperiodic settling) of the circuit.

3.3.4 Noise analysis of a basic current memory cell

In this section the noise contribution of the sampling process by the current memory cell will be analyzed. The noise originates from a fluctuation of the gate voltage of the memory transistor during the sampling phase due to different noise sources in the circuit. At the end of the sampling phase, the noise voltage is stored at the gate capacitance and results in a current noise at the output. Figure 3.8 shows the different noise sources that have been considered in this analysis. The noise of the memory transistor itself is modeled by the voltage source V_M and the noise of the switch transistor is given by V_R.

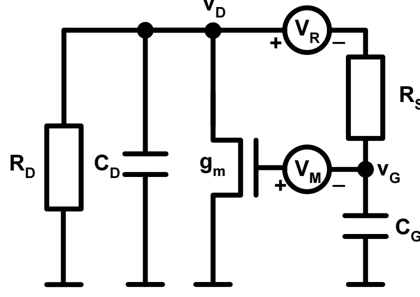

Figure 3.8: Noise sources considered for the noise analysis of the circuit.

Since this section will focus on the sample noise only, the noise contribution of the bias current source is not considered here. It will be added in quadrature to the sample noise in section 3.3.6 to obtain the total noise of the memory cell.

Summing all currents at the drain node v_{D} yields

$$\frac{v_{\mathrm{D}}}{Z_{\mathrm{D}}} + (v_{\mathrm{G}} + V_{\mathrm{M}})\, g_{\mathrm{m}} + \frac{v_{\mathrm{D}} - V_{\mathrm{R}}}{R_{\mathrm{S}} + \frac{1}{sC_{\mathrm{G}}}} = 0 \tag{3.8}$$

where Z_{D} is the drain impedance given by the parallel connection of the drain capacitance C_{D} and the output resistance R_{D}

$$Z_{\mathrm{D}} = \frac{R_{\mathrm{D}}}{1 + sR_{\mathrm{D}}C_{\mathrm{D}}} \tag{3.9}$$

By applying Kirchhoff's loop law

$$v_{\mathrm{D}} = V_{\mathrm{R}} + v_{\mathrm{G}}\,(1 + sR_{\mathrm{S}}C_{\mathrm{G}}) \tag{3.10}$$

and using equation (3.8), an expression for the voltage at the gate capacitance v_{G} is derived

$$v_{\mathrm{G}} = -\frac{V_{\mathrm{R}}}{g_{\mathrm{m}}Z_{\mathrm{D}} + 1 + s\,C_{\mathrm{G}}(R_{\mathrm{S}} + Z_{\mathrm{D}})} - \frac{V_{\mathrm{M}}}{1 + \frac{1 + s\,C_{\mathrm{G}}(R_{\mathrm{S}} + Z_{\mathrm{D}})}{g_{\mathrm{m}}Z_{\mathrm{D}}}} \tag{3.11}$$

The first part of equation (3.11) is related to the switch resistance noise, whereas the second part is related to the transistor noise. Both parts will be evaluated separately in the following.

Noise due to the switch resistance

Substituting the drain impedance Z_{D} from equation (3.9) in equation (3.11), the switch part becomes

$$v_{\mathrm{G,R}} = -\frac{V_{\mathrm{R}}}{g_{\mathrm{m}}R_{\mathrm{D}} + 1}\,\frac{1 + s\,C_{\mathrm{D}}R_{\mathrm{D}}}{1 + s\frac{C_{\mathrm{D}}R_{\mathrm{D}} + C_{\mathrm{G}}R_{\mathrm{S}} + C_{\mathrm{G}}R_{\mathrm{D}}}{g_{\mathrm{m}}R_{\mathrm{D}} + 1} + s^2\frac{C_{\mathrm{G}}R_{\mathrm{S}}C_{\mathrm{D}}R_{\mathrm{D}}}{g_{\mathrm{m}}R_{\mathrm{D}} + 1}} \tag{3.12}$$

where the second fraction in equation (3.12) correponds to a transfer function with two poles and one zero. To calculate the mean square value of the gate voltage, the squared modulus of equation (3.12) is integrated over all frequencies. Using the noise integral from appendix B.3 and the voltage power spectral density of a resistance, given by $V_R^2 = 4kTR_S$, $\langle v_G^2 \rangle_R$ can be expressed as

$$\begin{aligned} \langle v_G^2 \rangle_R &= \frac{4kTR_S}{(g_m R_D + 1)^2} \frac{1}{4} \frac{g_m R_D + 1}{C_D R_D + C_G R_S + C_G R_D} \left(1 + \frac{C_D^2 R_D^2 (g_m R_D + 1)}{C_G R_S C_D R_D}\right) \\ &= \frac{kT}{C_G} \frac{1}{g_m R_D + 1} \frac{C_D R_D (g_m R_D + 1) + C_G R_S}{C_D R_D + C_G R_S + C_G R_D} \end{aligned} \quad (3.13)$$

The following assumptions will now be used to simplify equation (3.13):

$$\begin{aligned} R_D &\gg R_S \\ g_m R_D &\gg 1 \\ \Rightarrow \frac{C_D}{C_G} \frac{R_D}{R_S} (g_m R_D) &\gg 1 \end{aligned}$$

Using these assumptions[2], equation (3.13) reduces to

$$\langle v_G^2 \rangle_R \approx \frac{kT}{C_G} \frac{C_D}{C_D + C_G} \quad (3.14)$$

Note, that for a fixed drain voltage, which can be achieved by setting $R_D = 0$ or $C_D \to \infty$ in equation (3.13), the circuit becomes a voltage sample and hold cell and the switching noise at the gate capacitance is given by

$$\langle v_G^2 \rangle_{R_D=0} = \langle v_G^2 \rangle_{C_D \to \infty} = \frac{kT}{C_G} \quad (3.15)$$

This corresponds to the known kT/C noise of a voltage sample and hold cell, as expected.

Noise due to the storage transistor

Substituting the drain impedance Z_D from equation (3.9) in equation (3.11), the transistor part becomes

$$v_{G,M} = -\frac{V_M g_m R_D}{g_m R_D + 1} \frac{1}{1 + s\frac{C_G R_S + C_D R_D + C_G R_D}{g_m R_D + 1} + s^2 \frac{C_G R_S C_D R_D}{g_m R_D + 1}} \quad (3.16)$$

For the transistor, the noise analysis can focus on thermal noise only for several reasons. First, thermal noise is predominant due to the large bandwidth of the circuit. Second, large area transistors (in the order of $100\,\mu m^2$) are used for sampling which reduce

[2] Due to the cascode circuit, R_D is expected to be much larger than R_S and g_m^{-1}. This ratio cannot be compensated by realistic gate and drain capacitances, so that the last assumption is applicable.

1/f noise contributions. Finally, 1/f noise is further suppressed by correlated double sampling inherently performed by the memory cell. Thus, the voltage power spectral density of the transistor noise is given by $V_{\mathrm{M}}^2 = \frac{2}{3} 4kTg_{\mathrm{m}}^{-1}$. Calculating the mean square value of the gate voltage due to the transistor noise V_{M} yields

$$\left\langle v_{\mathrm{G}}^2 \right\rangle_{\mathrm{M}} = \frac{2}{3} \frac{kT}{C_{\mathrm{D}}} \frac{g_{\mathrm{m}} R_{\mathrm{D}}}{g_{\mathrm{m}} R_{\mathrm{D}} + 1} \frac{R_{\mathrm{D}} C_{\mathrm{D}}}{C_{\mathrm{G}} R_{\mathrm{S}} + R_{\mathrm{D}}(C_{\mathrm{D}} + C_{\mathrm{G}})} \tag{3.17}$$

Using the two pole noise integral from appendix B.2. With the assumption that $R_{\mathrm{D}} \gg R_{\mathrm{S}}$ and $g_{\mathrm{m}} R_{\mathrm{D}} \gg 1$, equation (3.17) can be approximated by

$$\left\langle v_{\mathrm{G}}^2 \right\rangle_{\mathrm{M}} \approx \frac{2}{3} \frac{kT}{C_{\mathrm{D}} + C_{\mathrm{G}}} \tag{3.18}$$

Total sampling noise of the cell

The square sum of the different noise sources at the gate of the transistor is converted to a current noise by the transconductance g_{m}, leading to a total root-mean-square at the output

$$i_{\mathrm{RMS}} = g_{\mathrm{m}} \sqrt{\langle v_{\mathrm{G}}^2 \rangle_{\mathrm{M}} + \langle v_{\mathrm{G}}^2 \rangle_{\mathrm{R}}} = g_{\mathrm{m}} \sqrt{\frac{kT}{C_{\mathrm{G}}} \left(\frac{C_{\mathrm{D}} + 2/3 C_{\mathrm{G}}}{C_{\mathrm{D}} + C_{\mathrm{G}}} \right)} = g_{\mathrm{m}} \sqrt{\frac{kT}{C_{\mathrm{G}}}} \cdot \alpha \tag{3.19}$$

As in a simple voltage sample and hold storage the noise performance of the cell is independent of the switch resistance R_{S}. Thus, the switch resistance is a degree of freedom to optimize the settling behavior of the circuit without deteriorating the noise performance.

The factor α in equation (3.19) is between 1 and $\sqrt{2/3}$, for all ratios of drain and gate capacitances. This leads to an upper limit of the sampling noise i^*_{RMS} given by

$$i^*_{\mathrm{RMS}} = g_{\mathrm{m}} \sqrt{\frac{kT}{C_{\mathrm{G}}}} \tag{3.20}$$

Furthermore, the parasitic drain capacitance C_{D} turns out to be a drawback of the circuit. On the one hand, it decreases the settling time of the cell in a similar way as the gate capacitance, see equation (3.3). On the other hand, it barely improves the noise figure of the cell.

3.3.5 Design flow

It has been shown that the gate capacitance C_{G} and the transistor transconductance g_{m} are the crucial parameters that govern the settling behavior and noise performance of the memory cell. To achieve fast settling, a large transconductance g_{m} and a small gate capacitance C_{G} is advantageous, see equation (3.3). According to equation (3.20), this

is contrary to the noise performance of the circuit. To find an optimal compromise, the settling time and sampling noise will be expressed in terms of the free design parameters of the transistor, the gate width W and length L. Afterwards, the product of sampling noise and settling time will be minimized.

The transconductance g_{m} of a transistor, loaded by a constant current I_{D} in strong inversion is given by

$$g_{\mathrm{m}} = \left.\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}}\right|_{I_{\mathrm{D}}} = \sqrt{2 I_{\mathrm{D}} c_{\mathrm{ox}}\, \mu \frac{W}{L}} \tag{3.21}$$

where μ is the carrier mobility and c_{ox} is the oxide capacitance per unit area. The total gate capacitance for a rectangular transistor in saturation is in first order given by [42]

$$C_{\mathrm{G}} = \frac{2}{3} \cdot c_{\mathrm{ox}} \cdot W \cdot L \tag{3.22}$$

Using equations (3.21) and (3.22) in equation (3.20) yields

$$i^{*}_{\mathrm{RMS}} = \sqrt{3\, I_{\mathrm{D}} \mu\, kT}\ 1/L \tag{3.23}$$

Hence, the sampling noise does not depend on the transistor width W but is given by its length L only. According to equation (3.3), the settling time τ is given by

$$\tau = \frac{\frac{2}{3}\, c_{\mathrm{ox}} W L + C_{\mathrm{D}}}{\sqrt{2 I_{\mathrm{D}} c_{\mathrm{ox}}\, \mu \frac{W}{L}}} \tag{3.24}$$

using equations (3.21) and (3.22) for the transconductance and gate capacitance, respectively.

The product of sampling noise i^{*}_{RMS} and settling time τ will be defined as the noise settling-time product (NST) and is given by

$$\mathrm{NST} \equiv i^{*}_{\mathrm{RMS}} \cdot \tau = \sqrt{kT} \cdot \sqrt{\frac{2}{3}\, c_{\mathrm{ox}} W L + 2 C_D + \frac{3}{2} \frac{C_{\mathrm{D}}^2}{c_{\mathrm{ox}} W L}} \tag{3.25}$$

The product is independent of the carrier mobility and is therefore, equal for nMOS and pMOS transistors. To find the minimal NST, the derivative of equation (3.25) with respect to the transistor width W is set to zero

$$\frac{d(\mathrm{NST})}{dW} \stackrel{!}{=} 0 \tag{3.26}$$

leading to a relation for the transistor dimensions

$$W = \frac{3}{2} \frac{C_{\mathrm{D}}}{c_{\mathrm{ox}}} \frac{1}{L} \tag{3.27}$$

Inserting equation (3.27) in equation (3.25) yields the optimal (minimal) NST-product, given by

$$\mathrm{NST}_{\mathrm{opt}} = 2\sqrt{kT C_{\mathrm{D}}} \tag{3.28}$$

The drain capacitance C_D directly limits the performance of the cell and should be reduced to a minimum. For a single memory cell the parasitic drain capacitance has been estimated to 75 fF, leading to an optimal NST-product of 35 (nA ns) at room temperature. This means for example that for a settling time of 3 ns ($\nu \approx 50$ MHz), the sampling current noise cannot be better than 12 nA.

The influence of the drain capacitance on the performance of the memory cell is particularly crucial for the design of the analog FIFO. Since the FIFO consists of several memory cells which are connected by a bus, the load capacitance is expected to be much higher than for a single memory cell. Hence, the FIFO size should be kept as small as possible to minimize the bus capacitance. However, it is advantageous that due to the two buffer cells in the analog front end, see section 3.2, the storage of the signal current in the FIFO can occupy two storage cycles. Thus, the FIFO cells are operated at half of the frequency than the other memory cells.

Radiation tolerant design using annular transistors

Using radiation tolerant layout rules with annular nMOS transistors, the aspect ratio cannot be chosen arbitrarily. Furthermore, the gate capacitance cannot be calculated using equation (3.22) since the transistor gate area is not given by the product of W and L, as extracted from the annular transistor model.

Figure 3.9 shows the measured gate capacitance as a function of the gate-substrate bias for 250 annular nMOS transistors connected in parallel. Each transistor has a width W=16.03 μm and length L=4 μm. The observed dependence corresponds to the behavior

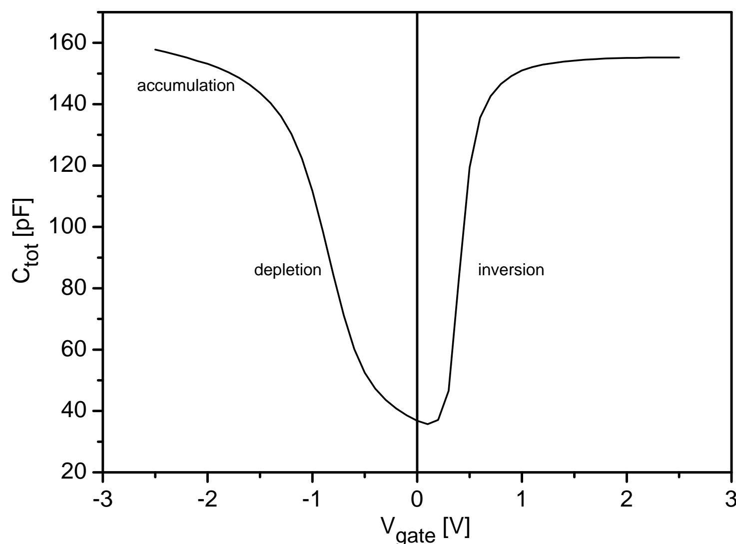

Figure 3.9: Measured total gate capacitance as a function of gate-substrate bias for 250 annular nMOS transistors connected in parallel with W=16.03 μm and L=4 μm (static behavior).

of a simple MOS capacitance. A detailed description of the MOS capacitance can be

			$I_D = 50\,\mu$A			$I_D = 65\,\mu$A		
L [μm]	W [μm]	C_G [fF]	g_m [μS]	τ [ns]	i^*_{RMS} [nA]	g_m [μS]	τ [ns]	i^*_{RMS} [nA]
1	4.78	29	317	0.33	118	361	0.29	134
2	**6.81**	**93**	**267**	**0.63**	**55.5**	305	0.55	63.2
3	8.82	189	248	1.06	36.1	283	0.93	41.2
4	10.79	319	238	1.66	26.7	271	1.45	30.4
5	**12.71**	**481**	231	2.41	21.1	**263**	**2.11**	**24.0**
6	14.33	677	224	3.36	17.2	255	2.95	19.6

Table 3.1: Key parameters for different memory cells using annular transistors with two biasing conditions $I_D = 50$ and $65\,\mu$A (see text).

taken from textbooks, e.g. [42]. The gate capacitance in the region of strong inversion at $V_{gate} = 1.5$ V is $C_{tot} = 157 \pm 1$ pF, leading to a mean capacitance per transistor of $C_G = 628 \pm 4$ fF. Note, that a mismatch of about 5-10 % for the capacitance distributed over a large chip has to be considered, being much higher than the given statistical error. With the dimensions of the transistor of $10.8 \times 9.5\,\mu m^2$ and a $2.8 \times 1.5\,\mu m^2$ spacing in the middle for the source contact, the gate area is $98.4\,\mu m^2$. Using a oxide capacitance of 6.23 fF per μm^2 from [43] yields a gate capacitance of 613 fF in good agreement with the measured value. For a rectangular transistor, the values of W and L would lead to a gate area of $64.1\,\mu m^2$ and a gate capacitance of about 400 fF. The deviation between this value and the correct one using the annular geometry is about 50 %. Since the BSIM transistor model assumes a rectangular shape, the SPICE simulations would show a wrong circuit behavior. Hence, for an accurate treatment of the memory cell using annular transistors, the gate capacitance has to be calculated by hand. For the simulations the missing capacitance has been considered by an additional gate capacitance.

Table 3.1 shows key parameters, like sampling noise and settling time for different memory cells using annular transistors. The gate capacitance C_G is calculated using equation (3.22) and replacing the product of W and L by the gate area of the annular transistor. Two biasing conditions have been considered, the first one using $I_D = 50\,\mu$A and the second one with $I_D = 65\,\mu$A. The settling time τ and sampling noise i^*_{RMS} have been calculated using equation (3.3) and (3.20), respectively. For the calculations $C_D \approx 75$ fF has been estimated and $\mu = 337\,cm^2/Vs$, $c_{ox} = 6.23\,fF/\mu m^2$ from [43] have been used. In the final design, see section 3.3.6 transistors with L=2 μm and L=5 μm are used for the two sampling stages. These transistors and their key parameters are marked bold in table 3.1.

3.3.6 Double stage memory cell

The influence of charge injection due to the sampling switch is inherent in any sampling system. Several techniques to minimize charge injection have been reported, e.g. in [44],[45],[46].

The contribution of charge injection to the error on the sampled output can be divided

into a constant offset and a signal dependent current: $\delta I = \delta I^{\text{const}} + \delta I^{\text{sig}}$. In the readout architecture discussed in section 3.2, the constant offset δI^{const} becomes non-relevant as it can be compensated using a tunable threshold in the current compare circuitry. The signal dependent charge injection δI^{sig}, on the contrary, will cause a nonlinearity in the transfer behavior of the memory cell. Hence, it should be reduced to a minimum.

To reduce the signal depending charge injection δI^{sig}, an n-step memory cell is proposed in [47]. For the current memory cell in CURO, a double stage cell is used, very similar to the one proposed in [47] with n=2. The schematic of the double stage cell is shown in Fig. 3.10. It consists of two successive memory cells, a coarse and a fine one, each

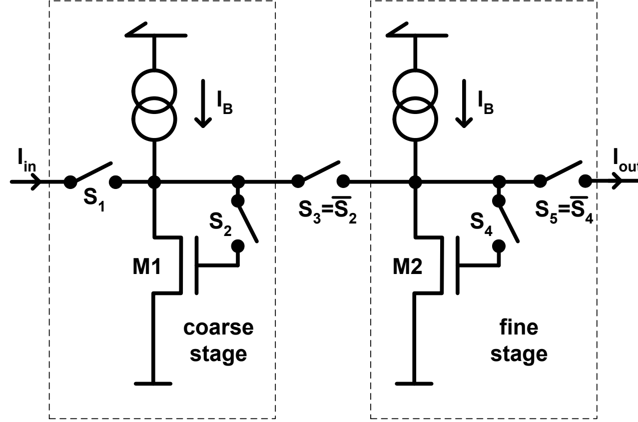

Figure 3.10: Basic schematic of the double stage current memory cell.

corresponding to the basic memory cell, described in section 3.3.1. The steering of the double stage cell is described in the following.

At any time, switches S2 and S3, as well as switches S4 and S5 are driven complementary, as indicated in Fig. 3.10. The initial state of the switches is: S1, S2 and S4 closed. After the first sampling step (S2 is opened), the resulting current through M1 is

$$I_{\text{M1}} = I_{\text{in}} + I_{\text{B}} - \delta I_{\text{c}} \tag{3.29}$$

where $\delta I_{\text{c}} = \delta I_{\text{c}}^{\text{const}} + \delta I_{\text{c}}^{\text{sig}}$ indicates the total error (including charge injection) made by the coarse stage. As the input current is still connected to the circuit, the resulting output current of the coarse stage is δI_{c}, which becomes the input current of the succeeding fine stage. After the second sampling step (S4 is opened), the current through M2 is

$$I_{\text{M2}} = \delta I_{\text{c}} + I_{\text{B}} - \delta I_{\text{f}} \tag{3.30}$$

where $\delta I_{\text{f}} = \delta I_{\text{f}}^{\text{const}} + \delta I_{\text{f}}^{\text{sig}}$ is the fine stage's error. Finally, the input switch S1 is opened resulting in an output current

$$I_{\text{out}} = -I_{\text{in}} + \delta I_{\text{f}} \tag{3.31}$$

The error of the coarse stage δI_{c} does no longer contribute to the sampled output. Even though the constant parts of the errors δI_{c} and δI_{f} are similar, their signal dependent

parts are different because the input range of the fine stage δI_c is much smaller than the input range of the coarse stage I_{in}. Since the signal dependent part of charge injection causes the nonlinearity of the cell, it can be reduced significantly by the double stage sampling.

Due to the inverting feature of the memory cell itself, a total cancellation of charge injection can be achieved if an even number of double stage cells are used successively, as is the case for the pedestal subtraction and buffer cell in the CURO architecture. The output current after two double stages is

$$I_{out} = -\left(-I_{in} + \delta I_{f1}\right) + \delta I_{f2} \tag{3.32}$$

Assuming that the charge injection of both fine stages are the same ($\delta I_{f1} = \delta I_{f2}$), a total cancellation of charge injection is achieved. This is possible since the charge injection of the fine stages is dominated by the constant fraction and not by the signal dependent part and should, therefore, be similar. However, a total cancellation is not crucial for the readout architecture, as mentioned before.

The use of the double stage design is further advantageous since the time interval for both sampling steps does not need to be the same. In particular, both parts should be designed differently. The coarse part should provide a high bandwidth to sample the input current very fast. Consequently, its sampling noise and other errors like charge injection will be comparatively high. However, due to the resampling feature of the fine part, the error of the coarse part including the sampling noise will not contribute to the output, as shown in equation (3.31). The fine part can be operated much more slowly and should be optimized with respect to the noise and the accuracy performance of the cell.

Final Design

For the coarse and fine part of the memory cell, transistors with L=2 μm and L=5 μm, see table 3.1 have been chosen, respectively. The layout of the cell is shown in Fig. 3.11. The metal layers M2-M5 are not shown to keep the layout concise. Layers M2 and M3 are used for the distribution of GND and VDDA, respectively. Layer M4 is used for the input/output connection of the memory cell and M5 distributes the steering strobes.

To ensure aperiodic settling of each memory cell, the sampling switches are implemented using linear transistors. Due to their layout constraints, annular transistors are not able to provide the required switch conductance. It has to be verified whether the design with linear switches is radiation hard enough for a dose of 200 kRad, as expected for 5 years operation at the ILC. If linear transistors can be used for switching, dummy switch techniques [48] should be considered in the next design to reduce the effect of charge injection further on. For the sampling switch of the coarse part, W = 0.55 μm and L = 0.25 μm (g_s = 360 μS) has been chosen. The fine switch is W = 0.3 μm and L = 0.25 μm (g_s = 190 μS). The coarse stage is biased with I_D = 50 μA, whereas 65 μA is used for the fine part. Hence, an equal g_m for both parts is achieved.

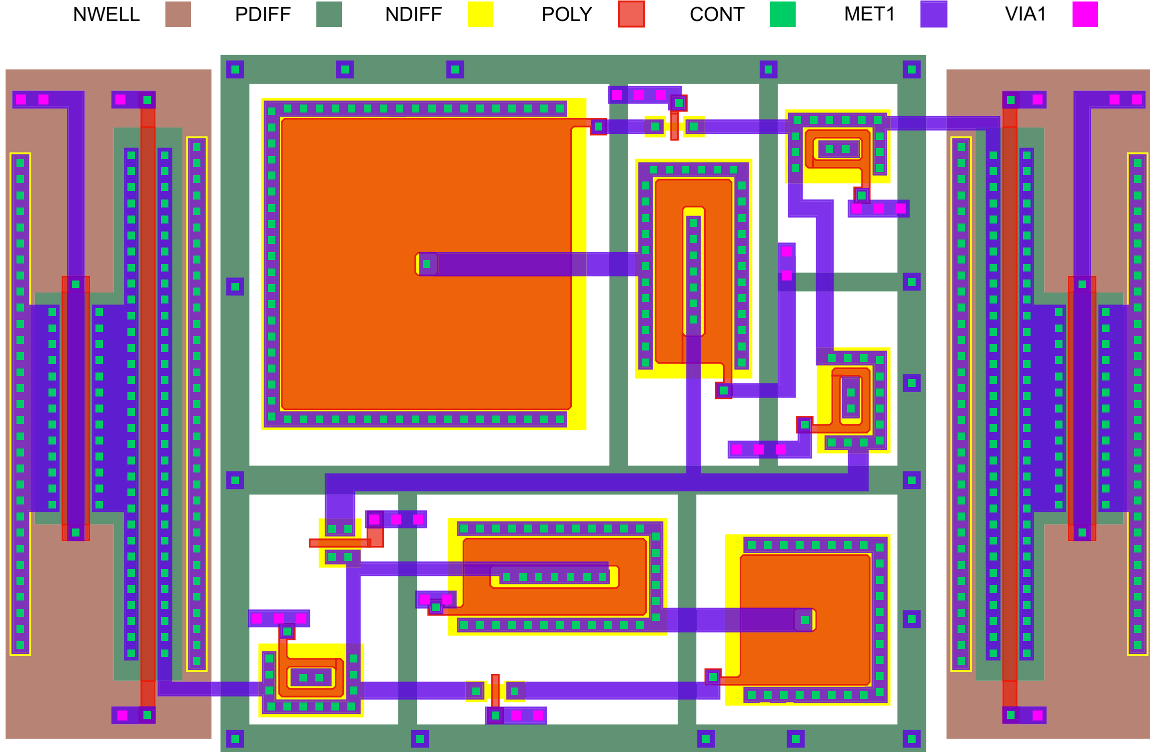

Figure 3.11: Layout of the current memory cell ($25 \times 40\,\mu m^2$).

To estimate the total noise contribution, the sampling noise of the cell as well as the thermal noise of the bias current sources are considered. Assuming a bandwidth of 50 MHz, the noise contribution for both current sources ($g_m = 75\,\mu S$) is $i_{B,RMS} = 16\,nA$ after CDS, inherently performed by the cell. Adding the sampling noise of the fine part of i_{RMS}=19.6 nA in quadrature[3], a total noise of i_{RMS}=25.3 nA for the memory cell is expected.

3.3.7 Summary of the memory cell design

In this section the design of a current memory cell for the CURO architecture has been described. Sampling in the current domain offers a large dynamic range and a trivial and accurate current subtraction can be performed. The design trade-offs concerning settling time and noise performance and the non-ideal effects, such as charge injection and limited output conductance of the memory cell have been discussed.

Concerning the settling behavior of the circuit, the memory cell is a second order system where the sampling switch conductance is the determining design parameter. The dominant noise contribution of the memory cell is given by kT/C-noise, due to the sampling process which is also the main noise source in voltage sample and hold systems. Since

[3]The noise has been calculated using equation (3.19) for a gate capacitance being much larger than the drain capacitance.

the sampling noise is independent of the switch conductance, the switch can be designed to optimize the settling behavior without affecting the noise performance of the cell. The parasitic drain capacitance of the memory cell is a drawback in the design and should be minimized as it decreases the noise versus speed performance of the system significantly.

To reduce the effect of charge injection and to improve the linearity of the memory cell, a double stage cell has been used. The bandwidth of the double stage is designed to operate at 50 MHz with a total noise contribution of the cell of about 25 nA. For the complete readout chain, consisting of three sampling stages, a total noise of about 45 nA is expected.

3.4 Input stage realized by a regulated cascode

Cascode techniques are commonly used to increase the output resistance of transistor circuits, as for example in section 3.3.2. In case of an unregulated cascode, shown in Fig. 3.12 (left), the gate of the cascode transistor M1 is kept at a constant potential. Figure 3.12 (right) shows the basic principle of a regulated cascode, where the gate

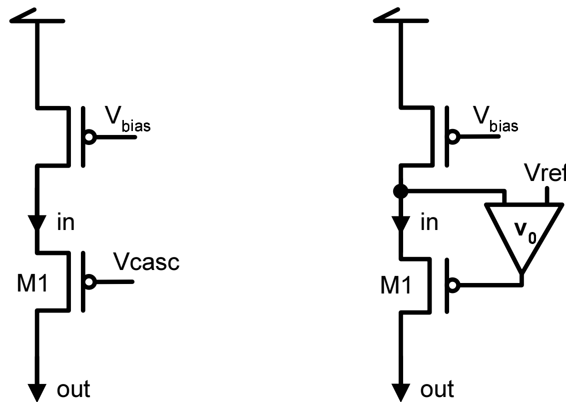

Figure 3.12: Unregulated cascode stage with a constant voltage V_{casc} at the gate of cascode transistor (left). Regulated cascode using a feedback stage for the gate voltage (right).

voltage of the cascode transistor is regulated by a feedback stage with respect to voltage swings at the input node. Compared to an unregulated cascode, the output resistance of the regulated cascode is further improved by the open loop gain v_0 of the feedback stage.

Basically, the improvement of the output resistance of cascode circuits is achieved by keeping the potential at the input node of the cascode transistor as constant as possible. Hence, a regulated cascode configuration will be used for the input stage of CURO to provide a low input impedance for the sensor current.

Dynamic behavior of the regulated cascode

Since a stable performance of the input stage is a crucial issue in the design, the dynamic behavior of the regulated cascode will be analyzed in this section. Figure 3.13 (left) shows the circuit of the regulated input cascode used in CURO. The feedback is realized by a

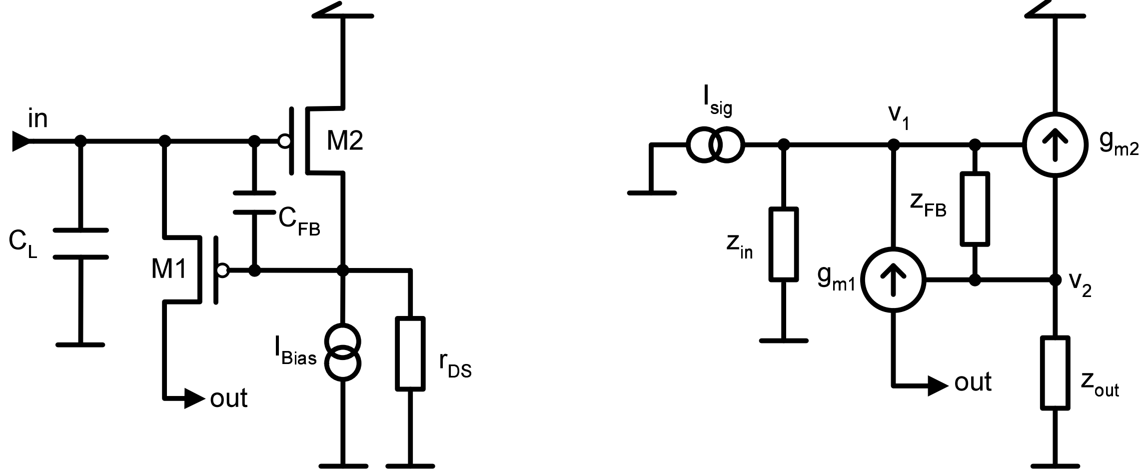

Figure 3.13: Circuit of the regulated input cascode with a simple amplifier feedback stage (left). Small signal equivalent circuit of the regulated input cascode (right).

simple amplifier stage implemented by M2 and biased by I_{Bias}. The open loop gain of the amplifier stage is given by $v_0 = g_{m2} \cdot r_{DS}$, where g_{m2} is the transconductance of M2 and r_{DS} is the output resistance of the amplifier stage. C_L is the load capacitance at the input node of the cascode and C_{FB} is the parasitic feedback capacitance. Using the small signal equivalent circuit of the regulated cascode in Fig. 3.13 (right) and summing all currents at the input node v_1 of the amplifier stage yields

$$\begin{aligned} I_{sig} &= -g_{m1}(v_2 - v_1) + \frac{v_1}{z_{in}} + (v_1 - v_2)\frac{1}{z_{FB}} \\ &= v_1\left(\frac{1}{z_{FB}} + g_{m1} + \frac{1}{z_{in}}\right) - v_2\left(\frac{1}{z_{FB}} + g_{m1}\right) \end{aligned} \tag{3.33}$$

Summing all currents at the output node v_2 yields

$$v_1 g_{m2} + (v_2 - v_1)\frac{1}{z_{FB}} = -v_2\frac{1}{z_{out}}$$

$$v_2 = v_1\frac{(1 - g_{m2}z_{FB})}{z_{out} + z_{FB}} \cdot z_{out} \tag{3.34}$$

where z_{in} is the load impedance of the cascode and z_{FB}, z_{out} are the feedback and output impedance of the amplifier, respectively. Substituting equation (3.34) in equation (3.33) and using $z_{FB} = \frac{1}{sC_{FB}}$, $z_{in} = \frac{1}{sC_L}$ and $z_{out} = r_{DS}$, results in:

$$v_1 = \frac{I_{sig}}{g_{m1}(1 + g_{m2}r_{DS})} \cdot H(s) \tag{3.35}$$

with

$$H(s) = \frac{1 + s r_{\mathrm{DS}} C_{\mathrm{FB}}}{1 + s\frac{C_{\mathrm{FB}} + C_{\mathrm{L}} + r_{\mathrm{DS}} g_{\mathrm{m2}} C_{\mathrm{FB}}}{g_{\mathrm{m1}}(1 + g_{\mathrm{m2}} r_{\mathrm{DS}})} + s^2 \frac{r_{\mathrm{DS}} C_{\mathrm{FB}} C_{\mathrm{L}}}{g_{\mathrm{m1}}(1 + g_{\mathrm{m2}} r_{\mathrm{DS}})}} \tag{3.36}$$

The transfer function is of second-order and is characterized by one zero $z_1 = r_{\mathrm{DS}} C_{\mathrm{FB}}$ and two poles. Assuming that the open loop gain of the amplifier is much larger than 1 and that the load capacitance is much larger than the parasitic feedback capacitance

$$v_0 = g_{\mathrm{m2}} r_{\mathrm{DS}} \gg 1 \quad , \quad C_{\mathrm{L}} \gg C_{\mathrm{FB}}$$

the poles in the transfer function

$$H(s) = \frac{1 + s z_1}{1 + s(p_1 + p_2) + s^2 (p_1 \cdot p_2)} \tag{3.37}$$

simplify to $(p_1 + p_2) = \frac{C_{\mathrm{L}} + r_{\mathrm{DS}} g_{\mathrm{m2}} C_{\mathrm{FB}}}{g_{\mathrm{m1}} g_{\mathrm{m2}} r_{\mathrm{DS}}}$ and $p_1 \cdot p_2 = \frac{r_{\mathrm{DS}} C_{\mathrm{FB}} C_{\mathrm{L}}}{g_{\mathrm{m1}} g_{\mathrm{m2}} r_{\mathrm{DS}}}$.
Calculating the poles yields

$$p_{1/2} = \frac{2 r_{\mathrm{DS}} C_{\mathrm{FB}} C_{\mathrm{L}}}{C_{\mathrm{L}} + v_0 C_{\mathrm{FB}} \pm \sqrt{(C_{\mathrm{L}} - v_0 C_{\mathrm{FB}})^2 + 4 C_{\mathrm{L}} v_0 C_{\mathrm{FB}} (1 - r_{\mathrm{DS}} g_{\mathrm{m1}})}} \tag{3.38}$$

For ordinary cascode applications the load capacitance and the feedback capacitance enlarged by the Miller effect, $v_0 C_{\mathrm{FB}}$, are distinct. With C_{L} being the load capacitance of a DEPFET matrix, C_{L} becomes large and of the same order of magnitude as $v_0 C_{\mathrm{FB}}$, so that the first term in the root of equation (3.38) is small. The output resistance of the amplifier r_{DS} is preferably high, much larger than $\frac{1}{g_{\mathrm{m1}}}$, so that the second term in the root is negative. Thus, the poles easily become complex conjugated pairs and the response of the circuit in the time domain can show a violent overshoot that degrades the performance of the circuit. Furthermore, it should be possible to operate the chip with various matrix sizes having different load capacitances.

To ensure a controlled response behavior of the circuit independently of the load capacitance, pole-zero cancellation is used. This is done in the following way. For the special case, where

$$\frac{1}{g_{\mathrm{m1}}} \stackrel{!}{=} r_{\mathrm{DS}}$$

the poles become $p_1 = r_{\mathrm{DS}} \cdot C_{\mathrm{FB}}$ and $p_2 = \frac{C_{\mathrm{L}}}{g_{\mathrm{m2}}}$, where p_1 and the zero z_1 are now equal and cancel each other (pole-zero cancellation). Details concerning the technique of pole-zero cancellation can be found in textbooks, e.g. in [49]. After the cancellation, the remaining pole in the circuit is given by

$$p = \frac{C_{\mathrm{L}}}{g_{\mathrm{m2}}} \tag{3.39}$$

The settling behavior of the cascode is now critically damped providing a phase margin of $\varphi = 90°$ for any values of C_{L}, v_0 and C_{FB}. It is advantageous that the cancellation does

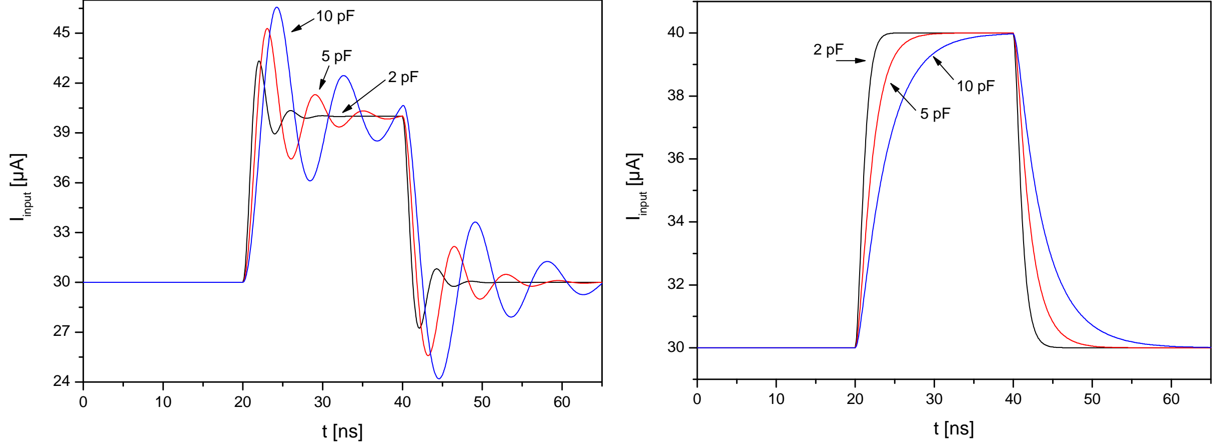

Figure 3.14: Simulated response behavior of the regulated cascode for an input swing of $10\,\mu$A without (left) and with (right) pole-zero cancellation for load capacitances C_{L}=2,5 and 10 pF.

not depend on C_{FB} since its value is hardly accurately determinable. A simulation of the behavior of the circuit using the BSIM3.3 transistor model [50] is shown in Fig. 3.14 for load capacitances of 2 pF, 5 pF and 10 pF. The other parameters used in the simulation were: $g_{\mathrm{m1}} = 270\,\mu$S, $g_{\mathrm{m2}} = 2350\,\mu$S, the feedback capacitance is in the range of 100 fF. The simulation shows that an aperiodic settling of the circuit is reached independently of the load capacitance for the cancellation case, as intended. For the uncanceled case, the settling of the circuit does strongly depend on the used load.

On the other hand, the input resistance of the cascode has been significantly degraded to $r_{\mathrm{in}}^{-1} = g_{\mathrm{m1}}\, v_0 = g_{\mathrm{m1}}\, g_{\mathrm{m2}}\, r_{\mathrm{DS}} = g_{\mathrm{m2}}$ by the pole-zero cancellation. A comparable input resistance could also have been achieved by an unregulated cascode stage biased by a large current to raise the transconductance of the transistor to a high value equivalent to g_{m2}. Although the cascode transistor itself does not contribute to the noise performance, the additional current sources for sinking and draining the bias current do. Assuming a transconductance of $350\,\mu$S for both current sources and a bandwidth of the sampling stage of about 50 MHz, the thermal noise contribution of the input stage is $\mathrm{i}_{\mathrm{RMS}} \approx 40\,$nA after CDS, which is already in the range of the total noise performance of the analog part of 45 nA. In case of the damped circuit by the pole-zero cancellation the input stage is formed by M1 with a negligible noise contribution, whereas a fast settling time can be obtained by choosing a high g_{m2}. According to equation (3.39) the bandwidth of the circuit is then given by

$$\nu = \frac{g_{\mathrm{m2}}}{2\pi C_{\mathrm{L}}} \tag{3.40}$$

In practice, the cancellation is done by self biasing the amplifier M2 with a dioded pMOS identical to M1. This provides a load with an output resistance of $r_{\mathrm{DS}} = 1/g_{\mathrm{m1}}$. For the feedback transistor M2, the width and length were chosen to be W=94 μm and L=0.3 μm respectively, resulting in $g_{\mathrm{m2}} = 2350\,\mu$S in the self biased case. The dimensions of transistor M1 were chosen to W=15μm and L=0.5 μm. According to equation (3.40),

a row rate of 20 MHz (sampling with 40 MHz) is therefore possible up to $C_\mathrm{L} \approx 9.5\,\mathrm{pF}$, which is fast enough for the readout of a small 64×128 DEPFET pixel matrix with an expected capacitive load of 4-5 pF (plus interconnections) [31].

Besides the dioded transistor for self biasing, an additional current source is added in parallel to reduce r_DS further. By choosing $r_\mathrm{DS} < 1/g_\mathrm{m1}$, the settling of the circuit is then no longer critically damped since the pole quality factor

$$Q = \frac{\sqrt{p \cdot q}}{p+q} = \frac{\sqrt{r_\mathrm{DS} g_\mathrm{m1} C_\mathrm{L} v_0 C_\mathrm{FB}}}{C_\mathrm{L} + v_0 C_\mathrm{FB}} < 0.5 \tag{3.41}$$

and the system will show an underdamped response. The amount of peaking A_P in the time response (overshoot) is then given by [49]

$$A_\mathrm{P} = \frac{Q}{\sqrt{1 - \frac{1}{4Q^2}}} \tag{3.42}$$

Thus, for larger capacitive loads the additional current source can be used to tune the response behavior of the circuit for the specific load.

3.5 Current comparator for hit discrimination

The comparator stage identifies currents from the analog part that are above a certain threshold. Performing a current compare for all columns in parallel, a binary hit pattern is generated every clock cycle. The pattern is handed to the digital part and is used for zero suppression. A schematic overview of the comparator unit used in CURO II is shown in Fig. 3.15. The comparator itself is implemented as a simple inverter stage

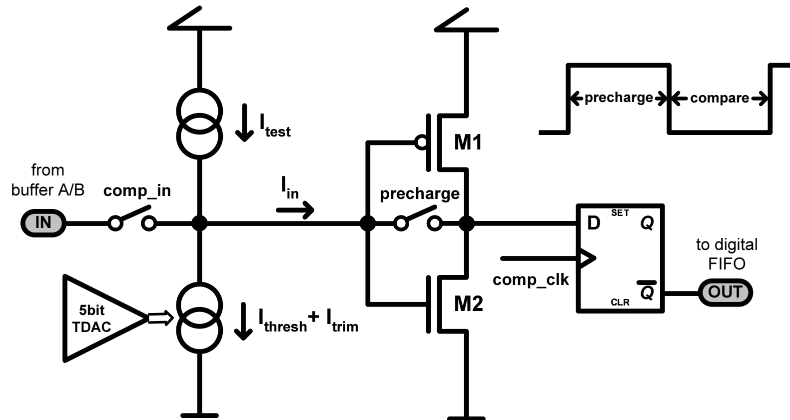

Figure 3.15: Overview of the comparator unit (for each of the 128 channels).

realized by the transistor pair M1 and M2 [51]. If the resulting input current $\mathrm{I_{in}}$ is positive (that means that the probed current is above the threshold) the combined gate

capacitance of the inverter will be charged up to the upper voltage rail of the circuit and the output of the inverter will be low. If the current is negative, with the probed current below the threshold, the input node is discharged to ground and the output becomes high. To speed up the comparison, positive feedback is applied to the inverter in the first half of the clock cycle by closing the "*precharge*" switch. During the second half of the clock cycle, the switch is opened and the result of the current compare is buffered in a flip-flop. Since the comparator is precharged to the trip-point the current compare is performed very fast even for input currents close to the threshold. The threshold current can be selected by an 8 bit DAC for the whole chip. To compensate dispersions in the chip, the threshold can be trimmed by a 5 bit DAC implemented in each channel. For testing purpose the comparator stage can be separated from the analog part by the "*comp_in*" switch and a current source I_{test} can be used as an input current. For the precharge switch a minimal size transistor is chosen to reduce the effect of charge injection when opening the switch. During the precharge phase of the circuit, the inverter stage consumes maximum power. Therefore, transistors M1 and M2 are optimized to reduce the power consumption while still obtaining a settling time less than 10 ns from both supply rails to the trip-point. Further on, both transistors are balanced to set the trip-point to the middle of the supply rails.

3.6 Hitscanner and digital part

Instead of storing the complete binary pattern generated by the current compare, a zero suppression is done by the hitscanner and only the addresses of the hits in the pattern are stored. They are deposited in the Hit-RAM for later read out. Due to the zero suppression this on-chip RAM can be kept small. Taking into account that a single 128 channel chip reads out 128×1000 pixels in the innermost layer, the expected hit density of 0.05 hits per BX and mm^2 due to the dominating pair background leads to less than 34000 events integrated over a complete bunch train. Thereby, an average cluster of 3 pixels per track has already been taken into account. With 22 bit (7 bit column, 10 bit row stamp and 5 bit frame counter)[4] per event, the expected total data volume is less than 100 kB that has to be stored in the RAM.

The zero suppression performed by the hitscanner has to be fast enough to meet the row rate of the analog part. Hence, the pattern has to be scanned within 50 ns (20 MHz). Finding hits in a binary pattern seems to be a trivial task, but a linear scan, for example, through a 128 cell pattern in 50 ns imposes a scan clock of $50 \times 128 = 2.56$ GHz. This is hard to achieve even with nowadays most advanced process technologies. The required clock rate can be relaxed by scanning the pattern from both ends or by subdividing the pattern into even smaller parts. Performing more and more scans in parallel leads to a binary tree architecture proposed in [52] for the readout of micro strip detectors.

The operational principle of the hitscanner is shown in Fig. 3.16 (left) for a 4 bit wide

[4]Appropriate compression may reduce the data volume further.

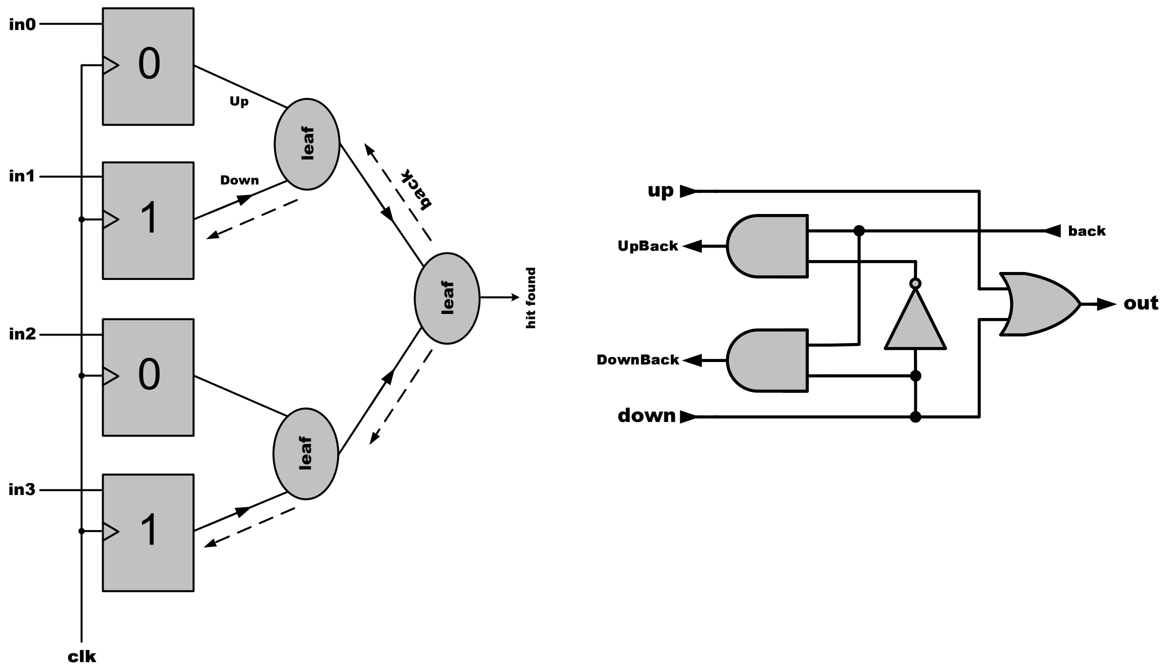

Figure 3.16: Operational principle of the hitscanner architecture. The illustration is restricted to 4 inputs (left). Schematic of one scanner leaf. Only one back propagating part is shown (right).

input pattern example. First, the pattern is loaded into the input register. The hits propagate immediately through the tree since the leaves of the tree are just a logical OR in the down direction. If one or more hits are found, the top and bottom hits are traced back via the back propagating feature of the leaves. The logic implemented in each leaf (for the bottom traced hit) is shown in Fig. 3.16 (right). The truth table of the schematic is given in table 3.2. If only one input of the OR gate (Up/Down) and the back propagating input (back) are active, the corresponding back propagation output is active. If both inputs of the OR gate are active, only the lower back propagation output is set active. The upper output is set to zero, so that the second hit is not propagating

Up	Down	back	out	UpBack	DownBack	comment
0	0	1	0	0	1	impossible
0	1	1	1	0	1	down hit
1	0	1	1	1	0	up hit
1	1	1	1	1	0	both hits
0	0	0	0	0	0	no back propagation
0	1	0	1	0	0	no back propagation
1	0	0	1	0	0	no back propagation
1	1	0	1	0	0	no back propagation

Table 3.2: Truth table of the scanner leaf shown in Fig. 3.16 (right).

back (priority logic). To find up to 2 hits simultaneously, each leaf includes an equivalent logic for the top traced hit using the UP input instead of the DOWN input. After the hits are traced back completely, their addresses are binary coded in the levels of the back propagating tree and are stored in the Hit-RAM. The corresponding hits are reset in the input register in the next clock cycle and the scan starts again with the reduced pattern. If the pattern is emptied completely the next patten is loaded.

Compared to the linear scan, the time needed for the hit detection is given by the propagation and back propagation delay through all levels of the tree. In case of a 128 bit pattern, ${}_2\log(128) = 7$ levels have to be passed. With a rough estimation of the delay of one level of 350 ps (down and back) the hitscanner itself is very fast. The layout of one scanner leaf of the tree including one bit of the input register is shown in Fig. 3.17. To keep the layout visible, the metal layers M2, M3 (mainly used for the

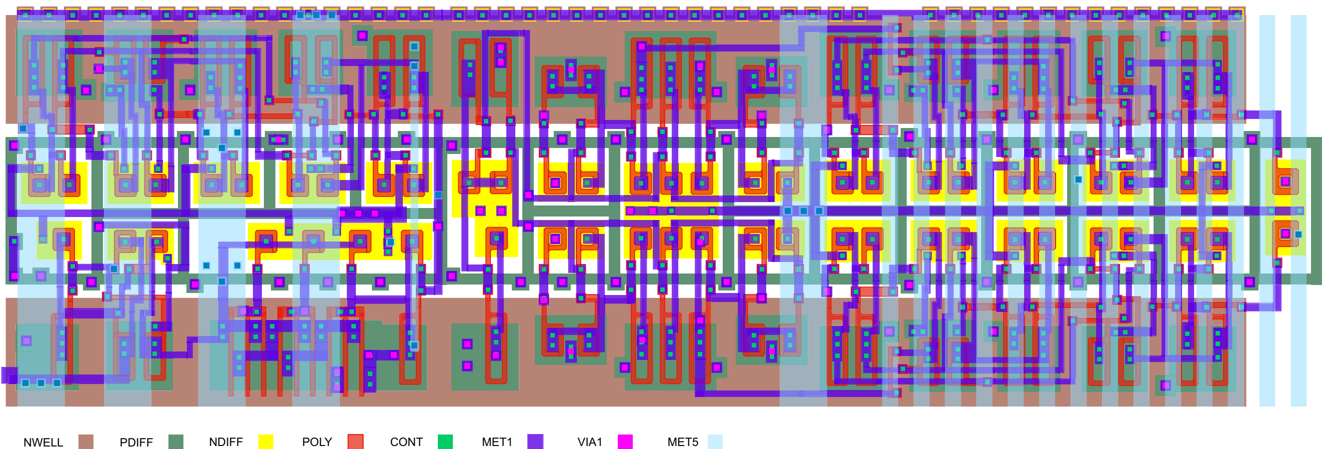

Figure 3.17: Layout of one leaf of the scanner tree and one bit of the input register using radiation tolerant design rules ($25 \times 80\,\mu\text{m}^2$).

distribution of GND and VDD, respectively) and M4 (used for interconnections) have been removed. Using radiation tolerant design rules [53] one leaf is $25 \times 80\,\mu\text{m}^2$ large. The challenge concerning the overall layout is to line up the leaves of the tree structure in a row. Finally, the whole scanner consumes an area of only $3200 \times 85\,\mu\text{m}^2$.

With the capability of the hitscanner to find 2 hits per cycle in a 128 bit pattern, the mean occupancy of below 1 % at the innermost layer of the vertex detector, see section 1.4.2, can easily be handled. Since the mean hit rate in the vertex detector will fluctuate, a FIFO is inserted in front of the scanner for derandomization. For this purpose a non-conventional FIFO structure has been implemented where two different clocks are used for the read and write access. In addition, both clocks do not need to be synchronous. A write pointer and a scan pointer, incremented by the write and scan clock respectively, administrate the FIFO. During operation the FIFO runs full and hits are lost if the write pointer is going to overtake the scan pointer. In this case, new patterns from the current compare are thrown away and a FIFO-Full flag is set in the chip for later control.

To estimate the required FIFO size coping with different occupancies a simulation has

been done. The number of hits inserted in a new FIFO row is generated according to a Poisson distribution with a certain mean hit rate. It is assumed that the hitscanner can be operated twice as fast as the analog front end, e.g. a 20 MHz write clock and a 40 MHz scan clock. This is taken into account by adding new hits to the FIFO every second simulation cycle only. Based on the capability of the scanner, up to 2 hits per cycle are removed from the scanned FIFO row. Figure 3.18 shows the relative occurrence of the FIFO fill-level for 10^6 generated events [54]. A mean rate of 4 hits every second cycle

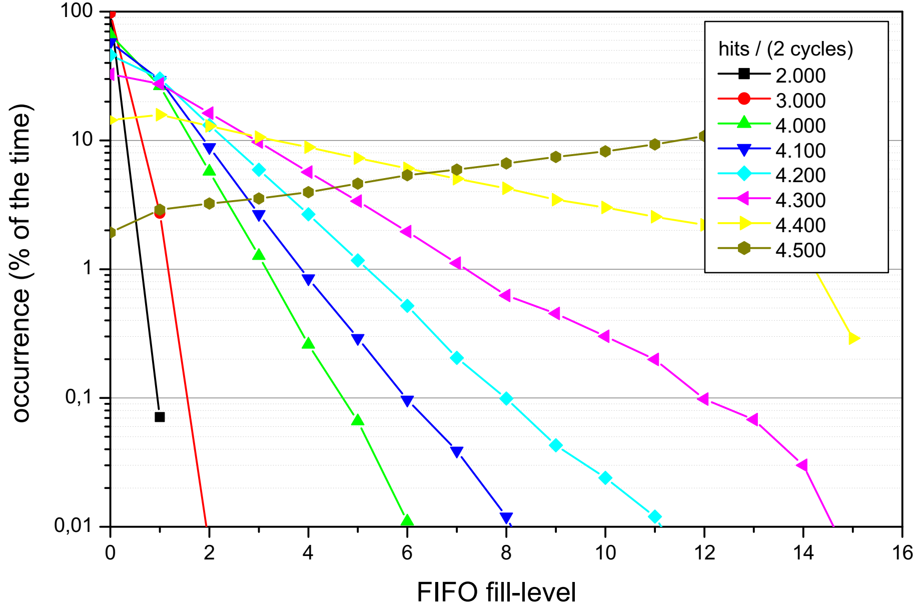

Figure 3.18: Simulation of the required FIFO depth for different occupancies [54].

seems to be an intrinsic limit where the FIFO fill-level rises vastly. This is comprehensible as even the largest FIFO runs full, if the mean number of hits put into the FIFO is larger than the number of hits taken out by the scanner, being equivalent to 2 hits/cycle. The simulation shows that for the expected occupancy at the ILC of about 1 hit/cycle, the probability of losing hits in a 4 row FIFO is already very rare (In the simulation with 10^6 events the FIFO was never 4 rows full for an occupancy of 1 hit/cycle). Although implementing a 4 row FIFO would be sufficient for the ILC operation, a FIFO depth of 8 rows is chosen to tolerate even higher occupancies.

3.7 Summary of the CURO design

A novel architecture for a DEPFET readout, the CURO (**CU**rrent **R**ead**O**ut) architecture has been devised and realized. It is based on current mode operation and therefore, perfectly adapted to the output mode of the DEPFET detector, which is a current. Moreover, the usage of current mode techniques is advantageous in the design since a large dynamic range is possible and the implementation of algebraic operations, such as

current subtractions are easily done. The major components of the readout architecture have been discussed.

A regulated cascode circuit is used to provide a low impedance input stage for the current based readout. Due to a pole-zero cancellation a proper settling of the stage, independent of the detector capacitance is ensured. With the current design of the cascode, a readout of a capacitive load up to about 10 pF, adequate for a 64×128 DEPFET pixel matrix, with the required row rate of 20 MHz is possible.

For the analog FIFO as well as for the pedestal subtraction, a current memory cell for temporary storage of a current is needed. The design parameters concerning operational speed and noise performance of such a current memory cell have been analyzed. According to the present design, the noise of a single memory cell is expected to be about 25 nA, of which 20 nA are related to sampling noise. With three memory stages for the complete readout chain, a total noise contribution of about 45 nA is expected. For the present DEPFET devices with an internal amplification of $g_q \approx 283\,pA/e^-$, this translates into ENC $\approx 160\,e^-$. Using advanced DEPFET devices with an improved internal amplification of up to $g_q = 1\,nA/e^-$, a noise contribution of the readout of ENC=45 e^- is possible. These numbers are in good agreement with the ILC requirement, demanding a noise below 100 e^-. The bandwidth of the cell is designed to enable operation up to 50 MHz. Since two samples per readout cycle are needed, this performance corresponds to a row rate of 25 MHz. The memory cell consumes an area of $25 \times 40\,\mu m^2$.

Due to the triggerless operation of the ILC vertex detector, hit detection and zero suppression are implemented in the readout architecture. Furthermore, an automatic pedestal subtraction suppresses inhomogeneities in the sensor matrix. Due to the fast correlated double sampling performed in the analog part, the 1/f noise performance of the system is improved.

Zero suppression is done by a fast hitscanner, that is arranged in a parallel tree structure. The scanner finds up to two hits per clock cycle in the binary pattern, which is enough to cope with the expected occupancy of about 1.7 hits in a 128 pixel matrix row. This ratio can even be improved since the hitscanner is expected to operate at much higher frequencies than 20 MHz and the analog front end and the digital part (i.e. FIFO and scanner) can be operated at different clock rates. To derandomize the Poisson distributed hit rate fluctuation of the detector to a constant rate that can be processed by the hitscanner, a digital FIFO is added in front of the hitscanner. A simulation demonstrated that a FIFO depth of 4 is already enough for an efficient derandomization.

While zero-suppression is performed, the detector signals are buffered in an analog FIFO, arranged equivalently to the digital one. Hit coordinates of an entire bunch train are stored in an on-chip RAM and are read out in the long bunch gaps. The hit information is digitized by external ADCs and is associated to the coordinates after the RAM is read out. By integrating an adequate ADC on the chip a standalone operation of the readout chip during a bunch train would be possible. Since the digitization is done after zero suppression the required rate of the ADC is moderate.

4 Performance of the CURO II chip

In this chapter the single performance of the 128 channel readout chip CURO II will be presented. Results concerning the analog part comprise the linearity, pedestal subtraction and noise contribution. Furthermore, the channel dispersion of the chip before and after an internal calibration will be presented. Results on the digital performance and on the power consumption of the chip will be reported as well.

Since the CURO architecture is current based, the measurements presented in this chapter are related to current signals. The current values can be converted to a signal charge by the internal amplification g_q of the DEPFET detector. Present sensors with a conservative layout achieve an amplification of about $283\,\mathrm{pA/e^-}$. It can be assumed that sensors with a more aggressive design will achieve a gain of up to $1\,\mathrm{nA/e^-}$.

4.1 Overview of the readout chip CURO II

Before the full-size readout chip CURO II has been fabricated, the basic functionality of several building blocks of the architecture (i.e. current memory cell, current compare and the complex hitscanner) have been tested by a prototype chip CURO I (shown in Fig. 4.1 right). Since the results of the CURO I chip are almost redundant, this chapter will focus on the full CURO II chip. Details concerning CURO I can be found in [55]. Both chips are fabricated in a TSMC $0.25\,\mu$m, 5 metal process. The rules for radiation tolerant design have been followed. In particular, enclosed transistor structures have been used whenever possible. With a design and fabrication process similar to the pixel and strip readout chips used at the LHC, which have been proven to sustain radiation doses higher than 50 MRad [56], CURO is expected to cope with the radiation doses expected at the ILC ($\approx 200\,$kRad).

The $4.5 \times 4.5\,\mathrm{mm}^2$ CURO II chip is shown in Fig. 4.1 (left). Compared to the general CURO architecture introduced in section 3.2, CURO II implements only one analog FIFO row, so that the readout has to be interrupted for the analog readout if more than two hits are found in a row. For a continuous analog readout which can cope with higher occupancies the analog FIFO size can be scaled easily to a suitable size in a future chip version. Furthermore, a continuous binary operation with high occupancies is possible, as the full digital FIFO size is implemented.

For the operation of the complex analog part several steering signals are needed (up to 5 for each of the 4 memory cells and the current comparator). All these strobes are derived from one single clock on the chip, the w_clk. As described in section 3.3.6, the

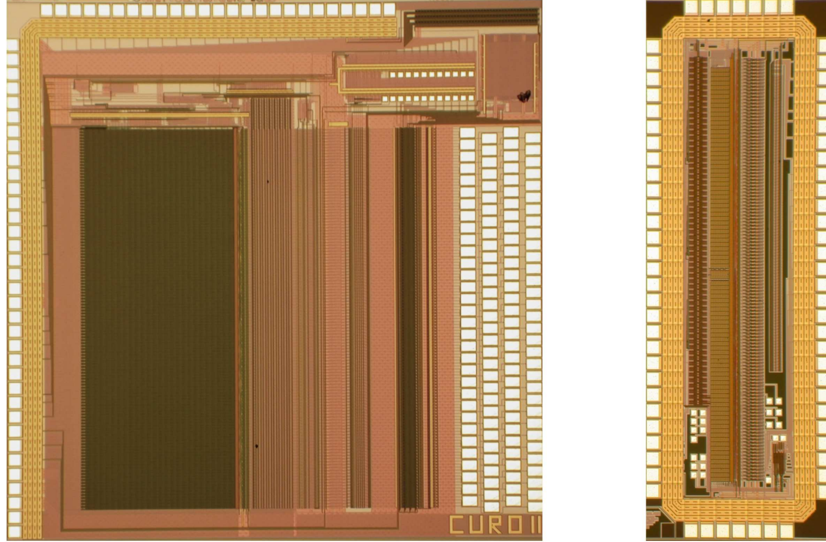

Figure 4.1: Micro photograph of the $4.5 \times 4.5\,\mathrm{mm}^2$ CURO II chip (left) and the $1.5 \times 4\,\mathrm{mm}^2$ prototype chip CURO I (right) fabricated in a $0.25\,\mu$m process.

memory cells used for the current storage consist of a coarse and a fine part to achieve a better performance. The fraction of the total sampling interval (given by the w_clk) that is used for the coarse and fine sampling strobe is adjusted by a multiplexer (MUX) set by 4 bit. An extra sampling time of 6.5 ns can be added for the coarse part, if needed. One of the steering signals, the coarse sample of the "pedestal subtraction cell", can be monitored at an output pad of the chip. Figure 4.2 (left) shows the observed sampling strobe with and without the activated extra sampling time. The measured sampling strobe as a function of the MUX-setting is shown in Figure 4.2 (right). A sampling time per MUX unit of 1.02 ± 0.02 ns is obtained by a linear fit to the data. The LSB of the strobe unit is realized by a queue of 20 inverters. The observed number corresponds to a mean propagation time of a single inverter of $\Delta\mathrm{T} = 51 \pm 1$ ps which is in good agreement with the quoted delay number for the fabrication process [43]. This allows a maximum sampling time of 24 ns for the coarse stage. The rest of the sampling interval will be used for the fine part.

Since the timing between some of the steering signals may become crucial, a deskewing unit has been added for each signal. The LSB of the deskewing unit, realized by 2 inverter stages, has been measured to 103 ± 4.5 ps. The unit is set by 5 bit, leading to a total adjustment range of 3.3 ± 0.14 ns.

For all fast signals from and to the chip that are active during the operation, LVDS ports are used to reduce digital cross talk. The slow signals are provided by standard CMOS ports to save power.

On the chip, 12 global 8 bit DACs are implemented for a flexible biasing of the several parts. The design of the 8 bit DAC has been adopted from the development of the ATLAS Pixel Chip [38]. The measurements presented in this chapter are performed using the DAC biasing parameters listed in the appendix in table C.2, if not quoted

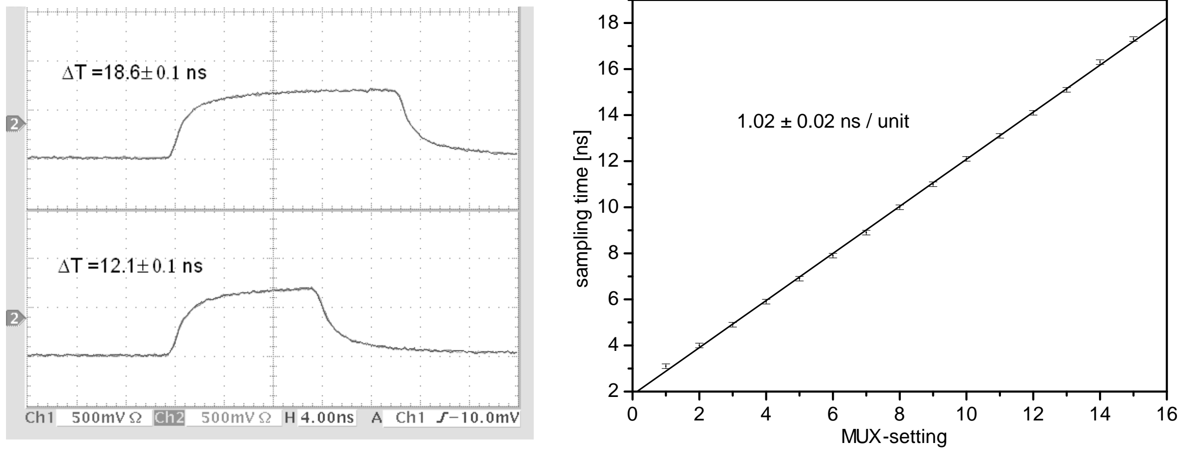

Figure 4.2: Screenshots from an oscilloscope, showing the sampling strobe for the coarse part of the “pedestal subtraction cell” for two different sampling times (left). Sampling time of the coarse part of the memory cell as a function of the MUX-setting (right).

otherwise. All deskewing units are set to a neutral position.

4.2 Linearity of the analog part and performance of the pedestal subtraction

To offer standalone testability of the analog part, a global test current source is implemented on the chip. As shown in Fig. 4.3, the current source can be multiplexed to the input pad of each individual channel and imitates a DEPFET pixel with a certain signal current superimposed on a pedestal current. Both currents can be varied by an

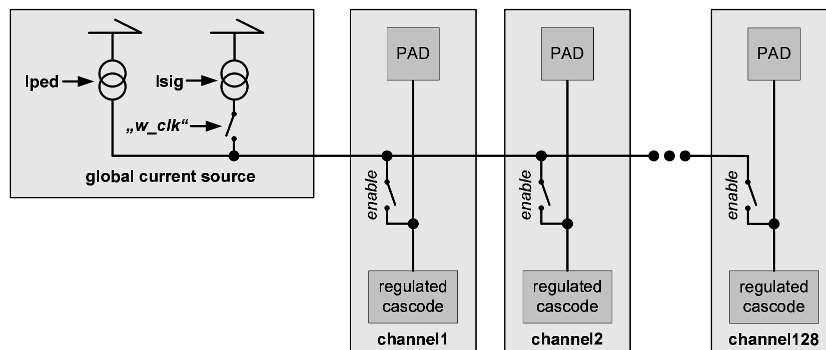

Figure 4.3: Analog on-chip testability showing the global current source that can be multiplexed to each individual channel.

8 bit DAC. The capacitive load at the input node using the test current source has been estimated to approximately 10 pF and is dominated by the routing transistors of the

bus. All measurements concerning the analog part are performed with a row rate of 24 MHz since this maximum analog frequency is given by the present readout system. This frequency corresponds to 48 MSPS[1] since two samples are done (pedestal and signal) in one clock cycle. The sampling time of the coarse stages was set to approximately 7 ns, leading to a remaining sampling fraction of approximately 13.8 ns for the fine part.

The linearity of the complete analog part, e.g. the input cascode and 3 successive sampling stages (pedestal subtraction, buffer and FIFO cell), is shown in Fig. 4.4 for channel 12. A linear fit yields a transfer characteristic of 1.00 ± 0.01. The integral-non-

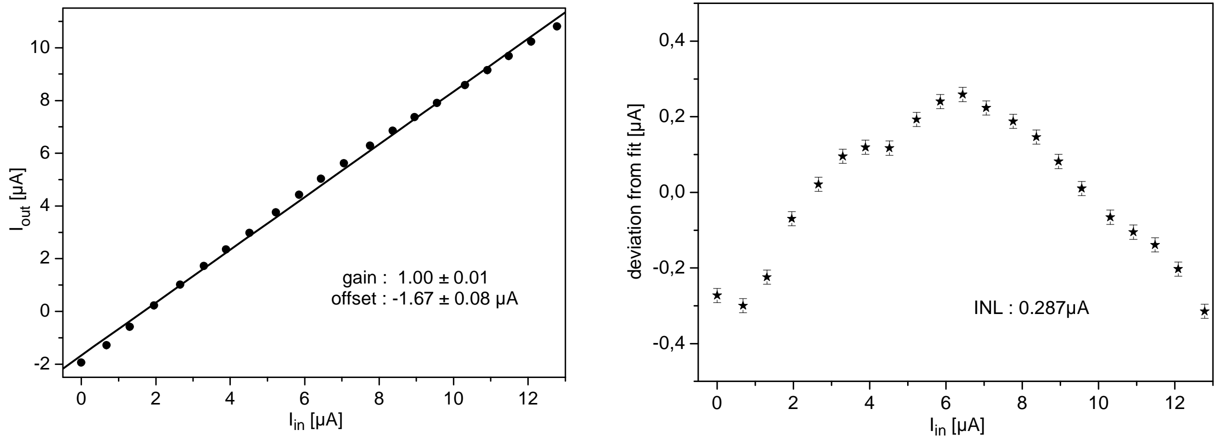

Figure 4.4: Linearity of one analog channel of CURO II. The output current is plotted as a function of the input current (left) and the deviation from a linear fit is shown (right).

linearity INL is defined as the maximum deviation from the proportionality divided by the observed dynamic range Δy

$$\mathrm{INL} = \frac{{}_{\max}|y_\mathrm{i} - y_\mathrm{i,f}|}{\Delta y} \tag{4.1}$$

where y_i are the measured data and $y_\mathrm{i,f}$ the numbers given by the linear fit. According to Fig. 4.4 (right) an INL of 2.3 % for a dynamic range of 12.5 μA is observed. Assuming a signal of 4000 e^- for a MIP in a 50 μm thin detector and an amplification of 1 nA/e^- of the DEPFET device, this range complies with the signal range of approximately three MIPs. Figure 4.5 (left) illustrates that the measured integral-non-linearity of the analog part is uniformly distributed over the chip showing a mean INL of 2.460 ± 0.003 % and a total range of 0.49 %. The transfer characteristic for all 128 channels are shown in Fig. 4.6. Both plots are zero suppressed. Due to the properties of the memory cell, the transfer behavior is, in first order, insensitive to fluctuations of the supply voltage and a narrow dispersion of the transfer gain with a mean deviation from a perfect transfer of $9 \cdot 10^{-5}$ and a total range of 0.012 is achieved. Such techniques have not been taken into account for the offset where a much broader dispersion is observed. However, any

[1]**M**ega **S**amples **P**er **S**econd

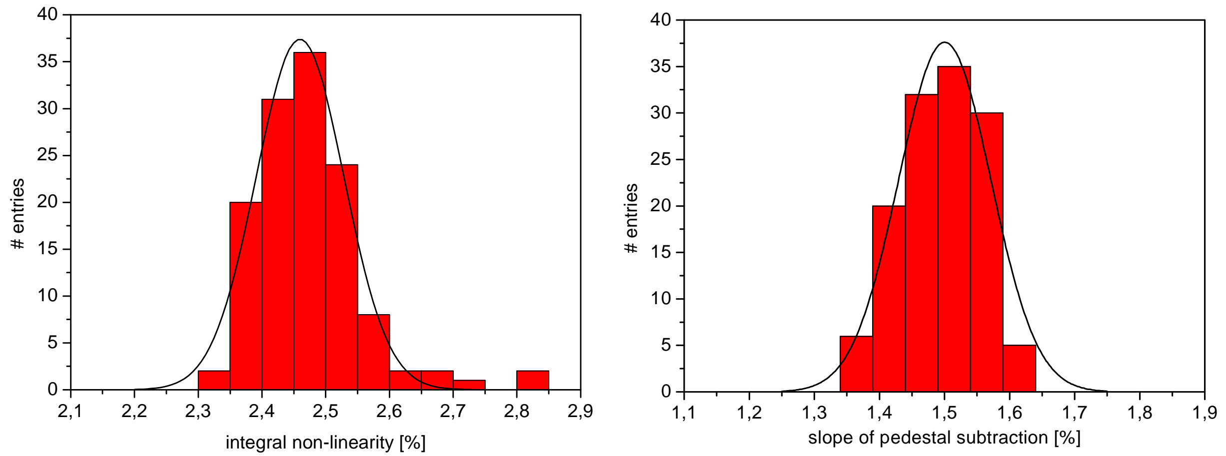

Figure 4.5: Dispersion of the integral non-linearity of the analog part of CURO II for a signal range of 12.5 μA (left) and the dispersion of the pedestal subtraction (right) for all 128 channels.

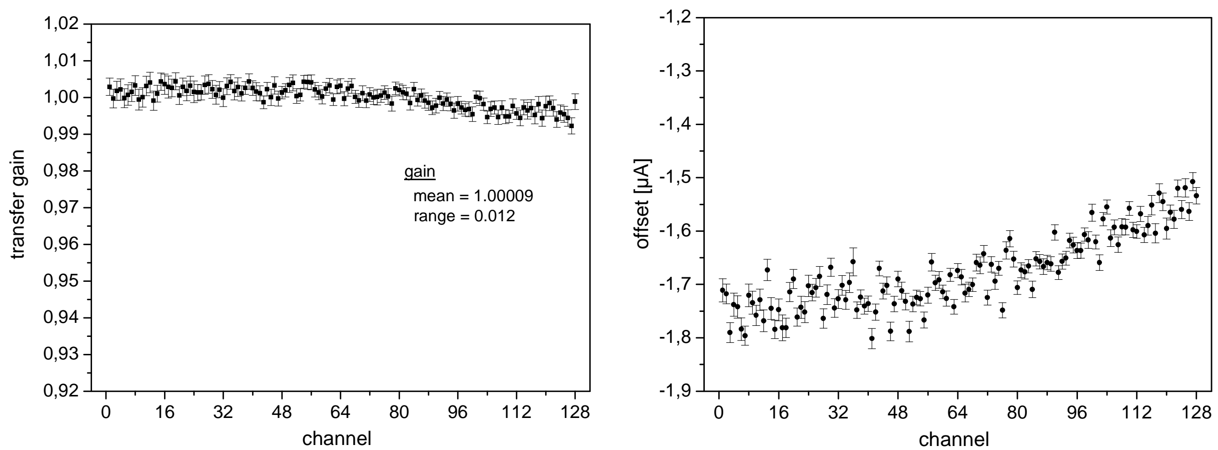

Figure 4.6: Homogeneity of the transfer gain (left) and offset (right) of the analog part for all 128 channels of CURO II.

inhomogeneity in the offset is of minor importance since it can be compensated by a threshold calibration using a 5 bit DAC integrated in the comparator unit, as discussed in section 4.4.

After the sample and hold process is performed, leakage current discharges the sampling capacitance of the memory cell. This deteriorates the performance of the memory cell when operating the chip at very low frequencies. However, for short sampling intervals (less than a second) this effect is expected to be small. To measure the discharge effect, the output signal of a single current memory cell, implemented as a teststructure, has been monitored after the sample and hold has been performed. Figure 4.7 shows the drift of the output current as a function of time. Using a linear fit, a drift of about 80 nA per second was extracted for the fine part of the memory cell. Hence, an operation of the chip at lower frequencies than 24 MHz without a noticeable performance loss is possible.

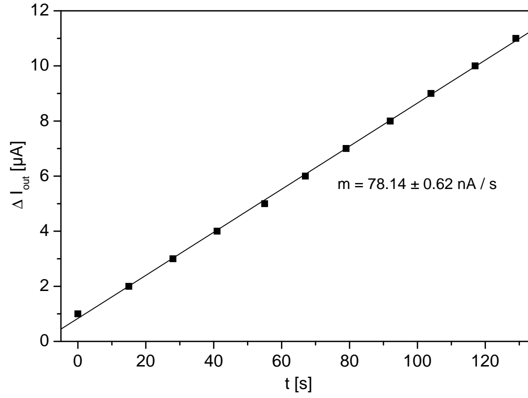

Figure 4.7: Drift of the output current of the current memory cell (fine part) at room temperature.

The performance of the pedestal subtraction has been measured by sweeping the pedestal current of the test source for a constant signal current. An accurate pedestal subtraction is needed since a global threshold will be used for the hit detection in the comparator stage. In the ideal case, the output of the analog part is independent of the pedestal for a given signal. The more the output current depends on the pedestal (i.e. the worse the pedestal subtraction is performed), the higher the comparator threshold needs to be set to compensate the pedestal variation. A channel wise dispersion of the pedestals in a matrix could also be compensated by the calibration unit implemented in the current comparator, see section 4.4. Inhomogeneities within a matrix column, on the other hand, cannot be compensated by this calibration. Further on, the number of rows in a ladder of the vertex detector is much larger than the number of columns. Hence, a much higher pedestal dispersion is expected within a column and an accurate pedestal subtraction is needed. Figure 4.8 (left) shows the observed output current of the chip as a function of the pedestal current for a constant signal current of 6.8 μA. The plot is

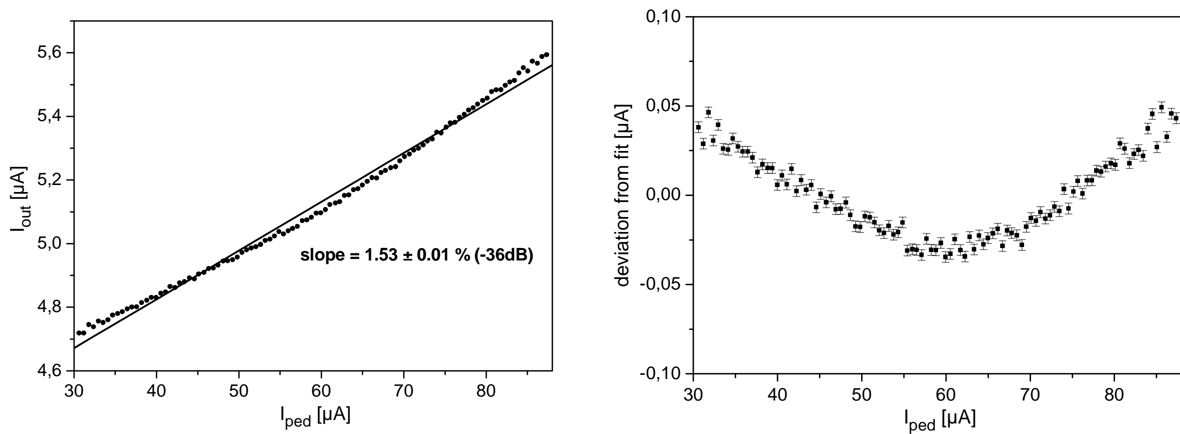

Figure 4.8: Performance of the pedestal subtraction. The output current is plotted as a function of the pedestal current for a constant signal current of $I_{sig} = 6.8\,\mu A$ (left). The deviation from a linear fit is shown (right).

zero suppressed. Although a linear dependence is not necessarily expected, a linear fit is used to qualify the pedestal subtraction. A slope of $1.53 \pm 0.01\,\%$ is observed. Assigning this performance to a DEPFET matrix with a statistical spread of $5\,\mu$A in the pedestals [57], a variation of 75 nA would remain after pedestal subtraction. This variation can be further reduced by an off chip fixed pattern correction. For the on-chip hit detection using a global threshold, this performance is more than sufficient. As shown in Fig. 4.5 (right), the pedestal subtraction is uniform for the whole chip since a mean slope of $1.500 \pm 0.008\,\%$ with a total spread of 0.26 % for all 128 channels has been observed.

4.3 Noise contribution of the readout

The dominant noise contribution of the CURO II chip is given by the current memory cells in the analog part, as described in section 3.3.4. It has been measured by observing the response of the comparator stage, shown in Fig. 3.15 in section 3.5, when sweeping the threshold for a given input current. The measurement has been performed at a row rate of 24 MHz at room temperature. As shown in Fig. 4.9, the ideal step response of the comparator is convoluted with the Gaussian noise distribution of the analog front end. The error bars in x are given by the uncertainty of the threshold current due to

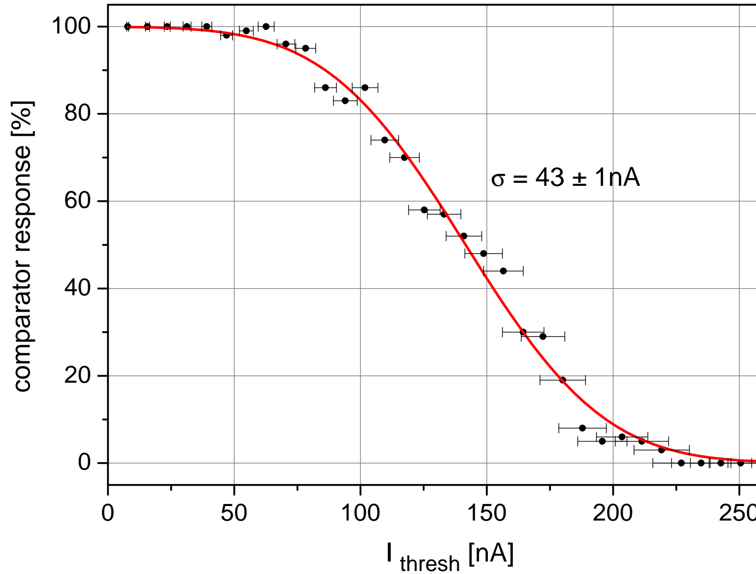

Figure 4.9: Noise contribution of the CURO II chip comprising an internal test current source and two sample stages measured at 24 MHz row rate. The comparator response has been fitted by an error function.

the non-linearity of the simple steering DAC in the order of 5 %. The function

$$y = \operatorname{erf}\left(\frac{x}{\sqrt{2}\sigma}\right) + \frac{1}{2} \tag{4.2}$$

with the inverse error function

$$\mathrm{erf}(z) = 1 - \frac{2}{\sqrt{\pi}} \int_0^z e^{-u^2}\, du$$

is fitted to the comparator response and a noise of $\sigma = 43 \pm 1\,\mathrm{nA}$ is found. Since the current comparator is located behind the pedestal and the buffer stage (see Fig. 3.2), this noise figure comprises of 2 memory cells and the test current source. Subtracting the noise of the current source of $\mathrm{i_{RMS}} \approx 23\,\mathrm{nA}$ after CDS (Correlated Double Sampling) in quadrature, the contribution of one current memory cell is $\mathrm{i_{RMS}} = 26.0 \pm 0.8\,\mathrm{nA}$. This number is in good agreement with the expected value of 25.3 nA calculated in section 3.3.6.

The noise induced by the memory cells is fixed by the bandwidth of the sampling circuit and will neither depend on the used sampling frequency nor on the load capacitance of the sensor. It is therefore important to measure the noise contribution for different sampling frequencies as soon as an adequate readout system is available.

With a total number of three sampling stages for the complete chip, the total noise would be $\mathrm{i_{RMS}} = 45 \pm 1\,\mathrm{nA}$ for the readout chain. However, the expected total noise has not been confirmed yet due to prominent pick-up noise in the test system.

4.4 Channel dispersion

Any inhomogeneity in the analog channels of the chip will cause a threshold dispersion in the comparator unit. To tune all channels to a global threshold, a 5 bit DAC is implemented in every channel for calibration, as shown in Fig. 3.15. The remaining dispersion after calibration should not exceed the noise performance since both figures, added in quadrature determine a lower limit of the threshold that can be used for hit discrimination. By performing threshold scans by the comparator unit as shown in Fig. 4.9 for every channel, the dispersion of the chip can be measured. Figure 4.10 shows the mean value of an error function fit applied to the comparator response before and after an internal calibration of all 128 channels. Without calibration, a dispersion of 1385 nA ($\sigma = 222 \pm 15\,\mathrm{nA}$) is observed. Such a dispersion is not tolerable since it is a factor of 5 times higher than the noise performance of the analog part. After applying the internal calibration the remaining dispersion is reduced to $\sigma = 25 \pm 3\,\mathrm{nA}$, which is well below the noise value of the analog part. Hence, the channel dispersion in the chip imposes no limit to the threshold for hit discrimination.

4.5 Zero suppression and digital tests

To test the functionality of the digital part a programmable testpattern has been implemented on the chip. The schematic overview of the test configuration is shown in

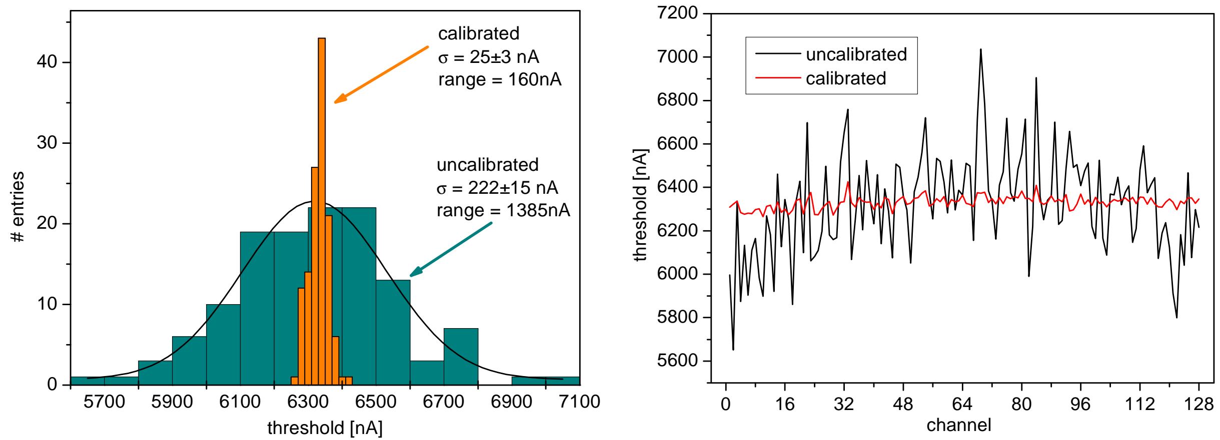

Figure 4.10: Channel dispersion of the comparator threshold before and after the internal calibration.

Fig. 4.11. The testpattern can be operated in a ring configuration so that an alternating and known pattern is applied in every cycle. Only patterns are reasonable, for which the number of hits that are written into the FIFO is less than the number of hits that are moved out by the hitscanner (up to 2 hits per s_clk cycle). Otherwise, the FIFO runs full after a few cycles and hits are lost. Such an incident can be validated by a "*FIFO-FULL*"-flag which is set in the chip if the FIFO runs full at any time. After the Hit-RAM is read out, the identified hits can be compared to the alternating test pattern. The tests show that the zero suppression by the digital part works up to a frequency of 110 MHz for both clocks. With up to two hits found in one clock cycle the digital part outperforms the expected occupancy at the innermost layer of the vertex detector of 1.7 hits every 20 MHz by more than a factor of 5.

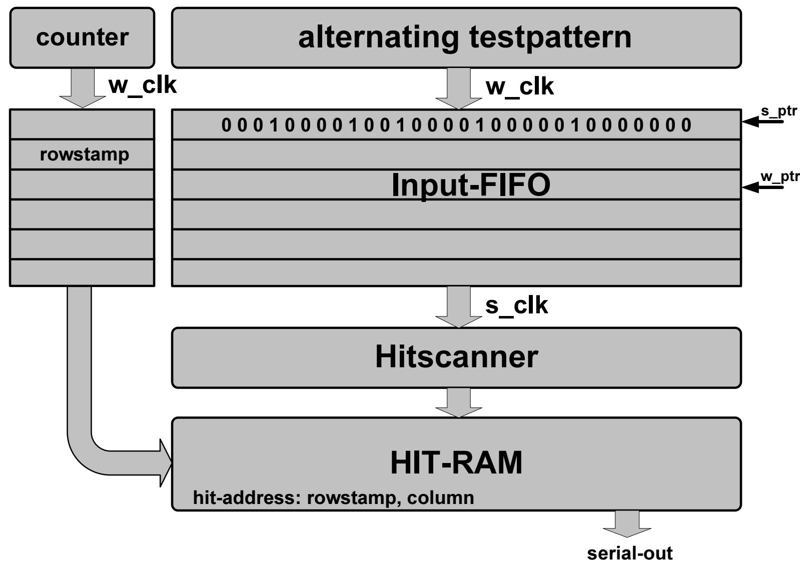

Figure 4.11: Schematic overview of the configuration for the digital tests.

4.6 Power consumption

To estimate the total power consumption of a DEPFET pixel based vertex detector (see chapter 5.3) the power consumption of the CURO II chip has been quantified by measuring the mean current $\bar{I}$ of the chip at the nominal supply voltage of U=2.5 V. The power consumption, given by $P = U \cdot \bar{I}$, as a function of the operating frequency is shown in Fig. 4.12. Both, the s_clk and the w_clk have been operated at the quoted

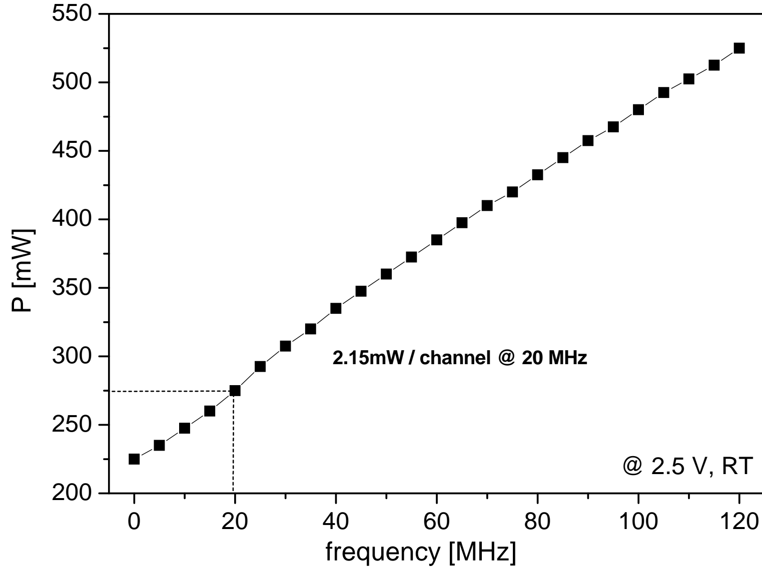

Figure 4.12: Total power consumption of the 128 channel readout chip CURO II as a function of the operating frequency (w_clk and s_clk).

frequency. The input cascode has been operated in the self biased case (DAC = 0). A static power consumption of 1.75 mW per channel has been measured at a very low frequency (10 kHz) to avoid that dynamic nodes in the current memory cells drift away. By switching of specific parts of the chip by appropriate biasing, their power contribution can be estimated:

- The regulated input cascode consumes 254 μW per channel in the self biased case (DAC=0), as expected.
- Their power contribution rises up to 859 μW per channel in case of maximum bias (DAC=255), as expected.
- The current memory cells dissipate 977 μW per channel. This number corresponds to a biasing current of 112 μA for each of the 3 memory cells and 55 μA for the pedestal subtracting cell.

A total power consumption of 2.15 mW per channel is observed at 20 MHz. Operating the chip at 50 MHz consumes 2.81 mW per channel. The power consumption of the chip and the several bias contributions are summarized in table 4.1.

total power	per channel
@ 20 MHz	2.15 mW
@ 50 MHz	2.81 mW
"static"	1.75 mW
bias contributions	**per channel**
current memory cells	977 μW
input cascode (self biased)	254 μW
input cascode (max. bias)	859 μW

Table 4.1: Power consumption per channel of the CURO II chip. The total power consumption for two different operating frequencies as well as some bias contributions are listed.

4.7 Towards an ILC CURO generation

Designed for a small 64 × 128 DEPFET pixel matrix, the first full size readout chip CURO II already meets the demanding requirements of the ILC. However, a final chip for a large scale ILC ladder will need modifications. The most important ones will be addressed in the following:

- The analog FIFO has to be scaled to a suitable size to cope with the expected occupancy.
- It would be advantageous if common mode correction, see section 6.5, is performed in the FIFO itself, since the analog information of the non-hit pixels in a row is lost after zero suppression. Such a correction can be implemented in the analog part conveniently because algorithmic operations, such as the calculation of a mean value and a pedestal subtraction can be performed easily and very accurately using currents.
- A more sophisticated clustering logic is needed in the digital part keeping at least the closest neighbors of an identified hit.
- Reading out a full size ladder with a larger capacitive load, the input impedance of the regulated cascode needs to be improved to achieve an adequate analog performance. This will need more power in the input stage. Furthermore, it may become necessary to move to a smaller process technology (e.g. 0.13 μm).
- A fast power down feature is needed to reduce the stand by power of the chip to a negligible contribution during the bunch gaps, see section 5.3.

All these topics are logical extensions of the existing chip and are not considered to impose severe difficulties.

4.8 Summary of the CURO II performance

For a fast readout of a DEPFET matrix a standalone 128 channel ASIC, CURO II has been successfully designed and fabricated. The DEPFET readout chip uses current mode techniques which are perfectly adapted to the current signals of the detector. Pedestal subtraction and current compare for standalone hit detection are performed on chip for a complete triggerless operation at the ILC. Zero suppression is implemented in the chip as well. The chip shows full functionality. The performance of the chip will be summarized in the following.

The analog part of the chip has been operated at a frequency of 24 MHz, faster than the row rate of 20 MHz needed at the ILC. Since two samples are performed per clock cycle this corresponds to a sampling rate of 48 MSPS. The transfer characteristic of the analog part has been measured to 1.00 ± 0.01 with an integral-non-linearity of 2.3 % for a dynamic range of 12.5 μA. Assuming a signal of 4000 e^- for a MIP in a thin DEPFET detector, a nonlinearity of 92 e^- has to be considered. Although this performance is sufficient, the non-linearity could be calibrated afterwards if a better performance is needed.

After pedestal subtraction the remaining dependence of the output current on the pedestal value is only 1.53 ± 0.01 %. Assigning this performance to a large DEPFET matrix with a typical spread of 5 μA in the pedestals, results to a variation of 75 nA after pedestal subtraction. The remaining variation could be further reduced by an off chip fixed pattern correction.

The noise contribution of the chip is dominated by the sampling noise in the current memory cells. The noise of a single memory cell has been measured to $i_{RMS} = 26.0 \pm 0.8$ nA, in perfect agreement with the calculated value, leading to an expected total noise contribution of the readout chain with 3-fold sampling of $i_{RMS} = 45 \pm 1$ nA.

Any channel dispersion of the readout chip can be calibrated by an internal 5 bit trimming DAC. After the calibration, a dispersion of $\sigma = 25 \pm 3$ nA has been observed. The dispersion is well below the noise figure of the chip, so that the dispersion in the chip does not limit the threshold for hit discrimination.

Zero suppression and the digital part have been successfully tested up to 110 MHz finding up to 2 hits per clock cycle in the binary pattern. With an expected hit density of 1.7 hits per row at a rate of 20 MHz, the digital part outperforms the occupancy at the ILC by more than a factor of 5.

It has been demonstrated that the performance of the CURO chip complies with the challenging requirements needed at the ILC. With minor extensions, the chip can be used for the readout of a full DEPFET pixel vertex detector.

5 Design consideration of a DEPFET pixel based vertex detector

Starting from the general requirements on the ILC vertex detector discussed in section 1.4, a conceptual design based on the DEPFET technology will be presented in this chapter. The crucial points of the proposed design, such as material budget, power consumption, a suitable thinning technology, the radiation tolerance and the expected noise performance will be discussed.

5.1 Module concept

As mentioned in section 1.4.2, the principle design of the vertex detector consists of 5 barrels arranged cylindrically around the beam pipe having a material budget of not more than $0.1\,\%\,X_0$ per layer. Each barrel is composed of several ladders to cover the whole cylinder area. A sketch of one end of a ladder is shown in Fig. 5.1. For lowest

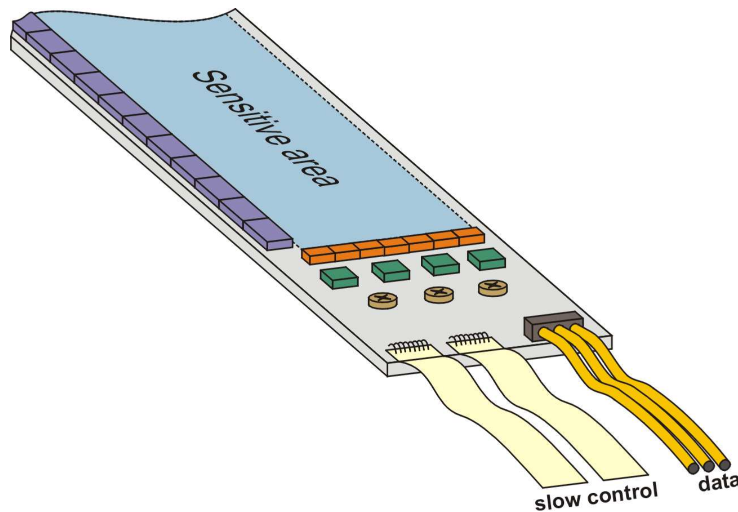

Figure 5.1: Sketch of one end of a DEPFET based ladder with thinned sensitive area supported by a silicon frame for the first layer of the ILC vertex detector.

material budget the sensitive area is thinned down to $50\,\mu$m supported by a thicker frame for mechanical stabilization. The steering chips for a row wise operation of the matrix are thinned to $50\,\mu$m as well and are attached to the thick frame along the long

layer	radius	ladder L×W	# pixels	# ladders	row rate / read out time	# hits
	[mm]	[mm^2]	[MPixel]	[r-ϕ/z]	[MHz] / [μs]	[BX^{-1}mm^{-2}]
1	15	100 × 13	2.1	8/1	20/50	4.3
2	26	125 × 22	4.4	8/2	20/250	2.4
3	37	125 × 22	4.4	12/2	20/250	0.6
4	48	125 × 22	4.4	16/2	20/250	0.1
5	60	125 × 22	4.4	20/2	20/250	0.1

Table 5.1: Key parameters of the DEPFET pixel based vertex detector.

side of the ladder by bump bonding technology. The signal traces from the steering chips to the sensor are integrated onto the support frame of the sensor module. The power consumption in the sensitive area is kept very low due to the row wise operation of the matrix, so that a simple cooling gas flowing along the beam pipe is sufficient. The readout electronics, the traces for power, slow control, and data transmission are placed at both short sides of the ladder outside the sensitive volume of the vertex detector. More elaborated cooling can be used there if needed. A detailed overview of the number of ladders per layer and their sizes are listed in table 5.1. In the innermost layer, only one ladder of 100 mm length extends along the z-direction. In layer 2-5 two ladders are attached to each other to cover a full length of 250 mm. For the calculation of the number of pixels per layer in table 5.1, a pixel size of $25 \times 25\,\mu\text{m}^2$ is assumed. The present pixel size with a conservative layout is approximately $30 \times 30\,\mu\text{m}^2$. A pixel dimension of 25 μm will be adopted in the next sensor generation. By exploiting charge sharing between neighboring pixels along with the excellent signal to noise ratio of the device, a much better spatial resolution in the order of a few microns compared to a binary read out is expected. A further reduction of the pixel size will not necessarily improve the resolution since more parameters like the set threshold for hit detection, the size of the charge cloud and the signal to noise ratio have an influence. The dependence of the spatial resolution on these parameters is currently under investigation to obtain an optimal pixel size and geometry.

The ladder pairs in layer 2-5 are read out in both directions as shown in Fig. 5.2 (top). For the innermost layer, the number of readout channels will be doubled with two readout chips placed at either side. Each chip reads out a quarter of the sensor matrix. With a pixel width of 25 μm the interconnections on the sensor will have a pitch of 12.5 μm. Like the steering chips, the readout chips will be connected to the sensor using bump bond and flip chip technology. The routing of the interconnections under the chip is done on the sensor using two metal layers, so that the effective pitch for the bonding is 50 μm. The access for slow controls and communication with the readout chips takes place at the side of the chip. The ladders in layer 2-5 are 5 times longer than in layer one but are read out in 250 μs instead of 50 μs. By doubling the channel density for the innermost layer a constant row rate for all ladders is achieved in a row wise operation. However, to satisfy the quoted frame rates of 20 kHz, see section 1.4.2, a row rate in the

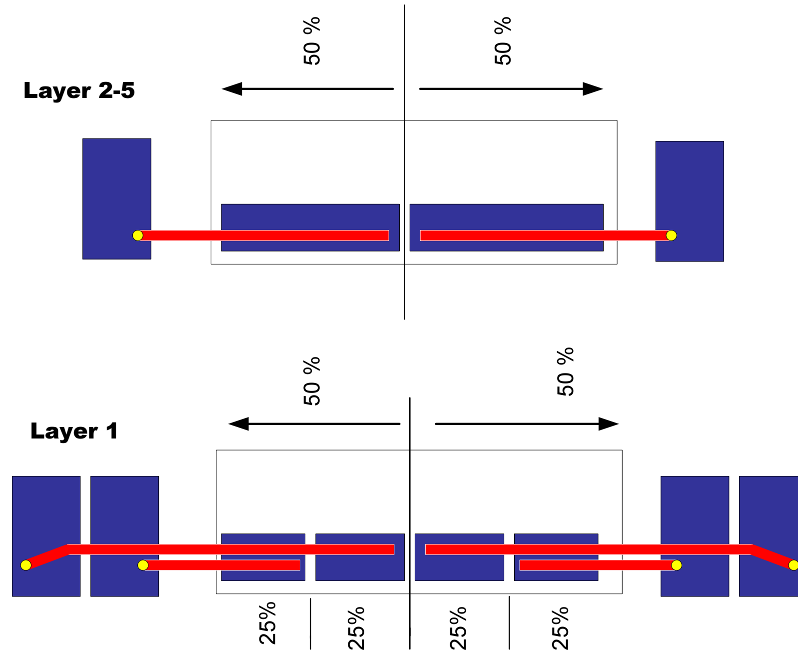

Figure 5.2: Readout concept for the innermost layer of the vertex detector (bottom) and for layer 2-5 (top).

vertex detector of 20 MHz is needed. This imposes a firm requirement on the sensor as well as on the matrix steering and readout since the cycle for a single row comprises two sampling steps with a clear of the sensor in between. Furthermore, the clear should optimally be complete to avoid additional reset noise. The readout scheme of the matrix is discussed in detail in section 3.1.

5.2 Thinning concept of a DEPFET device

As described in section 1.4.2, the reduction of material in the detector system is mandatory to minimize the multiple scattering contribution to the impact parameter resolution. The design of the DEPFET pixel based vertex detector therefore implies a sensor thinned down to about 50 μm thickness. Since the whole substrate of the DEPFET is used for charge generation, this thickness is a compromise between the total material budget and the achievable signal to noise ratio.

Back thinning technologies for microelectronic chips are already established in semiconductor industry. Such technologies like mechanical lapping and chemical etching (e.g. CMP[1]) remove the unused silicon from the back side of the wafer until a desired thickness is achieved. These conventional technologies present a way of thinning CCDs or MAPS [58] since these options do not rely on a back side treatment of the sensor. The DEPFET approach, on the other hand, needs an active back side in form of a p^+ im-

[1]**C**hemical **M**echanical **P**olishing

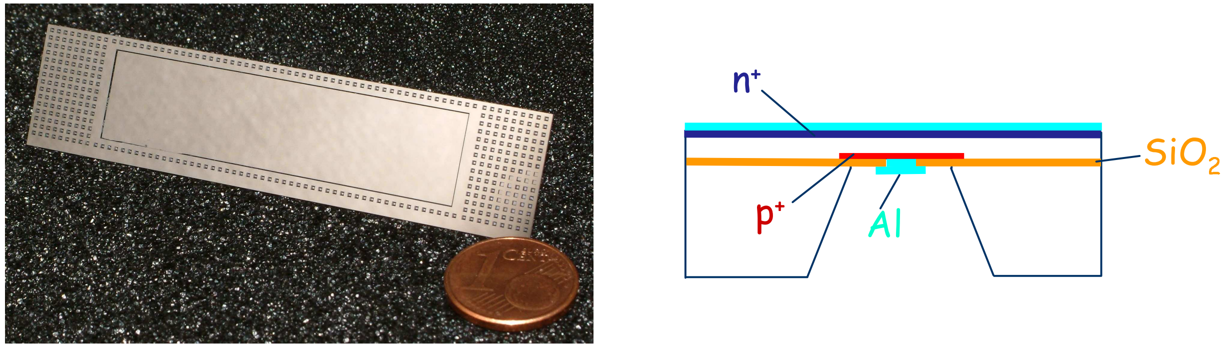

Figure 5.3: Mechanical sample of a $13 \times 50\,\mathrm{mm}^2$ large thinned silicon structure. The central area has been etched down to $50\,\mu$m keeping a $300\,\mu$m thick frame for stiffening. Holes have been etched in the frame area for further reduction of the amount of material (left). Cross section of a PiN diode on high resistivity n-substrate (right) [61].

plantation and a structured metalization to obtain a fully depleted sensor volume. If a standard thinning process is applied to the DEPFET device, the processing of the back side would have to be done afterwards. The treatment of such a thin and fragile foil of silicon is difficult and not possible with equipment designed to normally deal with thick wafers.

To overcome these difficulties an alternative thinning technology suitable for double sided devices has been developed at the MPI Semiconductor Laboratory in Munich. The key points of the thin sensor production are the so called "direct wafer bonding" [59] and the "deep anisotropic etching" [60]. A detailed description of the thinning technology can be found in [61].

Figure 5.3 (left) shows a mechanical sample which has been manufactured at the MPI Semiconductor Laboratory in Munich [61]. To demonstrate the feasibility of the technology beyond the mechanical scope, PiN diodes[2] of different sizes have been produced on thin substrate. The principle design of such a diode is given in Figure 5.3 (right). The back side configuration corresponds already to a final DEPFET production, whereas the front side has been left unstructured with a large area ohmic contact. Capacitance measurements of these diodes show that full depletion is achieved at a bias voltage of only $V_{RB} = 2.5$V for a $50\,\mu$m thick device [61]. Furthermore, a volume related leakage current of reverse biased diodes in the range of 120 nA per cm^3 at $V_{RB} = 5$V has been observed at room temperature [61]. Compared to an unthinned device this volume related leakage current is a factor of four higher. However, since the sensor volume is reduced for the thin devices by a factor of five, the area related leakage current is equal for both. The successful integration of diode structures on a thinned substrate show that this technology is viable to produce thin sensors for the ILC. Certainly, bringing the processing steps of a DEPFET device and the thinning technology together, has still to be demonstrated.

[2] A PN junction with intrinsic material in between.

5.3 Material budget and power consumption

In this section the power consumption and the material budget of a DEPFET pixel based vertex detector will be roughly estimated. The calculations are based on the baseline design of the detector mentioned in section 5.1.

The intrinsic advantage of the row wise operation of the DEPFET matrix is that only a minor fraction of the matrix is active for readout at the same time. Consequently, the power dissipated in the active area by the sensor, where cooling is particularly difficult, is small. The steering chips, mounted on one side of the support frame, are also placed in the active region of the vertex detector, so that their heat dissipation must be minimized. The access to the readout chips, situated at the ladder ends, is much easier and active cooling is an option without compromising the material budget in the central region. Furthermore, the material used there is outside of the active area of the vertex detector. However, this material should be reduced to a minimum as well since it has an impact on the outer tracking components.

Power consumption

For the estimation of the power consumption, the present steering and readout chips are taken into account. Hence, the SWITCHER II chip is considered for the matrix steering and the CURO II chip is used for readout. Details concerning SWITCHER II can be taken from [38]. The CURO II chip has been discussed in detail in chapters 3 and 4. The standalone power consumption of the components has been measured to be:

- 2.15 mW per channel for the CURO II chip at a frequency of 20 MHz, as presented in section 4.6.
- 250 μW for a DEPFET pixel, using $V_{DS} = 5$ V and $I_D \approx 50\,\mu$A [32].
- 4.3 mW per channel for the SWITCHER II chip at a frequency of 20 MHz and 0.5 mW per channel for the idle chips in the ladder [62].

To estimate the total power consumption of the vertex detector, the number of readout channels and the number of rows have been enumerated and are listed in table 5.2. To compute the number of pixels per row and channel a pixel size of $25 \times 25\,\mu m^2$ has been assumed. The number of readout channels per layer is given by multiplying the number of ladders per layer with the number of channels per ladder, considering the different readout multiplicities for each layer.

For the readout chips, a total number of 115200 readout channels is considered. The number of active DEPFET pixels is equivalent to the number of readout channels.

- The readout chips consuming 2.15 mW per channel dissipate 248 W in total at the ladder ends.

layer	# ladders/ r/o mult.	# channels per ladder	# channels per layer	# rows per ladder	# rows per layer
1	8/4	520	16640	4000	32000
2	8/2	880	14080	10000	80000
3	12/2	880	21120	10000	120000
4	16/2	880	28160	10000	160000
5	20/2	880	35200	10000	200000
total	**144**		**115200**		**592000**

Table 5.2: Enumeration of the readout channels and matrix rows to estimate the total power consumption of the DEPFET pixel based vertex detector.

- With a mean power consumption of 250 μW per pixel, the sensor will contribute 28.8 W for the whole vertex detector.

The low power contribution of the sensor is achieved since only a very small part of the pixels is active at a time. Operating all 510 MPixels at the same time would consume 127.5 kW. Therefore, only a row wise operation of the DEPFET is feasible at the ILC.

For the steering chips, the number of active rows is calculated by summing all ladders in the vertex detector, taking the readout multiplicity into account. Furthermore, the rest of the 592000 rows in the ladders have to be switched off.

- With a total number of 144 active rows at a time, the switching contribution of the steering chip is 0.6 W.
- 296 W static power is needed by the idle steering chips to keep the rows switched off.

Since the power of the steering chips is dissipated in the active volume with difficult cooling access, the static power consumption will be minimized in a future chip generation.

With 29 W coming from the sensor, 248 W from the readout chips and 297 W from the steering chips, the total power consumption of the vertex detector is 574 W, operated continuously. Taking into account that the detector only needs to be operated during the bunch crossings of the beam, a mean power consumption of 2.9 W can be achieved in a pulsed mode with a duty cycle of 1:199. This assumes that the dissipation of the chips in the bunch gaps is made negligible by appropriate circuit design and that the pulsed operation can be perfectly synchronized to the bunch timing of the machine. Such a fast power down feature is not implemented in the present chips and will be a crucial addition for future chip generations. A perfect timing between the pulsed operation of the chips and the beam bunches is rather optimistic so that a power reduction of 1:199 is not realistic. However, a duty cycle of 1:30 would still result to a mean power of less than 20 W.

area	thickness [μm]	width [mm]	mean thickness [μm]	% X_0 (Si)
frame	300	$50\,\% \cdot 4$	35.29	0.038
chip	50	3	8.823	0.009
sensor	50	13	38.24	0.041
total			82.35	**0.088**

Table 5.3: Material Budget for layer one of the vertex detector.

Material Budget

For a rough estimation of the material budget the cross sectional sketch of a module ladder as shown in Fig. 5.4 is considered. The sensor area is thinned down to 50 μm

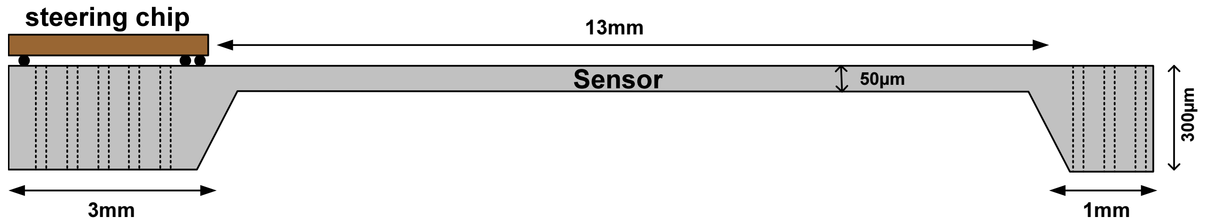

Figure 5.4: Cross section of a ladder perpendicular to the beam pipe showing the thinned sensor area, the perforated frame with etched holes and the steering chips bump bonded to one sensor side.

and the 300 μm thick frame for mechanical stabilization is perforated to save 50 % of the material. The steering chips bump bonded to side of the sensor are assumed to be thinned down to 50 μm as well. It is assumed that the power consumption of the detector can be held that low that the cooling can be done by a gas. Therefore, any material for cooling in the active area will not be considered in the following.

By smearing the material over the whole ladder of 17 mm width, a mean ladder thickness is calculated. The individual contributions by the sensor, the frame and the steering chip are given in table 5.3 and a mean thickness of 82.35μm is obtained. With the radiation length of X_0=9.36 cm for silicon this corresponds to 0.088 % X_0. Even with a few additional traces to further support the large area of the thinned sensor material, the total material is not expected to exceed 0.1 % X_0. For the outer layer (2-5) having approximately twice the width, an additional support trace is foreseen in the middle of the ladder. The material distribution is therefore similar to the innermost layer and an equivalent mean material budget is expected.

Although the conceptual design of a DEPFET based vertex detector requires steering chips in the active area, a material budget of 0.1 % X_0 per layer can be achieved and an excellent impact parameter resolution for low particle momenta is obtained. On the other hand, the inhomogeneous distribution of the material has to be considered in the later analysis and might make track reconstruction more complicated.

5.4 Radiation Tolerance

The whole vertex detector has to sustain the radiation dose expected at the ILC. This comprises ionizing radiation, such as e^+e^- pairs produced by the beam-beam interaction, and NIEL[3] damage due to neutron background. Concerning ionizing radiation an integrated dose of 100-200 kRad after 5 years of operation is expected [13]. Neutrons are produced as secondaries if the beamstrahlung, e^+e^- pairs, or other particles hit parts of the detector or elements of the beam delivery system. In the vertex detector a neutron flux of 10^9 MeV equivalent n/(cm^2 year) is expected. The neutrons reaching the vertex detector are mainly produced by the e^+e^- pairs [63].

Since the transistors integrated in the DEPFET pixels are MOS transistors with thick gate oxides, the device is inherently susceptible to ionizing radiation. The main total ionizing dose effect, the shift of the threshold voltage to more negative values, is caused by radiation induced charge built up in the oxide and interfacial regions. To investigate the radiation tolerance of the current sensors, single pixels have been irradiated with a dose rate of 20 kRad(SiO_2)/h using ^{60}Co X-rays at the GSF facility in Munich [64]. The irradiation was stopped after 912 kRad(SiO_2). The devices under test were identical to the DEPFET pixels in the matrix, except for a larger gate area (gate lengths L=6 μm, 7 μm and widths W=25 μm). During normal operation at the ILC, the DEPFET pixel is switched off most of the time and is activated only for readout of the device current. Thus, the irradiation of four test devices was done with the transistors in "*off state*" to test the radiation tolerance in this most frequent operation mode. To investigate the implication of the biasing conditions on radiation tolerance, two transistors were also irradiated in "*on state*". The input characteristic of the devices were measured immediately (approximately 1 min.) after each irradiation period and the threshold voltage was extracted by a quadratic extrapolation of the $I_D(V_G)$-curve to $I_D = 0$. Figure 5.5 shows the threshold voltage shift ΔV_{th} and the density of the oxide trapped charge ΔD_{OT} of six pixels, biased in "*off state*" and "*on state*", as a function of the total ionizing dose. For the transistors irradiated in "*off state*", the threshold voltage shift saturates after an ionizing dose of about 100 kRad. The voltage shift at 200 kRad is about $-4\,V$. The DEPFETs irradiated in the "*on state*" are less radiation tolerant and the saturation of the voltage shift is less significant. The reason for the different radiation effects between both biasing conditions is yet not fully understood and is still under investigation. It can be attributed to different field configurations inside the oxide in the respective situations. Based on small number of irradiated devices, identical DEPFET pixels, biased in the same way during irradiation, show very similar characteristics after irradiation. Hence, the radiation induced threshold voltage shift can most likely be compensated by a gradual decrease of the gate voltage needed for the selection of a pixel row.

To investigate the effect of radiation damage on the noise performance of the device an ^{55}Fe spectrum using a single pixel (L=6 μm) has been taken after an irradiation dose of 912 kRad(SiO_2) [64]. The spectrum is shown in Fig. 5.6 and has been taken at room

[3] **N**on-**I**onizing **E**nergy **L**oss

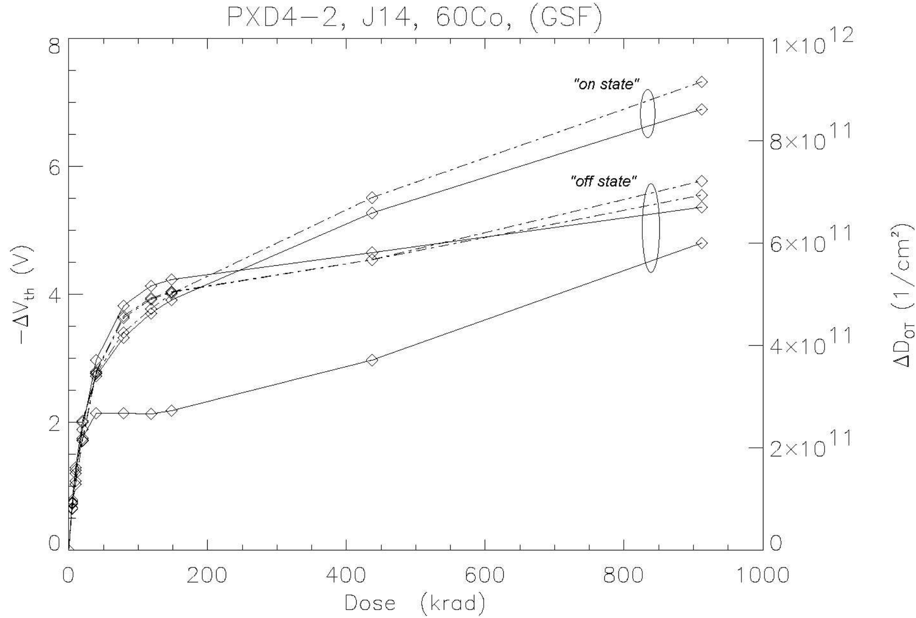

Figure 5.5: Threshold shift ΔV_{th} and generated oxide trapped charge ΔD_{OT} during ^{60}Co irradiation [64].

temperature with a shaping time of $\tau_S = 6\,\mu$s. Fitting a gaussian curve to the ^{55}Fe k_α-peak yields an energy resolution (FWHM) of $174 \pm 2\,$eV. After subtracting the Fano noise in quadrature, a noise figure of ENC=$14.5 \pm 0.2\,e^-$ remains. This noise figure after irradiation is an order of magnitude better than needed at the ILC.

Hence, DEPFET pixels are radiation hard at ILC doses concerning their noise performance and the principle transistor operation in a matrix. Radiation effects on the efficiency of the device clear, realized by a MOS structure (cleargate) and NIEL damages in the bulk by hadron irradiation still have to be investigated. However, damage of the silicon bulk due to NIEL is expected to be of minor importance for the device since there is no charge transfer[4] during the operation of DEPFET matrices.

The readout and steering chips have to sustain the mentioned radiation doses as well. The readout chip, CURO II, is fabricated in a deep sub micron process. In addition, radiation tolerant layout rules [53] have been followed wherever possible. The fabrication process and the layout rules are similar to the ones used for the strip and pixel readout chips developed for the ATLAS experiment. Hence, the readout chip is expected to tolerate the radiation dose at the ILC. The present steering chip, SWITCHER II, partially uses transistors with thicker gate oxide to multiplex the high voltages needed for the clear. Their radiation tolerance has not been demonstrated yet. On the other hand, measurements presented in [32] show that for an optimized DEPFET layout a complete clear can already be achieved with voltages in the range of 5 V. Since these voltages can be covered by standard CMOS processes with better radiation tolerance, an alternative steering chip in CMOS technology can be fabricated if the current steering chip turns

[4]For a discussion of NIEL damage in CCDs, see [65].

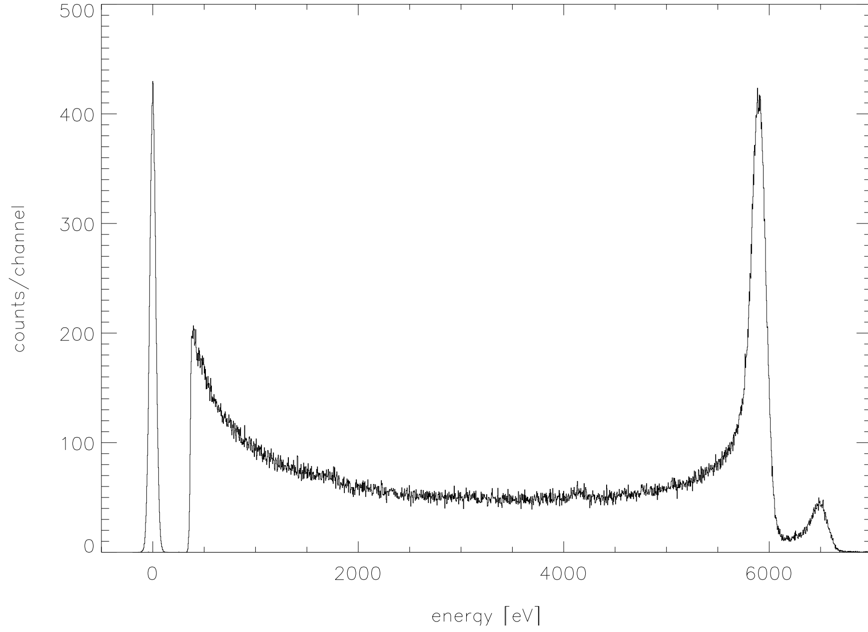

Figure 5.6: ^{55}Fe spectra ($\tau_{\mathrm{S}} = 6\,\mu$s) of a DEPFET single pixel at room temperature after irradiation with a dose of 912 kRad using ^{60}Co [64].

out to be not sufficiently radiation tolerant.

5.5 Estimated noise performance

To estimate the expected noise performance of a DEPFET system operated at the ILC timing scheme the following noise sources will be analyzed in this section:

- Sensor noise after performing correlated double sampling (CDS) in the readout chip.
- Noise contributed by the readout chip, CURO II.
- Switching noise after CDS due to the steering chip, SWITCHER II.

As shown in Fig. 5.7 (left), a voltage noise $\langle V_{\mathrm{G}}^2 \rangle$ at the gate of the DEPFET transistor can be converted into a current noise $\langle I_{\mathrm{D}}^2 \rangle$ according to the external transconductance g_{m} of the transistor

$$\langle I_{\mathrm{D}}^2 \rangle = g_{\mathrm{m}}^2 \cdot \langle V_{\mathrm{G}}^2 \rangle \tag{5.1}$$

To obtain the mean square value of the equivalent noise charge $\langle \mathrm{ENC}^2 \rangle$, the current noise $\langle I_{\mathrm{D}}^2 \rangle$ is divided by the square of the amplification of the internal gate g_{q}

$$\langle \mathrm{ENC}^2 \rangle = \langle q^2 \rangle = \frac{\langle I_{\mathrm{D}}^2 \rangle}{g_{\mathrm{q}}^2} \tag{5.2}$$

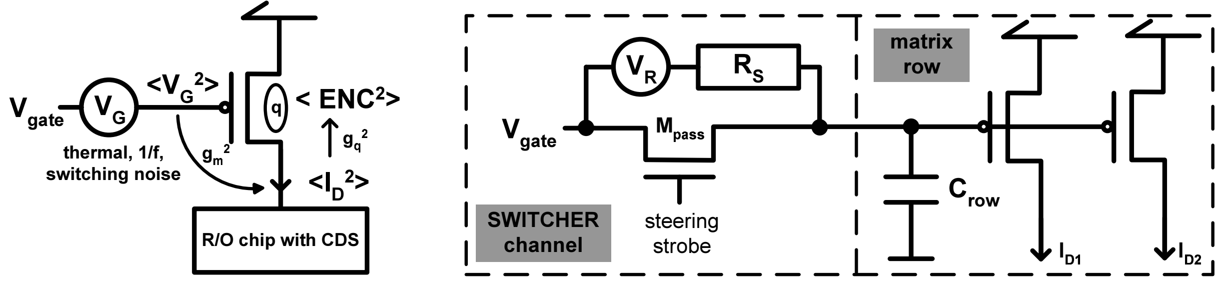

Figure 5.7: Conversion of a voltage noise at the gate of the DEPFET transistor into a current noise and into an equivalent noise charge (left). Simplified output stage of one channel of the SWITCHER II chip steering a matrix row (right).

Using equation (5.1) in equation (5.2) yields

$$\langle \mathrm{ENC}^2 \rangle = \frac{g_\mathrm{m}^2}{g_\mathrm{q}^2} \langle V_\mathrm{G}^2 \rangle \tag{5.3}$$

Hence, a voltage noise source at the gate can be translated into an equivalent noise charge using the external transconductance g_m and the amplification of the internal gate g_q.

DEPFET sensor

For the sensor, 1/f noise, thermal noise and shot noise due to leakage current are taken into account.

1/f noise has a severe impact on the sensor noise, if the bandwidth is not limited at the low frequency end. Therefore, in the readout chip fast correlated double sampling is performed. The influence of CDS on the different noise contributions has been treated in detail in appendix A. It has been shown that the suppression of 1/f noise strongly depends on the relation between the bandwidth of the sampling circuit ν_c and the sampling interval τ [66].

The power spectral density for 1/f-noise of a DEPFET sensor given by

$$s_{1/\mathrm{f}}^2 = a_{1/\mathrm{f}} \frac{g_\mathrm{m}^2}{g_\mathrm{q}^2} \tag{5.4}$$

where $a_{1/\mathrm{f}}$ is the 1/f noise coefficient. Using the 1/f power spectral density in equation (A.9) leads to

$$\langle \mathrm{ENC}_{1/\mathrm{f}}^2 \rangle = a_{1/\mathrm{f}} \frac{g_\mathrm{m}^2}{g_\mathrm{q}^2} \cdot 2 \int_0^\infty \frac{1 - \cos(2\pi\nu_\mathrm{c}\tau \cdot x)}{x\,(1 + x^2)}\, dx \tag{5.5}$$

Solving the integral numerically and using

- a 1/f noise coefficient of $a_{1/\mathrm{f}} = 1.8 \cdot 10^{-11}\,\mathrm{V}^2$ (from [4], scaled to a transistor size of W=20 and L=5),
- a system bandwidth of ν_c=50 MHz,
- and an interval of τ=50 ns for the consecutive samples (20 MHz row rate respectively)

results in a 1/f noise contribution of $\mathrm{ENC}_{1/\mathrm{f}} \approx 1.6\,\mathrm{e}^-$ at room temperature.

Thermal noise is hardly affected by CDS. For a DEPFET device the thermal power spectral density is described by

$$s_\mathrm{th}^2 = 4kT\,\frac{2}{3\,g_\mathrm{m}}\,\frac{g_\mathrm{m}^2}{g_\mathrm{q}^2} \tag{5.6}$$

with the thermal voltage power spectral density $V_\mathrm{th}^2 = 4kT\frac{2}{3\,g_\mathrm{m}}$ of the DEPFET transistor. According to equation (A.7), thermal noise contributes

$$\langle \mathrm{ENC}_\mathrm{th}^2 \rangle = 4kT\,\frac{2}{3}\,\frac{g_\mathrm{m}}{g_\mathrm{q}^2}\,\nu_\mathrm{c}\pi\left(1 - e^{-2\pi\nu_\mathrm{c}\tau}\right) \tag{5.7}$$

after CDS. Using ν_c=50 MHz and τ=50 ns yields a thermal noise of $\mathrm{ENC}_\mathrm{th} \approx 29\,\mathrm{e}^-$ at room temperature.

Integrating a leakage current of 0.178 pA/pixel, measured in section 6.4 at room temperature, over a frame time of 50 μs, a charge fluctuation of $\mathrm{ENC}_\mathrm{shot} \approx 8\,\mathrm{e}^-$ is expected. Since the DEPFET device can, in principle, be cleared completely [67], the clearing process can be neglected in the noise analysis. When the clear is not complete [32], the noise contribution due to the charge fluctuation in the internal gate has to be considered as well.

Readout chip

The dominant noise of the CURO II chip is given by the current memory cells. The noise contribution of a single current memory cell has been measured to $\mathrm{i}_\mathrm{RMS} = 26.0 \pm 0.8\,\mathrm{nA}$ at room temperature, see section 4.3, in good agreement with the calculated value, see section 3.3.6. For the readout chain with 3-fold sampling the expected total noise is $\mathrm{i}_\mathrm{RMS} = 45 \pm 1\,\mathrm{nA}$. With $\mathrm{g}_\mathrm{q} = 282.6 \pm 3.3\,\mathrm{pA/e}^-$, the noise contribution of the readout is $\mathrm{ENC}_\mathrm{CURO} = 159 \pm 5\,\mathrm{e}^-$.

Steering chip

A simplified output stage of one channel of the steering chip is shown in Fig. 5.7 (right). The gate voltage V_gate is multiplexed to a matrix row by a pass transistor M_pass. The

switch resistance of the pass transistor is indicated by R_S. The dominant noise contribution of the steering chip is due to thermal noise of the pass transistor. Its voltage power spectral density is given by

$$V_\mathrm{R}^2 = 4kTR_\mathrm{S} \tag{5.8}$$

By using the power spectral density

$$s_\mathrm{steer}^2 = 4kTR_\mathrm{S}\,\frac{g_\mathrm{m}^2}{g_\mathrm{q}^2} \tag{5.9}$$

in equation (A.7), the thermal noise contribution of the pass transistor to a DEPFET readout after CDS calculates to

$$\langle \mathrm{ENC}_\mathrm{steer}^2 \rangle = 4kTR_\mathrm{S}\,\frac{g_\mathrm{m}^2}{g_\mathrm{q}^2}\,\frac{\omega_\mathrm{c}}{2}\left(1 - e^{-\omega_\mathrm{c}\tau}\right) \tag{5.10}$$

The switch resistance R_S and the capacitive load of a matrix row C_row form a low pass that filters the voltage noise at the DEPFET gate. Assuming that this is the dominant pole in the system, the cut-off frequency is given by $\omega_\mathrm{C} = (R_\mathrm{S}C_\mathrm{row})^{-1}$ and equation (5.10) becomes

$$\begin{aligned}
\langle \mathrm{ENC}_\mathrm{steer}^2 \rangle &= 2\cdot\frac{kT}{C_\mathrm{row}}\,\frac{g_\mathrm{m}^2}{g_\mathrm{q}^2}\left(1 - e^{-\tau/R_\mathrm{S}C_\mathrm{row}}\right) \\
&\approx 2\cdot\frac{kT}{C_\mathrm{row}}\,\frac{g_\mathrm{m}^2}{g_\mathrm{q}^2} \quad \text{for} \quad \tau \geq 2\pi R_\mathrm{S}C_\mathrm{row}
\end{aligned} \tag{5.11}$$

whereas the approximation in equation (5.11) assumes that the sampling interval τ is longer than the time constant of the low pass[5]. Note, that the noise is of kT/C-nature and that the absolute value of the switch resistance does not contribute. For typical values of $C_\mathrm{row} \approx 15\,\mathrm{pF}$, $g_\mathrm{m} \approx 40\,\mu\mathrm{S}$ and $g_\mathrm{q} = 282.6 \pm 3.3\,\mathrm{pA/e^-}$ of the present DEPFET devices, a noise contribution of $\mathrm{ENC}_\mathrm{steer} \approx 3.3\,\mathrm{e^-}$ at room temperature is calculated.

Total noise

The calculated noise contributions are summarized in table 5.4. Summing all noise sources in quadrature results to a total noise of $\mathrm{ENC} \approx 162\,\mathrm{e^-}$ for a fast ILC-readout with the present sensors having a $\mathrm{g_q} \approx 283\,\mathrm{pA/e^-}$. It is dominated by the contribution of the readout chip. The noise figure can be improved by:

- using sensor devices with a higher internal amplification. For proposed devices having a $\mathrm{g_q} = 1\,\mathrm{nA/e^-}$ [68] the noise will be about $48\,\mathrm{e^-}$.

[5]This is a reasonable assumption, otherwise the matrix steering is not fast enough.

noise source	ENC
switching noise due to the steering chip	$\approx 3.3\,e^-$
sampling noise in the readout chip	$159 \pm 5\,e^-$
1/f noise of the sensor	$\approx 1.6\,e^-$
thermal noise of the sensor	$\approx 29\,e^-$
shot noise due to leakage current	$\approx 8\,e^-$
total noise	$\approx 162\,e^-$

Table 5.4: Calculated noise contributions for an ILC DEPFET-System.

- operating the system at a lower temperature, which may be necessary at the ILC anyway. For example, reducing the temperature to 100 K, the noise will correspond to $95\,e^-$ with the present devices.

Using 50 μm thin DEPFET devices with a MIP signal of $4000\,e^-$, these noise figures of 50-100 e^- translate to an excellent signal to noise ratio of 40-80.

5.6 Summary of the DEPFET pixel based vertex detector

The requirements on the vertex detector of the ILC are demanding in various respects. Studies done by the LCFI-group show that in order to achieve a sufficient impact parameter resolution for c-tagging, a material budget not higher than 0.1 % X_0 per detector layer is mandatory. The baseline design of the vertex detector consists of 5 barrels starting with the innermost layer right outside the beam pipe, 15 mm away from the interaction point and covers a radius up to 60 mm. With the proposed design an unprecedented impact parameter resolution of

$$\sigma(d_0) = 3.9 \oplus \frac{7.8}{p \cdot \sin^{\frac{3}{2}} \theta}\ \mu\text{m} \tag{5.12}$$

is expected.

By placing the detector that close to the interaction point, the occurring background rate induced by beamstrahlung of the focused beam becomes very high. To achieve an adequate occupancy of $\approx 1\,\%$ for efficient track finding, the vertex detector has to be read out with a row rate of 20 MHz. The baseline design of the vertex detector is still in progress. It is therefore possible that the readout requirements may change. For example, reasons related to the machine design might force the beam pipe to a larger radius. However, moving the innermost layer more outside requires a longer ladder to cover the same angular coverage of the detector and the resulting row rate will be similar.

A principle design concept of a DEPFET pixel based vertex detector has been presented that complies with the demanding requirements of the ILC. Using an adequate thinning

technique, the sensor area is thinned to 50 μm and only a small frame of 300 μm thickness is left for the mechanical handling of the device. The average material budget expected is below 0.1 % X_0 per detector layer. The power consumption of the detector is a crucial point as well, since introducing cooling components would increase the material budget intolerably. The power consumption can be kept low due to the row wise operation of the DEPFET matrix, where only a minor part of the detector is active at a time. Operating the detector with a duty cycle of 1:30 (the duty cycle of the bunch train is 1:199, leaving sufficient time for settling of the system) a mean power consumption of 20 W for the entire vertex detector is achieved. It is expected that simplest cooling in form of a cooling gas flowing along the beam pipe can cope with this power dissipation. Furthermore, operation at room temperature is not problematic for a DEPFET based vertex detector.

Measurements on the radiation hardness of the sensor show a tolerance against ionizing radiation of up to 1 MRad, a factor of 5 more than expected at the ILC. The occurring shifts in the threshold voltages of the device can be compensated by adjustment of the steering voltages. Radiation tolerance of the clear operation and radiation damage due to neutron background has still to be investigated.

The total noise performance of a DEPFET system operated at speed suited for the ILC has been calculated. For the present DEPFET sensors, a noise figure of about 162 e^- at room temperature is expected. Using devices with a higher amplification due to smaller transistor gate lengths, a noise below 50 e^- is possible. One of the most significant properties of the DEPFET sensor is the fully depleted bulk that is used for charge generation by impinging particles. Therefore, a large signal of 4000 e^- is produced for a MIP, even in a 50 μm thin detector. Together with the expected noise performance an excellent signal to noise ratio of 40-80 is a reasonable estimate for DEPFET pixels at the ILC.

6 The ILC DEPFET-System

As an intermediate step towards a full size ladder for the ILC vertex detector, a prototype system for the operation of a 64×128 DEPFET pixel matrix has been developed. The system uses two dedicated chips, SWITCHER II providing the matrix steering and CURO II for readout. In this chapter the buildup of the prototype system and the readout sequence for the operation of the DEPFET matrix will be described. Results obtained with X-rays in the energy range from 6 to 60 keV using different radioactive sources will be reported. The noise performance has been studied in comparison with calculated values. The internal amplification of the DEPFET sensor and the linearity of the system is determined.

6.1 Description of the system

A photograph of the ILC DEPFET-System is shown in Fig. 6.1 (left). A schematic overview of the system is given in Fig. 6.2. It consists of three main parts: a USB communication board, a S2E DAQ board and a sensor hybrid. The USB and S2E board are connected to the sensor hybrid by a ribbon cable. The sensor hybrid hosts the DEPFET pixel matrix, the two SWITCHER II steering chips and the CURO II readout chip. The two current outputs of the CURO chip are converted into differential voltages by a set of transimpedance amplifiers (I2U). During commissioning of the sensor hybrid it turned out to be advantageous to use an unpackaged version of the transimpedance amplifier and to wire bond the bare chips directly to the CURO to reduce stray capacitances and pick-up noise in the system. The voltage signals of the transimpedance amplifiers are digitized by two 14bit ADCs on the S2E-Board and stored in an SRAM for subsequent readout. Integral part of the S2E-Board is a SPARTAN 2E FPGA providing the configuration of all chips and managing the synchronization between the components during data acquisition. The USB-Board provides the communication with a PC using the USB 1.1 standard. A protection board, attached to the S2E-Board monitors the proper ranges of the supply voltages handed to the hybrid.

Figure 6.1 (right) shows a micro photograph of the sensor hybrid with the 64×128 pixel DEPFET-Matrix in the middle, two steering chips SWITCHER II at the side and the readout chip CURO II at the bottom. The chips are interconnected with the matrix via wire bonds. The measurements presented here have been done using the matrix G01, which has a pulsed cleargate and is fabricated without highE-implantation. The matrix

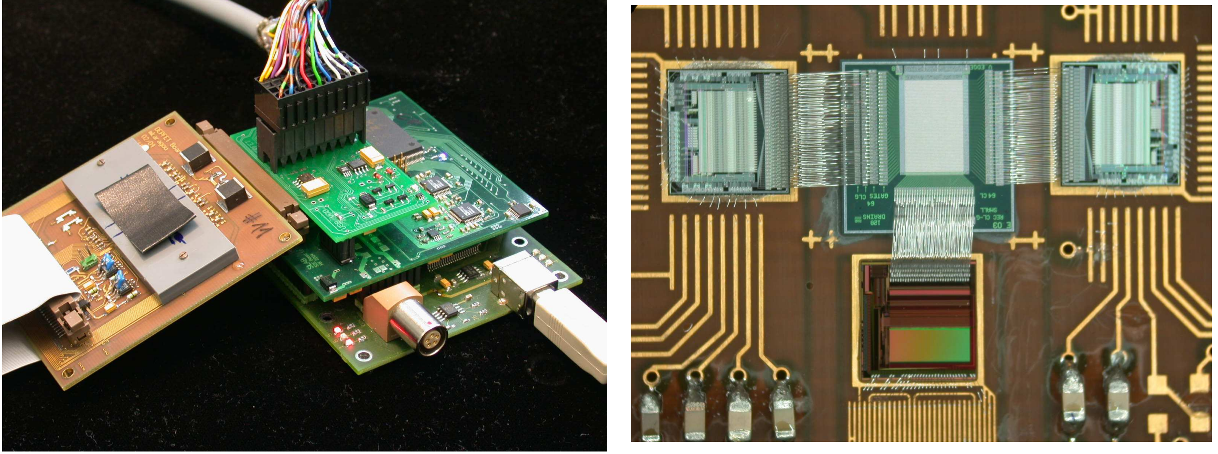

Figure 6.1: Photograph of the ILC DEPFET-System. The sensor matrix on the sensor hybrid and the chip assembly are protected by a plastic cap (left). Micro photograph (area shown ≈ 23x16 mm^2) of the chip arrangement on the sensor hybrid, a 64 × 128 pixel DEPFET-Matrix in the middle, two steering chips SWITCHER II at the side and the readout chip CURO II at the bottom (right).

is 450 μm thick.[1] As described in section 2.6, the matrix is arranged in double pixels of 57 × 36 μm^2 leading to an effective pixel size of 28.5 × 36 μm^2. As a sensor matrix without highE is used, a clear performance not as good as for matrices with highE is expected [32]. Therefore, an operation using a pulsed cleargate voltage, see section 2.3, is chosen to improve the clear efficiency. Due to the additional steering signal introduced by the pulsed cleargate, a second SWITCHER II chip becomes necessary. Matrices operated with static cleargate need only a single steering chip.

If not mentioned otherwise, the DEPFET matrix is operated using the parameters listed in table 6.1.

gate on	-1.9 V	*cleargate on*	5 V
gate off	6.5 V	*cleargate off*	0 V
clear on	16.5 V	*source*	7 V
clear off	2.5 V	*bulk*	2 V
backplane	-170 V		

Table 6.1: Operating parameters of the DEPFET matrix.

[1]The thinning process of the wafer substrate, described in section 5.2 has not been adapted to a DEPFET pixel production yet.

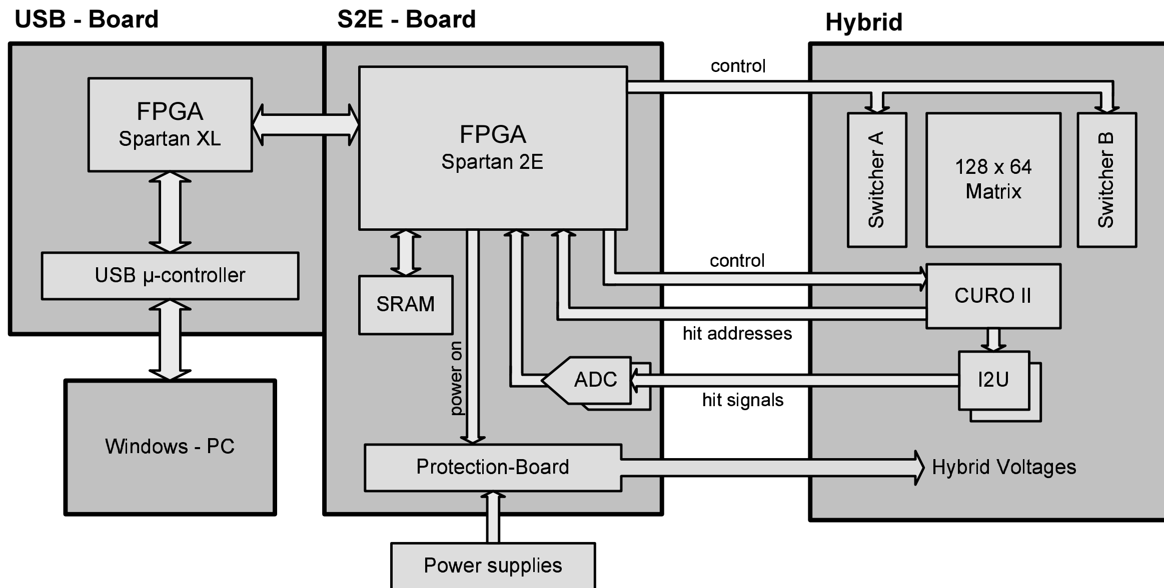

Figure 6.2: Schematic overview of the ILC DEPFET-System.

6.2 Readout sequence

The timing scheme for the readout of a single matrix row is shown in Fig. 6.3. The processing time for a row cycle consisting of two samples with the clear in between is ΔT=1.1 μs. This readout time corresponds to a row rate of 0.9 MHz. Although all

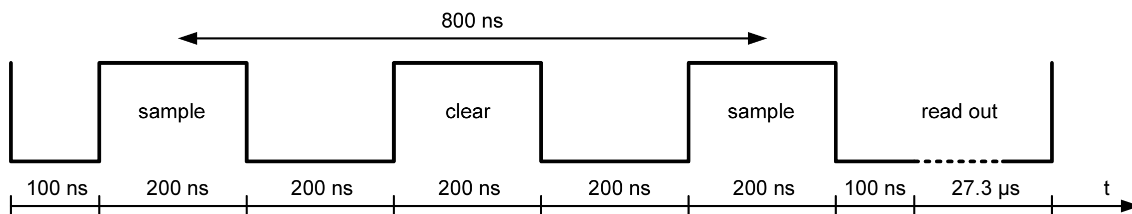

Figure 6.3: Timing scheme for the readout of a matrix row without zero suppression. For all pixels of a row, the two samples with the clear in between are taken in parallel. Afterwards, all pixels of the row are multiplexed to the ADCs.

components of the system are able to operate at much higher row rates, the timing between these components has not been optimized yet, so that a slower readout was chosen.

During the measurements the zero suppression option has not been used. Hence, every pixel of the matrix is read out. To establish the readout without zero suppression, the hitscanner, see sections 3.6 and 4.5, is loaded with a testpattern showing a hit in every pixel. In this readout mode each half of the matrix is read out by one transimpedance amplifier and one ADC. Although the time to process a matrix row is only 1.1 μs, a much longer time of 27.3 μs is needed to multiplex every pixel of the row to the DAQ system

due to the non zero suppressed readout. Hence, the resulting frame rate is 1.8 ms.

The non zero-suppressed readout allows to perform a common mode correction for which the signals of all pixels of a row are used. The significant noise reduction due to common mode correction is presented in section 6.5. It would be advantageous to integrate the common mode correction in the readout chip. Hence, common mode correction would be possible for a zero suppressed readout as well. Therefore, such an addition will be implemented in the next chip generation.

The frame repetition rate for a continuous readout is limited to 10 Hz because the frame data is transfered to the PC via the slow USB 1.1 protocol. To avoid a saturated internal gate due to leakage current, the readout sequence is comprised of two consecutive matrix frames, where the first one is used to clear the matrix and only the second one is acquired.

6.3 System calibration

To calibrate the system gain of the entire readout chain (CURO chip, transimpedance amplifier and ADC) an internal test current source, implemented in each channel of the CURO chip is used. The pedestal current is provided by the DEPFET matrix which is operated using the sequence described in section 6.2. The signal current is provided by the test current source and can be varied. To eliminate any signal current from the DEPFET matrix, permanent clear is applied to the whole matrix by setting both clear voltages (*clear on* and *clear off*) to 16.5 V. Both *cleargate* voltages are set to 5 V. Figure 6.4 shows the system response in units of the ADC as a function of the signal current. A common mode correction, as described in section 6.5 has been performed. A

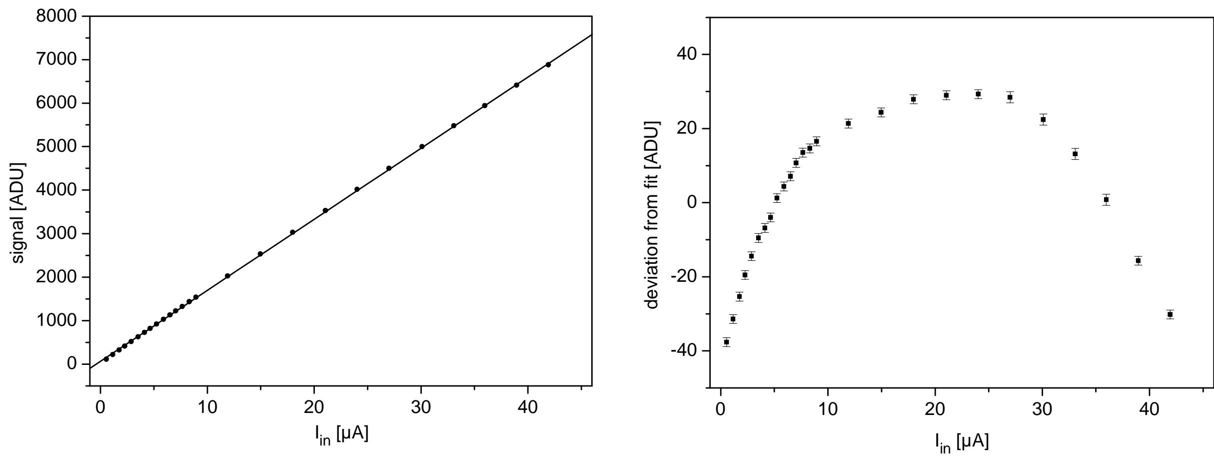

Figure 6.4: System calibration of the complete readout chain (CURO, transimpedance amplifier and ADC) for channel 23. The DEPFET pixel matrix provides the pedestal current. The internal current source of the chip is used for calibration. The system response (left) and the deviation from a linear fit (right) is shown.

linear fit yields a system gain of

$$\text{gain} = 169.8 \pm 0.3\,\frac{\text{ADU}}{\mu\text{A}} \tag{6.1}$$

and an offset of 26 ± 2 ADU. The integral-non-linearity is INL=0.5 % for a dynamic range of 45 μA, using the definition of the INL from equation (4.1). For the subsequent measurements the gain will be used to convert the system response given in ADU into an input current.

6.4 Leakage current

Before the noise performance of the system will be discussed, a measurement to determine the leakage current of the DEPFET matrix will be presented. During the integration time of the system, leakage current in the sensor generates an offset to the signal. The statistical variation of the leakage current causes an additional noise contribution, see section 5.5.

The leakage current of the DEPFET matrix has been measured by observing the system pedestal as a function of the integration time after a clearpulse has been applied. The longer the integration time, the more charge is accumulated in the internal gate due to leakage current. Hence, the system pedestals are shifted.

Since leakage current is temperature-dependent, the temperature has been monitored during the measurement. The temperature was 25 °C and has been measured close to the hybrid. It is therefore possible that the sensor matrix itself has a much higher temperature. However, the system has been operated for at least an hour before the measurement has been performed. It is therefore assumed that the sensor temperature was stable.

The result of the measurement is shown in Fig. 6.5 for integration times from 1.8 ms to 8.6 ms. The system pedestal in ADU has been converted into charge in the internal gate according to the system gain from equation (6.1) and the internal DEPFET amplification $g_q = 282.6 \pm 3.3\,\text{pA/e}^-$. Only the slope of the graph is significant since the baseline right after the clear pulse (integration time equal to zero) is not subtracted. A linear fit to the data yields a leakage current of $I_{Leak} = 178 \pm 14$ fA per pixel. With a pixel size of $28.5 \times 36\,\mu\text{m}^2$ this number translates into $I_{Leak} = 17.4 \pm 1.4\,\text{nA/cm}^2$.

6.5 Noise Performance

In this section the noise performance of the system will be determined and compared with the expected noise figure. To improve the noise performance, a common mode correction is performed. Common mode correction cancels correlated signal variations in several pixels. Due to the row wise operation of the ILC DEPFET-System, all pixels

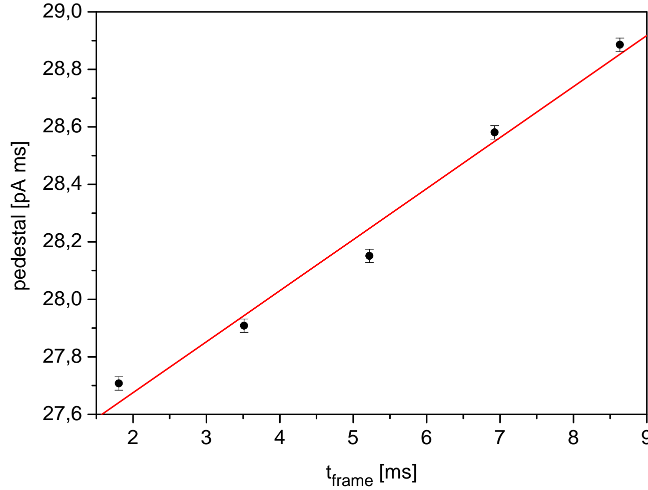

Figure 6.5: Measurement of the leakage current per pixel in a DEPFET sensor matrix. The system pedestal converted to charge in the internal gate is plotted as a function of the integration time. The measurement has been performed at room temperature.

of a row are processed in parallel and the common mode correction is very effective if applied to each row. For example, interferences on the gate voltage of the matrix transistors are thereby canceled. To apply a common mode correction, the mean value (common mode) is computed using the pedestals of all pixels of a row[2] and is subtracted from each pixel afterwards.

Due to the different readout chains (transimpedance amplifier and ADC) that are used for the readout of both matrix halves, the system pedestals for both parts are different. Therefore, the common mode correction is done for each matrix half (column 1-64 and column 65-128) separately. In Fig. 6.6 (left) the system pedestals, itemized for each column averaged over all rows are shown. An offset between both readout chains of about 230 ADU is observed. After the common mode correction, applied to both matrix halves separately, the pedestals are well distributed around zero, as shown in Fig. 6.6 (right). The response behavior of column 127 is anomalous. It is assumed that the column is defective. The column is therefore excluded from the succeeding analysis.

In Fig. 6.7 the observed noise, itemized for each matrix column averaged over all rows is shown before and after common mode correction. The common mode correction reduces the noise significantly from ~ 40 ADU to ~ 13 ADU.

Using the system gain from equation (6.1) and the internal DEPFET amplification $g_q = 282.6 \pm 3.3\,\mathrm{pA/e^-}$, the noise of 12.9 ± 0.08 ADU after common mode correction translates into $\mathrm{ENC} = 268.8 \pm 3.6\,\mathrm{e^-}$. According to the calculation presented in section 5.5 an ENC of about $162\,\mathrm{e^-}$ is expected. However, the matrix is read out more slowly than at the ILC timing scheme, assumed in section 5.5. The difference between both readout sequences is:

[2]Pixel showing a signal are excluded from the common mode computation.

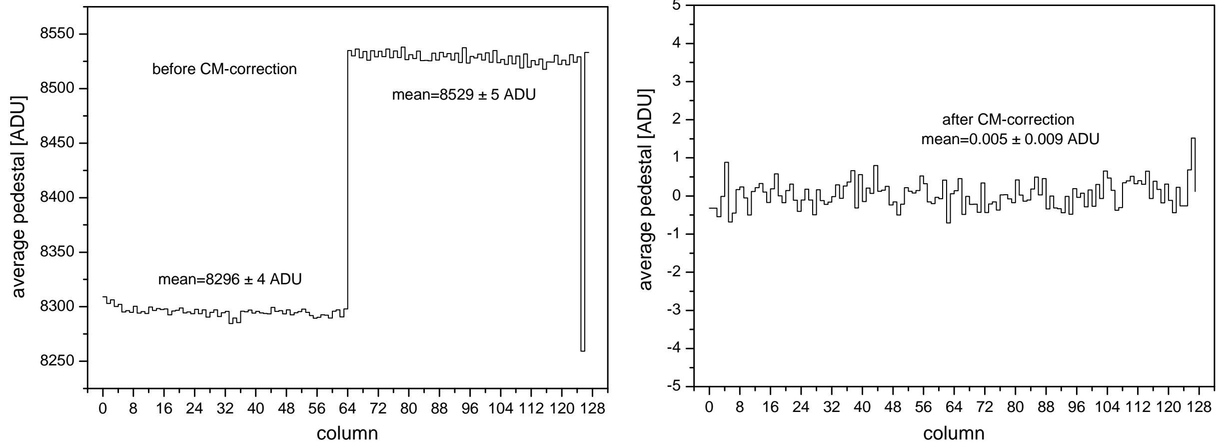

Figure 6.6: System pedestals before (left) and after (right) common mode correction (CM) for each matrix column averaged over all rows. The two matrix halves are readout by separate readout chains.

- The frame time is 1.8 ms, not 50 μs.
- The time interval between the two measurements is 800 ns, not 50 ns.

Consequently, 1/f noise after CDS and shot noise due to leakage current will be higher, which both increase with sampling time and integration time, respectively. Their noise contributions for the slower readout are:

- Due to the longer integration time, the leakage current will contribute with $\mathrm{ENC_{shot}} \approx 45\,\mathrm{e^-}$ instead of $8\,\mathrm{e^-}$.
- The longer sampling interval leads to an increased 1/f noise of $\mathrm{ENC_{1/f}} \approx 2.1\,\mathrm{e^-}$ which can be neglected here.

Furthermore, the used external transimpedance amplifier causes an additional noise of $\mathrm{i_{RMS}} = 26.5\,\mathrm{nA}$ [69]. This number translates into $\mathrm{ENC_{I2U}} \approx 94\,\mathrm{e^-}$ using the internal amplification of $\mathrm{g_q} \approx 283\,\mathrm{pA/e^-}$. A current mode ADC implemented in future generations of the readout chip avoids the signal conversion and will eliminate this noise contribution. Considering all additional noise sources leads to a total expected noise of $\mathrm{ENC_{total}} \approx 192\,\mathrm{e^-}$ for the present setup. Compared to the observed noise of $\mathrm{ENC} = 268.8 \pm 3.6\,\mathrm{e^-}$, a significant noise contribution of about $188\,\mathrm{e^-}$ is still not accounted for.

Due to the maximum clear voltages that can be applied to the matrix, it is very likely that the matrix without highE cannot be cleared completely. The *clear on* voltage is limited by the grounding scheme of the system and cannot be chosen higher than 17 V. Measurements in [32] that have been performed using a 4×8 pixel matrix with a similar design, showed a very incomplete clear for the chosen clear voltages. Unfortunately, an exact small counterpart of the 64×128 pixel matrix was not available and has

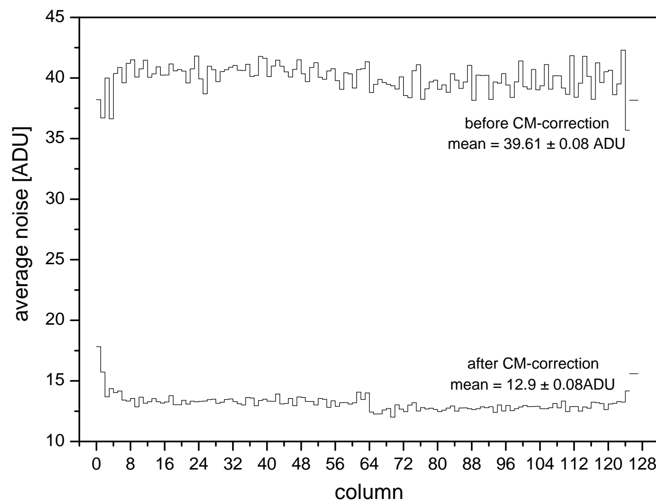

Figure 6.7: Noise before and after common mode correction (CM) for each matrix column averaged over all rows. Column 127 has been excluded.

therefore not been analyzed according to the clear efficiency. Due to the incomplete clear, additional clear noise will contribute. Furthermore, the influence of an incomplete clear contributes twice (see the readout sequence in section 6.2). The first time, when the matrix is cleared before the frame is taken, and the second time in the acquisition frame itself. To quantify the clear noise contribution, detailed measurements on the clear efficiency of this matrix are needed. However, complete clear has already been demonstrated for different matrices, mostly with highE implantation [32]. The ILC DEPFET-System should therefore be operated with a matrix offering complete clear. It can also not be excluded that pick-up noise degrades the noise performance further and that the shielding of the setup was insufficient.

Although the theoretical noise limit has not been achieved yet, the present noise figure already translates into a signal to noise ratio of S/N $\approx$ 120 for MIP detection with the 450 μm thick matrix.[3].

6.6 Measurements using X-rays

The system has been used for the detection of X-rays in an energy range from 5.9 keV (^{55}Fe) up to 59.6 keV (^{241}Am) using different radioactive sources. The dominant X-ray-energies of the used radioactive sources are listed in table 6.2. The spectra for Rubidium to Terbium were provided using a variable X-ray source. This source consists of an ^{241}Am primary source and variable metal foils. The ^{241}Am source illuminates one of the selected metal foils which fluoresce the characteristic X-ray spectrum of the foil.

To perform an energy calibration of the DEPFET sensor, the system response for the different X-rays is observed. Before the energy calibration is presented, the energy

[3]The proposed sensor thickness for the ILC vertex detector is 50 μm.

source	abbreviation	E_γ [keV]
Iron	^{55}Fe	5.9
Rubidium	Rb	13.37
Molybdenum	Mo	17.44
Silver	Ag	22.1
Barium	Ba	32.06
Terbium	Tb	44.23
Cadmium	^{109}Cd	22.1
Americium	^{241}Am	59.6

Table 6.2: Radioactive sources and the emitted dominant X-ray-energies. A variable X-ray source provided the spectra for (Rb) to (Tb).

spectrum of an ^{241}Am source is discussed as an example for all other spectra.

^{241}Am spectrum

The energy spectrum of the ^{241}Am-source is shown in Figure 6.8. After performing a

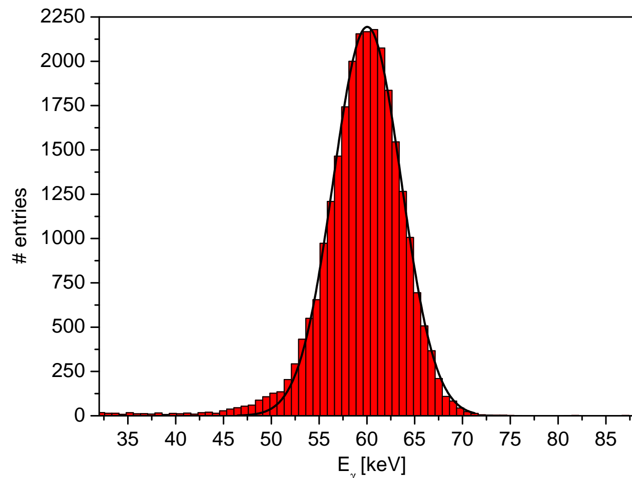

Figure 6.8: Energy spectrum for clusters consisting of 4 pixels from an ^{241}Am-source taken with the ILC DEPFET-System.

row wise common mode correction, clusters are reconstructed by identifying neighboring pixels, where every pixel contains a signal higher than five times its noise. For the energy conversion, the system calibration from equation (6.1) and an internal DEPFET amplification of $g_q = 282.6 \pm 3.3\,\mathrm{pA/e^-}$ is used. Fitting a Gaussian distribution to the energy peak for 4-pixel-clusters yields $E_\gamma = 60.0 \pm 0.3\,\mathrm{keV}$, in good agreement with the expected value of 59.6 keV.

The width of the 60 keV peak is $\sigma = 972 \pm 83\,\mathrm{e^-}$. Since the clusters consist of four pixels, this results to a noise of $\sigma = 486 \pm 42\,\mathrm{e^-}$ per pixel . The observed noise from the energy

peak does not correspond to the noise of $268.8 \pm 3.6\,e^-$ obtained from the noise peak in section 6.5. The fano noise at 60 keV is about $40\,e^-$ and can be neglected here. It is very likely that the wider energy peak is due to gain variations in the matrix. Since a global sensor amplification g_q has been used for the entire matrix, pixel-to-pixel variations are not considered. To compensate for this effect, gain calibration of every pixel is needed. This has not been done due to the low statistics in every pixel. Furthermore, the energy spectrum has not been taken to demonstrate the spectroscopic performance of the system.

Internal amplification and linearity

As for the ^{241}Am source, energy spectra have been taken for Rubidium (Rb), Molybdenum (Mo), Silver (Ag), Cadmium (Cd), Barium (Ba) and Terbium (Tb) to determine the internal amplification of the DEPFET matrix and the linearity of the entire system. In Fig. 6.9 the mean signal, obtained by a Gaussian fit to the spectrum peak is plotted as a function of the X-ray-energy of the different radioactive sources. Within the errors of

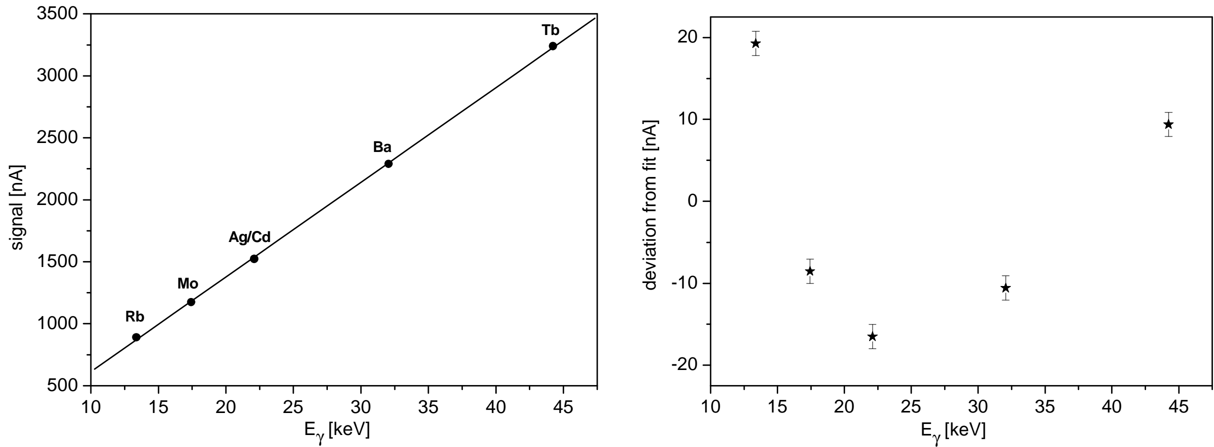

Figure 6.9: Linearity of the ILC DEPFET-System. The sensor response is plotted for different radioactive sources (left) and the deviation from a linear fit is shown (right).

the measurement, the Cadmium (Cd) and the Silver (Ag) source, both emitting 22.1 keV X-rays obtained the same results. To convert the system response in ADUs to an input current the system calibration from equation (6.1) has been used.

A linear fit to the data yields an internal amplification of the DEPFET sensor of

$$g_q = 282.6 \pm 3.3\,\mathrm{pA/e^-} \tag{6.2}$$

The observed amplification is significantly below the simulated value of about $400\,\mathrm{pA/e^-}$, presented in section 2.2. Recent measurements reported in [32] have shown that the charge collection efficiency strongly depends on the clear and cleargate potential. It is

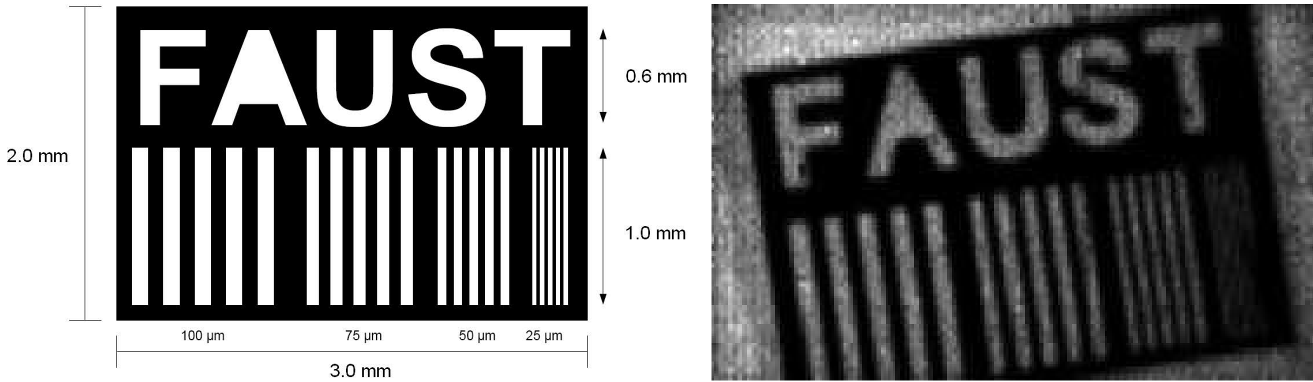

Figure 6.10: Sketch of a 75 μm thick tungsten test chart (left). ^{55}Fe-radiogram of the $2 \times 3\,\mathrm{mm}^2$ test chart taken with the ILC DEPFET-System (right).

therefore possible that for the chosen clear and cleargate parameters the charge collection is incomplete. In case of an incomplete charge collection, the obtained internal amplification is reduced. A systematic analysis of the charge collection efficiency with respect to the operating parameters is therefore needed to find an optimal internal amplification.

The integral-non-linearity of the system is better than INL=0.8 % for a dynamic range of about 8500 e^-. In a 50 μm thin sensor device aimed for the ILC, this dynamic range is large enough for the detection of about two MIPs. The non-linearity is surprisingly good. On the one hand, a quadratic dependence of the transistor current with respect to the potential of the internal gate is expected, due to the JFET character of the pn-junction formed by internal gate and the transistor channel. On the other hand, the more charge is accumulated in the internal gate, the weaker the coupling of the charge to the transistor channel is expected to be [31]. Hence, a non-constant amplification depending on the accumulated charge in the internal gate has to be considered. Both effects seem to partly compensate each other, leading to a highly linear dependence of the observed dynamic range.

^{55}Fe-radiogram

The capability of spatial detection of X-rays with the system has been demonstrated using a 75 μm thick tungsten test chart with an engraved logo and several line structures. A sketch of the $2 \times 3\,\mathrm{mm}^2$ test chart is shown in Fig. 6.10 (left). The line structures have a pitch of 100, 75, 50 and 25 μm, from left to right, respectively. A radiogram of the test chart is shown in Fig. 6.10 (right). It has been taken by placing the test chart on the backside of the detector and irradiating the system with an ^{55}Fe-source. The radiogram has been obtained by summing the pulse heights for pixels that contain a signal higher than five times their noise. For the radiogram, $2 \cdot 10^5$ frames have been accumulated. Although no spatial reconstruction techniques, such as center of gravity or η-function have been used to improve the spatial resolution, the 50 μm lines in the radiogram are clearly visible.

6.7 Summary of the ILC DEPFET-System

A prototype system for the operation of a 64×128 DEPFET pixel matrix has been developed as an intermediate step towards a full size ladder for the ILC vertex detector. The system uses the SWITCHER II chip to provide the matrix steering signals and the CURO II chip for readout. For the first time, a 64×128 DEPFET pixel matrix from the dedicated ILC sensor production has been successfully operated. In the system a matrix without highE implantation, with pulsed cleargate and a pixel size of $28.5 \times 36\,\mu\text{m}^2$ has been used.

The system was operated at a reduced row rate of about 1 MHz so that timing between the components (SWITCHER, matrix, CURO) is not crucial. The single components of the system are capable of much higher row rates. In the future, the overall system speed needs to be increased to meet a row rate of 20 MHz or more as required for the ILC operation.

The noise performance achieved with the system is ENC=$268.8 \pm 3.6\,\text{e}^-$ after common mode correction. Based on the calculations presented in section 5.5, a total noise of ENC=$192\,\text{e}^-$ is expected, taking the slower readout mode and an additional noise contribution from the transimpedance amplifier into account. Due to limitations on the provided clear voltages, it is most likely that for this matrix without highE complete clear cannot be achieved. Hence, an additional noise due to incomplete clear has to be considered. Furthermore, it cannot be excluded that pick-up noise deteriorates the noise performance and that the shielding of the system may need improvements. Using this prototype system with a $450\,\mu$m thick sensor for MIP detection, the achieved noise performance corresponds to a signal to noise ratio of S/N $\approx$ 120.

The spatial X-ray detection capability of the DEPFET pixel matrix has been demonstrated by taking a radiogram of a $75\,\mu$m thick tungsten test chart irradiated with an ^{55}Fe-source. Using different X-rays in an energy range from 13 to 45 keV, the internal amplification of the DEPFET has been determined to $\text{g}_\text{q} = 282.6 \pm 3.3\,\text{pA/e}^-$. The observed integral-non-linearity of the system is better than 0.8 % for a dynamic range of about $8500\,\text{e}^-$.

After the successful operation of the system, detailed measurements on the clear performance and the charge collection efficiency with respect to the operating parameters are needed.

Summary and Outlook

The DEPFET pixel concept is a proposed technology for the vertex detector at the International Linear Collider (ILC). The DEPFET detector combines in-pixel amplification with particle detection by integrating a field-effect-transistor in a fully depleted silicon sensor. Due to the integrated amplification stage, the detector offers an excellent noise performance. Charge generation and collection is provided by the entire, fully depleted detector substrate. For the ILC vertex detector, the DEPFET detector offers the possibility to fabricate 50 μm thick sensor devices which still offer an excellent signal to noise ratio.

The proposed baseline design of the DEPFET pixel based vertex detector consists of five barrel layers arranged cylindrically around the beam pipe. To achieve an outstanding impact parameter resolution the innermost layer of the vertex detector is placed very close to the interaction point at a radius of 15 mm. Furthermore, the material budget per detector layer should not exceed 0.1 % of a radiation length to reduce multiple scattering effects. To achieve minimum material, the sensor is thinned down to 50 μm and no active cooling is foreseen. A row wise operation of the detector modules is proposed. Hence, power consumption is minimized and steering and readout components are placed at the boundary of the matrix. To achieve an adequate detector occupancy of about 1 %, the whole vertex detector needs to be read out in 50 μs. For a row wise operation, this number translates into a required row rate of 20 MHz.

For the fast readout of a DEPFET pixel matrix, a 128 channel readout chip, CURO II, has been designed and fabricated. The chip uses novel, current mode signal processing, perfectly adapted to the current signal of the DEPFET detector. Pedestal subtraction and correlated double sampling are performed by fast current memory cells in the chip. Zero-suppression is done by an on-chip hitscanner arranged in parallel. In standalone tests, the analog part of the chip has been successfully operated at a row rate of 24 MHz, faster than the row rate of 20 MHz required for the ILC. The digital part of the chip has been successfully tested up to 110 MHz. With the capability of finding two hits per clock cycle, the digital performance of the chip outperforms the occupancy expected at the innermost layer of the vertex detector by more than a factor of five.

A prototype system for the readout of a 64×128 DEPFET pixel matrix has been developed. The system uses the CURO II chip for matrix readout and additional chips, SWITCHER II, to provide the matrix steering. For the first time, a 64×128 DEPFET pixel matrix has been successfully operated with the system. The system was operated

at a row rate of about 1 MHz as the timing between the components has not yet been optimized. The functionality of the system has been demonstrated using different radioactive sources in an energy range from 6 keV to 60 keV. The internal amplification of the matrix has been determined to $g_q = 282.6 \pm 3.3\,\mathrm{pA/e^-}$. The system shows an integral-non-linearity of 0.8 % for a dynamic range of 8500 e^-. The noise performance achieved with the system is ENC=$268.8 \pm 3.6\,e^-$. Converting this performance into MIP detection, a signal to noise ratio of S/N=120 is expected for the present sensors being 450 μm thick.

After the successful operation of the ILC DEPFET-System in the laboratory, test beam experiments are in preparation. Detailed studies concerning the tracking efficiency and the spatial resolution of the device for MIP detection are necessary to demonstrate the feasibility of the DEPFET technology for the ILC.

In the near future, the system needs to meet the row rate of 20 MHz required at the ILC. The single components of the system already show a compatible performance.

Towards a full scale demonstrator for the ILC vertex detector, new versions of the steering and the readout chip will be produced. A crucial addition of the present chips is a fast power down feature to enable a pulsed operation. Adapting the chip operation to the duty cycle of the accelerator (1:199), reduces the power consumption significantly. Furthermore, the present CURO chip has been designed for the readout of a small 64×128 pixel matrix. For the readout of large scale matrices with a higher capacitive load, the input stage realized by a regulated cascode will be improved. Concerning the steering chip, SWITCHER, a more radiation tolerant design than the present one using transistors with thick gate oxide is needed.

Larger DEPFET matrices with up to 512×1024 pixels are designed. By reducing the gate length of the amplifying transistor in the pixel, an improved internal amplification is obtained. Simulations have shown that new pixel generations designed at the technological limit enhance the internal amplification by a factor of three. This will improve the signal to noise performance of the system even further. The fabrication of 50 μm thin detectors is in progress. With the improved internal amplification, these thin devices will provide a signal to noise ratio of S/N=40.

A Correlated Double Sampling

Correlated Double Sampling (CDS) is a technique originally implemented for the readout of CCDs [70]. In the mean time, CDS has become a common technique exploited by almost all integrating imaging sensors. In the case of CDS the output signal of a system, e.g. a sensor, is sampled at two different times. One time, to measure the signal itself and one time, to determine the baseline of the system after it has been reset. By subtracting both values all correlated contributions to the signal will be canceled. Hence, baseline variations (spatial and temporal) are suppressed and a significant improvement of the noise performance is achieved. In [66] the effect of CDS on 1/f noise is treated in the time domain. In this chapter, the influence of CDS on the different noise sources of a sensor, thermal noise, 1/f noise as well as shot noise due to leakage current, will be discussed in the frequency domain. In section 5.5 the results of this chapter will be used to determine the total noise contribution of a DEPFET sensor read out by the CURO readout chip.

A.1 Weighting function for correlated double sampling

In this section the influence of a CDS process on a periodic signal with the frequency ω will be analyzed. In the frequency domain the transfer function of CDS with two samples taken at the times t and $t+\tau$ is given by the z-transformation [71]

$$H^{CDS}(\omega) = 1 - e^{-i\omega\tau} \tag{A.1}$$

leading to the squared modulus transfer function of CDS

$$\left|H^{CDS}(w)\right|^2 = 2 \cdot (1 - \cos(\omega\tau)) = 2 \cdot W^{CDS}(\omega) \tag{A.2}$$

The term $W^{CDS}(\omega) = 1 - \cos(\omega\tau)$ in equation (A.2) has the meaning of a weighting function and describes how much an input signal with the frequency ω contributes to the output after CDS with a relative time interval of τ is performed. The weighting function $W^{CDS}(\omega)$ is shown in Fig. A.1. Signals with frequencies ω_0 corresponding to multiples of the inverse sampling interval τ

$$\omega_0 = n \cdot 2\pi \cdot \frac{1}{\tau} \tag{A.3}$$

are canceled completely, whereas signals with intermediate frequencies are even intensified by up to a factor of two. Although CDS offers an effective suppression of low

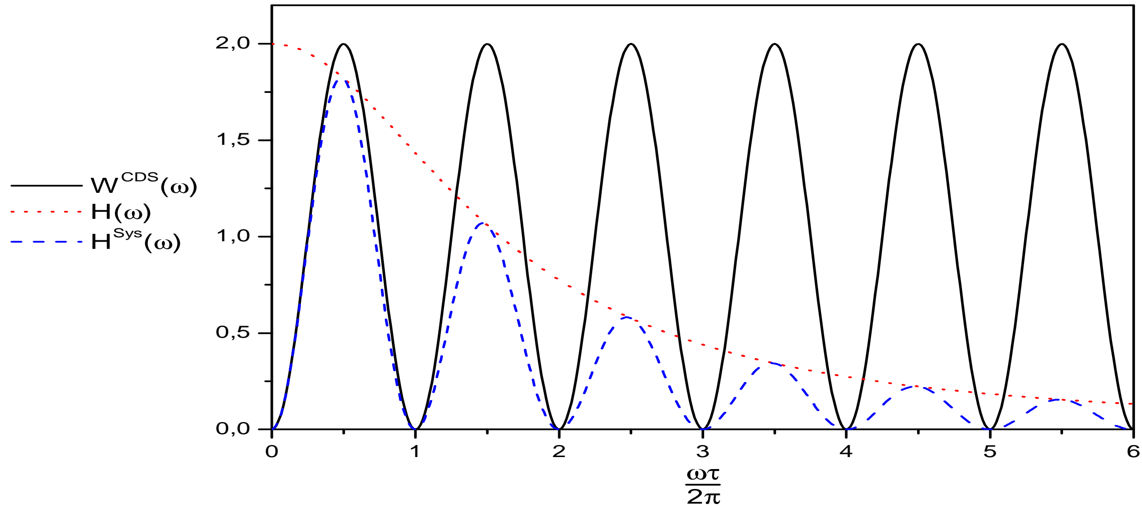

Figure A.1: Weighting function for the correlated double sampling process $W^{CDS}(\omega)$. Transfer function of a CDS system additionally filtered by a single pole low-pass filter $H^{Sys}(\omega)$. The transfer function of the low-pass filter is illustrated by $H(\omega)$.

frequency contributions, it is not limiting the bandwidth due to the periodical extend of the weighting function to infinity. To achieve a finite noise figure an additional low-pass filter is needed. The low-pass filter is usually given by the limited bandwidth of the succeeding system. In Fig. A.1, a first order low-pass filter is illustrated by $H(\omega)$. The total transfer characteristic comprising of CDS and low pass filter is given by $H^{Sys}(\omega)$.

A.2 Influence of CDS on the system noise

To analyze the influence of correlated double sampling on the different noise sources, a system shown in Fig. A.2 is considered. The noise sources are modeled by a total power

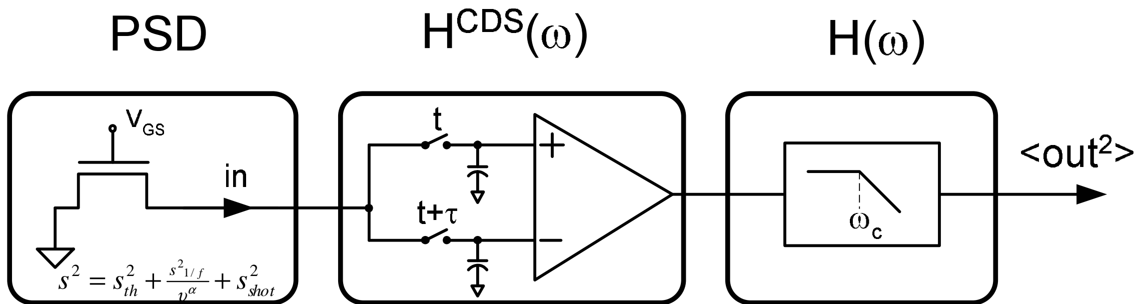

Figure A.2: Principle setup of a system performing correlated double sampling. The input is determined by a total power spectral density (PSD) comprising thermal, 1/f and shot noise. The CDS process is described by $H^{CDS}(\omega)$ and the transfer function of the system is described by $H(\omega)$.

spectral density function (PSD)

$$s^2 = s_{\mathrm{th}}^2 + \frac{s_{\mathrm{1/f}}^2}{\nu^\alpha} + s_{\mathrm{shot}}^2 \tag{A.4}$$

comprising thermal noise s_{th}^2, 1/f noise $s_{\mathrm{1/f}}^2$ and shot noise s_{shot}^2 contributions. The correlated double sampling performed by the system is described by the transfer function $\mathrm{H}^{\mathrm{CDS}}(\omega)$, and the frequency behavior of the remaining system is given by the transfer function $\mathrm{H}(\omega)$.

CDS and thermal noise

In case of thermal noise the mean square value of the output signal after CDS is given by

$$\left\langle \mathrm{out}^2 \right\rangle_{\mathrm{th}} = \int_0^\infty s_{\mathrm{th}}^2 \cdot \left| H^{CDS}(w) \right|^2 \cdot \left| H(w) \right|^2 d\nu \tag{A.5}$$

with a white (frequency independent) power spectral density s_{th}^2 and the transfer function for CDS from equation (A.2). Using a first order low-pass filter characterized by the transfer function

$$\left| H(w) \right|^2 = \frac{1}{1 + \left(\frac{\omega}{\omega_{\mathrm{c}}} \right)^2} \tag{A.6}$$

with the cut-off frequency ω_{c} and integrating over all frequencies yields

$$\left\langle \mathrm{out}^2 \right\rangle_{\mathrm{th}} = s_{\mathrm{th}}^2 \cdot \frac{\omega_{\mathrm{c}}}{2} \cdot \left(1 - e^{-\omega_{\mathrm{c}} \cdot \tau} \right) \tag{A.7}$$

The output noise shows a linear dependence on the cut-off frequency ω_{c}, as it is the case for thermal noise without CDS. To observe the influence of CDS on thermal noise, the mean square output value normalized to s_{th}^2 and the cut-off frequency ν_{c} is plotted as a function of $\omega_{\mathrm{c}}\tau$ in Fig. A.3. For sampling intervals much longer than the characteristic response time of the system $\tau_{\mathrm{c}} = \frac{2\pi}{\omega_{\mathrm{c}}}$, the output noise becomes a constant value that is equal to the noise that would be achieved without CDS. For sampling intervals much shorter than the response time, the noise decreases. On the other hand, the signal response of the system degrades in the same way for shorter sampling intervals due to the limited bandwidth given by the low pass transfer function. The signal to noise ratio for all parameters therefore remains constant and the thermal noise performance is not affected by CDS.

CDS and 1/f noise

In case of a 1/f like input noise spectrum the mean square value of the output signal after CDS is given by

$$\left\langle \mathrm{out}^2 \right\rangle_{1/\mathrm{f}} = \int\limits_0^\infty \frac{s_{1/\mathrm{f}}^2}{\nu^\alpha} \cdot \left| H^{CDS}(w) \right|^2 \cdot \left| H(w) \right|^2 d\nu \tag{A.8}$$

Using the single pole transfer function from equation (A.6) and substituting $x = \frac{\omega}{\omega_\mathrm{c}}$ yields

$$\left\langle \mathrm{out}^2 \right\rangle_{1/\mathrm{f}} = 2 \cdot s_{1/\mathrm{f}}^2 \cdot \left(\frac{2\pi}{\omega_\mathrm{c}} \right)^{\alpha - 1} \int\limits_0^\infty \frac{1 - \cos(k \cdot x)}{x^\alpha (1 + x^2)} \, dx \tag{A.9}$$

with $k = \omega_\mathrm{c} \cdot \tau$. The integral in equation (A.9) can only be solved numerically. To compare 1/f noise with thermal noise contribution, the mean square value from equation (A.9) is normalized to $s_{1/\mathrm{f}}^2$ and is plotted in Fig. A.3 for $\alpha = 1$ as a function of $\omega_\mathrm{c}\tau$. For a pure 1/f noise spectrum ($\alpha = 1$), the output noise depends only on the product of

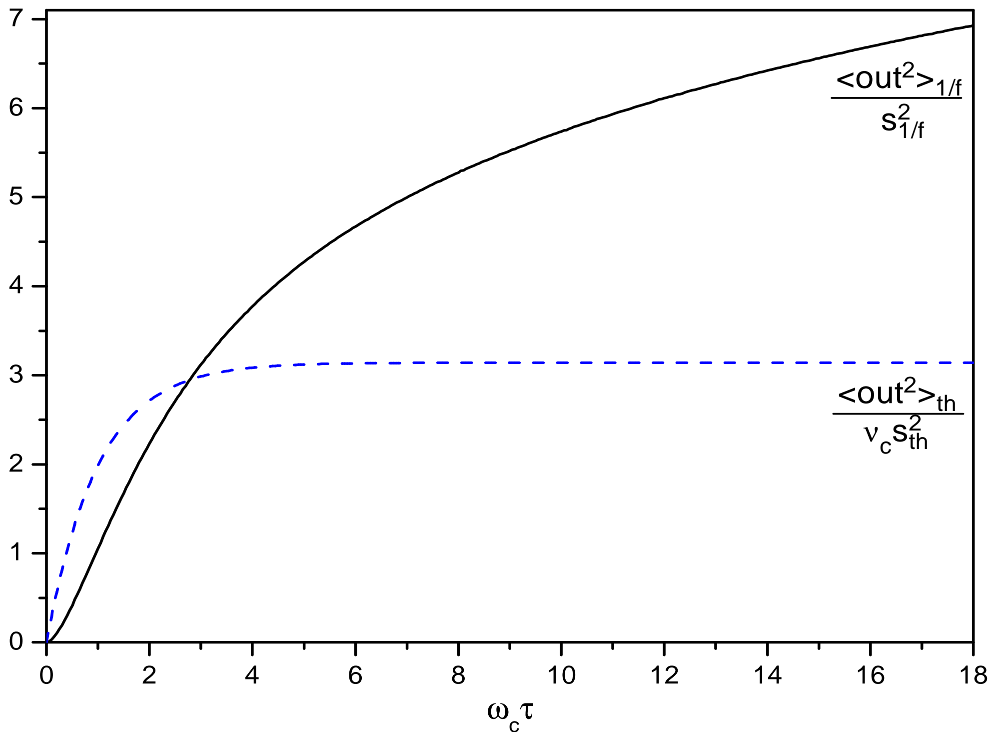

Figure A.3: Normalized output noise contribution of thermal and 1/f-noise as a function of $\omega_\mathrm{c}\tau$, where ω_c is the cut-off frequency of the low-pass filter and τ is the CDS sampling interval.

$\omega_\mathrm{c}\tau$ and not explicitly on the cut-off frequency ω_c, as thermal noise does. Hence, a high bandwidth does not necessarily deteriorate the 1/f noise performance, as long as the

chosen sampling interval τ corresponds to the bandwidth ω_c of the circuit. Operating a circuit at slower sampling intervals than given by the bandwidth, on the other hand, will lead to a worse noise performance.

CDS and shot noise due to leakage current

During the integration time of the system, leakage current in the sensor generates an offset to the signal. The statistical variation of the leakage current causes a shot noise contribution. Performing CDS, one of the two samples is taken directly after the system has been reset. Leakage current does therefore not affect the sample after the reset, but only the sample after the integration time τ. As there is no correlation between these two samples, shot noise due to leakage current cannot be suppressed by CDS.

B Noise integrals

To determine the noise figure of a system with an input noise spectrum filtered by a transfer function $H(\omega)$ the root-mean-square value at the output is calculated. In case of white noise where the power spectral density is a constant (frequency independent), this corresponds to the calculation of the squared modulus of the transfer function integrated over all frequencies (noise integral)

$$\int_0^\infty |H(\omega)|^2 \, d\nu$$

As $|H(\omega)|^2$ is symmetric in ω, the boundaries of the integral can be extended, going from minus infinity to infinity and Cauchy´s theorem can be used. The integrals with the singularities at the poles of the transfer functions will be calculated using the residue theorem. Note, that the number of poles has to be larger than the number of zeros, otherwise the integral does not converge. In the following, the noise integrals of transfer functions with one pole, two poles and two poles with one zero will be analyzed.

B.1 One pole

In case of a transfer function with a single pole ω_1

$$H(\omega) = \frac{1}{1 + i\frac{\omega}{\omega_1}} = \frac{-i\,\omega_1}{\omega - i\,\omega_1} \tag{B.1}$$

the integral over all frequencies becomes

$$\begin{aligned}
\int_0^\infty |H(\omega)|^2 \, d\nu &= \frac{1}{4\pi} \int_{-\infty}^{\infty} H(\omega) H^*(\omega) \, d\omega = \frac{1}{4\pi} \int_{-\infty}^{\infty} \frac{-i\omega_1}{\omega - i\omega_1} \frac{i\omega_1}{\omega + i\omega_1} \, d\omega \\
&= \frac{\omega_1^2}{4\pi} \int_0^\infty \frac{1}{(\omega - i\omega_1)(\omega + i\omega_1)} \, d\omega = \frac{\omega_1^2}{4\pi} \, 2\pi i \, \mathrm{Res}\left[\frac{1}{(\omega - i\omega_1)(\omega + i\omega_1)} \, ; \, i\omega_1\right] \\
&= \frac{\omega_1}{4}
\end{aligned} \tag{B.2}$$

B.2 Two poles

In case of a two pole transfer function with the two poles ω_1 and ω_2

$$\begin{aligned} H(\omega) &= \frac{1}{\left(1+i\frac{\omega}{\omega_1}\right)\left(1+i\frac{\omega}{\omega_2}\right)} \qquad \text{(B.3)} \\ &= \frac{1}{1+i\omega A-\omega^2 B} \quad \text{with} \quad A=\frac{\omega_1+\omega_2}{\omega_1\omega_2}, \quad B=\frac{1}{\omega_1\omega_2} \\ &= \frac{-\omega_1\omega_2}{(\omega-i\omega_1)(\omega-i\omega_2)} \end{aligned}$$

the integral over all frequencies becomes

$$\begin{aligned} \int_0^\infty |H(\omega)|^2\,d\nu &= \frac{1}{4\pi}\int_{-\infty}^{\infty}\frac{-\omega_1\omega_2}{(\omega-i\omega_1)(\omega-i\omega_2)}\frac{-\omega_1\omega_2}{(\omega+i\omega_1)(\omega+i\omega_2)}\,d\omega \\ &= \frac{\omega_1^2\omega_2^2}{4\pi}\int_{-\infty}^{\infty}\frac{1}{(\omega-i\omega_1)(\omega-i\omega_2)(\omega+i\omega_1)(\omega+i\omega_2)}\,d\omega \\ &= \frac{\omega_1^2\omega_2^2}{4\pi}\,2\pi i\sum_{\omega_j=\omega_1,\omega_2}\text{Res}\,[F(\omega)\,;\,i\omega_j] \\ \text{with} \qquad F(\omega) &= \frac{1}{(\omega-i\omega_1)(\omega-i\omega_2)(\omega+i\omega_1)(\omega+i\omega_2)} \end{aligned}$$

Calculating the residuals of $F(\omega)$ yields

$$\begin{aligned} \int_0^\infty |H(\omega)|^2 d\nu &= \frac{\omega_1^2\omega_2^2}{4\pi}2\pi i\left(\frac{1}{(i\omega_1-i\omega_2)(i\omega_1+i\omega_1)(i\omega_1+i\omega_2)}+\frac{1}{(i\omega_2-i\omega_1)(i\omega_2+i\omega_1)(i\omega_2+i\omega_2)}\right) \\ &= -\frac{\omega_1^2\omega_2^2}{2}\left(\frac{1}{(\omega_1-\omega_2)\,2\,\omega_2\,(\omega_1+\omega_2)}+\frac{1}{(\omega_2-\omega_1)(\omega_2+\omega_1)\,2\,\omega_2}\right) \\ &= -\frac{\omega_1^2\omega_2^2}{4}\left(\frac{\omega_2}{(\omega_1-\omega_2)\,\omega_1\omega_2\,(\omega_1+\omega_2)}-\frac{\omega_1}{(\omega_1-\omega_2)(\omega_2+\omega_1)\,\omega_2\omega_1}\right) \\ &= \frac{1}{4}\,\frac{\omega_1\omega_2}{\omega_1+\omega_2}=\frac{1}{4A} \qquad \text{(B.4)} \end{aligned}$$

B.3 Two poles and one zero

With a transfer function comprising the two poles ω_1, ω_2 and one zero z_1

$$H(\omega) = \frac{\left(1+i\frac{\omega}{z_1}\right)}{\left(1+i\frac{\omega}{\omega_1}\right)\left(1+i\frac{\omega}{\omega_2}\right)} \qquad \text{(B.5)}$$

$$
\begin{aligned}
&= \frac{1+i\omega C}{1+i\omega A-\omega^2 B} \qquad \text{with} \qquad A=\frac{\omega_1+\omega_2}{\omega_1\omega_2}, \qquad B=\frac{1}{\omega_1\omega_2}, \qquad C=\frac{1}{z_1} \\
&= \frac{-i\omega_1\omega_2}{z_1}\frac{\omega-iz_1}{(\omega-i\omega_1)(\omega-i\omega_2)}
\end{aligned}
$$

the noise integral becomes

$$
\begin{aligned}
\int_0^\infty |H(\omega)|^2\,d\nu &= \frac{1}{4\pi}\frac{\omega_1^2\omega_2^2}{z_1^2}\int_{-\infty}^{\infty}\frac{\omega^2+z_1^2}{(\omega-i\omega_1)(\omega-i\omega_2)(\omega+i\omega_1)(\omega+i\omega_2)}\,d\omega \\
&= \frac{1}{4\pi}\frac{\omega_1^2\omega_2^2}{z_1^2}\,2\pi i\sum_{\omega_j\,=\,\omega_1,\,\omega_2}\text{Res}\;[F(\omega)\,;\,i\omega_j] \\
\text{with} \qquad F(\omega) &= \frac{\omega^2+z_1^2}{(\omega-i\omega_1)(\omega-i\omega_2)(\omega+i\omega_1)(\omega+i\omega_2)}
\end{aligned}
$$

Calculating the residuals of $F(\omega)$ yields

$$
\begin{aligned}
\int_0^\infty |H(\omega)|^2 d\nu &= \frac{\omega_1^2\omega_2^2}{z_1^2}\frac{i}{2}\left(\frac{(i\omega_1)^2+z_1^2}{(i\omega_1-i\omega_2)(i\omega_1+i\omega_1)(i\omega_1+i\omega_2)}+\frac{(i\omega_2)^2+z_1^2}{(i\omega_2-i\omega_1)(i\omega_2+i\omega_1)(i\omega_2+i\omega_2)}\right) \\
&= -\frac{\omega_1^2\omega_2^2}{z_1^2}\frac{1}{2}\left(\frac{z_1^2-\omega_1^2}{(\omega_1-\omega_2)(\omega_1+\omega_1)(\omega_1+\omega_2)}+\frac{z_1^2-\omega_2^2}{(\omega_1-\omega_2)(\omega_2+\omega_1)(\omega_2+\omega_2)}\right) \\
&= -\frac{\omega_1^2\omega_2^2}{z_1^2}\frac{1}{4}\frac{1}{(\omega_1-\omega_2)(\omega_1+\omega_2)}\left(\frac{z_1^2-\omega_1^2}{\omega_1}-\frac{z_1^2-\omega_2^2}{\omega_2}\right) \\
&= -\frac{\omega_1\omega_2}{z_1^2}\frac{1}{4}\frac{1}{(\omega_1-\omega_2)(\omega_1+\omega_2)}\left(z_1^2\omega_2-\omega_1^2\omega_2-z_1^2\omega_1+\omega_2^2\omega_1\right) \\
&= -\frac{\omega_1\omega_2}{z_1^2}\frac{1}{4}\frac{1}{(\omega_1-\omega_2)(\omega_1+\omega_2)}\left((z_1^2+\omega_1\omega_2)(\omega_2-\omega_1)\right) \\
&= \frac{1}{4}\frac{\omega_1\omega_2}{z_1^2}\frac{z_1^2+\omega_1\omega_2}{\omega_1+\omega_2} \\
&= \frac{1}{4}\frac{\omega_1\omega_2}{\omega_1+\omega_2}\left(1+\frac{\omega_1\omega_2}{z_1^2}\right)=\frac{1}{4A}\left(1+\frac{C^2}{B}\right)
\end{aligned} \tag{B.6}
$$

Summary

In this section the integrals over transfer functions (noise integrals) with different numbers of poles and zeros have been calculated. They can be used to determine the total root-mean-square noise figure in case of a white noise spectrum. The integrals are summarized in table B.1.

classification	$H(\omega)$	$\int_0^\infty \lvert H(\omega)\rvert^2 \, d\nu$
one pole: ω_1	$\frac{1}{1+i\frac{\omega}{\omega_1}}$	$\frac{\omega_1}{4}$
two poles: ω_1, ω_2	$\frac{1}{\left(1+i\frac{\omega}{\omega_1}\right)\left(1+i\frac{\omega}{\omega_2}\right)}$	$\frac{1}{4}\frac{\omega_1\omega_2}{\omega_1+\omega_2}$
two poles: ω_1, ω_2 and one zero: z_1	$\frac{\left(1+i\frac{\omega}{z_1}\right)}{\left(1+i\frac{\omega}{\omega_1}\right)\left(1+i\frac{\omega}{\omega_2}\right)}$	$\frac{1}{4}\frac{\omega_1\omega_2}{\omega_1+\omega_2}\left(1+\frac{\omega_1\omega_2}{z_1^2}\right)$

Table B.1: Noise integrals for different transfer functions.

C CURO II reference

C.1 Command and Data Register

Two different serial shift registers are implemented in CURO II, the command and the data register. The data register, listed in table C.1, is 541 bit long and is used to configure the chip. Each of the global DACs has a resolution of 8 bit with an increment of $I_{LSB} \approx 1.4\,\mu A$ leading to a dynamic range of $\approx 360\,\mu A$. The outputs of each DAC are balanced with current mirror stages to obtain the desired range and resolution. The appropriate biasing values of the DACs, their ratios and ranges as well as the standard settings are given in table C.2. The command register contains 6 bit and is used to send commands to the chip. Table C.3 lists the command register, the different multiplexer modes (S0 and S1) are given in C.4.

Both registers are loaded via the pads: *com_in*, *com_out*, *com_clk* and *com_load*. *Com_in* and *com_out* are the input and output nodes of the shift registers, respectively. *Com_clk* shifts the registers on the rising edge, whereas *com_load* has two different tasks. First, it multiplexes the *com_in* and *com_out* nodes either to the command or data register and second, it latches the data that has been loaded into one of the registers. That ensures that the data becomes valid only after the register has been written completely. In case *com_load* is high, one has access to the command register via *com_in* and *com_out*, while the content of data register is set. Shifting the command register, the previous values are latched until *com_load* becomes low again. Note, that the multiplexer as well as the latches are level sensitive.

C.2 Analog Part

The general schematic of a current memory cell is shown in Fig. C.1. The steering signals of the memory cell are typed in italic. A detailed overview of the architecture of one analog channel of CURO II is given in Fig. C.2. Furthermore, the steering signals as well as the biasing currents of the different parts are shown in Fig. C.2. All steering signals are typed in italic. Note, that the bias current source (Ibias1) in the coarse part of the “pedestal subtraction cell” (pedsub) is omitted. The bias current is delivered by the pedestal of the input current.

overflow	indicates an overflown FIFO (read only function)
d1	2bit delay (deep inside the scanner)
d0	(it is not needed - fallback position)
counter_en	enables rowcounter in the Hit_RAM
bypass FIFO	bypasses the FIFO (FIFOout=FIFOin)
en_scanpattern	use scanpattern instead of current comparator output
continuous load	same scanpattern is loaded each cycle (independent of S1)
scanpattern $\langle 127:0 \rangle$	binary testpattern for the digital part
comp_en	enables comparators input
skewLD $\langle 1:23 \rangle$	load signal for the different deskewings
delayLD(coarse1)	load signal for the delay units, respectively
delayLD (coarseA)	"
delayLD (coarseB)	"
trimLD $\langle 4:0 \rangle$	load signal for the trimDAC in the current comparator
skew/delay $\langle 4:0 \rangle$	5bit value for either deskew, delay or trimDAC
comp $\langle 127:0 \rangle$	sets bitx of 5bit trimDAC (x selected by trimLD $\langle 4:0 \rangle$)
monitor_I_{BUS}	applies the analog testbus to the mon_out pad
mon_DAC_reference	applies the LSB value of the DAC reference to mon_out pad ($\approx 9\,\mu A$)
en_ped	enables a pedestal current source in columns (mask: hitpattern)
en_Test	enables a signal current source in columns (mask: hitpattern)
en_globalTest	routes a global current source to a column according to the hitpattern
DAC1..12 $\langle 0:8 \rangle$	sets the 8bit DACs, see table C.2.
hitpattern $\langle 127:0 \rangle$	enables the local current sources, see above

Table C.1: Data Register of CURO II (541 bit).

DAC number	biasing value	ratio	I_{LSB}	range	standard DAC setting
1	Icasc	1:1	1.4 μA	360 μA	150
2	Incasc1	"	"	"	100
3	Incasc2	"	"	"	115
4	Ipcasc1	1:2	0.7 μA	180 μA	66
5	Ipcasc2	"	"	"	90
6	Ibias1	"	"	"	66
7	Ibias2	"	"	"	90
8	Iped	"	"	"	–
9	Isig	"	"	"	–
10	Iin	1:16	87.5 nA	22.5 μA	–
11	Ithresh	"	"	"	–
12	Itrim,LSB	1:512	2.7 nA	700 nA	–

Table C.2: Overview of the 12 DACs (8 bit) and their corresponding biasing values, ratios and ranges. Although each DACs comprises 8 bit, 9 bits are used in the data register for configuration. Bit 9 applies the DAC current to the mon_out pad for monitor purposes.

1	ser_mode	enables readout mode for the Hit_RAM
2	hit_reset	resets the Hit_RAM counter
3	input_reset	resets the Input_FIFO counter
4	readback	sets the readback function in the next clock cycle
5	parallel_load	Mux_input: S1
6	serial_shift	Mux_input: S0

Table C.3: Command Register of CURO II.

S1	S0	function
0	0	hold
0	1	serial_shift
1	0	dump current compare
1	1	load register

Table C.4: Multiplexer settings used in the command register.

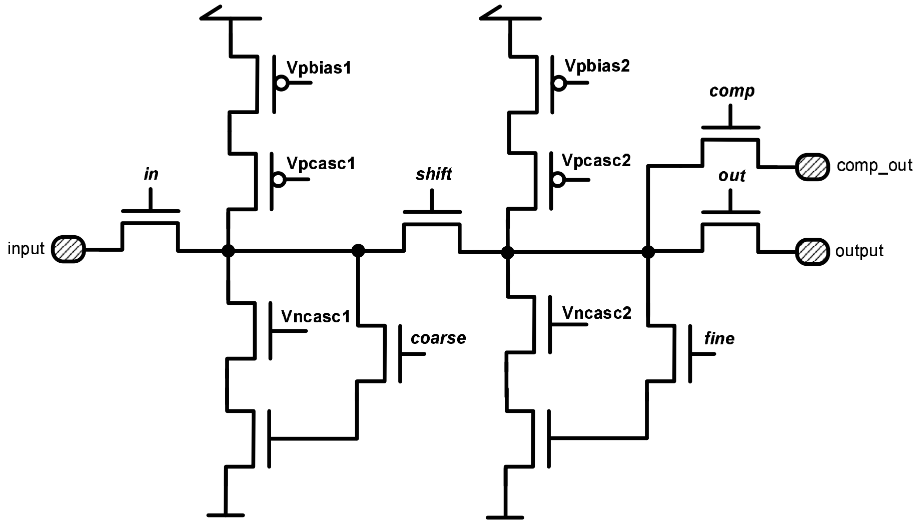

Figure C.1: General schematic of a current memory cell illustrating the different steering signals and biasing voltages.

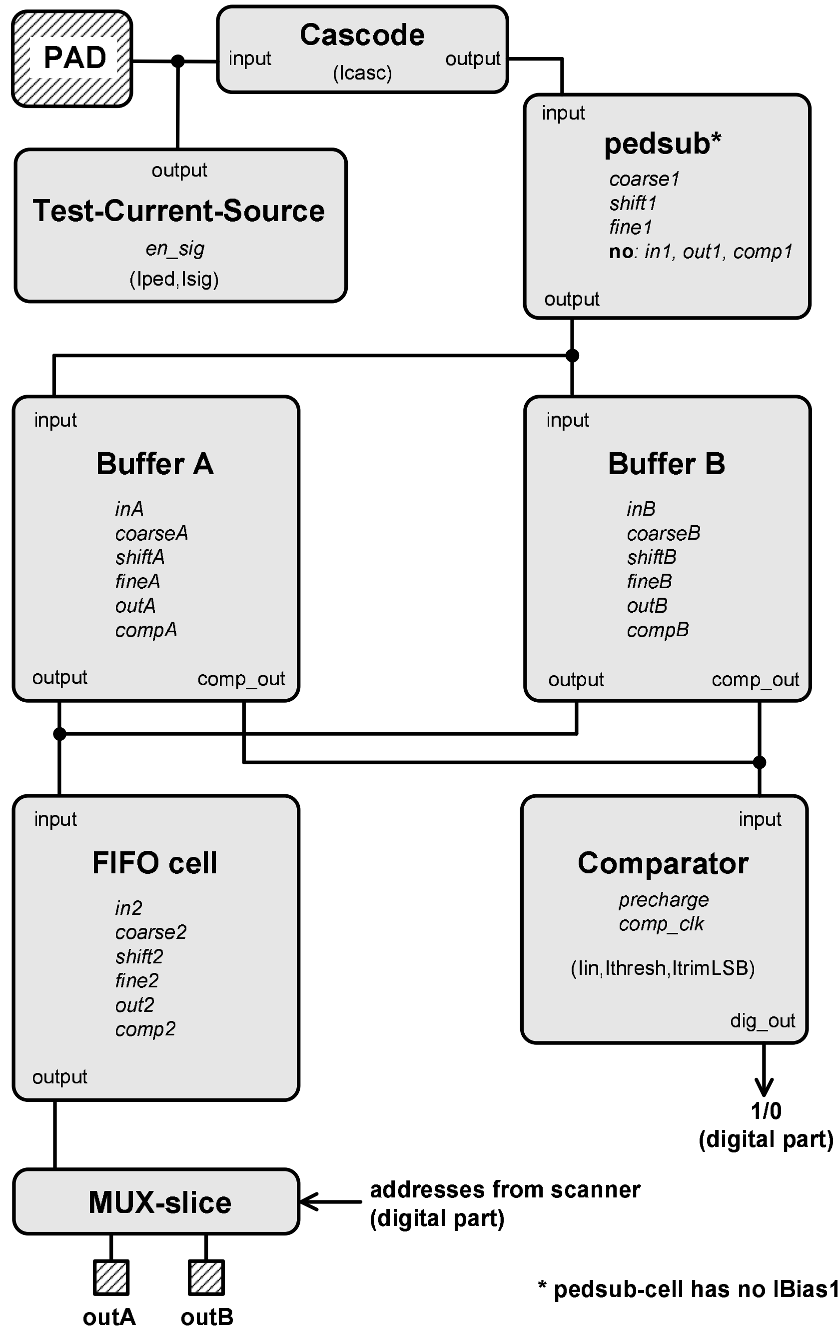

Figure C.2: Overview of one analog channel of CURO II. The steering signals as well as the biasing currents of the different parts are listed.

List of Figures

1.1 Principle overview of the proposed TESLA facility. The linear collider as well as the X-ray laser laboratory is shown. 11
1.2 Expected cross sections for selected e^+e^- annihilation processes depending on the center-of-mass energy $\sqrt{s}$ of the collider [8]. 12
1.3 Schematic drawing of one quadrant of the TESLA detector. All dimensions are in mm. The magnetic flux return yoke is instrumented as a muon detector. 15
1.4 Schematic overview of the tracking system of the TESLA detector (see text). 16
1.5 Detailed overview of the forward region of the TESLA detector. The LCAL, LAT and the forward disks (FTD) are shown. The vertical scale has been stretched [13]. 19
1.6 Feynman diagrams for incoherent pair production: Breit-Wheeler, Bethe-Heitler and Landau-Lifschitz process (from left to right). 20
1.7 Number of hits per bunch crossing (BX) due to pair production at different distances from the interaction point for various center of mass energies and magnetic field strengths [23]. 21
1.8 Baseline layout of the ILC vertex detector [24]. 22
1.9 Impact parameter resolution $\sigma(d_0)$ in $r\phi$-plane as a function of the particle momentum for different detector options [25]. 23
1.10 Bunch timing scheme of the ILC accelerator. 23

2.1 Principle of the sidewards depletion (left). Distribution of the resulting electrical field (right) and the potential (middle) in the detector substrate for different biasing conditions. 26
2.2 Cross section of a DEPFET pixel through the transistor channel, illustrating the principle of operation. 27
2.3 Simulation of the internal amplification g_q of a DEPFET device as a function the effective gate length using the TeSCA simulator [31]. 28
2.4 Cross section of a DEPFET pixel perpendicular to the transistor channel (view from drain to source) showing the clear principle of the device. Present devices are 450 μm thick, for the ILC a thickness of 50 μm is proposed. 29

2.5 Two possible readout concepts for a DEPFET pixel: A voltage based readout using a source-follower configuration (left) and a current based readout at the drain of the transistor (right). 31
2.6 Readout principle of a DEPFET matrix in a row wise operation with steering chips at the side of the matrix and a readout chip at the bottom. 33
2.7 Simplified geometry of a DEPFET double-pixel structure (left). Circuit showing the control and readout lines of a double-pixel structure (right). 34

3.1 Principle readout scheme of a DEPFET sensor matrix operated row wise. 35
3.2 Schematic overview of the CURO-Architecture. 37
3.3 Basic principle of the current memory stage [39]. The current source I_B is not necessarily needed and therefore drawn gray (left). Conventional voltage sample and hold (right). 39
3.4 Sampling transistor M1 of the current memory cell with the sampling switch S_2. A cascode transistor is integrated to improve the output conductance. 41
3.5 Small signal equivalent circuit of a current memory cell during the charging phase. With (left) and without (right) the sampling switch. 42
3.6 Response behavior of a second order system for the overdamped (left) and the underdamped (right) case illustrated the settling error. 43
3.7 Normalized settling error ε of a second order system ($\omega_0 = 500 \cdot 10^6\,\mathrm{s}^{-1}$) after t=15 ns as a function of $g_\mathrm{s}/g_\mathrm{crit}$. ε_0 indicates the limit for $g_\mathrm{s}/g_\mathrm{crit} \rightarrow \infty$. The star indicates the settling error for the critical switch conductance. 44
3.8 Noise sources considered for the noise analysis of the circuit. 45
3.9 Measured total gate capacitance as a function of gate-substrate bias for 250 annular nMOS transistors connected in parallel with W=16.03 μm and L=4 μm (static behavior). 49
3.10 Basic schematic of the double stage current memory cell. 51
3.11 Layout of the current memory cell ($25 \times 40\,\mu\mathrm{m}^2$). 53
3.12 Unregulated cascode stage with a constant voltage V_casc at the gate of cascode transistor (left). Regulated cascode using a feedback stage for the gate voltage (right). 54
3.13 Circuit of the regulated input cascode with a simple amplifier feedback stage (left). Small signal equivalent circuit of the regulated input cascode (right). 55
3.14 Simulated response behavior of the regulated cascode for an input swing of 10 μA without (left) and with (right) pole-zero cancellation for load capacitances C_L=2,5 and 10 pF. 57
3.15 Overview of the comparator unit (for each of the 128 channels). 58
3.16 Operational principle of the hitscanner architecture. The illustration is restricted to 4 inputs (left). Schematic of one scanner leaf. Only one back propagating part is shown (right). 60
3.17 Layout of one leaf of the scanner tree and one bit of the input register using radiation tolerant design rules ($25 \times 80\,\mu\mathrm{m}^2$). 61

3.18 Simulation of the required FIFO depth for different occupancies [54]. . . 62

4.1 Micro photograph of the $4.5 \times 4.5\,\mathrm{mm}^2$ CURO II chip (left) and the $1.5 \times 4\,\mathrm{mm}^2$ prototype chip CURO I (right) fabricated in a $0.25\,\mu$m process. 65
4.2 Screenshots from an oscilloscope, showing the sampling strobe for the coarse part of the “pedestal subtraction cell” for two different sampling times (left). Sampling time of the coarse part of the memory cell as a function of the MUX-setting (right). 66
4.3 Analog on-chip testability showing the global current source that can be multiplexed to each individual channel. 66
4.4 Linearity of one analog channel of CURO II. The output current is plotted as a function of the input current (left) and the deviation from a linear fit is shown (right). 67
4.5 Dispersion of the integral non-linearity of the analog part of CURO II for a signal range of $12.5\,\mu$A (left) and the dispersion of the pedestal subtraction (right) for all 128 channels. 68
4.6 Homogeneity of the transfer gain (left) and offset (right) of the analog part for all 128 channels of CURO II. 68
4.7 Drift of the output current of the current memory cell (fine part) at room temperature. 69
4.8 Performance of the pedestal subtraction. The output current is plotted as a function of the pedestal current for a constant signal current of $I_{sig} = 6.8\,\mu$A (left). The deviation from a linear fit is shown (right). . . . 69
4.9 Noise contribution of the CURO II chip comprising an internal test current source and two sample stages measured at 24 MHz row rate. The comparator response has been fitted by an error function. 70
4.10 Channel dispersion of the comparator threshold before and after the internal calibration. 72
4.11 Schematic overview of the configuration for the digital tests. 72
4.12 Total power consumption of the 128 channel readout chip CURO II as a function of the operating frequency (w_clk and s_clk). 73

5.1 Sketch of one end of a DEPFET based ladder with thinned sensitive area supported by a silicon frame for the first layer of the ILC vertex detector. 76
5.2 Readout concept for the innermost layer of the vertex detector (bottom) and for layer 2-5 (top). 78
5.3 Mechanical sample of a $13 \times 50\,\mathrm{mm}^2$ large thinned silicon structure. The central area has been etched down to $50\,\mu$m keeping a $300\,\mu$m thick frame for stiffening. Holes have been etched in the frame area for further reduction of the amount of material (left). Cross section of a PiN diode on high resistivity n-substrate (right) [61]. 79
5.4 Cross section of a ladder perpendicular to the beam pipe showing the thinned sensor area, the perforated frame with etched holes and the steering chips bump bonded to one sensor side. 82

5.5 Threshold shift ΔV_{th} and generated oxide trapped charge ΔD_{OT} during ^{60}Co irradiation [64]. 84
5.6 ^{55}Fe spectra ($\tau_S = 6\,\mu$s) of a DEPFET single pixel at room temperature after irradiation with a dose of 912 kRad using ^{60}Co [64]. 85
5.7 Conversion of a voltage noise at the gate of the DEPFET transistor into a current noise and into an equivalent noise charge (left). Simplified output stage of one channel of the SWITCHER II chip steering a matrix row (right). 86

6.1 Photograph of the ILC DEPFET-System. The sensor matrix on the sensor hybrid and the chip assembly are protected by a plastic cap (left). Micro photograph (area shown ≈ 23x16 mm^2) of the chip arrangement on the sensor hybrid, a 64×128 pixel DEPFET-Matrix in the middle, two steering chips SWITCHER II at the side and the readout chip CURO II at the bottom (right). 92
6.2 Schematic overview of the ILC DEPFET-System. 93
6.3 Timing scheme for the readout of a matrix row without zero suppression. For all pixels of a row, the two samples with the clear in between are taken in parallel. Afterwards, all pixels of the row are multiplexed to the ADCs. 93
6.4 System calibration of the complete readout chain (CURO, transimpedance amplifier and ADC) for channel 23. The DEPFET pixel matrix provides the pedestal current. The internal current source of the chip is used for calibration. The system response (left) and the deviation from a linear fit (right) is shown. 94
6.5 Measurement of the leakage current per pixel in a DEPFET sensor matrix. The system pedestal converted to charge in the internal gate is plotted as a function of the integration time. The measurement has been performed at room temperature. 96
6.6 System pedestals before (left) and after (right) common mode correction (CM) for each matrix column averaged over all rows. The two matrix halves are readout by separate readout chains. 97
6.7 Noise before and after common mode correction (CM) for each matrix column averaged over all rows. Column 127 has been excluded. 98
6.8 Energy spectrum for clusters consisting of 4 pixels from an ^{241}Am-source taken with the ILC DEPFET-System. 99
6.9 Linearity of the ILC DEPFET-System. The sensor response is plotted for different radioactive sources (left) and the deviation from a linear fit is shown (right). 100
6.10 Sketch of a $75\,\mu$m thick tungsten test chart (left). ^{55}Fe-radiogram of the $2 \times 3\,\mathrm{mm}^2$ test chart taken with the ILC DEPFET-System (right). 101

A.1 Weighting function for the correlated double sampling process $W^{CDS}(\omega)$. Transfer function of a CDS system additionally filtered by a single pole low-pass filter $H^{Sys}(\omega)$. The transfer function of the low-pass filter is illustrated by $H(\omega)$. 106
A.2 Principle setup of a system performing correlated double sampling. The input is determined by a total power spectral density (PSD) comprising thermal, 1/f and shot noise. The CDS process is described by $H^{CDS}(\omega)$ and the transfer function of the system is described by $H(\omega)$. 106
A.3 Normalized output noise contribution of thermal and 1/f-noise as a function of $\omega_c\tau$, where ω_c is the cut-off frequency of the low-pass filter and τ is the CDS sampling interval. 108

C.1 General schematic of a current memory cell illustrating the different steering signals and biasing voltages. 116
C.2 Overview of one analog channel of CURO II. The steering signals as well as the biasing currents of the different parts are listed. 117

List of Tables

1.1 Energy loss ΔE due to synchrotron radiation for different circular accelerator configurations. 11
1.2 Baseline parameters of the TESLA collider for 500 GeV and 800 GeV center-of-mass energies [10] compared to the LEP collider [11]. 14

3.1 Key parameters for different memory cells using annular transistors with two biasing conditions $I_D = 50$ and $65\,\mu A$ (see text). 50
3.2 Truth table of the scanner leaf shown in Fig. 3.16 (right). 60

4.1 Power consumption per channel of the CURO II chip. The total power consumption for two different operating frequencies as well as some bias contributions are listed. 74

5.1 Key parameters of the DEPFET pixel based vertex detector. 77
5.2 Enumeration of the readout channels and matrix rows to estimate the total power consumption of the DEPFET pixel based vertex detector. . . 81
5.3 Material Budget for layer one of the vertex detector. 82
5.4 Calculated noise contributions for an ILC DEPFET-System. 89

6.1 Operating parameters of the DEPFET matrix. 92
6.2 Radioactive sources and the emitted dominant X-ray-energies. A variable X-ray source provided the spectra for (Rb) to (Tb). 99

B.1 Noise integrals for different transfer functions. 113

C.1 Data Register of CURO II (541 bit). 115
C.2 Overview of the 12 DACs (8 bit) and their corresponding biasing values, ratios and ranges. Although each DACs comprises 8 bit, 9 bits are used in the data register for configuration. Bit 9 applies the DAC current to the mon_out pad for monitor purposes. 115
C.3 Command Register of CURO II. 116
C.4 Multiplexer settings used in the command register. 116

Bibliography

[1] D. Griffiths (1987): "*Introduction to Elementary Particles*", John Wiley & Sons, New York

[2] C. Quigg (1983): "*Gauge Theories of the Strong, Weak and Electromagnetic Interactions*", HarperCollins Publishers

[3] S. Weinberg (1976): "*Implications of dynamical symmetry breaking*", Phys. Rev. D13, pp.974-996

[4] M. Porro et al. (2004): "*Spectroscopic performances of DePMOS detector/amplifier device with respect to different filtering techniques and operating conditions*", IEEE Nuclear Science Symposium Conference Record Vol.2, pp.724-728

[5] J. Ulrici et al. (2003): "*Imaging Performance of a DEPFET pixel Bioscope system in Tritium autoradiography*", NIM A547, pp.424-436

[6] P. Allport et al. (2005): "*Linear Collider Flavour Identification: Case for Support*", P306/D89506

[7] K. Wille (1996): "*Physik der Teilchenbeschleuniger und Synchrotronstrahlungsquellen*", Teubner Studienbücher, 2.Auflage

[8] R. D. Heuer, D. Miller, F. Richard, P. Zerwas (2001): "*TESLA - Technical Design Report, Part III, Physics at an e^+e^- Linear Collider*", ISBN 3-935702-03-5, DESY Hamburg

[9] R. Brinkmann, K. Klöttmann, J.Roßbach, P. Schmüser, N. Walker, H. Weise (2001): "*TESLA - Technical Design Report, Part II, The Accelerator*", ISBN 3-935702-02-7, DESY Hamburg

[10] "*TESLA - Technical Design Report*" (2001), ISBN 3-935702-00-0, DESY Hamburg

[11] G. Altarelli et al. (1996): "*Physics at LEP*", ISBN 92-9083-081-6, CERN Geneva

[12] G. Materlik, Th. Tschentscher (2001): "*TESLA - Technical Design Report, Part V, The X-ray Free Electron Laser*", ISBN 3-935702-04-3, DESY Hamburg

[13] T. Behnke, S. Bertolucci, R. D. Heuer, R. Settles (2001): "*TESLA - Technical Design Report, Part IV, A Detector for TESLA*", ISBN 3-935702-05-1, DESY Hamburg

[14] R. Santonico, R. Cardarelli (1981): "*Development of resistive plate counters*", NIM 187, pp.377-380

[15] F. Sauli (1997): "*GEM: A New Concept for Electron Amplification in Gas Detectors*", NIM A386, pp.531ff

[16] Y. Giomataris, P. Rebourgeard, J.P. Robert, G. Charpak (1997): "*Micromegas: a High Granularity Position Sensitive Gaseous Detector for High Particle Flux Environments*", NIM A386, pp.531ff

[17] F. Badaud et al. (2001): "*Si-W calorimeter performances*", LC-DET-2001-058, DESY Hamburg

[18] O. Napoly, D. Schulte (1998): "*Luminosity Monitor Options for TESLA*", contribution to Linac98, Chicago

[19] K. Yokoya, P. Chen (1991): "*Beam-Beam Phenomena in Linear Colliders*", KEK-91-002, Tsukuba

[20] P. Chen (1988): "*Disruption, beamstrahlung and beamstrahlung pair creation*", SLAC-PUB-4822, Stanford

[21] M. S. Zolotorev, E. A. Kuraev, V. G. Serbo (1987): "*Estimates of Electromagnetic Background Processes for the VLEPP Project*" SLAC-TRANS-0227, IYF-81-63(translation)

[22] D. Schulte (1997): "*Study of Electromagnetic and Hadronic Background in the Interaction Region of the TESLA Collider*", PhD thesis, Hamburg University

[23] C. Hensel (2002): "*Search for Nearly Mass Degenerate Charginos and Neutralinos in e^+e^- Collisions*", PhD thesis, Hamburg University

[24] C. J. S. Damerell et al. (2001): "*A CCD-based Vertex Detector for TESLA*", LC-DET-2001-023, DESY Hamburg

[25] S. Hillert et al. (2005): "*Recent results from R&D towards a vertex detector at the future linear collider*", Vertex 2004, proceedings submitted to NIM

[26] T. Kuhl (2003): "*Vertex Detector as a physics tool for TESLA*", NIM A511, pp.221-224

[27] J. Kemmer, G. Lutz (1987): "*New semiconductor detector concepts*", NIM A253, pp.356ff

[28] L. Strüder (1999): "*Wide field imaging spectrometer for ESA's future X-ray mission: XEUS*", NIM A436, pp.53-67

[29] E. Gatti, P. Rehak (1984): "*Semiconductor drift chambers: an application of a novel charge transport scheme*", NIM A225 pp.608ff

[30] P. Klein (1995): "*Entwicklung, Bau und Test eines Halbleiter-Bildzellendetektors für den Einsatz in der Teilchenphysik*" PhD thesis, University of Munich

[31] R. H. Richter - *private communication*

[32] C. Sandow (2005): "*Ladungssammlung und Löschvorgang von DEPFET-Pixel-Sensoren*", Diploma thesis, Physical Institute, Bonn University

[33] J. L. Chu (1972): "*Thermionic injection and space-charge-limited current in reach-through p^+np^+ structures*" Journal of Applied Physics 43(8), pp.3510ff.

[34] C. Sandow et al. (2005): "*Characterization of the clear-mechanism of linear DEPFET-pixel structures*", 10th European Symposium on Semiconductor Detectors, proceedings submitted to NIM

[35] A. S. Niculae (2003): "*Development of a low noise analog readout for a DEPFET pixel detector*" PhD thesis, Siegen University

[36] C. Gemme (2001): "*Study of indium bumps for the ATLAS pixel detector*", NIM A465, pp.153-158

[37] ATLAS Collaboration (1999): "*ATLAS Detector and Physics Performance, Technical Design Report, Volume 1*", CERN/LHCC/99-14,25

[38] I. Peric (2004): "*Design and Realization of Integrated Circuits for the Readout of Pixel Sensors in High-Energy Physics and Biomedical Imaging*", PhD thesis BONN-IR-2004-13, Physical Institute, Bonn University

[39] J. B. Hughes, N. C. Bird, I. C. Macbeth (1989): "*Switched Currents - A New Technique for Analog Sampled-Data Signal Processing*", IEEE ISCAS (217) 333-4789, pp.1584-1587

[40] E. Säckinger, W. Guggenbühl (1990): "*A high-swing, high-impedance MOS cascode circuit*", IEEE Journal of Solid-State Circuits Vol.25, pp.289-298

[41] J. Millmann, A. Grabel (1988): "*Microelectronics*", McGraw Hill, New York

[42] Y. Tsividis (2003): "*Operation and Modeling of the MOS Transistor*", Oxford University Press, ISBN 0195170148, New York

[43] TSMC-Manual: "*0.25UM Logic 1PSM Salicide Spice Models*", T-025-LO-SP-005

[44] G. Wegmann, E. A. Vittoz (1990): "*Analysis and improvements of accurate dynamic current mirrors*", Journal of Solid-State Circuits Vol.25, pp.699-706

[45] B. Johnson, S. Eriksson (1993): "*New clock-feedthrough compensation scheme for switched-current circuits*", Elect. Letters Vol.29, pp.1446-1448

[46] C. Toumazou, N. C. Battersby, C. Maylaras (1990): "*High performance algorithmic dynamic current mirrors*", Elect. Letters Vol.26, pp.1593-1595

[47] C. Toumazou, S. Xiou (1994): "*An N-Step charge injection cancellation scheme for switched current circuits*", Electronics Letters Vol.30, pp.680-681

[48] C. Eichenberger, W. Guggenbühl (1990): "*On charge injection in analog MOS switches and dummy switch compensation techniques*", IEEE Transactions on Circuits and Systems, Vol.37, pp.256-264

[49] K. R. Laker, W. M. C. Sansen (1994): "*Design of Analog Integrated Circuits and Systems*", ISBN 0-07-036060-X, McGraw Hill, New York

[50] W. Liu (2001): "*Mosfet Models for Spice Simulation, Including BSIM3v3 and BSIM4*", Wiley-IEEE Press, ISBN 0-471-39697-4

[51] D. G. Nairn, C. A. T. Salama (1988): "*Algorithmic Analog/Digital Convertor Based on Current Mirrors*", Elect. Letters Vol.24 No.8

[52] P. Fischer (2001): "*First implementation of the MEPHISTO binary readout architecture for strip detectors*", NIM A461, pp.499-504

[53] W. Snoeys et al. (2000): "*Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip*", NIM A439, pp.349-360

[54] P. Fischer - *private communication*

[55] M. Trimpl et al. (2003): "*A Fast Readout using Switched Current Techniques for a DEPFET-Pixel Vertex Detector at TESLA*", NIM A511, pp.257-264

[56] R. Beccherle et al. (2002): "*The Readout Architecture of the ATLAS Pixel System*", Pixel 2002, Proceedings submitted to NIM

[57] J. Ulrici (2003): "*Bildgebung mit DEPFET-Pixelmatrizen für autoradiographische Anwendungen*", PhD thesis BONN-IR-2003-01, Physical Institute, Bonn University

[58] G. Deptuch (2005): "*Tritium Autoradiography with Thinned and Back-Side Illuminated Monolithic Active Pixel Sensor Devices*", NIM A543, pp.537-548

[59] Q.Y. Tong, U. Goesele (1999): "*Semiconductor Wafer Bonding*", John Wiley & Sons, New York

[60] G. Yan, P. C. H Chan, I-M. Hsing, R. K. Sharma, J. K. O. Sin, Y. Wan (2001): "*An improved TMAH Si-etching solution without attacking exposed aluminium*", Sensors and Actuators A89, pp.135-141

[61] L. Andricek et al. (2004): "*Processing of ultra thin silicon sensors for future linear collider experiments*, IEEE Transactions on Nuclear Science, Vol.51 No.3, pp.1117-1120

[62] R. Kohrs - *private communication*

[63] G. Wagner (2001): "*Neutron Background Studies at the TESLA collider*", LC-DET-2001-048, DESY Hamburg

[64] L. Andricek et al. (2005): "*The MOS-type DEPFET Pixel Sensor for the ILC Environment*", Pixel 2005, proceedings submitted to NIM

[65] K. Stefanov (2001): "*Radiation Damage Effects in CCD Sensors for Tracking Applications in High Energy Physics*", PhD Thesis, Division of Energy and Material Science, Saga University

[66] R. J. Kansy (1908): "*Response of a Correlated Double Sampling Circuit to 1/f Noise*", IEEE Journal of Solid-State Circuits Vol.SC-15, pp.373-375

[67] N. Wermes et al. (2004): "*New Results on DEPFET Pixel Detectors for Radiation Imaging and High Energy Particle Detection*", IEEE Transactions on Nuclear Science, Vol.51 No.3, pp.1121-1128

[68] R.H. Richter et al. (2003): "*Design and Technology of DEPFET Pixel Sensors for Linear Collider Applications*", NIM A511, pp.250-256

[69] Analog Devices: "*AD8015 - Wideband/Differential Output Transimpedance Amplifier*", http://www.analog.com

[70] W. H. White, D. R. Lampe, F. C. Blaha, I. A. Mack (1974): "*Characterization of surface channel CCD image arrays at low light levels*", IEEE Journal of Solid-State Circuits Vol.SC-9, pp.1-14

[71] D. F. Mix, N. M. Schmitt (1985): "*Circuit Analysis for Engineers, Continuous and Discrete Time Systems*", John Wiley & Sons, New York

[72] M. Karagounis (2004): "*Entwicklung analoger integrierter Schaltungen für Pixeldetektoren*", Diploma thesis, Fernuniversität Hagen

Acknowledgments

During my thesis I worked together with many people. Most of them had a positive impact on me and my work. Therefore, I would like to thank everybody who helped and supported me during this time. In particular:

- Prof. Dr. N. Wermes for giving me the opportunity to work on this interesting topic, providing such excellent working conditions and giving good advice whenever needed. Moving to Bonn was a good choice for me.
- Prof. Dr. Peter Fischer for the enlightening discussions and the various tips and hints being essential for making the right decisions.
- The ILC-DEPFET Team in Bonn: R. Kohrs, L. Reuen, C. Sandow and H. Krüger. Thanks for boosting the project during the end of my thesis.
- J. Ulrici for all the fun and the time when we perfected: "The art of making Latte Macchiato".
- A. Ludwig for the mostly non-physics discussions.
- M. Karagounis and G. Comes for the help with CADENCE and with the submissions.
- J. Velthuis for proofreading this thesis and making many useful remarks.
- Not to forget, all the other people at the Physics Group in Bonn, providing a very fruitful environment with useful discussions, and not of minor importance, all the cocktail parties (also very fruitful).
- The team from the semiconductor laboratory of the MPI Munich, especially G. Lutz, R. H. Richter, L. Andricek, J. Treis and S. Herrmann. It was a pleasure working together with you, sharing ideas and starting this project from scratch.
- Im Besonderen möchte ich meine Eltern und meine Familie erwähnen und einfach sagen: "Danke, dass ihr immer für mich da wart. Ich hoffe, wir werden noch eine lange Zeit miteinander verbringen."
- Iris Luhle for all the love, the support and the patience, especially during the end of my thesis.

- Not to forget our guinea pigs: Benny†, Bilbo†, Timmy†, Floh, Silver and Devil. Silver, Floh and Devil (from left to right) are shown in the picture below. The picture has been taken using the ILC DEPFET-System equipped with a CMOS-Test-Matrix [72].
- The Yuishinkan Dojo in Kamen for always having the opportunity of taking part in excellent training and for finding good fellows there. "*Domo arigato gozaimashta.*"
- And at last, the people who invented and maintain "*http://dict.leo.org*", without you guys it would have been much harder writing this thesis.

By three methods we may approach wisdom:
First, by reflection, which is the noblest;
second, by imitation, which is the easiest;
and third, by experience, which is the bitterest.
Confucius

Erklärung
Hiermit versichere ich, daß ich diese Arbeit selbständig verfaßt und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt sowie Zitate kenntlich gemacht habe.

Bonn, 28.10.2005