

Modelling of Spintronic Nanodevices for Neuromorphic Sensing Chips

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OVERVIEW

We developed a finite element method-based model of an MgO-barrier TMR device in *COMSOL Multiphysics*® for integrated circuit designers to implement them in a hybrid spintronic-CMOS system [1].

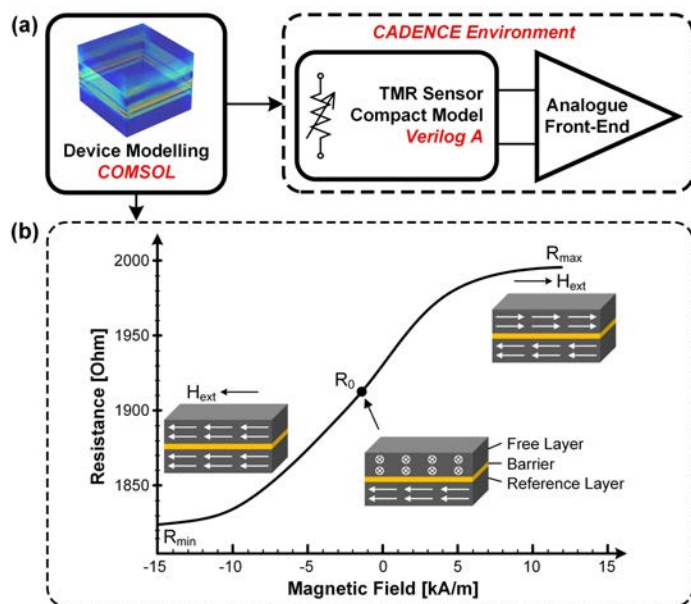


Figure 1: Proposed idea for extracting data from COMSOL Multiphysics® to Cadence® environment.

TMR STRUCTURE AND MODELING

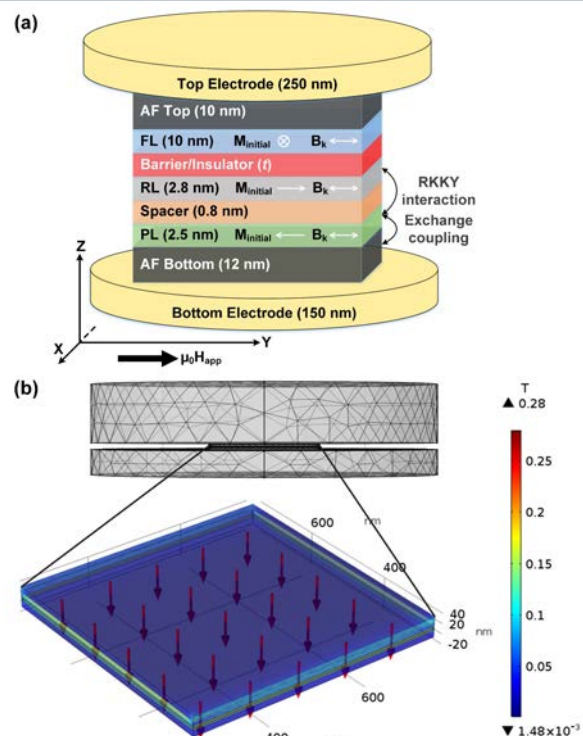
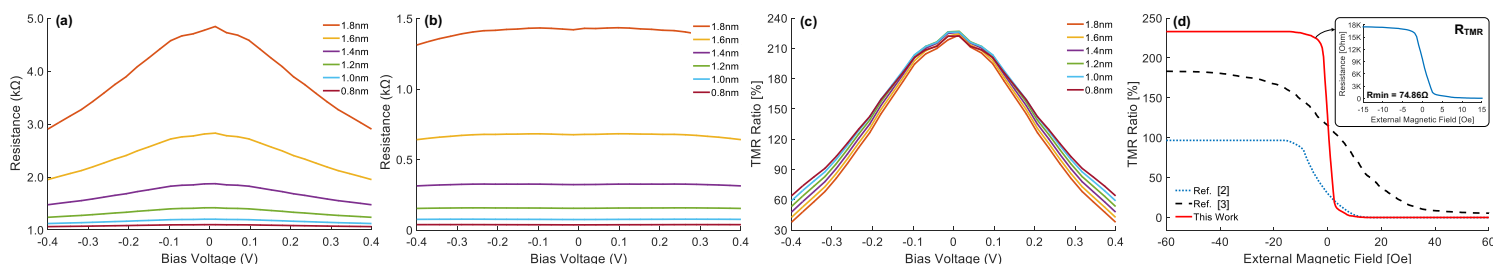


Figure 2: (a) TMR structure for FEM simulations; (b) Mesh created in COMSOL software and then zooming in on the MTJ.

SIMULATION RESULTS

These results are consistent with previous experimental results of fabricated MTJ samples reported in the literature, which show a higher TMR ratio and better small range linearization.

Figure 3: Effect of t_{ox} on (a) the anti-parallel and (b) the parallel resistances of the TMR sensor with different bias voltages. (c) Effect of t_{ox} on TMR ratio with different bias voltages. (d) TMR response compared to [2].

CONCLUSION AND FUTURE WORK

A novel TMR compact model was developed using *Verilog-A* extracted from accurate 3D FEM simulation. The effect of the insulator layer's thickness of TMR performance was presented for supporting spintronic-CMOS magnetic sensor development. A TMR ratio of 233% with 10 mV power supply was obtained from *COMSOL* and was verified *Verilog-A* model in Cadence.

REFERENCES

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