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AlGaN/GaN HEMT with Distributed Gate for Improved Thermal Performance

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***Abstract* — This paper reports a novel type of distributed gate (DG) HEMT fabricated using isolation by oxygen plasma. The technique results in planar devices with low gate leakage currents of only 1.3 μA/mm at -20 V gate voltage for devices with gate periphery of 1 mm. The DG-HEMT improves the thermal performance by reducing the current drop at higher drain voltages leading to higher output powers.**

***Keywords* — GaN high-electron-mobility transistor, distributed gates, gate leakage currents.**

I. Introduction

AlGaN/GaN HEMTs have an immense potential for high power and high voltage applications at microwave frequency range due to the superior material properties such as wide band gap, high critical field, high electron mobility and low intrinsic carrier density [1]. However, devices working at high voltage and high current conditions suffer from enhancement of heat generation in the device channel. This self-heating is one of the most undesirable effects in GaN power devices since it causes the degradation of the output current and limits the achievable device output power density, efficiency and device lifespan (which is directly related to channel temperature through the Arrhenius equation [2], [3]). Therefore it is crucial to employ a device geometry that reduces heat dissipation.

The use of high thermal conductivity substrates such as SiC or diamond improves the thermal performance, but the substrate alone is not enough to unlock the full potential of GaN [4]. Device layout with active and inactive regions along the width of the channel lead to channel temperature reduction. Darwish *et al.* used this distributed gate approach by forming inactive regions along the gate through etching the active layers [5]. Even narrow etched trenches (330 nm in [6]) along the channel are shown to reduce the thermal resistance improving the DC characteristics. A similar approach was taken by Lin *et al.* where the GaN layers were grown on Si substrate patterned with stripes of SiO_2 to achieve inactive and active regions along the device [7]. Using this approach, a good improvement in the thermal performance of the devices was demonstrated, but due to the etched mesa isolation the devices exhibited high gate leakage current.

In this paper, we demonstrate a novel method of obtaining a distributed gate GaN HEMT with planar isolation geometry obtained by oxygen plasma [8]. This approach not only improves the heat dissipation within the device but also shows lower leakage currents than any of the previous DG device fabrication attempts made by other groups [7].

II. Design and Fabrication

AlGaN/GaN HEMTs with were fabricated on a high thermal conductivity 4H-SiC substrate grown by metal organic vapour deposition. The epitaxial structure was composed of a thin Al nucleation layer followed by 1.8 µm high resistivity GaN, 200 nm of non-intentionally doped GaN, 20 nm of AlGaN with 25% Al content and 2 nm of GaN cap layer.

The source and drain Ohmic contacts were obtained by Ti/Al/Ni/Au (30 nm /180 nm/40 nm/100 nm) metal evaporation followed by annealing in nitrogen atmosphere at 800 °C for 30s. Ohmic contact resistances were measured to be 0.47 Ω·mm. Schottky gate contact was formed by evaporation of Ni/Au (20 nm/200 nm) metals. Oxygen plasma was used to isolate the devices (mesa isolation) and achieve a stripe patterned isolation along the device width.

The method of distributed gate efficiently improves the heat dissipation along the devices due to the fact that there is an active device region next to an inactive region as illustrated in Fig.1. Active device areas generate heat (indicated as ’’Hot’’ region), but inactive device areas don’t. These regions (indicated as ’’Colder’’ region) only absorb the heat leading to a reduced channel heating compared to a conventional device geometry with a continuous gate.

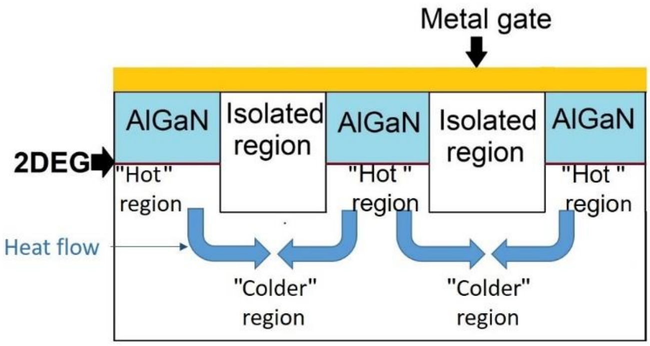

Fig. 1. Schematic illustration of heat dissipation principle in DG HEMT.

Two sets of devices were fabricated.

Firstly, DG-HEMT devices with a stripe pattern of 5.5 µm wide isolated lines and 4.75 µm active regions along the device width as illustrated in Fig. 2 and a conventional (C-HEMT) without distributed gates. The device geometry consisted of source-drain separation of 3.5 µm, gate length of 0.5 µm, gate pitch of 23.5 µm and an active device area of 10 x 100 µm. The sources were connected through metal bridges with polyamide layer underneath it for support.

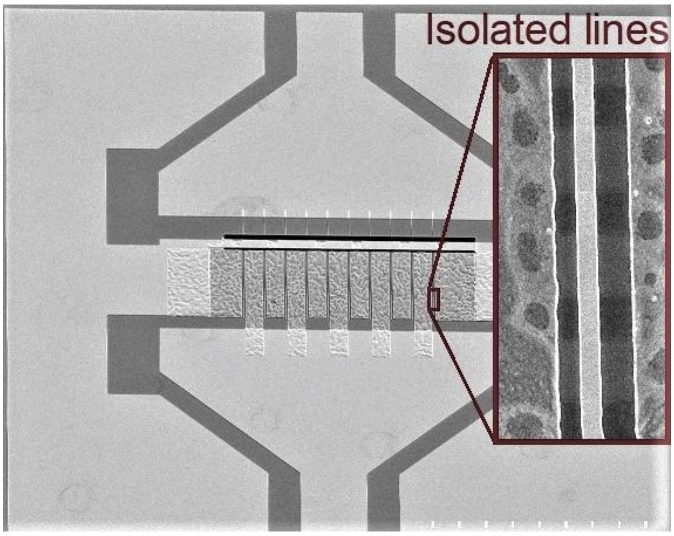

Fig. 2 SEM image of a fabricated 10 finger DG-HEMT with 0.5 µm gate length.

Secondly, DG- HEMTs and C-HEMTs were fabricated with the same drain-source separation of 3.5 µm and gate length of 0.5 µm, but the active area of 1 x 200 µm. The DG-HEMT pattern in 1 finger devices consisted of 6.5 µm wide isolated lines and 4 µm active regions. All devices were passivated with 30 nm ICP SiN and contact openings etched with SF6/N2 RIE.

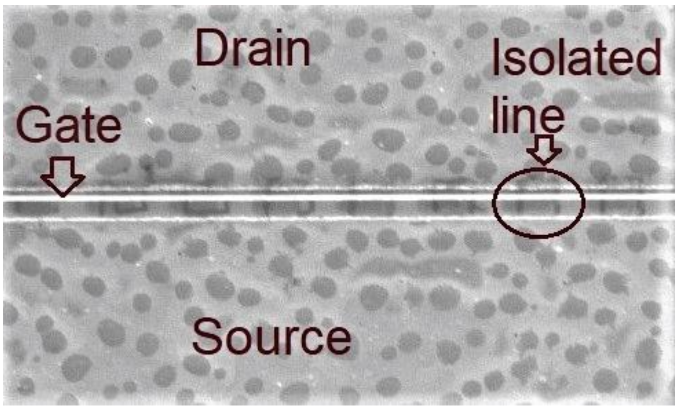

Fig. 3. SEM image of a fabricated 1 finger DG-HEMT with 0.5 µm gate length.

III. Results and discussion

Standard DC measurements were performed on the fabricated DG- and C-HEMTS.

A. *Devices with one finger*

The device output characteristics and transfer characteristics (at Vd = 5 V) shown in Fig. 4 and Fig. 5, respectively, demonstrate 15% improved device performance for the DG HEMT when compared to a C - HEMT. At gate voltages of 0 V and -1 V, the saturated drain current is higher for DG HEMTs. The higher currents and higher transconductance (gm, Fig. 5), is attributed to the reduced channel temperature due to the inactive regions along the device channel.

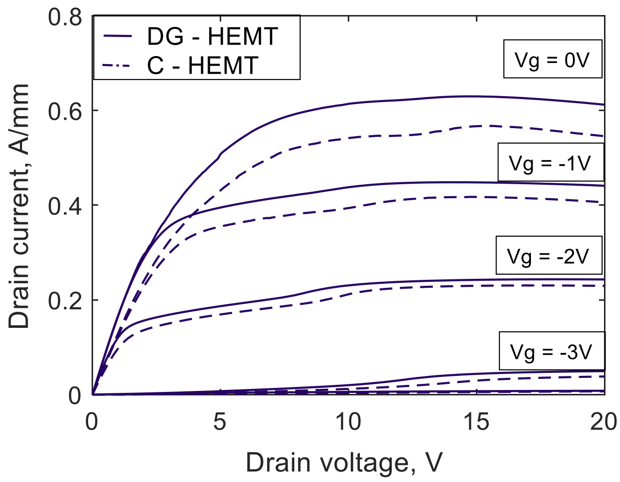

Fig. 4. Id - Vd characteristics for 1x200 µm DG-HEMT and C – HEMT geometries.

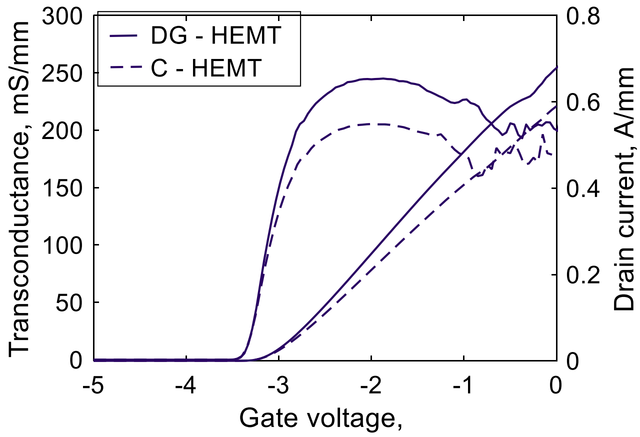

Fig. 5. Transfer characteristics at Vd = 5 V for 1x200 µm DG-HEMT and C-HEMT.

Fig. 6 shows the gate leakage currents; it is less than 1.8 µA/mm for both types of devices, which is 8 times less than in the etched DG geometries [7]. The difference in the leakage currents is negligible for the compared devices. There is no visible degradation in the leakage currents for DG device compared to C-HEMT due to the planar surface under the gate. This is the main advantage of the proposed technique over the etched distributed gates, since it also reduces the possibility of damaging the substrate during the etching process.

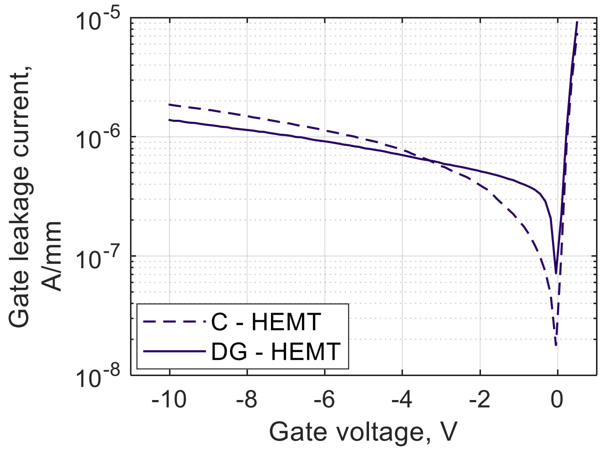

Fig. 6. Gate leakage currents at Vd = 0 V for 1x200 µm DG-HEMT and C-HEMT.

The device Id – Vg characteristics at 4 V drain bias are shown in Fig. 7. They show that the DG-HEMT and C-HEMT has the same gate threshold voltage (V_{th}) of -3.4 V.

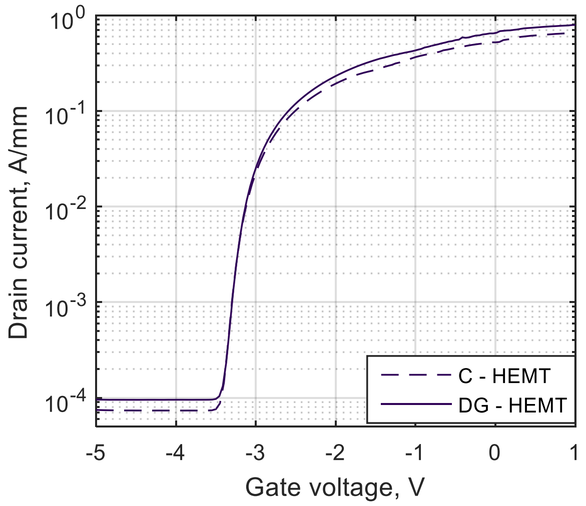

Fig. 7. Id- Vg characteristics at Vd = 4V for 1x200 µm DG-HEMT and C- HEMT.

The extrinsic current cut-off frequencies f_T (pad parasitics included) of the C-HEMT and DG-HEMT at 15 V drain voltage biased at the peak of g_m are measured to be 28 GHz and 22 GHz respectively. This is consistent with the previous work [5] which suggested that the DG geometry slightly increases the capacitances (Cds, Cgs, Cgd), and which leads to a lower f_T, because DG-HEMTs have larger total contact area and bigger bonding pads in order to achieve the same active area as C-HEMTs. There is therefore a trade-off between an optimised device geometry for reduced heat dissipation and electrical/ frequency performance of the device which must be considered when designing DG HEMTs, especially with large gate peripheries.

B. Multi-finger devices

Improved saturated output currents and transfer characteristics shown in one finger devices also translate to multifinger devices.

Fig. 8 Illustrates IV characteristics for DG and C-HEMT devices with 10 x 100 µm fingers measured continuously from Vg = 0 V to Vg = -5 V with 1 V increments. The self-heating can be most clearly seen in DC-IV characteristics at V_g = 0V, where after the knee voltage C-HEMT exhibits a steeper drop in the current at higher drain voltages. In addition, Fig. 8 also shows that the DG-HEMT exhibits smaller knee-walkout than C-HEMT. Both of these effects are consequences to self-heating in the channel region. Moreover, the level of saturated output current in DG-HEMT with the same total active area is slightly higher and the drop in the saturated current is significantly smaller than in the C-HEMT demonstrating improved heat dissipation in the channel region. However, the fact that the saturated output current still reduces with bias voltage means that the self-heating is not fully suppressed. Optimisation of the active and inactive regions along the gate width is still required to further reduce device self-heating.

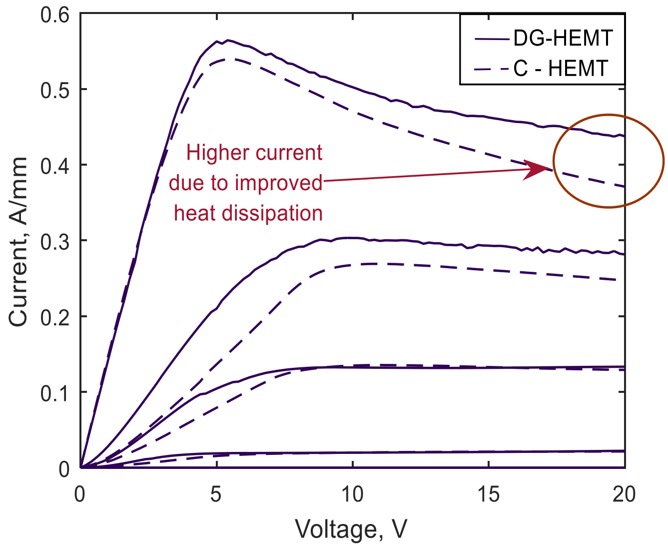

Fig. 8. Id-Vd characteristics of 10x100 µm DG-HEMT and C-HEMT.

Both DG- and C-HEMT devices have extremely low gate leakage currents as shown in Fig. 9. As in the case of 1 finger device (see Fig. 6), there is no degradation in the leakage currents for the DG-HEMT showing a huge advantage of this planar device geometry.

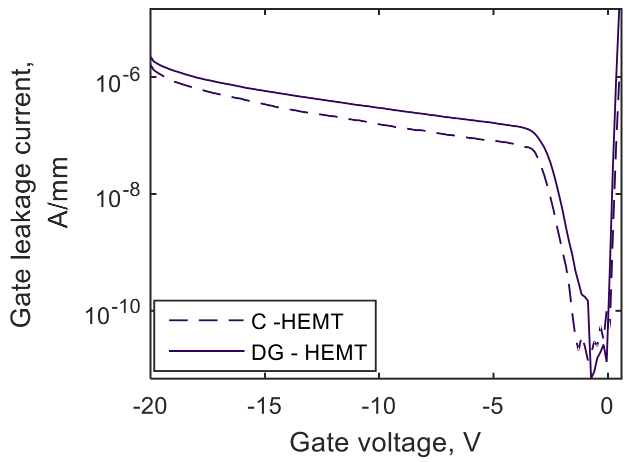

Fig. 9. Gate leakage currents at Vd = 0V for 10x100 µm DG-HEMT and C-HEMT.

IV. CONCLUSION

GaN HEMTs employing a novel planar isolation method and a distributed gate geometry have been described. They exhibit the lowest reported gate leakage currents of 1.3 µA/mm at -20 V gate voltage for 10x100 µm devices with distributed gate geometry. Moreover, the DG HEMTs exhibited enhanced saturated output current levels which we attribute to the improved heat dissipation. This new GaN HEMT technology is a highly promising one for high performance microwave power amplifiers and power electronics applications.

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