Correlation between Gate Length, Geometry and Electrostatic Driven Performance in Ultra-Scaled Silicon Nanowire Transistors

Talib M. Al-Ameri[1], Y. Wang[1], V. P. Georgiev[1], F. Adamu-Lema[1], X. Wang[1], L. Gerrer[1], A. Asenov[1, 2]
[1] Device Modeling Group, School of Engineering, University of Glasgow, Glasgow, G12 8LT, UK
[2] Gold Standard Simulations Ltd., Rankine Building, Oakfield Ave., Glasgow G12 8LT, UK
t.ali.1@research.gla.ac.uk

***Abstract*—This work investigates the impact of quantum mechanical effects on the device performance of n-type silicon nanowire transistors (NWT) for possible future applications. For the purpose of this paper we have simulated Si NWTs with six various cross-section shapes. However all devices in the cross-sectional area is kept constant in order to provide fair comparison between them. Additionally we expanded the computational experiment by including different gate length and gate materials for each of these six Si NWTs. As a result we were able to obtain correlation between the mobile charge distributions in the channel and gate capacitance, drain induced barrier lowering (DIBL) and the sub-threshold slope (SS). The mobile charge to gate capacitance ratio, which is an indicator of the intrinsic speed of the NWTs is also investigated. More importantly all calculations are based on quantum mechanical description of the mobile charge distribution in the channel. This description is based on Schrödinger equation, which is indeed mandatory for nanowires with such nano-scale dimensions.**

I. INTODUCTION

The gate-all-around (GAA) silicon nanowire transistors (NWT) have the potential to keep Moore's law continuing beyond the 7 nm mark [1-3]. One of the major reasons is that GAA design provides the best electrostatic integrity in comparison to all other different transistor architectures and therefore the best gate control over the channel [4, 5]. However, in such ultra-scaled GAA transistors, the quantum mechanical effects play a significant role and they must be considered in order to obtain accurate results about the device performance [6-8]. For example the quantum confinement effects lead to quantum threshold voltage shifts, simultaneously reducing the gate-to-channel capacitance and the available transport charge in the channel [9, 10]. The reduced gate-to-channel capacitance also has a negative effect on the electrostatic integrity. The impact of the above effects increases with the reduction of the characteristic confined dimensions and therefore will play a critical role in simulation-based research and design of sub-7nm NWT-based CMOS technology.

Moreover, the improvement in electrostatics can lead to much shorter effective channel length which will improve the density scaling. Also in conventional transistors, minimizing the interaction between source and drain is critical in improvement of the short-cannel effects. Such short channel effects can be evaluated with measurements or calculations of drain-induced barrier lowering (DIBL) and sub threshold (SS) slope. The theoretical limit value of DILB is ~ 0 mV/V and an ideal SS value is ~60 mV/dec at room temperature. In general, the short channel effect (SS and DIBL), and tunnelling current problems depends on the gate dielectric and electrostatic permittivity of the channel. Therefore solving the short channel effects can be obtained by careful device design consideration [2, 11]. For this reason in this work we also report results that establish a link between short-channel effects and various channel length and gate oxide materials.

Overall, in this paper, taking into account the quantum confinement effects, we provide a comprehensive view of the performance of six GAA NWTs as function of cross-section shape, channel length and different gate material. This includes comparing the impact of the nanowire cross-section shape on the SS and the DIBL of the simulated NWTs. The ultimate goal is to establish the strengths and the weaknesses of such devices and determine the best design configuration and parameters for specific application.

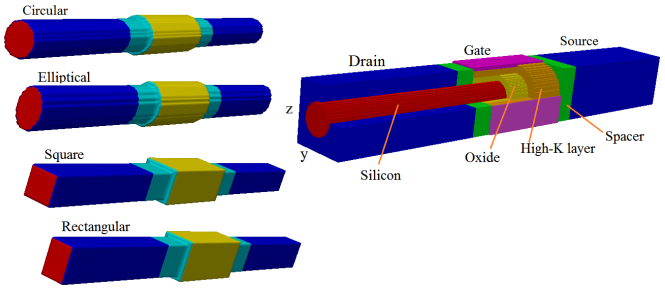

Fig. 1 3D schematic view of the circular NWT (right) and different cross-sectional shapes (left).

	Y(nm)	Z(nm)	Y/Z	Area (nm^2)
Circular	4	4	1	4π
Elliptical 1	3.448	4.64	0.74	4π
Elliptical 2	3.333	4.8	0.69	4π
Square	3.545	3.545	1	4π
Rectangular 1	3.0559	4.112	0.74	4π
Rectangular 2	2.954	4.2538	0.69	4π

Table 1 Physical dimensions of simulated devices.

T_{oxide} (nm)	0.8
Gate length (nm)	6-14
Spacer thickness (nm)	5.0
S/D peak doping (cm^{-3})	2×10^{20}
Channel doping (cm^{-3})	10^{15}
Substrate orientation	001
Nanowire orientation	110

Table 2 parameters of the simulated device

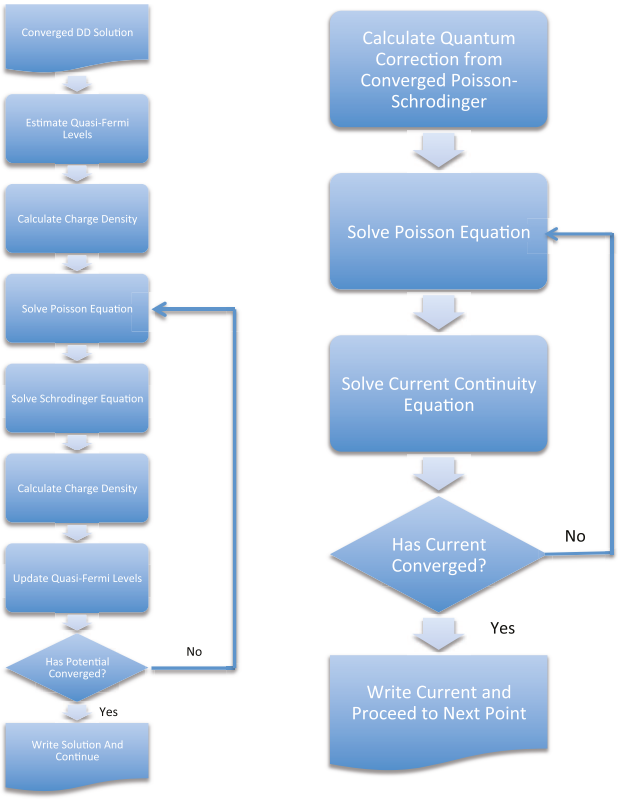

Fig. 2 Left: Flow diagram of the Poisson-Schrödinger model; Right: Flow diagram of the fixed Schrödinger quantum corrections DD model.

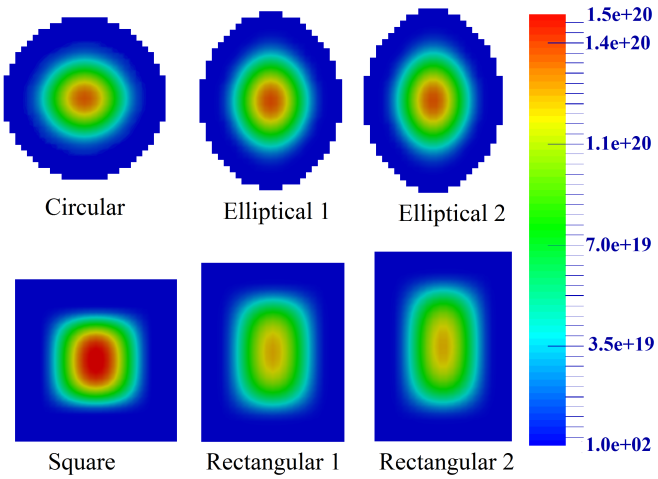

Fig. 3 Different NWT cross-sections simulated in this paper. Comparison of the charge distribution in the nanowire cross-section obtained from Poisson-Schrödinger simulations at Vg=0.65V.

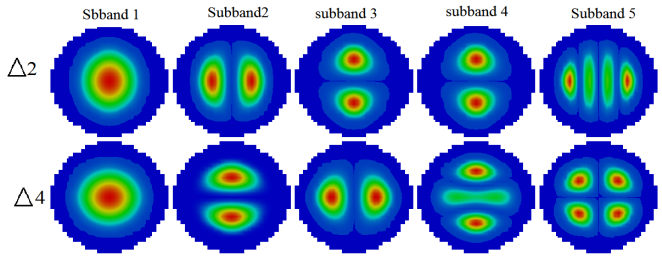

Fig. 4 Wavefunctions in the two-fold and four-fold degenerate valley in the 2D cross-section of a circular Si NWT (V_G=0.6V).

II. Simulation Methodology

A. The simulated nanowire transistors

The simulated NWTs considered in this paper have four different cross-section: cylindrical, elliptical, square and rectangular which are presented in Fig.1. Moreover, the elliptical and rectangular NWTs have two possible aspect ratio but all devices have an identical cross-section area of 4π nm^2. The precise cross-section dimensions for all six wires are shown in Table 1. The direction of transport is aligned along the crystallographic orientation <110>. Table 2 reveals the design parameters for all devices. All NWTs simulated in this paper have effective oxide thickness of t_{ox}= 0.8nm, gate length between 6-14 nm, spacer thickness of 5nm, source/drain doping peak of 2×10^{20} cm^{-3}, a channel doping of 10^{15} cm^{-3}.

B. Poisson-Schrödinger quantum correction

Our simulations are based on a Poisson-Schrödinger (PS) quantum correction technology achieved in a drift-diffusion (DD) module of the GSS 'atomistic simulator' GARAND [12] In our development, the PS model is coupled with the GARAND DD solution in stages to allow a computationally efficient manner of combining the impact of quantum confinement and carrier transport. To achieve this the DD simulation is carried out until convergence, then the quasi-Fermi level from the converged DD solution is used as a fixed reference within the Poisson-Schrödinger model to transfer the current transport behaviour. The PS model is then solved until convergence to obtain a QM solution of the charge density. This simulation flow is outlined in the left hand side on Fig. 2. After this the QM charge density from Schrödinger is used to obtain a fixed 'quantum correction' term. Using the fixed 'quantum correction' the GARAND DD loop is carried out again until convergence is obtained. The secondary DD loop is outlined in the right hand side on Fig. 2

More specifically in our case the quantum corrections in the DD modules is introduced by solving 2D Schrödinger equation. The 2D solutions of the Schrödinger equation are obtained in each cross-section along the gate length of the simulated transistor. The 2D Schrödinger equation is in an effective mass approximation [13, 14]. The charge distribution obtained from the solutions of the 2D Schrödinger equation is used to define the effective quantum-corrected potential. The 2D charge distribution for all NWTs is presented in Fig. 3. From the figure is clear that the quantum simulations capture the well-known volume inversion effects [15].

After this the 2D charge distribution for each cross-section solution is then combined to reform the 3D solution of the charge density of the device. This 3D charge density is then used in the Poisson solver to obtain the update potential. This updated potential is used as a driving potential in the solution of the current-continuity equation, keeping the charge distribution in the NWT cross-section identical to the charge distribution obtained from the solution of the Schrödinger equation. The simulations are finished when the current converges.

Also the 2D charge distribution is dictated by the quantum eigenvectors obtained by the Poisson-Schrodinger solution.

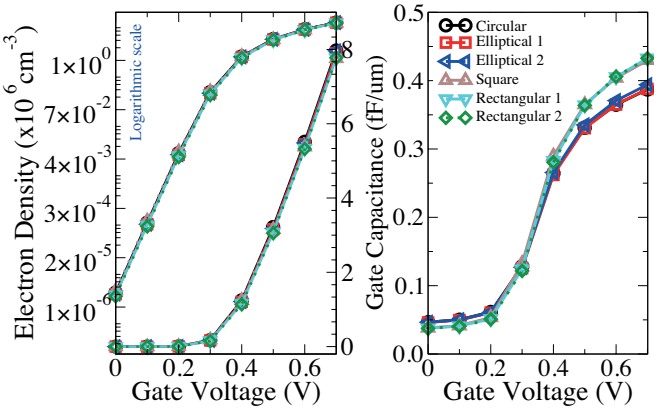

Fig. 5 Gate voltage dependence of the mobile charge in the channel (left) and capacitance-voltage (right) of all GAA NWTs at L_G=14nm.

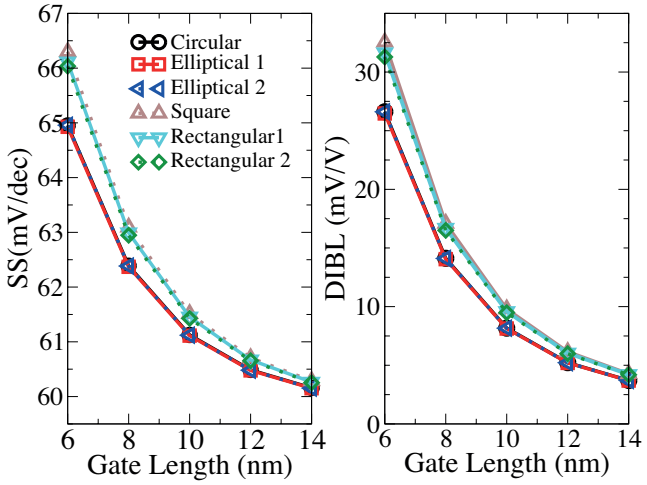

Fig 6 Impact of the gate length on SS (left) and DIBL (right) for all NWT with different cross-section.

	Q_M ($\times 10^6$/cm)	C_G (10^{-11}F/cm)	Q_M/C_G (10^{17}/F)
Circular	*5.80413*	*1.473629*	*3.938664345*
Elliptical 1	*5.8225*	*1.481912*	*3.929045719*
Elliptical 2	*5.8641*	*1.510259*	*3.882843936*
Square	*5.5937*	*1.810817*	*3.089047651*
Rectangular1	*5.7271*	*1.826929*	*3.134823521*
Rectangular2	*5.7678*	*1.829183*	*3.153211024*

Table 3 Q_M(V_G=0.60V), C_G (V_G=0.60V)and Q_M/C_G ratio at identical Q_M(G_V=0V) for NWTs at L_G=14nm.

The wavefunction in the two-fold (Δ2) and four-fold (Δ4) degenerate valleys in the cross-section of the circular nanowire are presented in Fig. 4. Additionally in our simulation the wavefunction penetration in the gate oxide is taken into account.

III. Gate Capacitance and Charge

Fig. 5 shows the gate voltage dependence of the mobile charge in the channel and capacitance-voltage (C-V) characteristics for all simulated NWTs. As it is expected the mobile charge (Q_M) and the gate capacitance (C_G) increases with increasing of the gate voltage. Moreover, both the gate capacitance and the mobile charge depend on the cross- section shape of the NWTs. In order to fairly evaluate the impact of the NWT shape on the potential performance, Table 3 compares Q_M (V_G=0.60V) for identical Q_M (V_G=0.0V). To make this comparison the Q_M (V_G) curves were aligned by changing the

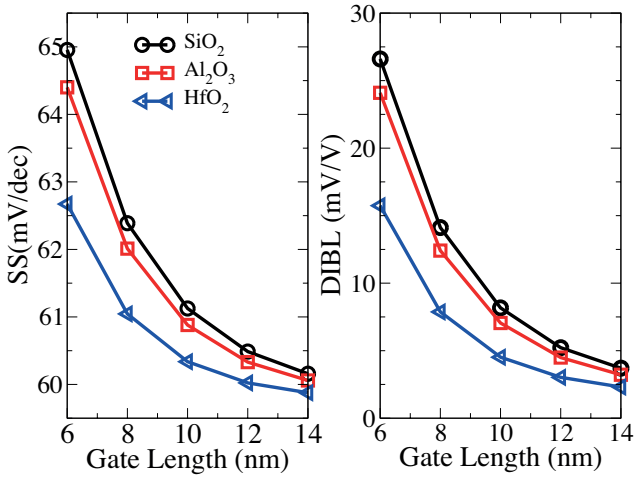

Fig. 7 The impact of three gate materials on SS (left) and DIBL (right) for circulat nanowire.

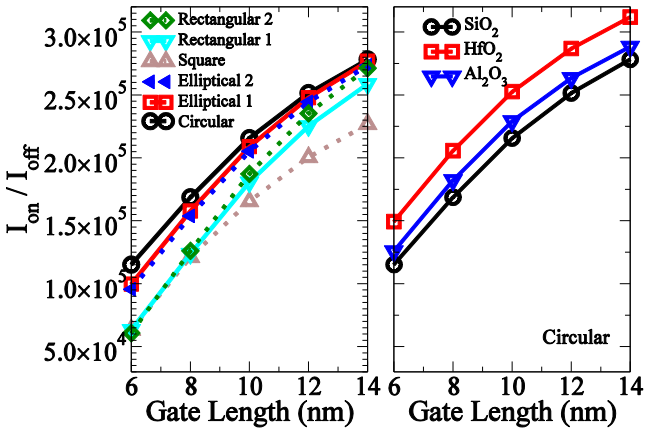

Fig. 8 *The impact of the six cross-section shapes on (I_{on}/I_{off}) (left) The impact of the three gate oxide material SiO_2, Al_2O_3 and HfO_2 on (I_{on}/I_{off}) (right) for circular nanowire.*

gate work function. From Table 3 the following important conclusions can be obtained. Firstly, circular and the two elliptical NTWs have ~9% more mobile charge in the channel in comparison to the square and rectangular devices. Also the mobile charge is affected by Y/Z ratio although the difference is not significant (see Table 1). Secondly, the gate capacitance increases with decreasing of the Y/Z ratio. Thirdly, overall all devise with circular shape have lower gate capacitance in comparison to the squared wires. Moreover Table 3 reveals information about the Q_M/C_G ratio, which is an indicator for the 'intrinsic' NWT speed. Clearly, the circular and elliptical devices show again better characteristics in comparison to the square and rectangular wires.

The impact of the gate length on drain-induced barrier lowering (DIBL), defined as $\Delta V_T/\Delta V_D$, and sub-threshold slope (SS) are illustrated in Fig. 6. There is relatively little difference in the electrostatic integrity between NTWs with different cross sections. However, all devices with circular shape perform slightly better in comparison to the other. We also would like to emphasize the fact that down to 6 nm gate length SS performance is comparable with the corresponding figures achieved by 22nm and 14nm FinFET CMOS technologies whereas DIBL performance is better. Moreover the SS for 14 nm channel length is very close to theoretical

limit of ~ 60 mV/dec at room temperature. Additionally all NWTs demonstrate excellent electrostatics even at ultra-short gate length of 6 nm. However, the two elliptical wires and the circular device are again performing better in comparison to all other NWTs.

Fig.7 compares the dependence of SS and DIBL of the channel length for the circular wire with three oxide materials – SiO_2, Al_2O_3 and HfO_2, where the dielectric constant value increases in the same order. The high-K layer (Al_2O_3 and HfO_2,) has 0.8 nm physical thicknesses and the interfacial SiO_2 layer is 0.3 nm. From Fig. 7 is clear that the devices with hafnium dioxide as a high-K gate layer material, which has the smallest equivalent oxide thickness (EOT), shows the best values for SS and DIBL characteristics.

Fig.8 (left) illustrates the dependence of (I_{on}/I_{off}) of the channel length for all NWT with different cross-section where I_{on} is leakage current and I_{off} is the drive current at low drain voltage V_D=0.05V and gate voltage V_G=0.6V. Fig.8 (right) compares the (I_{on}/I_{off}) for the circular nanowire wire with three oxide materials – SiO_2, Al_2O_3 and HfO_2. The calculated values of I_{on}/I_{off} curves are consistent with conclusions obtained for mobile charge (Q_M) and gate capacitance (C_G) presented in Table 3. Indeed the circular and elliptical NWTs shown better performance than square and rectangular wires. Moreover the nanowire with HfO_2 as a gate material shows the highest I_{on}/I_{off} ration in comparison to devices with SiO_2, Al_2O_3 as a high-K gate layer material.

IV. CONCLUSION

In this paper we report the quantum mechanical effects on the electrostatic performance of NWTs suitable for beyond the 7-nm CMOS technology. Moreover, we have revealed the fact that the NWT shape has an impact on the gate capacitance and the mobile charge in the channel of the transistors. Additionally, we also have demonstrated that different gate oxide materials have effect on the device characteristics such as sub-threshold slope and DIBL and thin EOT could lead to improvement of the device electrostatics. Also the different gate materials have impact on the I_{on}/I_{off} device characteristics. Similar as before the circular and elliptical wires perform better in comparison to the square and rectangular device. Overall our work shows that the circular and elliptical wires have better device characteristics, in terms of electrostatic driven performance, in comparison to square and rectangular ultra-scaled GAA NTWs.

V. REFERENCES

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