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SiGe *p*-channel MOSFETs with tungsten gate

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A self-aligned SiGe *p*-channel MOSFET tungsten gate process
with 0.1 μm resolution is demonstrated. Interface charge densities
of MOS capacitors realised with the low pressure sputtered
tungsten process are comparable with thermally evaporated
aluminium gate technologies (5 × 10¹⁰cm⁻² and 2 × 10¹¹cm⁻² for
W and Al, respectively). Initial results from 1μm gate length SiGe
p-channel MOSFETs using the tungsten-based process show
devices with a transconductance of 33mS/mm and effective
channel mobility of 190cm²/Vs.

Introduction: Recently there has been significant improvement in
the performance of SiGe *p*-channel MOSFETs, strained Si *n*-channel MODFETs and scaled bulk Si devices [1 – 3]. The motivation
for these enhancements is driven by CMOS shrinkage requirements, but also by the goal of realising microwave and millimetre
wave Si-based transceiver circuitry compatible with a standard
CMOS process flow.

One of the outstanding technological issues limiting the performance of 0.1μm gate length Si-based MOSFETs for both
CMOS and RF applications is the high resistance of conventional
poysilicon gate processes [4]. This has led to the development of
complex silicide and salicide gate stack processes [5] as well as the
demonstration of metal gate CMOS devices [6].

In this Letter a self-aligned SiGe *p*-channel MOSFET tungsten
gate technology with 0.1μm resolution is described, together with
the first results on 1μm gate length SiGe *p*-channel MOSFETs
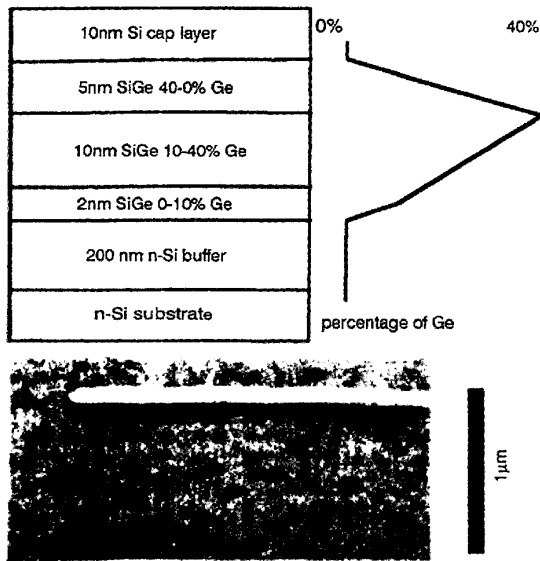realised with the process.

Fig. 1 *Layer structure showing percentage of Ge concentration, and SEM of 100nm W gate*

a Layer structure
b SEM

Fabrication: The layer structure on which devices are fabricated
was grown by MBE and is shown in Fig. 1*a*. Using both step and
linear grading, a maximum Ge concentration of 40% in the channel was achieved. The 200nm buffer layer, doped at 5 × 10¹⁷cm⁻³
n-type with Sb, is grown on an *n*-type Si substrate doped at 5 ×
10¹⁶cm⁻³. The channel comprises three layers: a 2nm SiGe layer
graded from 0 to 10% Ge followed by a 10nm SiGe layer graded
from 10 to 40% Ge, then a 5nm SiGe layer graded from 40 to 0%
Ge. Approximately 5nm of the 10nm Si cap layer is consumed
during the cleaning and oxidation processes. All layers above the
buffer are nominally undoped at a background level of 10¹⁵cm⁻³ *n*-type.

The device process flow begins with the growth of a 6nm gate
oxide using a 200min dry thermal oxidation performed at 750°C
to prevent any out-diffusion of Ge during the oxide growth. A further 30min 750°C anneal in an argon atmosphere results in a
device quality oxide layer. Next, the 100nm thick tungsten gate is
deposited by RF sputtering at a pressure of 2mtorr and power of
100W. To enable an assessment of the damage induced by the
sputtered tungsten process to be made, 100nm thick thermally
evaporated aluminium gate MOS capacitors were also defined for
comparison.

Tungsten gates with minimum feature sizes of 100nm as shown
in Fig. 1*b*, were fabricated using a Leica Microsystems Lithography LTD EBPG5 beamwriter and AZPN114 negative tone resist
to define the geometry, followed by tungsten patterning with a
2min, 100W SF₆ reactive ion etch performed at 9mtorr. *In situ*
reflectometry was used during the SF₆ etch to stop the gate metal
etch on the thin 6nm SiO₂ layer [7]. The self-aligned source and
drain contacts were produced using a shallow (< 100nm) BF₂
implant at an energy of 10keV and a dose of 10¹⁵atom/cm² activated by a 10s 900°C anneal. Source and drain metallisation of
100nm AlSi was followed by a 5min 400°C anneal. Finally, the
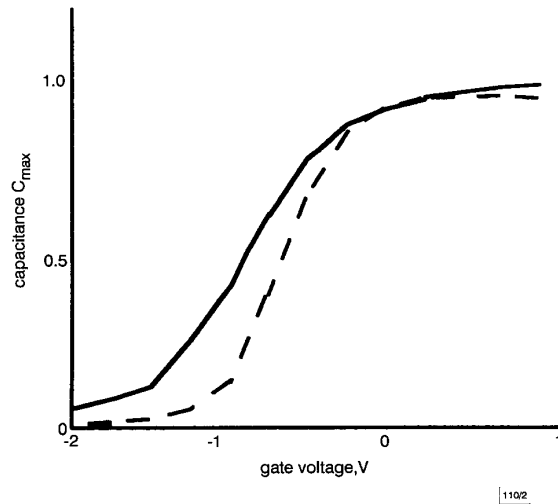devices were shallow trench isolated with a 5min, 100W SF₆ reactive ion etch performed at 9mtorr.

Fig. 2 *CV characteristics of W and Al MOS capacitors (20nm thick oxide)*
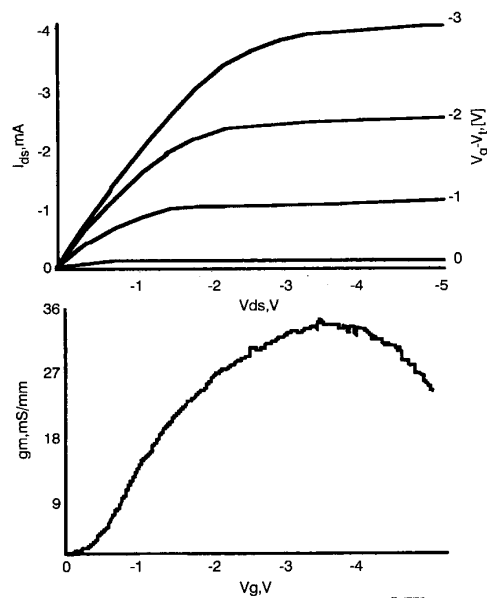
—— Al, Q_{int} = 2 × 10¹¹cm⁻²
- - - - W, Q_{int} = 5 × 10¹⁰cm⁻²

Fig. 3 *I-V and g_m characteristics of 1μm × 100μm p-SiGe W gate MOSFET*

Results: Fig. 2 shows the CV curve of SiGe-SiO₂ capacitors realised using both the sputtered tungsten and evaporated aluminium gate metallisations. The interface charge densities calculated from the flatband voltage shifts are 5×10^{10}cm^{-2} and 2×10^{11}cm^{-2} for W and Al, respectively, showing that the sputtered tungsten gate process causes only a small amount of damage. In addition the larger work function of tungsten results in a lower flatband voltage and thus a reduced threshold voltage when compared with the aluminium gate capacitors.

Using both the van der Pauw and four probe TLM methods, the resistivity of the 100nm thick sputtered tungsten gate metal film was determined to be 1.2Ω/□, a factor of 3 lower than similar geometry polysilicon and silicide gate structures [8]. The measured resistivity was independent of gate length down to 100nm.

Fig. 3 shows the I_{ds} (V_{ds}, V_{gs}) and g_m (V_{gs}) characteristics of a 1 × 100mm gate length SiGe MOSFET realised using the process described above. The maximum extrinsic transconductance is 33mS/mm. Estimating the channel hole concentration from the C(V) characteristic of the device and accounting for the channel access resistance of 500Ω measured with TLM structures, an effective channel mobility of 190cm²/Vs was extracted from the channel conductance at low drain bias ($V_{ds} = -0.1$V).

Conclusion: We have demonstrated a self-aligned SiGe *p*-channel MOSFET tungsten gate process with 0.1µm resolution. Interface charge densities of MOS capacitors realised with the low pressure sputtered tungsten process are comparable with thermally evaporated aluminium gate technologies (5×10^{10}cm^{-2} and 2×10^{11}cm^{-2} for W and Al, respectively) indicating that this a low damage process. The use of a tungsten gate produces devices with gate resistances of 1.2Ω/□ independent of gate length down to 100nm, making this process an attractive candidate for the realisation of low gate resistance devices for RF applications.

Initial results from 1µm gate length SiGe *p*-channel MOSFETs using the tungsten-based self-aligned gate process yielded a transconductance of 33mS/mm and effective channel mobility of 190cm²/Vs.

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References

1   VERDONCKT-VANDEBROEK, S.,   CRABBE, E.L.F.,   MEYERSON, B.S., HARAME, D.L., RESTLE, P.J., STORK, J.M.C., and JOHNSON, J.B.: 'SiGe-channel heterojunction *p*-MOSFETs', *IEEE Trans.*, 1994, **ED-41**, pp. 90–99

2   MAITI, C.K.,   BERA, L.K.,   and   CHATTOPADHYAY, S.:   'Strained-Si heterostructure field effect transistors', *Semicond. Sci. Technol.*, 1998, **13**, (11), pp. 1225–1246

3   TAUR, Y., BUCHANAN, D.A., CHEN, W., FRANK, D.J., ISMAIL, K.E., LO, S.-H., SAI-HALASZ, G.A., VISWANATHAN, R.G., WANN, H.-J.C., WIND, S.J., and WONG, H.-S.: 'CMOS scaling into the nanometer regime', *Proc. IEEE*, 1997, **85**, (4), pp. 486–504

4   SHAHIDI, G.G.,   WARNOCK, J.D.,   COMFORT, J.,   FISCHER, S., MCFARLAND, P.A., ACOVIC, A., CHAPPELL, T.I., CHAPPELL, B.A., NING, T.H.,   ANDERSON, C.J.,   DENNARD, R.H.,   SUN, J.Y.-C., POLCARI, M.R., and DAVARI, B.: 'CMOS Scaling in the 0.1-µm, 1.X-Volt regime for high performance applications', *IBM J. Res. Develop.*, 1995, **39**, (1/2), pp. 229–242

5   RISHTON, S., MII, Y.J., KERN, D.P., TAUR, Y., LEE, K.E., LII, T., and JENKINS, K.: 'High-performance sub-0.1µm silicon *n*-metal oxide semiconductor transistors with composite metal polysilicon gates', *J. Vac. Sci. Technol. B*, 1993, **11**, (6), pp. 2612–2614

6   BUCHANAN, D., MCFEELY, F., and YURKAS, J.: 'Fabrication of midgap metal gates compatible with ultrathin dielectrics', *Appl. Phys. Lett.*, 1998, **73**, (12), pp. 1676–1678

7   HICKS, S.E., PARKES, W., WILKINSON, J.A.H., and WILKINSON, C.D.W.: 'Reflectance modeling for in situ dry etch monitoring of bulk SiO₂ and III-V multilayer structures', *J. Vac. Sci. Technol. B*, 1994, **12**, (6), pp. 3306–3310

8   SHAHIDI, G.G.,   WARNOCK, J.D.,   COMFORT, J.,   FISCHER, S., MCFARLAND, P.A., ACOVIC, A., CHAPPELL, T.I., CHAPPELL, B.A., NING, T.H.,   ANDERSON, C.J.,   DENNARD, R.H.,   SUN, J.Y.-C., POLCARI, M.R., and DAVARI, B.: 'CMOS scaling in the 0.1µm, 1.X-Volt regime for high performance applications', *IBM J. Res. Develop.*, 1995, **39**, (1/2), pp. 229–242

Ultra-shallow junction technology by atomic layer doping from arsenic adsorbed layer

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A novel S/D junction technology for realising sub-0.1µm NMOSFETs is proposed. In this technology, S/D extensions are formed using arsenic (As) diffusion from an As adsorbed atomic layer on the silicon surface by high temperature RTA. This method provides an extremely shallow extension (below 20nm) with low sheet-resistance (below 2kΩ/□), maintaining a low junction leakage. NMOSFETs fabricated using this technology show better suppression of the short channel effect compared to conventional FETs.

Introduction: In sub-0.1µm NMOSFETs, an extremely shallow junction in a source and drain region is required to suppress a short channel effect (SCE). Recent shallow doping methods instead of low energy As implantation have mainly used phosphorus ion as a dopant [1]. Although As is the preferred N-type dopant in the shallow junction formation, another As doping method apart from ion implantation has not been presented until now.

In this Letter, we investigate the As diffusion from an As adsorbed atomic layer on the silicon surface, and propose process conditions to achieve ultra-shallow junction with low resistance and low junction leakage. Finally, the device characteristics of sub 0.1µm NMOSFETs fabricated by this method are evaluated.
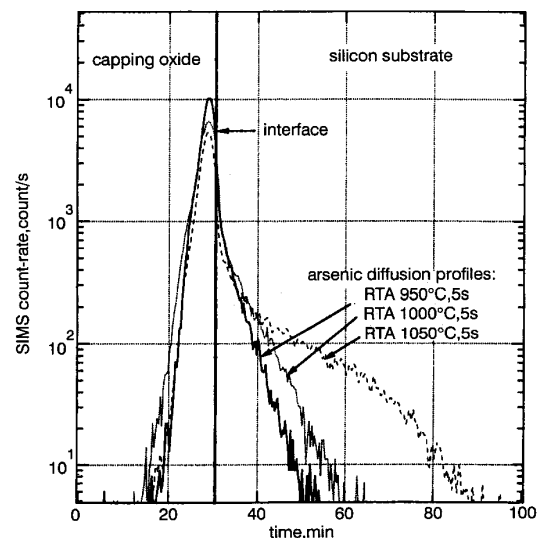

Fig. 1 *Typical SIMS profiles under different RTA conditions of As atomic layers formed by AsH₃ injection at 550 °C for 30min*

Shallow junction formation: The As layer doping consists of three essential steps. First, AsH₃ is supplied to the silicon surface for the As layer formation. Secondly, non-doped silicon glass (NSG) film, used as a capping film, is deposited on the As adsorbed layer by using the APCVD method. Thirdly, rapid thermal annealing (RTA) is carried out. The maximum As coverage (0.95 monolayer) on the silicon surface was obtained at AsH₃ reaction temperature