A Comparison of High-Power Converter Topologies for the Implementation of FACTS Controllers

Diego Soto, *Member, IEEE*, and Tim C. Green, *Member, IEEE*

***Abstract*—This paper compares four converter topologies for the implementation of flexible ac transmission system (FACTS) controllers: three multilevel topologies (multipoint clamped (MPC), chain, and nested cell) and the well-established multipulse topology. In keeping with the need to implement very-high-power inverters, switching frequency is restricted to line frequency. The study addresses device count, dc filter ratings, restrictions on voltage control, active power transfer through the dc link, and balancing of dc-link voltages. Emphasis is placed on capacitor sizing because of its impact on the cost and size of the FACTS controller. A method for the dimensioning the dc capacitor filter is presented. It is found that the chain converter is attractive for the implementation of a static compensator or a static synchronous series compensator. The MPC converter is attractive for the implementation of a unified power flow controller or an interline power flow controller, but a special arrangement is required to overcome the limitations on voltage control.**

***Index Terms*—flexible ac transmission system (FACTS), high-power inverter, multilevel converter, multipulse converter, static compensator (STATCOM), unified power flow controller (UPFC).**

I. Introduction

THE case for using high-power electronics equipment, under the concept of a flexible ac transmission system (FACTS) [1], to enhance and optimize the use of transmission facilities is compelling. During the last decade, the feasibility of modern FACTS controllers based on a voltage-source inverter (VSI) rated above 80 MVA has been demonstrated [2]–[4]. However, it is clear that there are still major issues to resolve before the full potential of VSI-FACTS controllers is realized and implementation becomes commonplace.

High-performance and cost-effective high-power inverters are a prerequisite for the realization of FACTS controllers such as the static compensator (STATCOM) [2], [3], the static synchronous series compensator (SSSC) [5], the unified power flow controller (UPFC) [4], and the interline power flow controller (IPFC) [6]. For some time to come, implementation of such inverters will be difficult because of limitations of the semiconductor devices. Typical voltage ratings are between 3–6 kV and are a small fraction of those required. Thus, series connection of devices is commonplace in FACTS designs. Power dissipation during conduction and switching is such that the switching frequency is severely limited. Typically, line-frequency switching is used. In the future, higher frequency operation might be possible but synchronous pulsewidth modulatin (PWM) at a low frequency is the best that is anticipated.

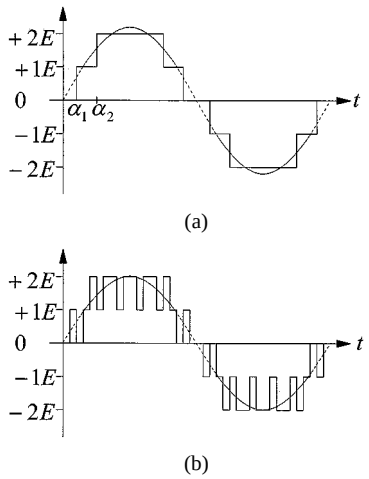

Fig. 1. Example five-level waveforms. (a) Line-frequency switched. (b) PWM.

Combining large numbers of semiconductor devices to achieve a high VA rating is well established. Choosing an arrangement where all the devices are individually controlled (rather than switched together in series) provides more control opportunities to set things like voltage magnitude and suppress harmonics. Further, switching each device from a voltage source that is a fraction of the total avoids the problem of designing the passive [7] or active [8] sharing mechanisms needed for series connections of devices switched from the total voltage.

Multilevel inverters [9]–[14], of which three implementations will be discussed later, can produce "staircase" voltage waveforms [Fig. 1(a)]. Each pair of levels (one negative and one positive) provides one control angle (α) per quarter-cycle (a degree of freedom) used to set the amplitude of one harmonic to zero. One degree of freedom can be used to set the magnitude of the fundamental.

PWM methods can be employed [Fig. 1(b)] to give good sine-wave representations if such a high switching frequency can be accommodated. Multilevel PWM is gaining acceptance in large industrial drives [13]. However, the line-frequency switched version remains of most interest in FACTS implementations.

The alternative to the multilevel converter is the multipulse converter [2]–[4]. Simple units producing three-phase quasi-square-wave voltage (or current) (known as six-pulse units) are combined via phase-shifting isolation transformers.

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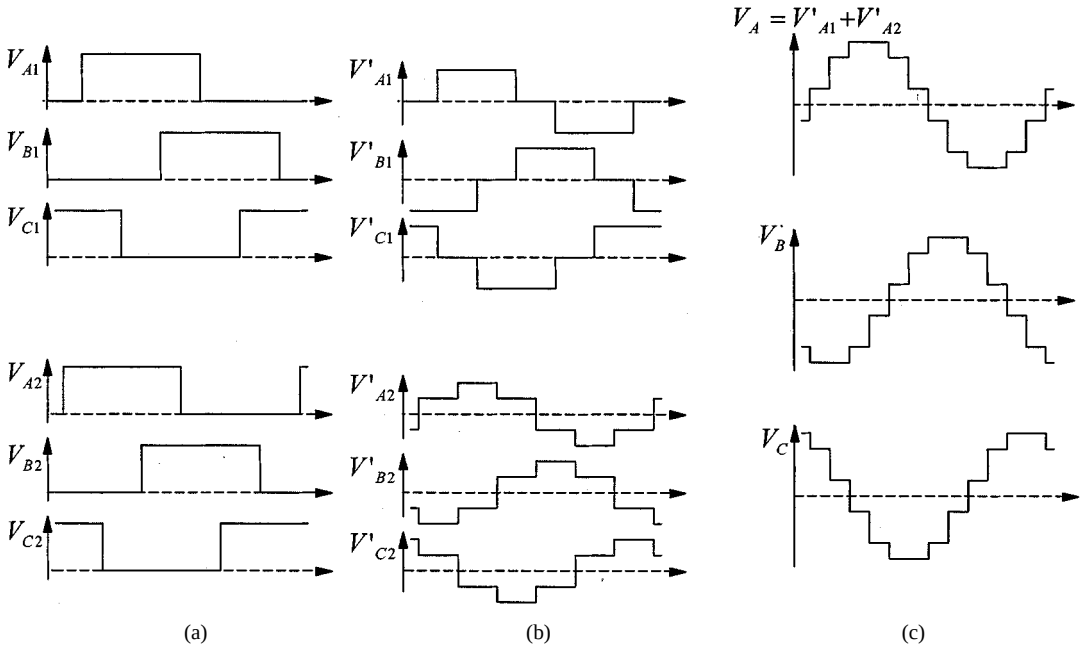

Fig. 2. 12-pulse waveforms created from two sets of six-pulse waveforms.

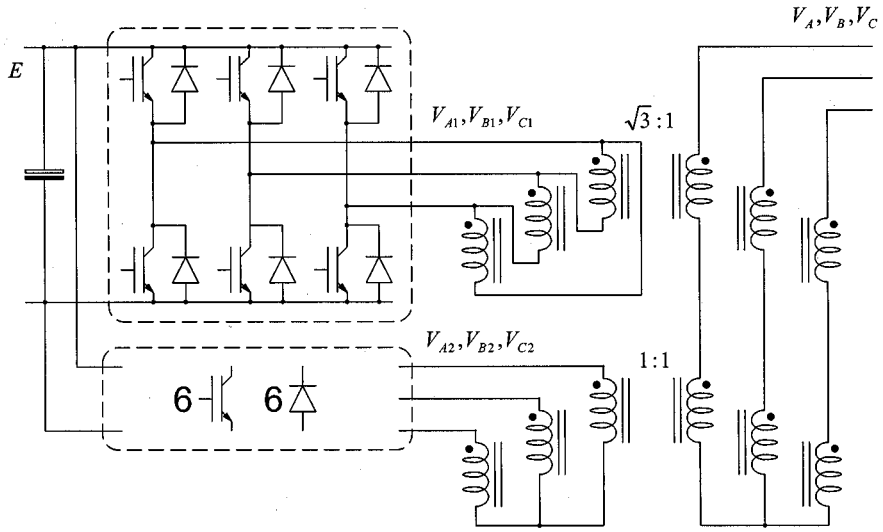

Fig. 3. 12-pulse inverter using delta/open and star/open connection of six-pulse units.

Each unit provides a fraction of the VA rating of the overall circuit. Fig. 2(a) shows two sets of three-phase six-pulse waveforms (V_{A1}, V_{B1}, V_{C1} and V_{A2}, V_{B2}, V_{C2}) with a time shift between them. Fig. 2(b) shows how these waveforms are affected by a delta–delta transformer (removal of zero sequence) for the first set and a star–delta transformer (line voltage to phase voltage transformation) for the second. Finally, in Fig. 2(c), the two sets of voltages are added in series to produce 12-pulse three-phase waveforms that are a reasonable approximation of a sine wave. Fig. 3 shows the circuit that would produce the multipulse waveforms of Fig. 2.

In this paper, all four converter topologies (one multipulse and three multilevel) will be compared in terms of device count, capacitor size, restrictions on the voltage control, ability to transfer power through the dc link, and ability to maintain the balance of the dc link (in the multilevel configurations). From this, the application areas will be identified where each converter may prove useful.

II. High-Power Converter Topologies

A. Multipulse Converter

The reduction in distortion that is achieved by increasing the number of six-pulse units, N_P, comes about through harmonic cancellation. Each unit produces a quasi-square-wave time shifted from that required for the final output. The phase-shift transformers align the fundamental components. The designer exploits combinations of time shift of a waveform with phase shift of transformers in order to cancel harmonics. Normally, a 12-pulse unit ($N_P = 2$) is arranged to cancel 5th and 7th harmonics (and those at $6(2k-1) \pm 1$ where k is any integer). In general, combining N_P six-pulse units provides a

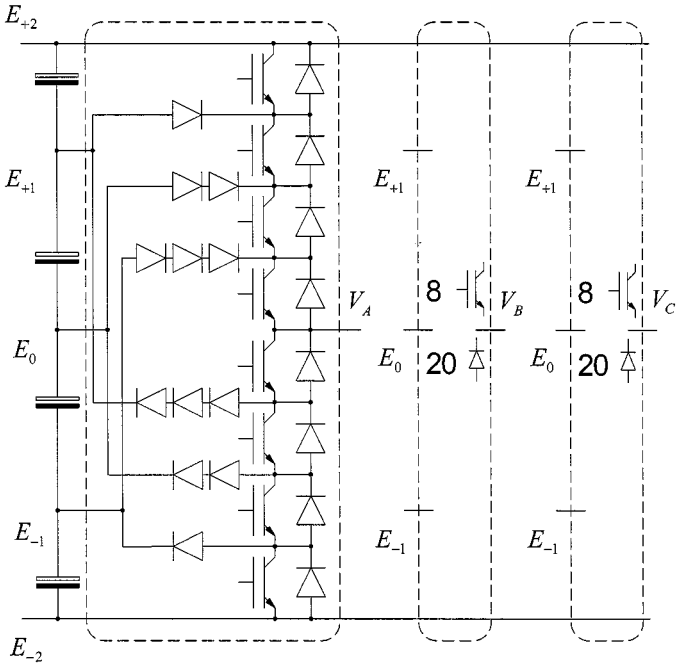

Fig. 4. Five-level multpoint-clamped inverter.

$6N_P$-pulse converter. All harmonics except those at $6kN_P \pm 1$ are cancelled.

The 12-pulse converter of Fig. 3 uses transformers with standard star and delta windings. For higher pulse numbers, the structure of the phase shift transformer becomes complex and its implementation appears difficult and expensive. Nevertheless, most existing VSI-FACTS controllers rated above 80 MvAr use either 24- or 48-pulse converters [2]–[4]. Each reported implementation uses a unique transformer design. There may be still a long way to go before a standard design is developed.

B. Multilevel Converters

Multilevel converters use an array of switches to select the output voltage from a number of available dc power supplies. The dc voltage sources are typically implemented using capacitors with a charge-balancing scheme used to maintain the voltage constant. All the implementations of the multilevel inverter require the same number of semiconductor switches for a given number of levels. Each extra level requires two switches per phase, i.e., $N_{S/P} = 2(N_L - 1)$, where $N_{S/P}$ is the number of switches per phase and N_L is the number of levels.

Despite using the same number of switches, there are importance differences between the three implementations of the multilevel inverter in terms of the numbers of passive components and in aspects of their operation.

1) Multipoint-Clamped (MPC) Converter: Fig. 4 shows a converter that is known as either the MPC or diode-clamped converter [10]. This converter is essentially an extension of the neutral-point-clamped (NPC) converter [9] which is also known as a three-level converter. The clamp diodes operate across several voltage levels [14] and are normally composed of series connections of diodes (each rated at the same voltage as the main devices). Therefore, the number of clamp diodes for an N_L-level converter is: $N_D = (N_L - 1)(N_L - 2)$. The large number and difficult physical layout of the diodes makes a converter with a large number of levels unattractive [14], [15].

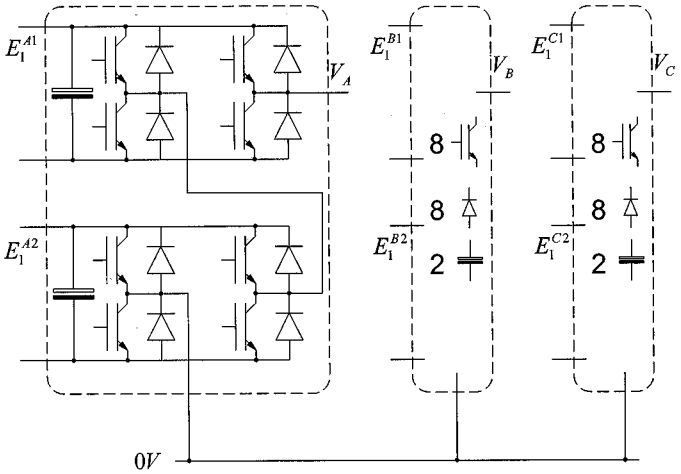

Fig. 5. Five-level two-cell chain inverter.

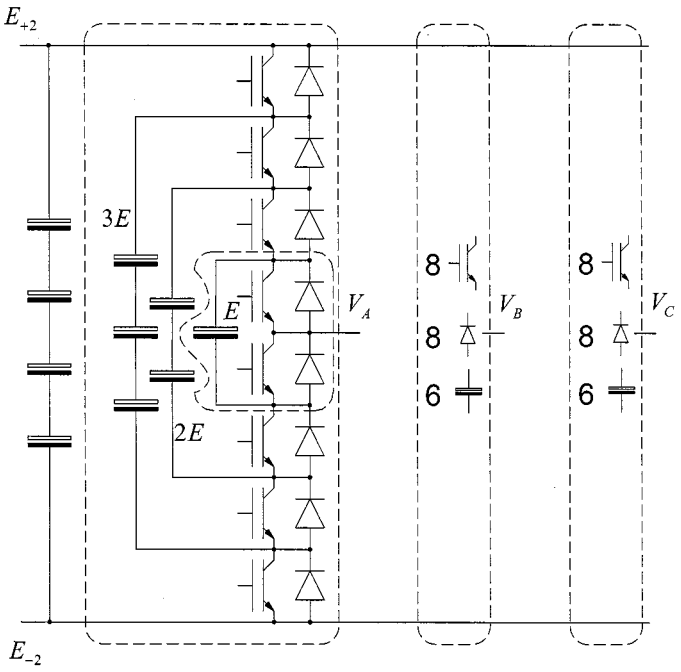

Fig. 6. Five-level nested-cell inverter.

2) Chain Converter: The multilevel technique can also be implemented in a series arrangement of standard H-bridge units [11], [14], [16], [17] as shown in Fig. 5. This is known as a chain or a cascade converter. Each H-bridge converter unit provides three voltage levels ($-E, 0, +E$). The total number of levels N_L that can be achieved using this configuration is $N_L = 2N_H + 1$, where N_H is the number of H-bridges in series arrangement. (There are four switches per H-bridge, $N_{S/P} = 4N_H$.)

3) Nested-Cell Converter: The nest cell converter is also known as the flying capacitor converter and is shown in Fig. 6. Each cell consists of a pair of switches (one upper and one lower operated as complements) and a capacitor that is not referenced to the dc bus [12], [14]. The capacitors are charged to a multiple of E that is one different from the adjacent cells. The contribution of each cell to the output voltage is E when

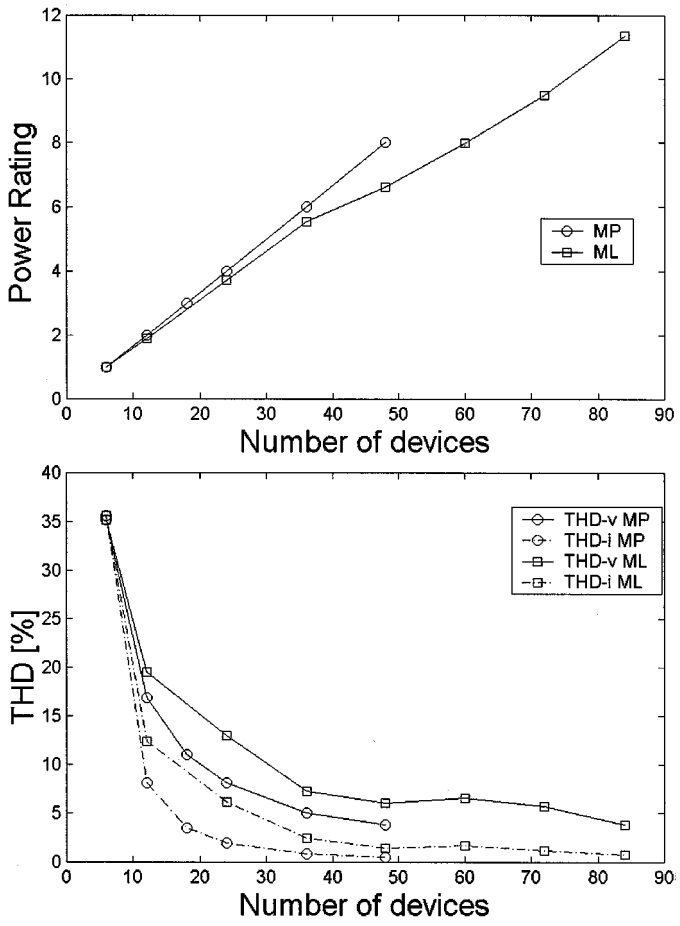

Fig. 7. Power rating, THD of the line voltage, and THD of the line current versus number of switches.

upper switch is on and zero when the lower switch is on (this view considers the output voltage to be offset by minus half the total bus voltage). If capacitors of the same voltage rating as the switches are used then series connection is required to support the voltages of the outer cells.

III. Power Rating, Harmonics, and Device Requirements

Fig. 7 shows how the power rating of a converter increases with number of semiconductor devices used. The power ratings are normalized to the power rating of a standard six-pulse converter. It has been assumed that the basic converter unit in a multipulse configuration uses a single device per switch and that a single device per level is used in the multilevel case. No distinction is necessary between the three types of the multilevel converter because they can produce the same waveforms and require the same number of switches. The clamp diodes of the MPC are considered as a special requirement of that converter and not included in the comparison at this stage.

A multipulse converter formed of $6N_P$-pulse converter units has a power rating of N_P times that of the six-pulse unit and requires a total of $6N_P$ switches.

The power rating of the multilevel converter is slightly lower than multipulse case. As the waveshape of the multilevel converter is refined by adding more levels, the peak of the fundamental is brought close to half of the sum of the DC voltages. The commutation angles were set to maximize the fundamental voltage amplitude and to eliminate as many low-order harmonics as possible. In contrast, the square waveforms in each unit of the multipulse converter produce a fundamental voltage amplitude greater than half of the dc voltage, $E/2$. The distortion that must be present to allow this is cancelled later.

The total harmonic distortion (THD) in the line voltage has been calculated and also shown in Fig. 7. The assessment of harmonic current distortion was with the converter connected to an infinite bus via a reactance of 0.15 p.u.. The multipulse converter has a superior THD to the multilevel converter for a given number of devices. Each addition of four switches per phase allows two levels to be added to the multilevel waveform. The extra degree of freedom can set one more harmonic voltage to zero. In contrast, 12 more switches in a multipulse converter will provide 12 extra pulses and allow four more harmonics (and related higher multiples) to be cancelled. Therefore, for a given power, both topologies will require the same number of switches but if they are arranged in a multipulse configuration a lower THD can be achieved.

The transformer complexity (and issues such as avoidance of saturation in transient state) is a major penalty of multipulse converter and so pulse number may be kept low and some switches place in simple series in order to achieve a given power rating. Thus, 24 switches could be used for a 24-pulse converter or they could be connected in series pairs for a 12-pulse converter. The THD of lower pulse number arrangement will not be as good. The same 24 switches could implement a five-level converter that would have a comparable THD to the 12-pulse converter. The multilevel and multipulse topologies, viewed on the basis of THD per circuit complexity will be closer than suggested by Fig. 7.

IV. Capacitor Sizing

Ratings of the dc-link capacitor bank of a voltage source converter may have a significant impact on the cost and physical size of a FACTS controller. The capacitor is sized for a specified ripple voltage, typically 10% of the nominal voltage. Deviation of the voltage compromises the voltage rating of the semiconductor switches and causes a modulation of the synthesized sine wave that may inject noncharacteristic low-order harmonics [18], [19]. The penalty for making the capacitor large is cost and physical volume. The STATCOM mode of operation (i.e., current and voltage in quadrature) yields the highest ripple current in the capacitor and hence the highest voltage ripple. This mode was used as the test case for the assessment of capacitor size.

The equivalent reactive power has been suggested [19] as a measure of the dc filter requirements in multipulse converters. A similar approach has been used in here. This measure is equivalent to that obtained by evaluating the total stored energy in the capacitor bank if normalized to the total stored energy of a three-phase capacitor bank derived from the rated values of the converter. The advantage of this measure is that it can also be related to the power rating of the converter. An equivalent capacitor obtained from the total stored energy and rated at the

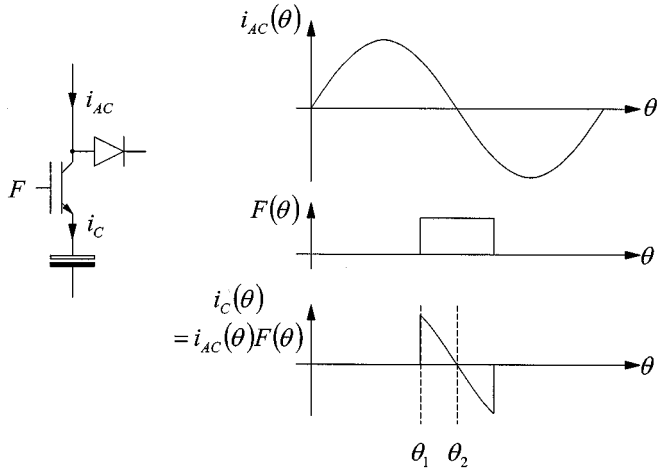

Fig. 8. Relationship between switching function and capacitor current.

total dc-link voltage has also been used to compare capacitor requirements [20].

For each topology a relationship can be established between the dc-side (i.e., capacitor) current, the switching function F_S, and the ac-side current $i_{\rm AC}$, as illustrated in Fig. 8. Assuming a sinusoidal ac-side current, the change in capacitor voltage, ΔE, can then be found by integrating the capacitor current

$$\Delta E = \frac{I_{\rm AC}}{\omega_L C} \underbrace{\int_{\theta_1}^{\theta_2} \sqrt{2}\sin(\theta) F_S(\theta) \cdot d\theta}_{k_I} \tag{1}$$

where $I_{\rm AC}$ is the rms amplitude of the ac-side current (assumed to be a sinusoidal waveform).

The integral in (1) can be evaluated for each converter topology and for each switching function associated with that particular topology. This integral can be quoted as a current factor k_I and the capacitance defined for a given voltage ripple can then be calculated as

$$C = \frac{I_{\rm AC}}{\Delta E \omega_L} k_I. \tag{2}$$

The shape of the current waveform is crucial to the current factor. Those topologies, such as the multipulse, which share the capacitor between all three phases have no low-order current harmonic in the dc link, under balanced conditions and will require much less capacitance for a given voltage ripple. Under unbalanced (negative sequence) conditions, this advantage is lost.

The analytical expressions for the voltage deviation were checked against a time domain simulation in Simulink. A three-phase positive-sequence set of currents of rated amplitude and leading the voltage by 90° was injected into the model. Unbalanced operation was also tested for the multipulse and MPC converter by injecting negative sequence currents of rated magnitude. Various phase angles between voltage and current, φ, were tested for the negative-sequence case.

No distinction need be made between balanced and unbalanced operation for either the chain or the nested-cell converters because they are essentially single-phase circuits. For the case of the nested-cell converter, a slight increase in the capacitance of the one capacitor that is shared by all three phases will be required to support unbalance. This does result in an increase in the total stored energy but it is small.

A normalized voltage ripple $\Delta E'$ is introduced to account for the relationship between the dc-side and ac-side voltages for each topology

$$\Delta E' = \frac{\Delta E}{E} = \frac{\Delta E}{\sqrt{2} V_{\rm AC}} k_V \tag{3}$$

where $V_{\rm AC}$ is the rms amplitude of the ac-side fundamental voltage and $k_V = \hat{V}_{\rm AC}/E = \sqrt{2}V_{\rm AC}/E$. This voltage ratio will be referred to as the voltage utilization factor hereafter.

Combining (2) and (3), yields the required capacitance as

$$C = \frac{1}{\Delta E'} \cdot \frac{1}{\omega_L} \cdot \frac{I_{\rm AC}}{V_{\rm AC}} \cdot \frac{k_V k_I}{\sqrt{2}}. \tag{4}$$

For a series-reactive compensator, this equation can be applied directly. For a shunt controller, such as a STATCOM, which is connected via a series inductance or a transformer, the ac-side voltage will be different from the line voltage by the inductive voltage drop, (6)

$$\overline{V}_{\rm AC} = \overline{V}_{\rm AC\,System} - jX_S I_{\rm AC}. \tag{5}$$

In (5), $V_{\rm AC\,System}$ is the voltage at the PCC and X_S is the reactance of the series inductor, or the leakage reactance of the transformer, via which the STATCOM is connected to the line. The highest capacitor voltage, hence, converter voltage, occurs when the converter is used to inject rated current in the capacitive mode. In per-unit form, $V_{\rm AC} = V_{\rm AC\,System}(1 + X'_S)$.

For the MPC, the maximum of the voltage ripple occurs at a control angle of $\alpha = 30°$ both for balanced and unbalanced operation. The balanced case considered only a phase angle of $\varphi = 90°$. For the unbalanced case the highest ripple voltage occurs at $\varphi = -60°$, 0° and $+60°$.

For the chain converter, the highest voltage ripple occurs when the cell generates the maximum possible voltage contribution with a control angle of $\alpha = 0°$.

For the case of the nested-cell converter, the highest voltage ripple occurs with the maximum control angle difference between adjacent cells. In general, the angle difference and hence the required capacitance for each cell, reduces with increasing number of levels. However, the number of cells also increases with the number of levels. The two factors approximately cancel and the overall capacitor rating does not change significantly with number of levels. For the assessment presented here, a five-level nested-cell converter was used as an example case and it is considered to be representative for converters using a higher number of levels.

In Table I the number, N_c and rating of capacitors (capacitance and stored energy) for each converter are compared. Each capacitor is chosen to support a nominal voltage of E. This is the natural requirement for the multipulse, MPC, and chain-cell converters. The nested-cell converter uses capacitors of voltage nE, with $n = 1, \ldots, N_L - 1$, but here (and in Fig. 6) it is assumed that they are implemented by series connection of n capacitors of voltage E. As noted in Section III, the multipulse converter makes better use of the available capacitor voltage

TABLE I
NUMBER OF BASIC CAPACITOR UNITS (OF VOLTAGE E), VOLTAGE UTILIZATION FACTOR, CURRENT FACTOR, REQUIRED PER-UNIT CAPACITANCE OF EACH CAPACITANCE, AND TOTAL STORED ENERGY FOR BOTH POSITIVE- AND NEGATIVE-SEQUENCE CURRENT. RESULTS ARE FOR 10% RIPPLE IN A STATCOM CONNECTED VIA A 0.15-P.U. INDUCTIVE REACTANCE

			Positive Sequence Case		
	N_C	k_V	K_I	C'	E_C' (=Q')
Multi-Pulse	1	$(2/\pi)/N_p$	$0.190/N_p$	0.74	$0.807/(N_p)^2$
MPC	$(N_L\text{-}1)$	$\approx 0.5/(N_L\text{-}1)$	0.707	$2.17(N_L\text{-}1)$	3.833
Chain-Cell	$3/2\times(N_L\text{-}1)$	$\approx 1.0/(N_L\text{-}1)$	1.414	$4.35(N_L\text{-}1)$	11.500
Nested-Cell	$(N_L\text{-}1)+3/2\times(N_L\text{-}1)(N_L\text{-}2)$	$\approx 0.5/(N_L\text{-}1)$	0.598	7.36	17.846

	Negative Sequence Case		
	$k_I^{(-)}$	$C^{(-)}{}'$	$E_C^{(-)}{}'$ (=$Q^{(-)}{}'$)
Multi-Pulse	1.414	$5.53N_p$	6.020
MPC	2.495	$7.52(N_L\text{-}1)$	13.267
Chain-Cell	-	-	-
Nested-Cell	-	-	-

than the multilevel converter. The third column in Table I gives the utilization factor K_V for each style of converter.

Each capacitance has been normalized using a capacitance base C_{base} derived from the impedance base Z_{base} and the frequency of the ac system

$$C' = \frac{C}{C_{\text{base}}} \quad C_{\text{base}} = \frac{1}{\omega_L Z_{\text{base}}} \quad Z_{\text{base}} = \frac{3V_{\text{AC System}}^2}{S_{\text{Rated}}} \tag{6}$$

where S_{Rated} is the rated apparent power of the STATCOM which is assumed to be rated at a voltage equal to the line voltage $V_{\text{AC System}}$.

The sixth column in Table I records the total stored energy of all the capacitors in the converter. This has been normalized using the base capacitance and the peak ac-side voltage $\hat{V}_{\text{AC System}}$

$$\begin{aligned} E_C' &= \frac{E_C}{E_{C\text{base}}} \\ E_{C\text{base}} &= \frac{3}{2}C_{\text{base}}\hat{V}_{\text{AC System}}^2 = 3C_{\text{base}}V_{\text{AC System}}^2 \\ E_C &= N_C\frac{1}{2}CE^2 = N_C\frac{1}{2}C\frac{V_{\text{AC}}^2}{k_V^2} \\ E_C' &= N_C\frac{C'}{6k_V^2}\cdot\frac{V_{\text{AC}}^2}{V_{\text{AC System}}^2} \\ &= N_C\frac{C'}{6k_V^2}\cdot(1+X_S')^2. \end{aligned} \tag{7}$$

For sinusoidal conditions, the reactive power of a capacitor can be defined by $Q = 3\omega_L CV_{\text{AC}}^2$ but also can be defined as the peak stored energy multiplied by the frequency $Q = \omega_L E_C$ (with $E_C = 3CV_{\text{AC}}^2$). Therefore, the dc-side capacitance can be discussed in terms of an equivalent reactive power if we assume that the stored energy was used in a sinusoidal system. Expressing the reactive power in terms of base quantities demonstrates that the per-unit reactive power is equivalent to the normalized stored energy

$$\begin{aligned} Q &= \omega_L E_C = \omega_L E_C' 3C_{\text{base}}V_{\text{AC}}^2 = E_C' S_{\text{base}} \\ Q' &= E_C'. \end{aligned} \tag{8}$$

Results in Table I shows that for operation with balanced (positive sequence) currents there is a significant difference in the capacitor requirements among the converters examined. In general, the capacitor rating, in the multipulse converter, is smaller than that of the converter and it decreases with increasing number of pulses. In contrast, in multilevel converters, the capacitor rating is almost independent of the number of levels and they are significantly larger than the VA rating of the converter itself (4–18 times depending on the converter). For operating condition involving negative sequence current components with rated magnitude, capacitor requirements, for the multipulse, MPC, and chain converters are similar, but nevertheless significantly smaller than that for the nested cell converter.

V. OUTPUT VOLTAGE CONTROL

In a STATCOM, the control of the converter output voltage is normally achieved by adjusting dc-link voltage [3], [18]. In turn, this is controlled by charging or discharging the dc-side capacitor by adjusting the phase angle of the output voltage so as to exchange real power with the ac system. Because this method involves only the phase shift of the switching pattern (and not adjustment of the control angles) it can be used in converters with fixed switching pattern such as a multipulse converter based on standard six-pulse units.

A STATCOM using converters where one degree of freedom is used to set the fundamental amplitude will work with a constant dc-side voltage that is sufficiently high to produce any normal ac-side voltage. This virtually eliminates the dynamics of the dc-side capacitor from the reactive power control loop and improves the dynamics of the STATCOM. A relatively slow control loop that sets the real power exchange of the converter can be used to maintain a constant dc-link voltage.

A multipulse converter can be operated with a constant dc-link voltage and still vary the ac-side output voltage. In [21], the system was altered so that it was composed of two multipulse converters operated with an adjustable phase shift between them to control the fundamental amplitude. A similar approach is used in the 80-Mvar STATCOM reported in [2], but in this case, instead of using a pair of converters, the six-pulse units were formed by H-bridges. In the Inez UPFC [4], the six-pulse units use three-level MPC converters that can vary their voltage amplitude. In each case, the number of

switches needed for a given pulse number has doubled (but the power rating for a given number of switches is not affected). Thus, if multipulse and multilevel converters are compared with the stipulation that the ac-side voltage magnitude is to be controlled (with a constant dc-link voltage) then the advantage of multipulse in terms of harmonic performance per switch (Fig. 7) is reduced.

In a multilevel converter, the control angles offer some control over the amplitude of the fundamental. However, if low amplitude is required, then the highest voltage levels must be removed from the waveform. In the MPC, particular capacitors and switches are dedicated to particular levels and removing the levels means that one control angle (an ability to control an harmonic) is lost. The chain cell converter is more flexible and any cell can be used for any control angle. Further, cells can contribute negative or positive voltage and so at low amplitude PWM-like output can be produced from line frequency switching [25] which provides better THD than the MPC. The nested-cell converter has redundant switch states, but these cannot be used to improve voltage quality at low amplitude because the cells cannot alternate their voltage contribution.

In a back-to-back configuration, variation of the control angles of the MPC may lead to a dc voltage imbalance since dc-link currents from one converter will not match the dc-link current of the other converter. This restricts the range of voltage control in back-to-back configurations (magnitude of converter voltages cannot be set to be too different) [22]–[24]. Back-to-back connection of nested-cell converters does not compromise the balance of the capacitor voltages.

A large range of voltage control can be provided by using two similar MPC units which are phase shifted (as in the case of multipulse converter [21] but needing only a simple transformer). Voltage levels need not be removed and therefore the THD is good. The method is suitable for back-to-back configurations such as that of the UPFC [24].

VI. Transfer of Active Power and DC Voltage Imbalance

The long-term exchange of active power with the ac system requires an energy source/sink on the dc side. This could be a generator or storage element but is normally a second power converter as in the case of the UPFC. In multilevel converters, the exchange of active power through the converter (i.e., from its ac to its dc side or vice-versa) compromises the maintenance of a constant capacitor voltages and, therefore, affects the operation of the converter. The variation or drift of the capacitor voltages has become known as dc voltage imbalance.

An MPC converter that transfers active power also has a power transfer between the innermost levels and the outermost levels of the dc link. To maintain dc voltage balance between all levels requires auxiliary converters to provide a compensating power flow between the capacitors of the link [10], [26], [27]. In MPC converters operated with PWM there is some scope for balancing using redundant states, but at full ac-side voltage magnitude this is not possible [26], [27]. In the case of two or more converters connected back-to-back and with balanced overall power flow, the power flow at each node can be balanced. This can be achieved by properly choosing the control angles of the converters [24], [28]. DC voltage imbalance due to transient conditions or pre-existing ac-side harmonics can be overcome by making small adjustments to the control angles [29]. Thus, the auxiliary converters are not needed (or at least can be made much smaller).

As shown in Fig. 5, the normal arrangement of the chain-cell converter is series connection of the ac sides of the cells which requires isolation of the various dc sides from each other. Thus, there is no direct way of implementing a back-to-back arrangement of two converters to form a UPFC. Isolated bidirectional dc–dc converters can be used to link the dc side of a cell in the first converter to one in the second. This is an additional conversion stage and, therefore, may require twice as many switches as the other configurations considered here. The alternative is to provide isolation on the ac side of the cells but this requires individual transformers for each cell. This arrangement has been used to implement cycloconverters, rated at power levels as high as 100 MVA, for railway applications [30]. However, this approach may involve higher power losses than that allowed in FACTS applications where transmission of electricity is the end product.

Even if no power transfer is intended through a chain-cell converter, a small real power exchange will be necessary to compensate power losses and maintain the overall dc-side voltage level constant. This power exchange will be uneven across the cells because it is dependent on the control angle of each cell. The control angle duties can be rotated around the various cells over several line-frequency cycles in order to balance the individual cell voltages.

The nested-cell converter has a number of redundant switch states. This can be exploited to maintain the capacitor voltages constant and balanced. The switching pattern used to determine the capacitor ratings in Section IV was chosen so as to minimize the time during which the capacitor carries current thus minimizing the effect of ripple current. It is also important to cancel the dc component of capacitor current when the converter is operated with voltage and current in quadrature for STATCOM applications. To enable the exchange of active power, the devices can be switched, at every cycle, according to different commutation angle so that the average current through each capacitor, over a certain number of cycles, is zero. In steady state, this could be accomplished, for example, by rotating the position of the switching pattern used to control the switches in the STATCOM case.

VII. Discussion

This section is devoted to present a summary of the main characteristics of each multilevel converter together with the FACTS application areas for which it is most suitable.

The dominant factors in determining which converter topology to use in FACTS controller are as follows:

- whether or not real power is to be transferred (and how this affects voltage balance);
- whether ac-side voltage control needs to be independent of dc-side voltage (i.e., modulation depth control);

- size of the dc-side capacitor required for the balanced and unbalanced current flow;
- overall complexity of the converter.

A. MPC Converter

As the number of levels of an MPC converter increases, the number of diodes grows as the square of the number of levels and their layout becomes complex. This may limit the number of levels of practical MPC converters to five or seven levels. To further reduce harmonic distortion to permissible levels, a number of these five- or seven-level units can be combined via magnetic coupling in a multipulse. Exchange of active power through the dc link is possible in back-to-back configuration of the MPC converter. This makes the MPC converter attractive for the implementation of a UPFC controller. However, a special configuration of MPC converters is required to provide independent control of both converter voltages.

B. Chain Converter

The topology of this converter is simple and, unlike the MPC and nested-cell converter, there is no escalating penalty in implementing a converter using a large number of levels. The synthesis of converter voltage is also less restricted than in the MPC and nested-cell converters. The dc-side capacitor required is large when compared to those of the multipulse and MPC converter under balanced conditions but not so if significant unbalance must be supported. The converter has a modular structure that can incorporate redundancy. The chain-cell converter is especially attractive for the implementation of FACTS controllers that do not involve the exchange of active power (which is difficult with isolated dc links) such as the STATCOM and SSSC.

C. Nested-Cell Converter

In terms of active power exchange and stability of capacitor voltages, the nested-cell converter is superior to the MPC and chain-cell converters. It allows simple back-to-back connection through a single dc link. In contrast, the MPC converter needs a dc-link connection for each level and the chain-cell converter does not allow direct connection. For line switching frequency operation, however, the realization of such capabilities may prove difficult and costly because of the large rating of the dc-side capacitor, even if its operation is restricted to STATCOM or SSSC.

VIII. Conclusions

This paper has shown that the power rating achieved increases linearly with the number of semiconductor devices and is independent of the topology used. The THD achieved by multipulse converters for a given number of levels is better than for multilevel converters but this advantage is lost if control of the ac voltage is to be made independent of the dc voltage.

In balanced (positive-sequence current) operation, there is a significant difference in the capacitor rating amongst the converters examined. The multipulse and MPC converter are at a significant advantage. However, if the converter must support significant negative sequence current then the capacitance rating of the multipulse, MPC, and chain-cell converters become similar. The nested-cell converter has the highest capacitor rating under all circumstances. The capacitor will have a large physical volume and will be a significant cost in the system.

Given a requirement for negative sequence current, the chain-cell converter is an attractive implementation for a STATCOM or SSSC. For a series controller, the chain-cell has the advantages of good waveform quality at low voltage magnitudes and variation of the voltage magnitude through fast-response switching angle control.

Back-to-back configuration to transfer real power through the dc link is required for the UPFC and IPFC. This is not directly possible with the chain-cell converter. It is possible with the multipulse, MPC, and nested-cell converters, but the voltage balancing of the multilevel converter needs to be addressed.

Promising use has been made of the multilevel converters in FACTS controllers but this should not overshadow the more well-established multipulse converter. The phase-shift transformer presents a considerable cost at high pulse number but it is a very effective method of cancelling harmonic components and enables a system to be built with a single relatively small dc-side capacitor.

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