A Systematic Approach to Process Selection in MEMS

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***Abstract*—A systematic approach is developed to select manufacturing Process Chains for the generic elements of a MEMS device. A database of MEMS Process Chains and their attendant process attributes is developed from an extensive review of the literature, and used to construct Process Attribute charts. The performance requirements of MEMS beams and trenches are translated into the same set of Process Attributes. This allows for a screening of the Process Chains to obtain a list of candidate manufacturing methods. This method is illustrated in a brief design example. [1202]**

I. Introduction

THE design of any mechanical device requires knowledge of the constraints imposed by material properties and manufacturing processes. In microelectromechanical systems (MEMS) the currently available set of manufacturing processes is much smaller than that for traditional mechanical design, and they impose limits on achievable dimensions, tolerances and performance. At present, the selection of materials and processes in MEMS is often done heuristically using processing capabilities available "in house," rather than by a systematic approach that considers all possible materials and fabrication routes. In the current state of micromechanical design, this may be acceptable, particularly as the introduction of new materials and processes carries a cost penalty. However, as the number of materials and processes available for microfabrication increases, a more systematic approach to material and process selection is needed to avoid cost penalties associated with changing fabrication plans at later stages in the design process. The present study outlines a design tool for the selection of MEMS fabrication routes, both to help the designer and to educate the student.

A major difference between traditional manufacturing processes and microfabrication lies in the level of complexity of shape that can be achieved. In the manufacture of macroscale devices, complex three-dimensional (3-D) shapes are routine. In microfabrication, almost all structures are defined by a combination of deposition, lithographic patterning and etching. Consequently, the complexity of shape is limited to projections of two-dimensional patterns, and most structures take on a limited variety of shape in the through-thickness direction. As a result, most MEMS structural elements can be broadly classified as *beam* or *trench* structures. In this broad classification beam includes the beams and plates of macro design, and trench refers to fully enclosed channels and can also define pillars or post structures. Fabrication is generally achieved by a sequence of steps using different technologies and procedures, rather than a single manufacturing process. Understanding these *Process Chains* is of the greatest importance for MEMS design.

The strategy adopted here is to construct a database of MEMS Process Chains, and to ascribe to each chain a set of process attributes. A general framework has been developed by Ashby [1], [2] for process selection, and this is adopted here. In the language of biological classification, the *kingdom* of manufacturing processes for MEMS beams and trenches is divided into *families* (such as bulk micromachining). Each family contains *classes* (such as wet etch) and *members* (such as anisotropic wet etching of (100) Si using KOH). The members of this process kingdom are each quantified by a set of *attributes*, which include the materials it can process, the dimensions and tolerances of which it is capable and the processing temperature and pressure.

The database is used for process selection via the strategy illustrated in Fig. 1. The performance of the planned MEMS design is *translated* into a set of desired feature-attributes such as material, shape, dimensions, precision etc drawn from the list used to characterize the Process Chains. The library of Process Chains is then *screened*, rejecting those incapable of making the desired feature from the desired material, with the desired dimensions and precision, leaving a subset of candidates that could be used to manufacture the MEMS device. Screening is done either manually using process selection maps or done electronically using an appropriately constructed database and software tool, such as the CES[1] Constructor and Selector system. The screened subset of processes are then *ranked*, using approximate economic criteria, the most obvious of which is time. The final step is to search for detailed *supporting information* for the top-ranked candidates, allowing an in-depth comparison of their relative merits; this step is beyond the scope of the present study.

The outline of the paper is as follows. The process selection methodology is reviewed. A reduced set of geometric and material *attributes* is ascribed to MEMS components in the form of beams and trenches. Process selection charts are constructed for currently available MEMS processing routes and their use is illustrated in a design example.

II. MEMS Process Selection Attributes

An appropriate set of Process Attributes must first be identified in order to construct a library of MEMS Process Chains. The discriminating attributes for MEMS identified here include

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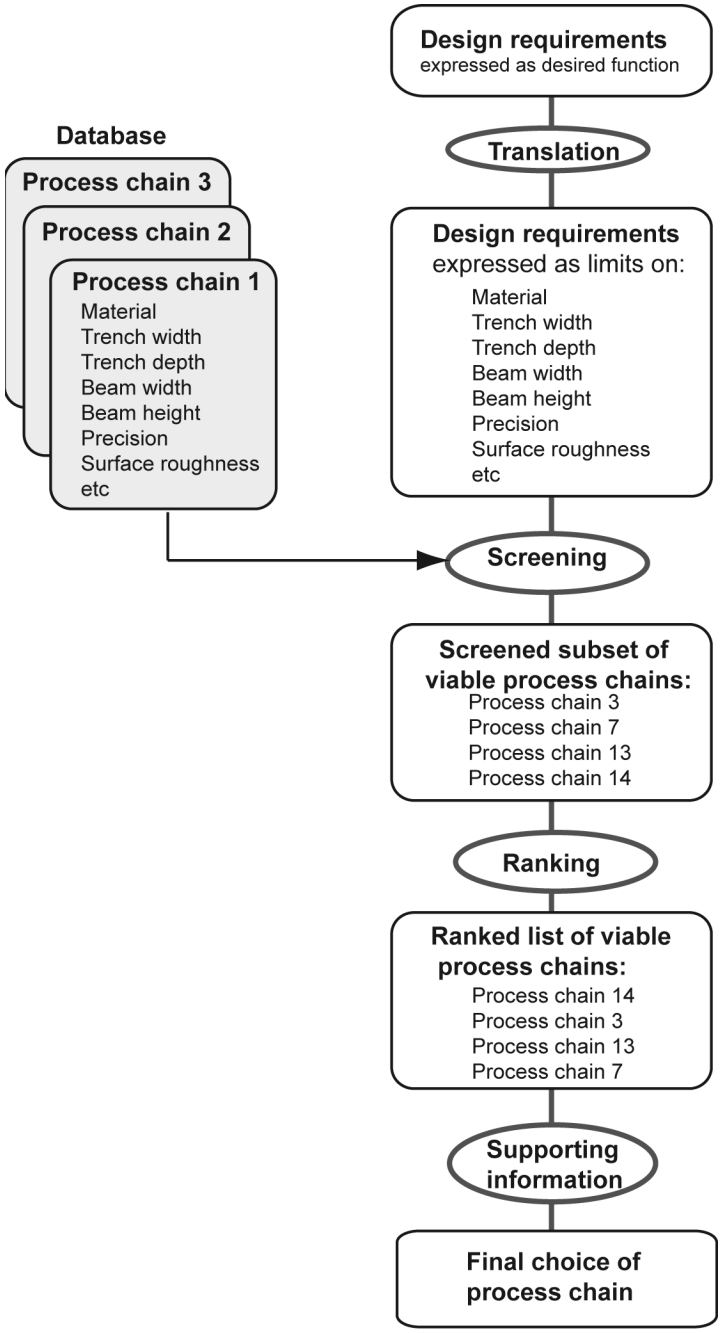


Fig. 1. Flow chart for process selection scheme.

material, shape (including tolerance and surface quality), and processing temperature and pressure.

A. Material Attributes

Until recently, the set of candidate materials for MEMS has been relatively limited and centred on silicon, Si [3]. As the set expands, it becomes important to identify the spectrum of materials which can be processed by each Process Chain [4]. Furthermore, in any MEMS fabrication sequence, several materials are used sacrificially. For example a material may be deposited and then etched away later in the sequence of process steps. To address this, one can classify a material used in a fabrication sequence as either *primary* or *secondary*. A primary material is the main structural material used, while secondary materials either no longer exist in the device after completion of the fabrication sequence or serve a nonstructural purpose, such as metallization or insulation layers.

B. Shape, Tolerance, and Surface Attributes

A number of geometric attributes can be ascribed to the beam or trench. They include the in-plane leading dimension w, the out-of-plane height h, the achievable tolerances Δw and Δh, and the root-mean square surface roughnesses R_w and R_h. This set of attributes is shown in Fig. 2 for the beam and in Fig. 3 for the trench; they are also listed in Tables I and II. The relative importance of each attribute varies from application to application. For example, the roughness R_w is particularly important in

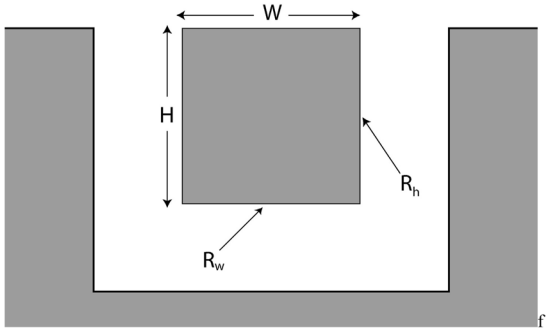


Fig. 2. Beam geometry. For the purposes of this paper the key dimensions of a beam are its width and height, and the tolerances associated with them.

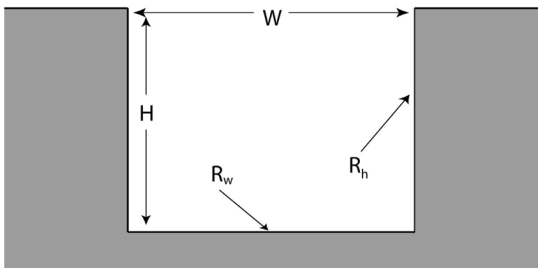


Fig. 3. Trench geometry. For the purpose of this paper the key dimensions of a trench are its width and depth and the tolerances associated with them.

TABLE I
GEOMETRIC ATTRIBUTES OF BEAM

BEAM - Geometric and Surface Attributes	
Dimension	**Description**
w	Beam width
Δw	Tolerance on beam width dimension (+/-)
R_w	In-plane rurface roughness of beam (RMS)
h	Beam height
Δh	Tolerance on beam height dimension (+/-)
R_h	Out of plane / wall roughness of beam (RMS)

TABLE II
GEOMETRIC ATTRIBUTES OF TRENCH

TRENCH - Geometric and Surface Attributes	
Dimension	**Description**
w	Trench width
Δw	Tolerance on trench width dimension (+/-)
R_w	Roughness of trench bottom (RMS)
h	Trench height
Δh	Tolerance on trench height dimension (+/-)
R_h	Roughness of trench sidewall (RMS)

the design of mirrors and in the avoidance of stiction [5]–[11]. These geometric features of the beam or trench structure are also process attributes and their achievable values depend upon the Process Chain employed.

C. Processing Attributes

A number of processing attributes dictate the subsequent performance of a part. For example, the maximum processing temperature has an effect upon the subsequent operating temperature. Here we include as representative process attributes the maximum processing temperature and the minimum processing pressure. These two parameters, in conjunction with knowledge of primary and secondary materials, can help serve as a cost indicator and help in the development of full device fabrication process flows as they help establish the compatibility of process chains.

In macroscale manufacture, it is usually the economic attributes of a process that ultimately distinguish it for selection over other processes with similar capabilities [1]. This is also true to a large degree in MEMS design, as the value of MEMS devices frequently lies in their ability to be mass-produced, such that large capital investments can be written off over time. However, the work presented here has focused on a preliminary evaluation of systematic process selection routines and tools based on performance attributes, not on their economics, for which reliable data are difficult to determine. Thus, no direct cost attributes are developed in the current study.

III. THE CONSTRUCTION OF PROCESS ATTRIBUTE CHARTS

A literature survey has been conducted to construct a representative set of Process Chains for MEMS structures. These fabrication sequences, along with a summary of the process flow and primary references, are listed in Table III. The geometric and processing attributes of these Process Chains have been assembled from the literature and stored in an electronic database. In cases where the data are sparse, estimates have been made from a knowledge of physical limitations and of the capabilities of similar processes. It is helpful to display these data in charts using process attributes as axes. The charts are of direct use in matching the requirements of beam and trench structures to a candidate set of Process Chains.

A. Dimensions

Fig. 4 presents the range of achievable out-of-plane (height) and in-plane (width) dimensions of microfabricated beam and trench structures. Minimum achievable dimensions are important for determining the compactness, natural frequency and thermal time constants of devices and can determine the sensitivity limits for sensors and actuators. In some cases upper limits on fabricated dimensions can also be important, particularly when deep etched features or thick deposited layers are required for high force or power applications. Where there is not a well-defined upper limit for a particular dimension, a nominal upper limit of 1mm has been used.

A high degree of overlap of processing capabilities is evident for the width dimension of both beams and trenches. This dimension is generally dictated by lithographic limits. LIGA, and soft-lithography processes such as Nano-imprint lithography (NIL) and replica molding (REM), are outliers on the h versus w plots because they use high resolution lithographic technologies such as X-ray and E-beam lithography. The deep etch, shallow diffusion process is limited by the width across which one can boron dope silicon by diffusion [26], [29].

The upper limits on the out-of-plane dimensions for both beam and trench structures are limited by practical limits of the etching or deposition processes. When deposition defines the out-of-plane dimension, as with surface micromachining, the upper limit is set by the ability of the structural material to be deposited without significant degradation of film quality, and without excessive residual stress [6], [7]. This limitation has

TABLE III
PROCESS CHAINS

Process Chain Family		Process Chain Name	Fabrication Sequence Summary	Primary Material	Secondary Material(s)	References
Bulk Micromachining	Wet Etch	Anisotropic Wet Etching of (100) Si - KOH	Deposit mask material; pattern; etch; remove mask material (if desired)	Si	SiO_2, SiN	[8, 12-22]
		Anisotropic Wet Etching of (110) Si - KOH	Deposit mask material; pattern; etch; remove mask material (if desired)	Si	SiO_2, SiN	
		Anisotropic Wet Etching of (100) Si - TMAH	Deposit mask material; pattern; etch; remove mask material (if desired)	Si	SiO_2, SiN	
		Anisotropic Etched Beam in (100) Si - KOH	Deposit mask material; pattern; underetch / release beam	SiN	Si	[8, 12-21, 23-25]
		Anisotropic Wet Etching of (100) Si - EDP with P++ Etch Stop	Thin wafer; boron diffuse and drive in; define mask and pattern; etch	Si	SiO_2, SiN	[5, 8, 9, 12-14, 16, 17, 19, 26-29]
	Dry Etch	Anisotropic Dry Etching (RIE) of Si - Metal Mask	Deposit (electroplate) metal mask and pattern; RIE; remove mask	Si	Metal (Ni)	[5, 8, 9, 12-14, 16, 17, 22, 24, 26, 30-35]
		Deep Etch, Shallow Diffusion Process	Deposit mask material; RIE; boron diffuse; short RIE; release OR bond to glass, thin and release	Si	Metal (Ni)	[5, 8, 9, 12-14, 16, 17, 22, 24, 26, 28, 29, 31, 34, 35]
		Dissolved Wafer Process	Etch anchor recesses; boron diffuse and drive in; pattern structure; etch recess in glass; bond Si wafer to glass; thin wafer; EDP etch	Si	Glass	[5, 8, 9, 12, 28, 34]
		SCREAM - Si (Thick Oxide Mask)	Short thermal oxidation and pattern; RIE; long (thick) thermal oxidation; RIE; thermal oxidation of sidewalls; deposit metal; deposit resist; isotropic release etch	Si	SiO_2	[5, 8, 9, 12, 25, 34, 36-42]
		SCREAM I - Si (Deposited Oxide Mask)	Deposit mask oxide and pattern; long RIE; deposit sidewall oxide; short RIE; long RIE; isotropic release etch; deposit metal	Si	SiO_2	[5, 8, 9, 12, 25, 34, 36-43]
		SCREAM II - GaAs	Deposit nitride mask and pattern; RIE; deposit nitride layer; deposit metal; spin on resist, bake and remove; RIE exposed metal; RIE nitride; isotropic release etch	GaAs	SiN	[5, 8, 9, 12, 25, 34, 36-43]
		Deep Reactive Ion Etching (DRIE - Bosch Process)	Deposit mask and pattern; short isotropic etch (SF6); passivate sidewalls (C4F8); repeat to desired depth	Si	C_4F_8	[8, 30, 32, 44-48]
		Trilayer Mask Dry Etch Process with Thermal Oxidation Finishing	Deposit mask layer #1 (metal); deposit mask layer #2 (resist and bake); deposit mask layer #3 (metal); pattern trilayer mask (RIE); RIE; thermal oxidize sidewalls; isotropic wet (finishing) etch of sidewalls	Si	Ni, SiO_2	[5, 8, 12, 13, 32, 36, 49]
Surface Micromachining		Polysilicon Surface Micromachining	Deposit isolation layer (if desired); deposit sacrificial layer (densification bake if necessary); open up anchors in sacrificial layer; deposit structural (polysilicon layer) and anneal (if necessary); pattern structure (RIE); wet isotropic release etch of sacrificial layer	PolySi	PSG, SiO_2	[7, 8, 11, 12, 34, 37, 50-53]
		Silicon Carbide Surface Micromachining	Deposit isolation layer (if desired); deposit sacrificial layer; open up anchors in sacrificial layer; deposit structural (Silicon Carbide); pattern structure (RIE); wet isotropic release etch of sacrificial layer	SiC	Si, PSG, SiO_2	[7, 8, 11, 12, 34, 37, 50, 51, 54-58]
		Polyimide Surface Micromachining	Deposit isolation layer; deposit sacrificial layer; spin-on thin polyimide layer and partial cure; deposit conductor layer (if necessary); alternate spin casting and soft baking for remaining structural depth; final cure; deposit metal mask and pattern; plasma etch; isotropic release etch	Polyimide	PSG, SiO_2	[7, 8, 11, 12, 34, 37, 50, 51, 59-61]
		Multilayer Polysilicon Surface Micromachining (Sandia SUMMIT / SUMMIT V)	Deposit buffer/isolation layer; deposit sacrificial layer; deposit structural (polysilicon) layer; planarize using CMP; repeat to desired height up to 5 structural layers; wet isotropic release structure	PolySi	PSG, SiO_2	[7, 8, 11, 12, 34, 37, 50-53, 62]
Soft Lithography Processes		E-beam Defined, Hard Master Mold Making (Nano-scale Molds)	Thermal oxidize layer and pattern (e-beam); RIE	Si, SiO_2	SiO_2	[8, 12, 24, 43, 63-67]
		Micro-contact Printing (μCP)	Ink master stamp with pattern material; transfer patter to target material (press); use pattern as etch or deposition mask (if desired)	"Inks" (polymers, SAMs etc.)	PDMS (Master Material)	[8, 63, 64, 68]
		Micro-molding in Capillaries (MMIC)	Press PDMS master mold against target substrate; insert liquid polymer via capillary action and cure; remove mold	Polymers	PDMS (Master Material)	[8, 63, 64, 66, 69, 70]
		Micro-molding in Capillaries (MMIC) - Vacuum Assisted	Press PDMS master mold against target substrate; insert liquid polymer via vacuum action and cure; remove mold	Polymers	PDMS (Master Material)	[8, 63, 64, 66, 69, 70]
		Micro Replica Molding (REM)	Cast and cure PDMS against hard master mold (Si, SiO_2, or SU8) and remove	PDMS	PDMS, SU8, Si (Master Material)	[8, 24, 63, 64, 66, 67]
		Micro Transfer Molding (μTM)	Fill master PDMS mold with liquid polymer; press / pattern against substrate; remove excess polymer and cure; remove mold	Polymers	PDMS (Master Material)	[8, 63, 64, 66, 67]
		Hard Master Embossing / Nano-Imprint Lithography (NIL)	Deposit polymer; imprint pattern into deposited polymer and cure; complete pattern transfer with RIE; deposit metal on patterned polymer and lift off	Polymers	SiO_2	[8, 63-65, 71, 72]
LIGA			Deposit thick resist layer (PMMA); X-Ray pattern and develop; electroplate metal and release	Metal (Ni)	PMMA	[8, 12, 73, 74]

been largely overcome for polysilicon structures by the Sandia SUMMIT process (multilayer polysilicon surface micromachining), where a proprietary low-stress deposition process, combined with intermediate planarization steps by chemical mechanical polishing (CMP) have been used to produce moderately thick structures, $h \approx 14\ \mu\mathrm{m}$ [62].

Virtually all etching used in microfabrication has a limiting height to width aspect ratio, as for a given width, there is a depth beyond which reaction products cannot be removed from the trench, thus halting the etch process. In fabrication sequences utilizing wet anisotropic etching of Si to define height dimensions, aspect ratio limits are dictated by the orientation of crystallographic planes [14], [17]. That is, when etching (100) silicon, etching is terminated on $\{111\}$ planes oriented at an angle of 54.74° to the $\{100\}$ planes; consequently, the maximum aspect ratios is less than unity.

Dry etching also produces a restricted aspect ratio due to the limited removal of reaction products and due to ion bowing: ions impact the side walls as etching proceeds. The aspect ratio is further limited by the durability of mask materials. The solubility of the mask material by the etchant not only limits the overall depth that can be achieved before the mask completely erodes but also limits the straightness of the sidewall: the mask material may become redeposited on the sidewalls of the etched features [8], [17], [22], [24], [31], [35].

The use of metal, trilayer resist and thick thermal oxide masks (as in SCREAM) allow for the highest aspect ratio of the dry etch Process Chains [42], [49], [75]. DRIE uses these same principles and repeated isotropic and sidewall passivation/protection steps to achieve not only a high aspect ratio, but also higher etch rates, thus allowing structures to be fabricated with dimensions comparable to the wafer thickness [47], [48], [76].

Limitations in aspect ratio can arise from physical effects in addition to the etching process. LIGA, for example, uses X-ray lithography to define the height of structures, and the aspect ratio limitations are attributed, in part, to diffraction of the X-ray beam [8]. In several soft lithography processes, such as nanoscale hard embossing (nano-imprint lithography—NIL) and replica molding (REM), the use of polymeric materials and moulds dictate minimum and maximum aspect ratios for patterns to be transferred with acceptable fidelity. The rheology of fluids in moulds and the deformation of master stamps overlarge surface areas limit the range of achievable aspect ratio [63], [64], [69], [77].

B. Tolerance

The $\pm$ amplitude of tolerances on height Δh, and on width, Δw, are important in the design of MEMS. The ability to manufacture to tolerances controls the precision and accuracy of the devices and also has economic consequences if subsequent "tuning"

or rework steps are required to compensate for poor tolerances. Tolerances, expressed as absolute dimensions, are plotted in the tolerance maps of Fig. 4 for the library of Process Chains.

Typically, the lithographic step dictates the width tolerance. This is reflected in the Process Chains using high-resolution lithographic steps such as LIGA and various soft-lithography processes. In addition to lithography, one must consider the subsequent etch steps of the fabrication sequence. If the etch gives significant mask undercutting, the tolerance on the width dimension increases. This is reflected by the relative width tolerance for anisotropic wet and dry etch based processes: the occurrence of mask misalignment and crystallographic etching in wet etch based processes leads to a greater width tolerance than anisotropic dry etch based processes, assuming the use of durable mask materials in the dry etch process [8], [14], [17]. Similarly, in DRIE, isotropic dry etching gives mask undercutting and a consequent increase in width tolerance [35].

Several soft lithography processes involve the casting and curing of polymers in a moulding or stamping process. The resulting shrinkage and expansion by 1–3% contribute to the tolerances that can be held in the in-plane dimensions [63], [64], [77]–[79].

Tolerances in the height dimension are generally dictated by the etching or deposition processes used in the fabrication sequence. Where deposition steps define the height of a structure, as in surface micromachining, the out-of-plane dimension can be controlled down to nanometer level. Poorer tolerances are achieved by multilayer surface micromachining where the tolerance on the out-of-plane dimension is cumulative over multiple deposition steps, and by polyimide surface micromachining where the use of spin casting is less accurate than other deposition techniques [59], [60].

Next, consider a structure of height dictated by a single etch step. Structures whose height is defined by a single etch step generally have tighter tolerances using dry etching than wet etching. In standard anisotropic wet etch processes, even if one has accurate control over the concentration, stirring and reactant removal, it is difficult to control the depth of etch to better than 10% of the nominal depth [17]. This is unacceptable when making structures requiring depths of etch in excess of a couple of hundred microns, such as in the fabrication of thin membranes, where control of the thickness of the membrane is critical. Tighter tolerances on depth dimensions can be attained by anisotropic dry etching due to close control over the pressure, bias, gas flow and other process variables [22].

The use of an etch stop in wet bulk micromachining allows for a tight tolerance on the depth dimension, see Fig. 5. For example, a diffused and driven-in boron layer (p++ doped) can be used to define the depth of etch. This diffusion layer is largely resistant to EDP etching, allowing for depth control in the submicron domain [8], [28]. Other etch stop procedures, such as electrochemical and material stops, particularly buried oxide layers in silicon on insulator wafers, have a similar performance [17], [27].

C. Roughness

Fig. 6 presents Process Attribute maps for in-plane surface roughness and side-wall roughness, given as the root-mean-square (rms) values. Roughness is important for optical applications where reflectivity is required. High roughness is undesirable in tribological applications, but may be desirable if stiction is to be avoided. Roughness also plays a role in dictating the strength of the resulting structure. Again, the roughness characteristics are dictated mainly by the combination of etching and deposition used in each Process Chain.

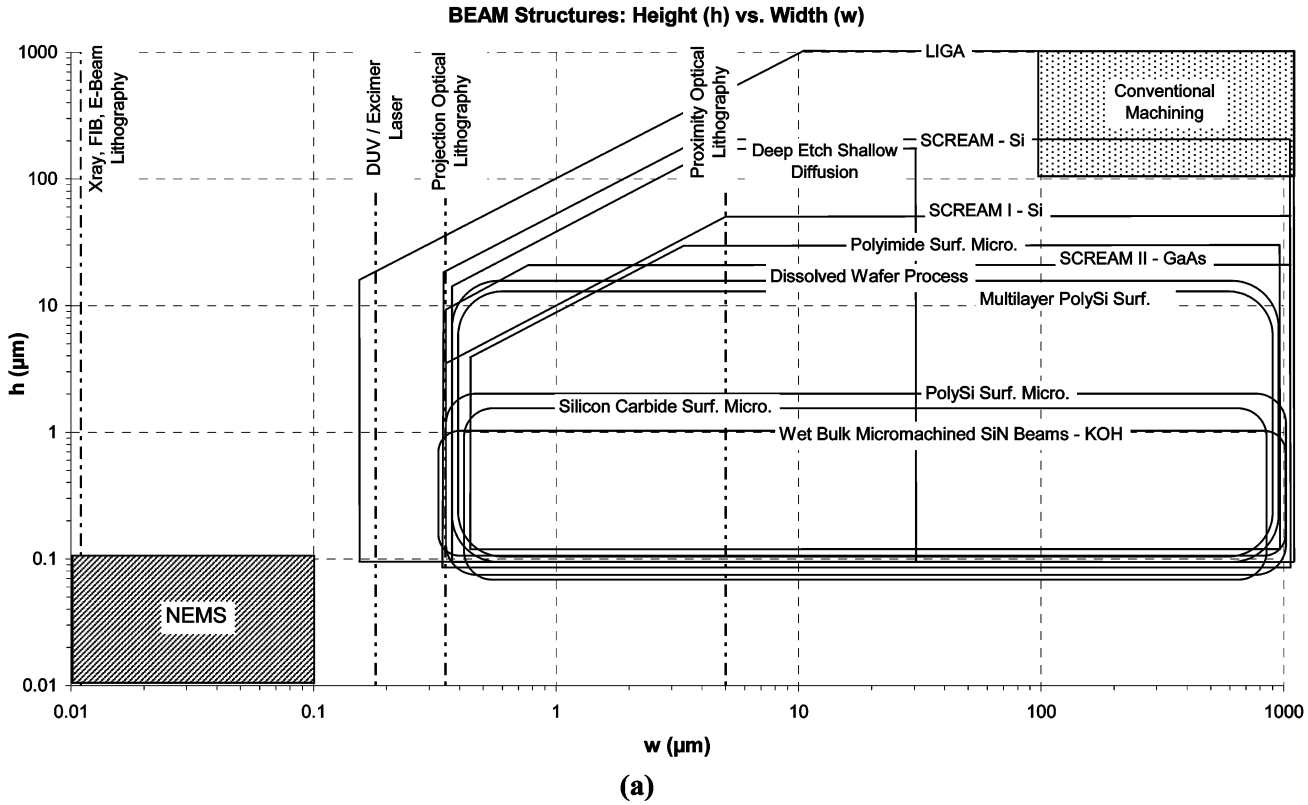
Dry etch processes have the potential for attaining very low surface roughness both in-plane and in the side-wall direction. An exception is DRIE, where the alternating etch and passivation steps creates a scalloping of the sidewalls and roughness up to the micron level [47], [48]. In anisotropic wet etching, the side-walls can be aligned with crystallographic planes and the resulting roughness can be of atomic magnitude. Wet etching also has the potential to leave extremely rough in-plane surfaces: the roughness of $\{110\}$ planes exceeds that of $\{100\}$ planes [15]. Improved surface roughnesses are achieved in doped silicon through the use of an etch stop or a deep etch shallow diffusion sequence.

The use of finishing steps to improve surface and side-wall roughness in Process Chains is included in Fig. 6. In-plane roughness can be improved dramatically by the use of CMP steps, as illustrated by multilayer surface micromachining. Another common technique for reducing both in-plane and sidewall roughness, shown here in combination with a trilayer resist mask dry etch process, is the use of an oxidation finishing step, where thermal oxidation followed by a wet etch dramatically reduces the roughness of the as-etched or oxidized surface [5], [19].

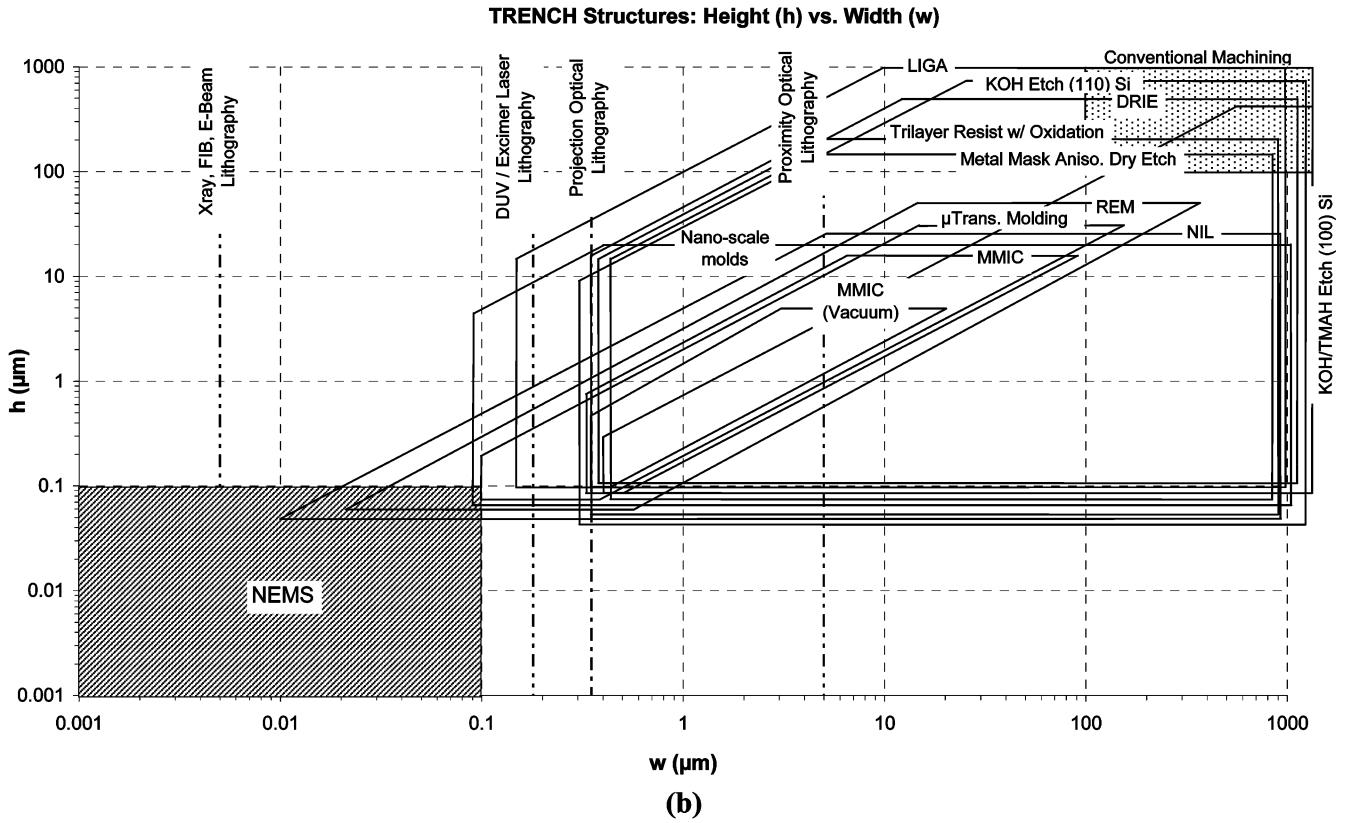
D. Pressure and Temperature

Fig. 7 presents a chart of the maximum process temperature versus minimum processing pressure for the MEMS Process Chains. These two parameters are important for several reasons. First, they are often indicative of the cost and time of a Process Chain, such as the capital cost of high temperature or vacuum equipment, and the time necessary to carry out high temperature or high vacuum steps. Second, these attributes allow the designer to discriminate between those candidate process chains that can be carried out "in-house" and those that must be outsourced for fabrication. This is an indirect cost indicator. And third, these parameters determine the compatibility of different Process Chains and materials. That is, if one wanted to fabricate a complete device using a series of Process Chains, compatibility can only be assured if the maximum temperature of the Process Chain considered does not exceed the melting temperature of the materials present in an early fabrication sequence. Similarly, one could not use a high vacuum fabrication sequence following a fabrication sequence that leaves potentially contaminating materials.

The maximum process temperature and minimum processing pressure also dictate whether these process sequences can be carried out on IC circuitry. The integration of mechanical and electronic subsystems is part of the more general issue of packaging, an important issue which must be addressed at the earliest stages of design [80]. Junction migration will occur at approximately 800 °C for shallow junctions. Thus, temperatures in excess of this limit should be avoided for integration with IC circuitry. In addition, aluminium and tungsten, common metals



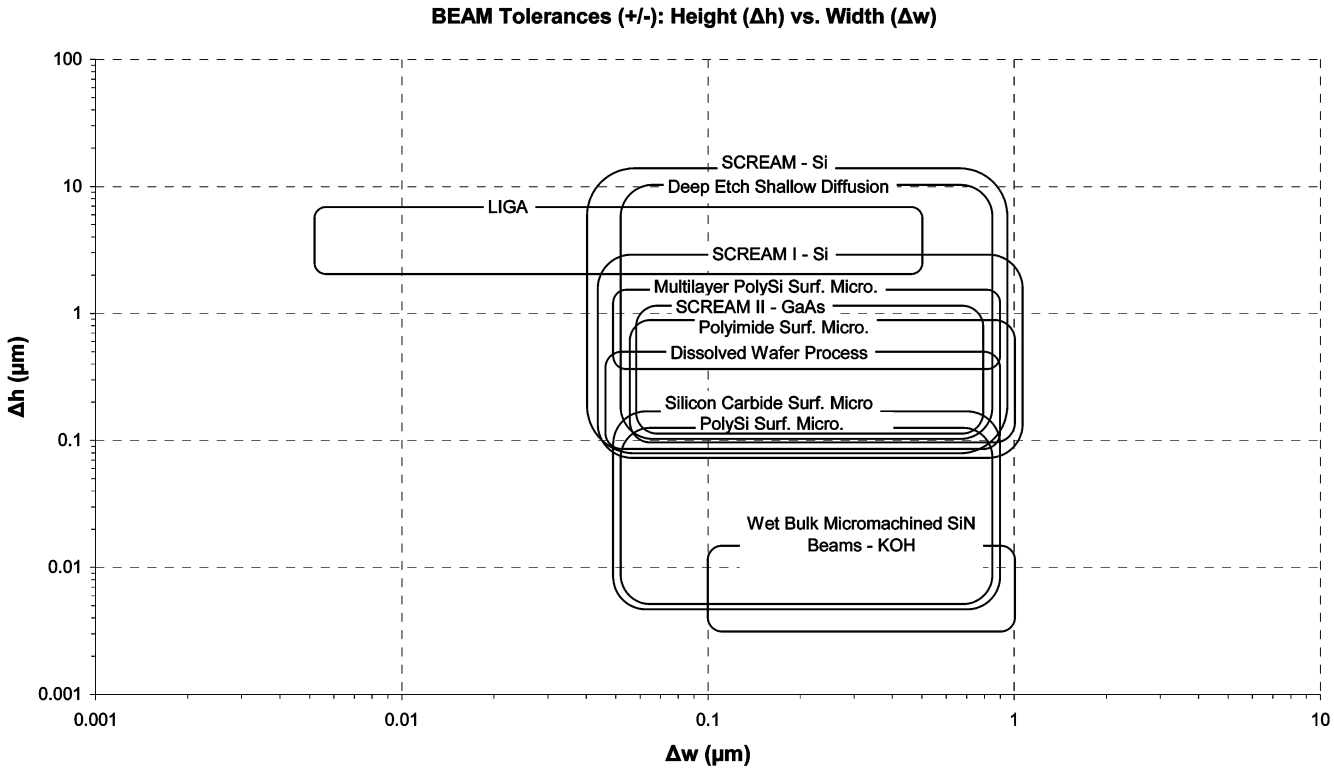
(a)



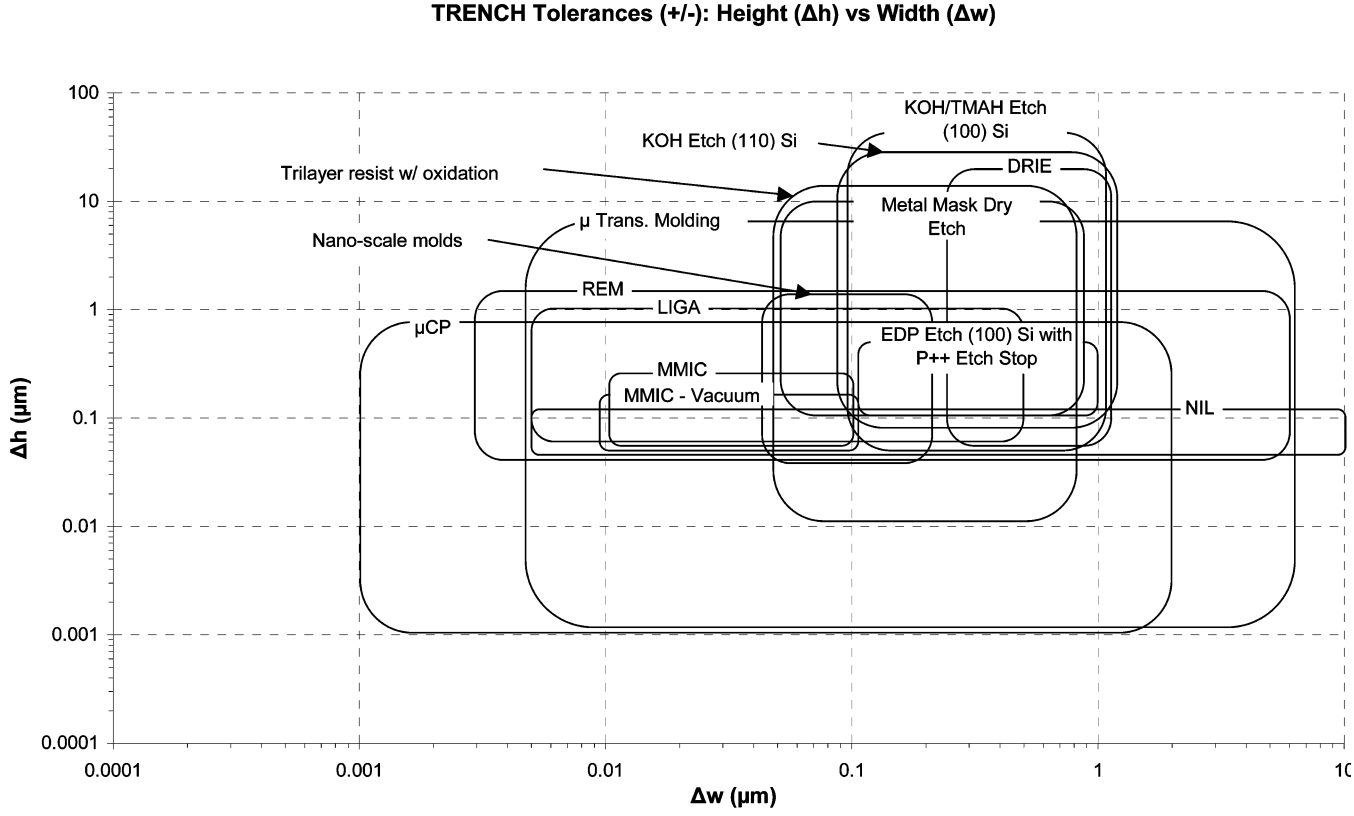
(b)

Fig. 4. Height versus width attribute charts for (a) beams and (b) trenches. The "envelopes" for each process chain are derived from the literature according to Table III. The height and width are arbitrarily limited to 1000 μm as a practical upper limit to microfabrication.

used in CMOS fabrication, generally begin to degrade when subjected to temperatures in excess of 400 °C and 600 °C, respectively. Thus, process chains that require temperatures in excess of these limits require careful consideration of the full fabrication sequence. Where high temperature steps, such as deposition and annealing steps, of a given process chain follow the IC fabrication steps, appropriate analyses must be performed to ensure that the integrated circuitry is sufficiently insulated.



(a)



(b)

Fig. 5. Height and width tolerance attribute charts for (a) beams and (b) trenches. This data is derived from the literature according to Table III.

IV. Applicaton of the Process Attribute Charts

How can the Process Attribute charts help in the design of a MEMS device? Conceptually, this is straightforward: upon translating device performance into a set of process attributes of each beam and trench, one can filter out the potential process sequences for use in fabrication. A detailed search for support information is then used to rank the list of

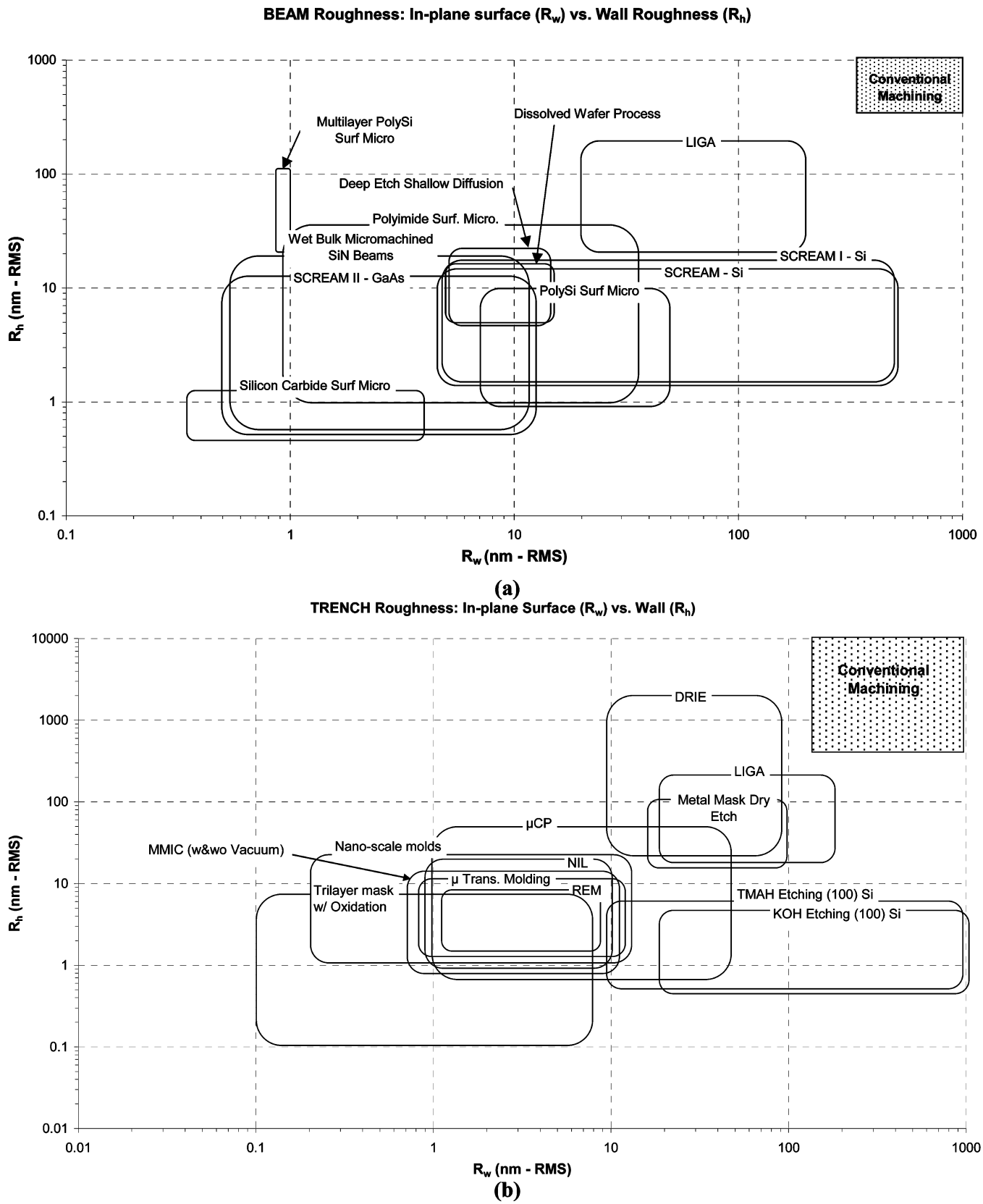


Fig. 6. In-plane surface and wall roughness attribute charts for (a) beams and (b) trenches. Data is derived from the literature according to Table III.

candidate Process chains and to select the most appropriate for the task. Subsequently, a detailed review of the process must be undertaken to understand additional limitations and secondary considerations.

As an illustrative example, consider a MEMS device with a pressure diaphragm comprising a Si plate with doped in piezoresistors. A detailed case study of such a device is provided in [80, Ch. 18]. In order to compete with existing devices

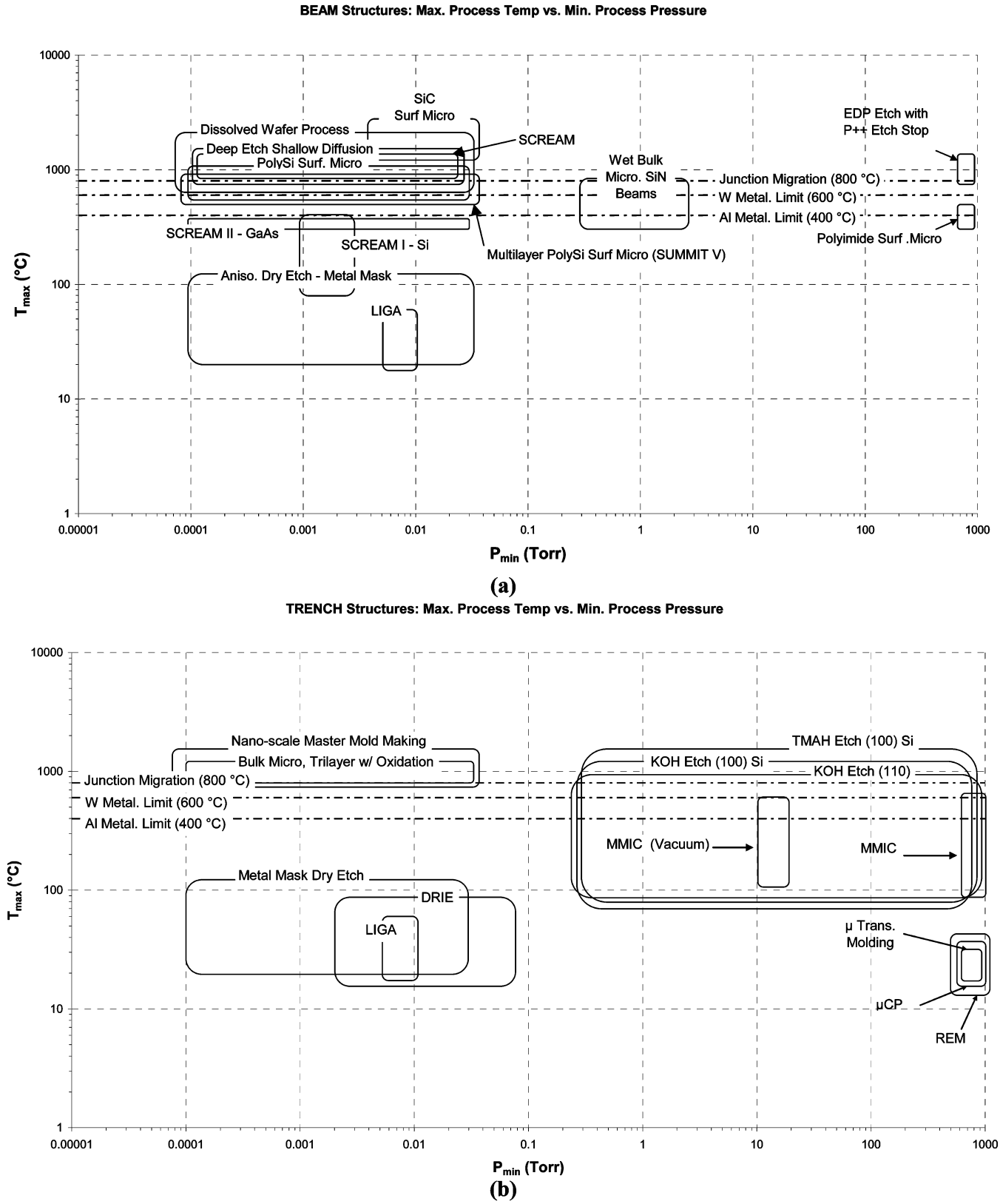


Fig. 7. Maximum process temp versus minimum process pressure attribute charts for (a) beams and (b) trenches.

the pressure sensitivity, K_P, must be better than 0.1 mv/V-kPa. From [80, eq. 18.46], given typical piezoresistor dimensions and piezoelectric coefficients it can be shown that for a square diaphragm K_P is given by

$$K_P = 39 \times 10^{-6} \left(\frac{L}{H} \right)^2 \tag{1}$$

where K_P is in units of mv/V-kPa, and where L and H are the in-plane dimension (width) and thickness of the diaphragm respectively. Thus to achieve the required sensitivity, L/H must exceed 50. Since the diaphragm is essentially a beam structure, this design constraint can be plotted on Fig. 4(a). It creates a triangular area in the bottom right-hand corner of most of the process lozenges. By this metric most of the bulk micromachining processes appear as candidates, capable of creating membranes with dimensions of 1000 μm by 20 μm thick down to 10 μm by 0.2 μm thick.

A second important consideration is the accuracy of the sensor. Currently piezoresistive pressure sensors require electrical calibration using laser trimming of the resistors. One contribution to this is the tolerances on the microfabrication of the diaphragm. An accuracy of better than 1% is required for automotive applications (see [80, Table 17.1, Ch. 17]). If this step could be avoided, by choice of a suitable process chain, then it would have considerable impact on the cost of fabrication of such sensors. Consider a large diaphragm, 1000 μm by 20 μm thick. In the absence of any thickness variation, a width (L) variation of 5 μm is permissible according to (1). This is clearly achieved, see Fig. 5(a). However, in the absence of any width variation, a thickness tolerance of 0.1 μm must be held. From Fig. 5(a), this is marginal for bulk micromachining processes, and given other sources of error, it is clear that microfabrication alone cannot be relied upon to achieve the required accuracy. Greater inaccuracies are anticipated for smaller pressure sensors in their as-processed state. We also note in passing that temperature compensation and packaging introduced stresses are additional drivers for the laser trimming step.

Pursuing the pressure sensor example further, accepting the need to use laser trimming to compensate for the limits in manufacturing tolerances, if the device is to have embedded IC circuitry with aluminium metallization, this requires the processing temperature not to exceed 400 °C, On referring to Fig. 7(a), this would eliminate some process chains involving bonding or doping. From Figs. 5(a) and 7(a) it can be seen that the principal candidate process chains are: DRIE, Anisotropic KOH etching or TMAH etching of (110) Si. In all cases the diaphragm would be formed by etching down from the backside of the wafer, either as a timed etch, or to an etch stop. Additional considerations of cost and process sequence compatibility are needed to identify the best choice. It is clear from this example that a systematic consideration of the functional requirements helps to narrow the process selection substantially.

V. Concluding Remarks

The most obvious limitation of the work presented here is that due to the accuracy and availability of processing data. Typically, the focus of much of the literature on fabrication sequences is neither on process control nor on absolute limits of the Process Chains but on particular devices fabricated using these Process Chains. Few, if any, statistical measures are given to indicate the distribution of the data. Nevertheless, for the purposes of evaluating the use of a systematic approach to MEMS process selection and its associated tools, the data presented here are considered to be adequate. An additional limitation is the lack of economic and time data presented here; this is the subject of future work.

A systematic approach to process selection in MEMS has been presented. Process Attribute maps have been constructed and used to quantify the relative merit of existing Process Chains for MEMS fabrication. In discussing the construction of these maps the process steps of lithography, deposition and etching have been highlighted as controlling the overall performance of MEMS fabrication sequences. The Process Attribute maps have additional value as educational tools and in motivating the further development of MEMS fabrication techniques to extend the coverage of processing space.

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