A SINGLE-STAGE, SINGLE-PHASE, AC-DC BUCK-BOOST CONVERTER FOR LOW-VOLTAGE APPLICATIONS

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Abstract —The suitability of a single-stage ac-dc buck-boost converter for low-voltage applications is investigated. In-depth discussion and analysis of the converter's operating principle, basic relationships that govern converter steady-state operation, and details of the necessary control structures needed to comply with the grid code are provided. The validity of the proposed system is confirmed using PSCAD/EMTDC simulations, and is substantiated experimentally. The buck-boost converter under investigation has good dynamic performance in both buck and boosts modes, and ensures near unity input power factor over the full operating range, whilst having fewer devices and passive elements than other published versions of the buck-boost converter.

Index Terms — ac-dc converter, unity power factor, buck-boost converter.

List of Symbols

δ	duty cycle	L_{dc}	dc side inductance (H)
ω	supply angular frequency (rad/s)	L_s	ac side inductance (H)
C_{dc}	dc side capacitance (F)	R_{dc}	*load resistance (Ω)*
C_s	ac side capacitance (F)	R_s	*ac side resistance (Ω)*
D_1 - D_4	bridge rectifier diodes	S	power electronic switch
D_{bd}	blocking diode	t_{on}	dwell time of the switch within each switching cycle (s)
$\bar{I}_c$	average dc capacitor current (A)	t_{off}	off time of the switch within each switching cycle (s)
$\bar{I}_{dc}$	average load current (A)	T_s	switching period (s)
$\bar{I}_i$	average current entering the dc link node: equal to the instantaneous dc inductor current I_L during Modes 2 and 4 only (A)	v_{cm}	peak ac source capacitor voltage (V)
		v_{cs}	ac source capacitor voltage (V)
I_L	instantaneous dc side inductor current (A)	V_{dc}	instantaneous dc output voltage (V)
$\bar{I}_L$	average inductor current (A)	$\bar{V}_{dc}$	average dc output voltage (V)
i_m	peak fundamental supply current (A)	$\bar{V}_L$	average dc inductor voltage (V)
i_s	input supply current (A)	V_m	peak supply phase voltage (V)
i_s^*	input current control reference (A)	v_s	supply voltage (V)

I. INTRODUCTION

AC-DC converters are widely used in power supplies for microelectronic systems, uninterruptible power supplies (UPS), battery chargers, wind energy conversion systems, household-electric appliances, dc motor drives, and high-voltage dc and flexible ac transmission systems [1-4]. Many single-phase ac-dc converters with power factor correction (PFC) have been studied. The topologies can be divided into two categories: single-stage and two-stage converters. Most single-stage ac-dc converters with PFC employ an H-bridge rectifier followed by a boost converter. The output dc voltage is therefore greater than or equal to the peak of the ac supply voltage [5-13]. Power factor correction is achieved by regulating the inductor current of the boost

stage. Several single-phase single-stage ac-dc buck converters have been proposed for electrical vehicle battery charging [5, 14, 15]. Several single-stage buck ac-dc converters with PFC have been proposed [16-19]. A two-stage ac-dc buck-boost converter has been proposed [20-23] that offers input PFC capability. This buck-boost converter requires independent control of the buck and boost stages, and suffers from control difficulties during transition between buck and boost modes. Additionally, it requires a large number of semiconductor devices and passive elements [24]. A single stage buck-boost converter that operates based on the zero current resonance principle, and which has a relatively low number of switches, has been proposed [25]. Its main limitation is that the use of resonance can make its implementation expensive since it utilises tuned inductors that need to be retuned frequently as the other passive elements age and their characteristics change. Another single-stage buck-boost converter [26-28] uses a single self-commutated switch, with a large number of diodes and passive elements.

Fig. 1(a) shows a single-stage ac-dc buck boost converter whose performance when operated with discontinuous dc side inductor current has been investigated [29]. Only the buck operating capability of this converter is therefore exploited, and power factor correction is performed, but no information about the shape of the input current waveforms is given.

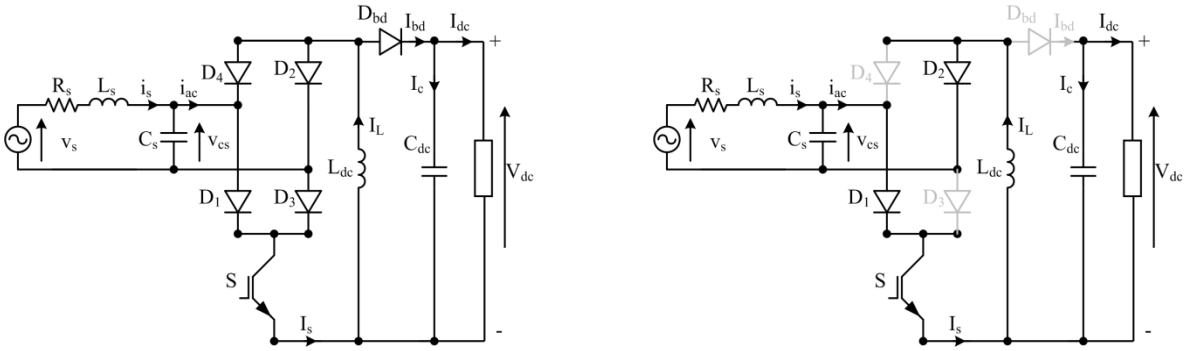
Nonlinear control has been used to regulate output dc voltage and provide power factor correction [30]. Although the circuit is simple, the proposed controller requires five feedback signals, thereby increasing the overall complexity, and potentially the cost, of the implementation. Performance of this complex system is demonstrated in buck mode only, using simulation and without experimental substantiation. Another nonlinear control study [31] on a buck-boost converter [29] proposes two control methods. The first control method regulates dc inductor current I_L instead of output dc voltage V_{dc} and requires an additional stage to adjust the dc output voltage. The second control method regulates dc output voltage V_{dc} directly using a single stage. However, both control methods use extremely high switching frequency of 100kHz, with supply current total harmonic distortion exceeding the levels specified in many grid codes and standards (THD of 7.47% and 19.81% for the first and second control methods respectively). No experimental results are presented, and the simulation results are for the buck operating mode only.

This paper describes the operating principles of the buck-boost converter in Fig. 1, and highlights its distinct attractive features such as buck-boost capability in a single stage with a single switch, reduced power circuit and

control system complexity since no isolated gate drives are needed, stable dc voltage output in both buck and boost modes, sinusoidal input current with unity power factor, suitability for grid interfacing of small-scale renewable ac sources, and the lack of requirement for a pre-charging circuit for the dc side capacitor C_{dc}. A simple linear controller is used that requires only two control loops. The outer control loop regulates converter dc output voltage and estimates the peak fundamental current i_m required to maintain the dc link voltage at any desired level, and then synchronises to the grid voltage to provide the reference current i_s^* to the inner current control loop. The inner control loop ensures sinusoidal input current at any power factor (in this study power factor is set to 1). The inner control loop estimates the ac side capacitor voltage v_{cs} required to force input current i_s to follow its control reference i_s^* and ensures the correct power balance between ac and dc sides using PI control. Additionally, in grid applications the inner control loop provides converter over-current protection during extreme transient conditions in the dc side.

II. PROPOSED BUCK-BOOST CONTROLLED BRIDGE

The basic converter topology is shown in Fig. 1(a) and includes three main parts: an LC filter, a diode rectifier and a buck-boost chopper. Note that the diode rectifier bridge is reversed so that the buck-boost converter gives positive output voltage. Operating Mode 1, where switch S is turned on during the positive half-cycle of the supply v_s, is shown in Fig. 1(b). In this mode, supply v_s energises dc inductor L_{dc} through switch S and diodes D_1 and D_2, while capacitor C_{dc} acts as an energy tank supplying the load. Operating Mode 2, shown in Fig. 1(c), is the free-wheeling period when switch S is turned off during the positive half-cycle of the supply v_s. Here, the energy stored in dc inductor L_{dc} during Mode 1 is used to supply the load and to recharge capacitor C_{dc}. For correct converter operation, therefore, dc capacitance C_{dc} and dc inductance L_{dc} must be sized to prevent discontinuity in the load and inductor currents. Operating Mode 3, shown in Fig. 1(d), is where switch S is turned on during the negative half-cycle of the supply v_s. Inductor L_{dc} is re-energised through switch S and diodes D_3 and D_4, whilst the energy stored in dc capacitor C_{dc} supplies the load. Modes 1 and 3 use the same switching device to modulate the ac source, and have the same effect on the state of charge of the dc side elements L_{dc} and C_{dc}. Operating Mode 4, where switch S is turned off (and its series diode is reverse biased) during the negative half-cycle of the supply v_s follows. Operating Modes 2 and 4 are identical.



(a) Single-phase ac-dc boost converter

(b) Operating Mode 1 - conducting

(c) Operating Mode 2 (4) - freewheeling

(d) Operating Mode 3 - conducting

Fig. 1: Schematic of the proposed single-phase ac-dc buck-boost converter and its operating modes.

Differential equations (1) and (2) describe circuit operation during Modes 1 and 3, whilst equations (3) and (4) describe circuit operation during Modes 2 and 4.

$$\frac{dI_L}{dt} = -\frac{v_{cs}}{L_{dc}} \tag{1}$$

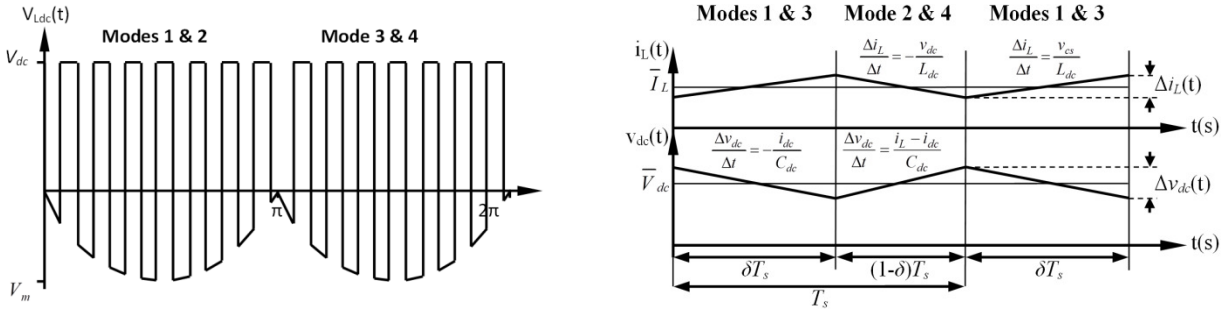
$$\frac{dV_{dc}}{dt} = -\frac{I_{dc}}{C_{dc}} \tag{2}$$

$$\frac{dI_L}{dt} = \frac{V_{dc}}{L_{dc}} \tag{3}$$

$$\frac{dV_{dc}}{dt} = \frac{I_L - I_{dc}}{C_{dc}} \tag{4}$$

The negative sign in equations (1) and (2) appears because the bridge rectifier is reversed. Neglecting the resistive voltage drop, the voltage across ac source capacitor C_s is given by (5).

$$v_{cs} = v_s - L_s \frac{di_s}{dt} \tag{5}$$



(a) Voltage across dc side inductor L_{dc} (b) dc side inductor current and dc side capacitor voltage

Fig. 2: Waveforms for the proposed single-phase ac-dc buck-boost converter.
[Note that V_m is the peak value of supply voltage v_s]

The mathematical relationships describing steady-state operation are obtained using inductor zero average volt-second and capacitor voltage balance principles [32]. The voltage across dc inductor L_{dc} is illustrated in Fig. 2(a) where, for simplicity, is it initially assumed that ac source stray inductance L_s is sufficiently small so that v_{cs} can be considered equal to v_s, shown in Fig. 1(a), without significant loss of accuracy. Following on from Fig. 2(b), which shows dc inductor current and dc capacitor voltage, it can be shown that the voltage across the dc inductor within each switching period T_s during operating modes 1 and 2 can be expressed by $v_L=-\delta v_{cs}$ and $v_L=(1-\delta)V_{dc}$ respectively, where $\delta=t_{on}/T_s$ and t_{on} is the dwell time of the switch within each switching cycle. Based on the inductor zero average volt-second principle [32], the average voltage across L_{dc} is calculated and set to zero as in (6)

$$\overline{V}_{L_{dc}} = \frac{1}{\pi}\int_0^{\pi} [-\delta v_s + (1-\delta)V_{dc}]\, d\omega t = 0 \tag{6}$$

where δ is the duty cycle of switch S. Assuming a sinusoidal source voltage defined by $v_s=V_m \sin\omega t$, where V_m is the peak phase voltage, ω is the supply angular frequency, and t is time, and that the average output dc voltage is defined by $\overline{V}_{dc} = \frac{1}{\pi}\int_0^{\pi} V_{dc}\, d\omega t$, then equation (6) reduces to

$$\overline{V}_{dc} = \frac{\delta}{1-\delta} \times \frac{2V_m}{\pi} \tag{7}$$

Since capacitor voltage balance [32] necessitates the average capacitor current $\bar{I}_c$ over one or a number of consecutive switching cycles to be zero, the relationship between the average inductor current $\bar{I}_L$ and the average load current $\bar{I}_{dc}$ is

$$\bar{I}_c = \frac{1}{\pi}\int_0^{\pi} [-\delta \bar{I}_{dc} + (1-\delta)(\bar{I}_L - \bar{I}_{dc})]\, d\omega t = 0 \tag{8}$$

In (8), the capacitor current in operating Modes 1 and 3, and in Modes 2 and 4 is expressed as $\bar{I}_c = -\delta \bar{I}_{dc}$ and $\bar{I}_c = (1-\delta)(\bar{I}_L - \bar{I}_{dc})$ respectively.

Equation (8) can be reduced to

$$\frac{1}{\pi}\int_0^{\pi} \bar{I}_{dc}\, d\omega t = \frac{(1-\delta)}{\pi}\int_0^{\pi} \bar{I}_L\, d\omega t \tag{9}$$

Equation (9) implies

$$\bar{I}_{dc} = (1-\delta)\bar{I}_L \tag{10}$$

Since, in practice, the average inductor current is maintained virtually constant, the dc output or load current $\bar{I}_{dc}$ remains constant and proportional to the inductor average current, as illustrated by (10). This feature can be exploited to reduce the voltage stresses on the switching devices of current source inverters and maintain a constant average input dc current when the proposed buck-boost converter is used as an active front end. For a resistive load the dc output voltage can be expressed in term of the average inductor current, as shown in (11).

$$V_{dc} = (1-\delta) R_{dc} \bar{I}_L \tag{11}$$

The converter passive elements L_{dc} and C_{dc} are selected based on the maximum permissible inductor current ripple and output voltage ripple, ΔI_{dc} and ΔV_{dc} respectively. Therefore, from (1) to (4) and Fig. 2(b), (12) and (13) are obtained.

$$L_{dc} = \frac{(1-\delta) T_s \times V_{dc}}{\Delta I_L} \tag{12}$$

$$C_{dc} = \frac{\delta T_s \times \bar{V}_{dc}}{\Delta V_{dc} \times R_{dc}} \tag{13}$$

III. CONTROL STAGE

The purpose of the controller is to force the ac line current to be sinusoidal and in phase with the input source voltage, and to control the average output dc voltage in both buck and boost operating modes.

a. Current Control

In order to obtain sinusoidal input current at any power factor, the required control system structure is derived accounting for the ac fundamental frequency and dc side dynamics. Since the output dc voltage V_{dc} is dependent

upon the magnitude of the voltage v_{cs} across the input filter capacitor, differential equation (14) can be used as the basis for current controller design.

$$\frac{di_s}{dt} = -\frac{R_s}{L_s} i_s + \frac{(v_s - v_{cs})}{L_s} \tag{14}$$

The voltage v_{cs} required to force input current i_s to follow its control reference i_s^* is unknown, but it can be obtained using a PI controller by setting

$$w = v_s - v_{cs} = k_p (i_s^* - i_s) + k_i \int (i_s^* - i_s) dt \tag{15}$$

$$\psi = k_i \int (i_s^* - i_s) dt \tag{16}$$

The current controller transfer function is obtained by substituting (16) into (15), and then substituting the result for v_s-v_{cs} into (14).

$$\frac{di_s}{dt} = -\frac{(R_s + k_p)}{L_s} i_s + \frac{\psi}{L_s} + \frac{k_p i_s^*}{L_s} \tag{17}$$

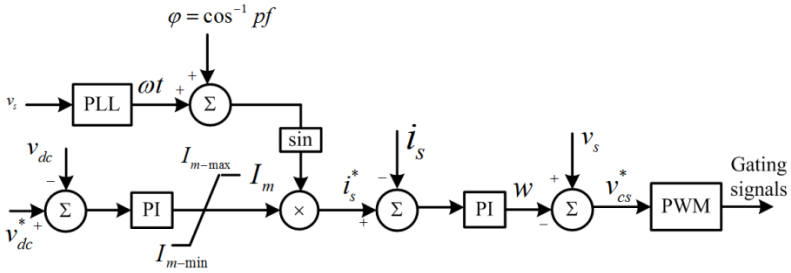
After Laplace manipulation of (17) and (16) the transfer function is defined as

$$\frac{I_s(s)}{I_s^*(s)} = \frac{\frac{k_p}{L_s} s + \frac{k_i}{L_s}}{s^2 + \frac{R_s + k_p}{L_s} s + \frac{k_i}{L_s}} \tag{18}$$

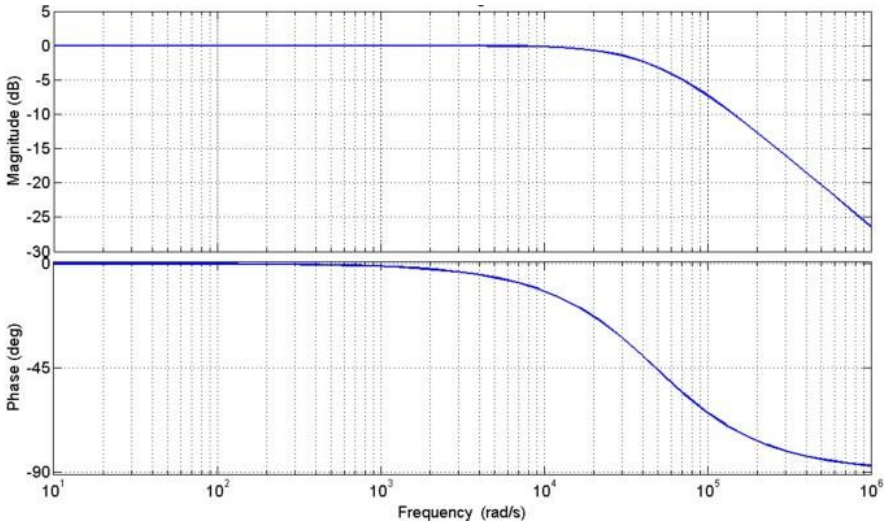
From (15), v_{cs} can be obtained as

$$v_{cs} = v_s - w \tag{19}$$

Note that w represents the output of the PI controller that regulates converter input current, and that v_s is the supply voltage that is incorporated as feed-forward control to improve dynamic response and for controlled start-up. The block diagram of the proposed control structure shown in Fig. 3(a) is derived based on equations (15) and (19). The supply current can be controlled to be sinusoidal and to achieve any power factor φ, where $|\varphi| \le \pi/2$, provided the controller (18) has sufficient bandwidth so as not to introduce distortion in the normalized version of the fundamental voltage component passed as a reference to the converter modulator. The frequency response of current controller (18), with gains k_p=120 and k_i=2000 selected to enable reproduction of any desired reference without magnitude attenuation or the introduction of phase shift, as shown in Fig. 3(b), highlights that the controller bandwidth is sufficient.



(a) Proposed control structure showing two control loops



(b) Controller Bode plots, with k_p=120 and k_i=2000

Fig. 3: Proposed controller and its frequency response.

b. Voltage Control

Equation (4), which describes the converter dc side dynamics, provides the basis for the dc voltage controller. Assuming a resistive load and substituting for $\bar{I}_{dc}$ results in (20)

$$\frac{dV_{dc}}{dt} = -\frac{\bar{V}_{dc}}{R_{dc} C_{dc}} + \frac{\bar{I}_{dc}}{C_{dc}} \tag{20}$$

where $\bar{v}_{dc}$ is the average dc link voltage, and $\bar{I}_i$ is the average current entering the dc link node and is equal to the instantaneous dc inductor current I_L during Modes 2 and 4 only. Assuming lossless conversion, power balance dictates that $P_{ac}=P_{dc}$. Therefore

$$\bar{V}_{dc}\bar{I}_i = \frac{1}{2} v_{cm} i_m \cos\varphi \tag{21}$$

where v_{cm} is the peak voltage across the ac side input capacitor, and i_m is the peak fundamental current. Using (7), this can be rewritten as (22) from which I_i can be obtained.

$$\bar{I}_i = \frac{1}{2}\frac{v_{cm}}{\bar{V}_{dc}}\cos\varphi \times i_m = \frac{\pi}{4}\frac{(1-\delta)}{\delta}\cos\varphi \times i_m \tag{22}$$

Equation (22) highlights that the relationship between peak fundamental current i_m and $\bar{I}_i$ depends upon quantities, such as duty cycle, which may vary according to operating conditions. Substituting (22) into (20) gives (23)

$$\frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R_{dc}C_{dc}} + A\frac{i_m}{C_{dc}} \tag{23}$$

where $A = \frac{\pi}{4}\frac{(1-\delta)}{\delta}\cos\varphi$.

The peak fundamental current i_m required to maintain the dc link voltage at any desired level can be estimated using PI control. Assuming that the controller gain terms also perform the necessary scaling for A in (23), i_m is expressed as

$$i_m = k_{pdc}(V_{dc}^* - V_{dc}) + k_{idc}\int (V_{dc}^* - V_{dc})\,dt \tag{24}$$

$$\lambda = k_{idc}\int (V_{dc}^* - V_{dc})\,dt \tag{25}$$

The voltage controller transfer function is obtained by substituting (24) into (23), and results in (26), whilst the derivative of λ is expressed in (27).

$$\frac{dV_{dc}}{dt} = -\left[\frac{1}{R_{dc}C_{dc}} + \frac{k_{pdc}}{C_{dc}}\right]V_{dc} + \frac{\lambda}{C_{dc}} + \frac{k_{pdc}}{C_{dc}}V_{dc}^* \tag{26}$$

$$\frac{d\lambda}{dt} = -k_{idc}V_{dc} + k_{idc}V_{dc}^* \tag{27}$$

Taking Laplace transforms of (26) and (27), and following manipulation, results in (28).

$$\frac{V_{dc}(s)}{V_{dc}^*(s)} = \frac{\frac{k_{pdc}}{C_{dc}}s + \frac{k_{idc}}{C_{dc}}}{s^2 + \left[\frac{1}{R_{dc}C_{dc}} + \frac{k_{pdc}}{C_{dc}}\right]s + \frac{k_{idc}}{C_{dc}}} \tag{28}$$

Since the change in the dc link voltage is much slower than that of the fundamental current due to limitations imposed by the magnitude of the energy storage devices (dc link capacitor), the outer control loop gains are selected such that the closed-loop poles or eigenvalues are located at s=-37 and s=-12.5. The gains corresponding to these poles are k_{pdc}=0.1A/V and k_{idc}=1AV^{-1}s^{-1}.

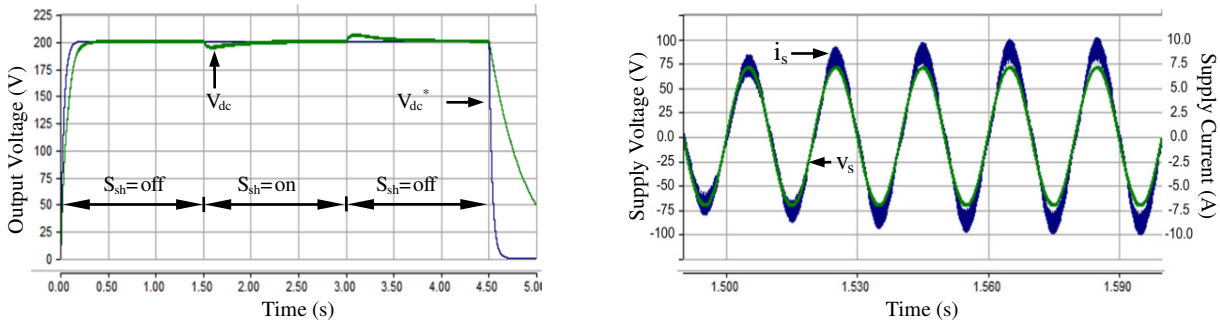
IV. SIMULATION STUDY

PSCAD/EMTDC simulation software was used to model the buck-boost converter of Fig. 1(a), complete with the current and voltage controllers defined in (15) and (24) respectively, to demonstrate the closed-loop performance of a 320W system. The parameters used in the simulation are defined in Table 1. Initially, the converter load is purely resistive, consisting of two series-connected resistances of 128Ω and 44Ω. The load is increased by short circuiting the 44Ω resistance using shunt semiconductor switch S_{sh}.

Table 1: System Parameters

Parameter	Value
supply voltage	50V
supply frequency	50 Hz
ac side inductance	2.22mH
ac side capacitance	1μF
dc side inductance	0.5mH
dc side capacitance	2200μF
switching frequency	10kHz

Fig. 4(a) shows the simulation results for the closed-loop controlled converter, where the dc link voltage is gradually increased from zero to 200V, and reduced to zero again at t=4.5s. At t=1.505s, corresponding to the positive peak of the supply voltage, the load resistance is decreased by turning on shunt switch S_{sh} for 1.5s, thereby mimicking a step increase in output power from 230W to 312W. Output power is then decreased to 230W by turning off the shunt switch S_{sh}. Fig. 4(a) shows the output voltage has minimum latency and over/undershoots during the load change. Simulation results in Fig. 4(b) show that, during the step power change, supply voltage and current remain sinusoidal with unity power factor (i.e. supply current and voltage are in phase), and that the transition in supply current is both rapid and smooth. This is achieved with a switching frequency of 10kHz, small ac side filter passive elements and dc side inductance, and a sizable dc side capacitor used as an energy reservoir to prevent discontinuous load current. The soft start-up and shutdown feature demonstrated in Fig. 4(a) makes this converter attractive as a front end for many grid-connected voltage and current source inverters since no capacitor pre-charging is required, as is the case with other converter topologies. Thus, because of the buck-boost functionality, the inrush currents during start-up can be expected to be minimal.



(a) dc output voltage

(b) Supply voltage and current during step increase in output power

Fig. 4: Simulation results for proposed single-phase ac-dc buck-boost converter, with P_{rated}=320W.

V. CONVERTER SCALABILITY

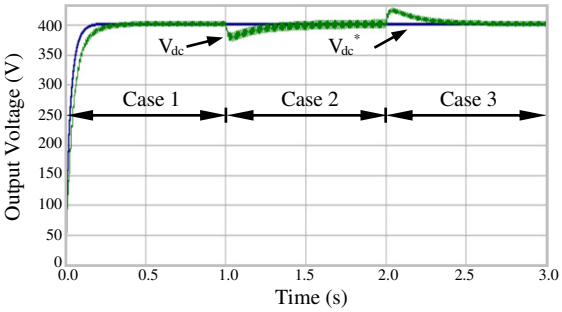
To show the potential for application of the proposed buck-boost converter at higher power ratings, a 3.8kW version is investigated. Simulation parameters are the same as in Table 1, except the input supply voltage v_s is increased to $220V_{RMS}$ and the ac side filter inductance L_s is reduced to 1mH. To test the converter's ability to provide stable dc output under different operating conditions, three different cases are investigated:

Case 1 Soft start, to prevent high charging currents in the input and output capacitors.

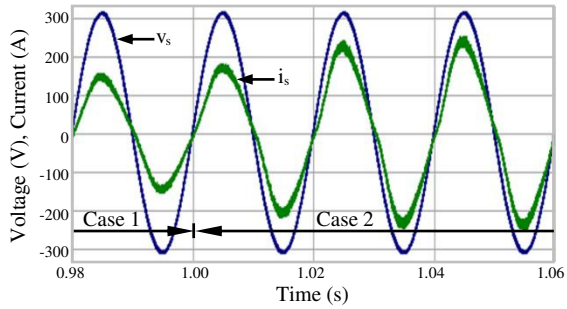
Case 2 Dynamic response to a step increase in load from 1.58kW to 3.66kW.

Case 3 Dynamic response to a step decrease in load from 3.66kW to 1.58kW.

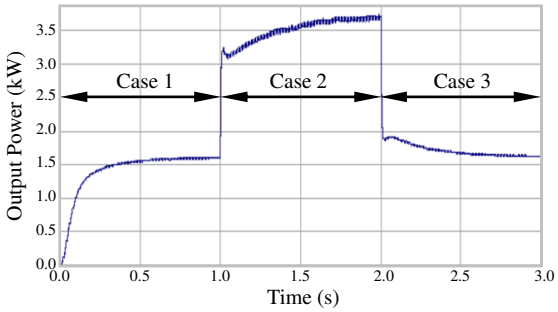
Fig. 5 shows the simulated response of the proposed converter under all three operating cases. Fig. 5(a) shows that the converter output voltage V_{dc} closely follows its 400V dc reference, with minimum latency and over/undershoot, as the load changes. Fig. 5(b) shows the input current during the transition from Case 1 to Case 2, and demonstrates that it remains sinusoidal with near unity power factor. Fig. 5(c) shows the dc output power response as the load varies during transitions between the three operating cases, and demonstrates that the control action is effective.



(a) Required dc output voltage and converter output voltage



(b) Supply voltage and current during change from Case 1 to Case 2



(c) Output dc power

Fig. 5: Waveforms illustrating possible scalability of the proposed buck-boost converter.

VI. EXPERIMENTAL RESULTS

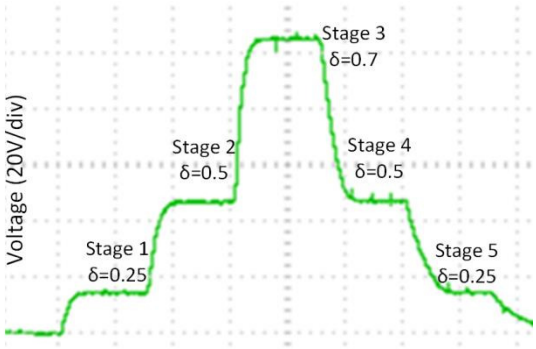
Open- and closed-loop performance of the buck-boost converter of Fig. 1(a) is demonstrated experimentally. The results from the open-loop tests are used to validate the mathematical relationships presented in Section II, without any interference from the control system. The closed-loop tests are used to illustrate converter performance when operated in grid mode, where it must comply with strict grid code requirements.

a. Open-Loop Performance

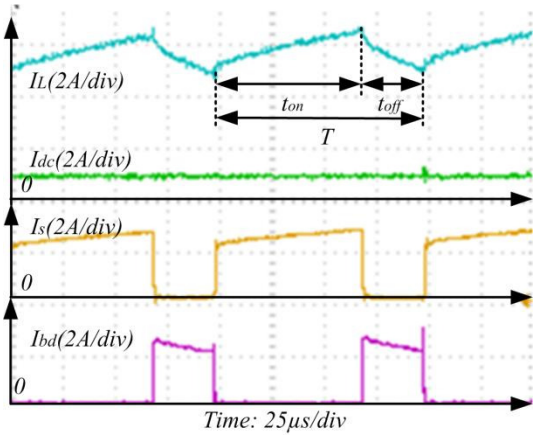
The parameters used in the experimental validation are specified in Table 1. The open-loop operating scenario consists of five different stages to demonstrate converter operation in both buck and boost modes. In Stage 1, the duty cycle δ is ramped from 0 to 0.25 and then maintained constant for 0.75s. In Stage 2, δ is ramped from 0.25 to 0.5 and maintained constant for 0.75s. In Stage 3, δ is ramped to from 0.5 to 0.7 and maintained constant for 1s. In stages 4 and 5, δ is decreased at rates reflecting those in stages 2 and 1 respectively. Fig. 6(a) shows converter output voltage V_{dc} during all five stages, which include both buck and boost operation. Fig. 6(b) shows the currents in the dc side inductor, I_{Ldc}, the load, I_{dc}, the blocking diode, I_{Dbd}, and the switch, I_S, when δ=0.7. It can be seen that I_{Ldc} is equal to I_S during the on period of switch S, and equal to I_{Dbd} during the

off period of switch S. Fig. 6(c) shows the voltage stresses on the switch, V_S, on the dc side inductor, V_{Ldc}, and on the blocking diode, V_{Dbd}, when δ=0.7.

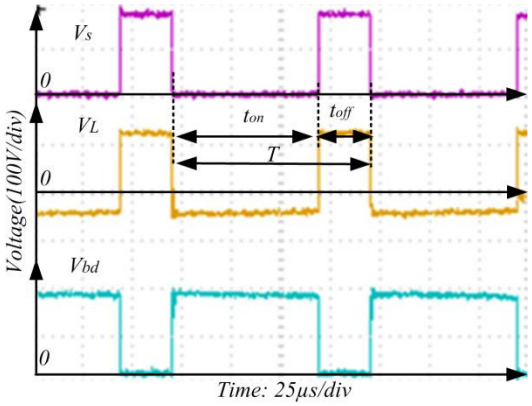
It can be seen from Fig. 6(c) that the average dc side inductor voltage equals zero over one switching (or fundamental) period. Also, switch voltage V_S is zero during the on period, and is equal to the sum of the dc side inductor voltage V_{Ldc} and the supply voltage v_s during the off period. Finally, the blocking diode voltage stress V_{Dbd} is equal to the sum of the dc side inductor voltage V_{Ldc} and the output voltage V_{dc} during the on period, whilst it is zero during the off period. These results show that the voltage ratings of switch S and blocking diode D_{bd} must be sufficient to withstand voltage stresses related to the sum of the ac source and the dc output. In this experiment, blocking diode D_{bd} is rated at 600V and 40A, whilst switch S is rated at 1200V and 40A.



(a) dc output voltage



(b) dc inductor, output, switch and blocking diode currents



(c) Detailed view of switch, dc inductor and blocking diode voltages

Fig. 6: Experimental waveforms showing open-loop performance of proposed buck-boost converter, with R_{dc}=172Ω.

b. Closed-Loop Performance

A single-phase buck-boost converter, as shown in Fig. 1(a), is operated under closed-loop control to substantiate the simulation results presented in Section IV. The system parameters and operating conditions are the same as for the simulations. The results in Fig. 7 are obtained when the reference dc voltage is changed from 0 to 200V

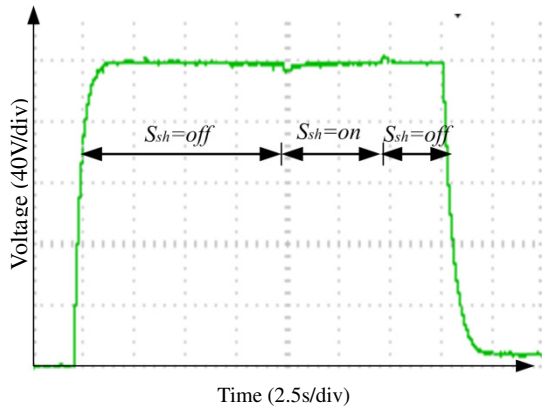
and reduced to zero after 14s (this is to demonstrate converter operation in boost and buck modes). Fig. 7(a) shows that dc output voltage V_{dc} closely follows its defined reference (a first-order low-pass filter is used to slightly reduce the rate of rise of the reference dc voltage as a result of the step function). Observe that the dc voltage is maintained nearly constant as load varies. Fig. 7(b) shows a detailed view of the dc voltage across the load, and supply current and voltage during the steady state. It can be seen that the converter operates at unity power factor, with 4.47% THD. Fig. 7(c) shows supply current i_s and voltage v_s, and dc voltage V_{dc} during start-up. Observe that the input supply current is sinusoidal and remains in phase with the supply voltage as the dc link voltage increases. From Fig. 7(d) it can be observed that the output dc voltage experiences a small decrease during the load change, while the ac side waveforms remain sinusoidal, with unity power factor.

To demonstrate the power quality profile of the input current during buck and boost modes, Fig. 8 presents supply current and voltage, and dc output voltage during different dc link reference voltages V_{dc}^{*}. Fig. 8(a) to (d) show that the proposed buck boost converter is able to provide a high-quality sinusoidal supply current, with near unity power factor over a wide operating range.

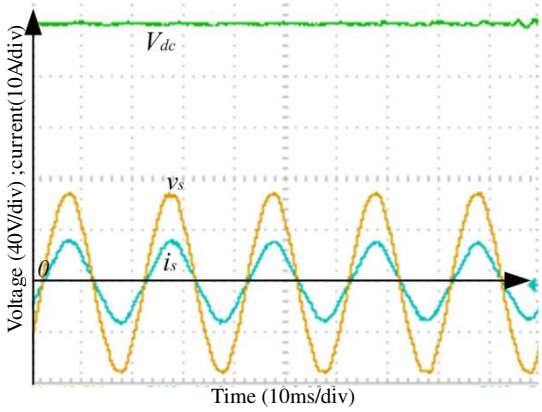
To highlight the significance of the proposed buck-boost converter, a general comparison with similar converter topologies from the open literature [25, 26] is presented in Table 2.

Table 2: Comparison of Proposed Buck-Boost Converter with those in [25, 26]

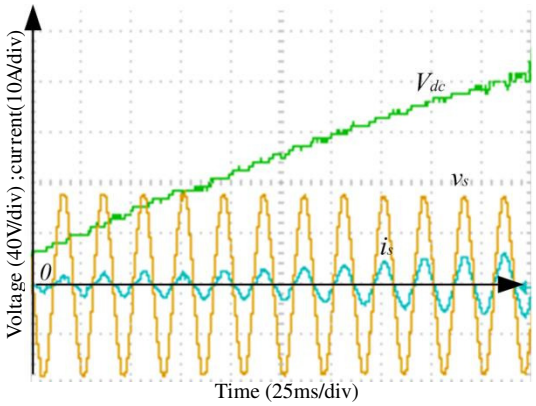
Feature	Proposed Converter	Converter [25]	Converter [26]
Number of Semiconductor Switches	low	moderately high	high
Number of Passive Elements	low	medium	high
AC Filter Requirements	L-C filter	L-C filter	not required
Output Voltage Control Region	full range including buck and boost mode	full range claimed but only boost operation is demonstrated	full range claimed but only buck operation is demonstrated
Soft Start-Up and Shutdown Capability	demonstrated in Fig.4(a), Fig.5(a), Fig.6(a) and Fig.7(a)	not mentioned	not mentioned
Power Factor Correction	near unity over the full operating range	near unity at high load and <0.9 at low load (Fig. 9)	near unity at rated load
Switching Frequency	5kHz-10kHz	40kHz	100kHz
Applications	low power scalable to medium power applications	low power	low power



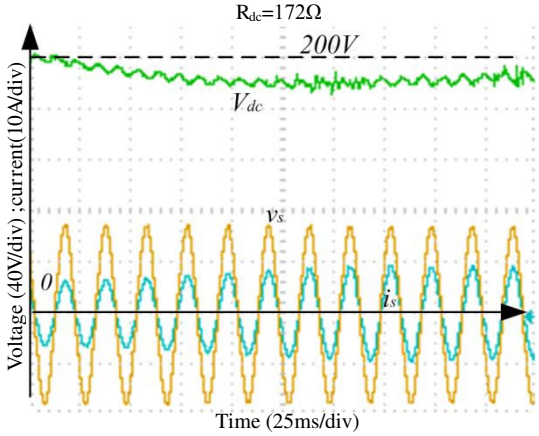
(a) dc output voltage



(b) Steady-state supply current and voltage, v_{dc}=200V and R_{dc}=172Ω

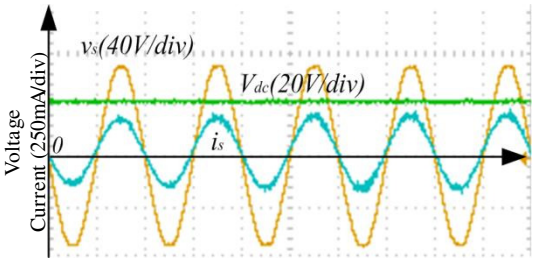


(c) Supply current and voltage, and output dc voltage during start-up

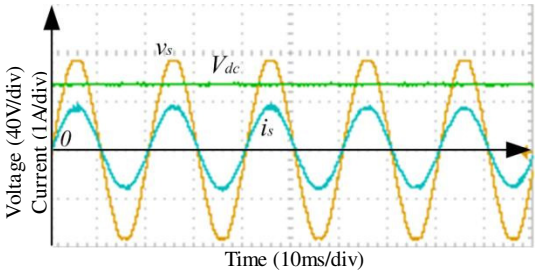


(d) Supply current and voltage and output dc voltage during step increase in output voltage

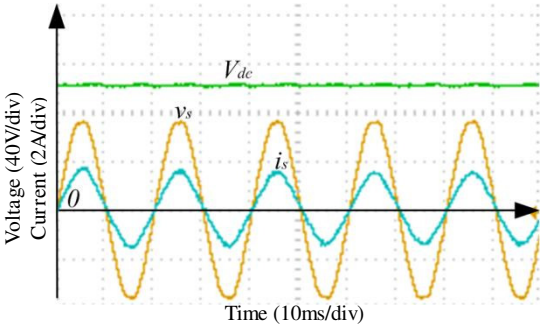
Fig 7: Experimental waveforms showing closed-loop performance of proposed buck-boost converter, with P=320W.



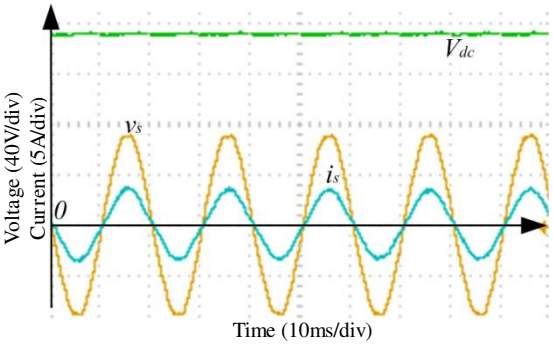
(a) Steady-state supply current and voltage THD=2.88% at V^*_{dc}=20V



(b) Steady-state supply current and voltage THD=2.08% at V^*_{dc}=50V



(c) Steady-state supply current and voltage THD=3.6% at V^*_{dc}=100V



(d) Steady-state supply current and voltage THD=4.09% at V^*_{dc}=150V

Fig 8: Experimental waveforms showing closed-loop performance of proposed buck-boost converter at different dc voltage output reference with R_{dc}=172Ω.

VII. CONCLUSION

The technical viability of a single-stage, single-phase, buck-boost converter operated as a PWM rectifier for a low-voltage general distribution system is investigated. Its operating principle is discussed in detail, and mathematical relationships describing its steady-state operation are presented. The control structures required to ensure sinusoidal input current and unity input power factor are discussed. Results obtained from PSCAD/EMTDC simulation and experimentation show that the proposed buck-boost converter is viable as a PWM rectifier, and as a front end for grid-connected current and voltage source converters

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