Journal of Electroceramics, 8, 233–241, 2002

Interface Characterization of All-Perovskite Oxide Field Effect Heterostructures

B. NAGARAJ, T. WU, S.B. OGALE, T. VENKATESAN & R. RAMESH

Department of Materials and Nuclear Engineering, Center for Superconductivity Research, Department of Physics, University of Maryland, College Park, MD 20742, USA

Submitted January 2002; Revised June 2002; Accepted July 2002

Abstract. All-oxide devices consisting of Niobium-doped Strontium Titanate (Nb:STO)/Strontium Titanate (STO)/Lanthanum Strontium Cuprous Oxide (LSCO) heterostructures were fabricated and characterized electrically for their interface properties through capacitance-voltage (*C-V*) and current-voltage (*I-V*) techniques, in the context of electric field effect studies. The *C-V* studies establish the occurrence of charge modulation in the LSCO channel. Absence of hysteresis in the *C-V* characteristic when the voltage is retraced suggests the absence of mobile ions in the gate oxide and slow interface traps. This is further corroborated by the absence of drift in the *C-V* characteristic and shift in the flat band voltage (V_{FB}) when the device is subjected to temperature-bias aging. The interface state density obtained from V_{FB} is $\sim 10^{12}/cm^2$. The uncompensated hole concentration in the LSCO channel calculated from the measured room temperature *C-V* data is $\sim 10^{20}/cm^3$ and is in good agreement with the expected hole concentration in LSCO. Current-time and current-voltage plots are invariant with respect to the polarity of the applied voltage up to ∼5 V. This, in a structure with asymmetric interfaces, indicates that the electrical contacts to STO are non-blocking and the conduction through STO is bulk-limited in this voltage regime. Thickness dependent current and capacitance studies also corroborate the bulk-limited nature of conduction through the device in this voltage regime. However, *I-V* characteristic shows a rectifying nature beyond ∼8 V indicating that the mechanism in this voltage regime could be interface limited.

Keywords: FET, perovskite oxide, interface, STO

Introduction

Use of external fields (electric, magnetic or light as well) is known to be a reversible method to tune the electrical properties of solids, and has led to many device concepts. The field effect transistor (FET), in particular, is an example of the significant impact of the field-tuning idea on the field of silicon microelectronics [1]. However, the ever-growing demand on higher density of transistor packaging, and correspondingly the shrinking dimensions of individual devices, have now begun to stretch the performance domain of silicon-based electronics because of the low carrier density in these materials that intrinsically leads to poor carrier statistics in very small systems. Thus, it has become essential to explore the electric field induced phenomena and field effect transistor (FET) action in other high carrier density systems.

Amongst the different high carrier density material systems which can potentially serve as candidates for the channel layer, the metal-oxides family stands out as the most promising one for various reasons and has been the subject of several investigations [2–19]. First, the properties of such oxides can be controlled from super-conducting to highly insulating by appropriate doping and strain control, thereby allowing the choice of carrier density in the channel as well as that of an epitaxially compatible gate layer: bandwidth control is much easier in oxides than in other materials. Second, metal-oxides display a much broader range of physical responses such as ferromagnetism, ferroelectricity, metal-insulator transitions, sensitivity to optical, mechanical and thermal perturbations, various ordering phenomena in cation and oxygen sublattices etc. as compared to other possible channel candidates, thereby allowing the possibility of realizing multifunctional

device concepts. Third, metal-oxides are much more stubborn against adverse mechanical conditions as compared to the softer pure metals/alloys or organic materials. Based on these considerations, considerable work has been initiated and done during the past decade or so, on electric field effects in oxide channels. The main systems that have attracted particular attention in this regard are the oxide perovskites; namely the high T_c superconductors and mixed-valent manganites. Not only is the proof of the field effect principle amply demonstrated in both these classes of perovskites, but this research has also led to many interesting ideas, such as the proposal of Mott Transition field effect transistor (MT-FET) by Newns et al. [20] and that of enhanced electric field effect with a complementarity of electric and magnetic field effects in manganites due to electronic phase separation in the channel by [19, 21]. Now the interest has shifted to issues such as the nature and degree of carrier injection, interface trap density, presence of an unintentional barrier layer at the interface, if any, created by interface chemistry, stability of the gate dielectric and the field and temperature dependence of its dielectric properties, the electrical uniformity of the channel layer etc. In this paper we attempt to address some of these by analyzing the Ag/Nb:$SrTiO_3$/$SrTiO_3$/LSCO/Pt heterostructure as a prototypical vehicle for experimentation.

Experiment

All layers of the heterostructure of $SrTiO_3$/$La_{1.85}Sr_{0.15}CuO_4$/Pt were grown by pulsed laser deposition by using a KrF excimer laser ($\lambda = 248$ nm, $t_p = 20$ ns) under optimized conditions. A (001)-oriented single crystal of conducting STO (doped with 1 at.% Nb) of resistivity 80 mΩcm was used both as the substrate for the growth of the heterostructure, and as gate electrode for the capacitors. The metallic nature of Nb:STO was verified using 4 point probe *I-V* measurements and the resistivity was found to be 80 mΩcm at room temperature. The surface preparation procedure of Kawasaki et al. [22] was followed to achieve an atomically flat substrate surface. On the top of 1 mm thick substrate, STO layers of various thicknesses were grown under an oxygen pressure of 100 m Torr at 750°C. Then at the same temperature, 80 nm LSCO layer was grown under an oxygen pressure of 150 m Torr. The sample was cooled down slowly in oxygen ambient

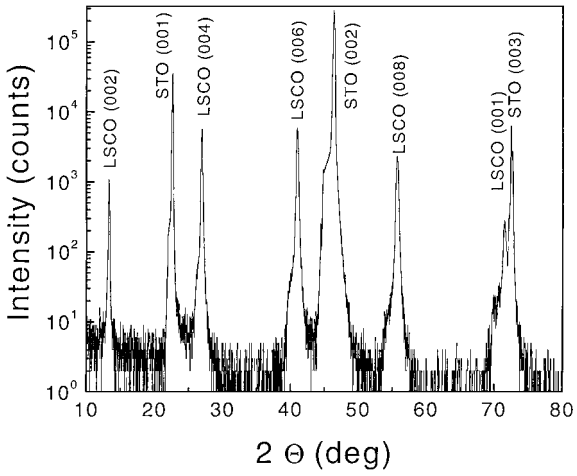

Fig. 1. X-ray-diffraction spectrum for a 100 nm LSCO/300 nm STO bilayer on Nb:STO substrate illustrating the high quality epitaxial nature of the heterostructure.

(∼500 Torr) before the other metal electrode Pt was deposited at room temperature. The resistivity of LSCO layer was measured to be 50 mΩcm. Ag was evaporated at the back of Nb:STO substrate for good electrical contact. Christen et al. [23] have reported the ohmic nature of Ag/Nb:STO contact. We have ascertained the ohmic nature of LSCO/Pt contact by two point *I-V* characteristic. A Rigaku x-ray diffractometer (XRD) with Cu K_α radiation was used for phase and crystallinity analysis. Figure 1 shows the x-ray-diffraction spectrum for a 100 nm LSCO/300 nm STO bilayer on Nb:STO substrate and illustrates the high quality epitaxial nature of the heterostructure. Rutherford backscattering spectroscopy (RBS) was used to measure the composition of the thin films. Capacitor structures with an area of 200 μm × 200 μm were fabricated using standard photolithography and chemical etching. Nb:STO layers were etched for ∼10 seconds using 0.5% Phosphoric acid. Since STO layers can be etched only using HF, etching stops when STO layer is reached. The final heterostructure used in the present work is Ag/Nb:STO/STO/LSCO/Pt. The capacitance-voltage measurements were done using a HP 4194A impedance analyzer. The leakage current through the heterostructure was measured using a Keithley 617 programmable electrometer. An American Probe and Technologies HC5004 temperature controller enabled measurements in the temperature range of 20°C to 200°C.

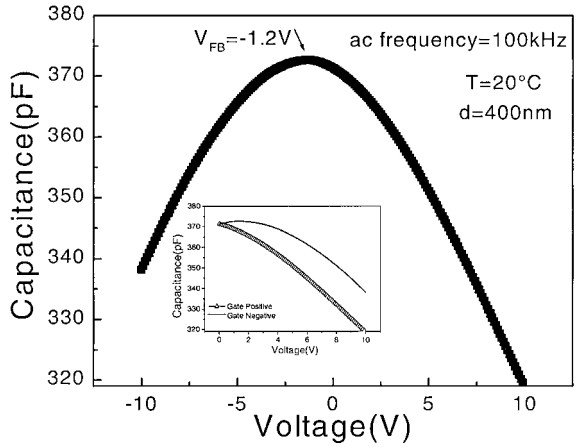

Fig. 2. Small signal *C-V* plot of a typical Nb:STO/STO (400 nm)/LSCO heterostructure. The inset clearly shows that the functional dependence of capacitance is different for positive and negative gate polarities.

Results and Discussion

Figure 2 shows the small signal capacitance-voltage plot of the Ag/Nb:STO/STO (400 nm)/LSCO/Pt heterostructure at 20°C and a frequency of 100 kHz. Note the asymmetry in the *C-V* plot with respect to the polarity of the applied voltage highlighted in the inset. The *C-V* behavior in this heterostructure can be understood by the following argument:

The Ag/Nb:STO and LSCO/Pt contacts being ohmic, the experimental device can be looked upon as a typical MIS capacitor. The LSCO channel used in the experimental device is a p-type material. The application of a negative voltage to the gate electrode induces positive charges in the channel, which are provided by the holes accumulating at the interface. Hence almost the entire applied voltage drops across the STO layer. Possible voltage division due to the presence of a reaction layer (dead layer) at the Nb:STO/STO interface and/or due to interface state charges at the STO/LSCO interface can be reckoned from the magnitude and sign of flat band voltage, V_{FB} and from the thickness dependence of *I-V* and *C-V* measurements as discussed later.

The decrease in capacitance with increasing negative voltages is due to the decrease in the dielectric constant of STO with increasing field. The dependence of the dielectric constant and hence the capacitance of a dielectric with the applied field can be derived from the expression for the free energy. The expression for free energy, G, of a stress free dielectric crystal in the cubic or tetragonal phase can be written in the polynomial approximation (in MKS units) as,

$$G(P) = AP^2 + BP^4 + CP^6 + DP^8 \qquad (1)$$

where P is the polarization along the applied field direction, A, B, C and D are the coefficients. We get the following expression for electric field by differentiating Eq. (1) with respect to P:

$$\frac{\partial G}{\partial P} = E = 2AP + 4BP^3 + 6CP^5 + 8DP^7 \qquad (2)$$

The field dependent part of the expression for the dielectric constant, can be obtained from Eq. (2), through successive approximations as [24]:

$$\varepsilon_E(T) - \varepsilon_0(T) = -KE^2 - LE^4 - ME^6 \qquad (3)$$

where $\varepsilon_E(T)$ and $\varepsilon_0(T)$ are dielectric constants of the dielectric material measured with and without d.c.bias and K, L and M are the coefficients. Iwabuchi and Kobayashi [25] have determined the values of the coefficients A, B, C, D etc. for STO films from the experimental data, from which it can be inferred that the coefficient K is positive for STO unlike in the case of $BaTiO_3$, for which K is shown to be negative [24]. The above authors have found good correlation between the experimental results and the theoretical data calculated using the polynomial expression up to 0.5 MV/cm.

On the other hand, when a positive voltage is applied to the gate electrode, negative charges are induced in the hole-conducting channel by forming a high resistivity depletion region near the interface. The width of the depletion region increases with increasing positive voltages. The overall capacitance would decrease as the channel capacitance is in series with the gate dielectric capacitance.

In the case of a linear dielectric, the capacitance of a typical MIS device under depletion is given by [26]:

$$\frac{C}{C_I} = \frac{1}{\sqrt{1 + \frac{2K_I^2\varepsilon_0}{qN_A K_S x_I^2} V}} \qquad (4)$$

where C is the effective capacitance of the device, C_I is the gate dielectric capacitance, K_I and K_S are the relative dielectric constants of the gate dielectric and the channel material, respectively, x_I is the thickness of

the gate dielectric, N_A is the uncompensated acceptor concentration near the interface and V is the gate voltage. This equation predicts that the total capacitance of the device will decrease as the square root of the gate voltage when the surface is being depleted. Therefore, a plot of $\{[\frac{C_1}{C}]^2 - 1\}$ vs V would be linear and passing through the origin. The intercept on the voltage axis would indicate the presence of capacitances due to the interface state charge and the dead layer coming in series with the MIS capacitance. The direct experimental verification would involve measuring the capacitance with a small ac field superimposed on a larger biasing field.

Even though the *C-V* plots shown in Fig. 2 appear to be symmetric to some extent at lower voltages, the inset in Fig. 2 clearly shows that the voltage dependence of the capacitance is different for the positive and negative polarities of the applied voltage. The functional dependence of the capacitance with voltage for the two polarities is illustrated in Fig. 3. Figure 3(a) shows the measured dielectric constant of STO Vs V for negative (accumulating) voltages (up to 10 V or a field up to 250 kV/cm) on the gate. The observed decrease of dielectric constant with the increase of accumulating voltages is exactly according to the behavior expected of a non-linear dielectric, as reflected by a very good fit of the data to Eq. (3), substantiating that the decrease in the capacitance in this voltage regime is indeed due to the field dependence of the STO dielectric constant. On the other hand, the decrease in capacitance for positive (depleting) voltages on the gate is more complex when a non-linear dielectric such as STO is used as the gate dielectric. When a linear dielectric such as SiO_2 is used as the gate dielectric, the entire change in the capacitance for depleting voltages can be attributed to field modulation of conductivity near the oxide-semiconductor interface. However, when a non-linear dielectric is used, the change in the capacitance for depleting voltages could be both due to the change in the dielectric constant of the gate dielectric and due to the change in the depletion width in the channel. The individual contribution to the change in capacitance depends on the proportion of incremental voltage drop across the gate dielectric and the channel oxide. The asymmetry in the *C-V* plot in Fig. 2, with a steeper drop in the capacitance for depleting voltages when compared to the corresponding accumulating voltages unambiguously shows that there is charge modulation in the channel oxide. However it is not easy to estimate the individual contributions. We tried to explore the extent to which the experimental data deviated from the depletion model by plotting the measured $[\frac{C_{STO}}{C}]^2 - 1$ as a function of V. We obtained a fairly good fit of the experimental data with $[\frac{C_{STO}}{C}]^2 - 1$ vs V behavior in the voltage range 3 V to 8 V shown in Fig. 3(b). The behavior in this voltage region is almost similar to what is expected when a linear dielectric is used. Such a behavior is possible only when the incremental voltage drops mostly across the channel depletion layer and shared very little with the gate dielectric. This is possible when the depletion region resistance is considerably higher

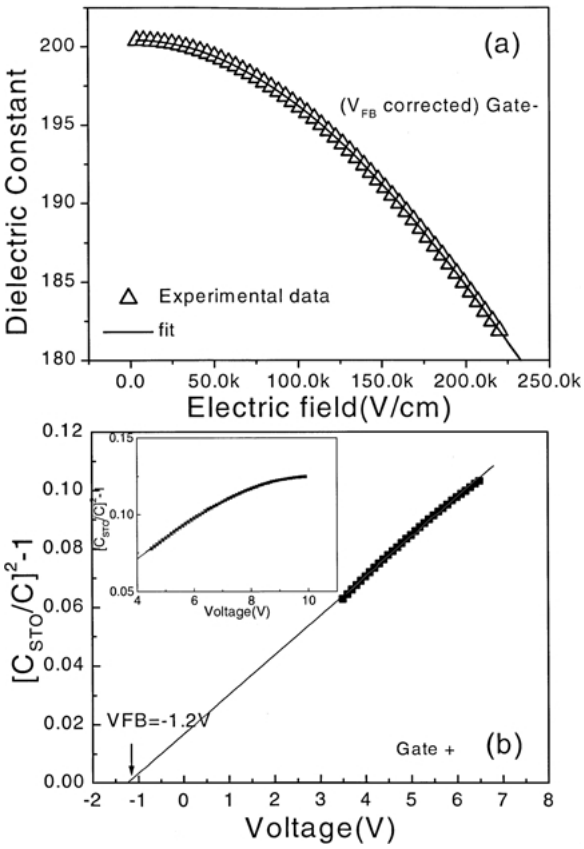

Fig. 3. (a) Dielectric constant vs V plot of a typical Nb:STO/STO (400 nm)/LSCO heterostructure for negative (accumulating) gate voltages. Very good correlation between the experimental result and the theoretical fit using the polynomial equation shows that the decrease in capacitance for accumulating voltages on the gate is due to the non-linear field dependence of STO dielectric constant. (b) $[C_{STO}/C]^2 - 1$ vs V plot for a typical Nb:STO/STO (400 nm)/LSCO heterostructure for positive gate voltages. The linearity of the plot shows that the channel capacitance is in series with the dielectric capacitance. The inset shows that the channel capacitance saturates for large depleting voltages.

compared to that of the gate oxide. The deviation from $[\frac{C_{STO}}{C}]^2 - 1$ vs V law for depletion voltages less than 3 V could be due to the sharing of voltage between the gate oxide and the still-forming depletion layer whose resistance is lesser or comparable to that of the gate oxide depending on the applied voltage. At voltages higher than 8 V, the channel oxide capacitance appears to saturate as seen in the inset of Fig. 3(b). Extrapolation of the plot in the voltage range of 3 to 8 V gives a flat band voltage of -1.2 V. The fact that the flat band voltage seen in the *C-V* plot in Fig. 2 is exactly the same as that obtained by extrapolating the plot in Fig. 3(b) supports the view that the capacitance behavior in this voltage range is in accordance with the depletion model. As a further verification, we calculated the uncompensated acceptor concentration in the LSCO channel from the slope of the room temperature $[\frac{C_{STO}}{C}]^2 - 1$ vs V plot (Eq. (4)). The calculated concentration of $\sim 10^{20}/\text{cm}^3$ is in good agreement with the expected hole concentration in LSCO at room temperature [27]. Further proof that charge modulation is indeed occurring is the experimental observation that the modulation efficiency increases with decrease in STO thickness shown in Fig. 4, wherein we have normalized the capacitance to its maximum value in each case to allow a useful comparison. This dependence is understandable from the fact that as the gate dielectric capacitance increases with decreasing dielectric thickness, the relative voltage drop across the channel depletion layer increases thereby increasing the modulation efficiency.

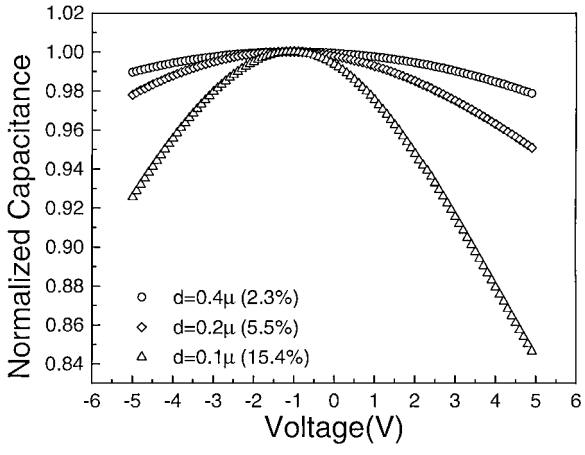

Fig. 4. Normalized *C-V* plots of Nb:STO/STO/LSCO heterostructure showing that the modulation efficiency $(C_{max} - C_{min})/C_{max}$ increases with decreasing STO thickness.

Having established that there is charge modulation in the LSCO channel layer, we now proceed to evaluate the quality of the interface between STO and LSCO. A bad interface in the context of field effect is the one with active interface traps, such as localized electronic states within the interface region that can be classified in to slow and fast interface states depending on the speed with which they interact with the channel oxide space charge region [26, 28]. The charge associated with the slow states is trapped within the gate oxide and cannot move to the channel layer. The gate oxide charges associated with the slow states can be classified as (i) immobile charges and (ii) mobile charges. Immobile ones are held in traps that are part of the intrinsic defect structure of the oxide. The mobile charges are due to ions that are capable of migrating through the oxide at elevated temperatures and high electric fields. Fast interface states are localized states located within 200 Å from the gate oxide-channel interface near the band edges so that they can exchange charge easily with the channel oxide. Injection effects have been well demonstrated in the literature [23, 29].

The following tests were conducted to see if there are fixed charges in the gate oxide and charge trapping at the interface. The small signal capacitance of the device was measured at room temperature at 100 kHz with a test signal of 500 mV (peak to peak) while the dc bias was swept from 0 to negative (accumulating) voltages. The capacitance goes through a maximum and decreases. Simultaneously holes are injected from the channel into the dielectric. If there is trapping of injected carriers, the maximum of capacitance would occur at higher voltages showing an increase in the flat band voltage when the voltage is swept back to zero. Another indication of trapping is the reduction in capacitance maximum consequent to the reduction in dielectric constant at higher voltages. It was seen that the *C-V* plots followed the same path without any hysteresis and without any noticeable change in the flat band voltage when the voltage was swept back and forth from accumulating to depleting voltages with increasing voltage spans. This is illustrated in Fig. 5(a) and (b). This observation clearly shows the absence of mobile charges in the gate oxide and slow interface traps at the STO/LSCO interface. This information was corroborated by the absence of drift and shift in the *C-V* characteristic measured before and after temperature-bias aging by maintaining the device at 200°C for 30 mins. at a field of 5×10^5 V/cm (Fig. 6). However

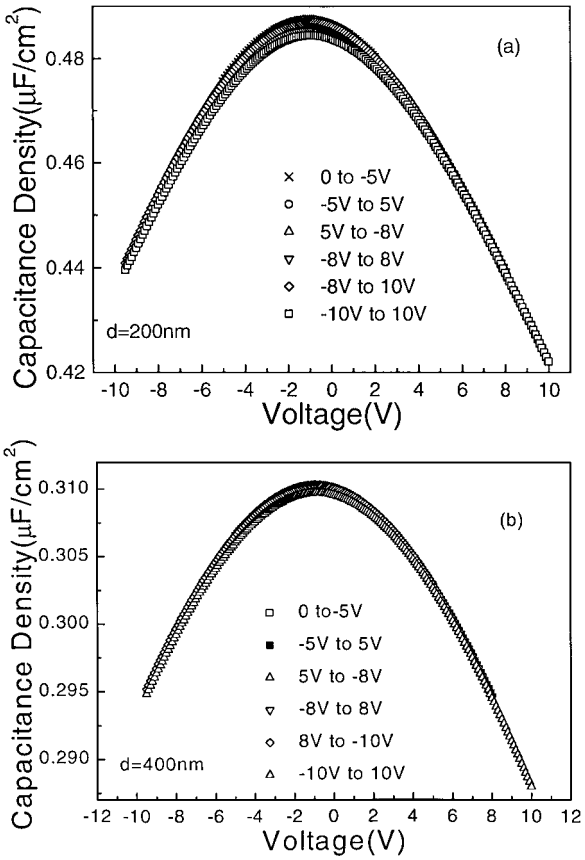

Fig. 5. C-V plots for Nb:STO/STO/LSCO heterostructure with (a) 200 nm and (b) 400 nm thick STO layers, showing no noticeable hysteresis and shift in the flat band voltage when the gate voltage was swept from accumulation to depletion voltages with successively increasing voltage levels.

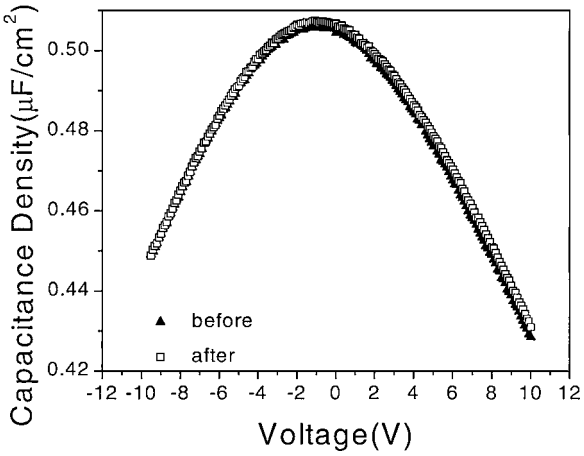

Fig. 6. C-V plots for Nb:STO/STO (200 nm)/LSCO heterostructure before and after temperature-bias aging at 200°C and a field of 5×10^5 V/cm for 30 mins. Note the absence of drift in *C-V* plot and shift in V_{FB}.

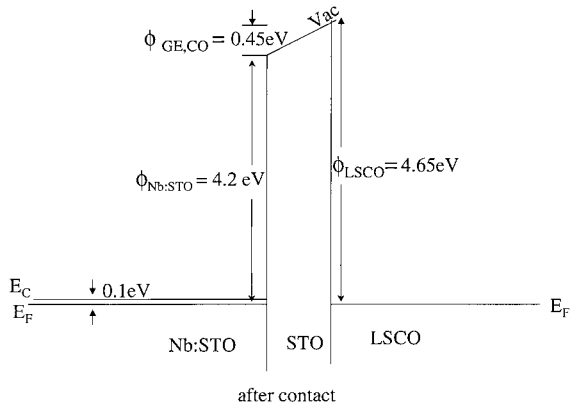

Fig. 7. Energy band diagram showing the work-function difference between 1% Nb doped STO and LSCO.

these tests cannot detect the possible presence of fast interface states.

The interface charges (Q_{ss}) along with gate electrode-channel oxide work function difference ($\phi_{GE,CO}$) and oxide charge (Q_{GO}) shift the flat band voltage from $V = 0$. The contribution of the above charges to the flat band voltage is given by,

$$V_{FB} = \phi_{GE,CO} - (Q_{SS}/C_{STO}) - (Q_{GO}/C_{STO}) \quad (5)$$

The work function difference between 1% Nb doped STO and LSCO has been estimated from the following information as shown in Fig. 7: Reihl and coworkers [30] have experimentally shown that the Fermi level of 1% Nb doped STO is 0.1 eV below E_c. Henrich and coworkers [31] have reported that the electron affinity of STO is 4.1 eV. These experimental data lead to the work function of Nb:STO to be 4.2 eV. However, to the best of our knowledge, we did not find any published report on the work function of LSCO. We have used the experimentally determined work function of LaSrCoO (4.65 eV) [32], as we believe that the work functions of LaSrCoO and LSCO would be similar. The contribution to V_{FB} from gate oxide charges was ignored due to the absence of hysteresis in the *C-V* characteristics and shift in V_{FB} when the device was subjected to voltage cycling and temperature-bias aging. The interface state density calculated from the expression 5 is $\sim 10^{12}/cm^2$. The shift of V_{FB} towards negative voltages

indicates that the interface state charges are positive. Although not shown, *C-V* measurements as a function of frequency did not show any significant frequency dependence of V_{FB}. V_{FB} increased only by ~0.05 V when the signal frequency varied between 100 and 10^6 Hz. This indicates that there is no significant dispersion of interface state trap relaxation times in this frequency range.

The effectiveness of a field effect device for transistor applications very much depends on the leakage property of the gate dielectric and the nature of electrical contact between the gate dielectric and the channel material. Figure 8(a) and (b) show the current-time plots of a typical Nb:STO/STO(200 nm)/LSCO structure for an applied voltage of 5 V at 50°C and

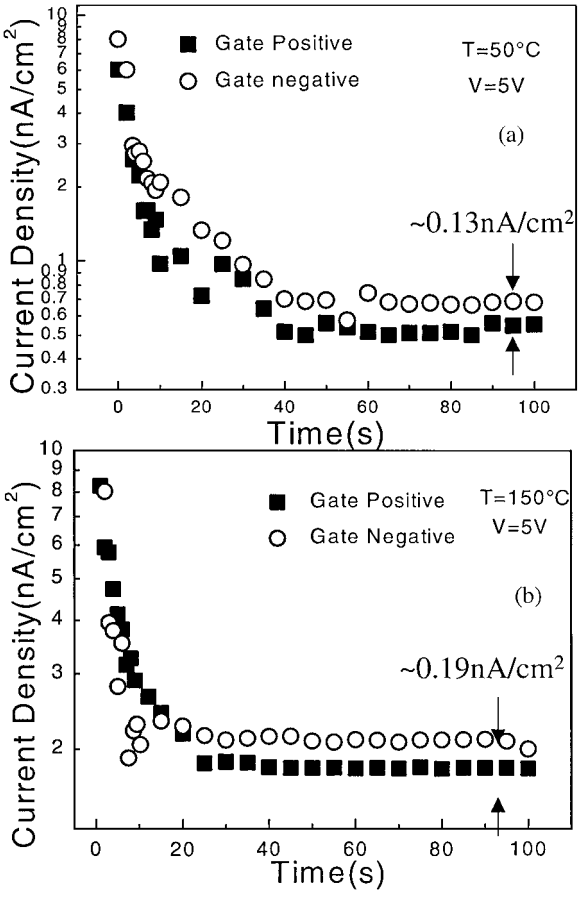

Fig. 8. I-t plots of a typical Nb:STO/STO (200 nm)/LSCO device at 50°C and 100°C for a gate voltage of 5 V. The insignificant polarity dependence of the plots shows that the interfaces are electrically similar (note that the current is plotted on log scale).

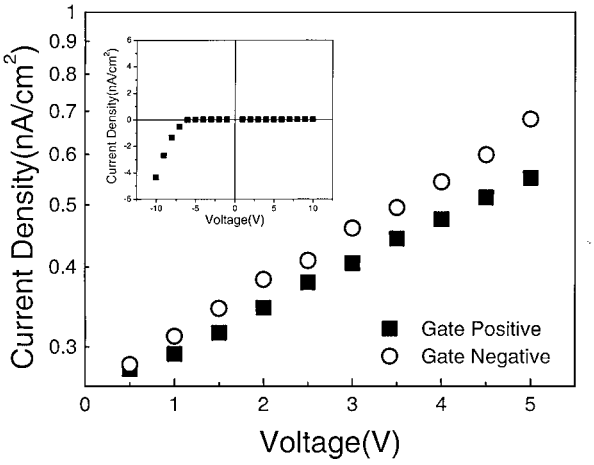

Fig. 9. I-V plot of a typical Nb:STO/STO (200 nm)/LSCO device. Note that there is no significant polarity dependence of current up to ~5 V. The inset shows the polarity dependence of *I-V* beyond ~8 V.

150°C. The steady state current density at 50°C for 5 V is as low as ~0.5 nA/cm^2 illustrating the good insulating property of STO. In our experimental studies we observe a fairly good polarity independence up to ~5 V shown in the plots in Figs. 8 and 9. The difference between the currents at 5 V for positive and negative voltages at 50°C and 150°C (Figs. 8(a) and (b) are ~0.13 nA/cm^2 and ~0.19 nA/cm^2. Fairly good polarity independence up to ~5 V can also be observed in the *I-V* plot in Fig. 9 indicating that the mechanism of conduction in this voltage regime is not interface limited but bulk limited. However, there appears to be significant polarity dependence of current for voltages larger than ~8 V as shown in the inset of Fig. 9 indicating that the mechanism of conduction beyond ~8 V could be interface limited.

Further proof that the mechanism of conduction is bulk limited up to ~5 V is the linear voltage-thickness (*V-d*) dependence for a certain current through the device shown in Fig. 10. This linear dependence indicates that the applied field drops uniformly across the bulk of STO layer and that the field decides the current through the dielectric film. This is possible only in the absence of or insignificant interfacial barrier. Thickness dependent capacitance studies also provide supporting information on the nature of interfaces. Figure 11 shows $1/C_{STO}$ vs d plots for various temperatures where C_{STO} is the capacitance density of the gate dielectric at flat band voltage. The linearity of the plots shows that the capacitance scales with the

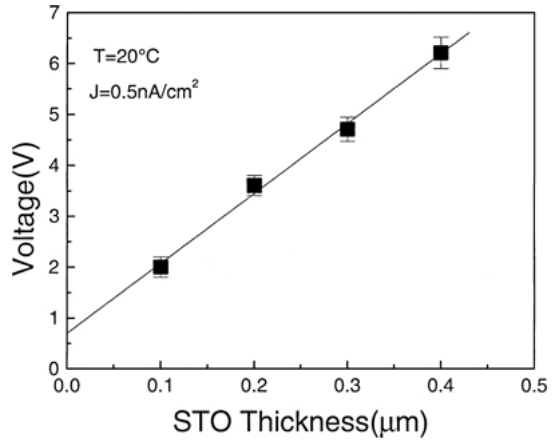

Fig. 10. *V-d* plot of a typical Nb:STO/STO (200 nm)/LSCO device for a current density of 0.5 nA/cm^2. The linearity of the plot in the voltage regime ∼5 V indicates a uniform field in the bulk of STO. Non-zero intercept on the voltage axis indicates the presence of a voltage sharing dead layer.

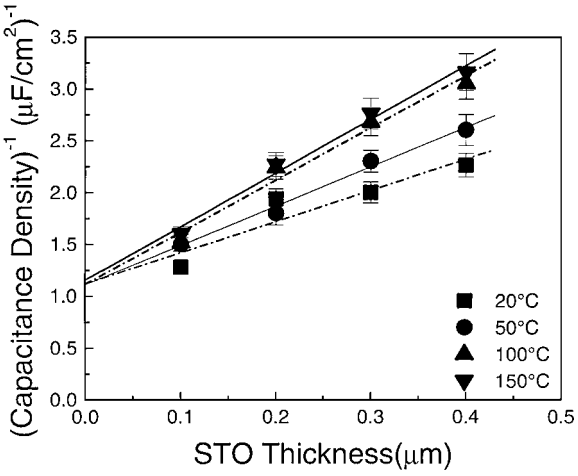

Fig. 11. $1/C_{STO}$ vs d plots of a typical Nb:STO/STO (200 nm)/LSCO device for various temperatures. Finite intercept on the capacitance axis reiterates the presence of a voltage sharing dead layer. However, convergence of the plots for various temperatures to the same point on the capacitance axis shows that the dead layer capacitance is not temperature sensitive and hence is passive.

dielectric thickness. The non-zero intercept similar to what was observed in *V-d* plot (Fig. 10) indicates that there is a series capacitor or a dead layer sharing the applied voltage. It is of interest to investigate whether this voltage-dividing layer is the space charge depletion region resulting from an interfacial Schottky barrier or whether it is a passive dead layer resulting from defect concentration or reaction at the interface [33–36]. This can be inferred from Fig. 11, which shows 1/*C-d* plots for various temperatures converging to the same point on 1/*C* axis. This indicates that the interfacial layer is temperature independent and hence of a passive nature. A possible explanation for the presence of dead layer at the Nb:STO/STO interface is as follows: It is known that during typical growth conditions such as used in this work, Nb doped STO can be turned from the conducting state into a highly insulating state by indiffusion of oxygen. This is a slow process in donor doped STO; still a so-called dead layer can be formed which may have considerable effect on *C-V* and *I-V* measurements. The dead layer effect seen in Figs. 10 and 11 could be due to the insulating layer at the Nb:STO/STO interface.

Conclusions

The field effect and the interface quality of all oxide Nb:STO/STO/LSCO heterostructures were evaluated through *C-V* and *I-V* techniques. These devices show a typical dielectric response for accumulating voltages and field modulation of conductivity in the LSCO channel for the depleting voltages, as is deduced from the voltage/field dependence of the device capacitance for the depleting and accumulating voltages. The majority carrier concentration of $\sim 10^{20}$/cm^3 calculated from *C-V* data by applying depletion theory, is consistent with the expected value. Further, the modulation efficiency is seen to increase with decreasing gate dielectric thickness. These facts unambiguously show that field modulation is indeed occurring in the LSCO channel. The interface quality was tested through *C-V* measurements by sweeping the voltage from accumulting to depleting voltages through successively increasing voltage spans. Absence of hysteresis and shift in the flat band voltage during voltage cycling confirm the absence of trapping due to injection and hence shows that the gate dielectric is free of oxide charge and slow interface state traps. Absence of shift in V_{FB} after temperature-bias aging reiterates the above conclusion. The density of fast surface states calculated from V_{FB} is $\sim 10^{12}$/cm^2. The absence of noticeable frequency dependence of V_{FB} in the frequency range from 100 to 10^6 Hz indicates that there is no significant dispersion of interface trap relaxation times in this frequency range. The nature of the electrical contact between the gate dielectric and the channel oxide was tested through current-time and current-voltage

measurements. A good polarity independence was observed in the *I-t* and *I-V* plots up to ∼5 V. This and the linearity of the *V-d* plot show that the electrical contacts to STO are non-blocking and that the mechanism of conduction through the dielectric is probably bulk-limited in this voltage regime. The linearity of $1/C_{STO}$ vs d plot again confirms the bulk dependence. However, the non-zero intercept observed in both the *V-d* and $1/C_{STO}$ vs d plots show that there is a series component to the dielectric capacitance. In other words the finite intercept indicates a dead layer. The fact that there is no change in the intercept of $1/C_{STO}$ vs d plots for different temperatures shows that the component sharing the applied voltage with the dielectric is not an active but a passive one. The dead layer could possibly have originated due to in-diffusion of oxygen in the interface Nb:STO layer at the typical growth conditions that prevailed during STO deposition. The strong polarity dependence above ∼8 V indicates that the leakage current mechanism in this voltage regime could be interface limited.

Acknowledgment

This work was supported by MRSEC Grant No. DMR-00-80008.

References

1. S.M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
2. J. Mannhart, D.G. Schlom, J.G. Bednorz, and K.A. Müller, *Phys. Rev. Lett.*, **67**, 2099 (1991).
3. J. Mannhart, *Mod. Phys. Lett.* B, **6**, 555 (1992).
4. A.T. Fiory and A.F. Hebard, *Phys. Rev. Lett.*, **52**, 2057 (1984).
5. A.T. Fiory, A.F. Hebard, R.H. Eick, P.M. Mankiewich, R.E. Howard, and M.L. O'Malley, *Phys. Rev. Lett.*, **65**, 3441 (1990).
6. U. Kabasawa, K. Asano, and T. Kobayashi, *Jpn. J. Appl. Phys.*, **29**, L86 (1990).
7. A. Levy, J.P. Falck, M.A. Kastner, W.J. Gallagher, A. Gupta, and A.W. Kleinsasser, *J. Appl. Phys.*, **69**, 4439 (1991).
8. X.X. Xi, Q. Li, C. Doughty, C. Kwon, S. Bhattacharya, A.T. Findikoglu, and T. Venkatesan, *Appl. Phys. Lett.*, **59**, 3740 (1991).
9. H. Lin, N.J. Wu, K. Xie, X.Y. Li, and A. Ignatiev, *Appl. Phys. Lett.*, **65**, 953 (1994); H. Liu et al., *Appl. Phys. Lett.*, **66**, 1172 (1995).
10. Yu.A. Boikov, S.K. Esayan, Z.G. Ivanov, G. Brorsson, T. Claeson, J. Lee, and A. Safari, *Appl. Phys. Lett.*, **61**, 528 (1992).
11. X.X. Xi, C. Doughty, A. Walkenhorst, S.N. Mao, Q. Li, and T. Venkatesan, *Appl. Phys. Lett.*, **61**, 2353 (1992).
12. A. Walkenhorst, C. Doughty, X.X. Xi, Q. Li, C.J. Lobb, S.N. Mao, and T. Venkatesan, *Phys. Rev. Lett.*, **69**, 2709 (1993).
13. Y. Watanabe, *Appl. Phys. Lett.*, **66**, 1770 (1995).
14. Z.W. Dong, Z. Trajanovic, T. Boettcher, I. Takeuchi, V. Talyansky, C.-H. Chen, and T. Venkatesan, in *Proceedings of the 3rd HTS-Workshop on Digital Applications, Josephson Junctions and 3-Terminal Devices*, University of Twente, The Netherlands, April 21–23, 1996, pp. 93–99.
15. S.B. Ogale, V. Talyansky, C.H. Chen, R. Ramesh, R.L. Greene, and T. Venkatesan, *Phys. Rev. Lett.*, **77**, 1159 (1996).
16. V. Talyansky, S.B. Ogale, I. Takeuchi, C. Doughty, and T. Venkatesan, *Phys. Rev.* B, **53**, 14575 (1996).
17. A.P. Ramirez, *J. Phys. Cond. Matter*, **9**, 8171 (1997).
18. Z.W. Dong, Z. Trajanovic, T. Boettcher, I. Takeuchi, V. Talyansky, C.-H. Chen, R.P. Sharma, R. Ramesh, and T. Venkatesan, *IEEE Transactions on Applied Superconductivity*, **7**, 3516 (1997).
19. S. Matthews, R. Ramesh, T. Venkatesan, and J. Benedetto, *Science*, **276**, 238 (1997).
20. D.M. Newns, J.A. Misewich, C.C. Tsuei, A. Gupta, B.A. Scott, and A. Schrott, *Appl. Phys. Lett.*, **73**, 780 (1998).
21. T. Wu, S.B. Ogale, J.E. Garrison, B. Nagaraj, A. Biswas, Z. Chen, R.L. Greene, R. Ramesh, T. Venkatesan, and A.J. Millis, *Phys. Rev. Lett.*, **86**, 5998 (2001).
22. M. Kawasaki, K. Takahashi, T. Maeda, R. Tsuchiya, M. Shinohara, O. Ishiyama, T. Yonezawa, M. Yoshimoto, and H. Koinuma, *Science*, **266**, 1540 (1994).
23. H.-M. Christen, J. Mannhart, E.J. Williams, and Ch. Gerber, *Phys. Rev.* B, **49**, 12095 (1994).
24. F. Jona and G. Shirane, *Ferroelectric Crystals* (Dover publications, New York, 1993), p. 134.
25. M. Iwabuchi and T. Kobayashi, *J. Appl. Phys.*, **75**, 5295 (1994).
26. A.S. Grove, *Physics and Technology of Semiconductor Devices* (John Wiley and Sons, New York), p. 272.
27. N.P. Ong, Z.Z. Wang, J. Clayhold, J.M. Tarascon, L.H. Greene, and W.R. McKinnon, *Phys. Rev.* B (Rapid Commun), **35**, 8807 (1987).
28. E.H. Nicollian and J.R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (John Wiley & Sons, New York, 1982).
29. Y. Wu, *IEEE Trans. Electron Devices*, **ED-21**, 499 (1974).
30. B. Reihl, J.G. Bednorz, K.A. Muller, Y. Jugnet, G. Landgren, and J.F. Morar, *Phys. Rev.* B, **30**, 803 (1984).
31. V.E. Henrich, G. Dresselhaus, and N.J. Zeiger, *Phys. Rev.* B, **17**, 4906 (1978).
32. B. Chalamala, S. Aggarwal, B. Nagaraj, and R. Ramesh, unpublished.
33. C. Zhou and D.M. Newns, *J. Appl. Phys.*, **82**, 3081 (1997).
34. H.-C. Li, W. Si, A.D. West, and X.X. Xi, *Appl. Phys. Lett.*, **73**, 464 (1998).
35. J.Z. Sun, D.W. Abraham, R.A. Rao, and C.B. Eom, *Appl. Phys. Lett.*, **74**, 3017 (1999).
36. S. Stadler, Y.U. Idzerda, Z. Chen, S.B. Ogale, and T. Venkatesan, *Appl. Phys. Lett.*, **75**, 3384 (1999).