The Design and Linearization of 60GHz Injection Locked Power Amplifier

A Thesis Presented by

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Abstract

The RF power amplifier is one of the most critical blocks of transceivers, as it is expected to provide a suitable output power with high gain, efficiency and linearity.

In this paper, a 60-GHz power amplifier based on an injection locked structure is demonstrated in a standard 65 CMOS technology. The PA core consists of a cross-coupled pair of NMOS transistors with an NMOS current source. This structure can achieve large output power and high PAE, but with poor linearity performance. In order to improve the linearity, several linearization techniques are investigated, including adaptive biasing and predistortion. The results show that the adaptive biasing technique can enlarge the linear operation region, but results in poor AM-PM performance. By instead using the predistortion technique, the AM-PM performance can be improved, but the linear region only extends slightly. Considering theses two techniques different advantages, we combine them together to improve not only the linear region but also the AM-PM performance.

Finally, a common source amplifier is added as the first stage. With proper bias, the linear operation region is then effectively extended by 7.3 dB. This two stage power amplifier achieves large output power, high linearity and high PAE simultaneously. It delivers a gain of 20dB, a P_{sat} of 16.3dBm, a P_{1dB} of 15.41dBm, and a PAE of 30%.

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Contents

Chapter 1

Introduction

1.1 Motivation for 60 GHz CMOS Power Amplifiers

Since the invention of radio-frequency (RF) wireless communication more than 100 years ago, mobile phones and other wireless communications products for civilian consumption have developed rapidly, especially in recent years. From the view of the personal mobile communication, the personal-oriented commercial mobile communication technology has expanded from Advantage mobile phone system (AMPS) to today's Time division long term evolution (TD-LTE), Frequency division duplex long term evolution (FDD-LTE) and so on. As another application for wireless communication, the accessing technology of broadband network is developing rapidly and it becomes a very active area. In recent years, new technologies are constantly emerging such as Bluetooth, Ultra wideband (UWB), Radio frequency identification devices (RFID) and Near field communication (NFC). There are two developing trends: one is towards low power consumption, including the RFID and NFC technologies; another is towards high bandwidth such as UWB technology.

Nowadays, with the rapid development of the communication system, the demand for larger volume and high data rate also rises sharply. The traditional wireless bandwidth is no longer able to meet some high-rate applications requirement. Based on Shannon's theorem, the maximum possible date rate of the communication channel is given by:

$$C = BW log_2(1 + \frac{S}{N}) \quad (1.1)$$

Where C is the maximum possible data rate, BW is the bandwidth of the channel, S is the total received power over the bandwidth, and N is the total noise power. It is obvious that the maximum data rate increases with increasing channel bandwidth.

Nowadays, the spectrum around 60GHz is available in various region over the world shown in Table 1. This available spectrum can enable a huge channel bandwidth (2500 MHz) compared to other wireless communication standards. Hence, it will take tremendous push function to the development and expansion. The 60GHz-band short-distance communication technology has become the hot topic of applied research. An enormous amount of research effort goes into designing mm-wave CMOS circuits for the up to 7 GHz unlicensed wide band around 60GHz and it brings not only opportunities but also challenges.

However, the free-space loss in 60 GHz band is high due to the oxygen absorption. This limits the maximum distance of communication. While this limit distances also offers interference and security advantages which make 60GHz band has prevailed for short-range, high data rate and high security wireless communication[1][2][3].

The 60Ghz band is developing under the IEEE standard 802.15.3c, 802.15.11ad, and the European Computer Manufacturers Association (ECMA) standard 387. And there are a lot of usages for communication at the band, such as the wireless personal area networks (WPANs) and wireless local area networks (WLANs). The application areas is including borne radar, cordless telephone, military use, medical endoscopes, high-definition TV (HDTV) and so on.

Region	Low frequency	High frequency	Bandwidth
USA	57 GHz	64 GHz	7 GHz
Canada	57 GHz	64 GHz	7 GHz
Europe	57 GHz	66 GHz	9 GHz
Japan	59 GHz	66 GHz	7 GHz
Australia	59.4 GHz	62.5 GHz	3.1 GHz

Table 1. Allocation of spectrum around 60 GHz in the various region around the world[4]

Traditionally, technologies based on SiGe and III-V semiconductor are widely used in millimeter-wave circuits and communication system. A direct advantage is that the high power gain and output can be achieved, and solve the signal attenuation

problem in such a high frequency band. However, its obvious disadvantage is the high cost manufacturing and low integration. This greatly limits the mass production and integration in system level and it can't realize the real SOC(system on chip). Hence, CMOS technology due to feasibility, low cost, low power consumption and high integration has become a trend. Moreover, with the increasing technological sophistication, the maximum frequency of operation (f_T) for the 90nm technology node is above 100GHz and it continues to increase for smaller nodes. The continuous progress of the CMOS technology make it possible for the millimeter wave communication system.

As we have seen, the RF power amplifier as the last building block before the antenna is critical for wireless communications system. In order to achieve high data rate, some complex digital modulation schemes are needed, which require highly linear transmitter to minimize both error vector magnitude (EVM) and spectral regrowth[5][6]. At the same time, the power amplifier contributes the most of power consumption of the whole transceiver, which means the efficiency of the power amplifier is significant, it directly determines the quality of the whole system. Besides the efficiency and linearity, the size, gain, output power level are also very important. However, it is impossible to maximize all the design criteria at the same time, some tradeoffs should be made.

Moreover, the power amplifier design realized by CMOS process at millimeter wave faces great challenges, such as the low breakdown voltage, parasitic capacitance and limited gain due to the low transconductance. And with the dimensions of the CMOS scaling down, the supply voltage dropping results in the low output power and bad performance as well. For example, with the breakdown voltage dropping, the supply voltage decreases. In order to maintain the same power as before, the current has to be increased. The increased current will result in reduction of the gain and efficiency due to the parasitic resistor; Moreover, to obtain larger DC current, we need to increase either the amplitude of the input signal or size of the transistor.

However, this will reduce the gain and much more parasitic capacitance will be introduced.

1.2 About this thesis work

This thesis is carried out at the Department of information and Electrical Technology (EIT) at Lund University. The main objective of this thesis project is to design a 60 GHz-Band injection locked power amplifier and increase linearity while maintaining the power gain and efficiency. In this thesis, all the circuits are designed by using the STM 65nm CMOS process.

1.3 Organization

This chapter provides a background based on RF wireless communication system at 60 GHz band frequency, and poses the motivation for CMOS power amplifier.

Chapter 2 reviews the basic structure and performance metrics of RF power amplifier. And different classes of power amplifiers are discussed as well.

Chapter 3 introduces a power amplifier based on the injection locked structure and explain its principle of operation.

Chapter 4 describes the linearization theory; several techniques are used to extend the linear operation. And the simulation results of each techniques are described and analyzed.

Chapter 5 summarizes the thesis and further work is also discussed.

Chapter 2

RF Power Amplifier Basics

2.1 Introduction

RF power amplifier is widely used in the wireless communication system. It is used to provide the output signal at a desirable gain with high linearity and efficiency. It should fulfill the output power requirement, which is the greatest different from small-signal amplifier. Due to the high power output, the transistor normally operates in large-signal model, and non-linear phenomenon is obvious. The characteristic of RF power amplifier is low power and large current. In order to withstand large current, the chip area must be increased. At the same time, parasitic capacitance and resistance increases as well and it results in degraded operating frequency and efficiency. Furthermore, the impedances of the input and output are complex number and it is hard to perform impedance matching. In order to get maximum output power and efficiency, the matching network is indispensable. A complete RF amplifier is normally consists of input matching network, DC biasing circuit, transistor amplifier circuit and output matching network. The basic block of RF power amplifier is shown in Fig. 2.1.

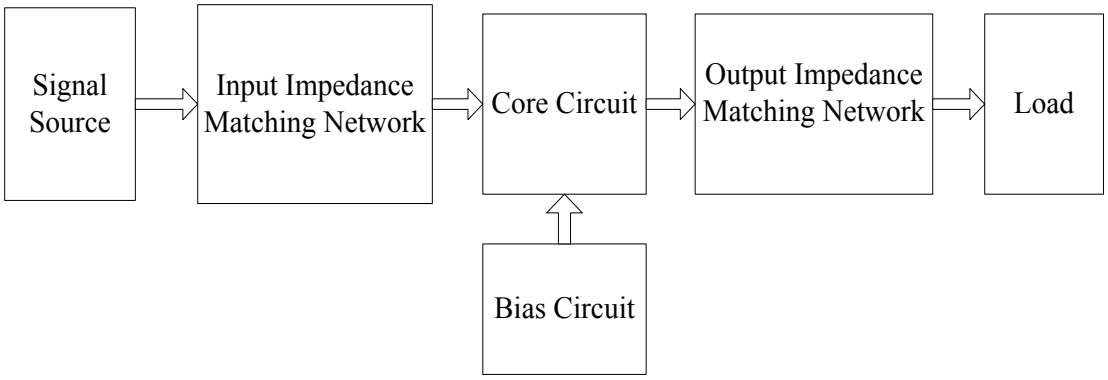

Fig. 2. 1Basic block of RF power amplifier

2.2 Performance metrics of power amplifiers

Many metrics are used to evaluate the performance of power amplifiers. In this section, some of the important metrics are discussed, such as the power gain, efficiency and linearity.

2.2.1 Power gain and Bandwidth

Power amplifier is required to amplify the power of the input signal. Hence, the level of the gain is power gain which is defined as the ratio of the output power delivered to the load to the input power.

$$G = \frac{Power\ delivered\ to\ the\ load}{Power\ at\ the\ input} = \frac{P_{out}}{P_{in}} \quad (2.\ 1)$$

If the input is sinusoidal signal and the load is a resistor, the power can be written as:

$$P_{out} = \frac{\hat{v}\hat{\imath}}{2} = \frac{\hat{v}^2}{2R} = \frac{\hat{\imath}^2 R}{2} \quad (2.\ 2)$$

Where $\hat{v}$ and $\hat{\imath}$ are the amplitudes of voltage and current swing respectively. And for most of the case, the output impedance is equal to 50 Ω.

The power amplifier bandwidth is the range of frequency for which the PA can obtain acceptable performance. Normally, it is defined as the frequency range for which the corresponding gain can be maintained at least 0.7 times of the peak value and is also called 3-dB bandwidth.

2.2.2 Stability

Stability is an important criteria that should be considered in power amplifier design. This is important because oscillation is a highly undesirable phenomenon. In such cases the amplifier performance may change strongly and it may lead to circuitry damage.

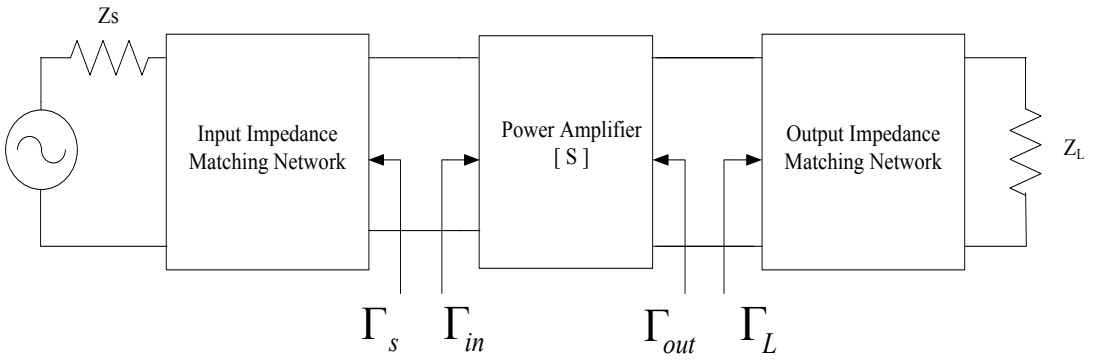

Fig. 2. 2 Block diagram of a one-stage PA

Fig.2. 2 shows the two-port system of power amplifier, Γ_{in} and Γ_{out} can be expressed in terms of transistor S-parameters and reflection coefficients (Γ_S and Γ_L) as given:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2. 3}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2. 4}$$

Oscillations are possible when resistance at the input or output are negative. And the power amplifier is unconditional stability when it meet the following conditions.

$$|\Gamma_S| < 1 \tag{2. 5}$$

$$|\Gamma_L| < 1 \tag{2. 6}$$

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2. 7}$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{2. 8}$$

Another way to mathematically express the necessary and sufficient conditions for unconditional stability is:

$$K_f = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2. 9}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2. 10}$$

2.2.3 Power Efficiency

Power efficiency is one of the most important PA performance metrics. It measures the ability of converting the DC power to the RF power at the output. An efficient PA will deliver most of the power drawn from the supply to the load. On the other hand, power amplifier with low efficiency will result in high level of heat dissipation. In the wireless transceiver, the power amplifiers are the most power-consuming components. Hence, to preserve the battery lifetime, the efficiency of PA is of great importance.

There are three definitions are commonly used: the drain efficiency, the power added efficiency and the overall efficiency.

The drain efficiency of PA is defined as:

$$\eta_{drain} = \frac{P_{Out}}{P_{DC}} \tag{2. 11}$$

Where P_{DC} is the DC power supplied to the amplifier, and P_{out} is useful signal power delivered to the load. The DC supply power can be written as:

$$P_{DC} = V_{DC} I_{DC} \tag{2. 12}$$

An ideal PA has η=100%, which implies that the entire supply power is delivered to the load. However, this is practically impossible to obtain. The drain efficiency ignores the input power to the PA, and in most of case, especially the high-frequency power amplifier, the overall power gain is low, the input power may become a substantial portion of the output power. The results we got from this definition will be higher than the real efficiency. In this case, the power added efficiency and the overall efficiency will be introduced to provide a more accurate measure of PA performances.

Power added efficiency (PAE) is defined as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = (1 - \frac{1}{G}) \frac{P_{out}}{P_{DC}} = (1 - \frac{1}{G})\eta \tag{2. 13}$$

Where P_{in} is the power of the input signal, and G is the overall power gain of the

PA. The power added efficiency is less than the drain efficiency, considering the input RF power. If the power gain is higher than 20dB, the input power can be ignored and at this time PAE is the same with drain efficiency. While the overall efficiency ($\eta_{overall}$) is defined as:

$$\eta_{overall} = \frac{P_{out}}{P_{DC} + P_{in}} \tag{2. 14}$$

To achieve a high efficiency, the power amplifier is always operated to a point near its point of saturation. Unfortunately, at the same time, the distortion will occur. Doherty amplifier circuit topology and Envelope-tracking power supply methods can be employed to improve the efficiency without sacrificing linearity.

2.2.4 Linearity

Besides efficiency, linearity is another key parameter for evaluating the performance of the power amplifier. For all the power amplifier, the relationship between the input and output is non-linear, especially when the signal is large. Assume the amplifier is a memoryless system, the transfer characteristic can be fit by the third order function approximately.

$$y(t) = \alpha_1 A cos\omega t + \alpha_2 A^2 cos^2 \omega t + \alpha_3 A^3 cos^3 \omega t \tag{2. 15}$$

If the input signal is sinusoidal waveform, $x(t) = Acos(\omega t)$, the output signal is:

$$\begin{aligned} y(t) &= \alpha_1 A cos\omega t + \alpha_2 A^2 cos^2 \omega t + \alpha_3 A^3 cos^3 \omega t \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) + \frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) \end{aligned} \tag{2. 16}$$

where $\left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t)$, $\frac{\alpha_2 A^2}{2}\cos(2\omega t)$ and $\frac{\alpha_3 A^3}{4}cos(3\omega t)$ are the fundamental component, second harmonics and third harmonics respectively. As we have seen, because of its nonlinear characteristics, the amplifier not only amplifies the input signal but also produce the harmonics. The amplification of the input signal is

$a_1 + 3a_3A^3/4$. If A is small enough, the amplification approximately equals to a_1 which is constant. This means the gain of the amplifier is constant and the amplifier has a good linear behavior. However, as the input signal level increase, $3a_3A^3/4$ becomes a substantial portion of this part, and the amplification drops, because $a_3 < 0$, ($a_3 > 0$ would mean that the amplifier oscillates, or that the quiescent point is close to the breakdown voltage)[7]. This gain compression phenomena is also called AM-AM distortion. And the concept of 1-dB compression point is proposed, which is defined as the power level where the amplification is 1dB less than the linear gain. 1-dB compression point is often used to measure the linearity of the amplifier and we can obtain this by measurement of output vs. input power. (see Fig. 2. 3).

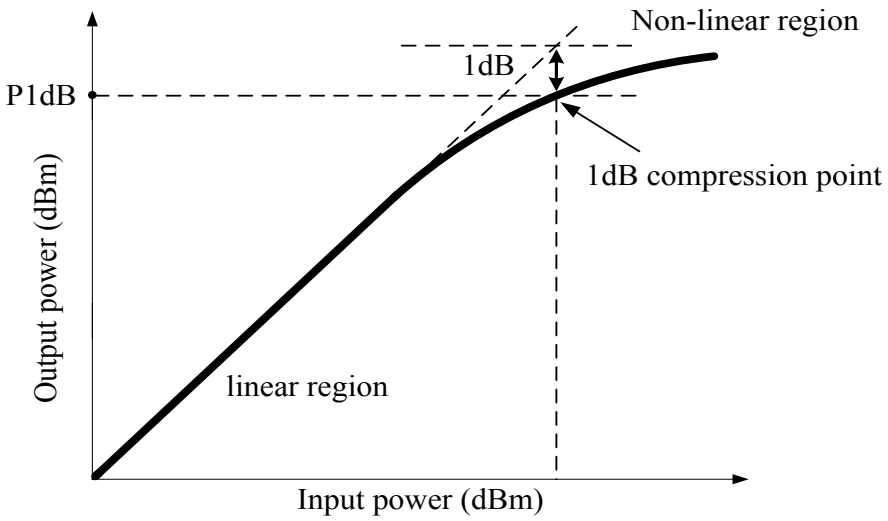

Figure 2. 4 Output vs. input power and 1-dB Compression point

Besides the AM-AM distortion, the amplifier nonlinearity will also cause the AM-PM distortion which is a phenomenon that the phase of the output depends on the level of the input. The AM-PM distortion is caused by the parasitic capacitance variation, especially the input gate capacitance. In other words, the output phase will follow the level of the input signal due to the variability of the capacitance and due to

this distortion, the modulation schemes such as OFDM is badly affected.

When the amplifier has two input signals with the same amplitude and similar frequency simultaneously, i.e. for $X_i(t) = A\cos\omega_1 t + A\cos\omega_2 t$. The output can be calculated by submitting the input signal into the transfer characteristics equation.

$$y(t) = (\alpha_1 A + \frac{9}{4}\alpha_3 A^3)cos\omega_1 t + (\alpha_1 A + \frac{9}{4}\alpha_3 A^3)cos\omega_2 t + \frac{3}{4}\alpha_3 A^3 cos(2\omega_1 - \omega_2)t + \frac{3}{4}\alpha_3 A^3 cos(2\omega_2 - \omega_1)t + \frac{1}{2}\alpha_2 A^2 cos2\omega_1 t + \frac{1}{2}\alpha_2 A^2 cos2\omega_2 t + \ldots \quad (2.17)$$

As can be seen, the output not only consists of the fundamental component (frequencies ω_1, ω_2), their harmonics (frequencies $2\omega_1$, $2\omega_2$) , but also the result of mixing of the input tones (frequencies $2\omega_1 - \omega_2$, $2\omega_2 - \omega_1$). Except for the fundamental parts, the additional signal are generated due to the PA nonlinearity. Of all the possible intermodulation products, the third order intermodulation component with the frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are the most critical. Because they have large amplitude and it is almost impossible to filter out as they are close to the carrier frequencies ω_1 and ω_2, and they can cause interference in multichannel communication. The IMD3 increases as the input power increases, and it is a theoretical point at which the desired output signal are equal to the third-order IM. This theoretical points is the IIP3 and the corresponding output is OIP3. IP3 is also widely used to evaluate the linearity of PA. A higher IP3 means lower distortion generation and better linearity performance. Fig.2.5 shows the output spectrum around the input tones, Fig.2.6 shows the third-order intercept point.

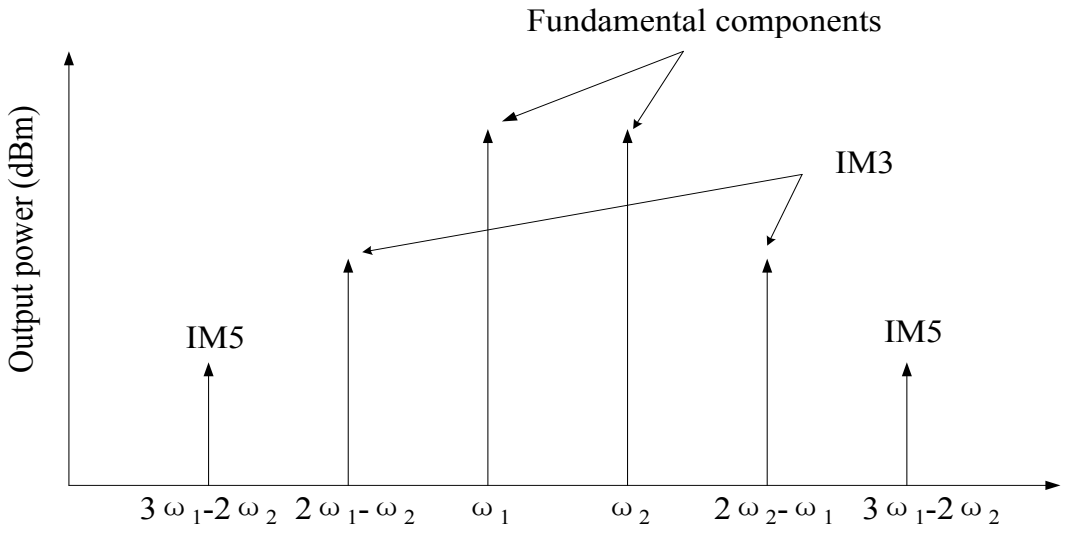

Fig. 2. 5 shows the output spectrum around the input tones

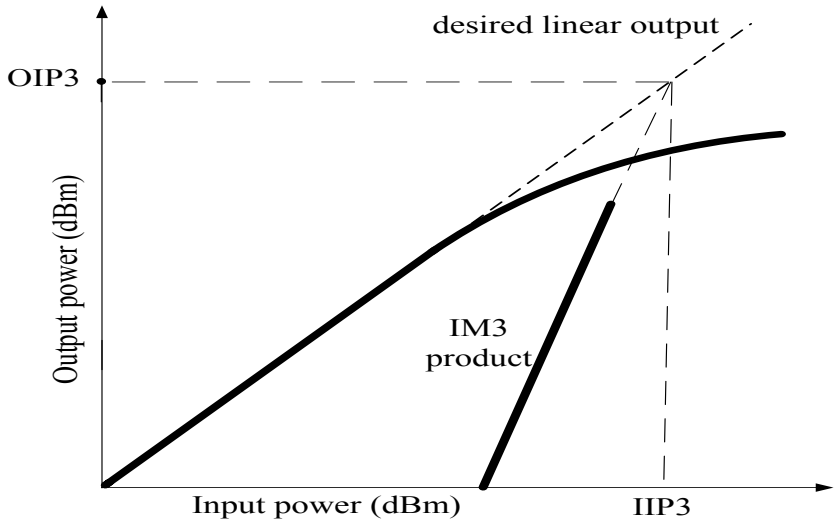

Fig. 2. 6 The third-order intercept point

2.3 Class of PA operation

The power amplifier can be divided into two types: Linear amplifiers and switching-mode amplifiers. Conventional linear amplifiers include Class-A, Class-AB, Class-B, and Class-C amplifiers and the transistor acts as a current source. These amplifiers can achieve high linearity with low efficiency. Switching-mode amplifiers include Class-D, Class-E, and Class-F amplifiers and the transistor acts as a switch. Theses amplifiers can achieve high efficiency at the price of linearity.

2.3.1 Linear power amplifiers

For the linear power amplifiers, the output signal is a linear function of the input signal. Class-A, Class-AB, Class-B and Class-C amplifiers can be seen as linear amplifiers and they have almost the same configuration which is shown in Fig 2.7.

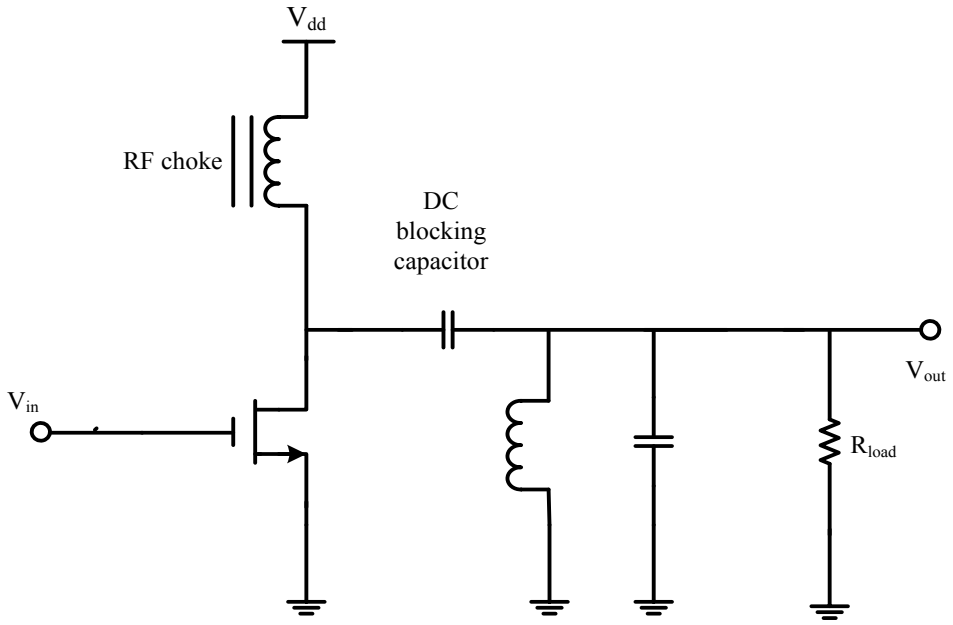

Fig. 2. 7 Typical configuration of class-A power amplifier

This circuit consists of a transistor, a RF choke, a DC blocking capacitor, a parallel LC tank and the load. The transistor remains in saturation region is used as a current source, driving a controlled current into the load network, and this current has the same shape with the input signal. The RF choke is a large inductor which provides the constant DC current to the transistor and also prevent the AC signal leaking into the supply. DC blocking capacitor blocks the DC current flowing into the load. The parallel LC tank tuned to be resonant at the fundamental frequency is used to filter out the out-of-band emission result from the non-linearity of the transistor[8][9].

2.3.1 .1 Class-A Power amplifier

Class-A power amplifier is the simplest, but has the highest linearity power amplifier over the other classes of operation. And it is similar with the small-signal amplifier. The main difference is the signal current in the small-signal amplifier is

small, it can't affect the biasing condition. But in power amplifier, in order to maximize the efficiency, the signal current may become a substantial portion of the biasing current and thus the certain distortion is inevitable.

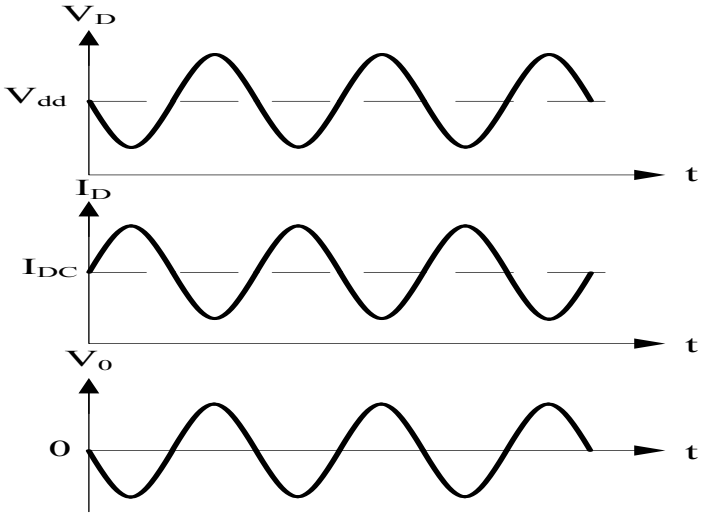

Fig. 2. 8 Voltage and current waveforms of an ideal class-A power amplifier

Class-A power amplifier achieve high linearity at the cost of efficiency. We can analyze the efficiency quantitatively, assuming that the power amplifier is perfectly linear, and the input is sinusoidal. The drain current of the transistor consists of the quiescent current and the signal current.

$$I_{DS}(t) = I_{DS,Q} + \hat{i}_d sin\omega_0 t \tag{2. 18}$$

Where $I_{DS,Q}$ is the quiescent current, $\hat{i}_d$ is the amplitude of the signal current swing and ω_0 is the signal frequency. The output voltage equals the signal current times load resistance.

$$V_0(t) = -\hat{i}_d R sin\omega_0 t \tag{2. 19}$$

The corresponding drain voltage consists of the DC voltage and signal voltage.

$$V_{DS}(t) = V_{dd} + V_0(t) = V_{dd} - \hat{i}_d R sin\omega_0 t \tag{2. 20}$$

The current and voltage waveforms is shown in Fig 2. 8. It is obvious that both the current and voltage on the transistor are large than zero during the entire period, which means the transistor dissipates power all the time.

The drain efficiency of the amplifier is:

$$\eta_{drain,max} = \frac{P_{out}}{P_{DC}} = \frac{\frac{1}{2}\hat{i}_d^2 R}{V_{dd} I_{DS,Q}} = \frac{\hat{i}_d R}{2V_{dd}} = 50\% \quad (2.\ 21)$$

The class-A amplifier is the most linear amplifier and have the highest gain. However, its biggest disadvantage is the ideal maximum efficiency of 50%., and any loss will further reduce its efficiency. In addition, the peak voltage across the transistor of $2V_{dd}$ is large. Therefore, the class-A amplifier is usually used in applications requiring high linearity, high gain, high-frequency operation.

2.3.1.2 Class-B Power Amplifiers

In order to increase the efficiency, the concept of the conduction angle is proposed. The idea is to bias the transistor with low quiescent voltage and the transistor conducts only for part of the cycle. In other words, the voltage waveform is the same as class-A amplifier, but the current waveform has a period time during which the current is equal to zero. And when it occurs, the voltage always gets the maximum value, so this technique can increase the efficiency obviously.

For the class-B amplifier, the conduction angle is π, meaning the transistor conducts only half of the period. The waveform of the drain voltage and current is shown in Fig. 2.9.

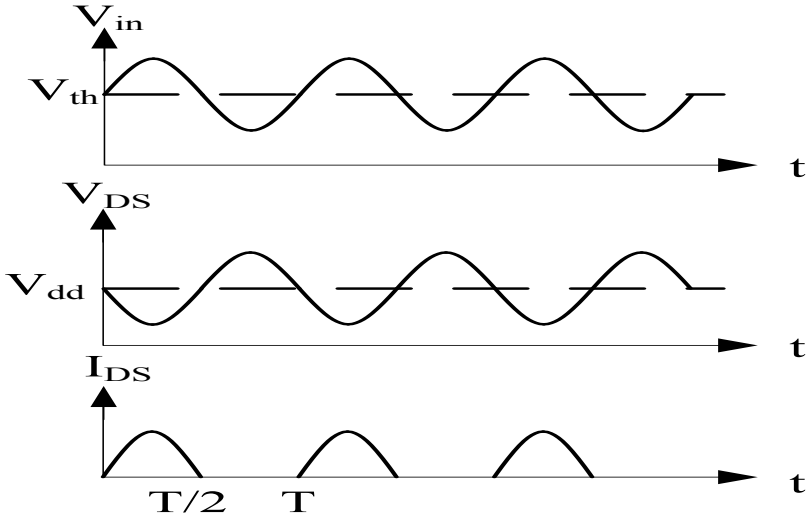

Fig. 2. 9 Voltage and current waveforms of an ideal class-B power amplifier

As we can see, the drain voltage waveform is the same as class-A amplifier, the drain current clipping occurs when the input signal level is less than the threshold voltage, and it can be written by:

$$I_{DS}(t) = \begin{cases} \hat{i}_d sin\omega_0 t, & if\ 0 < \omega t < \pi \\ 0, & otherwise \end{cases} \quad (2.\ 22)$$

The fundamental current is shown as below:

$$i_{fund} = \frac{2}{T}\int_0^{T/2} \hat{i}_d (sin\omega_0 t)(sin\omega_0 t)dt = \frac{\hat{i}_d}{2} \quad (2.\ 23)$$

The output voltage equals to the current times resistance:

$$V_0 = \frac{\hat{i}_d}{2} R sin\omega_0 t \quad (2.\ 24)$$

Since $V_0 \leq V_{dd}$, from the equation above we can get the maximum value for $\hat{i}_d$

$$\hat{i}_{dmax} = \frac{2V_{dd}}{R} \quad (2.\ 25)$$

And the average drain current can be calculated as:

$$\overline{i_d} = \frac{1}{T}\int_0^T I_{DS}(t)dt = \frac{\omega}{2\pi}\int_0^{\frac{\pi}{w}} \hat{i}_d sin\omega_0 t\ dt = \frac{\hat{i}_d}{\pi} = \frac{2V_{dd}}{\pi R} \quad (2.\ 26)$$

The maximum output voltage swing is $V_{dd,}$ so the maximum output power is:

$$P_{o,max} = \frac{V_{dd}^2}{2R} \quad (2.\ 27)$$

The DC power is given by:

$$P_{DC} = \frac{2V_{dd}^2}{\pi R} \quad (2.\ 28)$$

Thus, the maximum efficiency of the class-B amplifier is:

$$\eta_{max} = \frac{P_{o,max}}{P_{DC}} = \frac{\pi}{4} = 0.785 \quad (2.\ 29)$$

As we have seen, class-B amplifier is much more efficient than class-A amplifier, and its maximum efficiency reaches to 78.5%. However, the linearity is worse, and harmonic distortion will occur. Hence, the filter is necessary to eliminate the harmonics. In other words, the class-B amplifier can achieve increased efficiency at the cost of reduced linearity.

2.3.1.3 Class-AB Amplifier

The class-AB amplifier is a compromise between class A and class B amplifier in terms of efficiency and linearity, and it has a conduction angle of $\pi < \theta < 2\pi$. The maximum drain efficiency is between 50% and 78.5% and the linearity is also between class-A and class-B. The corresponding waveforms are shown in Fig. 2.10.

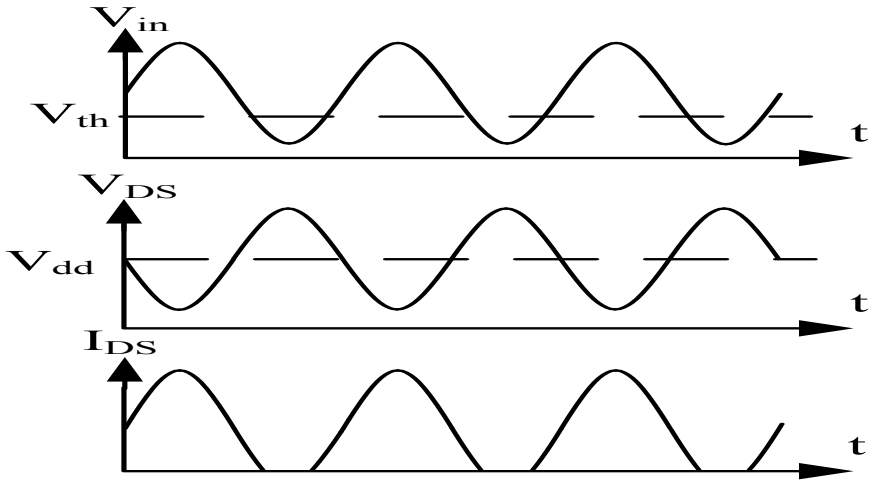

Fig. 2. 4 Voltage and current waveforms of an ideal class-AB power amplifier

2.3.1.4 Class-C Amplifier

In the Class-C mode, the conduction angle is less than π, and the transistor remains in the saturation region for less than half of the RF cycle. The overlapping between the drain voltage and current decreases compared to the Class-A and Class-B mode. However, due to the fixed maximum drain current, the amount of charge that can be injected into the load also diminishes and the output power drops. In order to maintain the output power level, the amplitude of input signal should be increased . In other words, the overall power gain decreases as the conduction angle. Fig 2. 5 shows the voltage and current waveforms of a Class-C PA.

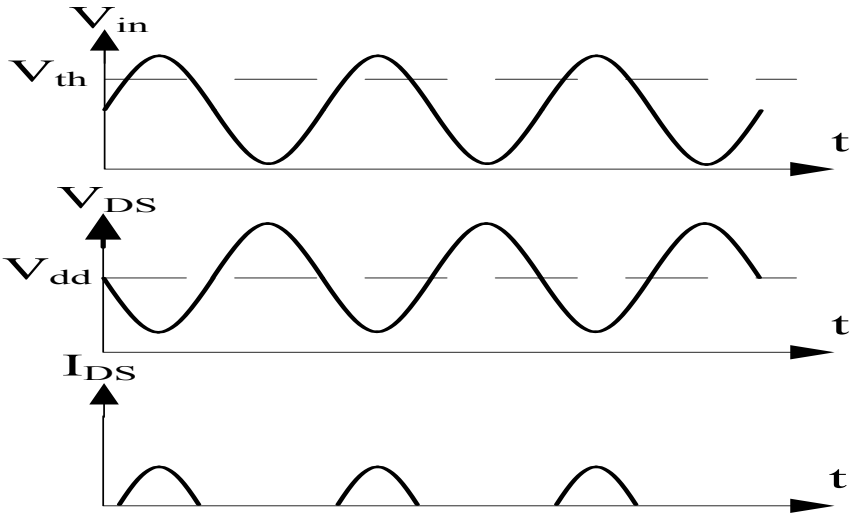

Figure 2. 6 Voltage and current waveforms of an ideal class-AB power amplifier

The maximum drain efficiency of the amplifier can be calculated from the following equation:

$$\eta_{max} = \frac{1}{4} \frac{\theta - sin\theta}{\sin\left(\theta/2\right) - \left(\theta/2\right)cos\left(\theta/2\right)} \quad (2.\ 30)$$

This equation can be also applied to all types of transconductance amplifiers. Where θ is the conduction angle, which is 2π for class-A, π for Class-B, between π and 2π for Class-AB and less than π for Class-C.

Besides efficiency, the output power is related to the conduction angle, the coefficient equation can be specified as:

$$P_{out} \propto \frac{\theta - sin\theta}{1 - cos(\vartheta/2)} \quad (2.\ 31)$$

It illustrates that the maximum efficiency of Class-C power amplifier is 100%. However, there are several drawbacks for this PA. Firstly, it's highly non-linearity, and secondly, as the conduction angle approaches to zero, the output power delivered to the load approaches to zero as well. Therefore, the Class-C power amplifier is only suitable for the system with low power gain and linearization techniques are required.

2.3.2 Switching-mode PA

In contrast to linear power amplifier, where operation in the saturation region, the

switching-mode power amplifier is operated in the triode region in order to optimal efficiency and output power. It is driven with a large amplitude input signal and the transistor acts as a switch. During the ON-stage, the transistor can be modeled as a small on-resistance and the voltage across it is zero and during the OFF-stage, the transistor is cut off and the current is zero. In these amplifiers, the efficiency increases by reducing the power dissipation. And we can achieve this by eliminating the drain voltage and current overlapping time. Ideally, the switching-mode power amplifier can achieve maximum 100% efficiency at the expense of linearity performance.

2.3.2.1 Class-D PA

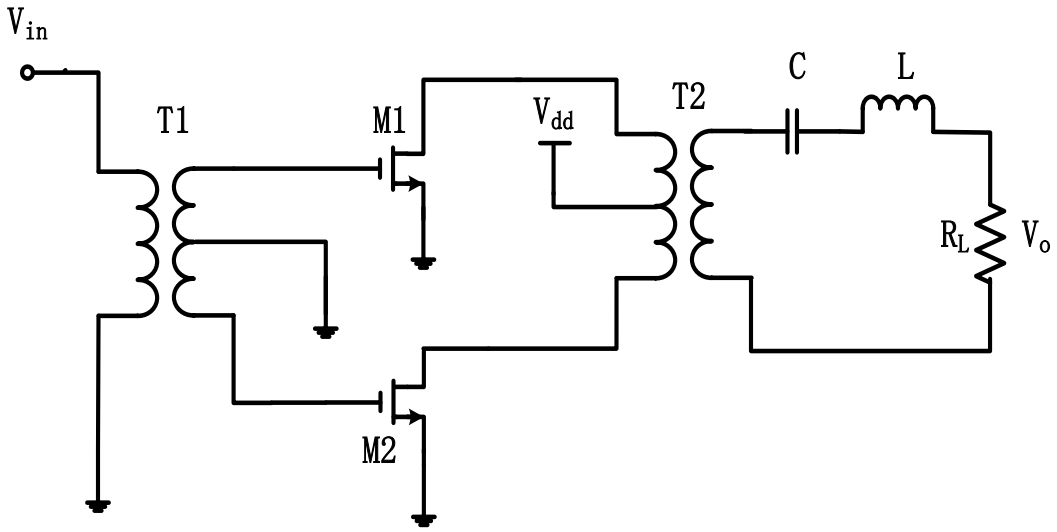

Fig. 2. 7 The basic configuration of Class-D power amplifier

The transformer coupled Class-D PA is shown in Fig. 2.12. The input transformer M_1 is used to convert the input signal to differential signal. The transistor M_1 and M_2 are driven by this differential input signal and turn on with no simultaneity. The series LC tank is tuned to the operation frequency and it is used to remove the harmonic components, so only fundamental signal can be delivered to the load. The waveform of voltage and current is shown in Fig. 2.13.

Class-D PAs have some disadvantages. First of all, two transistors and transformers are needed to implement and this introduces additional power losses. Secondly, in

high power and high frequency amplifiers, the devices are typically large in size, it could result in a large output capacitance which cannot be ignored in practical design. Furthermore, we assume that the transistors can be toggled between ON and OFF stage instantaneously, unfortunately, it is hard to realize in practice.

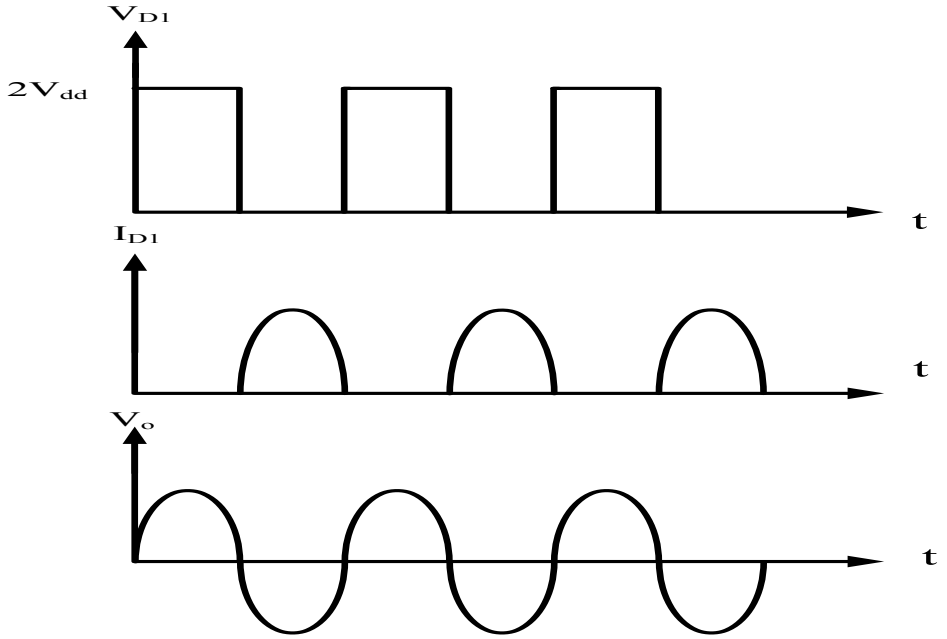

Fig 2. 8 Voltage and current waveforms of an ideal class-D power amplifier

2.3.2.2 Class-E Power Amplifier

The basic configuration of Class-E power amplifier is shown in Fig 2.14.

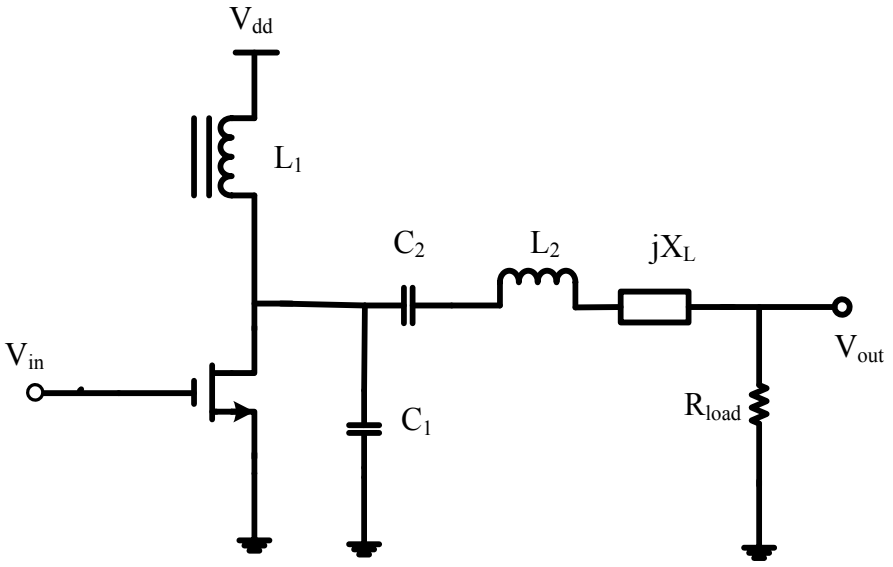

Figure 2. 9 The basic configuration of Class-E power amplifier

The transistor which is controlled by the input signal acts as an ON/OFF switch. The inductor L_1 prevent the AC signal flowing into the supply and provide the DC current as well. L_2 and C_2 are designed to be a series LC resonator to filter out the harmonics; The capacitance C_1 consists of two parts, and the parasitic capacitance of the transistor C_{ds} is also taken into account. This means the power amplifier can tolerate much larger parasitic capacitance, so the transistor with larger size can be used to optimize the overall efficiency.

During the time when the switch is OFF, the current flowing into the transistor is zero; when the switch is On, the voltage across the transistor is zero.

The waveform of class-E PA is shown in Fig. 2.15. It is seen that when the switch is ON, the voltage across the transistor has already fallen to zero, and there is no overlapping between the voltage and the current during operation. Class-E amplifier can achieve maximum 100% efficiency. However, class-E PA has main drawback in terms of peak voltage. The peak drain voltage is approximately $3.6V_{dd}$, this limited its application, especially in high frequency system.

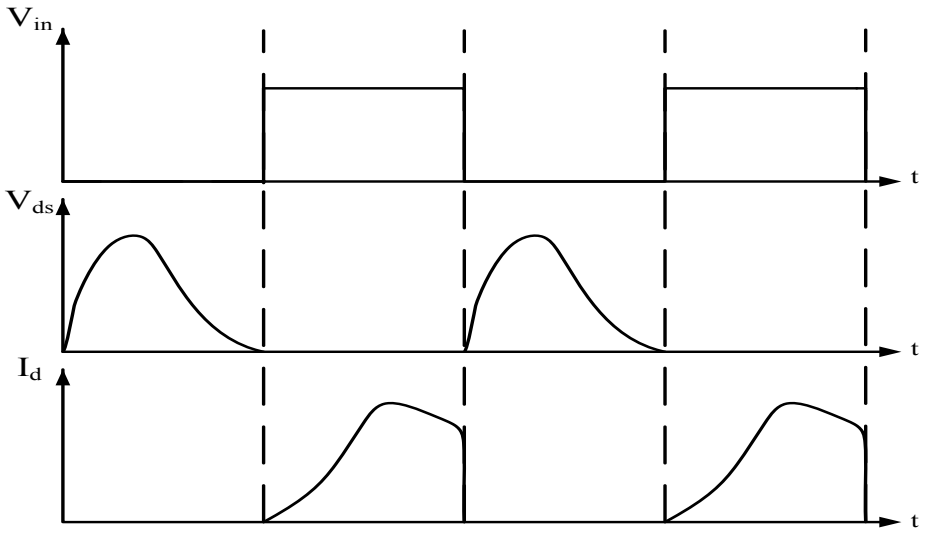

Fig. 2. 15 voltage and current waveforms of an ideal class-E power amplifier

2.3.2.2 Class-F Power Amplifier

The configuration of Class-F power amplifier is shown in Fig 2.16. This circuits consists of a quarter-wave transmission line and a harmonic resonator. At the center frequency, the resonator circuit can be seen open for fundamental frequency but short for the other frequency and the impedance at the fundamental frequency is R_{load}. At even harmonics, the quarter-wave transmission line leaves the circuit as a short circuits and at odd harmonics, the short circuit is transformed into an open circuit.

The voltage and current waveforms of class-F power amplifier is shown in Fig.2.16. It is capable of high efficiency and it can achieve maximum 100% efficiency, which means the voltage and current waveforms do not exist simultaneously, as shown in Fig.2.17. However, it is difficult to design the Class-F amplifier due to the complex output-matching network.

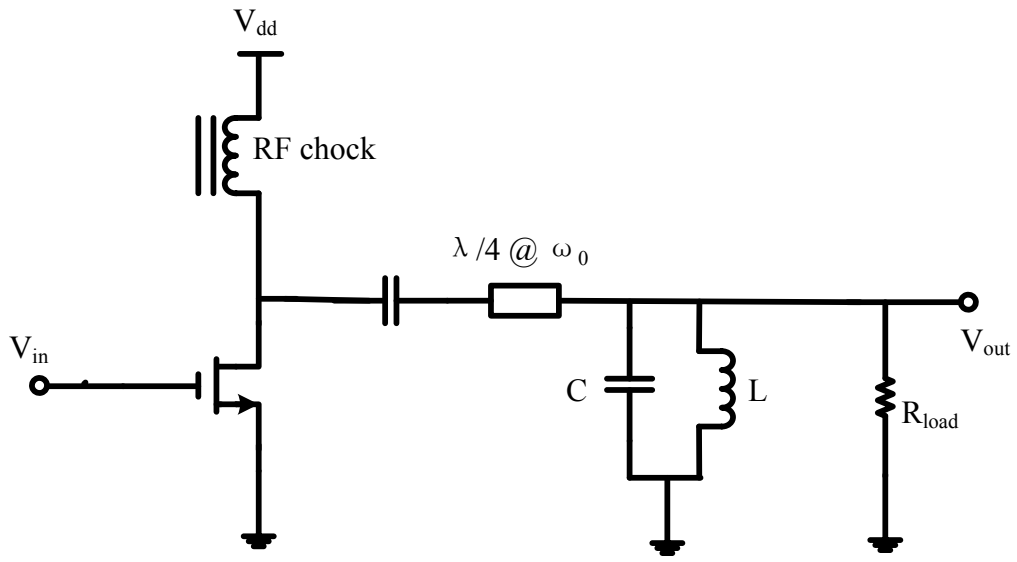

Fig. 2. 10 The basic configuration of Class-F power amplifier

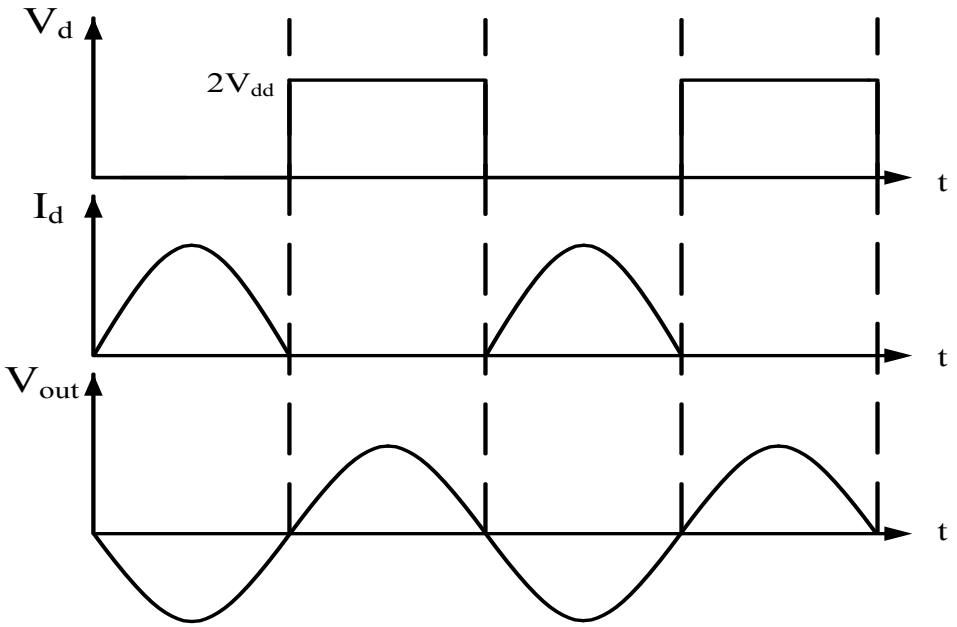

Fig. 2. 11 voltage and current waveforms of an ideal class-F power amplifier

2.3.3 Summary

The performance comparison in terms of output power, gain, efficiency and linearity for the different classes of power amplifiers is given in Table 2.1. As mentioned before, linearity and efficiency are the opposite requirements in power amplifier design. The efficiency of linear amplifiers decreases from Class-A to Class C power amplifier, however, when moving from Class-A to Class-C power amplifier, the power gain decreases and the amplifier trends to the higher nonlinearity. When design the power amplifier, the linearity and efficiency should be trade-off between the linear amplifiers and switching-mode amplifiers. While Class-A amplifiers are the most linear power amplifier, which can achieve a maximum efficiency of 50%. Switching-mode amplifier can achieve an ideal efficiency of 100%, but it is strongly non-linear. We can start from the Class-A or Class-AB amplifier and try to find a way to improve the efficiency, we can also choose the switching-mode configuration as the starting point in order to obtain high efficiency, and then use some linearization technology to improve the linearity[10].

Table 2. 1 Performances comparison for different classes of PAs

Class	Mode	Conduction Angle	Output Power	Ideal Efficiency	Gain	Linearity
A	Current Source	2π	Moderate	50%	Large	Excellent
AB		π～2π	Moderate	50～78.5%	Moderate	Good
B		π	Moderate	78.5%	Moderate	Moderate
C		0～π	Small	78.5～100%	Small	Poor
D	Switch	π	Large	100%	Small	Poor
E		π	Large	100%	Small	Poor
F		π	Large	100%	Small	Poor

2.4 Linearization of RF power amplifier

The nonlinear behavior of the RF front-end, especially RF transmitters, can significantly degrade the overall performance of the wireless systems. The power efficiency of an RF amplifier is optimal when it is operated near saturation. An amplifier operating in this nonlinear range generates IM distortion that interferes with neighboring channels. Therefore, there should be compensation for the nonlinearities and distortions of the RF transmitter.

Linearization is a systematic approach to reduce an amplifier's distortion which is inevitable for enhancing the linearity of an amplifier to the high input power drive levels and achieving linearity requirements when operating the device over its entire power range. Linearization allows a PA to generate more power and operate with higher efficiency for a given level of distortion[11][12] [13].

2.4.1 Power backoff

Power backoff is the simplest and most common linearization technique. It does not make any changes to the circuit configuration, just shrink the input voltage.

Its main principle can be illustrated by using Taylor series:

$$I_{out} = I_0 + a_1 V_{in} + a_2 {V_{in}}^2 + a_3 {V_{in}}^3 + \dots$$

Where I_{out} is the output current, V_{in} is the input voltage and I_0 is the bias output

current which can be easily blocked. As can be seen that, As the amplitude of input signal decreases, the fundamental part $a_1 V_{in}$ becomes dominant term and the higher order terms is no longer important as before. And 1dB reduction of the output power results in 3dB reduction in IM3 and 2dB linearity improvement respectively.

However, this approach also has its drawbacks, Firstly, the system can achieve high linearity performance at the price of the efficiency. Secondly, it cannot improve the linearity performance any more beyond a certain range. Hence, for some high linearity requirements circuit design, this technique is not sufficient, other linearization techniques has to be employed.

2.4.2 Feedforward

The idea of the feedforward method is to extract and remove the distortion at the output. Fig.2.18 shows the block diagram of the feedforward linearization method. The system consists of main amplifier, auxiliary amplifier, attenuator, couplers, combiner, and delay lines. The couplers is used to split the input signal into two paths, the delay lines is used for phase-matching and better signal performance can be achieved. The auxiliary amplifier is used to amplify the error signal.

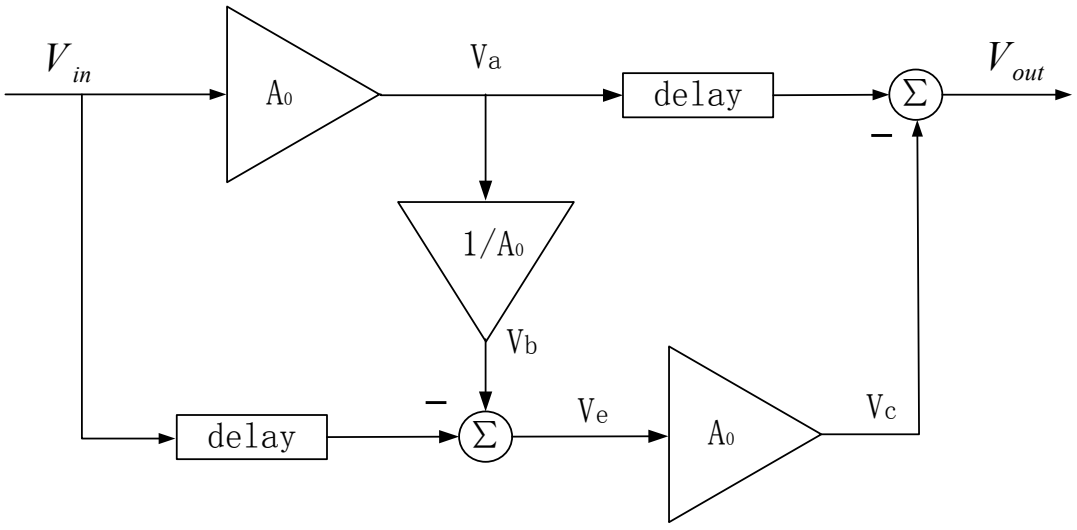

Fig. 2. 12 The basic block diagram of the feedforward linearization

Assuming that the nonlinear distortion signal can be seen as the sum of linear signal

and error signal.

$$V_a = A_0 V_{in} + V_d$$

The voltage of node b can be express as:

$$V_b = \frac{V_a}{A_0} = V_{in} + \frac{V_d}{A_0}$$

This error voltage can be get by using the comparator:

$$V_e = V_b - V_{in} = V_{in} + \frac{V_d}{A_0} - V_{in} = \frac{V_d}{A_0}$$

Error voltage is amplified by the auxiliary amplifier:

$$V_c = A_0 V_e = A_0 \frac{V_d}{A_0} = V_d$$

Then the amplified signal by main amplifier is combined with amplified error voltage in opposite phase.

$$V_{out} = V_a - V_c = A_0 V_{in} + V_d - V_d = A_0 V_{in}$$

As we can see, the distortion is cancelled out theoretically. And this method is inherently stable However, it is depend on accurate amplitude and phase matching, and susceptible to drift and aging. Due to the losses of delay line, couplers and auxiliary amplifier, the system is low power efficiency.

2.4.3 Feedback linearization

The block diagram of feedback linearization method is shown in Fig.2.19.

This method is based on the feedback loop, which is widely used in control theory. The output signal is fed back via feedback loop and subtracted from the input signal. If the gain is high enough, the local feedback can be used for linearization. However, in RF communication system, the gain is hard-earned, this method suffers the drawback of gain loss. Furthermore, the delay associated with the feedback loop will make the system unstable and limit its use to narrowband signals[14][15].

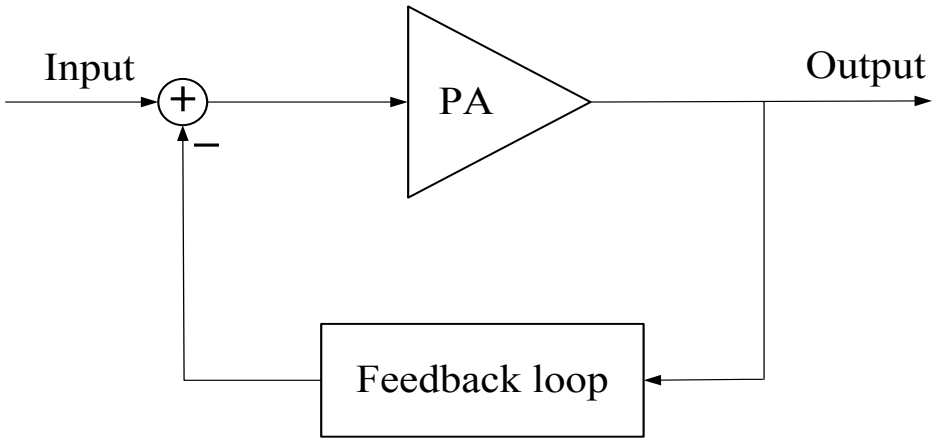

Fig. 2. 19 The basic block diagram of the feedback linearization

2.4.4 Predistortion

The block diagram of predistortion technique is shown in Fig.2.20.

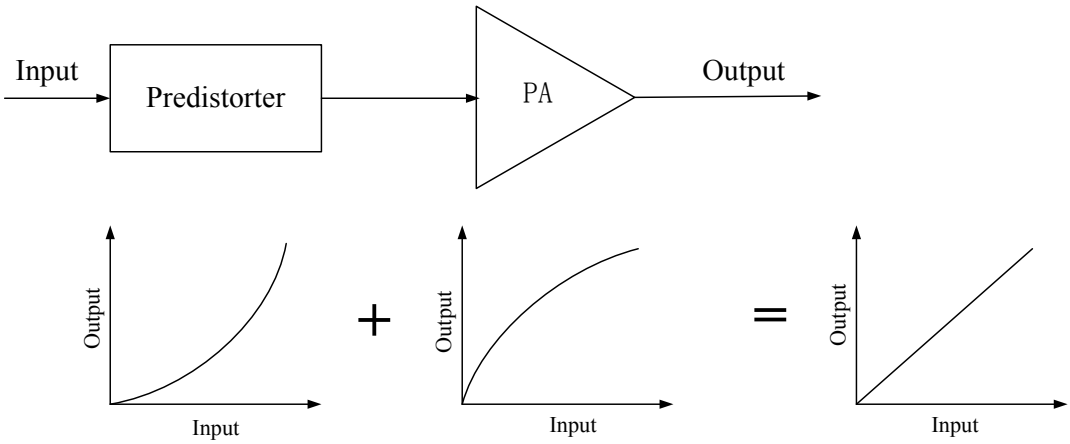

Fig. 2.20 The diagram of predistortion technique

As we known, at high power level, the power amplifier has gain compression which leads to signal distortion. In order to address this issue, a predistorter which has a transfer characteristic inverse to that of amplifier is introduced to the system. The nonlinear gain compression of the power amplifier is compensated by this predistorter and the 1 dB compression point is extended. The RF predistortion technique is widely used in academia community since it has a simple structure and does not suffer a bandwidth limitation[16].

Chapter 3

Power Amplifier Design

3.1 Power Amplifier specifications

Supply Voltage: 1.2V

Frequency: 60 GHz

Power gain: 20 dB

Output power at 1 dB compression: > 11 dBm

Saturated output power: > 15 dBm

Power added efficiency: > 10%

Input and output impedance: 50Ω

3.2 Injection locked power amplifier technique

In order to reduce the input driving requirement and improve the efficiency, the injection locked amplifier is investigated which is well-suited for power amplifier design.

Injection locked technique means the condition in which another self-oscillating circuit is forced to run at the same frequency as the input signal. A general model for the injection locked power amplifier is given in Fig.3.1. This positive feedback loop consists of a nonlinear gain block $g(v_i,v_o)$ and linear filter $H(j\omega)$, where the nonlinear block $g(v_i,v_o)$ is formed by the cross-coupled devices and $H(j\omega)$ is implemented by the matching and load network[17][18].

Without the external current flowing through the PA core, the PA core would self oscillate at a natural oscillating frequency ω_0 if the circuits satisfies the Barkhausen criterion: The loop gain should be greater than unity and the total phase shift around the loop has to be multiple of 2π[19].

$$|f|\cdot|H(j\omega_0)|\geq 1 \tag{3. 1}$$

$$\angle f+\angle H(j\omega)=2k\pi \tag{3. 2}$$

Where k is an integer. When the signal v_i with the frequency ω_i injects into the circuit, the output of f has a phase shift with the respect to the input signal, to compensate this extra phase shift, the $H(j\omega)$ must change its phase to ensure the total phase along the loop keep 2kπ, which also makes the oscillator to track the injected frequency ω_i.

Suppose that $v_i=V_{dc}+V_I\cos(\omega_i t)$ and $v_o=V_O\cos(\omega_o t+\varphi)$, where V_{dc} is the DC point. By using the Taylor series expansion of v_i around DC point $V_{dc.}$ f can be written as:

$$f(v_i,v_o)=\sum_{m-0}^{\infty}A_m\cos(m\omega_0 t+m\varphi)+\frac{1}{2}\cdot\frac{\partial A_m}{\partial v_i}\Big|_{vi=V_{dc}}\cdot\sum_{m=0}^{\infty}V_I\cos[(m\omega_o\pm\omega_i)t+m\varphi] \tag{3. 3}$$

Where the coefficient Am is the function of am and V_O. And the first part is the expression for the free-running oscillator, the second term shows the mixer products due to the presence of the injected signal.

If the first term is much smaller than the second term, g is almost in proportion to the magnitude of the injected signal V_I, so the magnitude of the output signal V_0 can be written as [20]:

$$V_0\approx|g|\cdot|\mathrm{H}|=\frac{V_I}{2}\sum_{m=0}^{\infty}|B_m|\cdot|\mathrm{H}(j\omega_0)|$$

It is obvious that the output power can be increased by the input power.

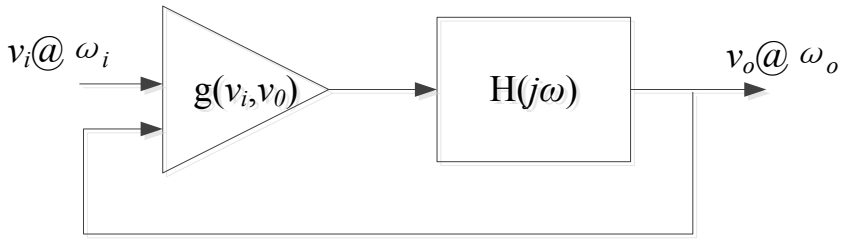

Fig. 3.1 Model of the proposed injection locked power amplifier

The Adler's equation can be used to establish the lock-in range [21]:

$$\frac{d\theta}{dt} = \omega_0 - \omega_1 - \frac{\omega_0 I_{INj}}{2QI_T}\sin\theta \qquad (3.\ 4)$$

Where I_{INj} is the peak current of the injected signal, I_T is the peak current through the negative resistance and θ is the phase difference between V_0 and V_{INJ}. At steady state, $d\theta/dt = 0$ and $|\sin\theta| \le 1$, the lock-in range is:

$$\omega_L = \omega_0 - \omega_1 = \frac{\omega_0 I_{INJ}}{2QI_T} \qquad (3.\ 5)$$

This equation implies that the injection locking only occur within a finite frequency range around the natural oscillation frequency and the locking range is positively correlated with the injection current. Hence, to expand the locking range, we can increase the size of the injection devices and decrease the cross-coupling pairs in design.

3.3 Circuit design

The power amplifier based on injection-locked structure will redound to improve gain and efficiency by means of reducing the input driving requirement. The schematic of the implemented PA is shown in Fig.3.2.

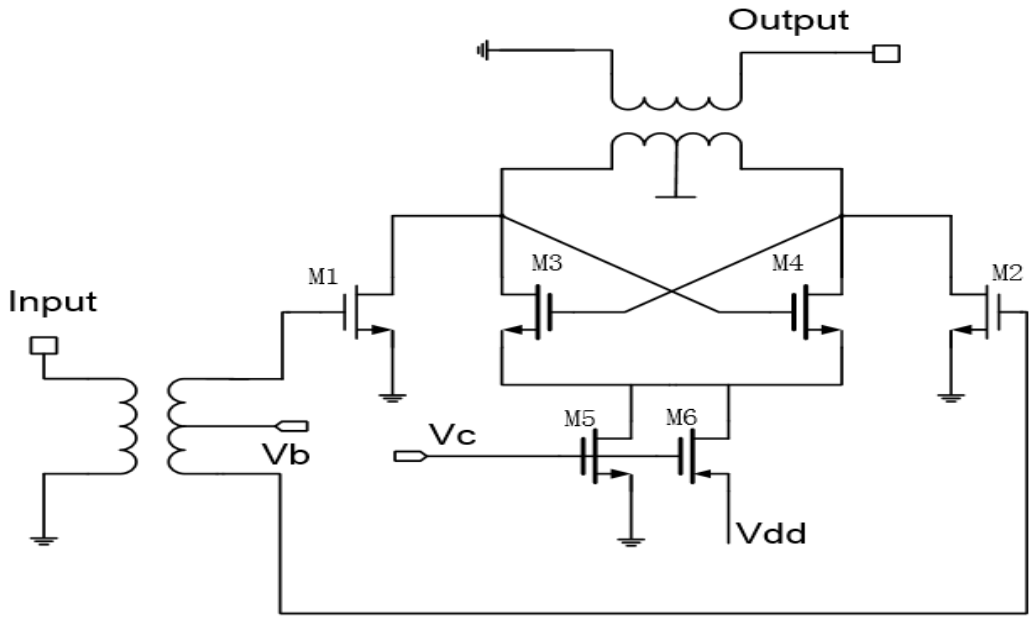

Fig. 3.2 The schematic of injection locked power amplifier

This PA core circuit consists of a NMOS cross-coupling pair together with NMOS transistors used for signal current injection. Among which M_1 and M_2 are driving transistors. M_3 and M_4 are the key devices, this cross-coupling pairs turn the circuits into an injection locked oscillator. An NMOS current source is used to control the free running output voltage swing of the PA core. The circuit is free running until the injected current is large enough to lock the output signal to the input signal.

To avoid self-oscillation, two conditions should be guaranteed. Firstly, we need to ensure that when the PA is powered up, the input power will always be available and large enough to make the output signal follow the input signal. Besides, a power-down mechanism is introduced to avoid free oscillation when PA is not driven. During power down, M_5 is turned off and M_6 will pull the local ground node to $V_{dd.}$, and the entire amplifier will be shut down[22][23].

Fig.3.3 plots the power gain versus different transistor size with a fixed bias voltage. In the left figure, the width of M_3 and M_4 is set to 30μm and the width of M_1 and M_2 is set to 60μm in the right figure. It is found that the power gain increases at first, then decreases with increasing of the transistor size. This is because the transistor size determines its current. For the injection transistor M_1 and M_2, the large width results

to the larger injection current and power gain. However, due to the circuit limitation, the power gain decreases finally. As mentioned before, the locking range is positively correlated with the injection current and inversely proportional to the core current. In order to improve the bandwidth, we decrease the size of the cross-coupled pair. However, the cross-coupling pairs M_3 and M_4 provide for a negative resistance, and too small transistor is unable to satisfy the oscillatory condition. Hence, we need to make our selection according to actual situation.

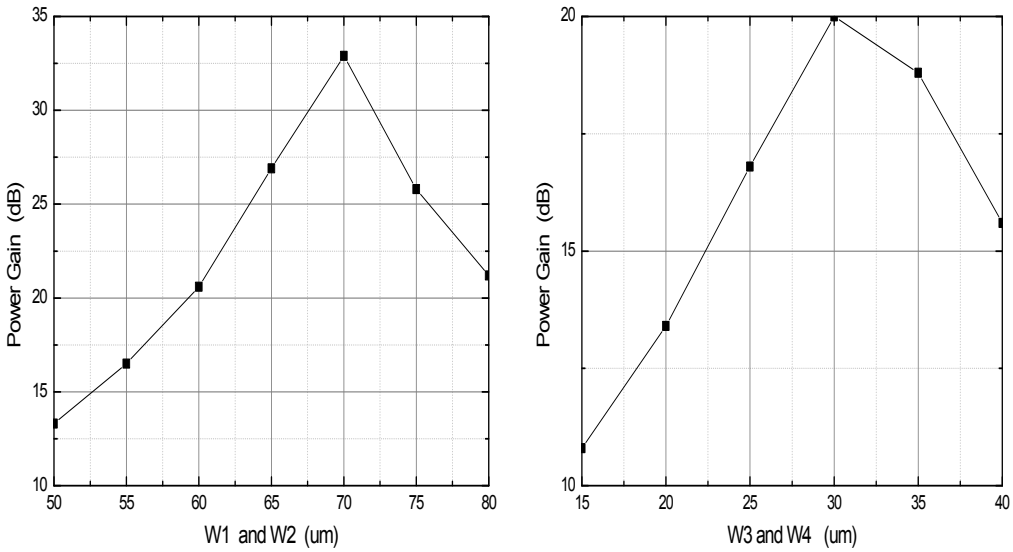

Fig. 3.3 Power gain versus different device size with $V_b = 0.3V$ and $V_c = 0.8V$

According to the simulation and optimization, the width/length of the injection driving transistors M_1,M_2 is 60μm/65nm, with the figure number of 50; the width/length of the cross-coupling pair M_3,M_4 is 30μm/65nm, with the figure number of 50; and for the current source M_5 is 120μm/65nm, with the figure number of 120.

3.4 Balun design

As a passive component, balun plays an key role in the power amplifier design. In practice, it performs the following functions: First of all, the differential structure is designed in the power amplifier core in order to reject the common-mode signal and noise, improve the output voltage swing and reduce the interference to the external circuit resulting from the power amplifier. However, the load of the power amplifier

is always single-ended, A balun is necessary to transfer between the single-ended and differential signals. Furthermore, as we known, in order to obtain the maximum output power, matching network is needed to transform the optimum load to a 50Ω load, and the balun can realize this function perfectly. Finally, balun also plays a role in isolation.

The balun is a three-port device which is used to convert the single-ended signal into differential signals. The amplitude of the output differential signals is equal and the phase is opposite, so when analyzing the balun performance, the amplitude and phase imbalance are the main figures of merit. Furthermore, the insertion loss is also a important parameter which measures the energy absorbed when the signal passing through the balun[24].

The balun is designed based on the Marchand type. The circuit diagram of Marchand balun with centre-tap is given in Fig 3.4.

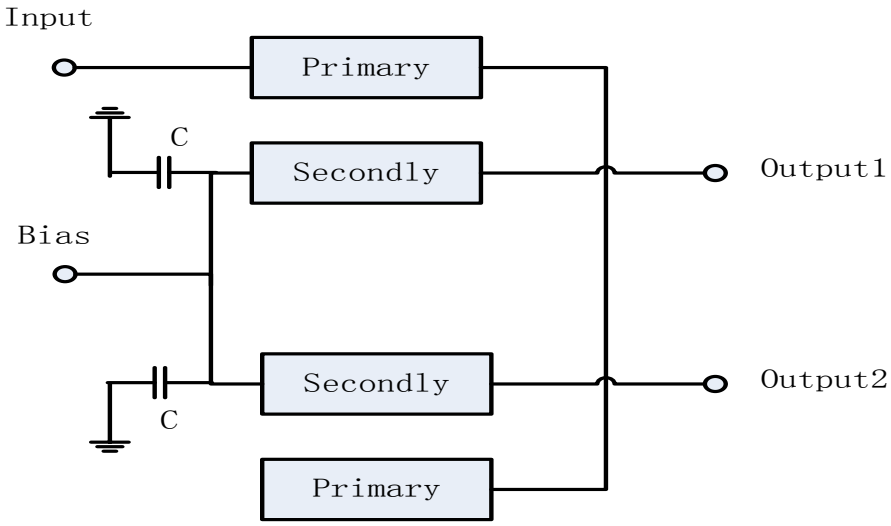

Fig 3.4 The Schematic diagram of Marchand balun

The balun consists of two symmetrical quarter-wave coupled lines, where the primary line is open-ended and the two secondary lines are connected to the two output ports respectively, and the top two metal layers M_6 and M_7 are used as broadside coupled lines. Center-tap for DC bias is added and two symmetrical capacitances are connected between the center-tap and the ground to provide an AC

path for the signal[25]. The balun is symmetric and the layout is shown in Fig.3.5.

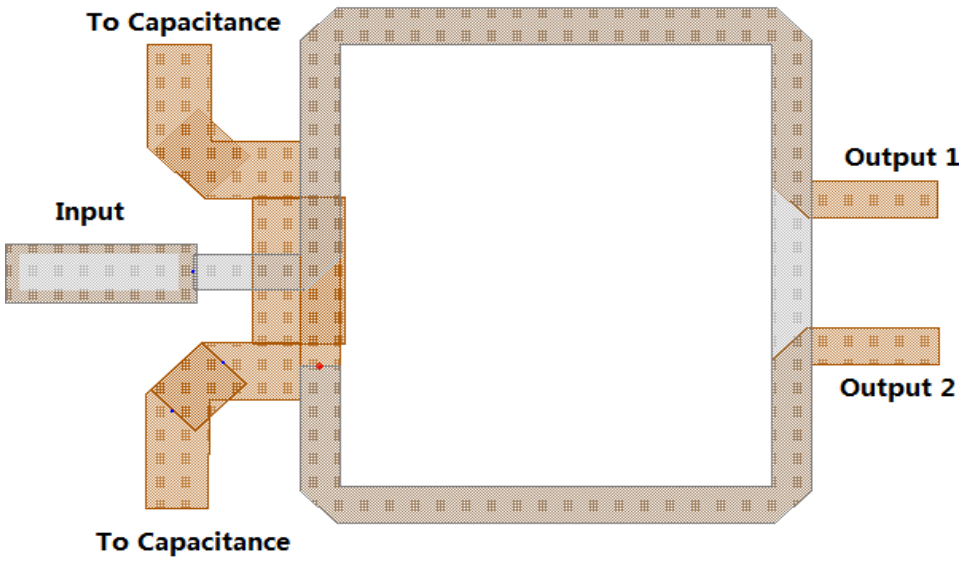

Fig.3.5 The layout of the balun

The carrier frequency of the balun is 60 GHz, and, the width and length of the coupled lines are optimized by the EM simulation in ADS, and the simulated S-parameters, insertion loss and imbalances are shown in Fig.3.6-3.8.

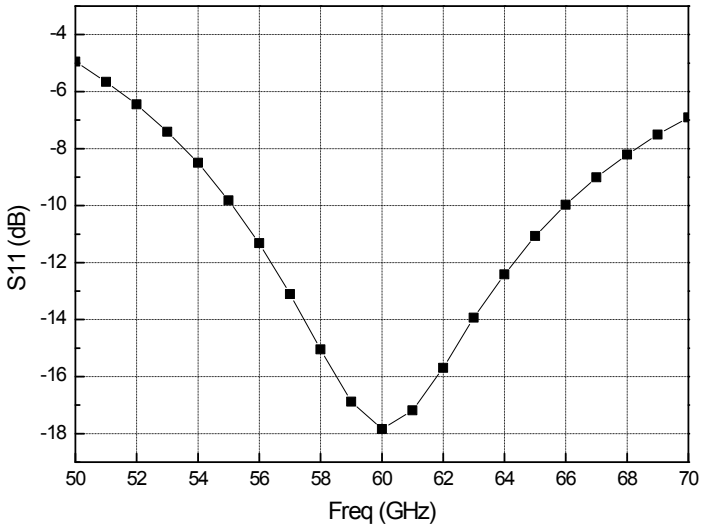

Fig.3.6 S11 for the input balun

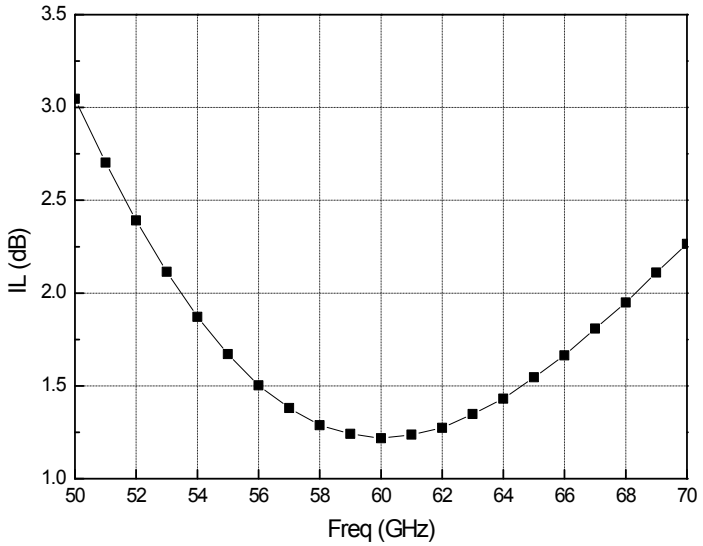

Fig.3.7 Insertion loss for the input balun

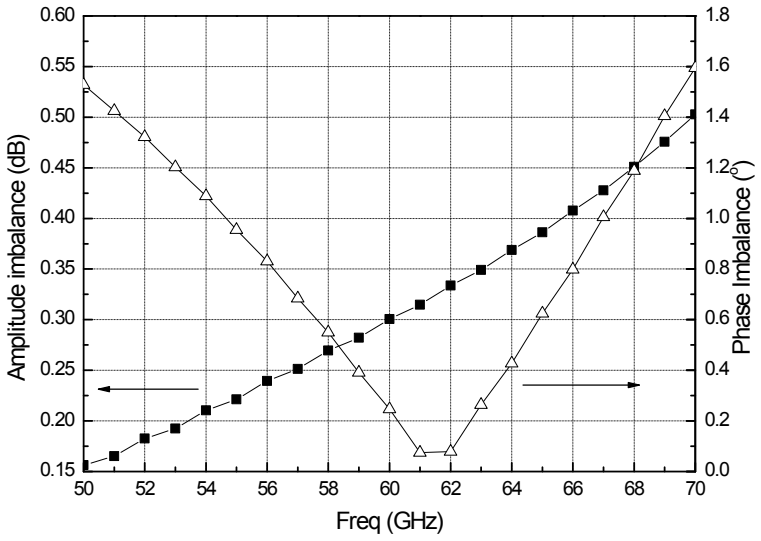

Fig.3.8 Amplitude and phase imbalance for the input balun

The input balun is matched to the input impedance of the PA core. S_{11} of the designed input balun is about -18dB at 60 GHz. The insertion loss (IL) is less than 1.5dB in the frequency ranging from 56 GHz to 64 GHz and the minimum insertion

loss is 1.21dB at 60 GHz. In this frequency band, the amplitude imbalance is 0.3 dB and the phase imbalance is less than 0.25°.

Comparing with the input balun, the output balun is matched to the output impedance of the PA core, and the width is thicker in order to flow through higher current. The simulation results of the output balun are shown in Fig.3.9-3.11. S_{11} is about -24dB at 60 GHz, the insertion loss is less than 1.5dB in the frequency ranging from 58 GHz to 62 GHz and the minimum insertion loss is 1.32dB at 60 GHz. In this frequency band, the amplitude imbalance is 0.9 dB and the phase imbalance is less than 0.7°.

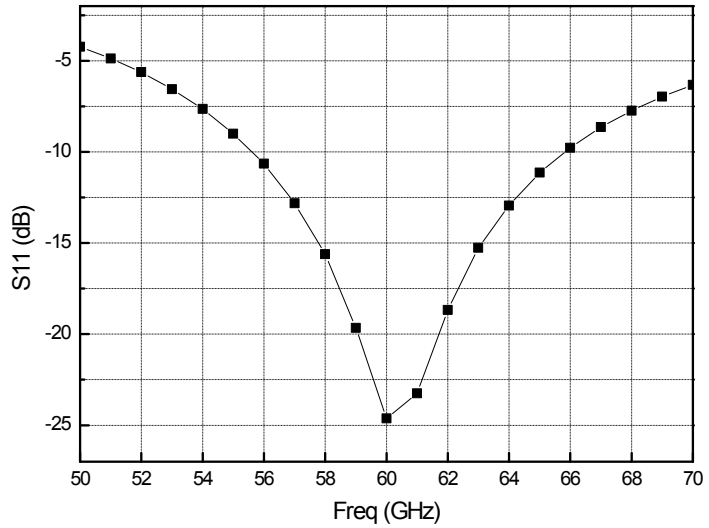

Fig.3.9 S11 for the output balun

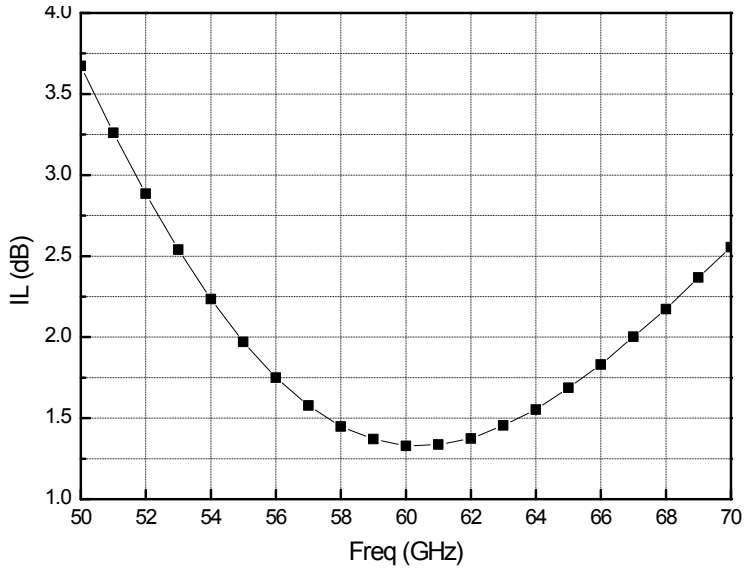

Fig.3.10 Insertion loss for the output balun

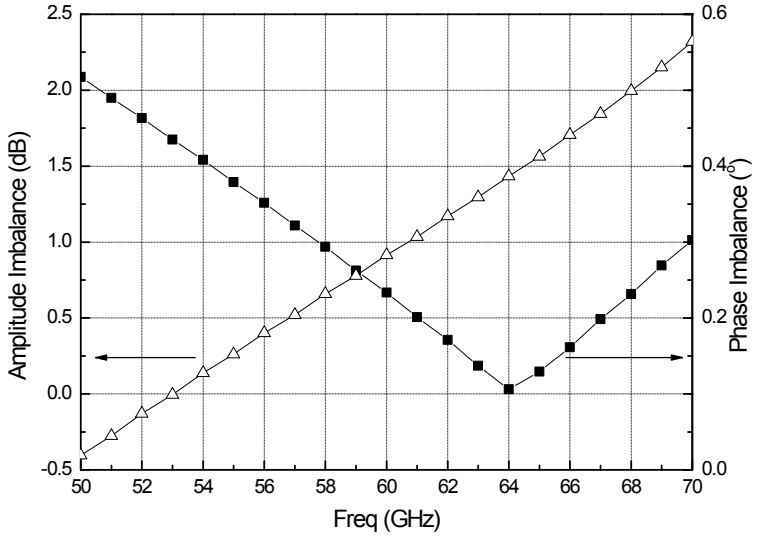

Fig.3.11 Amplitude and phase imbalance for the input balun

3.5 PA Simulation Results

The circuit is simulated by using ADS tools, and the single tone harmonic balance simulation is done to get the transducer power gain and the power efficiency. Fig.3.12 shows the transducer power gain. As expected, the gain decreases as the output power increases. At 1-dB compression point, the output power is 7.9 dBm.

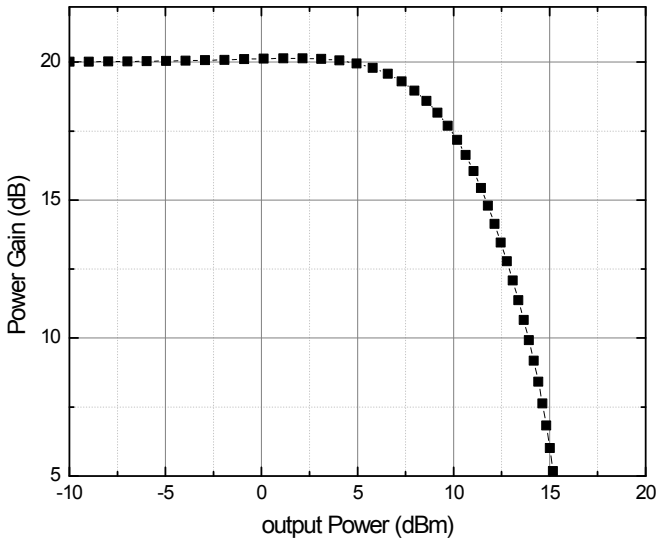

Fig.3.12 Power gain of PA

Fig 3.13 shows the power added efficiency of the amplifier. The efficiency is directly proportional with the output power. The PAE can reach its maximum value of 40% at the output power of 15dBm and at 1-dB compression point, the PAE is 6%.

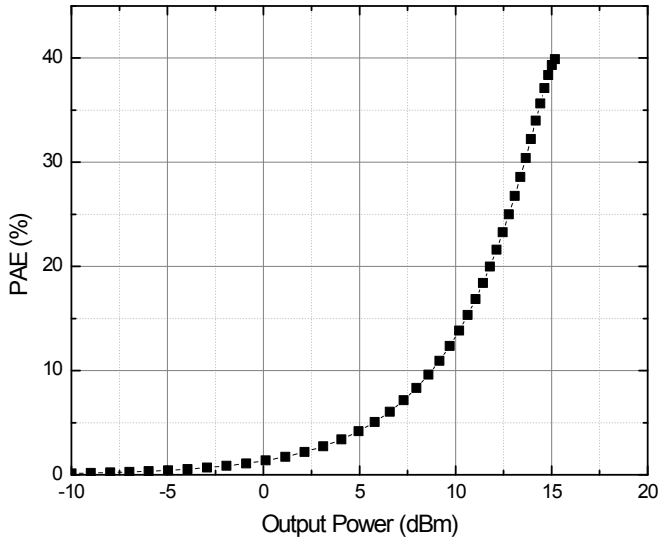

Fig.3.13 PAE of the PA

Fig.3.14 shows the power gain reduction and phase shift as the function of the input power. With the increasing of input power, the phase difference increases at first, and then decreases. When the input power increases to -11dBm, the gain difference is less than 1dB. And the phase shift increases as the input power increases. In the input power ranging from -25dBm to -10dBm, the AM-PM characteristics drops from -0.3 ° to -3.8 °.

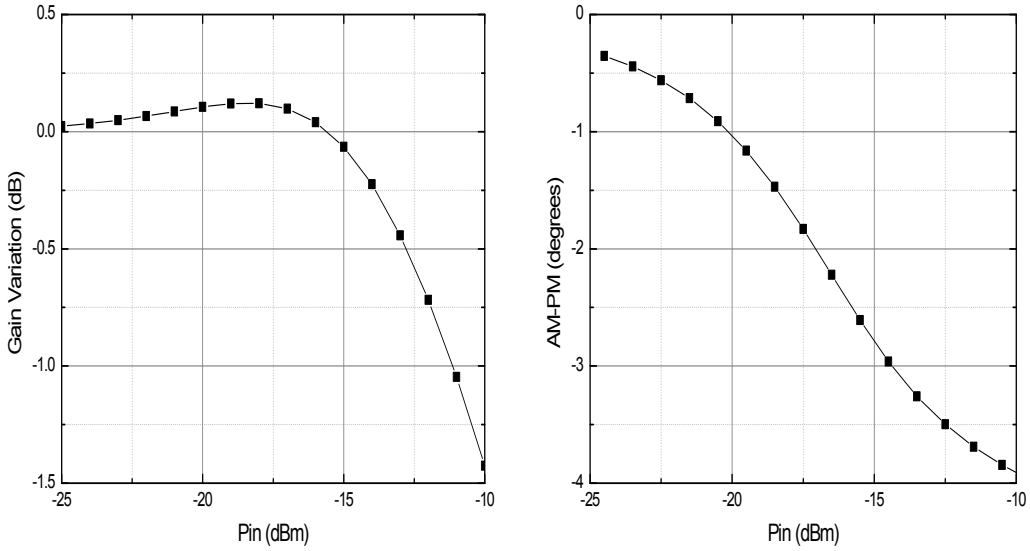

Fig. 3.13 AM to AM and AM to PM versus input power

The results show that the linearity performance of the power amplifier leaves much to be desired and cannot meet demand completely. In order to improve the available linear output power and the overall efficiency, the linearization enhancement technique is necessary. We will put emphasis on discussing the linearization of the power amplifier in next chapter.

Chapter 4

Power Amplifier Linearization

4.1 Adaptive biasing technique

To ensure the power gain is maintained in the whole amplification process, the bias is operated at a high quiescent point with the high output power. However, when the power is low, due to this high voltage bias, significant amount of power is wasted and the efficiency will be decreased greatly. Now adaptive biasing technique is proposed to solve this problem. Fig.4.1 shows the basic block diagram of this method. Actually, it is a feedback regulation. The dynamic bias control unit can track and monitor the output power in real time and then adjust the bias adaptively. The bias is lower than the normal value at low power level and it gradually increases with the increasing of the output power. As we known, after the amplifier reaches to its 1-dB gain compression point, the gain will be degraded. Fortunately, the increased adaptive bias will boost the power gain in order to compensate the gain reduction. In this way, the linear operation region extends and both the linearity and efficiency is improved at the same time[26][27][28].

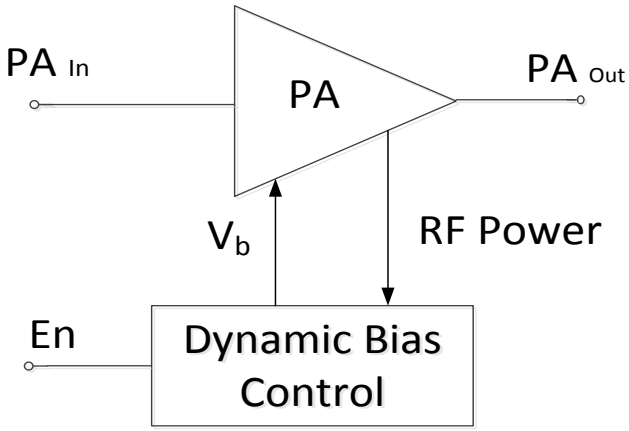

Fig.4.1 The basic block diagram of adaptive biasing technique

The schematic of the dynamic bias control part is shown in Fig.4.2.

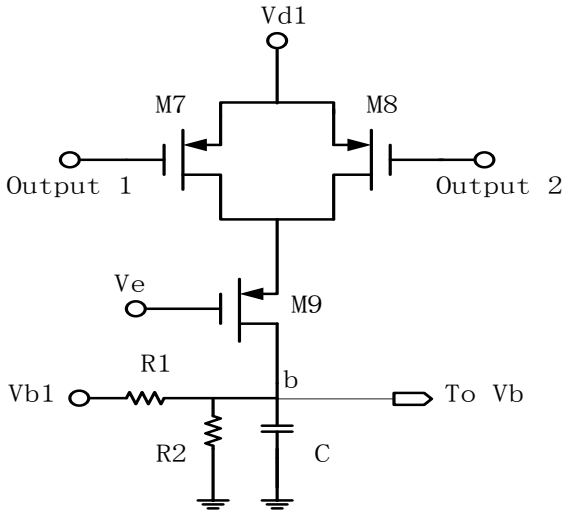

Figure 4.2 Schematic of the dynamic bias control part

Where, V_b is the bias of the injection transistor. Two low-threshold PMOS transistors M_7 and M_8 are connected to the differential output in order to sense the output level. These two transistors with small size and little current consuming have little influence on PA's performance. These transistors will turn off when the output power is low. At this time, the feedback voltage can be expressed as the following equation:

$$V_b = \frac{R_2}{R_1 + R_2} V_{b1} \tag{4. 1}$$

It is obvious that the starting point of the feedback voltage V_b is determined by the voltage V_{b1} and the resistor network. As the output voltage swing becoming larger than the threshold voltage, the feedback loop turns on and the feedback voltage can be calculated by using the following equations:

$$V_b = \frac{R_2}{R_1 + R_2} V_{b1} + i_b \cdot Z_b \tag{4. 2}$$

$$i_b = i_p + \frac{V_{b1} - V_b}{R_1} \tag{4. 3}$$

$$Z_b = (R_1 // R_2) // (\frac{1}{j\omega C_b}) \tag{4. 4}$$

Where i_b and Z_b represent the total current and impedance at the node b. It is apparent that the feedback voltage V_b increases with the increasing power level. And the same method is applied to V_c, which is the bias voltage of the current source.

Fig.4.3 shows the power gain versus different bias voltage. As we have seen, the power gain is proportional to the bias voltage.

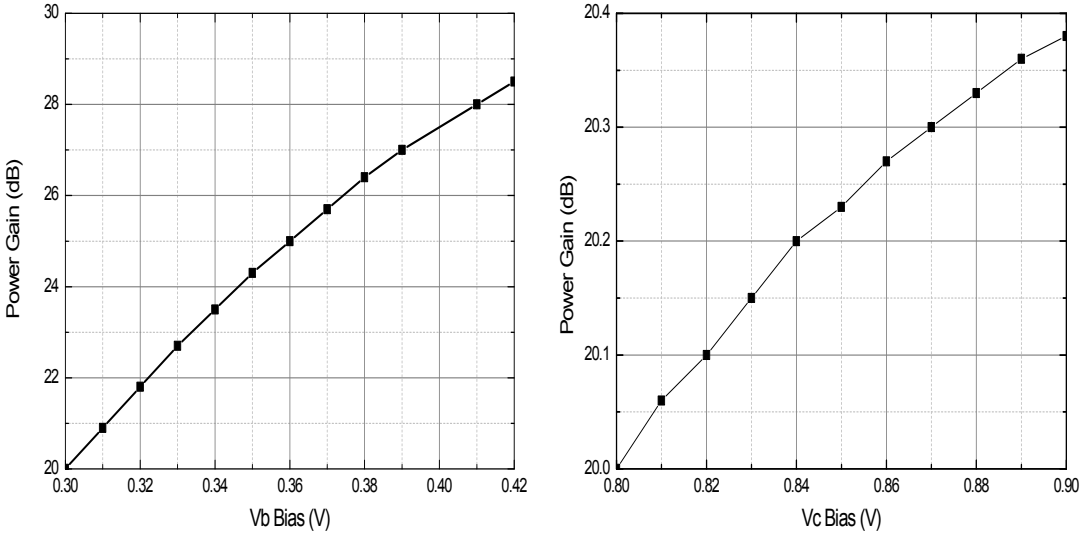

Fig.4.3 Power gain versus different bias voltage

Fig.4.4 plots the bias voltage versus different input power. When the power is low, the feedback loop doesn't work and the bias voltage maintain its original value. When the input power is more than -20dBm, the bias voltage V_b and V_c increase rapidly. As mentioned before, the power gain is proportional to the bias voltage. Hence, the power gain will increase greatly at the high power level by adjusting the bias voltage and this increased power gain can compensate for the gain reduction in order to extent the linear region.

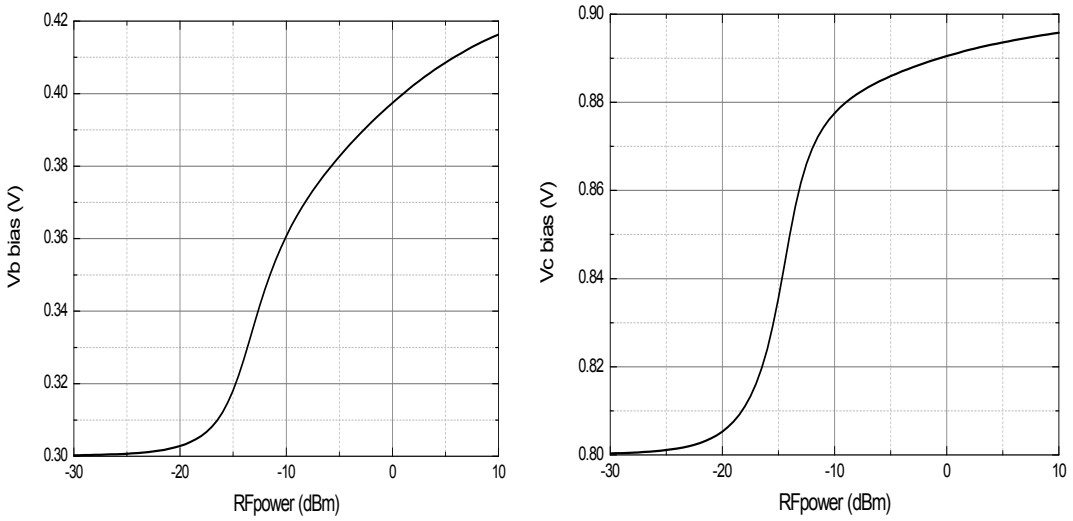

Fig.4.4 Bias voltage versus different input power

Fig.4.5 shows the power gain of PA with and without the adaptive biasing operated at 1.2V supply. When the output power is low, the power gain is the same as before because the transistors M_7 and M_8 are closed and the feedback loop doesn't work. As the power increases, because of the increased bias voltage, the power gain is boosted obviously. It starts to compress eventually until the maximum value of 21.3 dB is experienced. However, the parasitic capacitance in the layout will mitigate this overshoot in real design. The 1dB compression point increases from 7.9 dBm to 11.5dBm, and in this region, the power gain keep steady. In another words, the linear operation region is effectively extended by 3.6 dB.

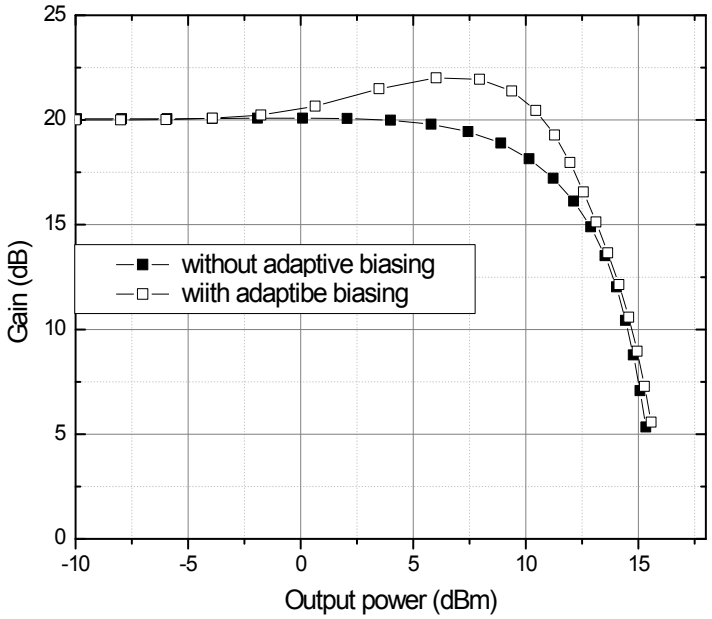

Fig.4.5 Simulated power gain with and without the adaptive biasing

Fig.4.6 compares the power added efficiency with and without the adaptive biasing. As we mentioned before, the PAE has obviously positive correlation with the power gain. Hence, the increased power gain results in the improvement of PAE. The PAE can reach its maximum value of 40 % at 15dBm of the output power and it can get the value of 17 % at 1-dB compression point. In conclusion, this technique improves not only the performance of linearity but also the efficiency.

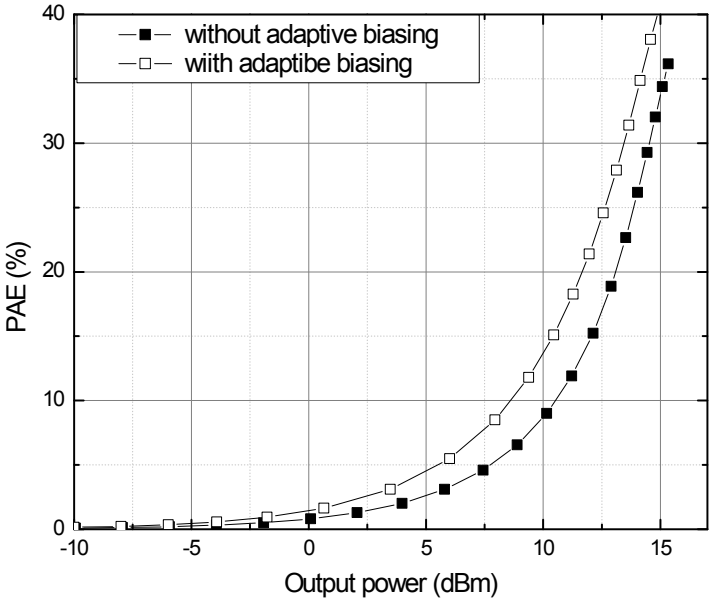

Fig.4.6 Simulated PAE with and without the adaptive biasing

Fig.4.7 plots the power gain variation and phase shift as the function of the input power. These curves represent the AM to AM and AM to PM characteristics under different conditions when the adaptive bias is on and off, respectively. In the input power ranging from -25dBm to -20dBm, the results of the original and adaptive biasing is almost the same. When the adaptive bias is on, the gain variation increases at first, then decreases with the increasing of input power and the maximum gain variation reaches to 1.25 dB. But when relatively large changes in bias levels occur, undesired phase shift occurs as well. The performance of AM to PM with adaptive biasing is worse than the original power amplifier, and the maximum phase shift reaches to -6.6 degrees.

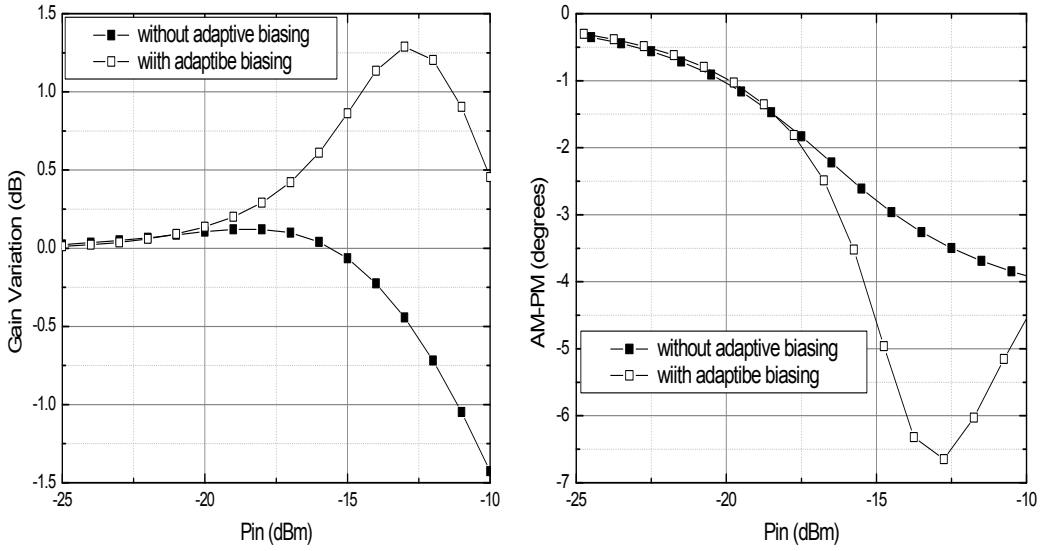

Fig. 4.7 AM to AM and AM to PM versus input power

4.2 Pre-distortion technique

As we mentioned in chapter 2, power amplifier exhibiting the gain compression at saturation region results in distortion. And a predistorter with a gain expansion characteristic is introduced to the system in order to compensate for the gain lost in compression and extend the linear output region. In this paper, a predistortion

linearizer using a shunt cold-mode structure is proposed. The schematic is shown in Fig.4.8.

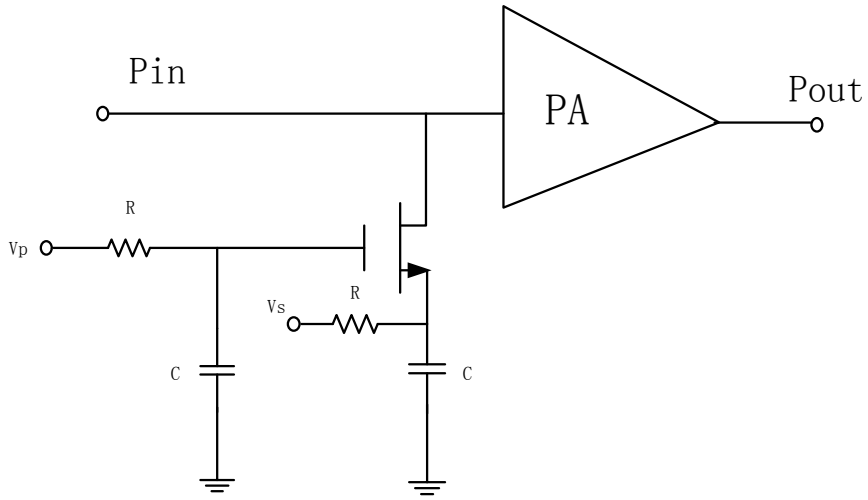

Fig.4.8 Schematic of the pre-distortion linearizer.

This circuit consists of a cold-mode operation transistor, two resistors and two bypass capacitors. It can be expressed as the combination of a capacitor (C_{off}) series with a small resistor (R_{off}) and a current source in parallel. The equivalent circuit model is shown in Fig.4.9.

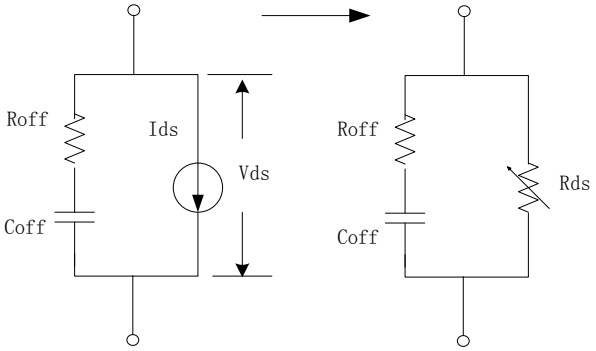

Fig. 4.9 The equivalent circuit model of predistortion linearizer

Consider that the variations of C_{off} and R_{off} are much smaller than the variation of R_{ds}. So the C_{off} and R_{off} are assumed to be constants and gain (S_{21}) can be expressed by:

$$S_{21} = \frac{2}{2 + Z_0\left(\frac{1}{R_{ds}} + \frac{1}{((\frac{1}{j\omega C_{off}}) + R_{off})}\right)} \tag{4. 5}$$

Where Z_0 is a 50Ω characteristic impedance and the drain to source resistor R_{ds} is the key element of the linearizer which can be expressed by using the equation below.

$$R_{ds} = \frac{1}{\frac{\partial I_{ds}}{\partial V_{ds}}} \tag{4. 6}$$

Where the $\partial I_{ds} / \partial V_{ds}$ indicates the slope of its DC-IV curve. As we have seen, there is negative correlation between R_{ds} and the slope of DC-IV curve. In Fig.4.10, when the input power is low, the transistor operates in the linear region and R_{ds} is constant. As the input power increases, the slop of DC-IV curve decreases especially near the pinch-off voltage which results in the increased R_{ds} [29][30][31].

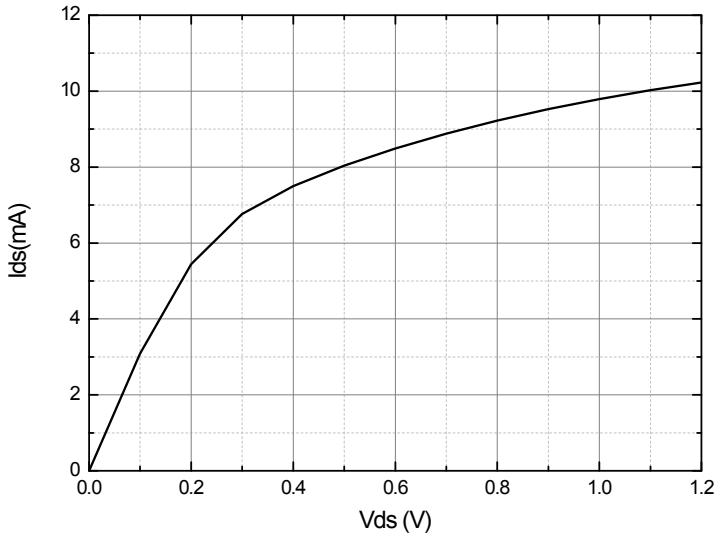

Fig.4.10 DC-IV curve of the transistor with $V_p = 1\,\mathrm{V}$ and $V_s = 0.6\,\mathrm{V}$

Fig.4.11 shows the gain expansion of the predistortion linearizer. At low input power, R_{ds} is a constant. As the input power increases, due to the gain is proportional to the R_{ds}, the increased R_{ds} will result in 1.4dB gain expansion.

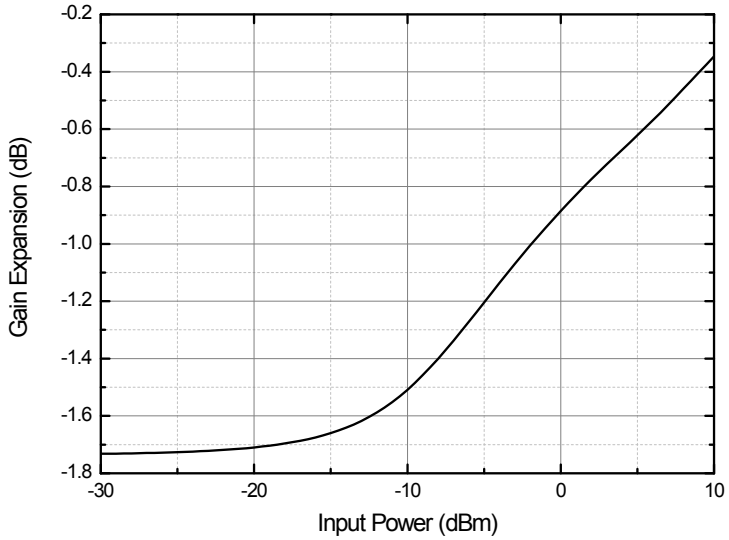

Fig. 4.11 Gain expansion of the predistortion linearizer

Fig.4.12 shows the power gain of PA with and without the predistortion linearizer. The result implies that the linearizer adopts insertion loss of 2 dB and at 1-dB compression point, the output power is 9 dBm and the linear operation region is extended by 1.1 dB. The improvement is not obvious because the original power gain has shown a sharp decline at the high output level, and the output power with predistortion linearizer is always less than the original power amplifier. Hence, its improvement of the linear region is limited to the original output power level.

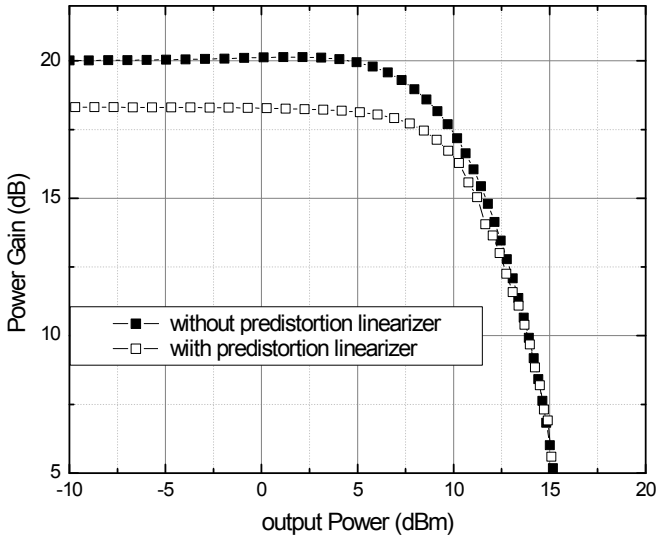

Fig.4.12 Power gain of PA with and without the predistortion linearizer

PAE versus output power has been investigated in Fig. 4.13. When the predistortion linearizer is introduced, PAE slightly decreases. But it improves PAE@OP_{1dB} from 6% to 9.5%.

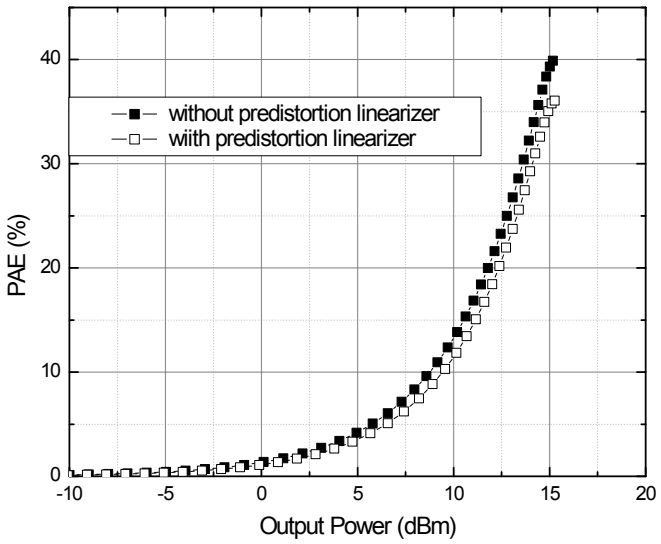

Fig.4.13 PAE of PA with and without the predistortion linearizer

Fig4.14 shows the AM-AM and AM-PM with the predistortion linearizer. Unlike the previous results, the result of the phase shift is positive value. The phase shift is within the range from 0 to 1.75 degrees.

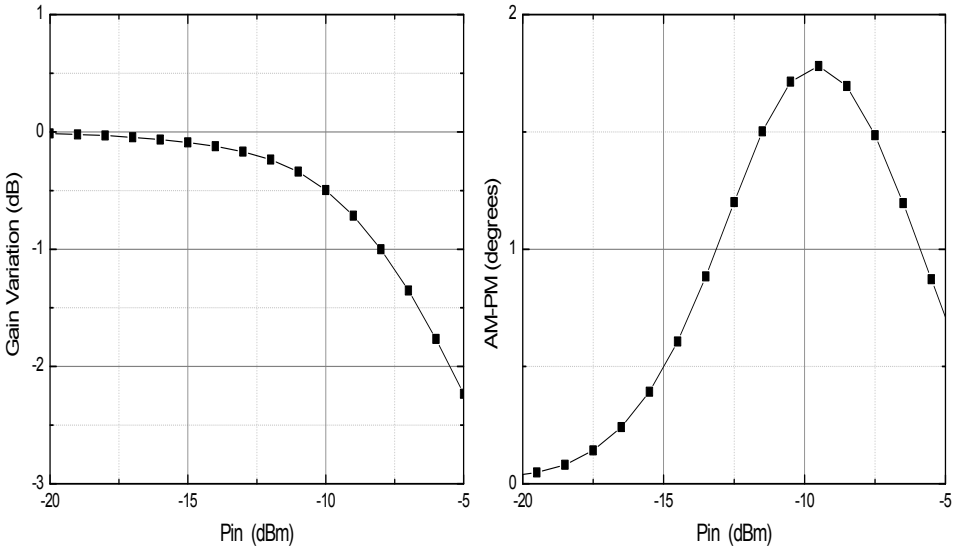

Fig.4.14 AM-AM and AM-PM with the predistortion linearizer

As we mentioned before, PA with adaptive biasing technique can extend the linear region but results in worse AM-PM performance and PA with predistortion linearizer will improve the AM-PM performance but it is limited to the low output power. Now, we combine these two techniques together to improve not only the linear region but also the AM-PM performance. Due to the insertion loss, the bias voltage is required to increase in order to maintain the gain of 20dB. Now, the gain and PAE of the power amplifier is shown in Fig.4.15. Compared with the results we got before, the power gain has delivered an obvious boost for the output power from 0dBm to 10dBm. This PA delivers a P_{1dB} of 11.5dBm, and a PAE of 13.5%.

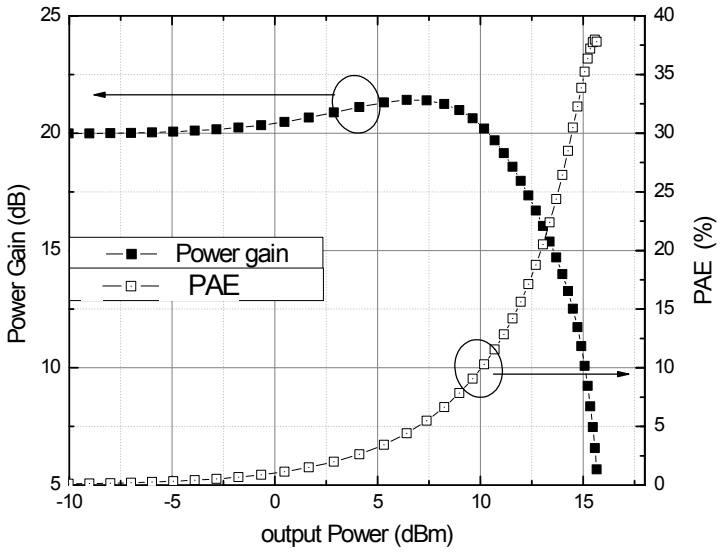

Fig.4.15 Gain and PAE of PA with adaptive biasing and predistortion technique

Fig.4.16 shows AM-AM and AM-PM performances of PA with adaptive biasing and predistortion technique. In the input power ranging from -20dBm to -15dBm, the gain variation increases from 0.5dB to 1.45dB, and then it drops with the increasing of the input power. When the input power is larger than -8.5dBm, then gain variation is less than -1dB. And AM-PM performance is improved a lot now. The phase shift is within the ranging from -1.75 to 0.5 degrees.

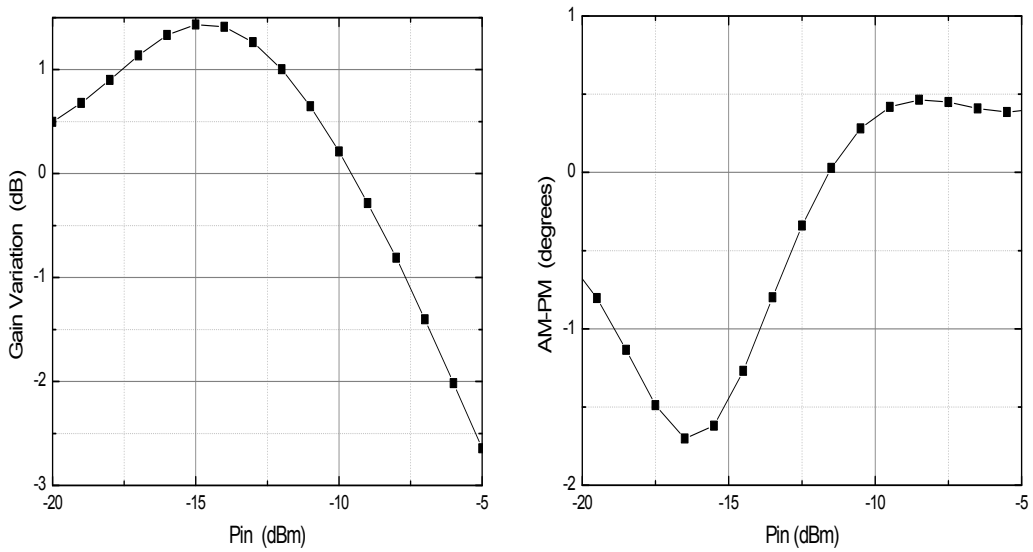

Fig. 4.16 AM-AM and AM-PM of PA with adaptive biasing and predistortion technique

4.3 Two-stage PA

In this section, two-stage power amplifier is proposed and its schematic is shown in Fig.4.17. The first stage circuit consists of a transistor, an inductor and a DC blocking capacitor is added between the input and injection-lock PA. The transistor is used as a current source, driving a controlled current into the load. The inductor provides the constant current to the transistor and DC blocking capacitor blocks the DC current flowing into the load. And the two amplifier stages are connected without any matching network. Furthermore, a voltage bias with a DC feed is added at the gate of the first stage. The results show that the power gain almost remains the same level and it is little affected by this voltage bias. However, this bias had significant effect on efficiency and linearity of the power amplifier. When this bias increases from 0.4V to 0.9V, PAE drops from 31% to 22%, but the AM-PM performance is improved obviously. As we mentioned before, efficiency and linearity have the opposite tendency, and a tradeoff must be made. In this thesis, we set voltage bias equal to 0.6V in order to achieve high linearity and high efficiency at the same time.

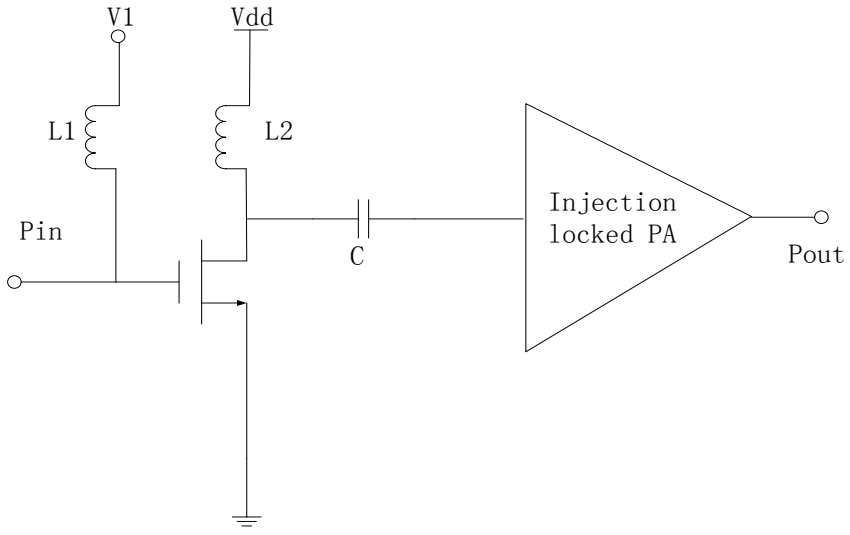

Fig. 4.17 The schematic of two-stage PA

Fig 4.18 shows the gain of the both two PA stages. As we can see, the first stage and injection-locked stage deliver a gain of 8dB and 12dB respectively. In the output

power ranging from -10dBm to 0dBm, power gain is maintained constant. With the increasing of the output power, the gain of the injection-locked stage decreases. Fortunately, the first stage delivers an expansion gain at the high power level. When the output power is 15dBm, its gain can get almost 12dBm. And the first-stage expansion gain can boost the overall power gain in order to compensate the second-stage gain reduction.

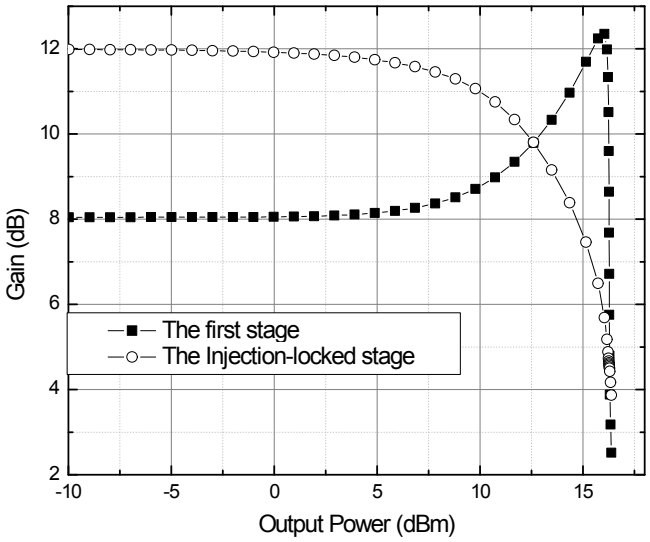

Fig.4.18 The gain of the both two PA stages

The overall power gain is shown in Fig.4.19. It is obvious that the first-stage expansion gain is matched to the gain reduction of the injection-locked stage perfectly. In the output power ranging from -10dBm to 10dBm, power gain is almost maintained constant. The results indicates that this power amplifier can deliver $P_{sat} = 16.3dBm$ and $OP_{1dB} = 15.41dBm$.

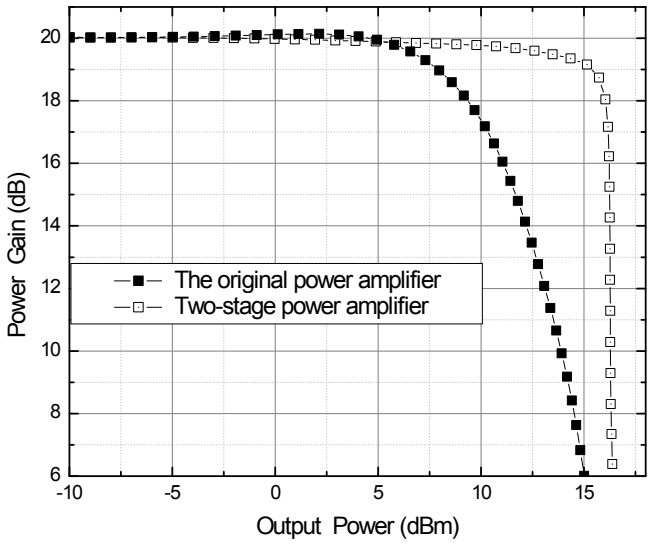

Fig.4.19 Power gain of original and two-stage power amplifier

PAE of the two-stage power amplifier is shown in Fig.4.20. The first stage is a linear PA. As we mentioned in chapter 2, it can get a good linear performance at the cost of the efficiency. So the introducing of the first stage can result in the reduction of efficiency. However, due to its linear region extended, we can get PAE from 6% to 30%.

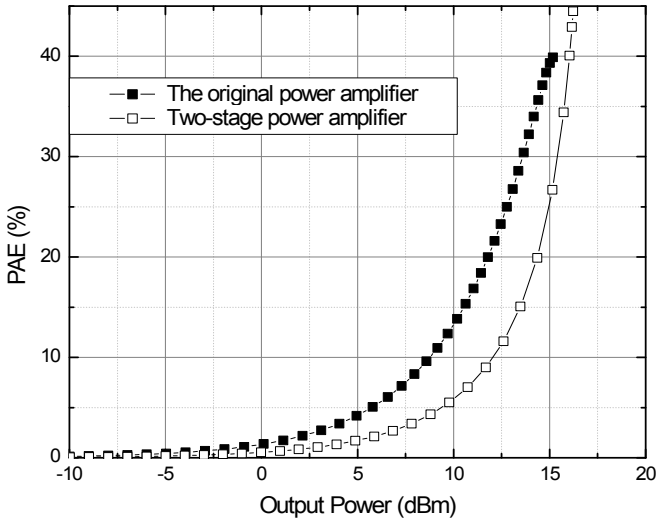

Fig. 4.20 PAE of original and two-stage power amplifier

Fig 4.21 shows the AM to AM and AM to PM characteristics versus the different input power. The AM-AM curve with two-stage is more flatten. Its gain variation is less than 1dB until the input power reaches to -3dBm. In the input power ranging from -20dBm to -10dBm, the phase shift is less than 2 degrees and its AM-PM

characteristic is better than the original PA as well. With the increasing of input power, the phase difference increases at first, and then decreases.

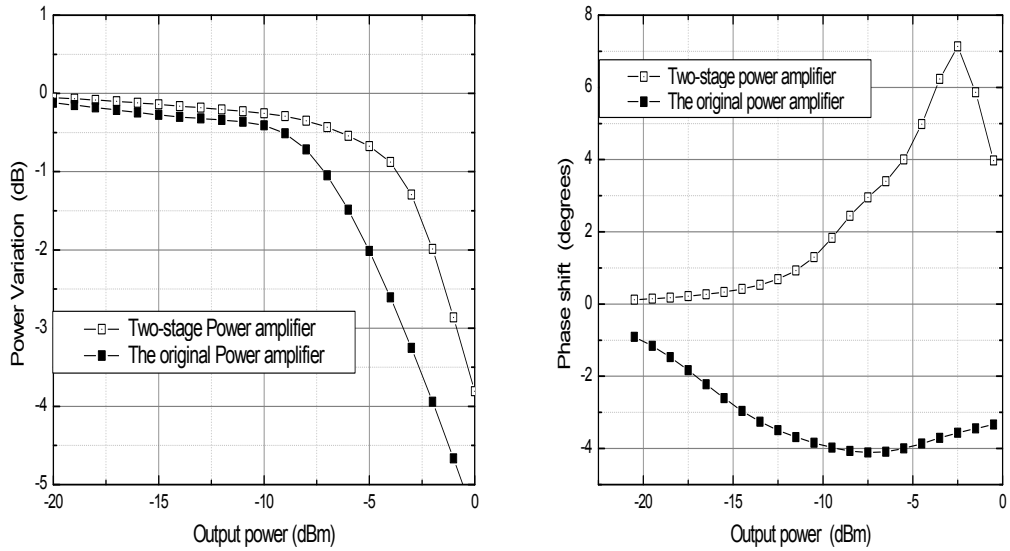

Fig.4.21 AM-AM and AM-PM of original and two-stage power amplifier

Chapter 5

Conclusion and the future work

The increasing demands for high data rates are pushing systems to utilize more and wider bands at higher frequencies. Now, the 60GHz-band short-distance communication technology has become the hot topic of the wireless researches. As the last building block before the antenna, RF power amplifier is critical for wireless communications system.

In this thesis, we have presented the design of a power amplifier based on the injection-locked technique in 60GHz band. First of all, the basic principle of the proposed injection locked power amplifier is analyzed. And then, the balun based on the Marchand type with centre-tap is introduced. Finally, the simulation results of this type of power amplifier are got. The results show that the amplifier delivers a gain of 20dB, a P_{sat} of 15dBm and a OP_{1dB} of 7.9 dBm under a 1.2V supply voltage. At 1-dB compression point, the power added efficiency is 6%.

Moreover, several methods are used to linearize this injection-locked power amplifier. First of all, adaptive biasing technique is introduced, and the simulation results show that the linear operation region is extended by 3.6 dB. Next, the pre-distortion technique is used and due to the output power limitation, the linear operation region is extended slightly, but its AM-PM performance is improved obviously. Considering the advantage of these two techniques respectively, we combine them together to improve not only the linear region but also the AM-PM performance. The simulation results show that the PA delivers a OP_{1dB} of 11.5dBm, a PAE of 13.5%, and phase shift is within the ranging from -1.75 to 0.5 degrees. Finally, two-stage power amplifier is proposed. The first stage and the injection-locked stage deliver a gain of 8dB and 12dB respectively. At the high output power level, the first stage produces a boost gain, and this expansion gain compensates the second-stage

gain reduction perfectly. The simulation results show that the power amplifier delivers a gain of 20dB, a P_{sat} of 16.3dBm, a P_{1dB} of 15.41dBm, and a PAE of 30%.

In this thesis, single tone harmonic balance simulation is used to simulate the amplifier and tuning for harmonic frequency components was discarded. The future work will focus on two-tone measurements and a good extension of this thesis would be to make further discussion of IM3.

Furthermore, for the two-stage power amplifier, we analyze and discuss the results but the operational principle is unknown and the next work is to figure out the reason and explain how it works.

Finally, we just give the pre-simulation results in this thesis, and the future work will focus on layout, post-simulation and test.

Reference

[1]. Umar H. Rizvi, Gerard J. M. Janssen, and Jos H. Weber. “Impact of RF Circuit Imperfections on Multi-Carrier and Single-Carrier based Transmissions at 60 GHz”. in Proc. IRWS2008,Orlando, FL. Jan. 2008, pp. 691-694.

[2]. J. Chen and A. M. Niknejad, “A Compact 1V 18.6dBm 60GHz Power Amplifier in 65nm CMOS” , ISSCC Dig. Tech. Papers,pp. 432-433, Feb. 2011.

[3]. Ahmed EI Oualkadi, “Trends and Challenges in CMOS Design for Emerging 60 GHz WPAN Applications”, Advanced Trends in Wireless Communications, ISBN: 978-953-307-183-1, InTech,Benedikt.

[4]. Mounir Youssef Bohsali, “Millimeter - Wave CMOS Power Amplifiers Design”, University of California at Berkeley, 2009.

[5]. Burcin Baytekin. “Analysis and Design of Monolithic Radio Frequency Linear Power Amplifiers”, University of California at Berkeley, 2004.

[6]. Jonas Fritzin, “CMOS RF Power Amplifiers for Wireless Communications.”, Linköpings universitet, 2011.

[7]. Srñan Glišić. “Design of Fully Integrated 60 GHz OFDM Transmitter in SiGe BiCMOS Technology”, 2011.

[8]. Mounir Youssef Bohsali. “Millimeter - Wave CMOS Power Amplifiers Design”, University of California at Berkeley Technical Report No. UCB/EECS-2009-25, 2009.

[9]. Steve C. Cripps, RF Power Amplifiers for Wireless Communications, Artech House, 1999.

[10]. Feiyu Wang. “Design and analysis of high-efficiency L-band power amplifiers”, Dissertation (Ph.D.), California Institute of Technology, 2006.

[11]. Mark A Briffa, “Linearization of RF Power Amplifiers”, Dissertation (Ph.D.), Victoria University of Technology, 1996.

[12]. T.H. Lee, “The design of CMOS radio-frequency integrated circuits”, 1 st Edition, Cambridge University Press, 1998.

[13]. Stephen Bruss, “Linearization methods”, 2003.

[14]. Steve C. Cripps, Advanced Techniques in RF Power Amplifier Design, Artech House, 2002

[15]. P. B. Kenington, “High linearity RF amplifier design”, Artech House Inc, 2000.

[16]. Morris KA & McGeehan, “Gain and Phase Matching Requirements of Cubic Predistortion Systems”, IEEE Electronics Letters, 36(21), 1822-1824.

[17]. A. Buonomo and A. Lo Schiavo, “Modelling and analysis of differential VCOs,” International Journal of Circuit Theory and Applications, vol. 32, no. 3, pp. 117–131, 2004.

[18]. L. J. Paciorek, “Injection locking of oscillators,” Proceedings of the IEEE, vol. 53, no. 11, pp. 1723–1727, 1965

[19]. R.Adler, “A study of locking phenomena in oscillators”, Proceed-ings of the IRE, vol. 34, no. 6, pp. 351–357, 1946.

[20]. S. Verma, H. R. Rategh, and T. H. Lee, “A unified model for injection-locked frequency dividers”, IEEE Journal of Solid-State Circuits,38(6) (2003) 1015-1027.

[21]. B. Razavi, “A Study of Injection Locking and Pulling inOscillators,” IEEE J. Solid-State Circuits, vol. 39, no.9, pp.1415-1424, Sep. 2004.

[22]. M. Tormanen, J. Lindstrand, and H. Sjoland, A 13dBm 60GHz-band injection locked PA with 36% PAE in 65nm CMOS, in:2011 Asia-Pacific Microwave Conference Proceedings (APMC), 2011, pp. 1-4.

[23]. King Chun Tsai, “CMOS Power Amplifiers for Wireless Communications,”

[24]. Y. Uemichi, H. Hatakeyama, T. Aizawa, K. Okada, H. Kiumarsi, S. Tanoi, N. Ishihara, and K. Masu, "Low-loss and compact millimeter-wave balun on Si," in 2011 IEEE MTT-S International Microwave Symposium Digest (MTT), Baltimore, USA, June 2011, 1-4.

[25]. Leijun Xu, Henrik Sjöland, Markus Törmänen, Tianhong Pan and Xue Bai. “A 60 GHz Marchand Balun with Floating Ground Centre-tap in CMOS Technology”. Progress In Electromagnetics Research Symposium, Taibei, Taiwan, March 25-28, 2013.

[26]. Jenny Yi-Chun Liu, “Millimeter-Wave Self-Healing Power Amplifier With Adaptive Amplitude and Phase Linearization in 65-nm CMOS”, IEEE Transactions on microwave theory and techniques, VOL. 60, NO. 5, MAY 2012.pp 1342-1352

[27]. Jenny Yi-Chun Liu, “A 60 GHz Tunable Output Profile Power Amplifier in 65 nm CMOS”,

IEEE Microwave and wireless components letters, VOL. 21, NO. 7, July 2011,pp 377-379

[28]. R. D. Singh and K. W. Yu, “A linear mode CMOS power amplifier with self-linearizing bias,” in ASSCC Dig. Tech. Papers, Nov. 2006,pp. 251–254.

[29]. J.-H. Tsai, H.-Y. Chang, P.-S. Wu, Y.-L. Lee, T.-W. Huang, and H. Wang, “Design and analysis of a 44 GHz MMIC low-loss built-in linearizer for high-linearity medium power amplifiers,” IEEE Trans. Microw. Theory Tech., vol. 54, no. 6, pp. 2487–2496, Jun. 2006.

[30]. Jeng-Han Tsai, “A 60 GHz CMOS Power Amplifier With Built-in Pre-Distortion Linearizer”, IEEE Microwave and wireless components letters, VOL. 21, NO. 12, DECEMBER 2011

[31]. Gary Hau, Takeshi B. Nishimura, “A Highly Efficient Linearized Wide-Band CDMA Handset Power Amplifier Based on Predistortion Under Various Bias Conditions” IEEE Trans. Microw. Theory Tech., vol. 49, no. 6, pp. 2487–2496, Jun. 2001.