Master's Thesis

Development of Ni-based Ohmic contacts to InAs and InGaAs

By

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Abstract

Low specific contact resistivity (ρ_c) of alloyed Ni/Pd/Au and nonalloyed Ti/Pd/Au Ohmic contacts to unintentionally doped n-InAs and n^+-$In_{0.63}Ga_{0.37}As$, which is a potential candidate for highly scaled HBTs and MOSFETs, is reported. Contacts were formed by UV-ozone oxidation and oxide removal with 1:1 HCl:DI water, and then deposited by either thermal evaporation or sputtering, followed by annealing. Finally, specific contact resistivities of Ohmic contacts were extracted using the transmission line model (TLM).

The lowest contact resistivity of Ni contacts was $3.02 \cdot 10^{-8}\ \Omega cm^2$ to unintentionally doped n-InAs after a 150 ℃ annealing for duration of 1 min, while the lowest contact resistivity of Ti contacts was found to be $3.29 \cdot 10^{-8}\ \Omega cm^2$ to n-InAs, annealed at 300 ℃. This indicates that the alloyed Ni contact exhibited somewhat lower contact resistivity than the nonalloyed Ti contact, but they are comparable. Furthermore, the lowest contact resistivity of all was obtained from the alloyed Ni contact to n-InAs. They have a narrow band gap where the Fermi level pins close to the conduction band, which in turn gives rise to better Ohmic contacts.

Acknowledgments

First and foremost I would like thank my advisor Erik Lind. His guidance, motivation and suggestions have been invaluable. He showed a constant willingness to help, and devoted many hours to discussions and explanations, as well as giving valuable suggestions on how to overcome obstacles and problems during the project. His optimism, encouragement and patience have been greatly appreciated throughout.

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I would like to thank my classmates and friends I've got in Sweden during the last two years. You in particular made the last two years enjoyable for me. I also want to thank my old friends abroad. Though I have seen much too little of you during the last years, your support and love have meant everything to me.

Also, despite being half a world away, my family has given me strength with their love and care throughout. I devote this thesis to them.

Eunjung Cha

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CHAPTER 1

1 Introduction

Due to their very high injection velocity [1][2], Ⅲ－Ⅴ compound semiconductors are highly attractive as a channel material and a contact layer in metal-oxide-semiconductor field-effect-transistors (MOSFETs) and heterojunction bipolar transistors (HBTs), respectively. In particular, Ⅲ－Ⅴ MOSFETs with InAs channels [3][4] as well as InGaAs channels [1][5][6] are being extensively studied for future high speed low-supply-voltage logic applications. In addition, InP-based HBTs with InGaAs contact layers have been employed in many of the widest-bandwidth electron devices [7][8] due to their advantages for scaling and thus potential for high speed operation with low power consumption. As device dimensions are scaled down to increase device bandwidths [9][10], both MOSFETs and HBTs require low resistance Ohmic contacts. For HBTs, emitter and base contact resistivities must be reduced proportionally to the inverse square of the transistor bandwidth [9]. MOSFETs similarly require reductions in contact resistivity proportionally to the inverse of the square of the device bandwidth [11]. Therefore, a reduction in contact resistivity is of central importance to the development of wide bandwidth electronics.

A self-alignment of metal contacts to source/drain (S/D) regions and emitter/base contact layers [12][13] are desirable for Ⅲ－Ⅴ MOSFETs and HBTs, respectively, to achieve low contact resistance which resembles the salicide process in Si CMOS technology [2]. Although self-aligned molybdenum (Mo) contacts to n-InAs and nickel germanide metal contacts to n-GaAs have demonstrated low contact resistance [14][15], historically there are few reports on the demonstration of a “silicide-like” contact for Ⅲ－Ⅴ materials using direct reaction between a metal and Ⅲ－Ⅴ materials. However, recently advances have been made and the existence of a stable “nickelide” metallic phase from the reaction of nickel with InAs and InGaAs via annealing has been demonstrated [2][4][5]. It has been reported that a NiInAs (nickelide) phase is in thermal equilibrium with InAs [16]. In addition, a stable low sheet resistance crystalline NiInAs forms a smooth

and abrupt interface with InAs as reported in [4][17]. Furthermore, a negligible Schottky barrier height at the nickelide/semiconductor ($In_xGa_{1-x}As$, $x > 0.7$) is expected which in turn contributes to better Ohmic contacts [5][18]. An abrupt and controllable Ni-InGaAs/InGaAs interface also has been demonstrated [2][5][6].

In this work, we report a development of Ni-based Ohmic contacts to unintentionally doped n-InAs (a carrier concentration of $5 \cdot 10^{18}$ cm^{-3}) and n^+-$In_{0.63}Ga_{0.37}As$, suitable for self-aligned metallization in order to achieve low contact resistivities. Since the contact resistivity has a strong dependence on surface preparation prior to contact deposition [10][19][20], we compare the effect between oxygen plasma ashing and UV-generated ozone. Ni/Pd/Au and Ni/W/Au are deposited by thermal evaporation and sputtering, respectively, followed by annealing for 1 min which results in the formation of Ni alloy. A transmission line model (TLM) is utilized to extract the contact resistivity between a metal and a semiconductor material afterwards. Since Ti/Pd/Au contacts have been showed to form nonalloyed Ohmic contacts with low resistance [19][21-24], Ti contacts are also developed and compared with alloyed Ni contacts.

CHAPTER 2

2 Theory

2.1 Ohmic contacts

The purpose of this project was to study the minimum possible contact resistivity of a metal-semiconductor contact. So it is important to know about the metal-semiconductor contacts first. There have been extensive studies about metal-semiconductor contacts over the past several decades since metal-semiconductor contacts are an essential part of semiconductor electronics and optoelectronic devices. After the Schottky (rectifying) contact was found first by Braun in 1874 [25], Walter Schottky [26] and N. F. Mott [27] proposed the theory on formation of a Schottky barrier which results in the rectification behavior of metal-semiconductor contacts. In addition, metal-semiconductor contacts can show non-rectifying (Ohmic) behavior which is extensively used in applications of semiconductor devices and integrated circuits.

Fig. 2. 1 shows the basic energy band diagram of a metal-semiconductor (n-type) contact. The Schottky barrier height φ_B between a metal with work function φ_m and a semiconductor with an electron affinity χ is given by

$$\varphi_B = \varphi_m - \chi \tag{2.1}$$

where χ is

$$q\chi = q\varphi_s - (E_c - E_{fs}) \tag{2.2}$$

and φ_s is the work function of the semiconductor, E_c is the conduction band energy and E_{fs} is the Fermi energy level in the semiconductor.

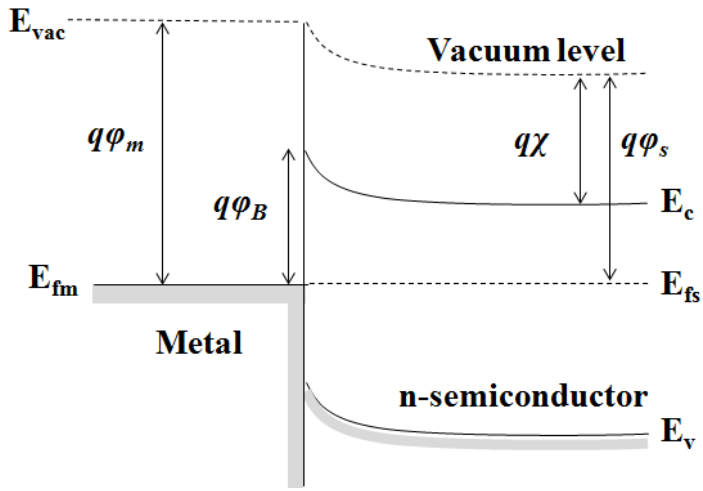


Fig. 2. 1. A basic energy band diagram at a metal-semiconductor (n-type) interface.

Unlike the Schottky-Mott theory which predicted a strong dependence of the Schottky barrier height on the metal work function, the Schottky barrier height is insensitive to the metal work function in practice. This is because of the "Fermi level pinning". Due to the non-ideal nature of the semiconductor surface, there are oxides or dangling bonds on the semiconductor surface which result in surface states within the energy band gap of the semiconductor [28]. These surface states can appear either as donor or acceptor surface states. For an n-type semiconductor, the donor surface states will exist with positive charges which result in upward band-bending near the semiconductor interface before contacting with the metal as presented in Fig. 2. 2 (a). The surface Fermi energy is known as the neutral level which appears $e\varphi_0$ above the surface valence band energy. Since there are an enormous number of surface states at the interface, the Fermi energy can be pinned effectively after being brought into contact as shown in Fig. 2. 2 (b). Hence this Fermi level pinning makes the Schottky barrier height little dependent on the metal work function and only dependent on the properties of the semiconductor [29] and the Schottky barrier height becomes

$$e\varphi_b = E_g - e\varphi_0 \tag{2.3}$$

where E_g is the band gap energy of the semiconductor. Note that although various theories have been tried to explain the origin of Fermi level pinning [30-34], it has yet to be clearly understood.

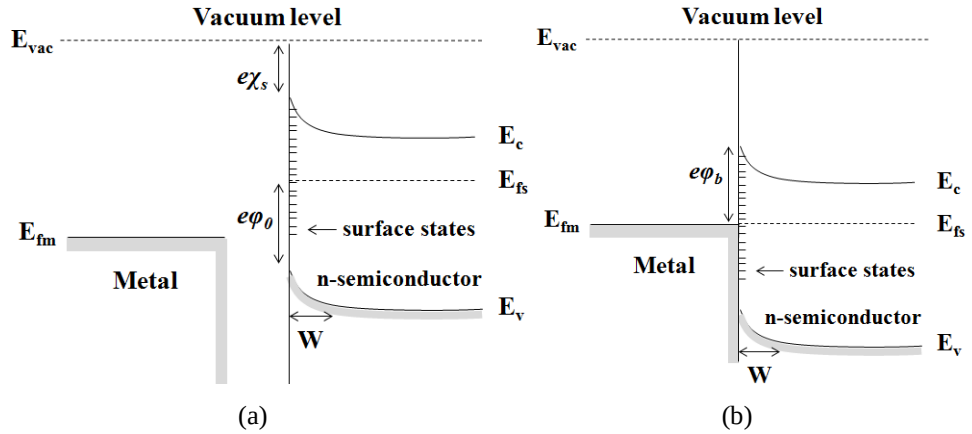


Fig. 2. 2. Energy band diagram of a metal-semiconductor (n-type) with surface states interface (a) before and (b) after contact.

Across the Schottky metal-semiconductor junction, electrons can travel both directions, from the semiconductor to the metal and vice versa. The difference between the two opposing current flows result in a net current and the overall current is determined by an applied voltage *V*. Fig. 2. 3 illustrates three basic mechanisms for current flow; 1- thermionic emission of electrons (the majority carrier) from the semiconductor into the metal, 2- tunneling of electrons from the semiconductor into the metal, 3- thermionic emission of holes (the minority carrier) from the metal into the semiconductor [28]. Thermionic emission can occur when the carriers have enough thermal energy to go over the barrier. For an n-type semiconductor, the thermionic emission current of electrons is dominant compared to the thermionic emission current of holes. Tunneling, which is a quantum mechanical phenomenon, can occur if the barrier width (depletion width, *w* in Fig 2. 2 (b)) is very small for heavily doped semiconductors which leads Ohmic contacts. Thus thermionic emission of electrons is the dominant contribution to the *I-V* characteristics for the Schottky junction. For forward bias, the energy barrier is lowered, giving exponential increase in current. For reverse bias, on the other hand, the energy barrier becomes higher, giving a constant reverse bias current. Hence the Schottky junction shows a rectifying behavior, and it is known as a Schottky diode [28].

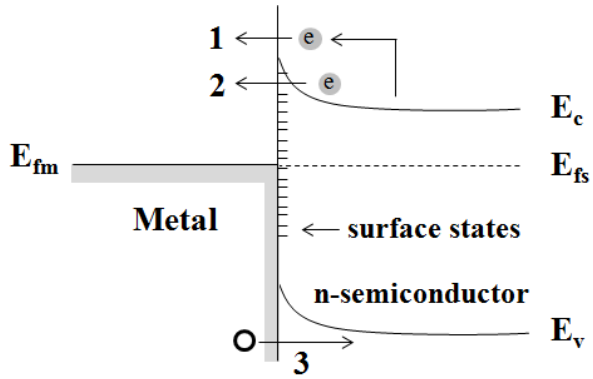


Fig. 2. 3. Schematic of three basic mechanisms for current flow in the metal-semiconductor junction.

On the other hand, in the case of Ohmic contacts, tunneling is a main carrier transport mechanism. It occurs when the width of the depletion region w becomes very thin with heavy doping concentration N in the semiconductor close to the interface, $w \sim N^{-1/2}$; electrons can tunnel through sufficient narrow depletion region in both directions as illustrated in Fig. 2. 4, giving a linear *I-V* characteristic [28]. Since Ohmic contacts allow current to flow between semiconductors and metals easily, it leads to a high current density at a low applied voltage which is attributed to a low resistance. Thus, Ohmic contacts are a crucial integral part of all semiconductor devices and find application in external wiring or circuits for applying voltages and supplying current from external metal sources to semiconductor materials.

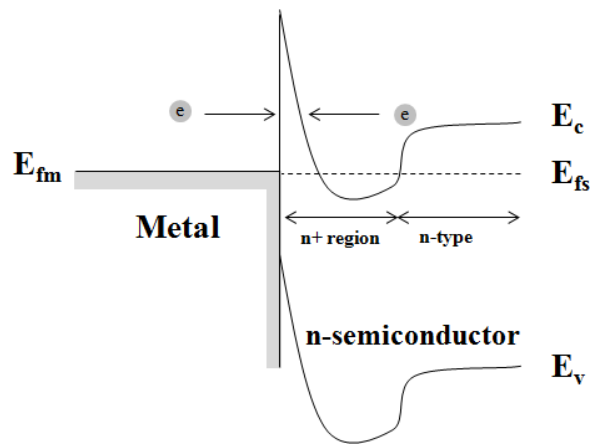


Fig. 2. 4. Schematic of an Ohmic contact between a metal and an n-type semiconductor, illustrating tunneling.

2.2 Contact resistance

For heterojunction bipolar transistors (HBTs), a scaling of transistors is continued in order to attain higher bandwidth. For scaling, contact resistivities are presently the most serious barrier since contact resistivities must be reduced by γ^2:1 in order to obtain a γ:1 increase in circuit bandwidth. γ is a scaling factor. For simultaneous THz f_t (the cutoff frequency) and f_{max} (the maximum oscillation frequency), a contact resistivity less than $2.5 \cdot 10^{-8}\ \Omega\ \mathrm{cm}^2$ is required [9].

In the case of MOSFETs, the current gain cut-off frequency f_t is given by

$$\frac{1}{2\pi f_t} = \frac{C_{gg,t}}{g_m} + \frac{C_{gg,t}}{g_m}(R_s + R_d)g_d + (R_s + R_d)C_{gd,t} \tag{2.4}$$

where $C_{gg,t} = C_{gs,t} + C_{gd,t} = C_{gs,i} + C_{gs,f} + C_{gd,t}$ is the total gate capacitance, g_d is the output conductance, $C_{gd,t}$ is the total gate to drain capacitance and R_s, R_d are the parasitic source and drain resistances as shown in Fig. 2. 5 [35]. For long gate lengths, the first term in (2.4) becomes $\frac{C_{gs,i}}{g_m}$ approximately and it is known as the intrinsic delay of the transistor $\tau_{int}=L_g/v$, where v is the electron velocity under the gate. The second and third terms in (2.4) refer to the RC delay time of the transistor [35].

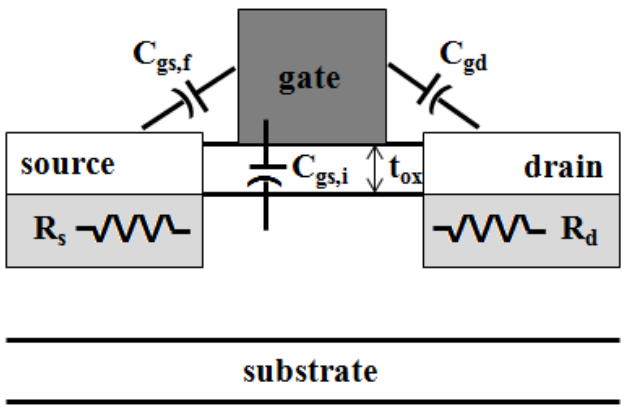


Fig. 2. 5. Schematic of a MOSFET showing all the capacitances and resistance in the on state ($V_{gs} = V_{ds} = V_{dd}$).

By scaling down both the lateral and vertical device dimensions by a factor of γ:1, the device bandwidth can be increased by γ:1 by reducing all the

delays and capacitances by γ^2:1 while keeping all resistances, voltages and currents constant [36]. First of all, reducing the gate oxide thickness t_{ox} leads an increase in the equivalent gate capacitance $C_{gs,i} = C_{eq} \approx 1/t_{ox}$ per unit area. Scaling the gate width W_g by γ:1 keeps $g_m \approx W_g C_{eq} v_{inj}$ and $I_d \approx W_g C_{eq} v_{inj}(V_g - V_t)$ constant.

As indicated in Fig. 2. 6, decreasing the gate length L_g by γ:1 reduces the total gate capacitance $C_{gs} = C_{eq} W_g L_g + \alpha W_g$ by γ:1 and other parasitic capacitances C_{gd}, C_{sb} and $C_{db} \propto W_g$ are also reduced by γ:1. While reducing L_g, the source/drain contact length $L_{s/d}$ is also reduced by γ:1 in proportion with the gate length. Since the source resistance $R_S = \frac{\rho_c}{L_{s/d} W_g} + \frac{\rho_c L_{s/d}}{W_g}$ should be kept constant, the specific contact resistivity ρ_c is required to be reduced by γ^2:1 [11]. As a result, ultra low resistance metal-semiconductor contacts are essential to the continued scaling of transistors and an Ohmic contact is a suitable option since it has very low resistance as explained above. Therefore, we have investigated Ohmic contacts between metals (Ni, Ti) and semiconductor materials (unintentionally doped n-InAs, n^+-$In_{0.63}Ga_{0.37}As$) and studied ways for reducing the contact resistivity ρ_c.

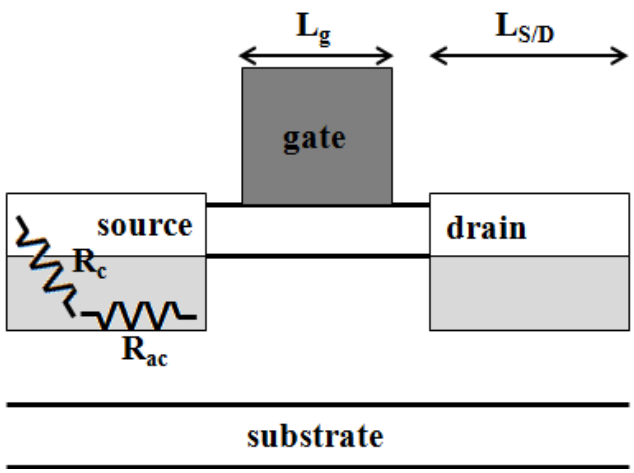


Fig. 2. 6. Schematic of a MOSFET showing the source resistance components.

Ⅲ－Ⅴ compound semiconductors are highly attractive as channel materials in metal-oxide-semiconductor field-effect-transistors (MOSFETs) due to their very high injection velocity [1][2]. In particular, Ⅲ－Ⅴ MOSFETs

with InAs channels [3][4] as well as InGaAs channels [2][5][6] are being extensively studied for future high speed low power logic applications. However, several challenges exist for realizing Ⅲ－Ⅴ's superior transport properties and high drain current performance. One of the most critical challenges is source/drain (S/D) engineering to achieve low access resistance which includes the S/D sheet resistance, the metal-semiconductor contact resistance and the metal sheet resistance [6]. In this project, the aim is to achieve a low metal-semiconductor contact resistance by developing Ohmic contacts with metal contacts (Ni, Ti) on semiconductors (unintentionally doped n-InAs, n^+-$In_{0.63}Ga_{0.37}As$).

First of all, we need to check whether n-InAs and n^+-$In_{0.63}Ga_{0.37}As$ form Ohmic contacts on metals. As shown in Fig. 2. 7 (a), since highly doped $In_{0.63}Ga_{0.37}As$ is used, the depletion width becomes very narrow which in turn was the result that tunneling is the main current transport mechanism although the Fermi level is pinned in the band gap and 0.2 *eV* below the conduction band [31]. Hence, n^+-$In_{0.63}Ga_{0.37}As$ forms Ohmic contact on metals. In addition, since InAs has a narrow band gap of 0.36 *eV* (the band gap of $In_{0.63}Ga_{0.37}As$ is 0.65 *eV*), the Fermi level is pinned 0.2 *eV* above the conduction band [37] as indicated in Fig. 2. 7 (b). It gives a lower Schottky barrier height, thus allowing electrons to tunnel across the Schottky barrier easily with lower effective electron mass m^*. Narrow band materials give better Ohmic contacts [38][39]. Thus, unintentionally doped n-InAs also form Ohmic contact to metals.

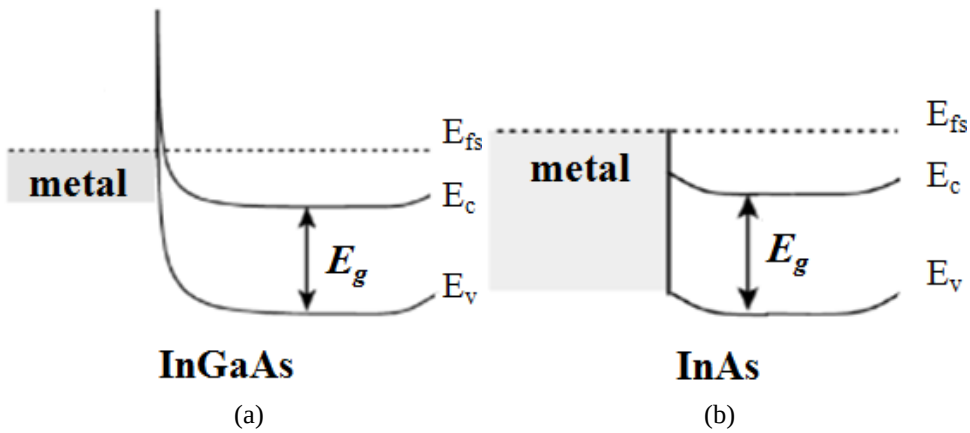


Fig. 2. 7. The metal-semiconductor contacts when using (a) n^+-$In_{0.63}Ga_{0.37}As$: Fermi level pinned in the band gap. (b) InAs: Fermi level pinned in the conduction band.

As a contact metal, Ni and Ti are introduced since they are easy to deposit by thermal evaporation and sputtering. In addition, recent advances have demonstrated that Ni reacts with InAs and InGaAs with annealing, and forms stable NiInAs and Ni-InGaAs metallic alloy phases [2][4-6]. As reported in [16], NiInAs (nikelide) is in thermal equilibrium with InAs. Also as reported in [2][4], NiInAs and Ni-InGaAs are mono-crystalline and poly-crystalline, respectively, and they exhibit an abrupt heterointerface. Therefore, the nickel metallic alloys formed after annealing also have Ohmic contacts on InAs and InGaAs. Unlike Ni, Ti does not form an alloy with either InAs or InGaAs, so we can compare between alloyed and nonalloyed Ohmic contacts to InAs and InGaAs with various annealing temperatures. However, as reported in [19][22-24], Ti starts to diffuse into a semiconductor layer (unintentionally doped n-InAs or n^+-$In_{0.63}Ga_{0.37}As$ in our case) above a certain annealing temperature which causes In outdiffusion from the semiconductor into the contact metal stack, so the Ti contact will exhibit degradation due to the intermixing of Au and In. In order to improve the thermal stability of the Ti contact, TiW based contacts, which behaved as an effective diffusion barrier, can be used instead of Ti [19].

One of the applications of the Ni contacts on the n^+-$In_{0.63}Ga_{0.37}As$ that can be found is a salicide-like metallization for InGaAs MOSFETs [2][6]. Since Ni directly reacts with InGaAs, self-aligned Ni-InGaAs metallic contacts are formed to the S/D regions comprising of n^+-InGaAs. In addition, self-aligned metal S/D n-MOSFETs using Ni-InGaAs alloy have been reported [5]. Due to low density of states in S/D regions [40], the reduction of the S/D resistance is one of the most critical challenges for realizing the full potential of Ⅲ－Ⅴ MOSFETs. Hence the Ni-InGaAs metallic S/D regions using the reaction of Ni with n-InGaAs (a channel layer) have been developed as a potential solution to reduce the resistance of S/D. However, it suffers from a high off-state drain current since there is no channel-to-S/D p-n junction.

In the case of Ni contacts on unintentionally doped n-InAs, nickelide has been utilized as ultrashallow metallic S/D junctions for self-aligned Ⅲ－Ⅴ nMOS [4]. Undoped InAs layers act as channels and ultrashallow metallic NiInAs S/D regions are formed by rapid thermal anneal (RTA) which shows controllable and atomically abrupt junctions.

Ti/Pd/Au contacts are used as conventional emitter electrodes on InGaAs contact layers for InP based HBTs [23]. Ti acts as an adhesive and barrier component and Pd blocks Au to penetrate into the underlying layers [21]. As explained above, Ti diffuses into InGaAs at high temperatures and thus can impair reliability [41]. However, the main purpose of developing Ti contacts in this project is to compare the contact resistivities of Ti contacts with that of Ni contacts which are alloyed Ohmic contacts.

Surface preparation plays an important role in determining the contact resistivity. In order to obtain very low resistivities ($< 10^{-8}\ \Omega cm^2$), removal of semiconductor surface oxides prior to contact deposition is crucial and the procedures used to remove surface oxides become decisive. Since *in situ* contact formation avoids air exposure to the samples after the surface preparation, it prevents surface oxidation and contamination [10]. On the other hand, *ex situ* techniques can cause a reproducible problem since the control of time between removing surface oxides and metal deposition is difficult even though *ex situ* contact formation can give low resistivities. As reported in [21], a $4.3 \cdot 10^{-8}\ \Omega cm^2$ contact resistivity to n-InGaAs and $1.7 \cdot 10^{-8}\ \Omega cm^2$ to n-InAs were obtained using *in situ* Ar^+ sputter cleaning prior to deposition of Ti/Pt/Au metal contact stack. Also, $\rho_c = 6 \cdot 10^{-9}\ \Omega cm^2$ to n^+-InAs was achieved with Mo contacts by *in situ* metal deposition. In the case of *ex situ* contact formation, with H_3PO_4 solution cleaning prior to Ti/Pt/Au contact metal deposition by electron beam evaporation, it provided $\rho_c = 2 \cdot 10^{-8}\ \Omega cm^2$ for n-InAs [39]. Adam et al. obtained $7.3 \cdot 10^{-9}\ \Omega cm^2$ resistivity Ohmic contacts to n-$In_{0.53}Ga_{0.47}As$ with Ti/Pd/Au layers, removing surface oxides by UV-ozone treatment and NH_4OH prior to e-beam deposition [19]. In this project, we have used *ex situ* contact formation and tried several different surface preparation procedures.

2.3 Transmission line model (TLM) analysis

The performance of metal-semiconductor Ohmic contacts is evaluated by extracting the specific contact resistivity ρ_c (ohm - cm^2) from a transmission line model (TLM) method. The TLM method was proposed by Berger [42] who developed a method for obtaining ρ_c for planar Ohmic contacts. Fig. 2. 8 shows the cross-sectional circuit model of the metal-semiconductor contact for the TLM method. The voltage and current differential equations in the contact region are

$$V'(x) = \frac{R_s}{W} I(x)dx \tag{2.5}$$

$$I'(x) = \frac{W}{\rho_c} V(x)dx \tag{2.6}$$

where W is the contact width and R_s is the semiconductor sheet resistance. Here the sheet resistances of the layer under the contact and outside the contact region are assumed to be the same. Combining (2.5) with (2.6), we get

$$V''(x) = \frac{R_s}{\rho_c} V(x) \tag{2.7}$$

The general solutions for $V(x)$ and $I(x)$ are

$$V(x) = \frac{IL_T R_s}{W} \frac{\cosh \frac{d - x}{L_T}}{\sinh \frac{d}{L_T}} \tag{2.8}$$

$$I(x) = I \frac{\sinh \frac{d - x}{L_T}}{\sinh \frac{d}{L_T}} \tag{2.9}$$

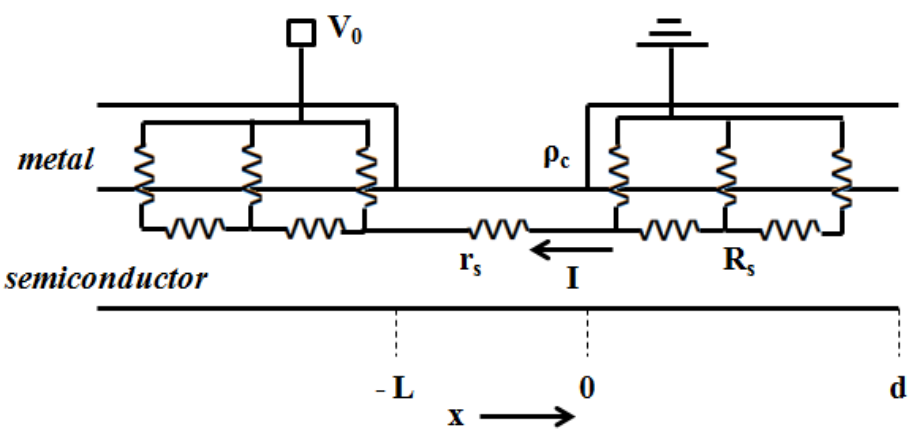


Fig. 2. 8. Circuit diagram of the metal-semiconductor contact for the TLM method.

where d is the contact length, I is the current flowing into the contact and L_T is the transfer length over which the voltage drops by $1/e$ along the contact. Then the contact resistance R_c at $x = 0$ is given by

$$R_c = \frac{V(0)}{I(0)} = \frac{\sqrt{\rho_c R_s}}{W} coth(\frac{d}{L_T}) \tag{2.10}$$

With the usual assumption of an electrically long contact $d \gg L_T$, for which $coth(\frac{d}{L_T}) \approx 1$, (2.10) becomes

$$R_c \approx \frac{\sqrt{\rho_c R_s}}{W} \tag{2.11}$$

and therefore

$$\rho_c \approx \frac{W^2 R_c{}^2}{R_s} \tag{2.12}$$

The total measured resistance R_T between two contacts separated by a gap, L_{gap}, is given by

$$R_T = \frac{2\rho_c}{WL_T} + \frac{R_s}{W} L_{gap} \tag{2.13}$$

and R_T can be plotted as a function of different pad spacings as shown in Fig. 2. 9. From the intersection of the y-axis,

$$R_c = \frac{\rho_c}{WL_T} \tag{2.14}$$

Therefore, from (2.11) and (2.14),

$$\rho_c = R_s \cdot L_T{}^2 \tag{2.15}$$

Then the transfer length L_T is then given by

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \tag{2.16}$$

which also can be measured from the intersection of the x-axis for $R_T = 0$ ($= -2L_T$) as shown in Fig. 2. 9. In addition, R_s is found from the slope ($= R_s/W$).

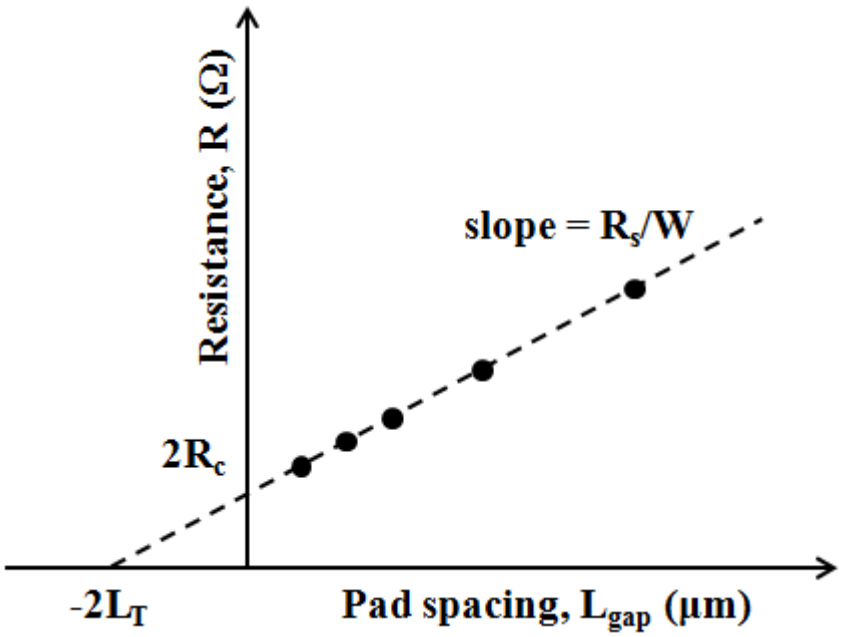


Fig. 2. 9. Plot of total resistance (R_T) as a function of L_{gap}.

CHAPTER 3

3 Method

3.1 Contact metal by thermal evaporation

For deposition of metal contacts, thermal evaporation and sputtering methods were used. In this section, the experimental details of thermal evaporation are presented.

First of all, the substrate was cleaned in a beaker with isopropanol (IPA) and ultra sonic, which made cleaning more effective, for 15 min. We used two different substrates; one was 50 nm undoped, but unintentionally doped n-InAs layers, with a carrier concentration of $5 \cdot 10^{18}$ cm^{-3}, grown on Si wafers using a 250 nm highly doped InAs buffer ($3 \cdot 10^{19}$ cm^{-3}) and the other was 20 nm highly doped $In_{0.63}Ga_{0.37}As$ layers grown on semi-insulating InP wafers with 100 nm $In_{0.53}Ga_{0.47}As$ buffer. Note that three different doping concentrations of Sn were used and the contact resistivity will be compared depending on the doping condition. After cleaning in an ultrasonic bath, the substrate was rinsed with IPA from a bottle and put in a new beaker with IPA. Then cleaning the substrate was finished after blowing N_2 gas to dry.

Next, photolithography was done before metal deposition to define the contact patterns. The sample was prebaked at 200 ℃ for 5 min, spin-coated LOR 3A at 3000 rpm for 45 s and soft baked at 160 ℃ for 3 min, and spin-coated S1813 at 4000 rpm for 60 s and soft baked at 115 ℃ for 90 s. After that, exposure of soft UV light and development of the exposed resist was done for two different purposes; the first exposure was done for removing the resist at the edges of the substrate which enhanced the resolution of the contact patterns since the resist thickness at parts close to the edges is usually thicker than the central, and the second exposure was for determining the contact patterns. The edge exposure was done by soft UV exposure for 8 s with soft-contact between the substrate and mask, and development of the exposed resist using MF 319 for 30 s. The contact

exposure was done in a similar way; soft UV exposure for 4 s with vacuum-contact, and development for 1 min. Before proceeding to the next step, the sample was rinsed with water for 1 min and inspected with an optical microscope in order to check that the contact patterns were well defined.

The next step is the deposition of the contact metal layers using thermal evaporation. Since a lift-off technique is used after evaporation, the resist layers were hard baked at 120 ℃ for 15 min in order to harden the resist to ensure that the pattern shape would not be deformed. To minimize the contact resistivity, the native oxide on the substrate surface was removed using either oxygen plasma ashing for 15 s or UV-generated ozone for 1 min, and then treated with 1:1 HCl:DI water for 30 s. As reported in [43], UV-ozone treatment not only oxidizes defective surface layers which can be easily removed by subsequent wet etching. But also, it results in a stoichiometric composition at the semiconductor surface after UV-ozone oxidation and oxide removal. After that, the sample was put into the thermal evaporation chamber, a step in which minimizing the time of the air exposure of the sample is important to get less native oxides on the surface of the samples. Ni (6 nm) / Pd (15 nm) / Au (200 nm) or Ti (6 nm) / Pd (15 nm) / Au (200 nm) were evaporated, where Au was used to make the measurement easier since it is very conductive and Pd to prevent the diffusion of Au into the Ni or Ti contacts. We have decided the thickness of the contact metal needs to be 6 nm as reported in [4]. A schematic picture of the sample with the evaporated metal layers is shown in Fig. 3. 1 (a). After the metal evaporation, the resist layers were removed by the lift-off process in which the sample was put in a remover 1165 at 70 ℃ in an ultrasonic bath for about 8 min. Fig. 3. 1 (b) illustrates the sample after the lift-off process.

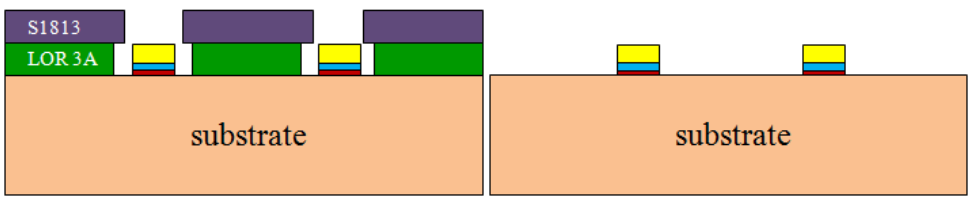
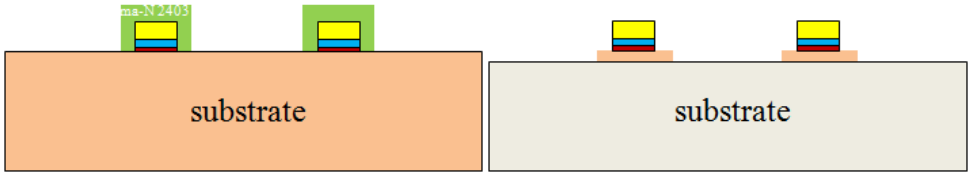


Fig. 3. 1. (a) The substrate after thermal evaporation of the contact metal layers (red – Ni or Ti, blue – Pd, yellow – Au). (b) After the lift-off process.



(a) (b)

Fig. 3. 2. (a) The substrate with the mesa patterns by photolithography when using negative resist (ma-N2403). (b) The sample after a wet etching with 1:1:25 H_3PO_4: H_2O_2:DI water. The grey and light brown parts in the substrate correspond to the Si or InP layer and the InAs or InGaAs, respectively.

The TLM structures were then isolated by developing mesa structures. In order for that, photolithography was used to pattern the mesa structures. One can use either a positive or a negative resist for this step and Fig. 3. 2 (a) shows the case with the negative resist of ma-N 2403 using deep-UV light exposure for 1 min and 30 s and ma-D 332 developer for 45 s. If one instead uses a positive resist such as S1813, soft UV exposure and MF 319 developer are needed. Note that as we eliminated resist at the edges first when the contacts were developed, the same procedures were used for the mesa structures; exposure of the edges, development of them and exposure of the mesa structures. Consequently, we proceeded with a wet etching with 1:1:25 H_3PO_4: H_2O_2:DI water (3 min for InAs and 90 s for InGaAs). After that, the resist was removed rinsing with acetone and one can find the final sample as illustrated in Fig. 3. 2 (b) where the isolation etching step is finished.

The final step is to anneal the sample by rapid thermal anneal (RTA) to make the contact metals (Ni and Ti) react with the substrate (InAs and InGaAs) and thus form a stable “nickelide” metallic phase in the case of Ni contacts [4]. As reported [4], the InAs with the Ni contacts was treated by RTA in N_2 ambient for 1 min at various temperature. Since the lowest R_s was measured at 350 ℃ where the monocrystalline NiInAs was found, we also decided to anneal the sample at 350 ℃ for 1 min [4]. In the case of the InGaAs substrates with the Ni contacts, a Ni-InGaAs metallic alloy is found at a low temperature of 250 ℃ with RTA for 1 min [2][5]. In addition, a formed Ni-InGaAs is thermally stable between 350 and 450 ℃ when it was RTA for 5 min [6]. Thus, the sheet resistance and the contact resistivity of the Ni contacts on the InAs and InGaAs substrates were evaluated with RTA in N_2 ambient at 150 – 400 ℃ for 1 min. The same RTA conditions were used for the Ti contacts on the InAs and InGaAs substrates.

In order to measure the resistance of the annealed samples, a probe station – Cascade 11000 B which is located at Lund nano lab of the nanometer structure consortium [44] – was used. While the current was applied ascending from - 10 to 10 mA, the potential drops were measured for several different gap spacings. In the case of the first TLM structure design, there were seven different gaps ascending from 10 to 70 μm increasing by 10 μm, and the width at a constant 20 μm. On the other hand, in the case of the redesigned TLM structure, three widths of 10, 20 and 30 μm were used, and for each width, there were twelve gaps; 1, 2, 3, 4, 5, 6, 8, 10, 15, 20, 25 and 30 μm.

To obtain a more precise contact resistivity, we had to measure the actual widths and gaps after all processing steps were finished. This is because the patterned structures on the substrate are almost always different from the designed structures on the mask mainly due to the limited resolution of lithography. First, for the measurement of the widths and gaps, an optical microscope – Axio Imager M1m Zeiss [44] was utilized. However, a 100 x magnification is the maximum which is insufficient during the measurement of the gaps, especially for the redesigned structures since the gap spacing becomes smaller than 10 μm which goes down to 1 μm. In order to improve the resolution, we used a scanning electron microscope – FEI Nova NanoLab 600 which produces images magnified over 2500 KX [44]. The distances were measured with built-in software right after obtaining images with the SEM as presented in Fig. 3. 3. We measured several gap distances and then averaged them out. It should give a reasonably close value to the actual gap spacing which in turn would help to extract a more accurate contact resistivity. However, it is still not enough to obtain an accurate gap distance using this method even if one measures more distances than shown in Fig. 3. 3. This is because the points at the corners of the gap show round shapes, instead of being at right angle, where the distances are bigger than them at the middle, straight parts at which we find the most desirable and closest distance to the structures on the mask.

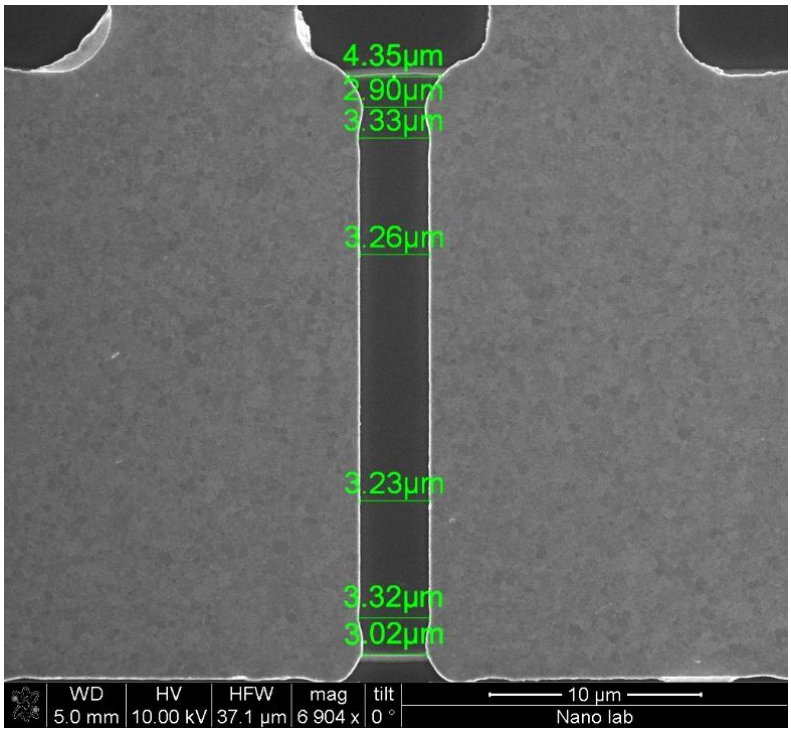


Fig. 3. 3. SEM image of the gap of 2 µm with the width of 32 µm – measuring the gap distance while taking an image with the SEM.

In order to get a more accurate measurement of the gap distance, the final method we used was a numerical integration. Specifically we used the Matlab program [45] to get a measure of the gap distances along the width. The gap was measured on the SEM image at more than 20 different places within the width. The integral for the resulting curve was given by the Matlab program, and the integral was then divided by the width, to yield a good estimate of the gap distance, see Fig. 3. 4. This method requires more time to measure the distances, especially at around the corners, but would be the optimal way of obtaining the gap distance with a higher accuracy than the other methods mentioned above. Note that one does not have to take many points at the middle parts since they do not vary much, but increasing the number of data points at the corners increases the accuracy of this method.

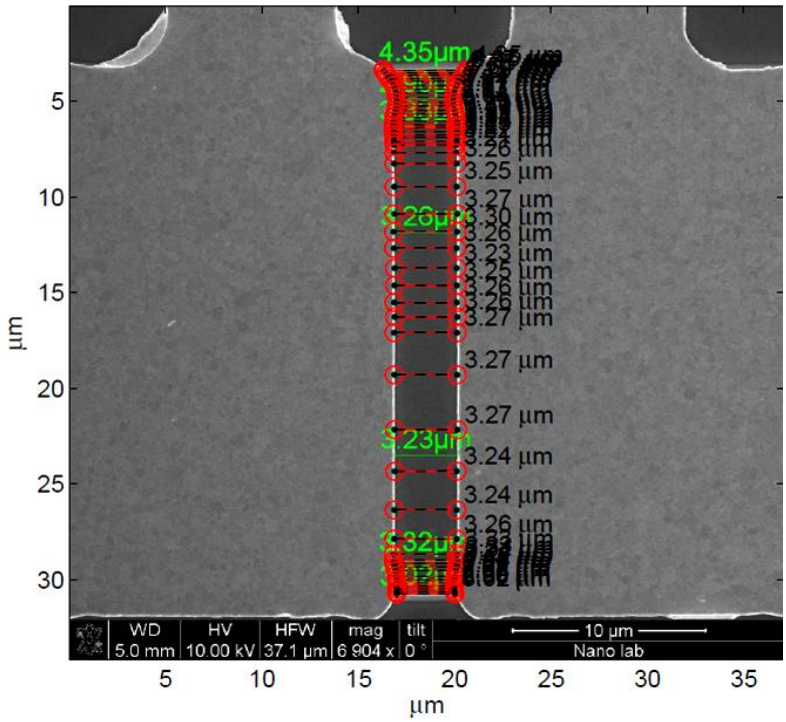


Fig. 3. 4. The same SEM image as shown in Fig. 3. 3, but showing another method of measuring the gap distance on the SEM image with the Matlab program.

3.2 Contact metal by sputtering

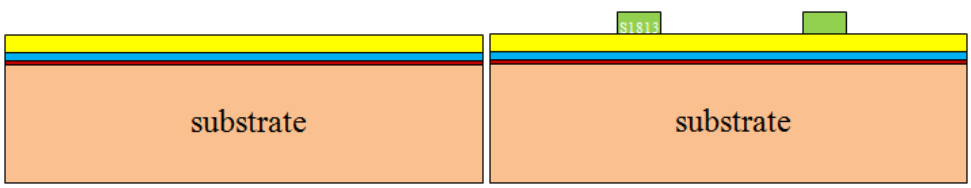
As another way of depositing of metal contacts, sputtering was used to deposit Ni and Ti on unintentionally doped n-InAs and n^+-InGaAs substrates. The lift-off process has a clear advantage of an easy processing, but it does not always give the sharpest shape of the structures. Also, our lift-off process was incompatible with sulfur passivation (see later in section 4.1.1.2), so we would like to compare the contact resistivity between sputtering and thermal evaporation. In addition, sputtering allows an *in situ* Ar^+ cleaning of the sample and deposition of metal contacts in the sputtering chamber. As explained in the theory section, the contact resistivity is strongly dependent on surface preparation. Thus, sputtering would improve the contact resistivity. In this section, the experimental details of sputtering are presented.

When developing the metal contacts by thermal evaporation, the structures were patterned by lithography and then the metal layers were deposited. On the other hand, for the sputtering method, deposition of the contact metal

should be done first instead. Before starting the deposition process, the substrate should first be cleaned the same way as done before the lithography step at section 3. 1. The substrate was cleaned in a beaker with isopropanol (IPA) and ultra sonic, for 15 min. After that, the substrate was rinsed with IPA from a bottle and put into a new beaker with IPA, and then dried with N_2 gas.

As mentioned in section 3. 1, before loading the sample into a sputter chamber, the native oxide on the substrate surface was removed using oxygen plasma ashing for 15 s or UV-ozone oxidation for 1 min, and then treated with 1:1 HCl:DI for 30 s. After that, the sample was immediately loaded into the sputter chamber and Ni (6 nm) / W (60 nm) / Au (200 nm) or Ti (6 nm) / W (60 nm) / Au (200 nm) were deposited on the semiconductor surface as shown in Fig. 3. 5 (a). Next, lithography followed. In contrast to the lift-off process, only one layer of photo resist (S1813 or ma-N2403) was spin coated and the subsequent UV exposure of the edges and structures and the development of them followed as illustrated in Fig. 3. 5 (b). Soft-baking the sample at 120 ℃ for 15 min hardened the patterned resist and ensured that the resist could act as an etch mask for a next etching process.

Prior to the etching of the metal layers, the unnecessary resist, which might still exist at undesired points, was removed using oxygen plasma for 30 s. After that, Au was etched by stirring it in a beaker with 1:2:17 KI:I_2:DI water for 1 min and the sample was rinsed with water for 15 s. Note that one needs to check thoroughly if the Au had been totally etched away with the optical microscope; otherwise W cannot be properly etched at the next step due to the blockade of the Au layer. A gold-etchant is very aggressive, so it can easily result in over-etching of Au, so repeated short dipping of the sample followed by optical microscope inspection is required.



(a) (b)

Fig. 3. 5. (a) The substrate after sputtering the contact metals (red – Ni or Pd, blue – W, yellow – Au). (b) The sample after the lithography process when positive resist (S1813) was used.

After the Au etching, W was removed with a reactive ion etching system – Trion T2 [44] using mixture gases of Ar and SF_6 for 45 s. Following the W dry etching, the resist which had acted as the etch mask was removed by oxygen plasma for 1 min and rinsed with acetone for 1 min. Finally Ni or Ti was etched. For Ni etching, we used H_2SO_4:HNO_3:CH_3COOH:DI water = 1:2.5:2.5:15 for 3 min. Note that this Ni etchant also etched the InAs and InGaAs substrates, so we added more DI water, up to the ratio presented above, to dilute the etchant so that we had more control over the Ni etching without etching the substrate too much. For Ti, the sample was dipped in a beaker with 1:10 HF:DI water for 30 s and then rinsed with water for 30 s.

All this was followed by mesa structure development and annealing steps, exactly as before, so we will skip the experimental details of them.

3.3 TLM structure design

In order to determine the accurate contact resistivity using a plot shown in Fig. 2. 9, it is important to have a well-designed TLM structure. For the first test, the structures shown in Fig. 3. 6 were used to find the contact resistivity. The resistance is determined by a four point probe measurement in which the current drives from I_{source} to the other one while the potential drop is measured at each V_{sense}. With four point probe measurement, the parasitic resistances, which include probe resistance as well as probe contact resistance, are excluded during the measurement. However, in these test structures, the measured resistance still contains the extra resistance due to the contact metal. The metal resistance component can be removed by measuring the potential drop at the contact edges as indicated in Fig. 3. 7, but in the first test structures, the potential drop was measured quite far from points close to the edges, so an error can arise when extracting the contact resistivity [10].

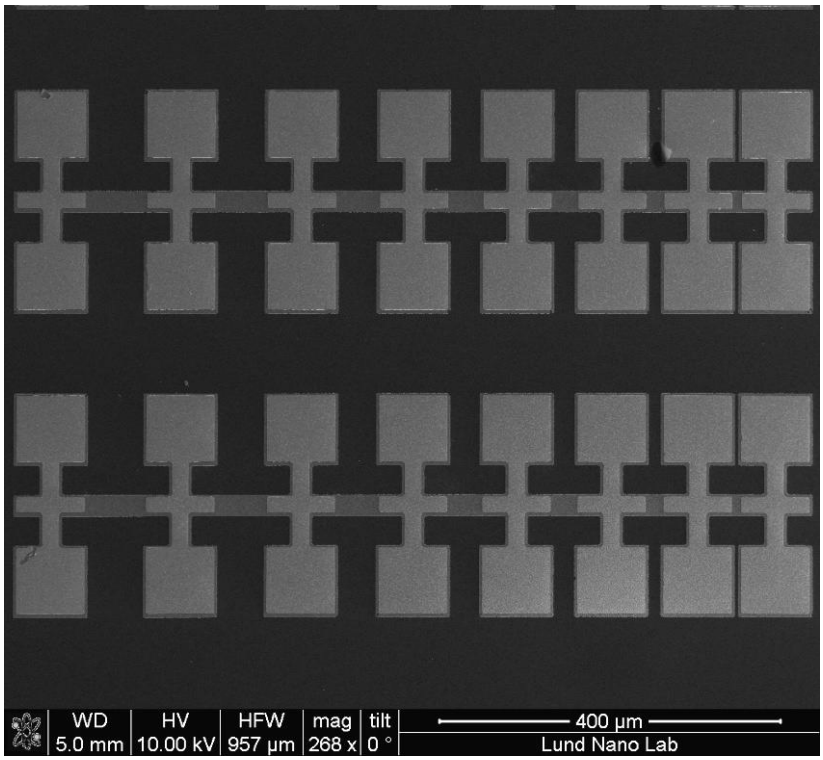


Fig. 3. 6. SEM image of the previous TLM structures.

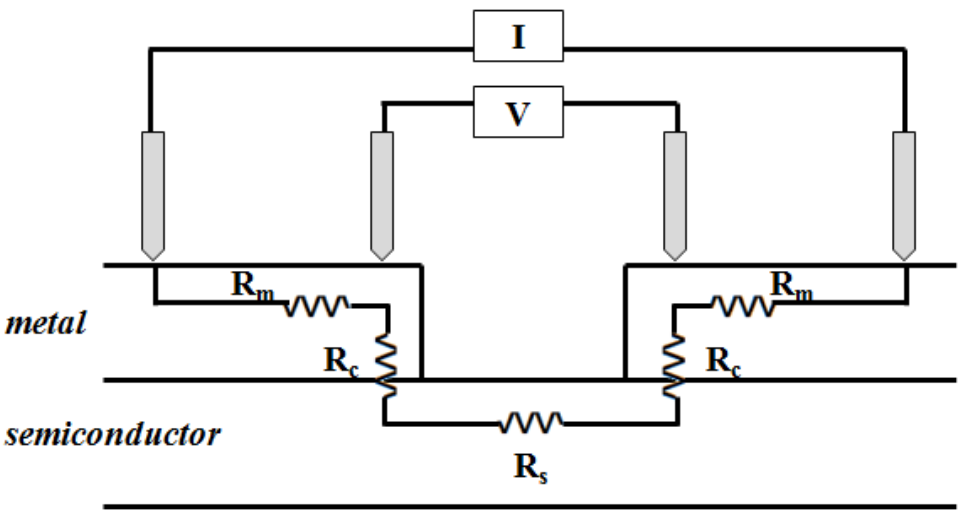


Fig. 3. 7. Schematic picture of four point probe measurement.

In addition, the big difference in width between the contact and mesa causes errors in the ρ_c calculation as the current spreads [10] when it flows in the semiconductor as shown in Fig. 3. 8. This is because of the error in design of mesa and contact patterns. Thus, the TLM structures were redesigned in order to exclude any component of metal resistance as well as to avoid current distribution [10].

For the new structure, shown in Fig. 3. 9, the potential drop is measured at the contact edges to minimize the metal resistance as mentioned above with Fig. 3. 7. In addition, we designed the mesa to have a width just the same as the contact width in order to prevent current spreading. To minimize the difference in width between the contact and mesa, the mesa widths were designed with three different widths; one the same as the contact width and the others in a range of ± 2 μm to the contact width. This is because the mesa width may not be developed as designed due to a limited resolution during lithography. This increases the likelihood of getting a mesa width fitting the contact width perfectly. Fig. 3. 10 shows the entire structures and the contact widths are set to be 10, 20 and 30 μm while L_{gap} increases from 1 to 30 μm.

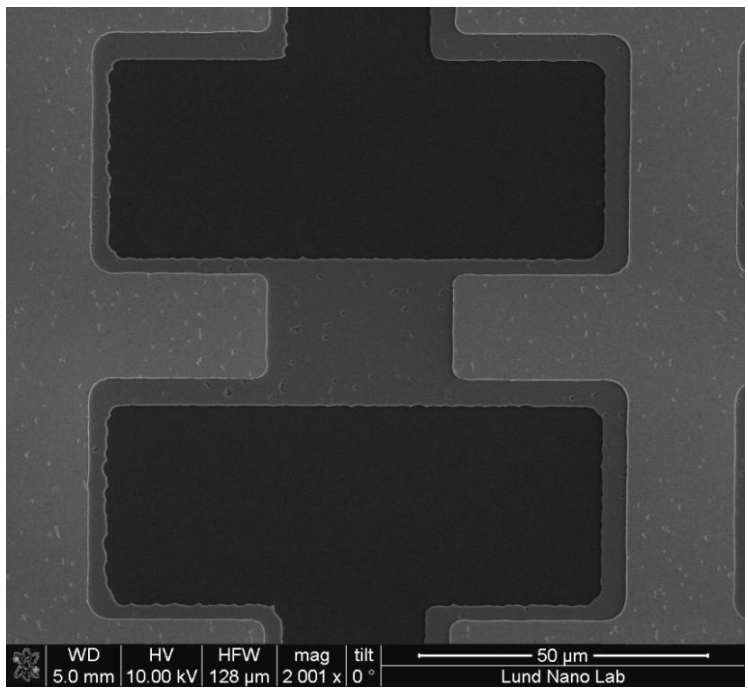
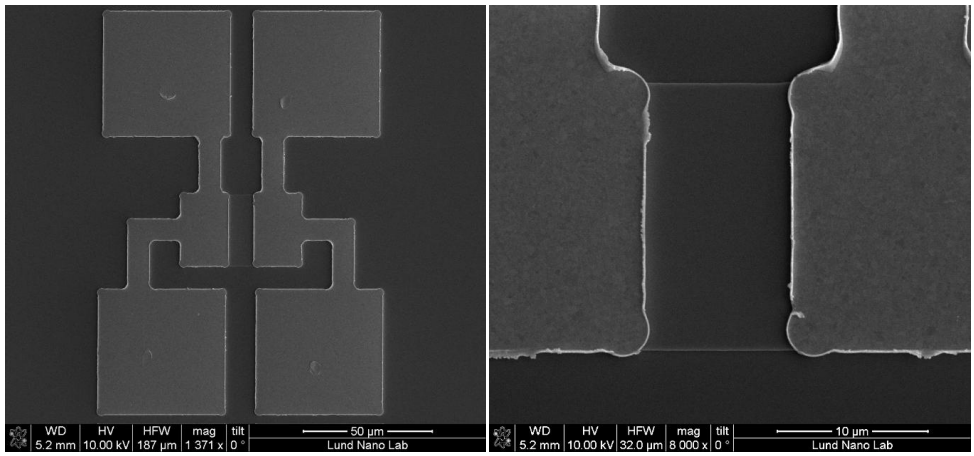


Fig. 3. 8. SEM image which shows the metal contact and the mesa of the first test TLM structure.



(a) (b)

Fig. 3. 9. SEM image of the re-designed TLM structures, showing (a) one structure and (b) zoom-in gap area used in this work.

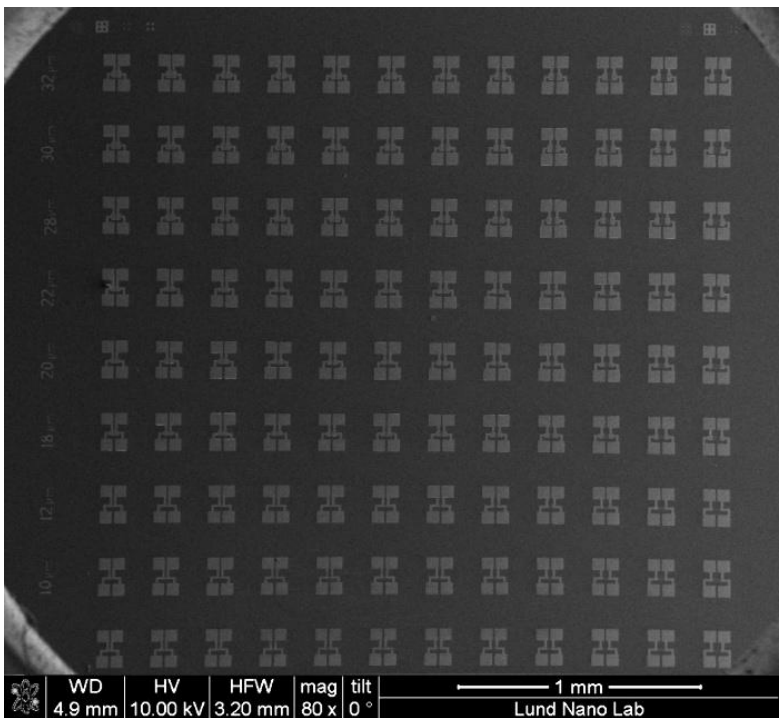


Fig. 3. 10. SEM image of the entire re-designed TLM structures.

CHAPTER 4

4 Results and discussion

In this section, the contact resistivities obtained for nickel (Ni) and titanium (Ti) contacts made to the unintentionally doped n-InAs and n^+-$In_{0.63}Ga_{0.37}As$ are discussed.

4.1 The InAs substrate

We will first consider the results for Ni contacts, and then move on to the Ti contacts to n-InAs.

4.1.1 Ni contacts

4.1.1.1 Previous mask

As in the first fabrication of TLM structures, we extracted the contact resistivity using the previous mask. Ni contacts were deposited by thermal evaporation on 50 nm n-InAs layers grown on Si wafers using a 250 nm highly doped InAs buffer. Fig. 4. 1 shows the contact resistivity as a function of annealing temperatures from 100 to 350 ℃ with 1 min of annealing time. One can also find the specific resistivity values as well as the sheet resistance and transfer length in table 4. 1. When looking at Fig. 4. 1, ρ_c has the lowest value at 200 ℃ and starts to degrade when the temperature rises towards 300 ℃. However, it drops again at 350 ℃ which makes it hard to trust the data, as we expect to see that once ρ_c attains its lowest value at a certain temperature, it increases as the temperature rises. In addition, the final structure as shown in Fig. 3. 8 can induce errors when extracting ρ_c due to the current spreading. Furthermore, since R_s indicates the sheet resistance of the semiconductor layer, it should provide a constant value, but it shows the changing sheet resistances. That is inevitable due to the design problem of the mesa structures even though one tries to align the contact and mesa structures perfectly. However, all the extracted L_T, shown in table 4. 1, are larger than twice the InAs thickness (300 nm). Thus the

one-dimensional current flow approximation used for resistance analysis is valid [46].

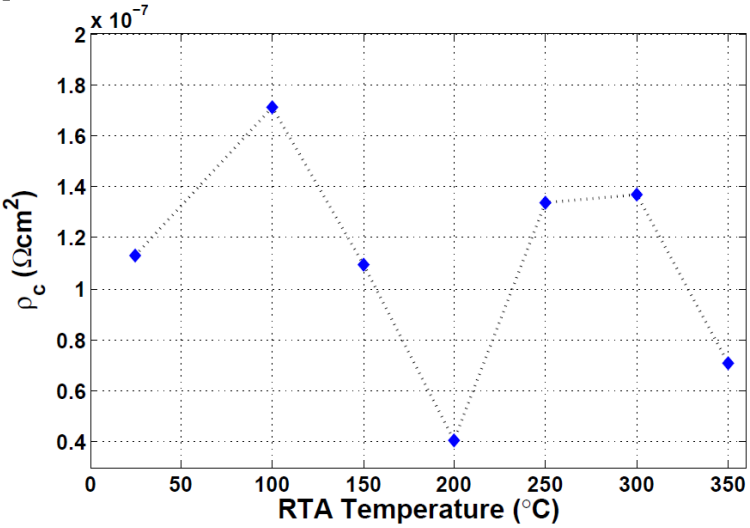


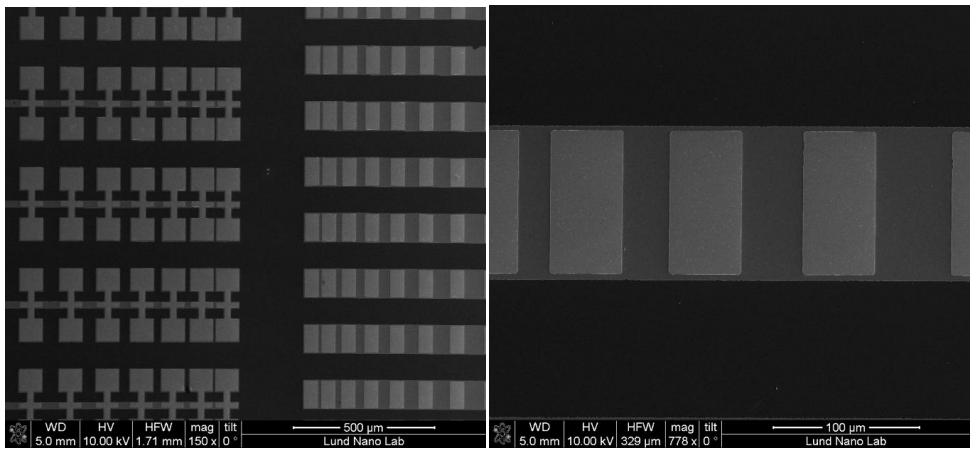
Fig. 4. 1. The evaporated Ni contact resistivity as a function of RTA temperature from the TLM structures of the previous mask.

TABLE 4. 1. THE SHEET RESISTANCE R_S, CONTACT RESISTIVITY AND TRANSFER LENGTH L_T AT VARIOUS ANNEALING TEMPERATURES.

Temp. (℃)	R_s (Ω)	ρ_c (Ωcm^2)	L_T (m)
25	10.14	$1.13 \cdot 10^{-7}$	$1.06 \cdot 10^{-6}$
100	9.39	$1.71 \cdot 10^{-7}$	$1.35 \cdot 10^{-6}$
150	9.42	$1.10 \cdot 10^{-7}$	$1.08 \cdot 10^{-6}$
200	10.20	$4.04 \cdot 10^{-8}$	$6.29 \cdot 10^{-7}$
250	9.60	$1.34 \cdot 10^{-7}$	$1.30 \cdot 10^{-6}$
300	8.92	$1.37 \cdot 10^{-7}$	$1.23 \cdot 10^{-6}$
350	9.70	$7.07 \cdot 10^{-8}$	$8.46 \cdot 10^{-7}$

In order to determine if the reason why the data do not seem trustworthy can be due to the mask, we decided to extract ρ_c with another structure which was also on the previous mask as shown in Fig. 4. 2 (a) on the right side referred as a pattern 2. The structures of pattern 2 have the same gap spacing as pattern 1 which is on the left side, but the width is 103 μm, as shown in Fig. 4. 2 (b), which is much bigger than the 15 μm of pattern 1.

Fig. 4. 3 shows ρ_c extracted from both patterns on the previous mask. It is still hard to find the temperature dependence of ρ_c for pattern 2 as the pattern 1. Since the gap width is way too wide, we do not expect to get a better ρ_c from pattern 2, but it gives a lower ρ_c at every annealing temperature which may be due to less current spreading. In other words, new structures on which the mesa widths will fit the contact widths were needed to avoid errors due to current spreading.



(a) (b)

Fig. 4. 2. (a) An overview of the entire structures on the previous mask. (b) The zoomed-in structures of pattern 2.

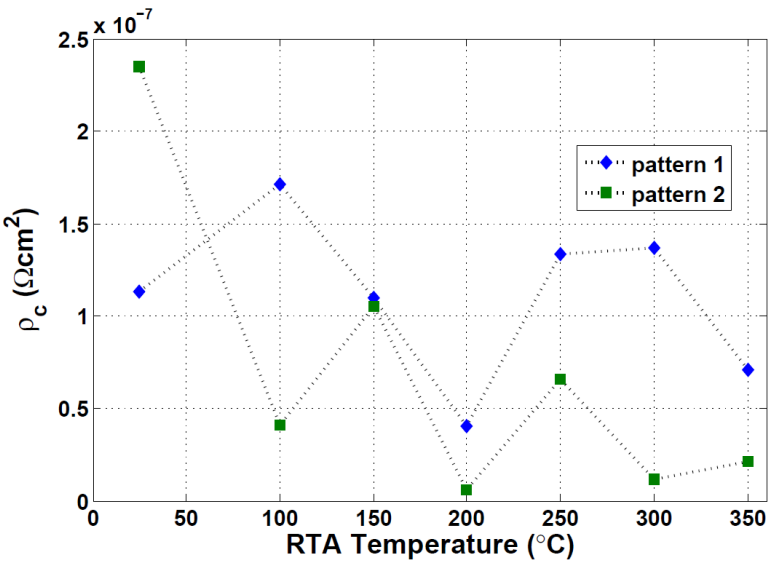


Fig. 4. 3. The comparison of ρ_c between pattern 1 and 2.

4.1.1.2 Surface preparation

Before making the new mask, we investigated the effect of different surface preparations before the metal deposition. Since the contact resistivity can deteriorate in the presence of native oxide, it is crucial that the native oxide can be removed effectively from the surface before metal deposition. As the first attempt, we removed the native oxide using oxygen plasma ashing for 15 s and then treated the sample with 1:1 HCl:DI water for 30 s. As an alternative to oxygen plasma ashing, we chose UV-ozone oxidation for 1 min and oxide removal with 1:1 HCl:DI water for 30 s. Fig. 4. 4 compares ρ_c between oxygen plasma and UV-ozone treatment before contact deposition. The UV-ozone oxidation improves the contact resistivity all over the annealing temperatures by $7.0 \cdot 10^{-8}$ Ωcm^2 at maximum and $9.0 \cdot 10^{-10}$ Ωcm^2 at minimum. Thus we decided to utilize UV-ozone oxidation and oxide removal with 1:1 HCl:DI water as the surface preparation. Vibhor et al. reported the effect of UV-ozone oxidation. With UV-ozone and diluted HCl, ρ_c of TiW contacts to n-InGaAs decreased by $1.2 \cdot 10^{-8}$ Ωcm^2 compared to oxide removal with concentrated NH_4OH etch without UV-ozone [20].

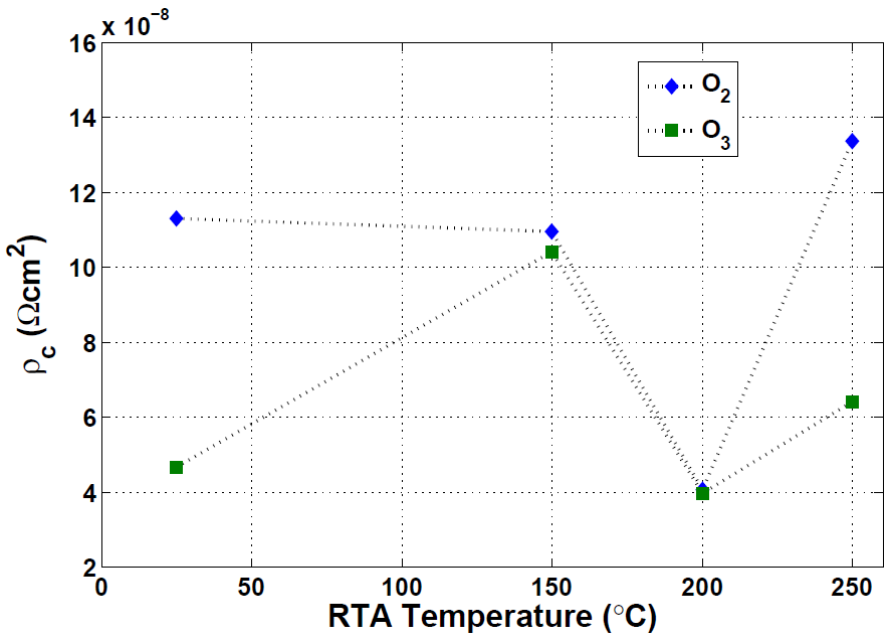
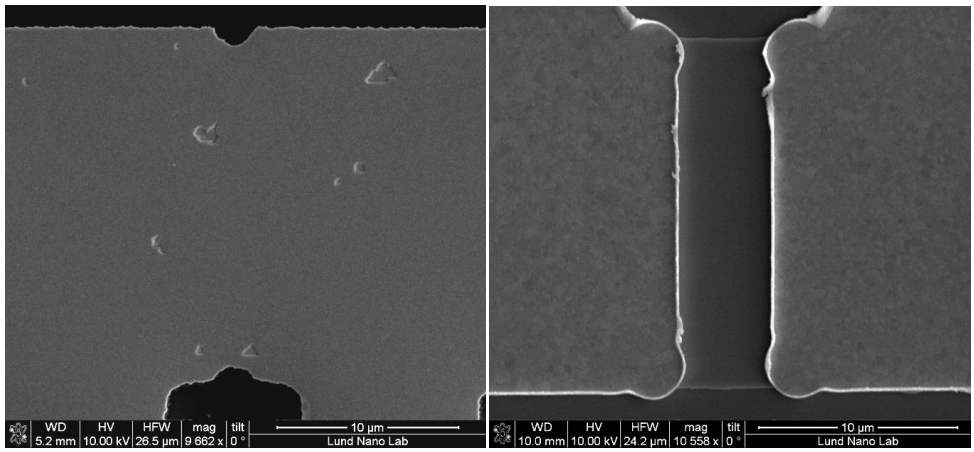


Fig. 4. 4. Comparison of the contact resistivity between O_2 and O_3 treatment before the metal deposition by thermal evaporation.

Since UV-ozone treatment gives a better surface condition, we also tried to find another method for surface oxide removal, instead of 1:1 HCl:DI water, which could improve the contact resistivity even more with UV-ozone. We used two different ways; the first was dipping in a beaker with 10 % $(NH_4)_2S$ for 10 min and rinsing with water for 15 s, and the second was an immersion in ammonium hydroxide (NH_4OH, 20.5 normality) for 15 s and drying with N_2 gas. However, both methods destroyed the patterned resist completely, so it was impossible to proceed to the next step. These two methods are incompatible with the lift-off process, so we should investigate the effect of these methods when studying sputtered metal contacts. Thus we conclude that when depositing the metal contacts by thermal evaporation, the surface should be treated with UV-ozone oxidation and removal of oxides with 1:1 HCl:DI water to obtain a good surface condition.

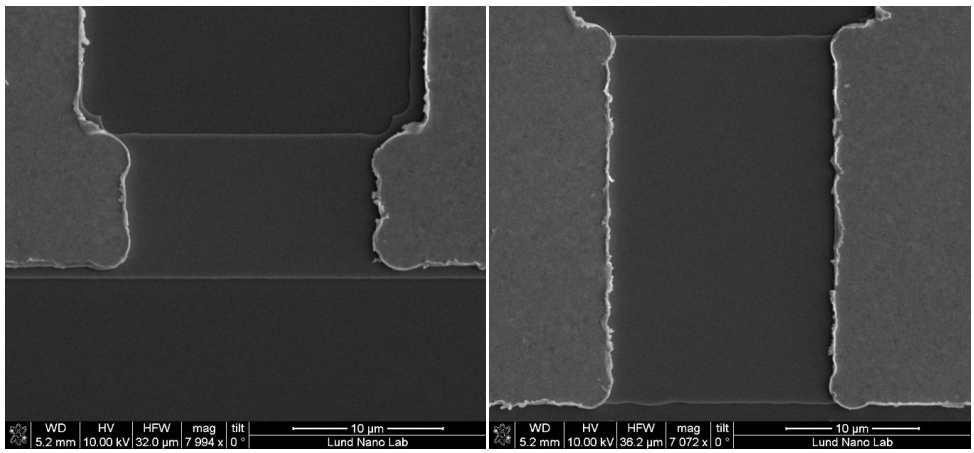
4.1.1.3 Re-designed mask

Fig. 3. 10 shows the newly designed mask and the zoomed-in structures can be seen in Fig. 3. 9. As mentioned in the method section, there are three different widths; 10, 20 and 30 μm, and twelve gaps; 1, 2, 3, 4, 5, 6, 8, 10, 15, 20, 25 and 30 μm. As shown in Fig. 4. 5, the structure with the 1 and/or 2 μm gap distance is not often patterned properly due to the limited resolution of UV lithography. Although it was successfully developed, it was usually about 1 or 2 μm wider than it should have been, but we still had enough narrow gaps which could contribute to a higher accuracy when extracting the contact resistivity. In addition, when extracting ρ_c from three different widths, we found that ρ_c from the wider widths of both 20 and 30 μm had values close to each other. On the other hand, ρ_c from the narrower widths of 10 μm tended to have the values which were rather far from them. This is because the structures with the narrower widths have much more irregular shapes as shown in Fig. 4. 6, so it makes ρ_c extraction less reliable. Thus we only measured the resistance on the structures with the widths of 20 and 30 μm and averaged the values from them.



(a) (b)

Fig. 4. 5. The TLM structures from the re-designed mask showing the gap of (a) 1 µm and (b) 5 µm with the width of 30 µm.



(a) (b)

Fig. 4. 6. Comparison between the widths of between (a) 10 µm and (b) 30 µm with the gap spacing of 15 µm.

The averaged ρ_c of the evaporated Ni contacts fabricated by the re-designed mask are shown in Fig. 4. 7. As one can see in table 4. 2, the contact resistivity has a lowest value of $1.92 \cdot 10^{-8}$ Ωcm^2 at 150 ℃ which is lower than that from the previous mask, $4.04 \cdot 10^{-8}$ Ωcm^2 at 200 ℃. However, the difference between the data is about an order of magnitude which was caused by a gap measurement error when using the optical microscope.

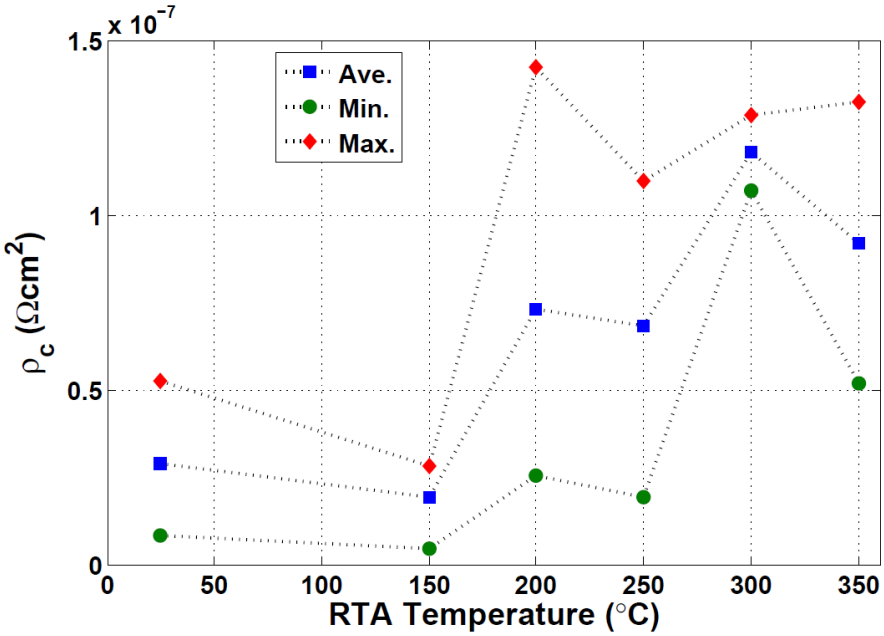


Fig. 4. 7. The contact resistivity of Ni contacts as a function of RTA temperature from the TLM structures of the re-designed mask.

TABLE 4. 2. THE SHEET RESISTANCE AND AVERAGE CONTACT RESISTIVITY OF NI CONTACTS AS WELL AS ITS MINIMUM AND MAXIMUM VALUES FROM THE RE-DESIGNED MASK.

Temp. (℃)	R_s (Ω)	ρ_c (Ωcm^2)	Min	Max
25	7.33	$2.91 \cdot 10^{-8}$	$8.32 \cdot 10^{-9}$	$5.29 \cdot 10^{-8}$
150	7.19	$1.92 \cdot 10^{-8}$	$4.78 \cdot 10^{-9}$	$2.82 \cdot 10^{-8}$
200	7.95	$7.34 \cdot 10^{-8}$	$2.54 \cdot 10^{-8}$	$1.42 \cdot 10^{-7}$
250	8.03	$6.85 \cdot 10^{-8}$	$1.94 \cdot 10^{-8}$	$1.10 \cdot 10^{-7}$
350	9.00	$9.23 \cdot 10^{-8}$	$5.19 \cdot 10^{-8}$	$1.33 \cdot 10^{-7}$

Thus, we recalculated all data with another method which measured gap distance on the SEM image with a Matlab program as explained in Fig. 3. 4. Fig. 4. 8 and table 4. 3 show the recalculated data. The recalculated lowest ρ_c of evaporated Ni/Pd/Au contacts is $3.22 \cdot 10^{-8}$ Ωcm^2 which is higher than before, but this value is much more trustworthy since the contact resistivity measured from two different widths are almost identical. In addition, Fig. 4. 9 shows TLM pattern resistance as a function of contact separation for Ni contacts to unintentionally doped n-InAs annealed at 150 ℃ and from a

linear regression to the data, the extracted L_T (~ $1.2 \cdot 10^{-6}$ m) is far larger than twice of InAs thickness (300 nm), so the one-dimensional current flow approximation used to resistance analysis is valid [46]. Therefore, we conclude that a 150 ℃ annealing for 1 min decreases the contact resistivity of Ni/Pd/Au contacts from $4.33 \cdot 10^{-8}$ to $3.22 \cdot 10^{-8}$ Ωcm^2 and the best contact resistivity of evaporated Ni contact on unintentionally doped n-InAs is $3.22 \cdot 10^{-8}$ Ωcm^2 at 150 ℃.

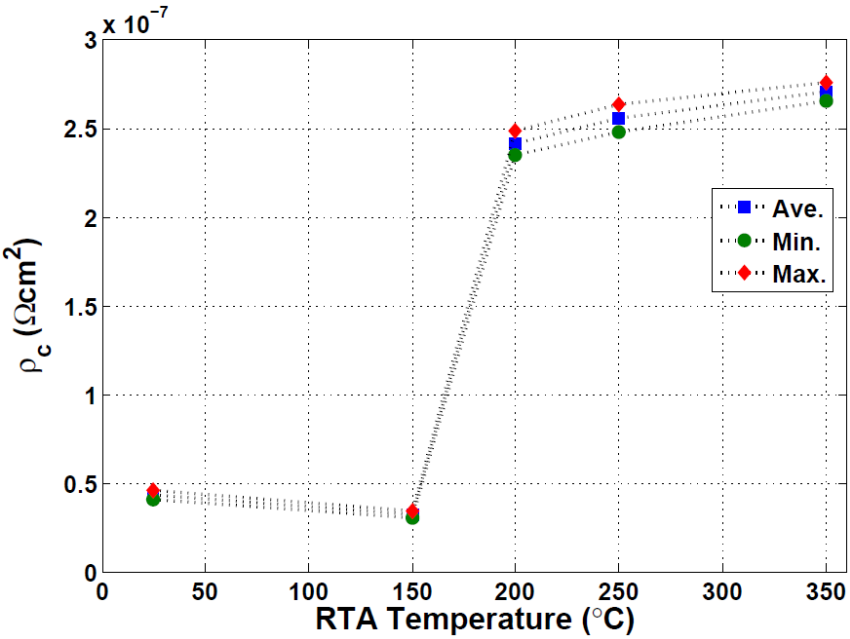


Fig. 4. 8. The contact resistivity of Ni contacts as a function of RTA temperature from the TLM structures of the re-designed mask with a SEM gap measurement.

TABLE 4. 3. THE SHEET RESISTANCE AND AVERAGE CONTACT RESISTIVITY OF NI CONTACTS AS WELL AS ITS MINIMUM AND MAXIMUM VALUES FROM THE RE-DESIGNED MASK WITH THE MEASUREMENT OF GAP DISTANCES WITH THE MATLAB PROGRAM.

Temp. (℃)	R_s (Ω)	ρ_c (Ωcm^2)	Min	Max
25	7.52	$4.33 \cdot 10^{-8}$	$4.04 \cdot 10^{-8}$	$4.61 \cdot 10^{-8}$
150	7.38	$3.22 \cdot 10^{-8}$	$3.05 \cdot 10^{-8}$	$3.44 \cdot 10^{-8}$
200	7.54	$2.42 \cdot 10^{-7}$	$2.35 \cdot 10^{-7}$	$2.49 \cdot 10^{-7}$
250	7.75	$2.56 \cdot 10^{-7}$	$2.48 \cdot 10^{-7}$	$2.64 \cdot 10^{-7}$
350	7.91	$2.71 \cdot 10^{-7}$	$2.66 \cdot 10^{-7}$	$2.76 \cdot 10^{-7}$

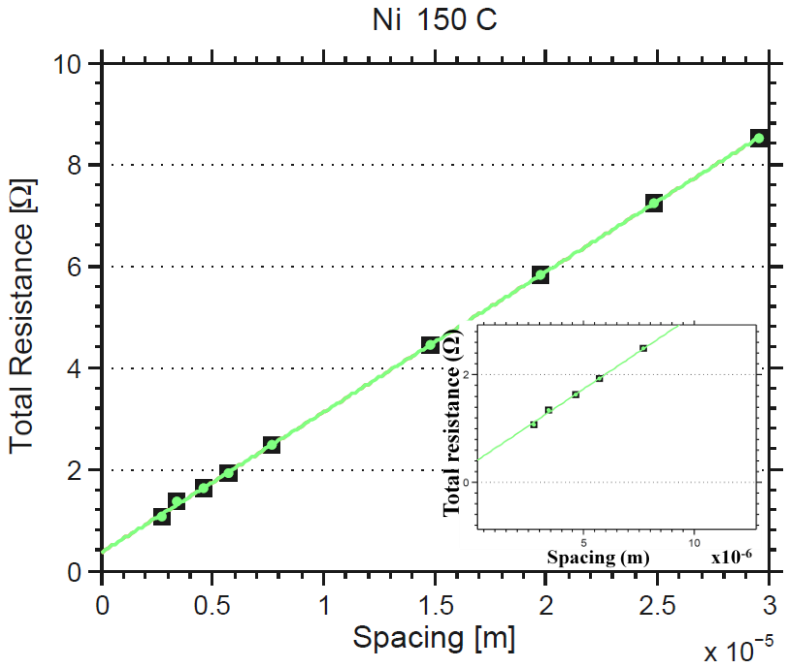


Fig. 4. 9. TLM pattern resistance as a function of contact separation (3-30 μm) for the Ni/Pd/Au contacts to InAs annealed at 150 ℃ with the linear regression of the data. The TLM pattern width was 30 μm. The inset shows the zoomed-in of the smallest spacing.

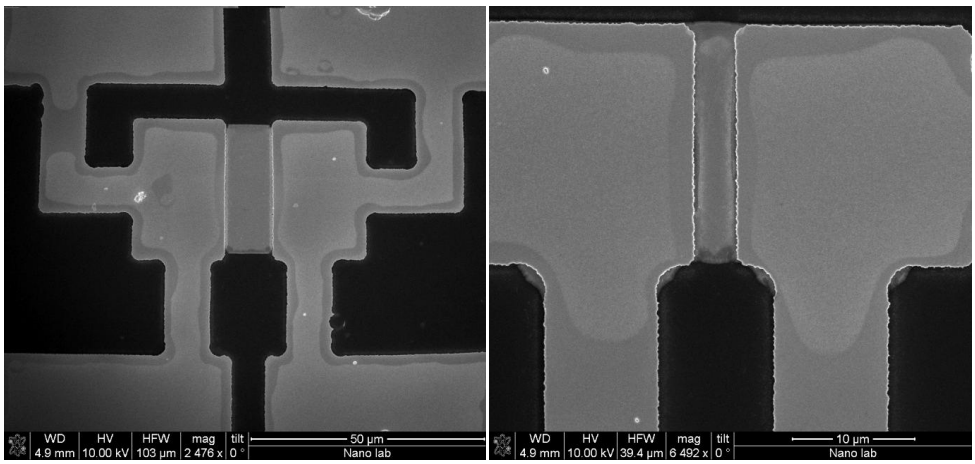
4.1.1.4 Sputtering

As another method for depositing the metal contacts, we sputtered Ni on the InAs substrate. 6 nm of Ni was etched H_2SO_4:HNO_3:CH_3COOH:DI water = 1:2.5:2.5:15 for 3 min with an etch rate of 0.33 nm/s. In order to use this Ni etchant, we had to determine the etch rate first since we had no previous information about that. 80 nm of Ni was blanket deposited on the InAs substrate and completely etched away after 10 min with the Ni etchant which yielded an etch rate of 0.13 nm/s. Thus, in order to etch 6 nm of Ni, the Ni should be etched for 46 s at least. In addition, the surface of the InAs substrate was clean after 10 min of etching, which proved that it did not etch the substrate very aggressively.

For the actual etching of 6 nm of Ni, we decided to etch longer than 46 s since we wanted to make sure there would be no Ni left. In addition, since the Ni etchant does not etch the InAs substrate very quickly, we could safely etch longer. Thus, we etched the Ni layer for 3 mi*n* and while etching, we constantly checked with the optical microscope if the Ni had been

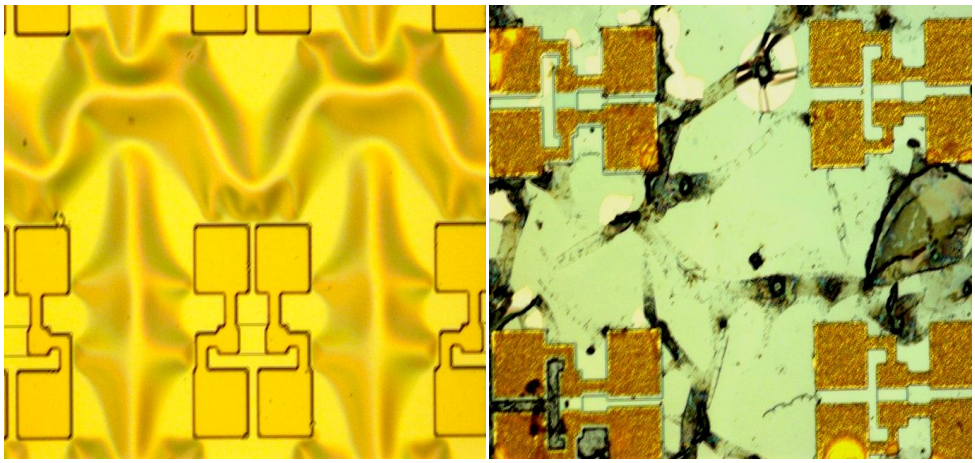
etched properly and the surface was clean. After that, the isolation processing followed.

Fig. 4. 10 shows the SEM images of the final sample. The sample has irregular shapes along the edges of the structures, shown in Fig. 4. 10 (a), and also at around the gap area; it is obvious that the thickness of the InAs is not uniform, as shown in Fig. 4. 10 (b). First, we concluded that the mesa isolation step did not work very well. This is because the InAs substrate might be etched somewhat during the Ni etching, so the ordinary mesa etching caused over-etching. Therefore we decided to do the isolation process first and sputtered the metal layers afterwards. Apart from the gap problem, we also decided to investigate the cross-section of the structures where the irregular shapes appeared using focused ion beam (FIB) as well as SEM.



(a) (b)

Fig. 4. 10. (a) SEM image of the sputtered Ni contacts on a sample without annealing. (b) Zoomed-in image of the gap area.



(a) (b)

Fig. 4. 11. (a) Optical image of the sample after the Ni/W/Au sputtering. (b) The surface after the Ni layer was etched away.

First of all, the mesa structures were defined and then the metal layers were sputtered. As shown in Fig. 4. 11 (a), the metal layers look fine around the TLM structure area, but they were crumbled on the Si area where the InAs was etched away. As a dummy sample, we also evaporated Ni/W/Au on the bare Si wafer where the same problem arose. Hence, we can conclude Ni has a bad adhesion to the Si surface and the sputtered metal layers only adhere around the TLM structures. Since the structures looked reasonable clean, we tried to etch the metal layers and the sample after Ni etching, which was the final etching step; the result is shown in Fig. 4. 11 (b). Since the height of each metal layer on the Si area was not constant, the metal layers were not etched uniformly. Especially, W and Ni were very hard to remove, and shows up as black clogs in Fig. 4. 11 (b). W was dry etched several extra times in order to make sure there was no W residue before Ni etching, but the black clogs were impossible to remove even after etching for twice as long in the Ni etchant. We conjectured that the black clogs were Ni and W that got tangled with each other. It could happen during developing in MF 319 since the non-uniform metal layers started to appear during the development of the resist for the first time, which was due to strain releasing in liquid. Thus, the Ni etchant could not etch the Ni/W clogs and there were a lot of Ni/W clogs attached to the TLM structures making further resistance measurement meaningless. Also, we found that defining the mesa structures first cannot be a solution for the non-uniform gap area.

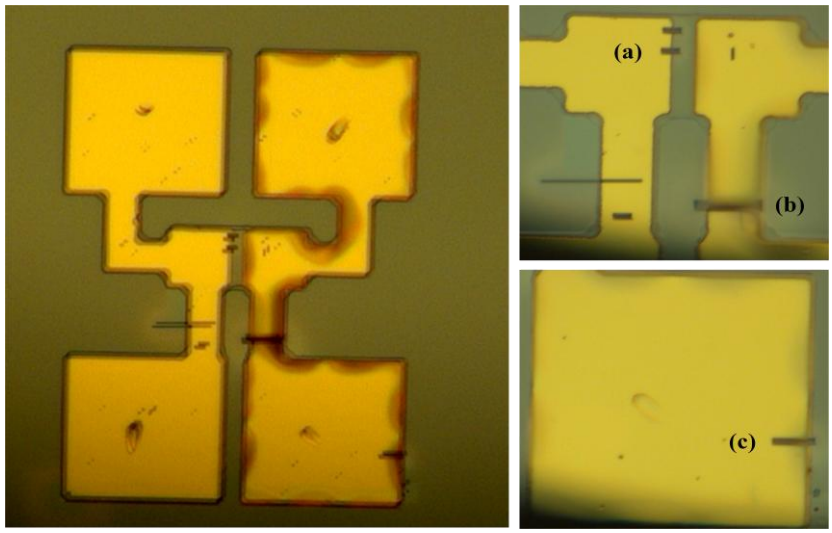


Fig. 4. 12. The optical microscopy image of the sample on which the FIB milling was done.

At the same time, we also investigated the cross-section of the TLM structures in order to, by simultaneous ion beam cross-sectioning and electron beam viewing, using FEI Nova NanoLab 600 [44]. Fig. 4. 12 presents an optical microscopy image of the sample on which FIB milling was done. The right part of the structures only shows the irregular shapes along the edges unlike the left part, so we milled the left (marked (a)) and right parts (marked (b) and (c)) and compared them.

Fig. 4. 13 shows the position marked (a) in Fig. 4. 12. The thickness of the InAs substrate in the gap area looks uniform unlike what we discussed above, so the mesa processing actually did work well and the Ni etchant did not etch the InAs substrate. But some W residues were found near the Ni contact. In addition, there is a slight gap between the metal layers and the InAs substrate. It was probably caused during the Ni etching which means that since the Ni etching time was longer than needed, the Ni was over etched.

It is more obvious that the Ni was over etched when looking at Fig. 4. 14. Since it was over etched, the etchant went under the Ni layer and etched Ni unintentionally, and the metal layers were lifted up when milling by focused ion beam. Thus, on the right part of the structures, marked (b) and (c) as shown in Fig. 4. 12 and 14, the irregular shapes along the edges turn out to be because the Ni was over etched.

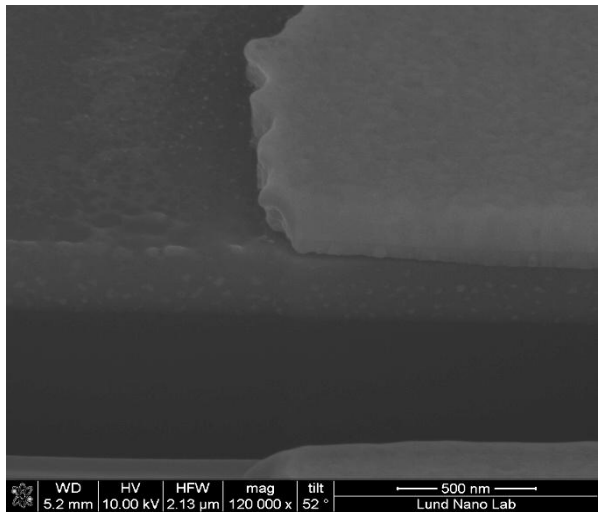
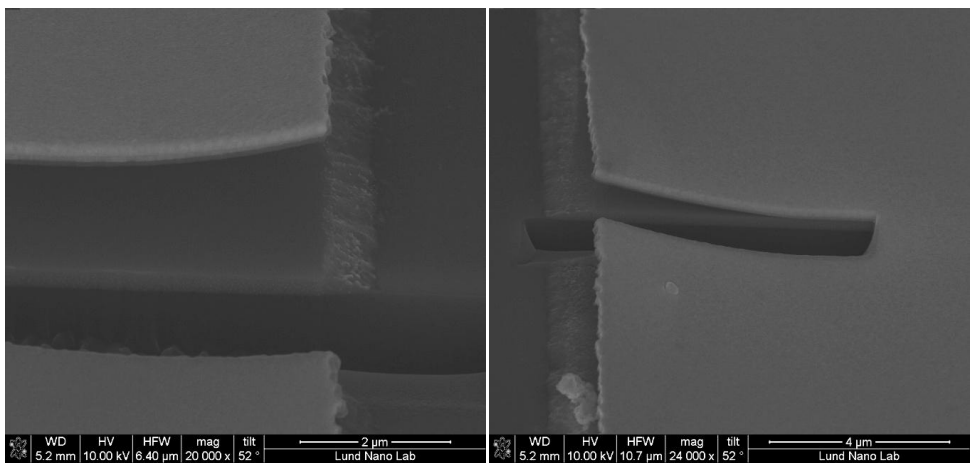


Fig. 4. 13. SEM image of (a) part of Fig. 4. 12.

We do not have a measurement result on the sputtered Ni contacts due to the lack of time, but if one reduces the Ni etching time to around 1 min or even less, we expect that one can fabricate the TLM structures with the sputtered Ni contacts without the Ni over-etching. Also, if Ni contacts by sputtering can be developed later, it would be interesting to see the effect of *in situ* Ar^+ sputter cleaning since *in situ* surface treatment prevents surface oxidation without exposing the samples to air. In addition, the effect of 10 % $(NH_4)_2S$ as well as NH_4OH can be studied further.



(a) (b)

Fig. 4. 14. (a) SEM image of the area marked (b) in Fig. 4. 12. (b) The position marked (c) in Fig. 4. 12.

4.1.1.5 Ti contacts

We have developed Ti contacts on unintentionally doped n-InAs by sputtering since a recipe for etching Ti has been used commonly using 1:10 HF:DI water. Fig. 4. 15 shows the contact resistivity of Ti contacts as a function of annealing temperature for InAs samples. Also the specific values of R_s and ρ_c are found in table 4. 4. ρ_c is almost constant showing a small degradation up to 250 ℃, and it exhibits a decrease from $5.95 \cdot 10^{-8}$ to $4.02 \cdot 10^{-8}$ Ωcm^2 at 300 ℃. Thus we do not observe a degradation of Ti contacts up to 300 ℃ due to the intermixing of In and Au as explained in the theory section. TLM pattern resistance as a function of contact spacing for the Ti contacts to InAs annealed at 300 ℃ is shown in Fig. 4. 16, and the extracted L_T ($\sim 1.3 \cdot 10^{-6}$ m) is larger than twice of InAs thickness. Thus the one-dimensional current flow approximation is appropriate [46].

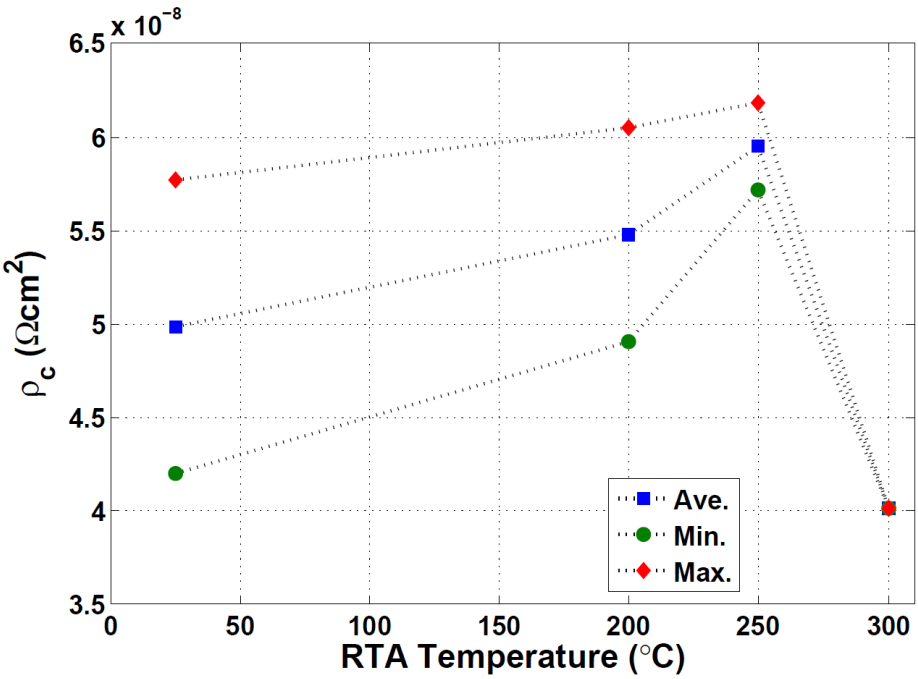


Fig. 4. 15. The contact resistivity of sputtered Ti contacts to InAs as a function of RTA temperature.

TABLE 4. 4. THE SHEET RESISTANCE AND AVERAGE CONTACT RESISTIVITY OF TI CONTACTS TO INAS AS WELL AS ITS MINIMUM AND MAXIMUM VALUES.

Temp. (℃)	R_s **(Ω)**	ρ_c **(Ωcm^2)**	**Min**	**Max**
25	8.38	$4.98 \cdot 10^{-8}$	$4.20 \cdot 10^{-8}$	$5.77 \cdot 10^{-8}$
200	8.44	$5.48 \cdot 10^{-8}$	$4.91 \cdot 10^{-8}$	$6.05 \cdot 10^{-8}$
250	8.01	$5.95 \cdot 10^{-8}$	$5.72 \cdot 10^{-8}$	$6.18 \cdot 10^{-8}$
300	8.43	$4.02 \cdot 10^{-8}$	$4.02 \cdot 10^{-8}$	$4.02 \cdot 10^{-8}$

Stareev et al. reported a ρ_c of $1.7 \cdot 10^{-8}$ Ωcm^2 of Ti/Pt/Au contact metal to n-InAs using *in situ* Ar^+ sputter cleaning prior to metal deposition [21]. It exhibited lower ρ_c than we obtained ($3.22 \cdot 10^{-8}$ Ωcm^2) which may be attributed to *in situ* Ar^+ cleaning as well as highly doped InAs. Hence we expect that *in situ* Ar^+ sputter cleaning prior to metal deposition would improve the contact resistivity in our case. In addition, Shiraishi et al. obtained $\rho_c = 2 \cdot 10^{-8}$ Ωcm^2 for Ti contacts to n-InAs with H_3PO_4 solution cleaning prior to metal deposition by e-beam evaporation [39]. It also showed lower ρ_c than we observed which appeared to be due to a high active carrier concentration ($2 \cdot 10^{19}$ cm^{-3}) and the different oxide removal procedure.

To conclude, the lowest ρ_c of Ti contacts deposited by sputtering is somewhat higher than that of Ni contacts ($3.22 \cdot 10^{-8}$ Ωcm^2) by thermal evaporation, but they are comparable.

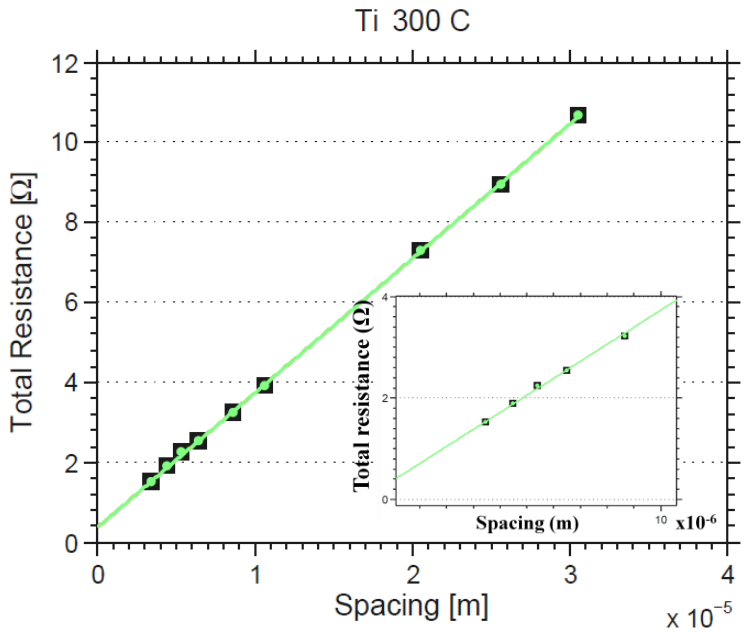


Fig. 4. 16. : TLM pattern resistance as a function of contact separation (3-30 µm) for the Ti/W/Au contacts on InAs annealed at 300 ℃ with the linear regression to the data. The TLM pattern width was 30 µm. The inset shows the zoomed-in of the small separations.

4.2 The InGaAs substrate

This section deals with Ni and Ti contacts on the InGaAs substrates.

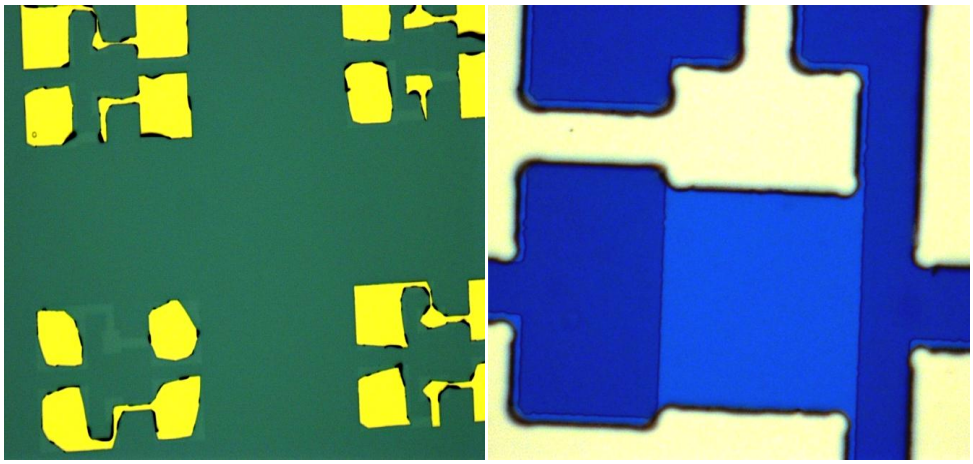
4.2.1 Ni contacts

In this section, we will discuss the contact resistivity of the Ni contacts extracted from the TLM structures fabricated on the InGaAs substrate which consisted of a 20 nm doped $In_{0.63}Ga_{0.37}As$ layer grown on an InP wafer with a 120 nm $In_{0.53}Ga_{0.47}As$ buffer. In addition, three different InGaAs substrates with three different doping concentrations of Sn were used. Table 4. 5 shows the flow rate for Sn used when the $In_{0.63}Ga_{0.37}As$ layer was grown on the InP, and its correspondent carrier concentrations (n). Note that a Sn flow of 220 sccm gives the highest n and the carrier concentration decreases as the Sn flow increases to 300 sccm. This is because if the doping level becomes too high, the Sn-atoms start to form cluster instead of being discrete dopant atoms, which gives rise to a lower doping level even if the amount of Sn in the InGaAs is higher.

TABLE 4. 5. THE FLOW RATE OF SN AND ITS CORRESPONDENT CARRIER CONCENTRATION.

Sn flow rate	**Carrier concentration *n* (cm^{-3})**
100 sccm	$2 \cdot 10^{19}$
220 sccm	$5 \cdot 10^{19}$
300 sccm	$3 \cdot 10^{19}$

We evaporated Ni/Pd/Au on the InGaAs substrate the same way as done for the InAs substrate. However, we faced a new problem during the lift-off process. As shown in Fig. 4. 17 (a), the Au layer, presented in yellow, is removed partly. It also looks like Ni/Pd layers still remain on the surface since the structures are shown with the traces, presented in grey, of the metal layers. It happened several times on the InGaAs substrate with any doping concentration. It can happen if the thickness of the LOR layer is comparable to that of the metal layers (Ni/Pd/Au); the Au layer, as the top layer, can be a continuous film, so it can be removed with the bi-layer of S1813 and LOR 3A at the same time. We are still not sure why the thickness of LOR 3A became thinner on the InGaAs substrate even though all parameters (spin speed, spin time etc) were the same as for the InAs substrate. We changed the bottom layer from LOR 3A to LOR 10A which forms a thicker layer with faster developing rate. LOR 10 A with spin speed of 6000 rpm gives a thickness of 10000 Å approximately, compared to LOR 3A which forms 4000 Å at spin speed of 3000 rpm [47]. As shown in Fig. 4. 17 (b), the TLM structures are defined well and without the problem during the lift-off process when using LOR 10A instead of LOR 3A since LOR 10A ensures discontinuous metal film deposition. Thus, we had used LOR 10A as a bottom of the bi-layer when developing Ni and Ti contacts through lift-off on the InGaAs substrates.



(a) (b)

Fig. 4. 17. (a) Optical microscopy image of the sample after lift-off in the case of using LOR 3A. (b) The sample with LOR 10A.

After mesa isolation, the samples were annealed from 250 to 350 ℃ for 1 min as a Ni-InGaAs metallic alloy is found at a low temperature of 250 ℃ with RTA for 1 min as reported in [2][5]. Afterwards, a four-probe measurement was done and the contact resistivity of the evaporated Ni contacts on the InGaAs substrate with two different doping concentrations is shown in Fig. 4. 18. Also one can see the specific values of R_s and ρ_c measured on 220 sccm and 100 sccm of Sn doping in table 4. 6 and 4. 7, respectively. The lowest ρ_c of the evaporated Ni contacts on the InGaAs substrate with 220 sccm of Sn is $8.28 \cdot 10^{-8}$ Ωcm^2 at 300 ℃ and ρ_c increases as temperature goes up. On the other hand, the lowest ρ_c from the InGaAs with 100 sccm of Sn is $1.16 \cdot 10^{-7}$ Ωcm^2 at 250 ℃ and ρ_c also increases. Since higher doping decreases the contact barrier thickness which in turn increases tunneling probability as well as provides a large number of conduction electrons, the Ni contacts on InGaAs with a higher doping concentration gives a lower ρ_c. Thus a high doping concentration is needed to minimize ρ_c. Note that since there is little deviation between minimum and maximum values, we can say that the averaged ρ_c is reasonably accurate. Furthermore, the extracted L_T ($\sim 1.4 \cdot 10^{-6}$ m) is far larger than twice the InGaAs thickness (120 nm), so the one-dimensional current flow approximation used to resistance analysis is valid [46].

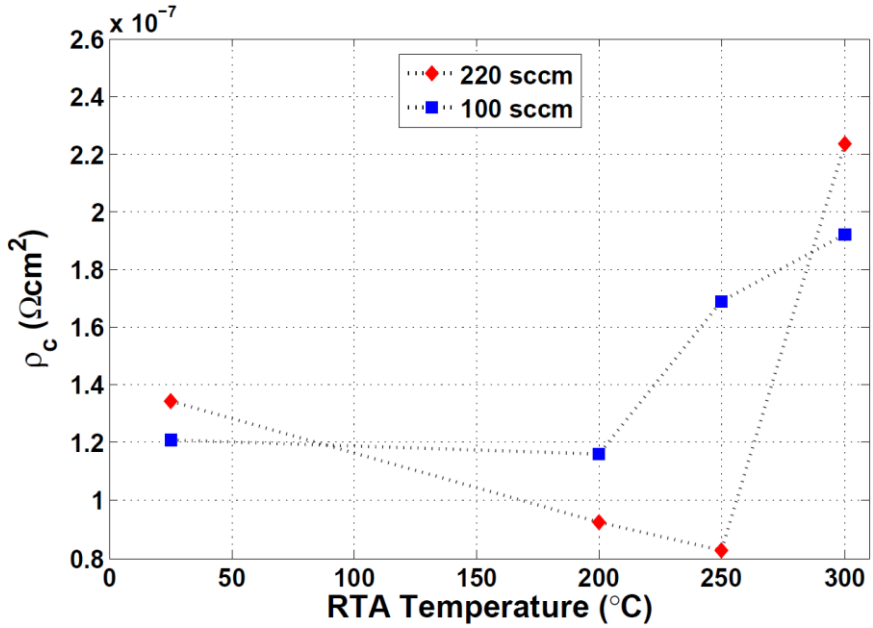


Fig. 4. 18. The contact resistivity of evaporated Ni contacts as a function of RTA temperature from the InGaAs substrates with two different doping concentrations.

TABLE 4. 6. THE SHEET RESISTANCE AND AVERAGE CONTACT RESISTIVITY OF NI CONTACTS AS WELL AS ITS MINIMUM AND MAXIMUM VALUES MEASURED ON THE INGAAS SUBSTRATE WITH 220 SCCM OF SN DOPING.

Temp. (℃)	R_s (Ω)	ρ_c (Ωcm^2)	Min	Max
25	16.02	$1.35 \cdot 10^{-7}$	$1.04 \cdot 10^{-7}$	$1.65 \cdot 10^{-7}$
250	16.11	$9.23 \cdot 10^{-8}$	$9.23 \cdot 10^{-8}$	$9.23 \cdot 10^{-8}$
300	16.31	$8.28 \cdot 10^{-8}$	$7.79 \cdot 10^{-8}$	$8.76 \cdot 10^{-8}$
350	16.18	$2.24 \cdot 10^{-7}$	$2.07 \cdot 10^{-7}$	$2.40 \cdot 10^{-7}$

TABLE 4. 7. THE SHEET RESISTANCE AND AVERAGE CONTACT RESISTIVITY OF NI CONTACTS AS WELL AS ITS MINIMUM AND MAXIMUM VALUES MEASURED ON THE INGAAS SUBSTRATE WITH 100 SCCM OF SN DOPING.

Temp. (℃)	R_s (Ω)	ρ_c (Ωcm^2)	Min	Max
25	16.29	$1.21 \cdot 10^{-7}$	$1.39 \cdot 10^{-7}$	$1.04 \cdot 10^{-7}$
250	16.52	$1.16 \cdot 10^{-7}$	$1.16 \cdot 10^{-7}$	$1.16 \cdot 10^{-7}$
300	16.02	$1.69 \cdot 10^{-7}$	$1.92 \cdot 10^{-7}$	$1.47 \cdot 10^{-7}$
350	16.52	$1.92 \cdot 10^{-7}$	$2.20 \cdot 10^{-7}$	$1.64 \cdot 10^{-7}$

In addition, since 300 sccm of Sn flow rate gives a lower carrier concentration than that of 220 sccm, the lowest ρ_c from 300 sccm, which is $1.77 \cdot 10^{-7}$ Ωcm^2 at 350 ℃, is higher than that from 220 sccm as presented in Fig. 4. 19 and table 4. 8. However, ρ_c does not have a clear temperature dependence because it goes up at 300 ℃ and decreases afterwards which makes the measurement data less trustworthy. Apart from the data from 300 sccm, when considering the doping concentration of 220 and 100 sccm, the lowest ρ_c of Ni contacts on the InGaAs substrate is $8.28 \cdot 10^{-8}$ Ωcm^2 with 220 sccm of Sn doping on the conducting layer. A 300 ℃ annealing for 1 min decreases the contact resistivity of Ni/Pd/Au contacts from $1.35 \cdot 10^{-7}$ to $8.28 \cdot 10^{-8}$ Ωcm^2. Czornomaz et al. reported $1.05 \cdot 10^{-6}$ Ωcm^2 resistivity Ni-InGaAs Ohmic contacts to n^+-$In_{0.53}Ga_{0.47}As$ with $1 \cdot 10^{19}$ cm^{-3} of active carrier concentration [6]. Our value is at least a factor of 10 better than the one reported in [6] compared to n^+-$In_{0.63}Ga_{0.37}As$ with 100 sccm of Sn flow which provides $2 \cdot 10^{19}$ cm^{-3} of carrier concentration.

Comparing the lowest ρ_c of the Ni contacts to the unintentionally doped n-InAs ($3.02 \cdot 10^{-8}$ Ωcm^2) to that to the n^+-$In_{0.63}Ga_{0.37}As$, the later one exhibited a higher value by $5.26 \cdot 10^{-8}$ Ωcm^2. In other words, the Ni contacts can achieve lower ρ_c on the unintentionally doped n-InAs than on the n^+-$In_{0.63}Ga_{0.37}As$. This in turn means that the narrow band gap material (InAs) appeared to form better Ohmic contacts.

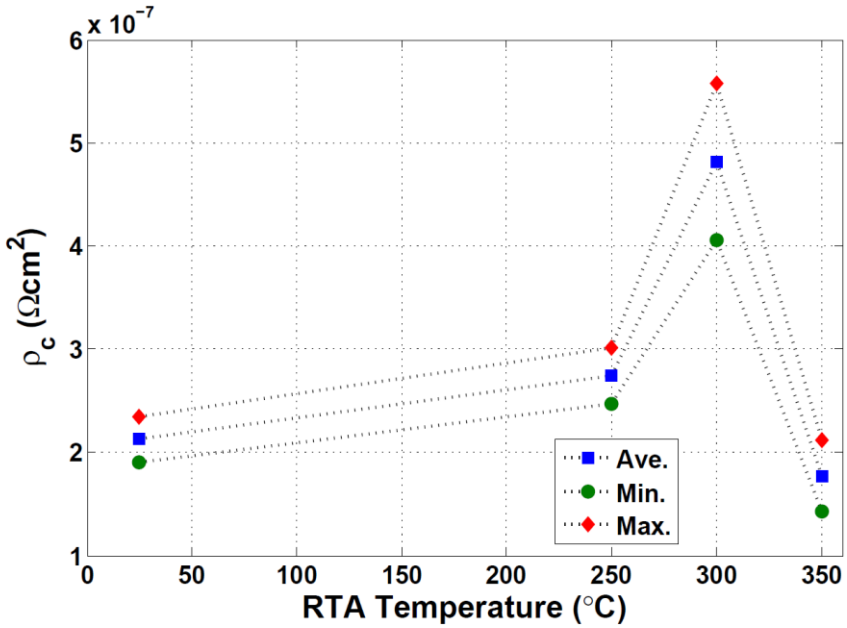


Fig. 4. 19. The contact resistivity of evaporated Ni contacts as a function of RTA temperature from the InGaAs substrates with 300 sccm of Sn flow rate.

TABLE 4. 8. THE SHEET RESISTANCE AND AVERAGE CONTACT RESISTIVITY OF NI CONTACTS AS WELL AS ITS MINIMUM AND MAXIMUM VALUES MEASURED ON THE INGAAS SUBSTRATE WITH 300 SCCM OF SN DOPING.

Temp. (℃)	R_s (Ω)	ρ_c (Ωcm^2)	Min	Max
25	4.32	$2.12 \cdot 10^{-7}$	$1.90 \cdot 10^{-7}$	$2.35 \cdot 10^{-7}$
250	4.04	$2.74 \cdot 10^{-7}$	$2.47 \cdot 10^{-7}$	$3.01 \cdot 10^{-7}$
300	4.08	$4.82 \cdot 10^{-7}$	$4.06 \cdot 10^{-7}$	$5.57 \cdot 10^{-7}$
350	4.13	$1.77 \cdot 10^{-7}$	$1.42 \cdot 10^{-7}$	$2.11 \cdot 10^{-7}$

4.2.2 Ti contacts

Ti contacts were deposited by thermal evaporation on n^+-$In_{0.63}Ga_{0.37}As$ with 220 and 100 sccm of Sn flow rate, and its contact resistivities as a function of anneal temperature are shown in Fig. 4. 20 and the specific values of R_s and ρ_c are exhibited in table 4. 9 and 4. 10. Both ρ_c measured from the two samples show small reduction up to 350 ℃, by $0.38 \cdot 10^{-7}$ Ωcm^2 and $1.02 \cdot 10^{-7}$ Ωcm^2 for 220 and 100 sccm of Sn flow, respectively. Ti contacts

to InGaAs also do not show any degradation up to 350 ℃ as Ti contacts to InAs. Since a higher doping concentration gives a large number of conduction electrons and decreases the depletion thickness which in turn increases tunneling probability, the contact resistivity from n^+-$In_{0.63}Ga_{0.37}As$ with 220 sccm of Sn flow is lower than that with 100 sccm. The lowest ρ_c of Ti contacts on the n^+-$In_{0.63}Ga_{0.37}As$ substrate is $1.01 \cdot 10^{-7}$ Ωcm^2 with 220 sccm of Sn doping. A 350 ℃ annealing for 1 min decreases the contact resistivity of Ti/Pd/Au contacts from $1.39 \cdot 10^{-7}$ to $1.01 \cdot 10^{-7}$ Ωcm^2. Also, the extracted L_T ($\sim 1.7 \cdot 10^{-6}$ m) is much larger than n^+-$In_{0.63}Ga_{0.37}As$ thickness (120 nm), so the one-dimensional current flow approximation is also appropriate [46]. Stareev at al. obtained $4.3 \cdot 10^{-8}$ Ωcm^2 resistivity Ohmic contacts to n^+-$In_{0.53}Ga_{0.47}As$ with an active doping of $5 \cdot 10^{19}$ cm^{-3} which is the same as we used, using *in situ* Ar^+ sputter cleaning [21]. It exhibited lower ρ_c than we obtained ($1.01 \cdot 10^{-7}$ Ωcm^2) which may be due to *in situ* Ar^+ cleaning. Hence again we expect that *in situ* Ar^+ sputter cleaning prior to metal deposition would improve the contact resistivity. In addition, Adam et al. reported $\rho_c = 7.3 \cdot 10^{-9}$ Ωcm^2 of Ti contacts to n^+-$In_{0.53}Ga_{0.47}As$ with with an active doping of $\sim 3.5 \cdot 10^{19}$ cm^{-3} using 10 min of UV-ozone and 10 s dip in NH_4OH (14.8 normality) prior to metal deposition by e-beam evaporation [19]. Even with low doping concentration, it showed a factor of 10 lower ρ_c than we reported which appeared to be due to a different surface preparation. A lower concentration of NH_4OH than used in our work (20.5 normality) seems to be compatible with lift-off procedure, so we expect that longer UV-ozone oxidation and oxide removal with NH_4OH can improve the contact resistivity.

Compared to Ti contacts on unintentionally doped n-InAs, Ti contacts to n-InAs shows lower ρ_c by $6.08 \cdot 10^{-8}$ Ωcm^2 than that of n^+-$In_{0.63}Ga_{0.37}As$. Once again, the narrow band gap material (InAs) forms better Ohmic contacts to metals. In addition, the lowest ρ_c of Ti contacts is higher than that of Ni contacts by $1.82 \cdot 10^{-8}$ Ωcm^2, so alloyed Ni contacts to n^+-$In_{0.63}Ga_{0.37}As$ also provide better contact resistivities than nonalloyed Ti contacts.

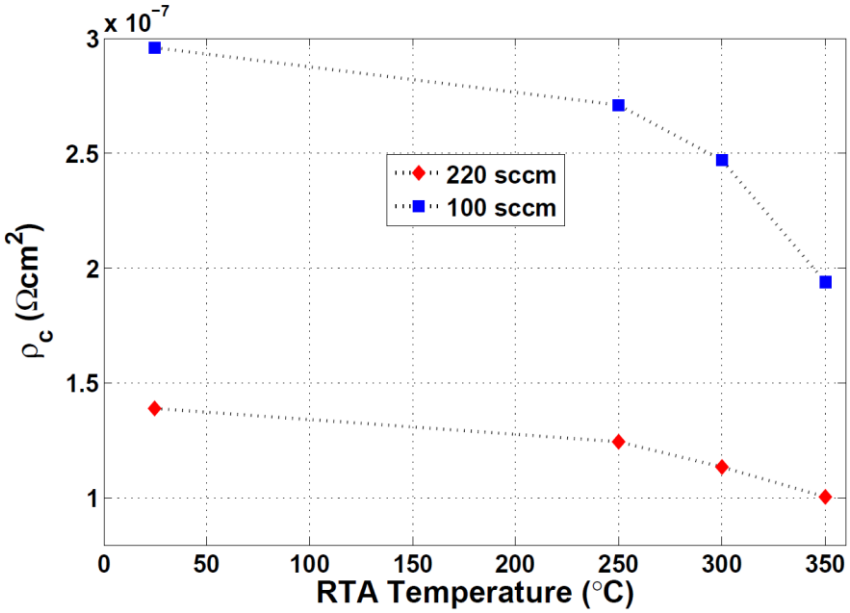


Fig. 4. 20. The contact resistivity of evaporated Ti contacts as a function of RTA temperature from the InGaAs substrates with two different doping concentrations.

TABLE 4. 9. THE SHEET RESISTANCE AND AVERAGE CONTACT RESISTIVITY OF TI CONTACTS AS WELL AS ITS MINIMUM AND MAXIMUM VALUES MEASURED ON THE INGAAS SUBSTRATE WITH 220 SCCM OF SN DOPING.

Temp. (℃)	R_s (Ω)	ρ_c (Ωcm^2)	Min	Max
25	16.03	$1.39 \cdot 10^{-7}$	$1.39 \cdot 10^{-7}$	
250	16.30	$1.25 \cdot 10^{-7}$	$1.17 \cdot 10^{-7}$	$1.33 \cdot 10^{-7}$
300	16.14	$1.14 \cdot 10^{-7}$	$1.12 \cdot 10^{-7}$	$1.16 \cdot 10^{-7}$
350	16.29	$1.01 \cdot 10^{-7}$	$9.66 \cdot 10^{-8}$	$1.05 \cdot 10^{-7}$

TABLE 4. 10. THE SHEET RESISTANCE AND AVERAGE CONTACT RESISTIVITY OF TI CONTACTS AS WELL AS ITS MINIMUM AND MAXIMUM VALUES MEASURED ON THE INGAAS SUBSTRATE WITH 100 SCCM OF SN DOPING.

Temp. (℃)	R_s (Ω)	ρ_c (Ωcm^2)	Min	Max
25	15.25	$2.96 \cdot 10^{-7}$	$2.96 \cdot 10^{-7}$	
250	15.14	$2.71 \cdot 10^{-7}$	$2.71 \cdot 10^{-7}$	
300	15.30	$2.47 \cdot 10^{-7}$	$2.28 \cdot 10^{-7}$	$2.66 \cdot 10^{-7}$
350	15.81	$1.94 \cdot 10^{-7}$	$1.94 \cdot 10^{-7}$	$1.95 \cdot 10^{-7}$

CHAPTER 5

5 Conclusion

Using transmission line model (TLM), we extracted the specific contact resistivities of Ohmic contacts. In order to achieve more accurate contact resistivities, we designed the new TLM mask and adapted a more precise gap measurement method.

Since we used *ex situ* contact formation, we studied different surface preparations. UV-ozone oxidation and oxide removal with 1:1 HCl:DI water reduced the contact resistivity by $7.00 \cdot 10^{-8}$ Ωcm^2 at most compared to using oxygen plasma ashing instead of UV-ozone.

We developed Ni and Ti Ohmic contacts to unintentionally doped n-InAs and highly doped n^+-$In_{0.63}Ga_{0.37}As$ with three different carrier concentrations and were able to reduce the contact resistivities of Ni and Ti contacts through annealing. Ni formed a metallic alloy with InAs and InGaAs, resulting NiInAs and Ni-InGaAs through annealing. On the other hand, Ti formed a nonalloyed Ohmic contact.

For unintentionally doped n-InAs with a carrier concentration of $5 \cdot 10^{18}$ cm^{-3}, the lowest contact resistivity was $3.02 \cdot 10^{-8}$ Ωcm^2 for the Ni contact annealed at 150 ℃ for 1 min. The Ti contact exhibited the $3.29 \cdot 10^{-8}$ Ωcm^2 resistivity Ohmic contact at anneal temperature of 300 ℃. It indicates that the alloyed Ohmic contacts were found to decrease the contact resistivities, but it is comparable to nonalloyed Ti contacts.

For n^+-$In_{0.63}Ga_{0.37}As$, the lowest contact resistivity obtained was $8.28 \cdot 10^{-8}$ Ωcm^2 for the Ni contact made to n^+-$In_{0.63}Ga_{0.37}As$ with an electron concentration of $5 \cdot 10^{19}$ cm^{-3} at anneal temperature of 300 ℃. A contact resistivity of $1.01 \cdot 10^{-7}$ Ωcm^2 was obtained for Ti contact for an electron concentration of $5 \cdot 10^{19}$ cm^{-3} as well. The alloyed Ni contact

exhibited a lower contact resistivity than the nonalloyed Ti contact. Furthermore, the lowest contact resistivity of all our results was obtained from the alloyed Ni contact to InAs who has a narrow band gap where the Fermi level pins close to the conduction band.

In conclusion, we have demonstrated low resistance Ni and Ti contacts to unintentionally doped n-InAs and n^{+}-$In_{0.63}Ga_{0.37}As$ via annealing which make them a potential candidate for highly scaled HBTs and MOSFETs which require low contact resistivities.

CHAPTER 6

6 Future work

TLM structures

- In order to increase the accuracy of contact resistivity, gap separations (L_{gap}) with 1 and 2 μm between the metal pads have to be developed which can be achieved by electron beam lithography. Even better if TLM structures can be designed with smaller separation than 1 μm. Since extrapolation is used to extract contact resistivity, it allows moving closer to the y-axis with increasing the accuracy.

Ni wet etching

- Since Ni deposited by sputtering was over-etched after 3 min in 1:2.5:2.5:15 H_2SO_4:HNO_3:CH_3COOH:DI water, the etching duration can be shorten.

Surface preparations

- Prior to metal deposition by sputtering, several surface preparations can be tried such as *in situ* Ar^+ cleaning, 10 % $(NH_4)_2S$ and NH_4OH if Ni wet etching works well.
- Before thermal evaporation, UV-ozone oxidation duration can be increased. Since the normality of NH_4OH was too high to be compatible with the lift-off process, it can be reduced up to 14.8, as reported in [19].

Cross section of Ni alloy

- The future work could involve transmission electron micrograph of the Ni alloy phase in order to observe the nickelide/semiconductor interface and see any changes as anneal temperature increases.

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