A Reconfigurable Optical Header Recognition System for Optical Packet Routing Applications

Chun Tian, Zhaowei Zhang, Morten Ibsen, Periklis Petropoulos, and David J. Richardson

***Abstract*—We demonstrate a reconfigurable all-optical packet processing system. The key device is a code-reconfigurable header decoder based on a fiber Bragg grating. The performance of the system is tested for different packet headers, and error-free operation is confirmed.**

***Index Terms*—Fiber Bragg grating (FBG), optical code, optical fiber communication, optical packet switching.**

I. Introduction

THE adoption of optical packet processing technology promises a route to more flexible optical networks offering potential advantages in terms of bandwidth utilization efficiency and payload transparency amongst others. A critical function in any optical packet-based network is the reliable generation and processing of headers. Most current schemes still use electronic means for this purpose and the associated speed limitations restrict the header recognition and processing times. This limitation can be overcome by employing photonic technologies in which the header recognition speed is determined primarily by the propagation delay for light traveling through some relatively short photonic structure, e.g., a fiber grating, or a planar lightwave circuit [1], [2]. Optical solutions are expected to employ an array of photonic processors to facilitate parallel processing of headers, and conventional bit-serial packet architectures, in which the packet header and payload are allocated different time slots and are transmitted sequentially [1], [3], [4], can be employed.

The codes we use in our proposed bit-serial configuration, have been extensively investigated for optical code-division multiple-access (OCDMA) applications [5] and can be generated and processed directly in the optical domain, thus guaranteeing ultrahigh-speed and minimum latency. Fig. 1 illustrates the operating principle of bit-serial networking using optical codes [4]. The optical encoder converts a single short optical pulse into a code represented by a specific sequence of individual pulses, and is normally designed, so that when a decoder with similar characteristics is assigned to it, then a distinct autocorrelation peak is produced via matched filtering. Conversely, for any unmatched codes or for the payload, only a low intensity noise-like cross-correlation appears at the decoder's output. The autocorrelation peak can be easily detected using threshold detection and used to control the routing actions of a suitable fast optical switch.

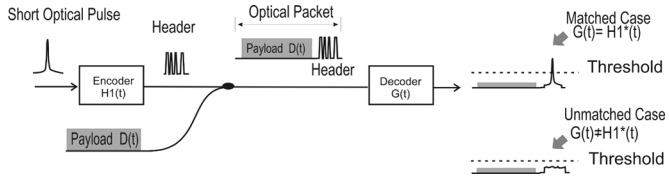

Fig. 1. Principle of header processing in a bit-serial packet routing system.

Our system relies on superstructured fiber Bragg gratings (SSFBGs) to generate and process the optical codes. SSFBGs are compact, polarization-insensitive devices, have the potential of low cost and relatively straightforward fabrication. The codes are written within the SSFBGs by means of a spatial amplitude or phase envelope superimposed upon an otherwise uniform FBG refractive index modulation profile. A matched filter for header recognition is formed by using an SSFBG which has the time-reversed profile of the encoding grating. We have previously demonstrated that it is possible to fabricate SSFBGs incorporating complex codes, including for example 255 chip quaternary phase-shift-keyed sequences [3].

However, despite the advantages offered by this technique, SSFBGs are normally passive devices carrying a fixed code. Thus, a different encoding/decoding SSFBG would be required to process each of the addresses used in the network. To enhance the flexibility of switched networks, it is highly desirable that header processing devices in the address bank array have the capability to tune to a different optical header on demand. To this end, we have developed thermally tuned code-reconfigurable devices based on uniform FBGs for optical code generation and recognition [6]. The thermally induced phase shifts along the FBG can produce superstructure characteristics (and hence codes) similar to fixed-coded SSFBGs, for dynamic optical header recognition. We have recently shown that these devices are compatible with fixed-coded SSFBGs and have a reasonably fast reconfiguration time of less than 2 s [7].

In this letter, we describe an experimental demonstration of a reconfigurable optical header processing system based on a code-reconfigurable decoder. Preliminary results of this work were presented in [8]. We show that a single decoding device can be electrically tuned to decode different codes, and we characterize the performance of the system.

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Color versions of Figs. 2 and 3 are available at http://ieeexplore.ieee.org.

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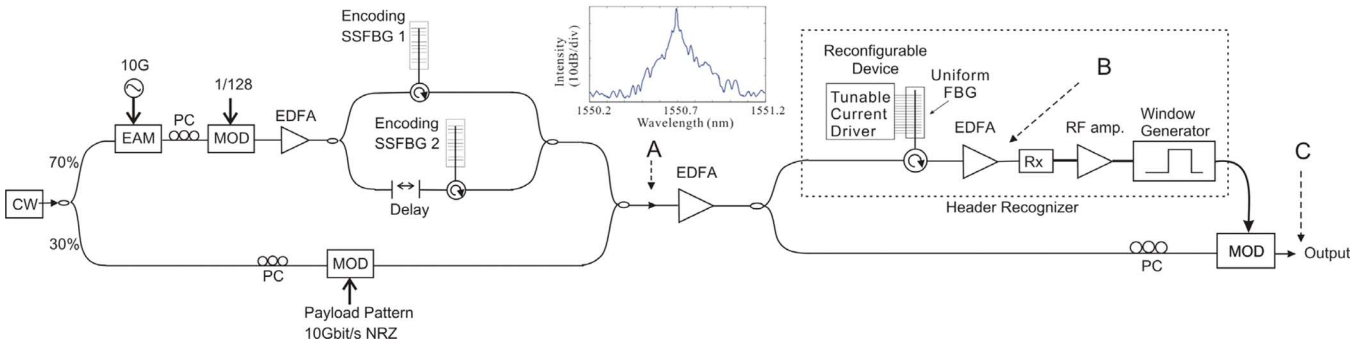

Fig. 2. Experimental setup of the reconfigurable packet routing system. Inset shows the spectrum of the transmitted signal.

II. Optical Packet Processing System

A. Experimental Setup

The experimental setup we used to demonstrate the operation of our scheme is shown in Fig. 2, and incorporated a packet transmitter and a reconfigurable packet processing node. The packet transmitter used a single continuous-wave (CW) laser source (tuned to the wavelength of the encoding SSFBGs) which was split into two paths to generate the headers and payload, respectively. For the header generation, the CW beam was carved using an electroabsorption modulator into a 10-GHz pulse train and then gated down to 78 MHz using a $LiNbO_3$ modulator. The generated 20-ps pulses were split again to generate two 400-ps-long headers (H1 and H2) from two different 16-chip, 40 Gchip/s quaternary phase-shift-keyed fixed-coded SSFBGs. The codes used to represent the headers were chosen from Family A Codes [9], which are designed for four-phase level coding with near-optimum correlation properties. Light in the second path was intensity modulated by a $LiNbO_3$ modulator with nonreturn-to-zero data sequences at 10 Gb/s which represented the payloads for both types of packets (P1 and P2). The relative delay between each header and associated payload was adjusted to allocate them sequential time slots before they were combined together.

At the packet processing node, optical header recognition was performed to control the switching of the payload. The incoming packet stream was split by a 3-dB fiber coupler. One part of the signal was input to a $LiNbO_3$ modulator which acted as an optical switch. The other part of the signal was injected into the code-reconfigurable FBG. This comprised a uniform FBG upon which 15 thin electrical wires were coupled in a direction perpendicular to the fiber axis. The wires were spatially separated by 2.5 mm corresponding to a temporal separation of 25 ps. Dynamic assignment of a phase-shift-keyed code on the FBG superstructure could be achieved by appropriate control of the current flowing through each of the wires due to the induced localized heating [7]. A Peltier cooler attached to the fiber ensured that the ambient temperature of the FBG remained stable to within $\sim$0.4 °C, as required for reliable operation of the decoder. The device was programmed to match either code of the SSFBG header generators. It should be noted that the wavelength-selective nature of the FBG means that no other filter is required for header processing, even when more than one channel is included in the system. The resulting autocorrelation peak reflected off the FBG was detected by a photodetector and triggered an electrical pulse generator, which generated an electrical pulse of a suitable width to drive the $LiNbO_3$ switch. By simply changing the code configuration of the decoding device, we were able to detect either header H1 or H2 and switch out either payload P1 or P2 accordingly.

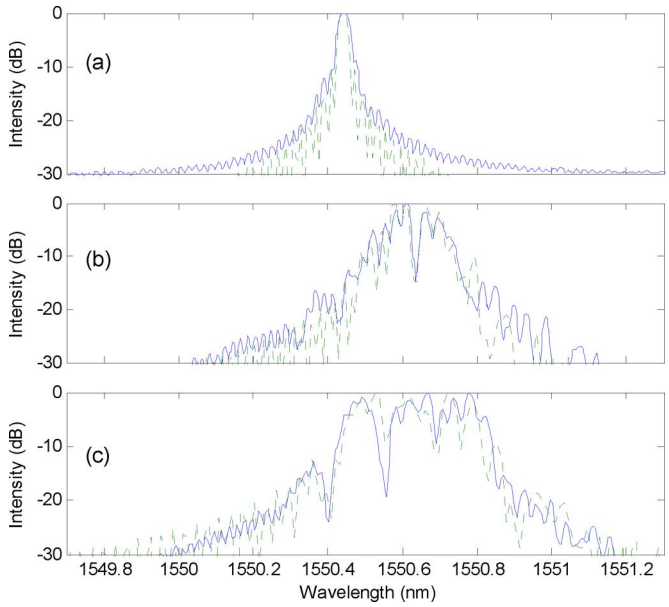

Fig. 3. Reflectivity spectra of the reconfigurable device when (a) no code (uniform FBG), (b) code H1, and (c) H2 were configured to the FBG. (Solid lines: measured results. Dashed lines: simulation results).

B. Experimental Results

Fig. 3 shows reflectivity spectra of the FBG when (a) no code is assigned to it, and when it is set to either (b) code H1 or (c) code H2. The bandwidth of the device changes from 0.19 nm at the 20-dB level when no phase shifts have been applied to it (corresponding to the bandwidth of the uniform FBG) to 0.52 nm once a code is configured on the FBG structure. This is determined by the bandwidth of the 25-ps-long chips comprising the codes. Simulation results are also shown in Fig. 3 which compares the experimental traces to the ideal spectra of the programmed codes, showing good agreement between the two. The

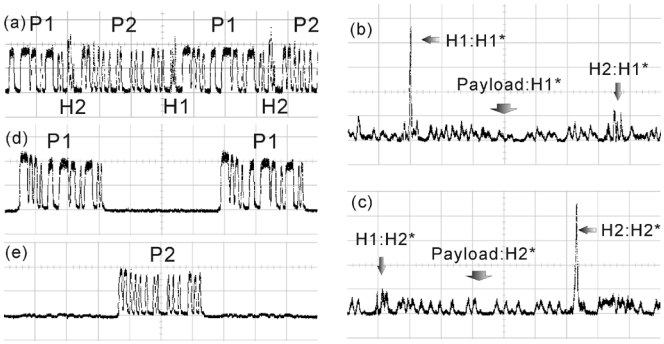

Fig. 4. Oscilloscope traces for (a) packet stream at Point A (2 ns/div), (b), (c) output of header recognition at Point B (1 ns/div), and (d), (e) dropped payload at Point C (2 ns/div).

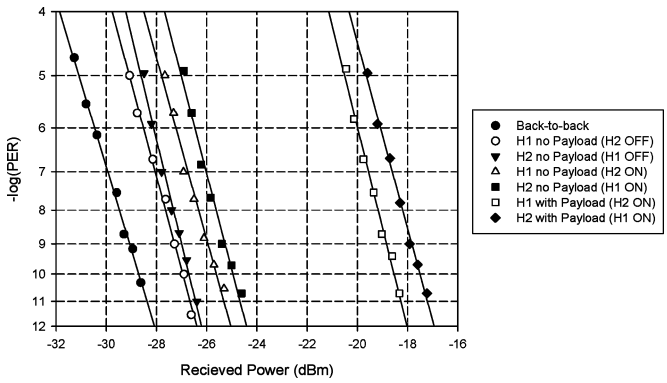

Fig. 5. PER test results.

figure also shows that there is a slight shift in the central wavelength of the FBG after application of a code, which is due to the thermally induced change in the Bragg condition.

Fig. 4(a) shows the generated packet stream at Point A, in which two different packets are transmitted alternately. Each packet has a length of 6.4 ns, which comprises the 0.4-ns header, the 5.2-ns payload, and 0.4-ns guard bands both before and after the header. Fig. 4(b) and (c) shows the output of the reconfigurable decoder at Point B, when the reconfigurable device is programmed to decode header H1 or H2, respectively. The corresponding header is decoded correctly as denoted by the distinct autocorrelation peak, which is detected by the threshold detector which controls the switch. The extinction of the correlation pulses is 5.5 dB (detailed measurements of the correlation properties of the device can be found in [7]). Fig. 4(d) and (e) show the corresponding dropped packets at Point C.

To evaluate the system performance of our system, we measured the packet error-rate (PER) as determined at Point B of the experimental setup. For comparison, we tested the back-to-back case (which contained no encoding), the one code autocorrelation case (which contained only one code), and the cases when the payloads were switched OFF and ON, respectively. As can be seen in Fig. 5, when there is no data payload in the packet, the power penalty due to the encoding process is $\sim$3 dB. Error-free performance is also achieved when the payload is switched ON, however, the remaining power of the cross-correlation signal between the FBG code and the payload reaches the receiver, resulting in an additional power penalty of $\sim$7 dB.

III. Conclusion

We have demonstrated the operation of an all-optical packet processing system based on optical header recognition through matched filtering in a dynamically reconfigurable FBG device. The decoding device used in our experiments incorporated 16-chip codes at a rate of 40 Gchip/s. Electrical adjustment of the heat-inducing electrodes allowed tuning of the decoder to match different codes/headers within a time of 2 s. The reconfigurable decoder can easily be scaled to accommodate even longer codes by using a longer uniform grating, and mounting more electrodes upon it. Faster (subsecond) response times should be possible by using a combination of thinner grating fibers and electrodes. Note that such tunable code recognition devices are also of significant interest for use in reconfigurable OCDMA systems where code tuning speed is a lesser concern.

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