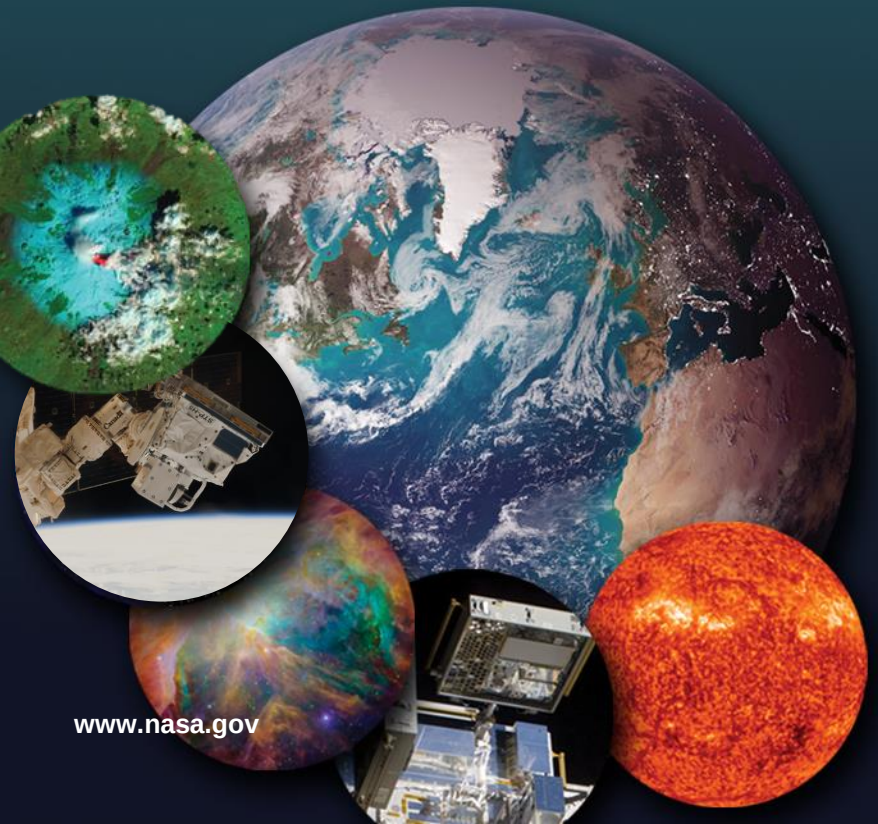
https://ntrs.nasa.gov/search.jsp?R=20200000731 2020-03-28T18:48:06+00:00Z

National Aeronautics and Space Administration

SpaceCube

A NASA Family of Reconfigurable Hybrid On-Board Science Data Processors

SpaceCube



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Future In-Space Operations (FISO)
Working Group Seminar

January 2020

www.nasa.gov

Outline

1. Background
2. Introduction to SpaceCube and Embedded Processing Group
3. SpaceCube v3.0 and Mini Overview
4. cFS and SpaceCube Software Development Kit
5. Intelligent Solutions for Space
6. Academic Partnerships

BACKGROUND

The Challenge

*The next generation of NASA science and exploration missions will require "**order of magnitude**" improvements in on-board computing power …*

Mission Enabling Science Algorithms & Applications Require More Capability

- Real-time Sensing and Control
- On-Board Data Volume Reduction
- Real-time Image Processing
- Autonomous Operations
- On-Board Product Generation
- Real-time Event / Feature Detection
- On-Board Classification
- Real-time "Situational Awareness"
- "Intelligent Instrument" Data Selection / Compression
- Real-time Calibration / Correction
- Inter-platform Collaboration

NASA Motivations

- **Support Science**: Processing requirements for future science sensors and instruments are dramatically increasing (e.g. higher resolution, shorter temporal spacing and improved accuracy etc…), onboard processing can alleviate data storage and data downlink requirements

> *"A critical element for all of these is the infrastructure for downloading and processing **ever-increasing data streams**."*
>
> *- Decadal Survey for Earth Science and Applications*

- **Reduce Costs, Improve Performance**: Traditional radiation-hardened processors are reliable, but costly and slow. Commercial devices provide more performance but can be affected by radiation

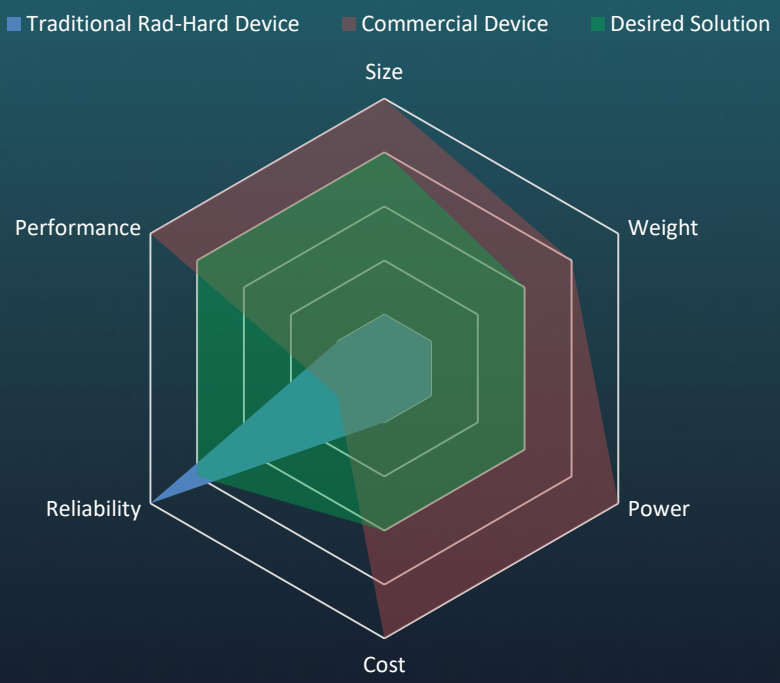
> "Flight computing technologies include ultra-reliable, radiation-hardened platforms, which, until recently, have been **extremely costly and limited in performance**. Future radiation hardening will be achieved by a combination of traditional parts-level hardening, rad-hard-by-design"
>
> - NASA Technology Roadmap TA 11.1.1

- **Enable Autonomy and Intelligent Systems**: State-of-the-art deep learning and artificial intelligence frameworks require substantial processing capabilities

> "**Performance is limited** by mission computing"
>
> - Autonomous Systems NASA Capability Overview

Space Computing Requirements

- Embedded space environments have strict requirements and restrictions
  - Performance (throughput and real-time)
  - Size, Weight, Power, and Cost (SWAP-C)
  - Reliability (device lifetime and radiation effects)
    - Single-Event Effects
    - Total Ionizing Dose
- Identifying solutions that provide optimal balance of crucial criteria



Example Comparison of Criteria with Radar Chart

Featured Technology

- Field Programmable Gate Array (**FPGA**)
  - Large amount of logic resources and specialized design units connected with complex and configurable routing network
  - Lower frequency and power over conventional CPU
  - Massive algorithm parallelism for immense speedup

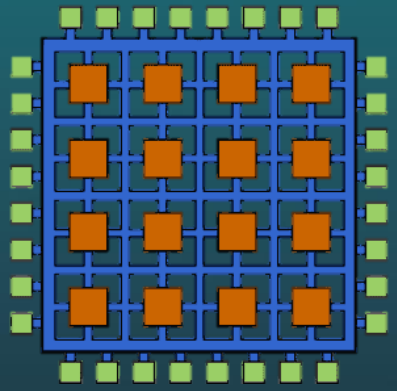


Image Courtesy:
B. Zeidman, EE Times "All about FPGAs"

- System-on-Chip (**SoC**)
  - Integrated Circuit that combines many processing technologies into single chip
  - Some applications are control-flow oriented and better suited for CPUs

XILINX®

Images Courtesy: Xilinx

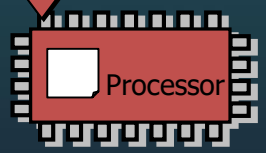
Hybrid Architectures

Examples Courtesy:
Dr. Greg Stitt, University of Florida

- FPGAs are NOT just "glue" logic for instruments and sensors, they can be used to rapidly hardware accelerate applications

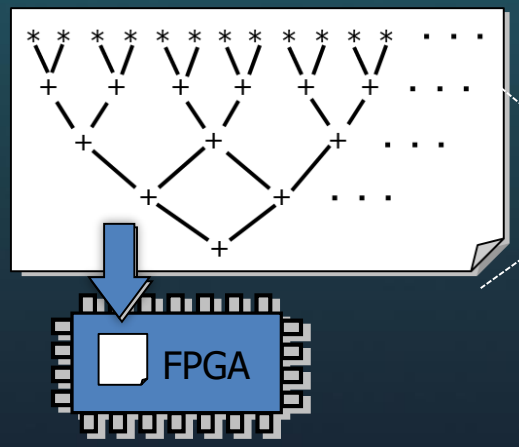
C Code

```
for (i=0; i < 128; i++)
  y += c[i] * x[i]
```



- 1000's of instructions
- Several thousand cycles

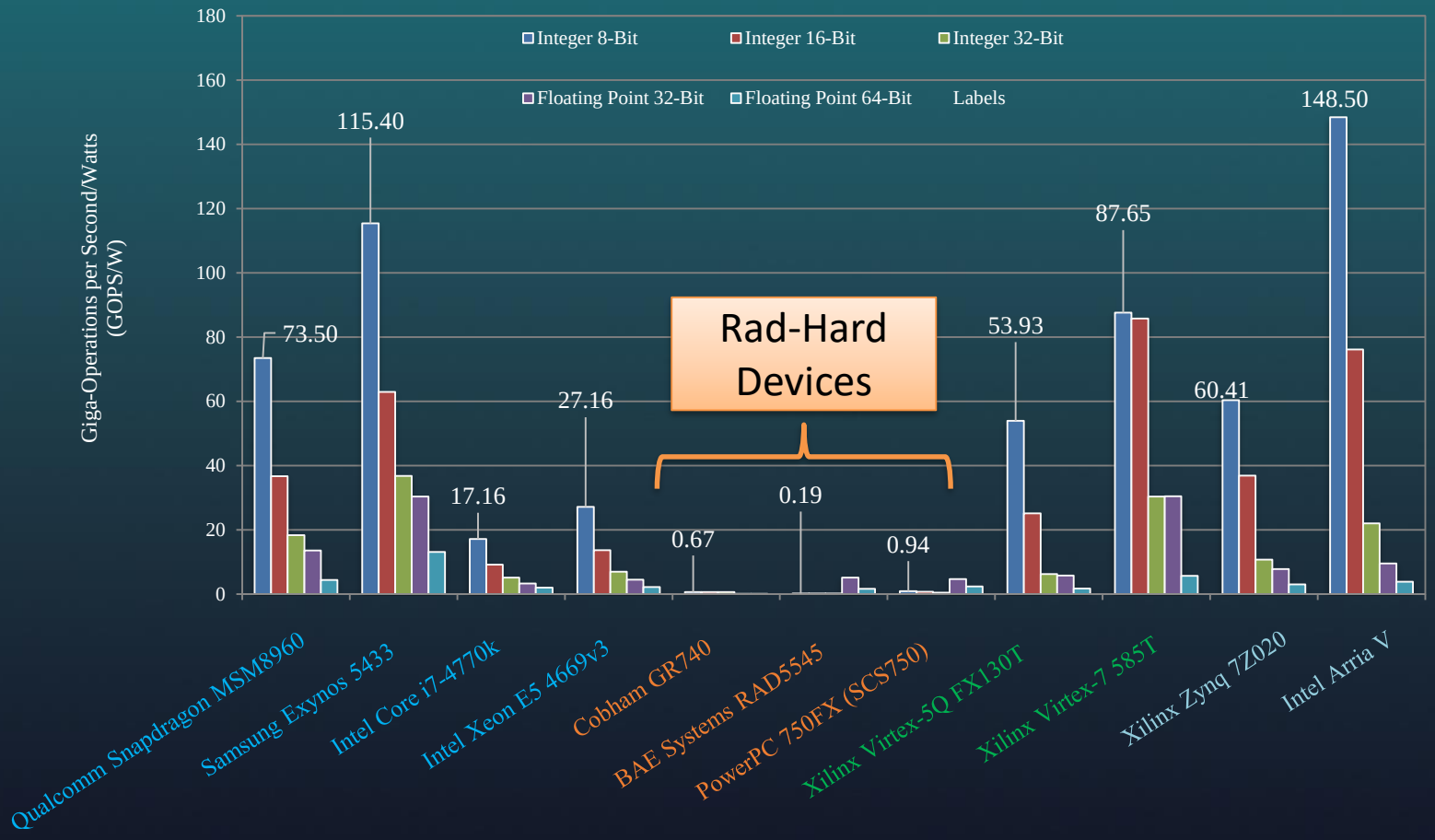
FPGA Circuit



- ~ 7 cycles (assuming 1 cycle per op)
- Speedup > 100x for same clock

- Not all applications have algorithm parallelism that can be improved by FPGAs (like desktop applications)
- Hybrid architectures allow developers to leverage different architectures for portions of the application they are best at

Commercial vs. Rad-Hard



GOPS/W = Giga-Operations Per Second / Watt

A. D. George and C. Wilson, "Onboard Processing with Hybrid and Reconfigurable Computing on Small Satellites," Proceedings of the IEEE, vol. 106, no. 3, pp. 458-470, Mar 2018.

Lovelly, T. M. and George, A D., "Comparative Analysis of Present and Future Space-Grade Processors with Device Metrics,"AIAA Journal of Aerospace Information Systems, Vol. 14, No. 3, Mar. 2017, pp. 184-197. doi: 10.2514/ 1.I010472

Harsh Space Environment

- Space is **difficult environment** to design for due to hazards of radiation effects
- Radiation Particles and Sources
  - Solar Flares & Coronal Mass Ejections
  - Galactic Cosmic Rays
  - Trapped Protons & High Energy Ions
- Radiation Effects
  - Temporal / Transient Effects
    - Single Event Effects (**SEE**): Upset (SEU), Transient (SET), Latchup (SEL), Burnout (SEB), Gate Rupture (SEGR),Functional Interrupt (SEFI)
  - Cumulative Effects
    - Total Ionizing Dose Levels (**TID**)
    - Enhanced low-dose-rate sensitivity (ELDRS)

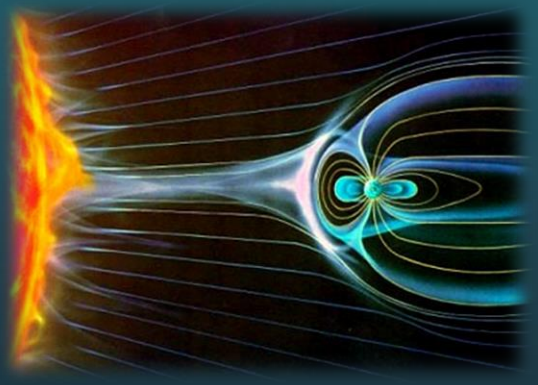


Image Courtesy:
J. Barth, 1997 IEEE NSREC Short Course

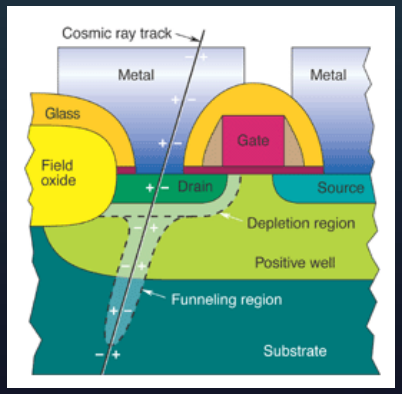


Image Courtesy:
National Academies,
Testing at the Speed of Light

INTRODUCTION TO SPACECUBE AND EMBEDDED PROCESSING GROUP

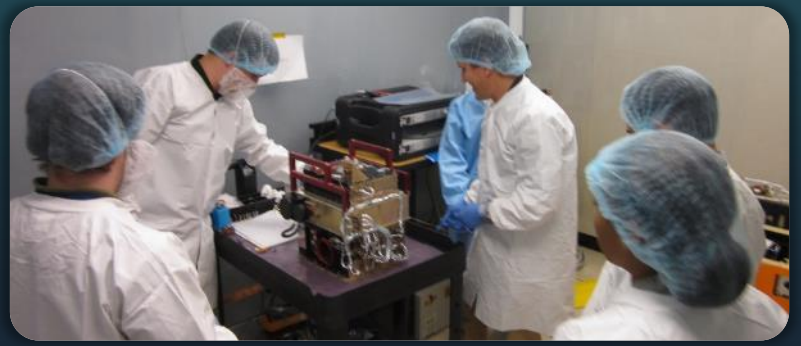
Science Data Processing Branch
Embedded Processing Group (EPG)

EPG Group Specializes in Embedded Development

- Hardware acceleration of algorithms and applications
- Intelligence, autonomy, and novel architectures
- Flight software integration for development platforms
- Advanced architectures and research platforms

Advanced Platforms for Spaceflight

- SpaceCube v2.0 and v2.0 Mini
- SpaceCube v3.0 and v3.0 Mini
- SpaceCube Mini-Z and Mini-Z45



Key Tools and Skills

- **Flight Software**: cFE/cFS, driver integration, flight algorithms
- **GSE**: COSMOS, GMSEC, system testbeds
- **FPGA Design**: Hardware acceleration, fault-tolerant structures
- **Mission Support**: Supporting flight cards, algorithm development
- **On-board Autonomy and Analysis**: deep-learning and machine-learning frameworks, unique architectures

SpaceCube v2.0

SpaceCube Approach

01 The traditional path of developing radiation-hardened flight processor **will not work** … they are always one or two generations behind

02 Use latest radiation-tolerant* processing elements to achieve massive **improvement** in "MIPS/Watt" (for same size/weight/power)

03 Accept that radiation-induced upsets may happen occasionally and just deal with them appropriately … nearly any level of reliability can be achieved via **smart system design!**

***Radiation tolerant – susceptible to radiation-induced upsets (bit flips) but not radiation-induced destructive failures (latch-up)**

SpaceCube Introduction

What is SpaceCube?

A family of NASA developed space processors that established a **hybrid-processing approach** combining radiation-hardened and commercial components while emphasizing a novel architecture **harmonizing** the best capabilities of CPUs, DSPs, and FPGAs

High performance reconfigurable science / mission data processor based on Xilinx FPGAs

- Hybrid processing - algorithm profiling and partitioning to CPU, DSP, and FPGA logic
- Integrated "radiation upset mitigation" techniques
- SpaceCube "core software" infrastructure (SCSDK) - Example (cFE/cFS and "SpaceCube Linux" with Xenomai)
- Small "critical function" manager/watchdog
- Standard high-speed (multi-Gbps) interfaces

SpaceCube v1.0

SpaceCube is Hybrid Processing…

Being Reconfigurable …

… equals BIG SAVINGS (both time and money)

During mission development and testing

- Design changes without PCB changes
- "Late" fixes without breaking integration

During mission operations

- On-orbit hybrid algorithm updates
- Adaptive processing modes
  - hi-reliability vs. high-performance
  - intelligently adapt to current environment

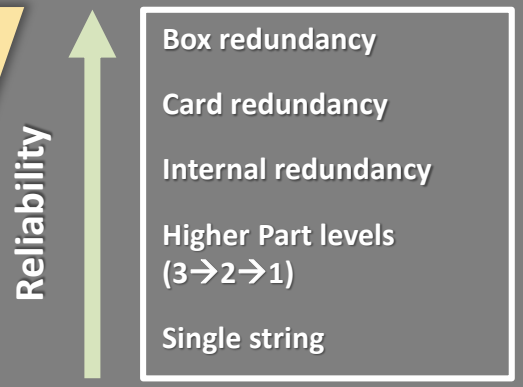
From mission to mission

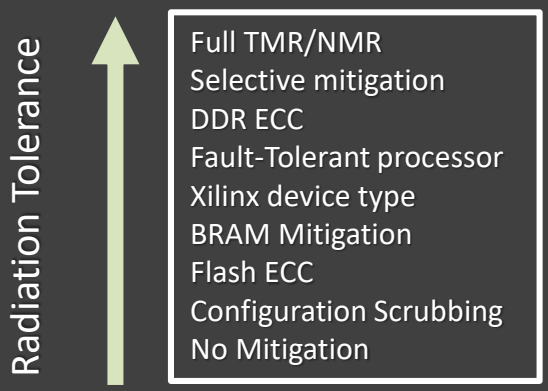
- Same avionics reconfigured for new mission

Reliability Spectrum (It's your choice)

Systems Trades

Computing Performance vs. Radiation Performance (adding levels of radiation tolerance requires some level of resources)





Mission Examples

Low End To High End, In Order Of Increasing Cost

Tech Demo

ISS, Single string, "EDU" parts, Config scrubbing, Flash ECC, Defense-grade Xilinx using PowerPCs

Class C

Level 2 parts, some redundancy, DDR ECC, FT processor for critical tasks, selective mitigation

Class A/B

Level 1 parts, Box redundancy, FT processor, memory EDAC, possibly full TMR

SpaceCube Heritage

Closing the gap with commercial processors while retaining reliability

- **57+ Xilinx device-years on orbit**
- **26 Xilinx FPGAs in space to date (2019)**
- **11 systems in space to date (2019)**

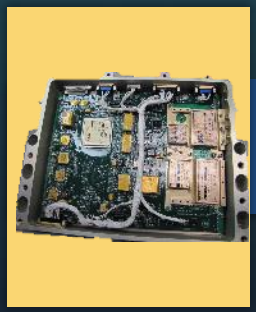
SpaceCube is Mission Enabling…

SpaceCube v1.0

STS-125, MISSE-7, STP-H4, STP-H5, STP-H6

SpaceCube v1.5

SMART (ORS)



SpaceCube v2.0-EM

STP-H4, STP-H5

SpaceCube v2.0-FLT

RRM3, STP-H6 (NavCube)

SpaceCube v2.0 Mini

STP-H5, UVSC-GEO

SpaceCube on the ISS

(Past and Present)

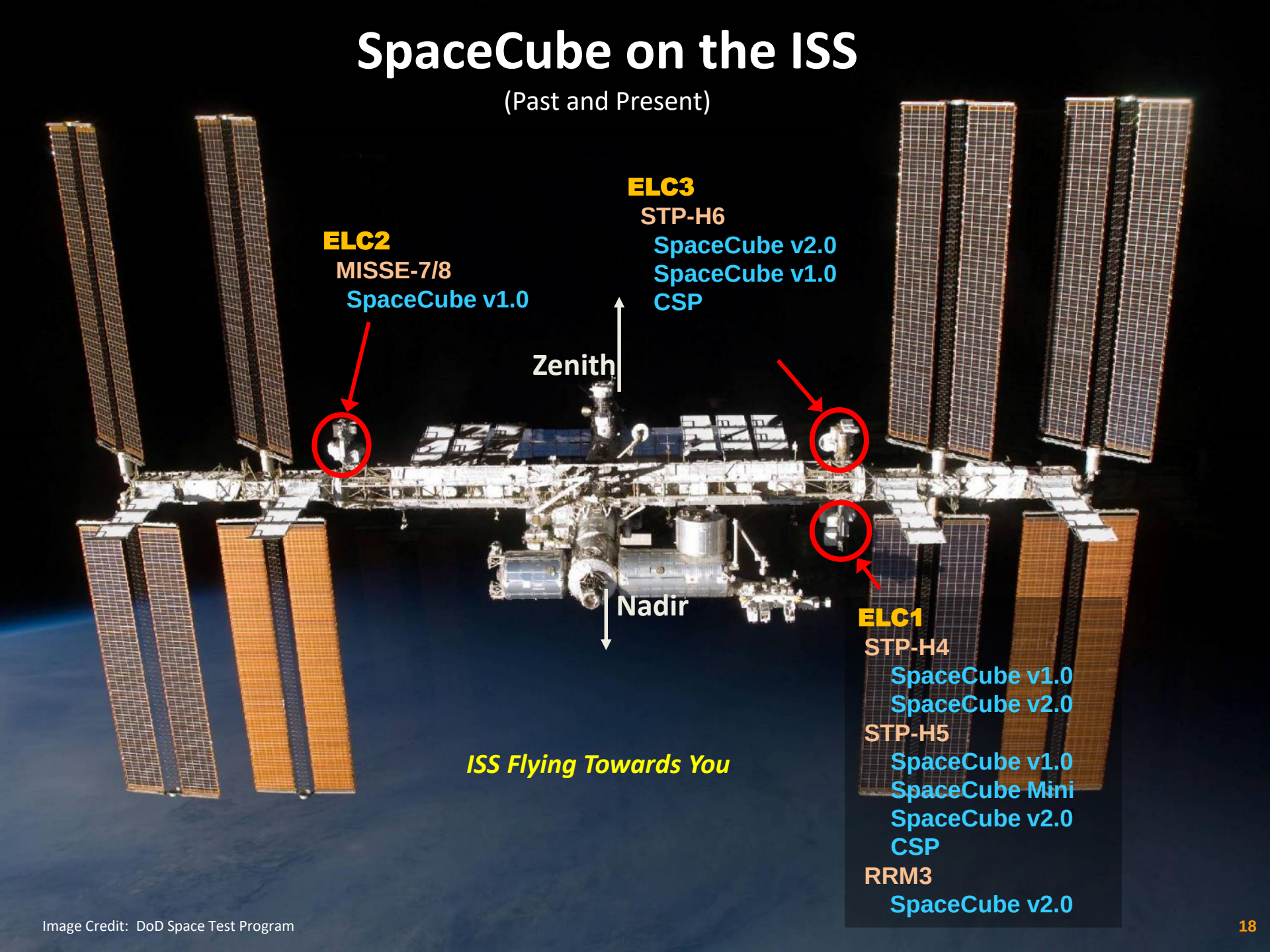


Image Credit: DoD Space Test Program

SpaceCube v2.0 Processor Card

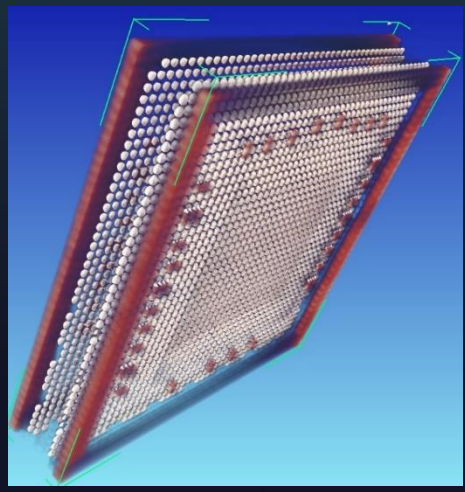
Overview

- TRL9 flight-proven processing system with unique Virtex **back-to-back** installed design methodology
- **3U cPCI** (190 x 100mm) size
- Typical power draw: 8-10W
- 22-layer, via-in-pad, board design
- IPC 6012B Class 3/A compliant

High-Level Specifications

- 2x Xilinx Virtex-5 (QR) FX130T FPGAs (FX200T Compatible)
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Timers
  - Auxiliary Command/Telemetry port
- 4x 512 MB DDR SDRAM
- 2x 4GB NAND Flash
- 1x 128Mb PROM, contains initial Xilinx configuration files
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 16-channel Analog/Digital circuit for system health
- Mechanical support for heat pipes and stiffener for Xilinx devices
- External Interfaces
  - Gigabit interfaces: 4x external, 2x on backplane
  - 12x Full-Duplex dedicated differential channels
  - 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Debug Interfaces
  - Optional 10/100 Ethernet interface

Back-to-Back FPGA Design



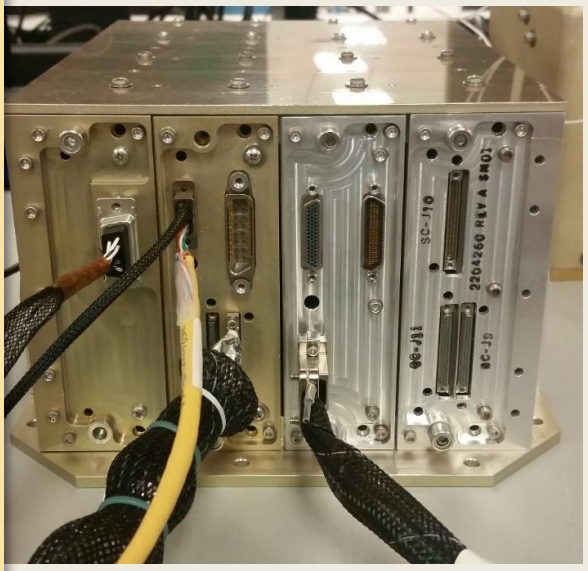
Robotic Refueling Mission 3 (RRM3)

Overview

- Technology demonstration experiment to highlight innovative methods to store and replenish cryogenic fluid in space

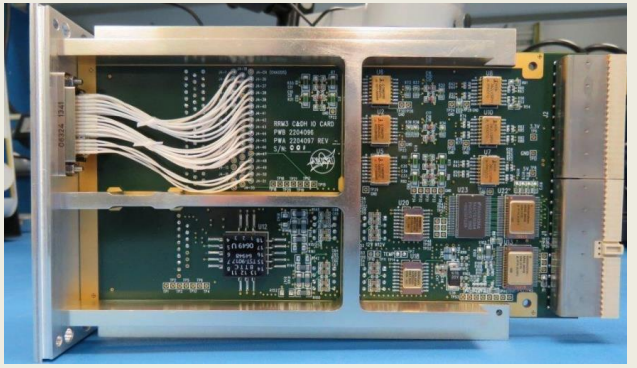
High-Level Requirements

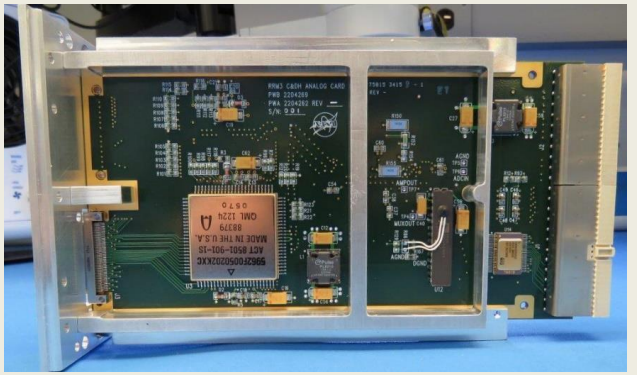
- Interface with ISS and RRM3 instruments: cameras, thermal imager, motors
- Monitor/Control cryo-cooler and fuel transfer
- Stream video data
- Motor control of robotic tools
- Host Wireless Access Point



Robotic Refueling Mission 3 SpaceCube

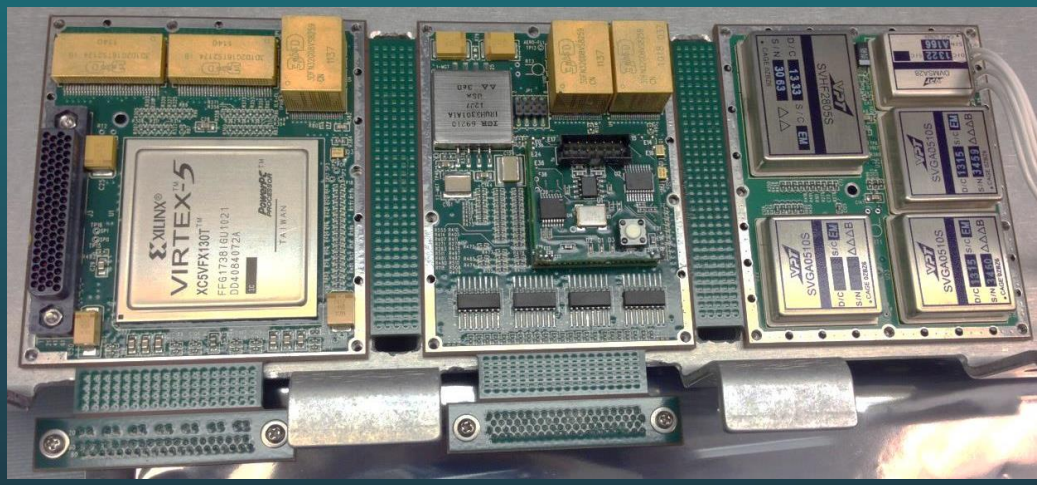
1553/Ethernet/Digital Card





Analog Card

SpaceCube v2.0 Mini



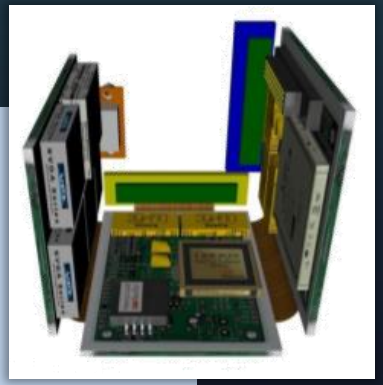
Overview

- TRL9 flight-proven processing system, miniaturized version of SpaceCube v2.0 Processor Card for **CubeSats**
- 1U CubeSat (10 x 10 x 10 mm) size
- Typical power draw: <10 W
- Scalable design allow daisy-chaining of Mini cards with Gigabit interface

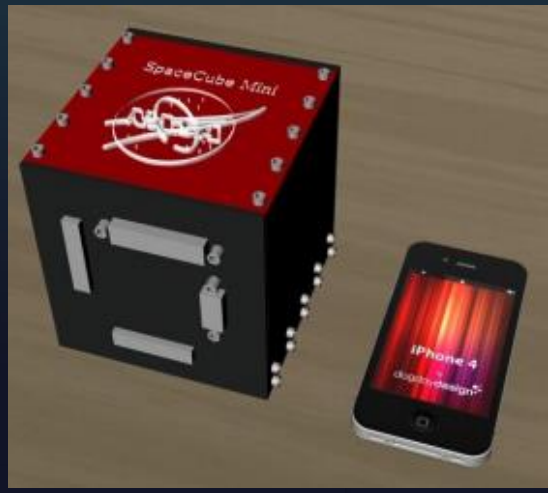
High-Level Specifications

- 1x Xilinx Virtex-5 (QR) FX130T FPGAs
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Scrubber
- 1x 512 Mx16 DDR SDRAM
- 3x 4GB NAND Flash
- 12 bit Analog/Digital converter
- External Interfaces
  - 2x SATA interfaces
  - 4x Spacewire or 8x LVDS interfaces
  - 8x RS-422 interfaces
  - 7x Xilinx MGT
  - 120 Singled-Ended
  - 2 Passive Thermistors
  - 5 Analog

Flight Deployment



Scale Comparison



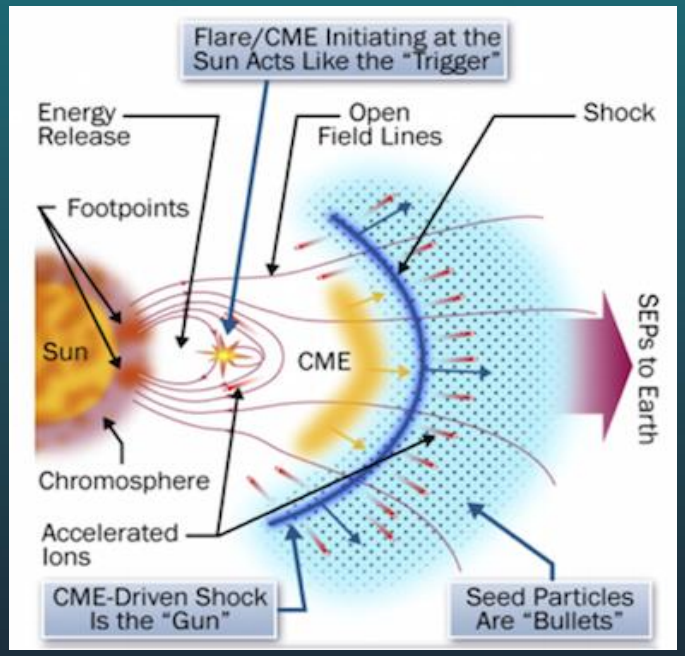
Ultraviolet Spectro-Coronagraph (UVSC) Pathfinder

Overview

- Combines ultra-violet spectrograph with novel, high-throughput coronagraph to search for presence of suprathermal seed particles near sun
- Particles are believed to be necessary for production of large solar energetic particle (SEP) events
- SEP events disrupt Navy/DoD space operations with **little or no warning**

High-Level Requirements

- Scheduled to fly in 2020 on STPSat6
- **SpaceCube v2.0 Mini** serves as the UVSC instrument processor
- Hybrid high-performance fault-tolerant software architecture



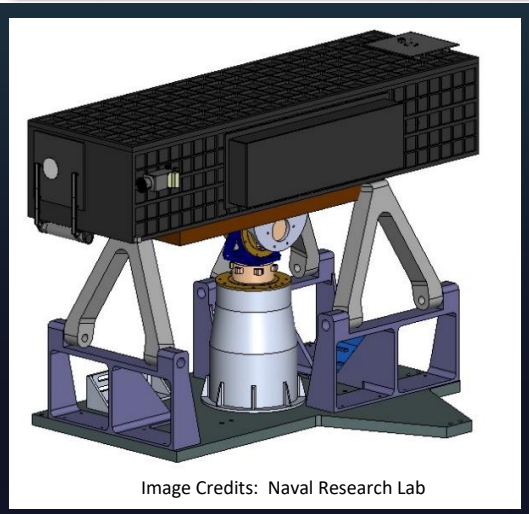


Image Credits: Naval Research Lab

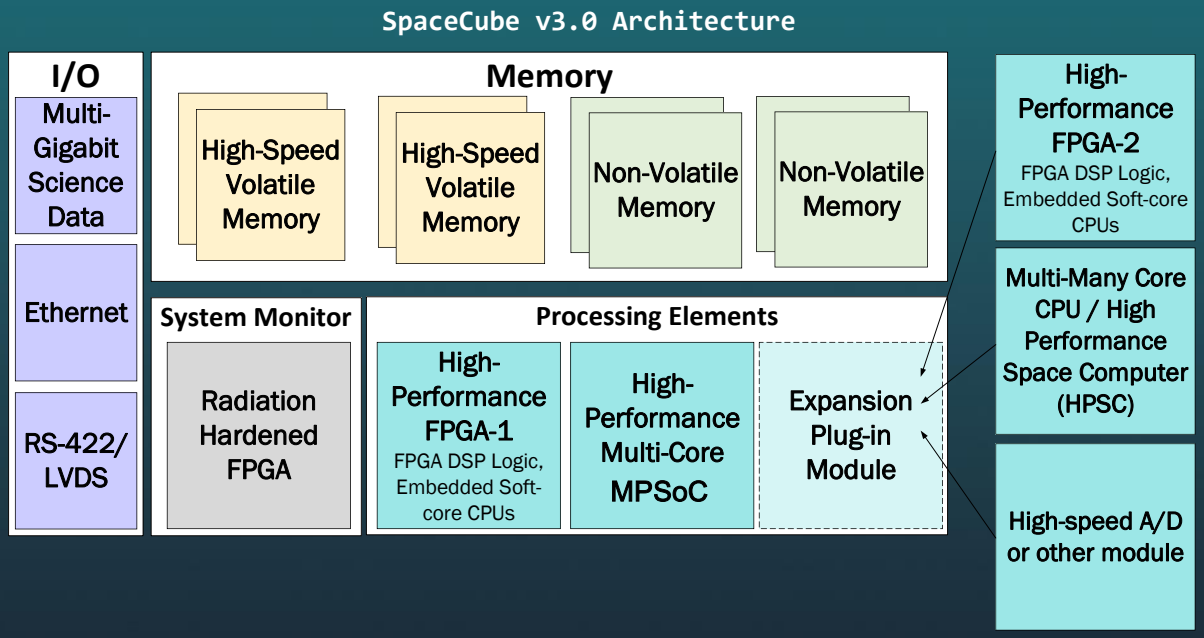
NASA Next-Generation High-Performance Processor
for Science Applications

SPACECUBE V3.0 PROCESSOR CARD

SpaceCube v3.0 Processor Card

Overview

- **Next-Generation** SpaceCube Design
- Prototype demonstration Q1 2020
- **3U SpaceVPX** Form-Factor
- Ultimate goal of using High-Performance Spaceflight Computing (**HPSC**) paired with the high-performance FPGA
  - HPSC will not be ready in time for the prototype design
  - Special FMC+ Expansion Slot



High-Level Specifications

1x Xilinx Kintex UltraScale

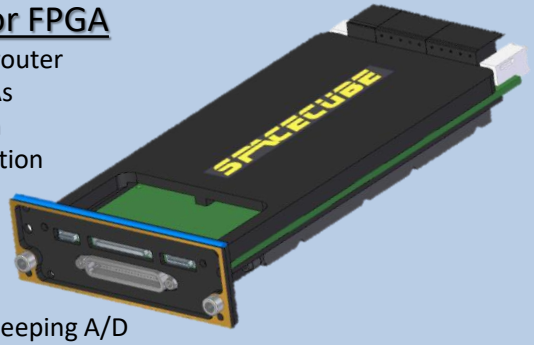
- 2x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - 24x Multi-Gigabit Transceivers
  - 75x LVDS pairs or 150x 1.8V single-ended I/O
  - 38x 3.3V single-ended I/O,
  - 4x RS-422/LVDS/SPW
- Debug Interfaces
  - 2x RS-422 UART / JTAG

1x Xilinx Zynq MPSoC

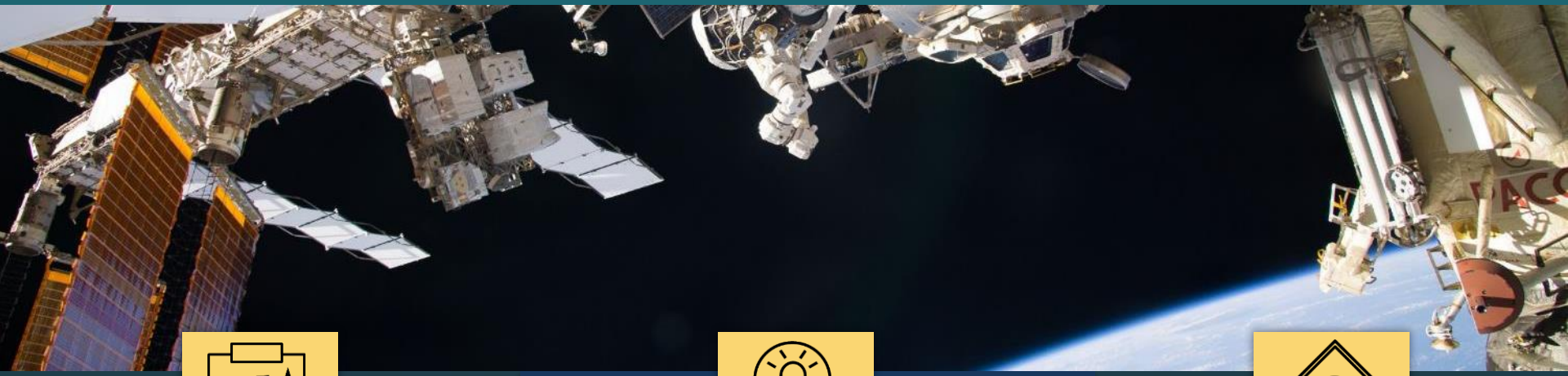
- Quad-core Arm Cortex-A53 processor (1.3GHz)
- Dual Arm R5 processor (533MHz)
- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - I2C/CAN/GigE/SPIO/GPIO/SPW
  - 12x Multi-Gigabit Transceivers
- Debug Interfaces
  - 10/100/1000 Ethernet (non-flight)
  - 2x RS-422 UART / JTAG

Rad-Hard Monitor FPGA

- Internal SpaceWire router between Xilinx FPGAs
- 1x 16GB NAND Flash
- Scrubbing/configuration of Kintex FPGA
- Power sequencing
- External Interfaces
  - SpaceWire
- 2x 8-channel housekeeping A/D with current monitoring



Goals, Motivations, Challenges



Goals

Develop reliable, high-speed hybrid processor using SpaceCube design approach to **enable next-generation instrument and SmallSat capability**

Motivations

Highly reliable designs for varying mission environmental scenarios

New capabilities to support sensor integration and design tool flows

Need exceptional resources to support **complex applications** such as artificial intelligence

Challenges

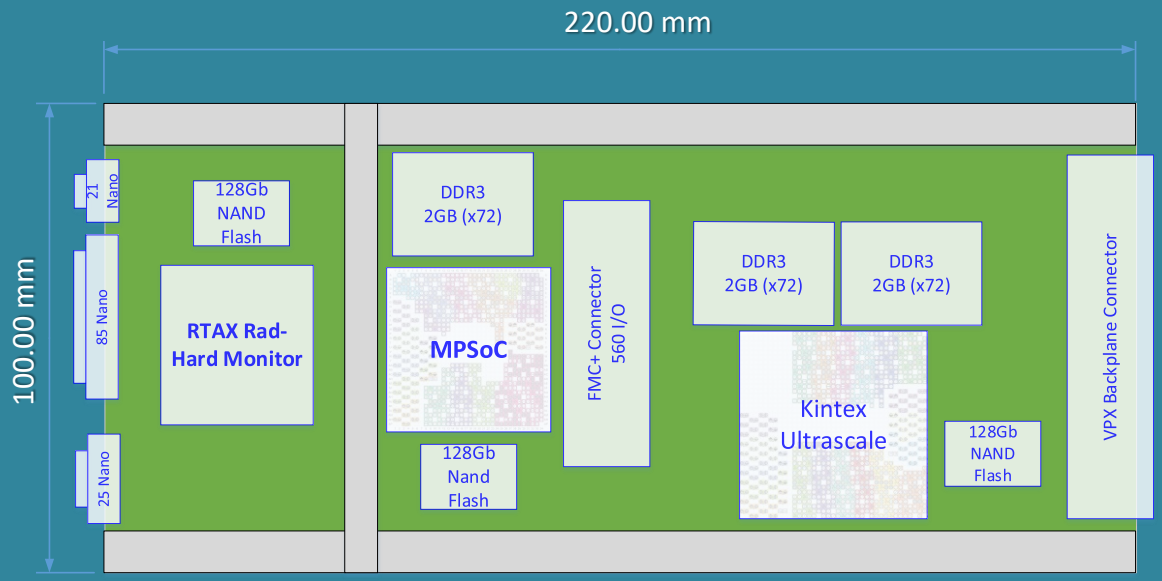
Managing PCB area restrictions for rad-hard components, balancing cost, routing, and **signal and power integrity**

Mechanical and **thermal**

Supporting integrated software development kit

Card Layout and Design Approach

SpaceCube v3.0 Processor Card



Reliable Monitor

Reliable supervisors for health monitoring, rollback, reconfiguration, and scrubbing

Quality Parts Selection

Flight-qualified parts where feasible, screening, qualification, and risk mitigation everywhere else

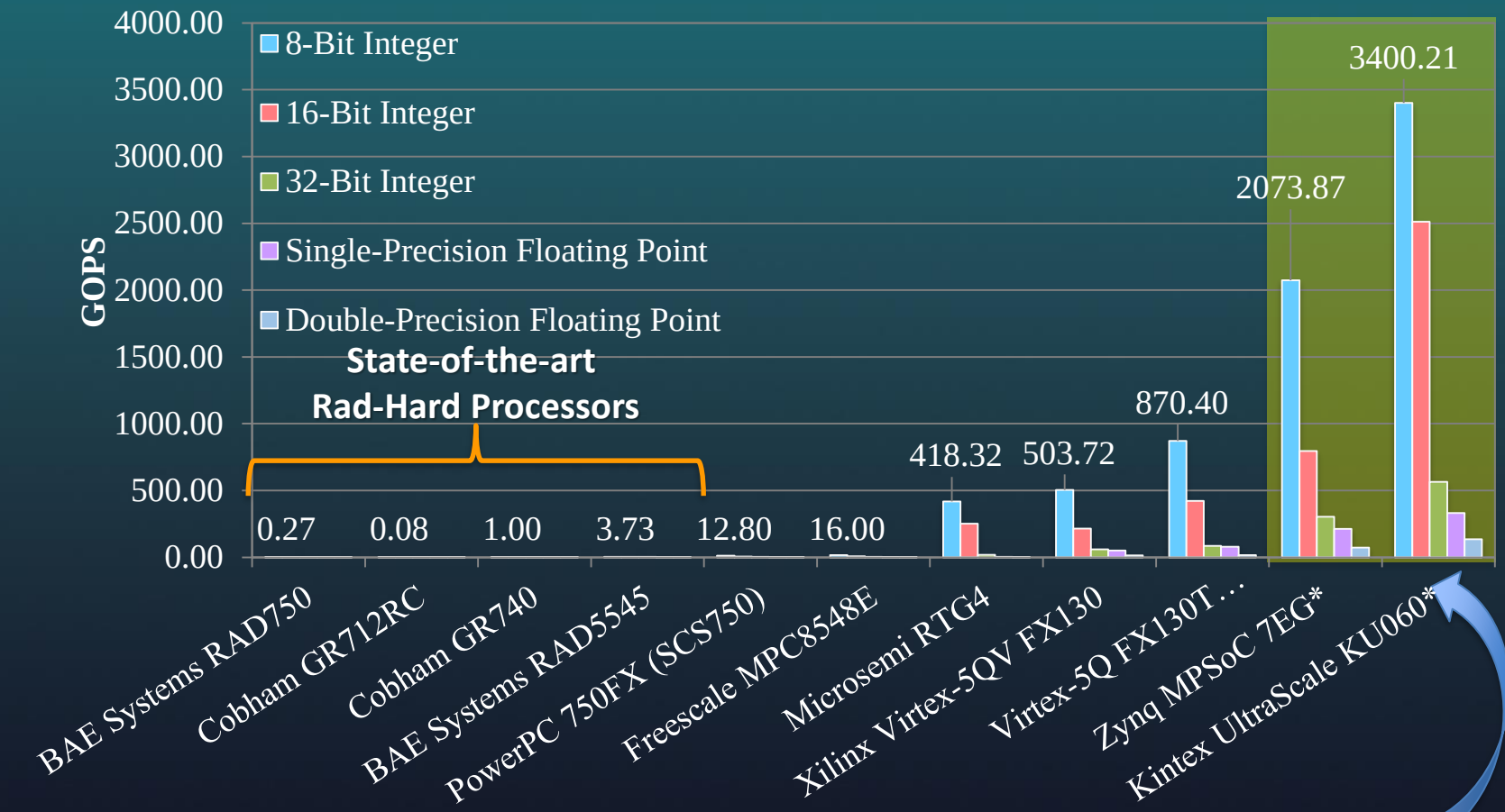
Modularity

Industry standard backplane-style interfaces for compatibility and expandability

Xilinx Devices and System Design

Emphasis on Xilinx designs for reconfigurability and flexibility, and focus on fault tolerance

Performance - Metrics



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Devices used in SpaceCube v3.0

*UltraScale results are an estimate based off of existing data, new metrics are in progress but not currently available

SpaceCube Family Comparisons

Processor	Configuration	CoreMark
MicroBlaze (Softcore FPGA Fabric)	Xilinx v8.20b Virtex-5, 5-Stage Pipeline 16K/16K Cache 125MHz	238[1]
IBM PowerPC 405 (SpaceCube v1.0 Virtex-4)	300 MHz	664.791[1]
IBM PowerPC 440 (SpaceCube v2.0 Virtex-5)	400 MHz, Bus 100 MHz	1155.62
	125 MHz, Bus 125 MHz	361.13
ARM Cortex-R5 (SpaceCube v3.0 Zynq MPSoC)	500 MHz	1286.03
ARM Cortex-A53 (SpaceCube v3.0 Zynq MPSoC)	1.2 GHz, -O3	16449.621[1]
	1.2 GHz, -O2	15866.62

Resources	SpaceCube v1.0	SpaceCube v2.0 (FX130)	SpaceCube v2.0 (FX200)	SpaceCube v3.0
LUTS (K)	101	164	246	562
FF (K)	101	164	246	1124
RAM (Mb)	0.79	21	33	49 + 27 UltraRAM
DSPs	256	640	768	4488

CoreMark®

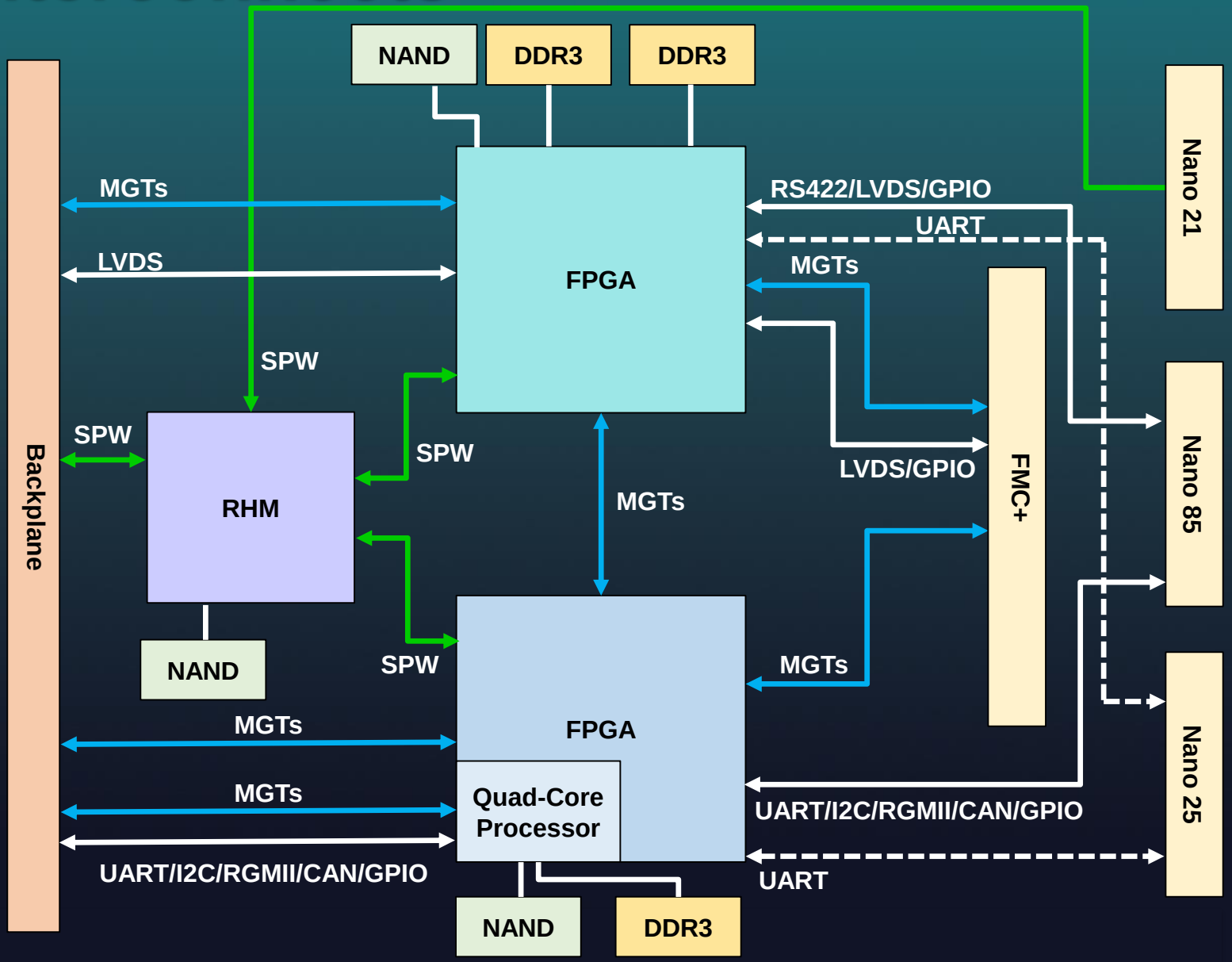
Benchmark by the Embedded Microprocessor Benchmark Consortium (EMBC), measures microcontroller and CPU performance. CoreMark is small, portable, simple, free, and displays a single number benchmark score. CoreMark has specific run and reporting rules, to avoid more problematic issues with Dhrystone

14x Increase in Processor Performance over Prior Generation

3.4x Increase in LUTs 6.85x Increase in FFs over FX130-based SCv2.0

[1] https://www.eembc.org/coremark/scores.php

Interconnects



HPSC Integration

Overview

- NASA/AFRL Collaboration for radiation hardened multi-core chiplet

Early Prototyping Effort

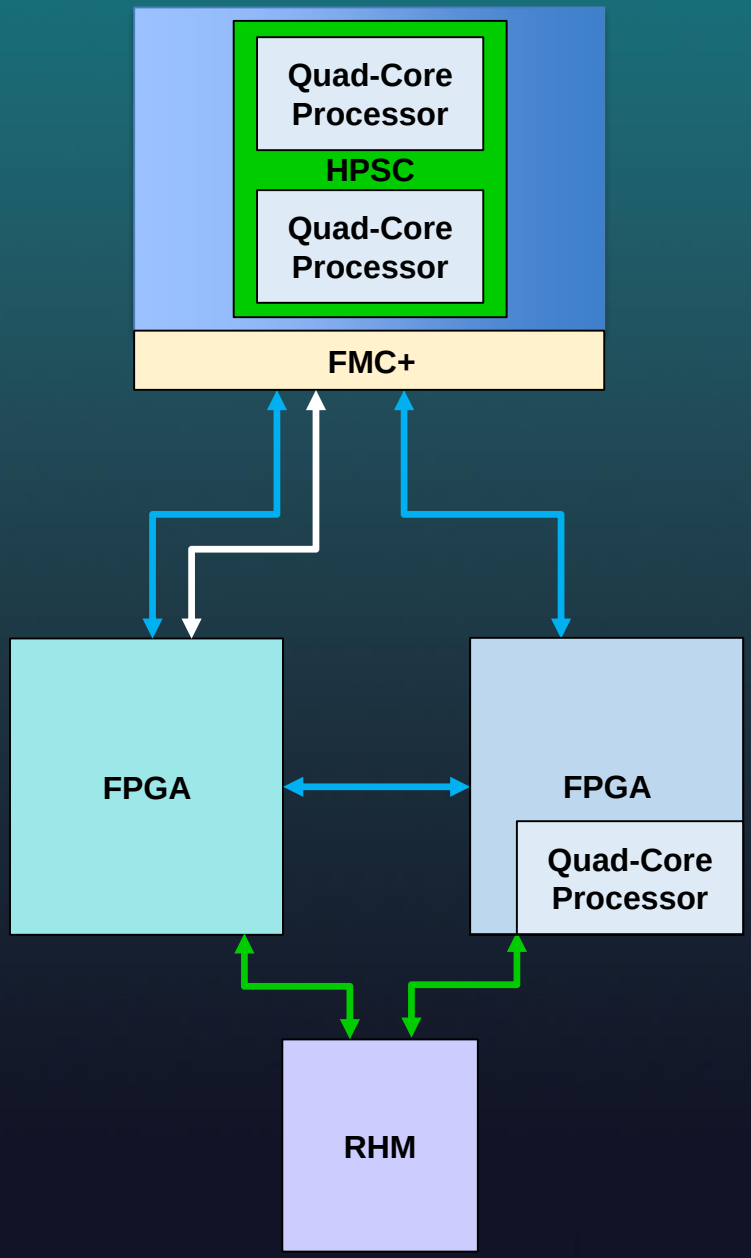
- HPSC chiplets will not be ready until 2021
- HPSC designs and prototypes can be conducted with MPSoC

MPSoC Replacement

- Next version of SpaceCube v3.0 can pair Xilinx Kintex Ultrascale with HPSC replacing MPSoC in design

FMC+ Expansion Add-on

- Separate FMC+ HPSC expansion card can be directly added to SpaceCube v3.0



W. A. Powell, "High-Performance Spaceflight Computing (HPSC) Project Overview," Radiation Hardened Electronics Technology (RHET) Conference, Phoenix, AZ, November 5-8, 2018.

Next-Generation Data-Processing System for
Advanced SmallSat/CubeSat Applications

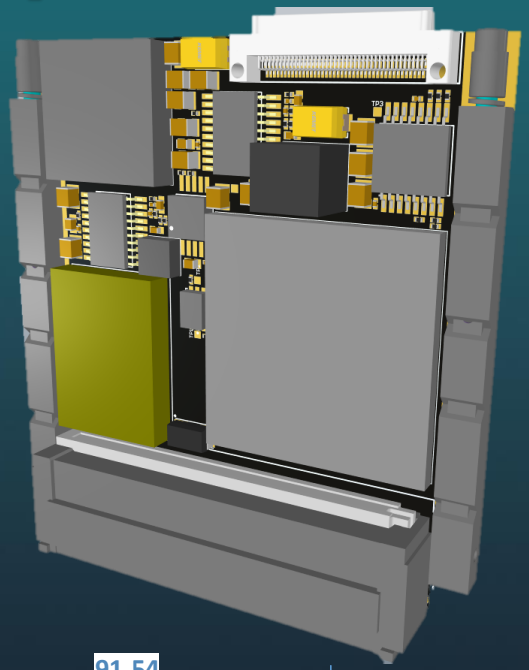
SPACECUBE V3.0 MINI, MINI-Z, AND SMALLSAT/CUBESAT SOLUTIONS

SpaceCube v3.0 Mini Specification

Overview

- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus MARES
- Evaluation board available with common interfaces for rapid prototyping and debug
- Conforms to NASA CubeSat Card Standard (CS2)

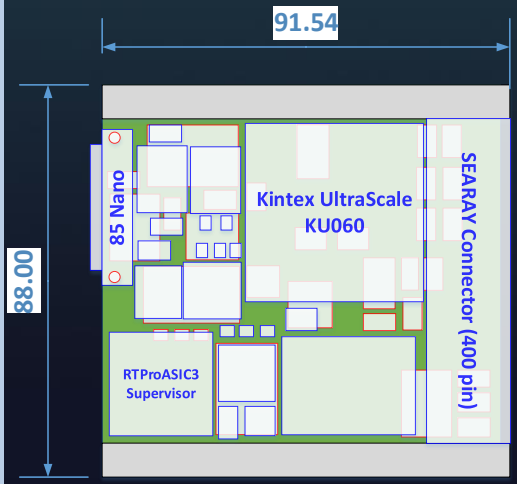
[CS]2 NASA S. goddard



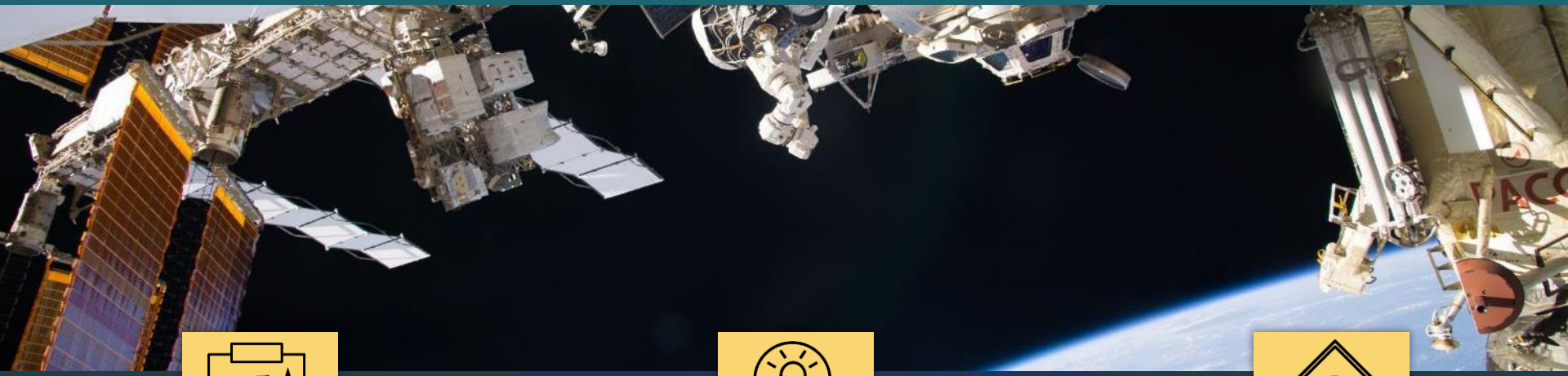
High-Level Specifications

1x Xilinx Kintex UltraScale

- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 48x 3.3V GPIO
  - SelectMAP Interface
  - (Front Panel) 24x LVDS pairs or 48x 1.8V single-ended I/O
  - (Front Panel) 8x 3.3V GPIO
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG



Goals, Motivations, Challenges



Goals

Develop reliable, high-speed hybrid processor using SpaceCube design approach to **enable next-generation instrument and CubeSat capability**

Motivations

Many commercial CubeSat processor offerings primarily target benign LEO orbits and do not strongly address **radiation concerns and parts qualification**

Need exceptional capability to support **complex applications** such as artificial intelligence

Challenges

Managing PCB area restrictions for rad-hard components, balancing cost, educating mission designers for key reliability differences

SmallSat/CubeSat Processor Challenge

Massively Expanding Commercial Market for SBCs

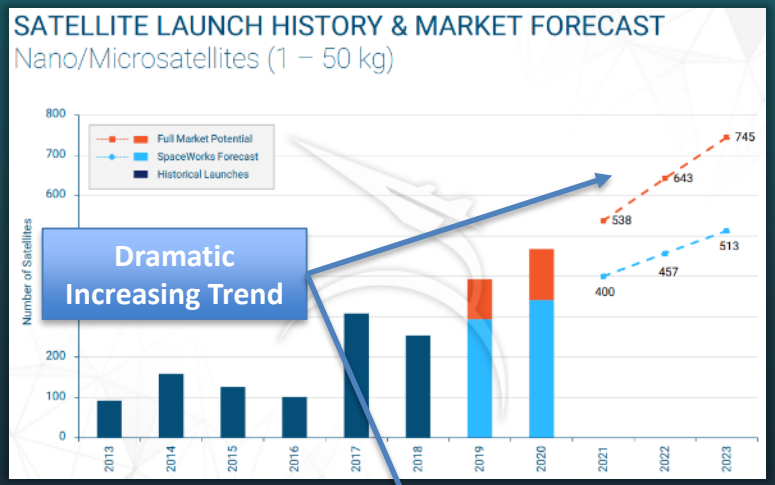
- Numerous commercial vendors in CubeSat Market (e.g. Pumpkin, Tyvak, GomSpace, ISIS, Clyde Space, etc…)

Mission Developers Seeking Commercial Hardware

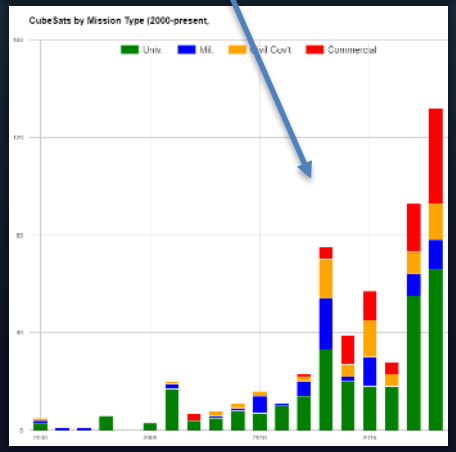
- Under pressure from cost-cap missions, and reducing costs in general
- Reduced RE for constellation mission concepts
- Attractive all-commercial solutions provided integrating several CubeSat "Kit" types of cards

Not Designed With Harsh Orbit Considerations Beyond LEO

- Many vendors have performed limited radiation testing and largely support missions in more benign LEO orbits
- Mission is radiation test approach
- Little-to-no additional radiation testing or parts qualification
- No recommendations for fault-tolerant configurations of offered SBCs

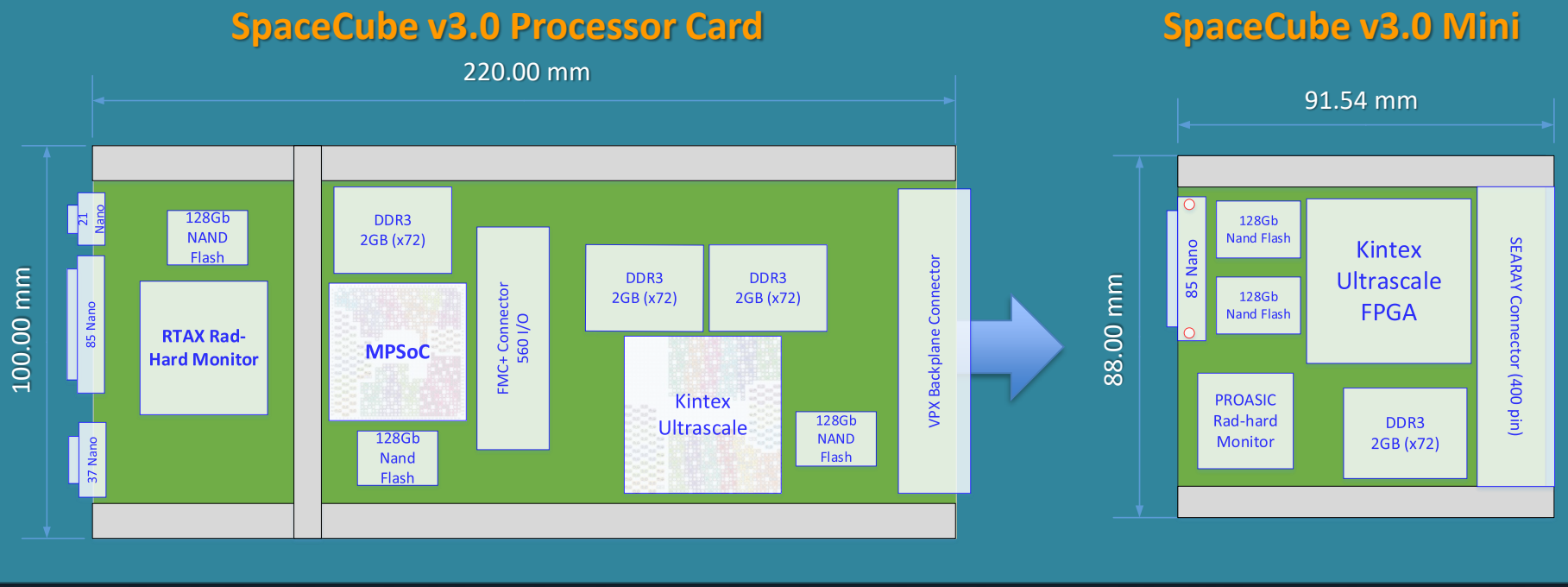


"2019 Nano/Microsatellite Forecast, 9th Edition," SpaceWorks Enterprises, Inc., Jan 2019.



M. A. Swartwout @ The CubeSat Database

Mini Design Philosophy



- **Same Approach, Smaller Size**
  SpaceCube design approach applied to smaller form-factor
- **Key Design Reused**
  Much of UltraScale design and interface remain same between cards including DDR Pinout
- **Supervision Requested**
  Radiation-hardened monitor architecture and code reusable
- **Trade in, Trade Out**
  EEE parts trades, analysis, and circuits extensively leveraged from main card design

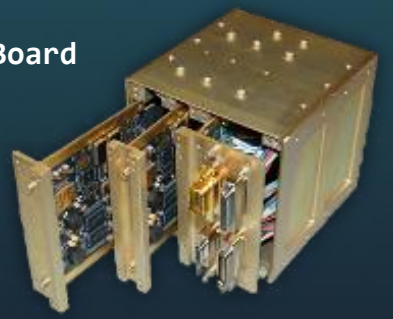
SpaceCube Mini-Z (CSPv1)

Overview of SpaceCube Mini-Z

- Collaborative development with **NSF CHREC** at University of Florida for Zynq-based 1U Board
  - Selective population scheme between commercial and rad-hard components
  - Rapid deployment prototyping
  - Convenient pre-built software packages with cFS
- **Re-Envisioned** to support quality-of-life upgrades and enable specific NASA mission needs

CSPv1 Development Board

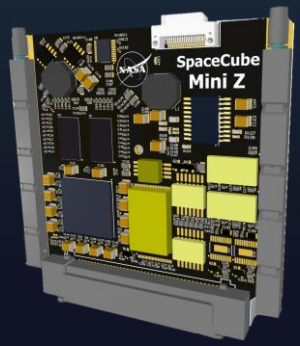
Original CSPv1



STP-H5/CSP Flight Unit

Missions and Heritage

- Launched Feb 2017 to ISS on STP-H5/CSP featuring 2 CSPv1 cards performing image processing
- Launched May 2019 to ISS on STP-H6/SSIVP featuring 5 CSPv1 for massive parallel computing
- Featured on many more…

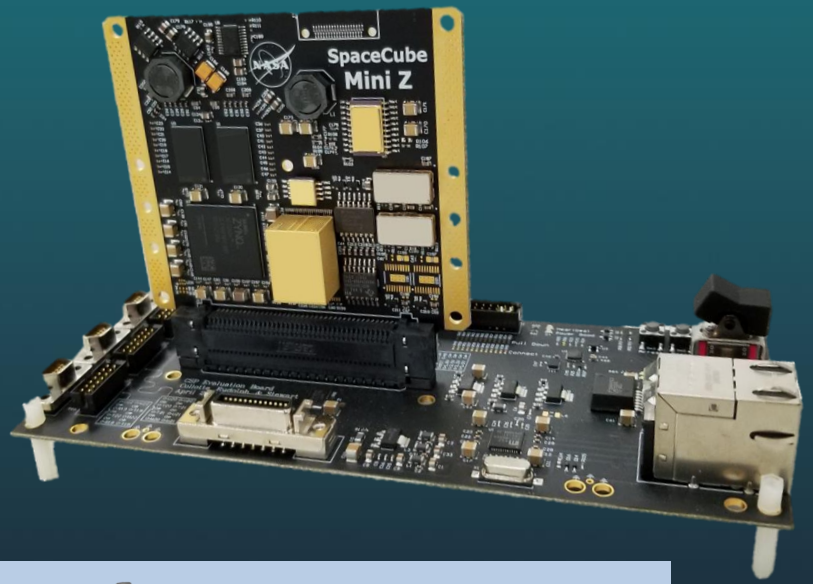


NASA SpaceCube Mini-Z

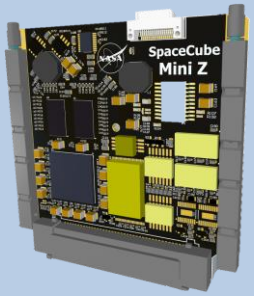
SpaceCube Mini-Z Specification

Overview

- **Re-envisioned and upgraded** version of popular CSPv1 design collaboratively developed between NASA GSFC and NSF CHREC
- Supports additional IO and form-factor changes to maintain compliance with MARES (GSFC's SmallSat bus) architecture



High-Level Specifications



Processing Capability

- Processing System (PS)
  - Xilinx Zynq-7020 SoC with Dual-Core ARM Cortex-A9 up to 667 MHz
  - 32KB I/D L1 Cache per core
  - 512KB L2 Cache
  - 256KB OCM
  - NEON SIMD Single/Double Floating Point Unit per core
- Programmable Logic (PL)
  - 85K Logic Cells
  - 53,200 LUTS /106,400 FF
  - 220 DSPs
  - 4.9Mb BRAM

Storage

- 1GB DDR3 SDRAM
- 4GB NAND Flash

IO

- MIO
  - 26 single-ended configurable IO into common interfaces such as UART, SPI, CAN, and I2C
- EMIO
  - 24 differential pairs and 12 single-ended IO
- Front Panel
  - 12 differential pairs

Dev. Tools

- CSP Evaluation Board
  - JTAG programming support
  - 10/100 Ethernet
  - MIO and EMIO breakout
  - 3 SpaceWire breakouts
  - Camera Link breakout
- USB-UART Board
  - USB to UART Converter

Physical Dimensions

- ~82g, 620 mil thick
- <1U CubeSat form factor
- 1.6-3.6W (FPGA load dependent)

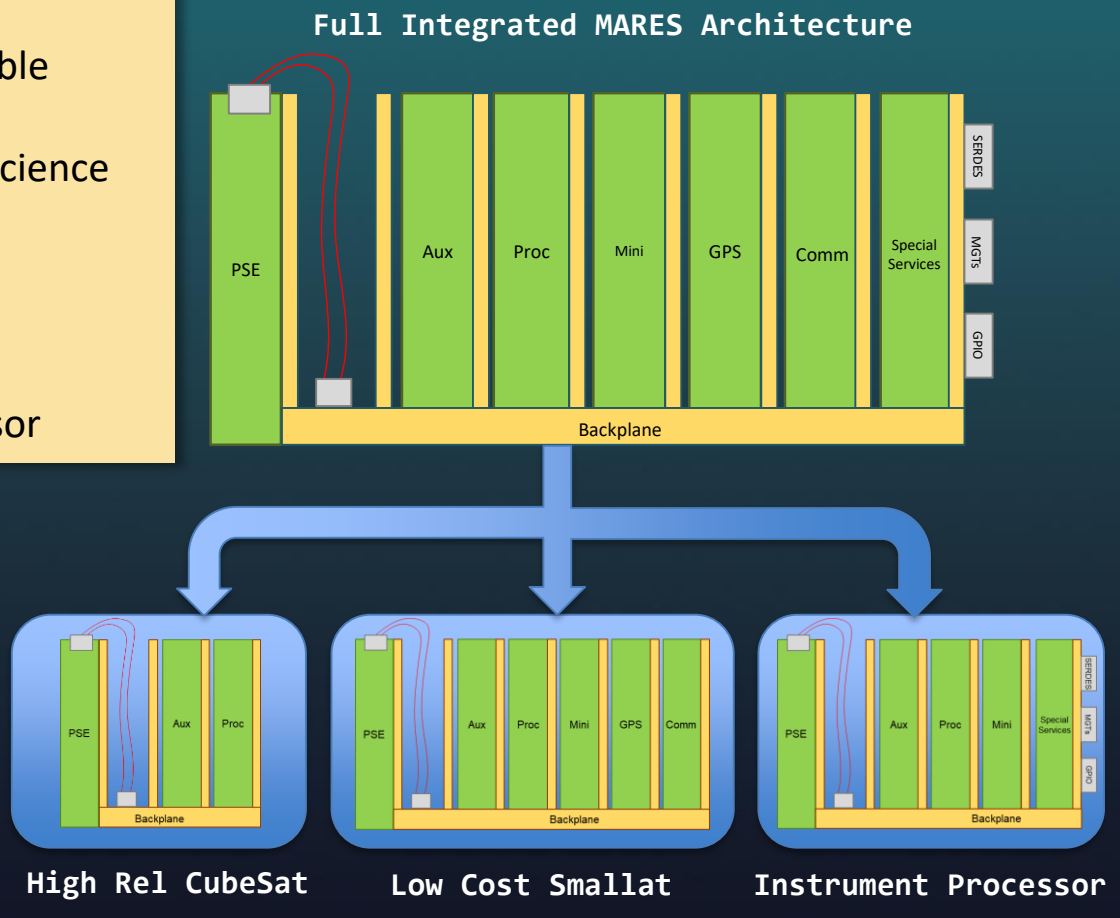
NASA MARES Architecture

Overview

- Modular Architecture for Resilient Extensible Smallsat (**MARES**)
- Enabling large volume, high-speed NASA science data for challenging environments
- Flexible architecture to support:
  - Small, inexpensive SmallSat bus
  - Reliable, powerful CubeSat bus
  - High-performance instrument processor

High-Level Specifications

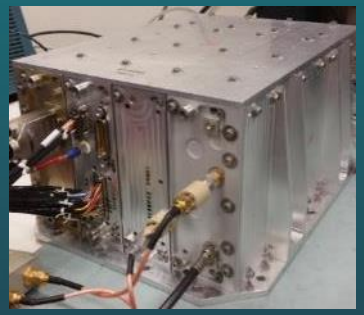
- Baseline flexible architecture to meet unique Goddard Science Missions (low power, long duration, autonomous, high data rate/volume, high radiation/temperature)
- System design includes:
  - Highly Reliable C&DH
  - SpaceCube Science Data Processing Card
  - Navigator GPS
  - Comm/Software Defined Radio
  - Power and Propulsion system



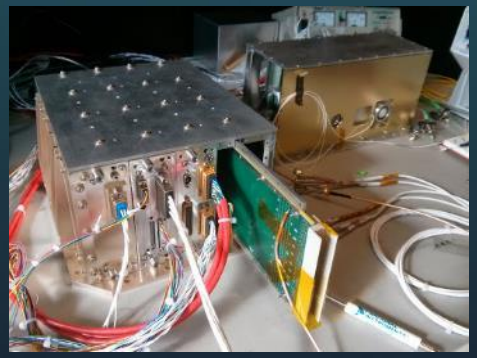
SpaceCube "Spin-offs" and Technology Infusion

SpaceCube designs have expanded to support variety of missions and projects

9 Mission-Unique SpaceCube I/O Cards in various stages of integration and test

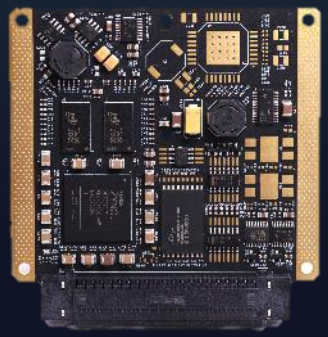


"NavCube"



GRSSLi Lidar

- SSCO Video Distribution Unit
- GRSSLi (Code 590)
- NavCube (Code 590)
- GEDI Digitizer design
- Complex PWB design using 1mm pitch CCGAs
  - TESS, GEDI, Mustang, OSIRIS-REx
- Proposal development
  - CycloPPS (Code 550 and Code 600)
  - DTN (Code 450)
  - DFB (Code 600)
  - Various others
- NICER/GEDI Ethernet Circuitry
- NSF CHREC Space Processor

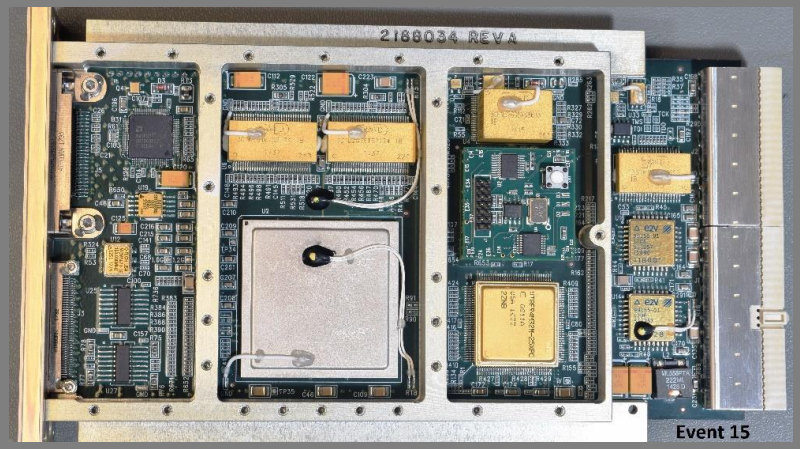


SpaceCube Commercialization

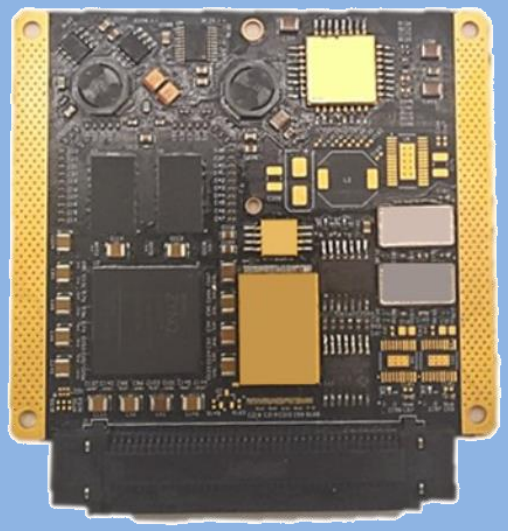
SpaceCube 2.0 → Genesis Engineering Solutions Inc. “GEN6000”

NSF CHREC Space Processor → Space Micro “CubeSat Space Processor”

GEN6000 Processor



Cubesat Space Processor



Commercialization for SpaceCube v3.0 and SpaceCube v3.0 Mini **in progress**!

CFS AND SPACECUBE SOFTWARE DEVELOPMENT KIT

Background

Within the capability-driven framework context, it is NASA's goal to **pursue commonality** across the spaceflight and supporting ground systems that use avionics while maintaining **highly scalable**, **upgradeable**, and **flexible** architectures.

NASA, "Technology Roadmaps," 2015

The need for **highly reliable, safe, and effective flight software** for CubeSats remains, but the rapid pace of change in this area has not yet produced a set of widely adopted community standards.

National Academies, "Achieving Science with CubeSats," 2016

Open source software and hardware hold a lot of promise for commercial and government spacecraft developers. Making a project open source is the first step. The **next step** is to socialize the software and **encourage developers to not only use but to contribute** back flight-proven algorithms, software modules, and hardware components.

NASA, "State of the Art of Small Spacecraft Technology," 2018

Goals, Motivations, and Challenges

- **Goal**: **Expand** and **enhance** NASA's open source flight software framework for next-generation missions
  - **Foster ecosystem** for collaboration of flight software across government, industry, and academia
  - Enable lower cost mission development by providing robust, reusable, and **verified flight software** components

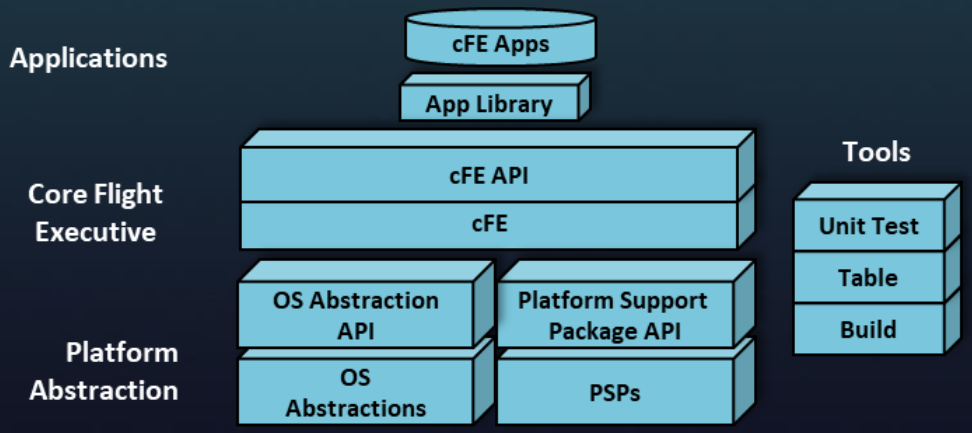
- **Motivations**: Literature highlights flight software as cross-cutting technology essential for missions
  - New adopters of cFS framework should be provided with clear documentation and **community support** starting new missions
  - Seasoned developers should be provided forum to share lessons learned and upload or discuss new compatible apps

- **Challenges**: **No organizational support or resources** to either enable or sustain cFS to provide tools, docs, or releases/updates to be "one-stop" flight software solution

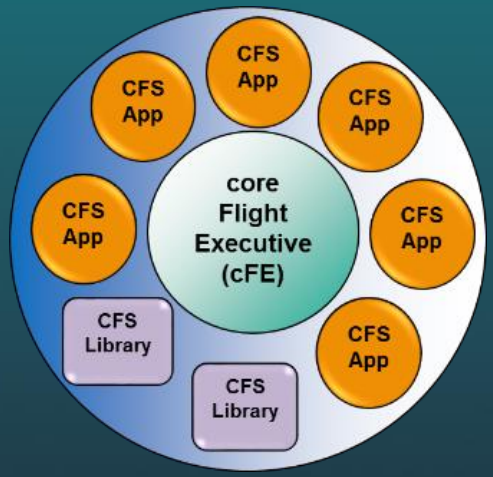
Core Flight System (cFS) Overview
What is it?

- NASA **multi-center** configuration controlled open source flight software **framework**
  - Layered architecture with standards-based interfaces
  - Provides development tools and runtime environment for user applications
  - Reusable Class A lifecycle artifacts: requirements, design, code, tests, and documents

- Framework is ported to platforms and augmented with applications to create **cFS distributions**
  - Highly reliable software with more than decade of flight heritage
  - **Worldwide community** from government, industry, and academia



Benefits of cFS
Why use it?



- **Portable**: Write once, **run anywhere**
  cFS framework has been deployed
  - Framework has been ported to many popular hardware platform/operating system platforms including MUSTANG, SpaceCube, and CSPv1
- **Open Source: 15** Goddard apps released as open source that provide common command and data handling
  - Stored command management and execution
  - Onboard data storage file management
- **Lowers Risk**: Reduces project cost and schedule risks
  - High quality **flight heritage applications**
  - Focus resources on mission-specific functionality
- Framework provides seamless application transition from technology demonstration efforts to flight projects

cFS Cost Savings

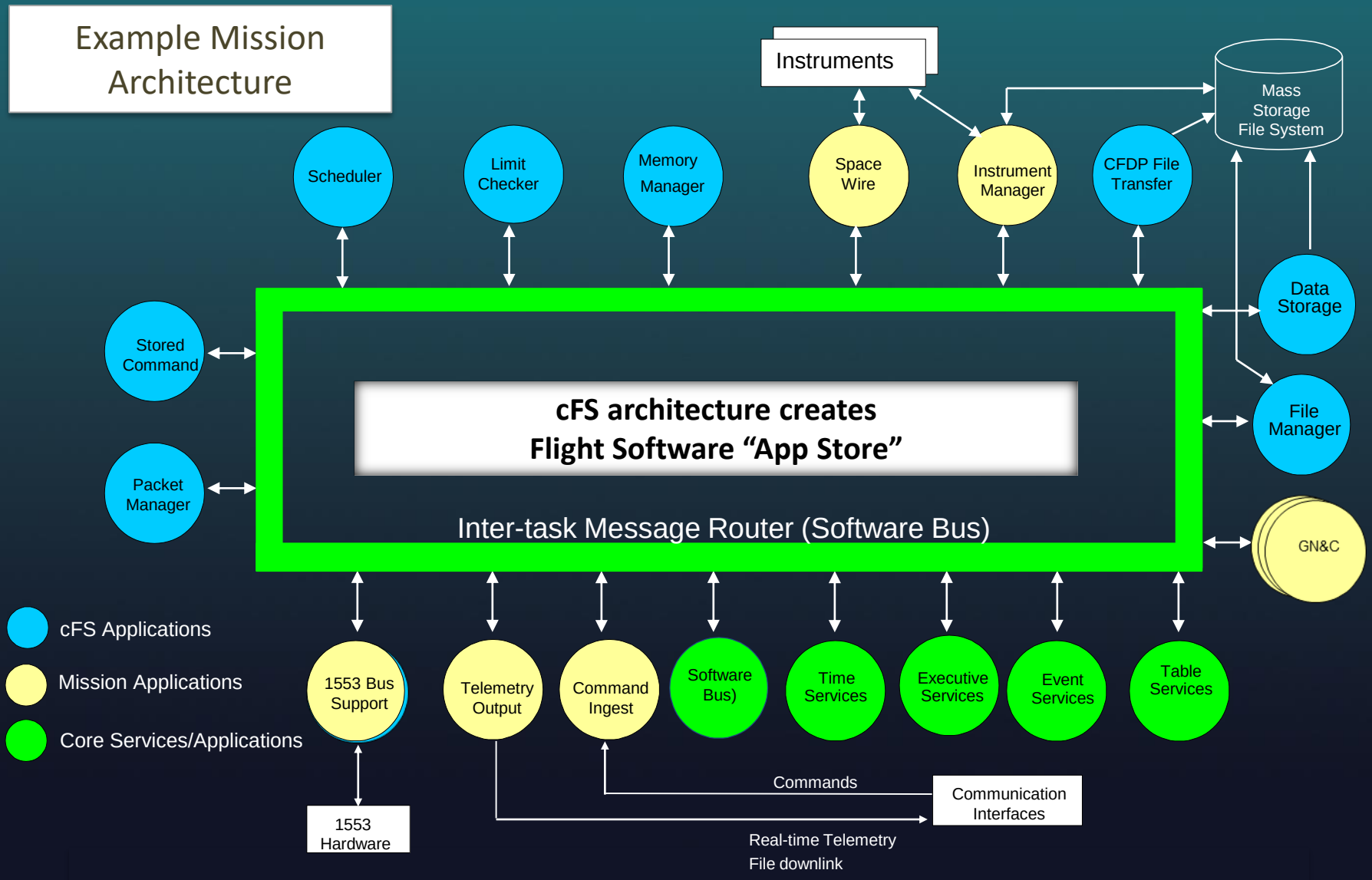
How does cFS help save costs?

Mission/ Payload Risk Class	Cost of Flight SW w/out CFS Reuse	Cost with CFS reuse (Min of 10%)	Minimum Savings (10%)	Max Savings (40%)	Notes
Class A	$30-$80+M	$27-$72M	$3-$8M	$12-$32M	Savings per mission. JSC, MSFC, KSC
Class B	$10-$30M	$9-27M	$1-3M	$4-12M	GSFC, JPL, ARC
Class C	$4-10M	$3.6-9M	$0.4-1M	$1.6-4M	ARC, GRC, LaRC
Class D	$1-4M	$0.9-3.6M	$0.1-0.4M	$0.4-1.6M	GSFC, ARC, GRC

- Estimates are based on mission costs for LRO, MMS, GPM, LADEE, LCRD, Morpheus, and current cost projections for HEO proposed missions (JSC).
- Projections are based on range of mission complexity in each Payload Risk Class
- Missions can expect to save between **10 and 40%** in software development costs

Example FSW Architecture

What are all the components of cFS?



Engaged NASA Partners

Who helps develop core cFS components?

- Johnson Space Center
  - Performed Class A certification on cFS framework on ARINC 653 in support of cFS being used on Orion backup processor
  - All Class A artifacts integrated back into framework
  - Contributed multiple open source applications and tools
- Ames Research Center
  - Created Simulink model-to-cFS application tool for LADEE
  - Allows code generated by Simulink's embedded code generator to run unmodified as cFS application
  - Enhanced by Goddard and used on NICER, GEDI, and PACE

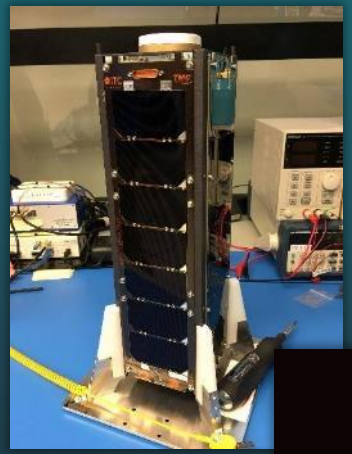
- NASA team working on standards-based command and telemetry tool chain for interoperability and ease of component integration
  - Provides infrastructure for efforts such as Lunar Orbital Platform-Gateway

cFS Community
Who uses cFS beyond NASA?

- Johns Hopkins Applied Physics Lab
  - Radiation Belt Storm Probe (2012)
  - Parker Solar Probe Plus (2018)
- Lunar Cargo Transportation and Landing by Soft Touchdown (CATALYST) program
  - All three commercial companies using cFS
  - Advancing cFS tools under CATALYST Space Act Agreement
- Space and Naval Warfare Systems Command (SPAWAR)
  - GSFC providing consultation for their CubeSats
- Air Force Research Lab (AFRL)
  - Evaluating cFS to replace their Space Plug-and-Play (SPA) system
- Universities / Academia
  - cFS used in University of Maryland Baltimore County (UMBC) curriculum
  - Routinely contacted by universities for CubeSat consultation
    - University of Pittsburgh, Capital College, Morehead State, Penn State, University of Colorado, University of South Florida, …
- International engagements include
  - Argentina, Australia, Brazil, Canada, ESA, JAXA, KARI, Taiwan

cFS Flight Heritage
What missions is cFS on?

- **ARC**
  - LADEE (2013), BioSentinel Cubesat (2018)
- **GRC**
  - SCaN testbed
- **GSFC**
  - Balloons: BITSE, OPIS
  - CubeSats: CeRes (2018), Dellingr (2017), STF-1, Small Satellite Program Office
  - ISS: GEDI, NICER (2017), RRM3, STP-6, STP-H5, STP-H6
  - Spacecraft: GPM, LRO, MMS, PACE, Restore, WFIRST
- **JPL**
  - Integrating their AMMOS Instrument Toolkit (AIT) ground system with cFS for Morehead State's Lunar IceCube project
- **JSC**
  - Orion backup computer
  - Multiple Advanced Exploration System projects
- **MSFC**
  - Transitioning iSAT CubeSat flight software to cfS
  - Providing developers for Astrobotic as part of Lunar CATALYST program



cFS Summary

- cFS is **cross-cutting** enabling technology for NASA
  - Provides framework for complicated next-gen missions
- **Widespread** domestic and international impact
  - Large community of adopters and practitioners
- Reduces mission risk with cost and schedule **savings**
  - **Reusable** flight software components across missions
  - **Validated** mission applications and core software
  - Provides more time for mission specific app development
- Potential to foster brimming flight software community
  - Easy intro. for new developers, simple to learn and setup
  - Robust to extend base framework capability to suit needs

SpaceCube Software Development Kit

SpaceCube provides software packages for mission development

SpaceCube includes support for several popular OS (Linux, RTEMS, FreeRTOS) and allows for end-to-end flatsat testing with ground station software such as Ball Aerospace's COSMOS and NASA's IRC. cFS is supported as flight software across all designs.

Ball Aerospace COSMOS

NASA SOFTWARE

NASA Open Source Core Flight System cFS

freeRTOS

RTEMS™

INTELLIGENT SOLUTIONS FOR SPACE

Why do we need this capability?

Massive Observatories with Multiple Large Instruments

- Numerous mission concept studies required multiple SpaceCube processor cards to process and compress enormous volumes of data

Unfortunately for FPGA Resources Everywhere… AI and Machine Learning

- Research shows AI/ML constructs have wide applicability for space, however, some complex models incur long execution times or massive resource overheads

Sematic Segmentation / Image Classification

- Computer Vision / Machine Learning Process learns to assign label to all pixels of image
- Parallel computations are scalable and certain accelerator sizes can only be supported on larger devices

S. Sabogal, A. D. George, and G. Crum, "ReCoN: Reconfigurable CNN Acceleration for Space Applications A Framework for Hybrid Semantic Segmentation on Hybrid SoCs," 12th Space Computing Conference, July 30 – August 1, 2019.

Adaptive Compression

- Regenerative compression technique by training neural-network codecs on satellite imagery to improve compression
- Lightweight neural network on spacecraft to encode compressed representation can be hardware accelerated

Advanced Applications Example: Semantic Segmentation

- Computer Vision / Machine Learning Process
  - Learns to assign label to all pixels of image
  - Pixels with same label share semantic characteristics
  - Output roughly resembles input
- Space Applications
  - **Science**: Earth observations and remote sensing
  - **Defense**: reconnaissance and intelligence gathering

S. Sabogal, A. D. George, and G. Crum, "ReCoN: Reconfigurable CNN Acceleration for Space Applications A Framework for Hybrid Semantic Segmentation on Hybrid SoCs," 12th Space Computing Conference, July 30 – August 1, 2019.

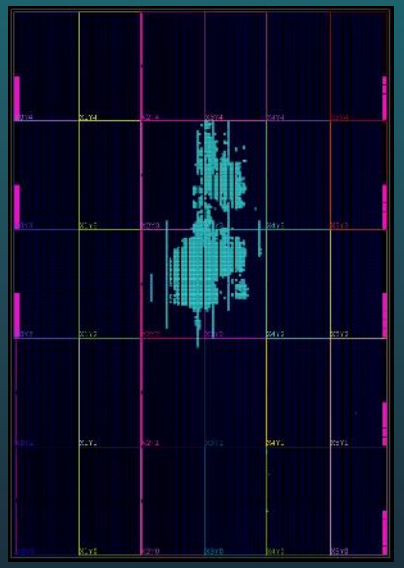
SpaceCube for Advanced Applications

Resource-Intensive Applications

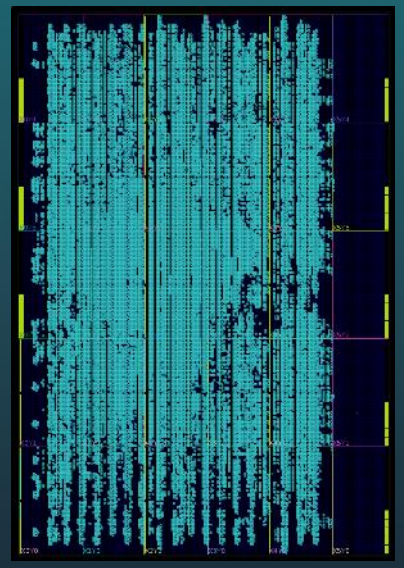
- Advanced deep-learning algorithms, such as semantic segmentation, are computationally expensive and prohibitive on traditional rad-hard processors

ReCoN (Reconfigurable CNN accelerator)

- ReCoN is designed for scalability and parameterization of CNNs and used for semantic segmentation demonstration
- Generated using Vivado High Level Synthesis (**HLS**)
- Parallel computations are scalable, and certain accelerator sizes **can only be supported on larger devices** such as Kintex UltraScale in SpaceCube Mini
- Demonstrated up to **306x improvement** in application over software baseline on SoC device featured on SCv3.0



MicroBlaze



ReCoN Accelerator

Resource Utilization of TMR Designs on KU060

Resource	MicroBlaze Stand Alone Reference	$ReCoN_{16}$
LUTs	2.41%	18.85%
CLB FF	1.19%	21.61%
BRAM/FIFO ECC (36 Kb)	6.94%	6.11%
DSP Slices	0.22%	84.64%

Deployment Configurations

- Small form factor makes SpaceCube Mini **versatile** for many use cases and multiple mission classes

Instrument Processing Unit

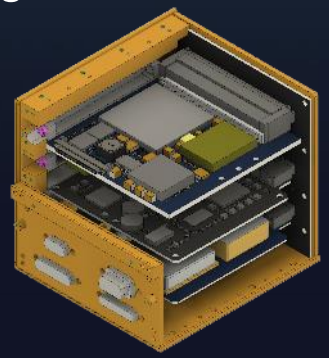
- Provides high-speed interface to instruments supporting 12 Multi-Gigabit Transceivers and over 70 LVDS pairs
- Convenient small enclosure for tight integration

High-Performance Processor

- Featured as the high-performance processor on NASA GSFC's highly reliable CubeSat Bus MARES
- Supports latest Xilinx FPGA development tools including high-level synthesis, reVISION, and Partial Reconfiguration

AI "Edge Node" Co-Processor System

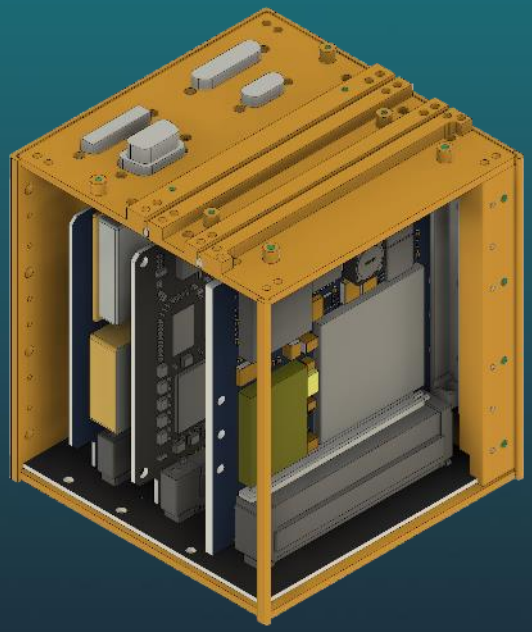
- Can combine SCv3.0 Mini with Mini-Z or Mini-Z45 to provide on-board autonomy and analysis dedicated co-processing node



AI "Edge Node" System

Artificial intelligence co-processors for on-board autonomy or analysis

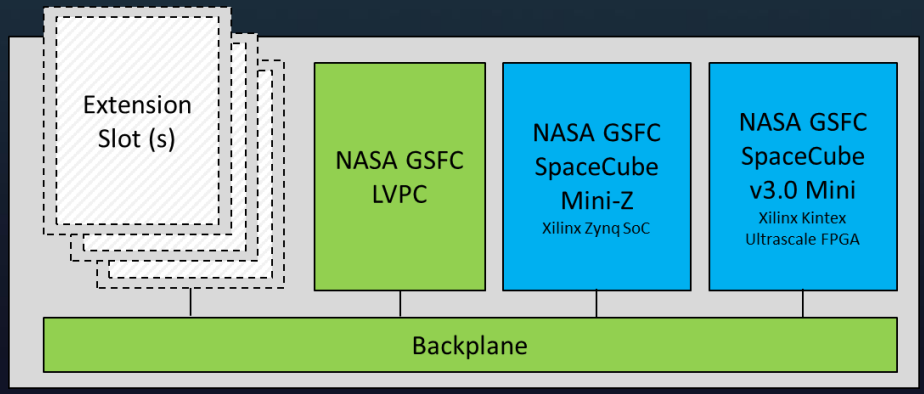
- Run machine-learning models on flight-qualified single-board computers networked together for fault tolerance, flexibility, and performance
- Currently deep learning models and applications rely on HPC resources like GPUs not broadly for spaceflight
- State-of-the-art radiation-hardened computers are **unable** to run modern neural networks
- Published research for running deep-learning models on flight systems



AI Co-Processor 1U Box

SpaceCube AI Co-Processor

- SpaceCube v3.0 Mini combined with SpaceCube Mini-Z or Mini-Z45



Expandable Design

ACADEMIC COLLABORATION

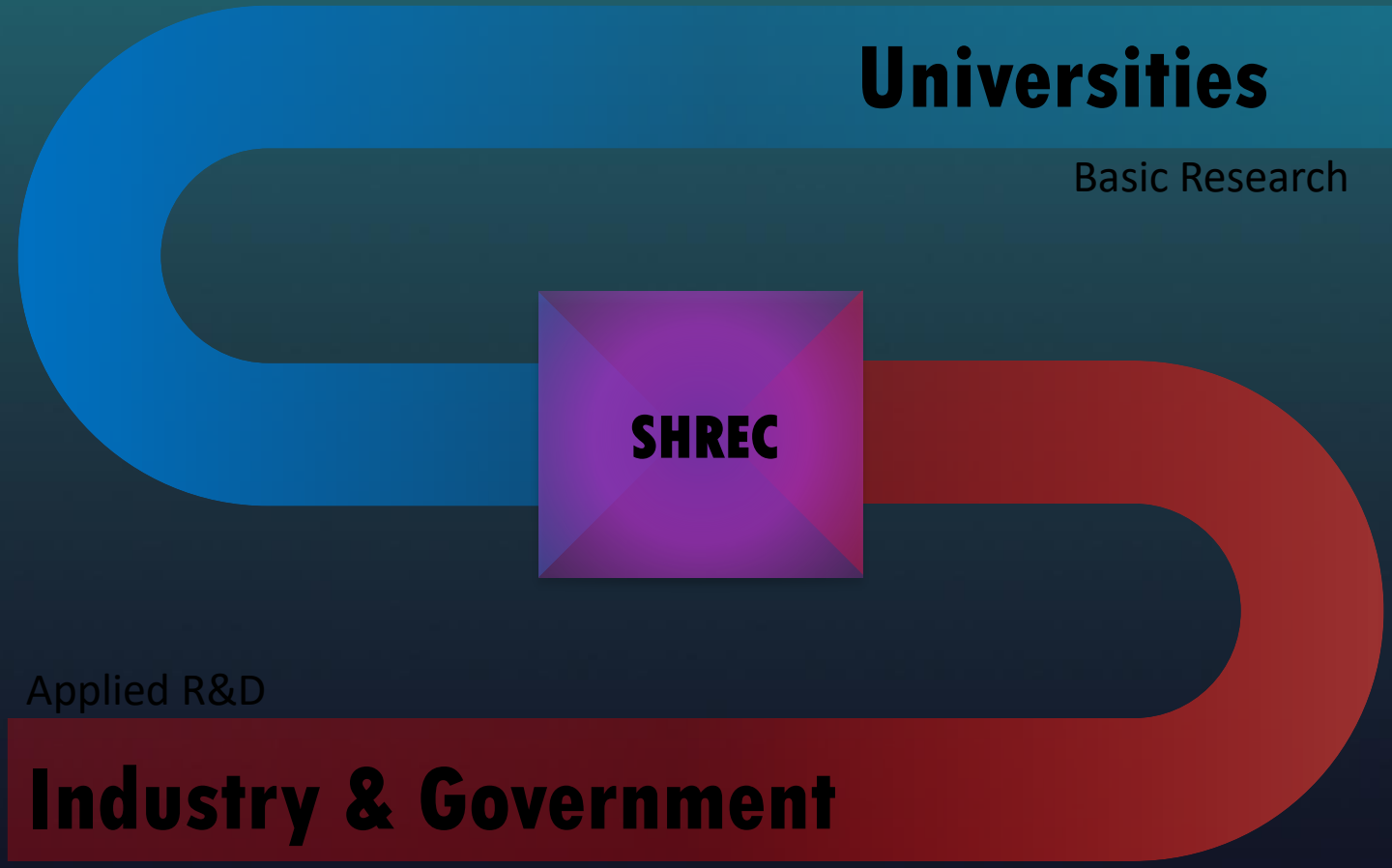
What is SHREC?

Mission-Critical Computing
NSF CENTER FOR SPACE, HIGH-PERFORMANCE, AND RESILIENT COMPUTING (SHREC)

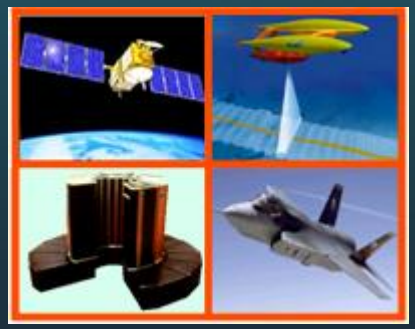
- NSF Center for Space, High-Performance, & Resilient Computing
  - Founded in Sep. 2017, replacing highly successful **NSF CHREC Center**
  - Leading ECE research groups @ four major universities
    - University of Pittsburgh (lead)
    - Brigham Young University (partner)
    - University of Florida (partner)
    - Virginia Tech (partner)

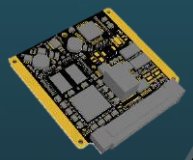
- Under auspices of **IUCRC Program** at NSF
  - Industry-University Cooperative Research Centers
    - Fostering university, agency, and industry R&D collaborations
  - SHREC is both **National Research Center and Consortium**
    - University groups serve as research base (faculty, students, staff)
    - Industry & government organizations are research partners, sponsors, collaborators, advisory board, & technology-transfer recipients

NSF Model for I/UCRC Centers



Center Mission



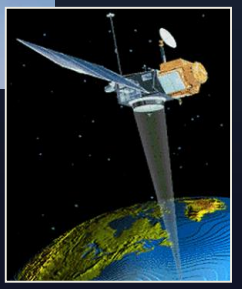


Space Computing

SHREC

High-Performance Computing

Resilient Computing



Theme: Mission-Critical Computing

Basic and applied R&D to advance S&T on advanced computing.

Many common challenges, technologies, & benefits, in terms of performance, power, adaptivity, productivity, cost, size, etc.

From architectures to applications to design concepts and tools.

From spacecraft to supercomputers!

Center Members (2019)

1. AFRL Sensors Directorate
2. AFRL Space Vehicles Directorate
3. Army Research Laboratory
4. BAE Systems
5. Ball Aerospace
6. Boeing
7. Collins Aerospace
8. Dell
9. Draper Lab
10. Emergent Space Technologies
11. Fermilab
12. Harris
13. Honeywell
14. Intel
15. L3 Space and Sensors
16. Laboratory for Physical Sciences
17. Lockheed Martin
18. Los Alamos National Laboratory
19. MIT Lincoln Laboratory
20. NASA Ames Research Center
21. NASA Goddard Space Flight Center
22. NASA IV&V Facility
23. NASA Johnson Space Center
24. NASA Kennedy Space Center
25. NASA Langley Research Center
26. National Reconnaissance Office
27. National Security Agency
28. Naval Research Laboratory
29. Raytheon
30. Sandia National Laboratories
31. Satlantis
32. Space Micro
33. Walt Disney Animation Studios

Each member funds 1 or more memberships (graduate students)

Center Membership Benefits

- **R&D breakthroughs, results, and tech transfer**
  - Solving problems selected by members
- **Expanded knowledge and insight**
  - Broader & deeper understanding in field
- **Student recruiting**
  - Ideally prepared; full-time and internship
- **Peer networking**
  - Technical interactions with other members
- **Resource leveraging**
  - Small investment (membership) reaps large ROI

NASA Partnership Benefits

- Overview: Membership funds for NSF SHREC provide substantial return on investment (ROI) providing NASA with
  - Cutting-edge research results and technology transfer
  - Extended partnerships and insight for ongoing development in industry and academia
  - Develops potential future hires and improves academic programs in NASA STEM-focus areas

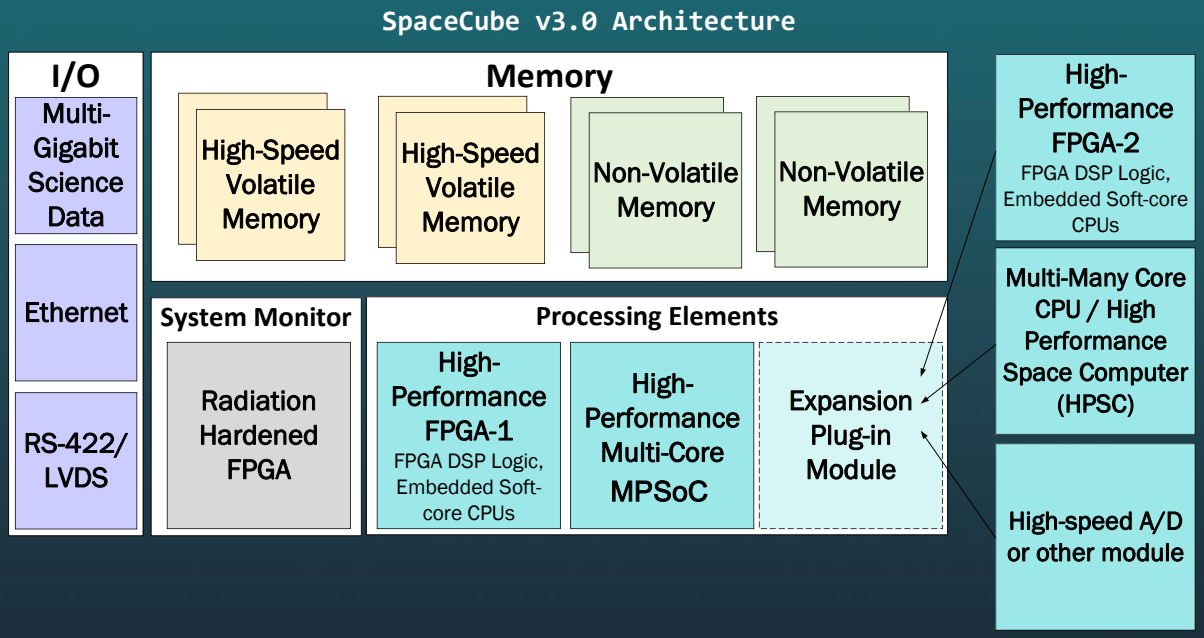
- Impact Examples
  - CHREC Space Processor (CSPv1): CSPv1 is hybrid CubeSat space processor developed by SHREC in collaboration with Code 587
  - Internships and Student Conversions: Several SHREC students have interned at Goddard and performed research that has led to academic publications
  - Radiation Testing: Performs many radiation tests of Xilinx FPGAs and fault-tolerant architectures collaborating with Los Alamos National Laboratory (LANL) and the Xilinx Radiation Testing Consortium (XRTC)
  - Tool Development: Hardware fault injector to simulate upsets in FPGAs, as well as, an open source Triple Modular Redundancy (TMR) tool to be used to create reliable VHDL designs

DESIGN SPECIFICATIONS

SpaceCube v3.0 Processor Card

Overview

- **Next-Generation** SpaceCube Design
- Prototype demonstration Q1 2020
- **3U SpaceVPX** Form-Factor
- Ultimate goal of using High-Performance Spaceflight Computing (**HPSC**) paired with the high-performance FPGA
  - HPSC will not be ready in time for the prototype design
  - Special FMC+ Expansion Slot



High-Level Specifications

1x Xilinx Kintex UltraScale

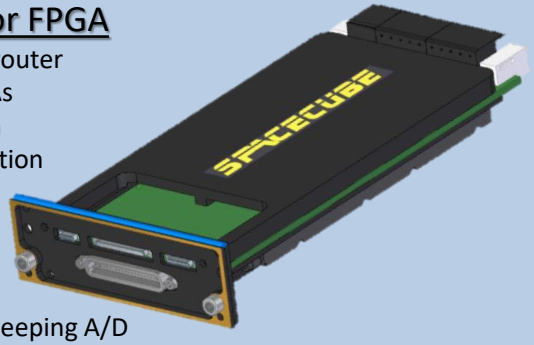
- 2x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - 24x Multi-Gigabit Transceivers
  - 75x LVDS pairs or 150x 1.8V single-ended I/O
  - 38x 3.3V single-ended I/O,
  - 4x RS-422/LVDS/SPW
- Debug Interfaces
  - 2x RS-422 UART / JTAG

1x Xilinx Zynq MPSoC

- Quad-core Arm Cortex-A53 processor (1.3GHz)
- Dual Arm R5 processor (533MHz)
- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - I2C/CAN/GigE/SPIO/GPIO/SPW
  - 12x Multi-Gigabit Transceivers
- Debug Interfaces
  - 10/100/1000 Ethernet (non-flight)
  - 2x RS-422 UART / JTAG

Rad-Hard Monitor FPGA

- Internal SpaceWire router between Xilinx FPGAs
- 1x 16GB NAND Flash
- Scrubbing/configuration of Kintex FPGA
- Power sequencing
- External Interfaces
  - SpaceWire
- 2x 8-channel housekeeping A/D with current monitoring

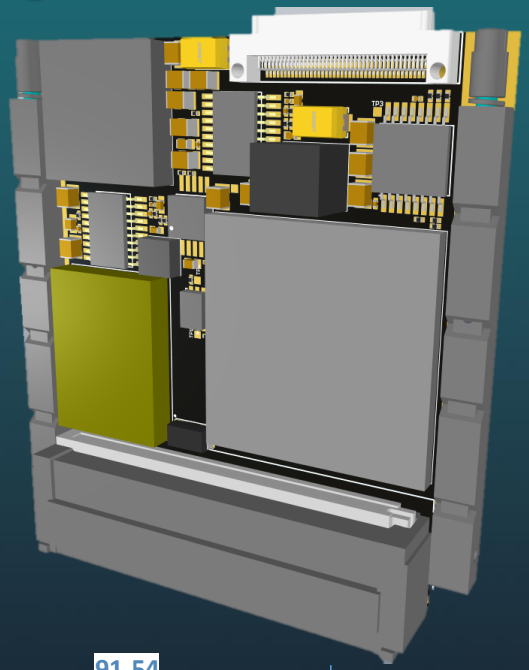


SpaceCube v3.0 Mini Specification

Overview

- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus MARES
- Evaluation board available with common interfaces for rapid prototyping and debug
- Conforms to NASA CubeSat Card Standard (CS2)

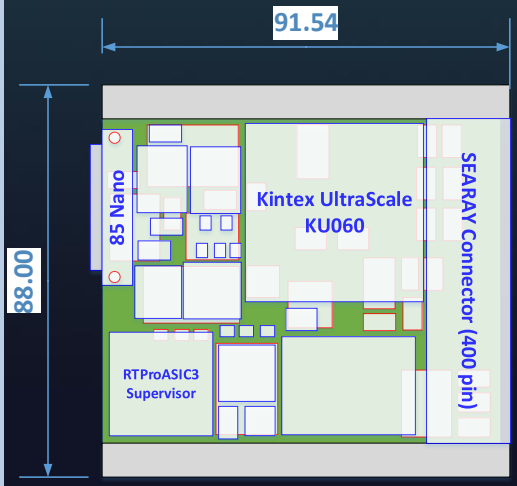
[CS]2 NASA S. goddard



High-Level Specifications

1x Xilinx Kintex UltraScale

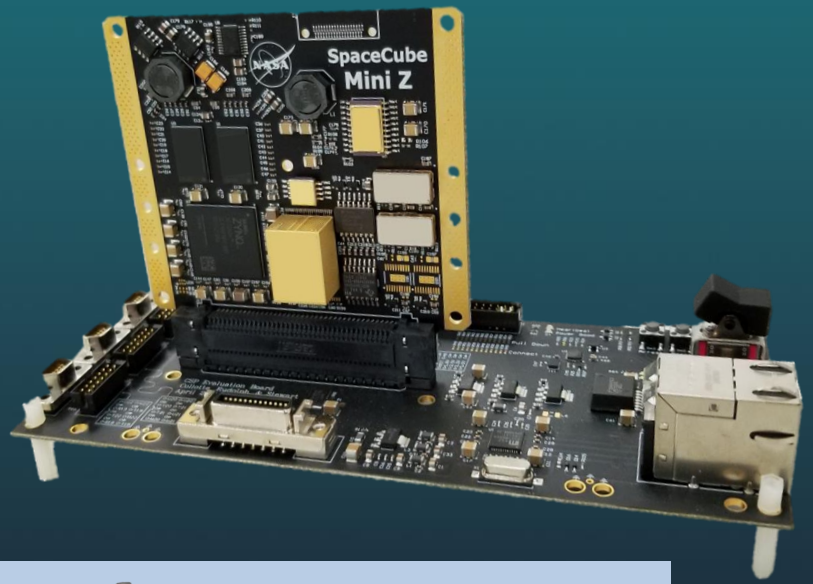
- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 48x 3.3V GPIO
  - SelectMAP Interface
  - (Front Panel) 24x LVDS pairs or 48x 1.8V single-ended I/O
  - (Front Panel) 8x 3.3V GPIO
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG



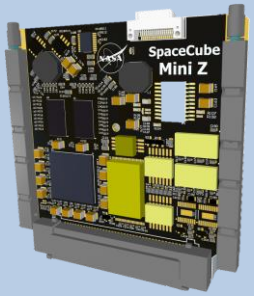
SpaceCube Mini-Z Specification

Overview

- **Re-envisioned and upgraded** version of popular CSPv1 design collaboratively developed between NASA GSFC and NSF CHREC
- Supports additional IO and form-factor changes to maintain compliance with MARES (GSFC's SmallSat bus) architecture



High-Level Specifications



Processing Capability

- Processing System (PS)
  - Xilinx Zynq-7020 SoC with Dual-Core ARM Cortex-A9 up to 667 MHz
  - 32KB I/D L1 Cache per core
  - 512KB L2 Cache
  - 256KB OCM
  - NEON SIMD Single/Double Floating Point Unit per core
- Programmable Logic (PL)
  - 85K Logic Cells
  - 53,200 LUTS /106,400 FF
  - 220 DSPs
  - 4.9Mb BRAM

Storage

- 1GB DDR3 SDRAM
- 4GB NAND Flash

IO

- MIO
  - 26 single-ended configurable IO into common interfaces such as UART, SPI, CAN, and I2C
- EMIO
  - 24 differential pairs and 12 single-ended IO
- Front Panel
  - 12 differential pairs

Dev. Tools

- CSP Evaluation Board
  - JTAG programming support
  - 10/100 Ethernet
  - MIO and EMIO breakout
  - 3 SpaceWire breakouts
  - Camera Link breakout
- USB-UART Board
  - USB to UART Converter

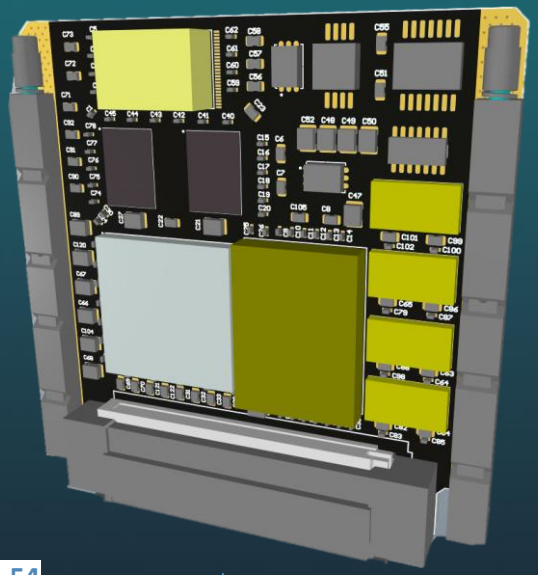
Physical Dimensions

- ~82g, 620 mil thick
- <1U CubeSat form factor
- 1.6-3.6W (FPGA load dependent)

SpaceCube Mini-Z45 Specification

Overview

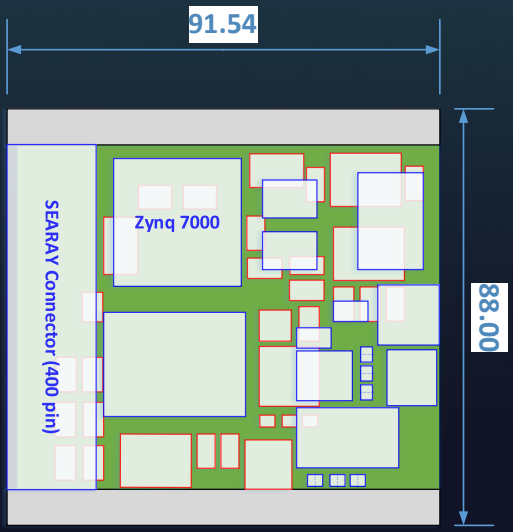
- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0 Mini and Mini-Z designs
- **Upgrade** capabilities of Mini-Z (CSPv1) to provide MGTs, more FPGA resources and more memory



High-Level Specifications

1x Xilinx Zynq 7000 System-on-Chip

- 1GB DDR3 SDRAM for ARM Processors
- 2GB DDR3 SDRAM for Programmable Logic
- 16GB NAND Flash
- Radiation-Hardened Watchdog
- External Interfaces
  - 8x Multi-Gigabit Transceivers
  - 31x LVDS pairs or 62x single-ended I/O (voltage selectable)
  - 28x Single-ended PS MIO
- Debug Interfaces
  - 1x RS-422 UART (external transceivers)
  - JTAG



Conclusion

*SpaceCube is a **MISSION ENABLING** technology*

Delivers exceptional computing power in number of form factors

Cross-cutting technology for Comm/Nav, Earth and Space Science, Planetary, and Exploration missions

Being reconfigurable equals BIG SAVINGS

Past research / missions have proven viability

Designs support AI applications for autonomy and analysis onboard

Successful technology transfer to industry through commercialization

SpaceCube Publications

- A. Geist, C. Brewer, M. Davis, N. Franconi, S. Heyward, T. Wise G. Crum, D. Petrick, R. Ripley, C. Wilson, and T. Flatley, “SpaceCube v3.0 NASA Next-Generation High-Performance Processor for Science Applications,” 33rd Annual AIAA/USU Conf. on Small Satellites, SSC19-XII-02, Logan, UT, August 3-8, 2019.
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- A. Schmidt, G. Weisz, M. French, T. Flatley, C. Villalpando, “SpaceCubeX: A framework for evaluating hybrid multi-core CPU/FPGA/DSP architectures,” IEEE Aerospace Conference, Big Sky, MT, March 4-11, 2017.
- D. Petrick, N. Gill, M. Hassouneh R. Stone, L. Winternitz, L. Thomas, M. Davis, P. Sparacino, and T. Flatley, “Adapting the SpaceCube v2.0 data processing system for mission-unique application requirements,” IEEE Aerospace Conference, Big Sky, MT, June 15-18, 2015.
- T. Flatley, “Keynote 2 — SpaceCube — A family of reconfigurable hybrid on-board science data processors,” International Conference on ReConFigurable Computing and FPGAs (ReConFig14), Cancun, Mexico, Dec 8-10, 2014.
- D. Petrick, A. Geist, D. Albaijes, M. Davis, P. Sparacino, G. Crum, R. Ripley, J. Boblitt, and T. Flatley, “SpaceCube v2.0 space flight hybrid reconfigurable data processing system,” IEEE Aerospace Conference, Big Sky, MT, March 1-8, 2014.
- D. Petrick, D. Espinosa, R. Ripley, G. Crum, A. Geist, and T. Flatley, “Adapting the reconfigurable spacecube processing system for multiple mission applications,” IEEE Aerospace Conference, Big Sky, MT, March 1-8, 2014.
- T. Flatley, “Keynote address I: SpaceCube: A family of reconfigurable hybrid on-board science data processors,” NASA/ESA Conference on Adaptive Hardware and Systems (AHS), June 25-28, 2012.
- M. Lin, T. Flatley, A. Geist, and D. Petrick, “NASA GSFC Development of the SpaceCube Mini,” 25th Annual AIAA/USU Conf. on Small Satellites, SSC11-X-11, Logan, UT, August 8-11, 2011.

SmallSat / CubeSat Publications

- S. Sabogal, P. Gauvin, B. Shea, D. Sabogal, A. Gillette, C. Wilson, A. D. George, G. Crum, and T. Flatley, "Spacecraft Supercomputing Experiment for STP-H6," 31st Annual AIAA/USU Conf. on Small Satellites, SSC17-XIII-02, Logan, UT, Aug 5-10, 2017.
- C. Wilson, J. MacKinnon, P. Gauvin, S. Sabogal, A. D. George, G. Crum, T. Flatley, "µCSP: A Diminutive, Hybrid, Space Processor for Smart Modules and CubeSats," 30th Annual AIAA/USU Conf. on Small Satellites, SSC16-X-4, Logan, UT, August 6-11, 2016.
- C. Wilson, J. Stewart, P. Gauvin, J. MacKinnon, J. Coole, J. Urriste, A. D. George, G. Crum, A. Wilson, and M. Wirthlin, "CSP Hybrid Space Computing for STP-H5/ISEM on ISS," 29th Annual AIAA/USU Conf. on Small Satellites, SSC15-III-10, Logan, UT, August 8-13, 2015.
- B. LaMeres, S. Harkness, M. Handley, P. Moholt, C. Julien, T. Kaiser, D. Klumpar, K. Mashburn, L. Springer, G. Crum, "RadSat – Radiation Tolerant SmallSat Computer System, "29th Annual AIAA/USU Conf. on Small Satellites, SSC15-X-8, Logan, UT, August 8-13, 2015.
- S. Altunc, O. Kegege, S. Bundick, H. Shaw, S. Schaire, G. Bussey, G. Crum, J. Burke, S. Palo, D. O'Conor, "X-band CubeSat Communication System Demonstration," 29th Annual AIAA/USU Conf. on Small Satellites, SSC15-IV-8, Logan, UT, August 8-13, 2015
- D. Rudolph, C. Wilson, J. Stewart, P. Gauvin, G. Crum, A. D. George, M. Wirthlin, H. Lam, "CSP: A Multifaceted Hybrid System for Space Computing," Proc. of 28th Annual AIAA/USU Conference on Small Satellites, SSC14-III-3, Logan, UT, August 2-7, 2014.
- S. Palo, D. O'Connor, E. DeVito, R. Kohnert, G. Crum, S. Altune, "Expanding CubeSat Capabilities with a Low Cost Transceiver," Proc. of 28th Annual AIAA/USU Conference on Small Satellites, SSC14-IX-1, Logan, UT, August 2-7, 2014.

AI/ML Publications

- J. Goodwill, D. Wilson, S. Sabogal, C. Wilson and A. D. George, “Adaptively Lossy Image Compression for Onboard Processing,” IEEE Aerospace, Big Sky, MT, Mar 7 - Mar 14, 2020.
- S. Sabogal, A. D. George, and G. Crum, “ReCoN: Reconfigurable CNN Acceleration for Space Applications A Framework for Hybrid Semantic Segmentation on Hybrid SoCs,” 12th Space Computing Conference, July 30 – August 1, 2019.
- J. Kelvey, “New Eyes on Wildfires,” EOS, 100, April 30, 2019. https://doi.org/10.1029/2019EO121485
- J. Manning, E. Gretok, B. Ramesh, C. Wilson, A. D. George, J. MacKinnon, G. Crum, “Machine-Learning Space Applications on SmallSat Platforms with TensorFlow,” 32nd Annual AIAA/USU Conference on Small Satellites, SSC18-WKVII-03, Logan, UT, Aug 4-9, 2018.

Acronyms

Acronym	Definition
BL-TMR	BYU-LANL TMR
cFE	Core Flight Executive
cFS	Core Flight System
CHREC	Center for High-performance Reconfigurable Computing
CPU	Central Processing Unit
CSP	CHREC/CubeSat Space Processor
DSP	Digital Signal Processor
ELC	ExPRESS Logistics Carrier
EM	Engineering Model
FF	Flip-Flop
FLT	Flight
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GMSEC	Goddard Mission Services Evolution Center
GOPS	Giga-Operations Per Second
ISA	Instruction Set Architecture
LEO	low-Earth Orbit
MGT	Multi-Gigabit Transceiver
MIPS	Million instructions per second
NSF	National Science Foundation
ORS	Operationally Responsive Space
PCB	Printed Circuit Board
RE	Recuring Engineering
SBC	Single-Board Computer
SEL	Single-Event Latchup
SEM	Soft Error Mitigation
SSIVP	Spacecraft Supercomputing for Image and Video Processing
STP-Hx	Space Test Program Houston
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TRL	Technology Readiness Level
UVSC	Ultraviolet Spectro-Coronagraph

Thank you! Questions?

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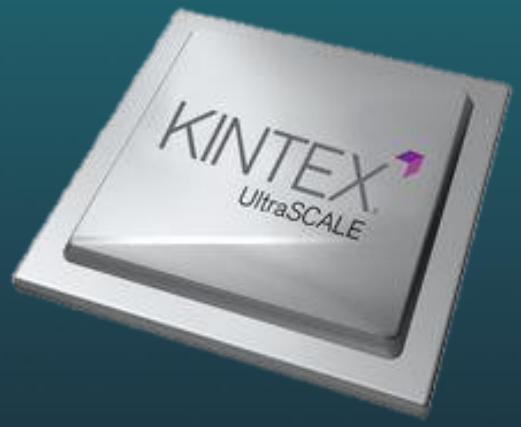
BACKUP

Xilinx Kintex UltraScale XQRKU060

- First 20 nm FPGA for Space
  - Designed for SEU mitigation (>40 patents)
  - Deploys same commercial silicon mask set
  - Uses Vivado UltraFast Development
- Ruggedized 1509 CCGA
  - 40 mm x 40mm package
  - Footprint compatible A1517
- Product Space Test Flows
  - B-Flow (QML-Q Equiv.) and Y-Flow (QML-Y Compliant)
- Commercial Radiation Testing Results
  - Improved Xsect compared to 7 series
  - No observed classical SEL signatures



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Berg, M., Kim, H., Phan, A., Seidleck, C., Label, K., and M. Campola, "Xilinx Kintex-UltraScale Field Programmable Gate Array Single Event Effects (SEE) Heavy-ion Test Report," NASA Electronic Parts and Packaging, 2017.

Fault-Tolerant Soft-Core Processing

Xilinx TMR MicroBlaze[1]

- Built-in Xilinx TMR solution for newer FPGAs
- Includes TMR SEM IP Core
- Vivado IP integrator for easy project creation

BL-TMR MicroBlaze[2]

- BYU-LANL TMR Tool (BL-TMR) provides automated TMR application
- Fault Injection on MicroBlaze performed for SpaceCube v2.0

BL-TMR RISC-V[3]

- RISC-V is a promising new ISA processor gaining popularity for Intel and Xilinx FPGAs
- Neutron radiation test of Taiga RISC-V
- 27% decrease in operational frequency, for 33x improvement in cross section

Resource Utilization of TMR Designs on KU040

Resource	Unmitigated MicroBlaze	Xilinx TMR MicroBlaze	BL-TMR MicroBlaze	BL-TMR RISC-V[3]
LUTs	3.29%	9.81%	15.58%	4.48 %
CLB FF	1.63%	4.77%	4.89%	0.6 %
BRAM/FIFO ECC (36 Kb)	12.50%	37.50%	37.50%	3.0 %
DSP Slices	0.31%	0.94%	0.94%	0.6 %
FMax	-----	0.95x	0.88x	0.73x

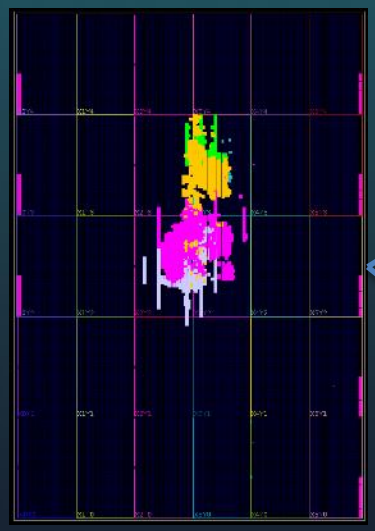
BL-TMR v6.3, MicroBlaze v11, 32-bit 5-stage, FPU, 32 Kb I/D, Vivado 2019.1,

[1]Microblaze Triple Modular Redundancy (TMR) Subsystem v1.0, https://www:xilinx:com/support/documentation/ip documentation/tmr/v1 0/pg268-tmr:pdf, Xilinx, 10 2018.

[2]http://reliability.ee.byu.edu/edif/

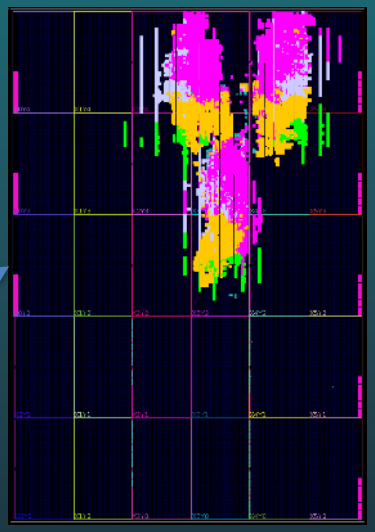
[3]A. Wilson and M. Wirthlin, "Neutron Radiation Testing of Fault Tolerant RISC-V Soft Processors on Xilinx SRAM-based FPGAs," 12th Space Computing Conference, July 30 – August 1, 2019.

TMR Floorplan Design on KU060

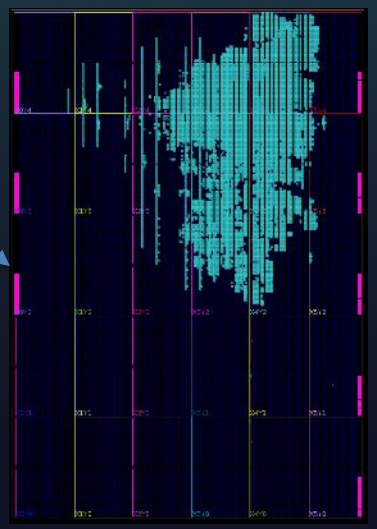


Unmitigated MicroBlaze

Different Granularity of TMR



Xilinx TMR MicroBlaze



BL-TMR MicroBlaze

- Microblaze
- Interconnects/AXI
- Caches
- Local memory

BL-TMR tool completely flattens design and removes hierarchical information about the design