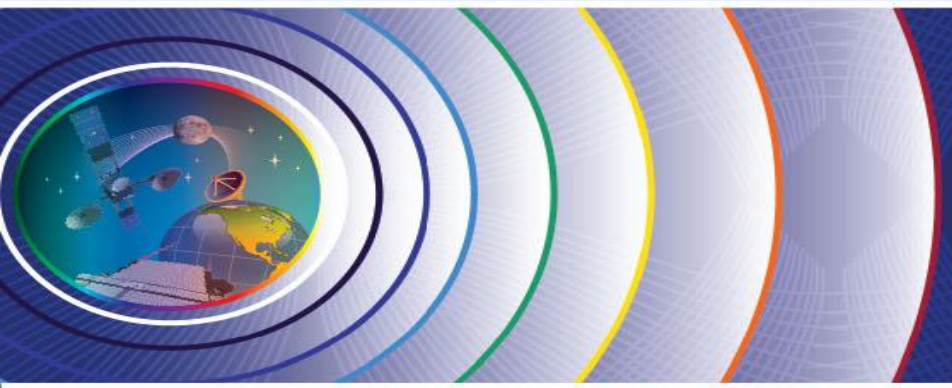


GSFC Annual SCaN Technology Review

November 5th, 2019

SpaceCube On-Board Processor Update

Dr. Christopher Wilson – Science Data Processing Branch/587

Outline

I. Background

II. Introduction

III. Roadmap

IV. FY19 Accomplishments and Key Highlights

V. Infusion

VI. Challenges

VII. Ongoing and Future Work

VIII. Conclusion

Background

Challenge

The next generation of NASA science and exploration missions will require "order of magnitude" improvements in on-board computing power …

Mission Enabling Science Algorithms & Applications

- Real-time Sensing and Control
- On-Board Data Volume Reduction
- Real-time Image Processing
- Autonomous Operations
- On-Board Product Generation
- Real-time Event / Feature Detection
- On-Board Classification
- Real-time "Situational Awareness"
- "Intelligent Instrument" Data Selection / Compression
- Real-time Calibration / Correction
- Inter-platform Collaboration

Background (continued)

Our Approach

01 The traditional path of developing radiation-hardened flight processor **will not work** … they are always one or two generations behind

02 Use latest radiation-tolerant* processing elements to achieve **massive improvement** in computing performance per Watt (for reduced size/weight/power)

03 Accept that radiation-induced upsets may happen occasionally and just deal with them appropriately … any level of reliability can be achieved via **smart system design!**

***Radiation tolerant – susceptible to radiation induced upsets (bit flips) but not radiation induced destructive failures (latch-up)**

Our Solution

SpaceCube

A family of NASA developed space processors that established a **hybrid-processing approach** combining radiation-hardened and commercial components while emphasizing a novel architecture **harmonizing** the best capabilities of CPUs, DSPs, and FPGAs

High-performance reconfigurable science / mission data processor based on Xilinx FPGAs

- Hybrid processing - algorithm profiling and partitioning to CPU, DSP, and FPGA logic
- Integrated “radiation upset mitigation” techniques
- SpaceCube “core software” infrastructure (SCSDK) – Example (cFE/cFS and “SpaceCube Linux” with Xenomai)
- Small “critical function” manager/watchdog
- Standard high-speed (multi-Gbps) interfaces

SpaceCube v1.0

SpaceCube is Hybrid Processing…

Introduction (continued)

Closing the gap with commercial processors while retaining high reliability

- **57+ Xilinx device-years on orbit**
- **26 Xilinx FPGAs in space to date (2019)**
- **11 systems in space to date (2019)**

SpaceCube is Mission Enabling…

SpaceCube v1.0

STS-125, MISSE-7, STP-H4, STP-H5, STP-H6

SpaceCube v1.5

SMART (ORS)

SpaceCube v2.0-EM

STP-H4, STP-H5

SpaceCube v2.0-FLT

RRM3, STP-H6 (NavCube)

SpaceCube v2.0 Mini

STP-H5, UVSC-GEO

Introduction: Reconfigurability

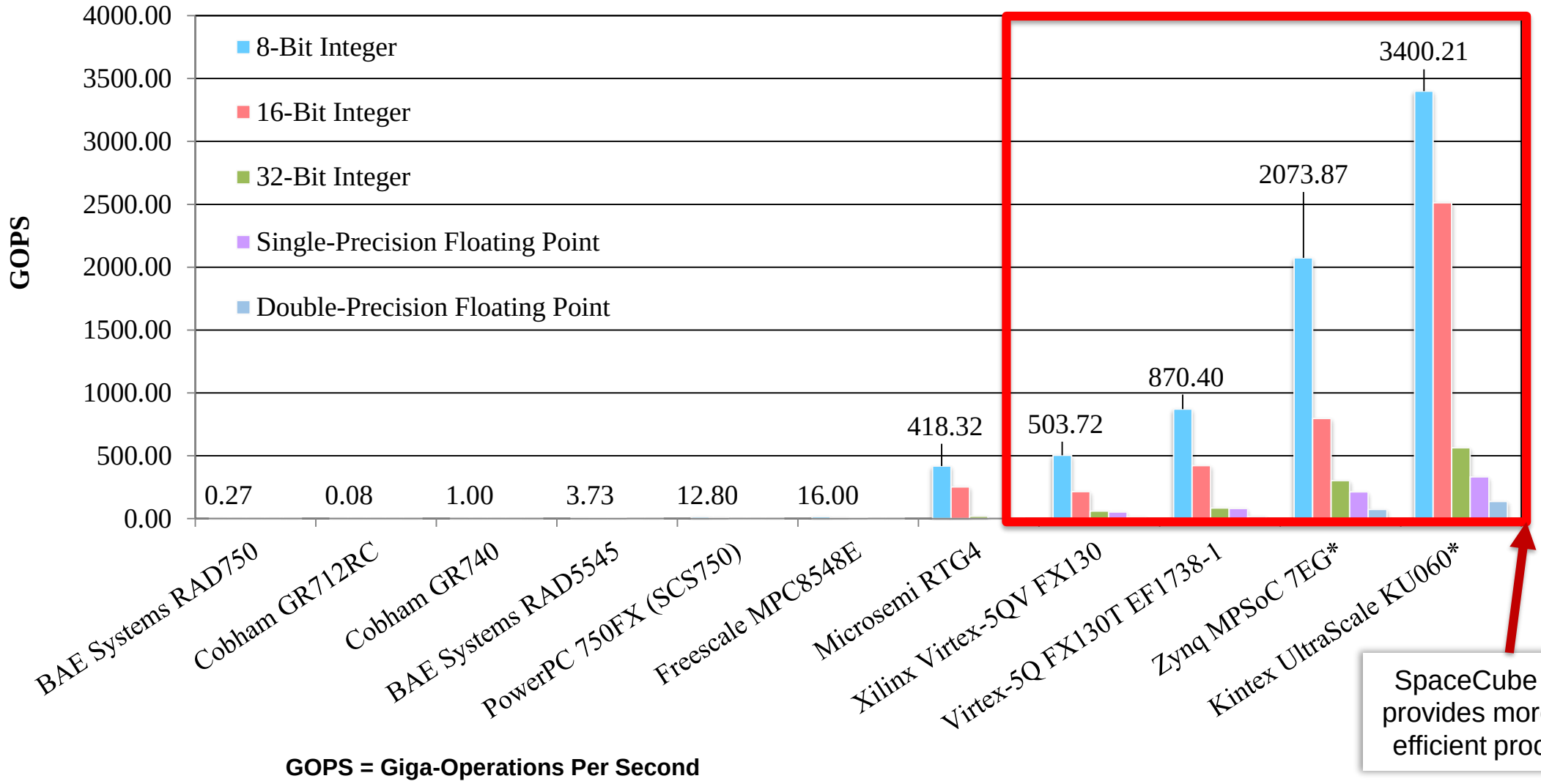
Being Reconfigurable …
… equals BIG SAVINGS (both time and money)

During mission development and testing
- Design changes without PCB changes
- "Late" fixes without breaking integration

During mission operations
- On-orbit hybrid algorithm updates
- Adaptive processing modes
  - hi-reliability vs. high-performance
  - intelligently adapt to current environment

From mission to mission
- Same avionics reconfigured for new mission

Introduction: Device Comparisons



SpaceCube Family provides more power efficient processing

GOPS = Giga-Operations Per Second

*UltraScale results are an estimate based off of existing data, new metrics are in progress but not currently available

T. M. Lovelly and A.D. George, "Comparative Analysis of Present and Future Space-Grade Processors with Device Metrics," AIAA Journal of Aerospace Information Systems, vol. 14, no. 3, pp. 184-197, Mar. 2017.

Roadmap: Flight Heritage

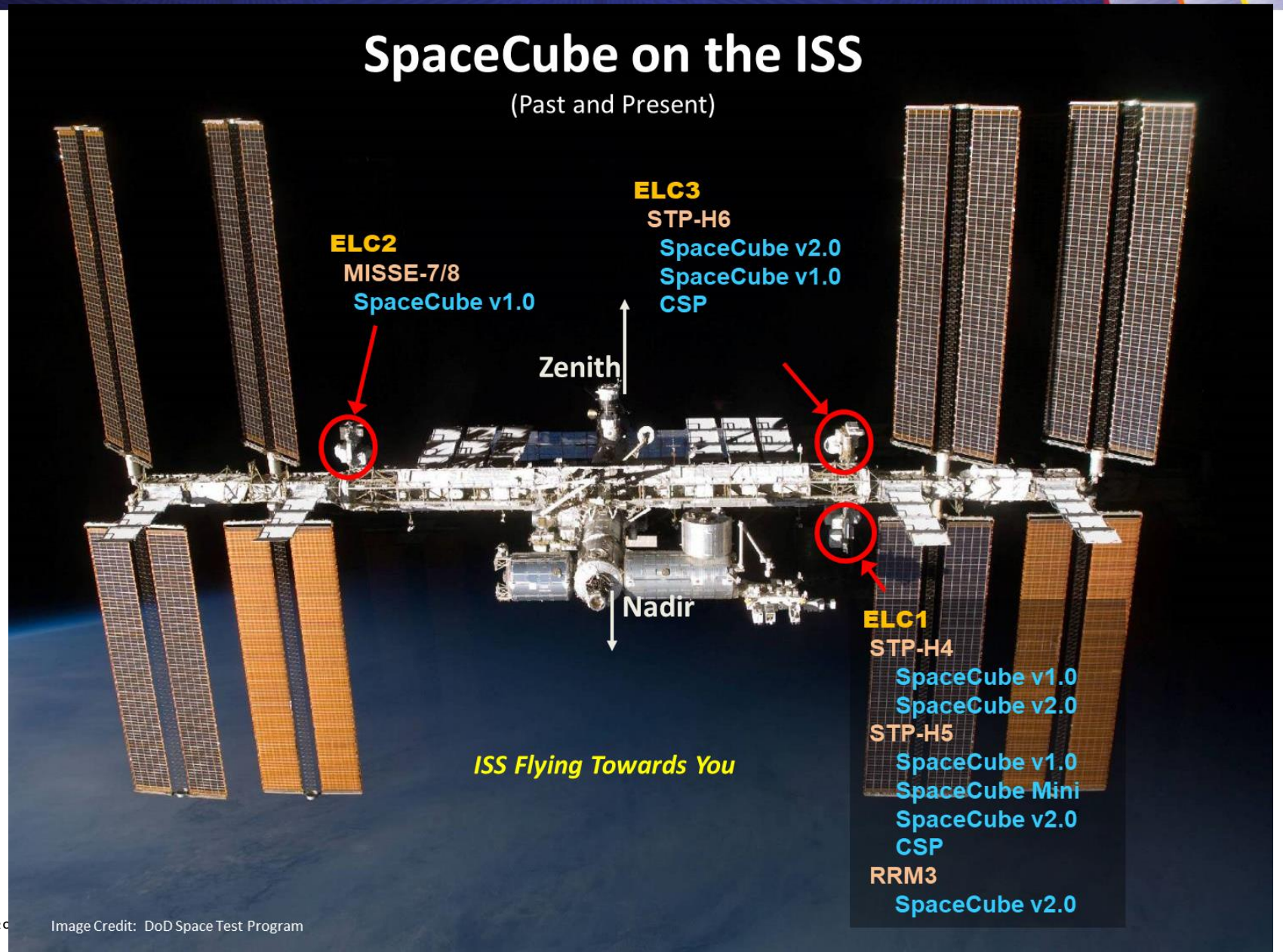


Image Credit: DoD Space Test Program

SpaceCube Family Flight Mission Timeline

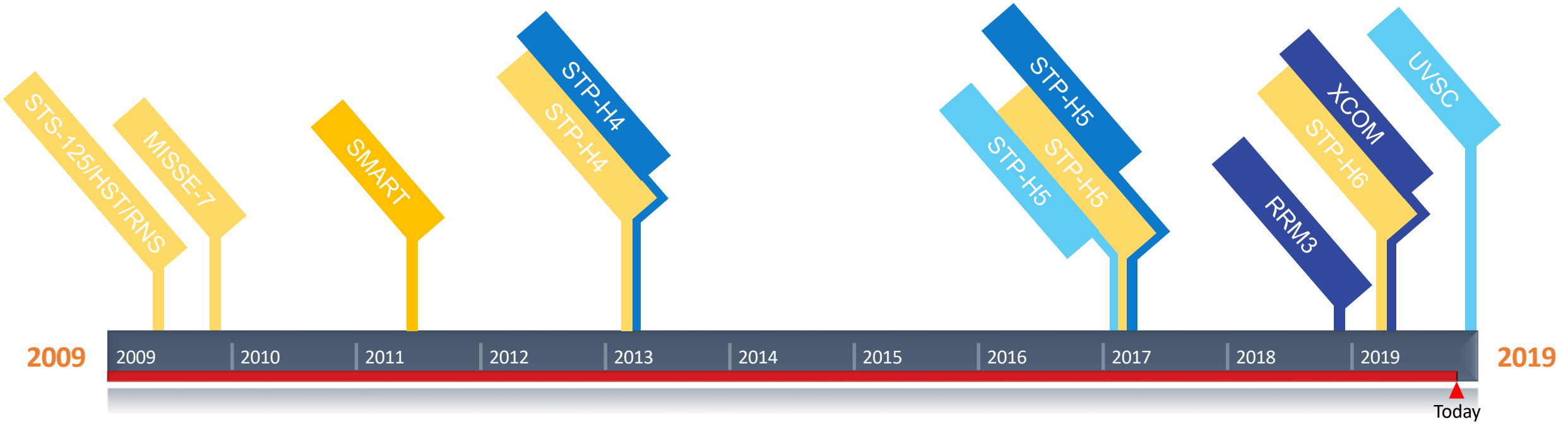
SpaceCube v1.0

SpaceCube v1.5

SpaceCube v2.0 Mini

SpaceCube v2.0-EM

SpaceCube v2.0-FLT



Accomplishments and Key Highlights: RRM3

Overview

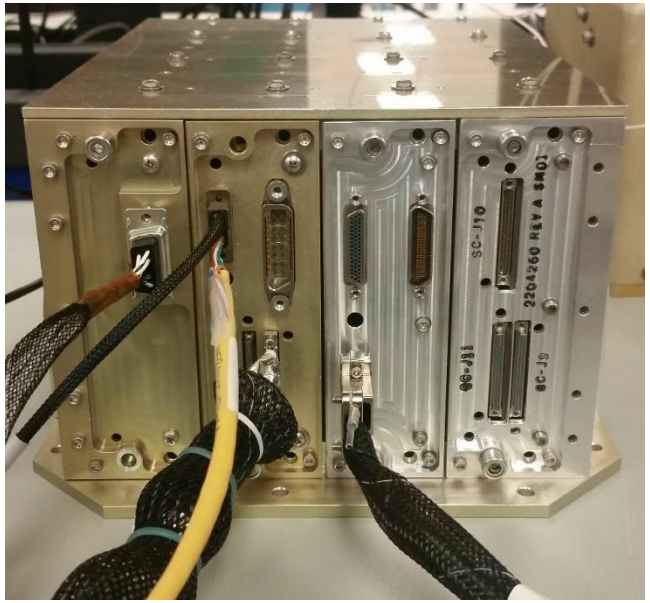
Robotic Refueling Mission 3 (RRM3)

- Technology demonstration experiment to highlight innovative methods to store and replenish cryogenic fluid in space

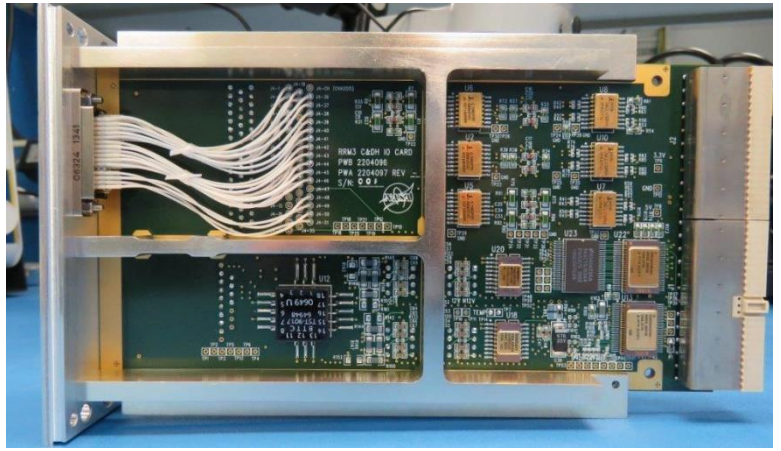
High Level Requirements

- Interface with ISS and RRM3 instruments:
  - Cameras, thermal imager, motors
- Monitor/Control cryo-cooler and fuel transfer
- Stream video data
- Motor control of robotic tools
- Host Wireless Access Point

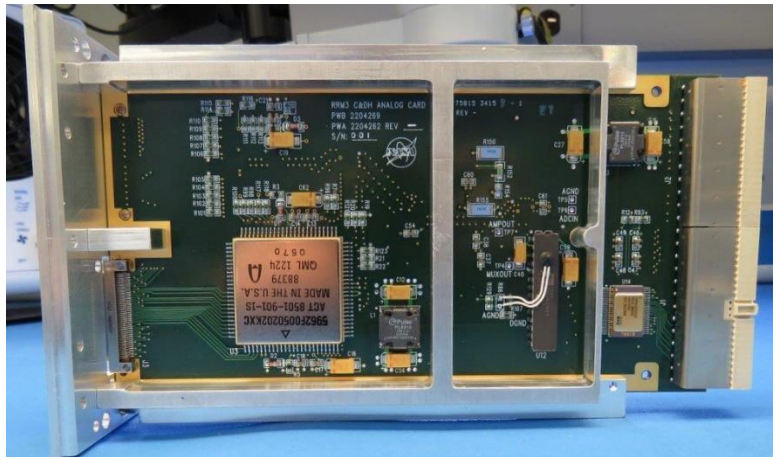
Robotic Refueling Mission 3 SpaceCube



1553/Ethernet/Digital Card



Analog Card

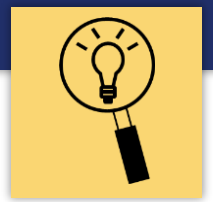


Accomplishments and Key Highlights: SpaceCube v3.0

Goals

Develop reliable, high-speed hybrid processor using SpaceCube design approach to **enable next-generation instrument and SmallSat capability**

Motivations



Highly reliable designs for varying mission environmental scenarios

New capabilities to support sensor integration and design tool flows

Need exceptional resources to support **complex applications** such as artificial intelligence

Challenges

Managing PCB area restrictions for rad-hard components, balancing cost, routing, and **signal and power integrity**

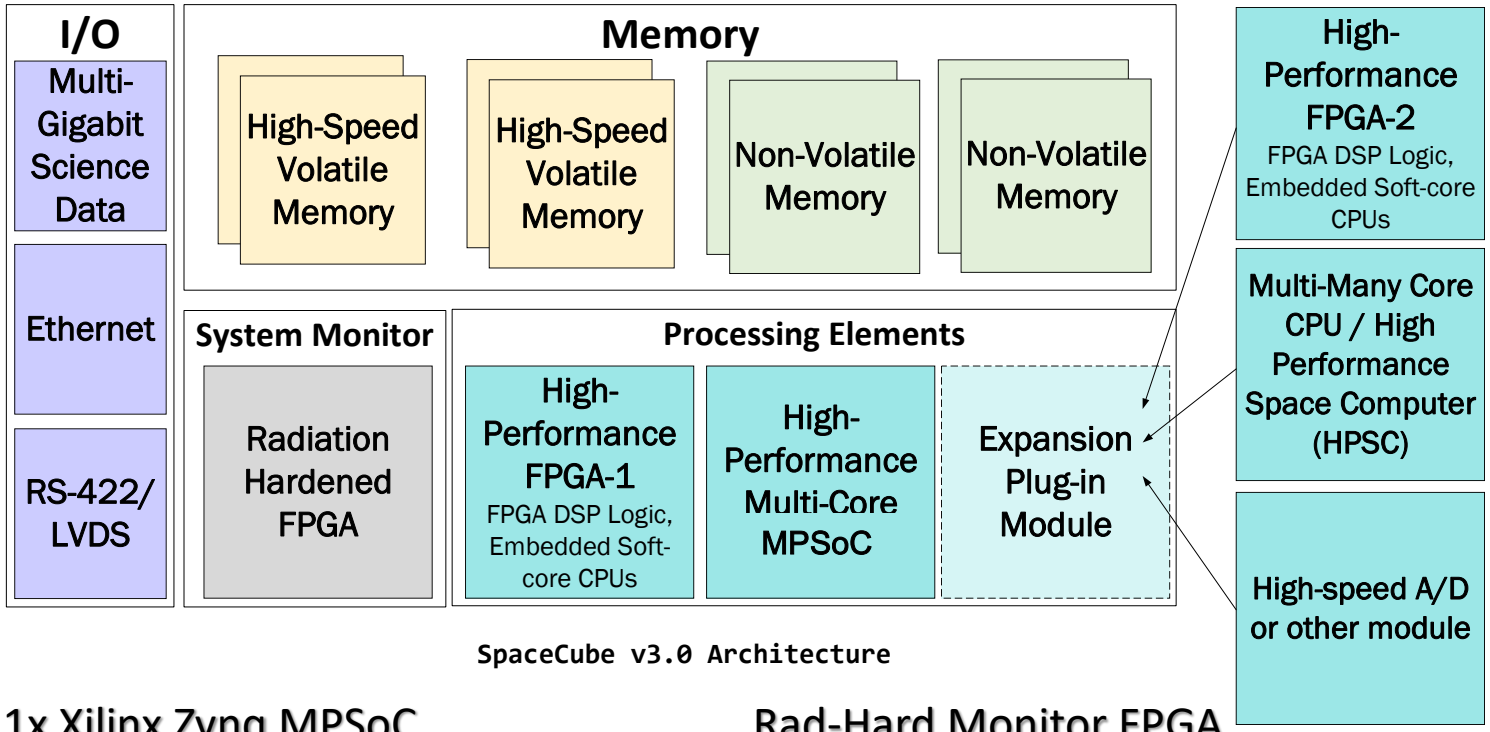
Mechanical and **thermal**

Supporting integrated software development kit

SpaceCube v3.0 Processor Card

Overview

- **Next-Generation** SpaceCube Design
- Prototype demonstration Jan. 2020
- **3U SpaceVPX** Form-Factor
- Ultimate goal of using High-Performance Spaceflight Computing (**HPSC**) paired with the high-performance FPGA
  - HPSC will not be ready in time for the prototype design
  - Special FMC+ Expansion Slot



SpaceCube v3.0 Architecture

Key Features

1x Xilinx Kintex UltraScale

- 2x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - 24x Multi-Gigabit Transceivers
  - 75x LVDS pairs or 150x 1.8V single-ended I/O
  - 38x 3.3V single-ended I/O,
  - 4x RS-422/LVDS/SPW
- Debug Interfaces
  - 2x RS-422 UART / JTAG

1x Xilinx Zynq MPSoC

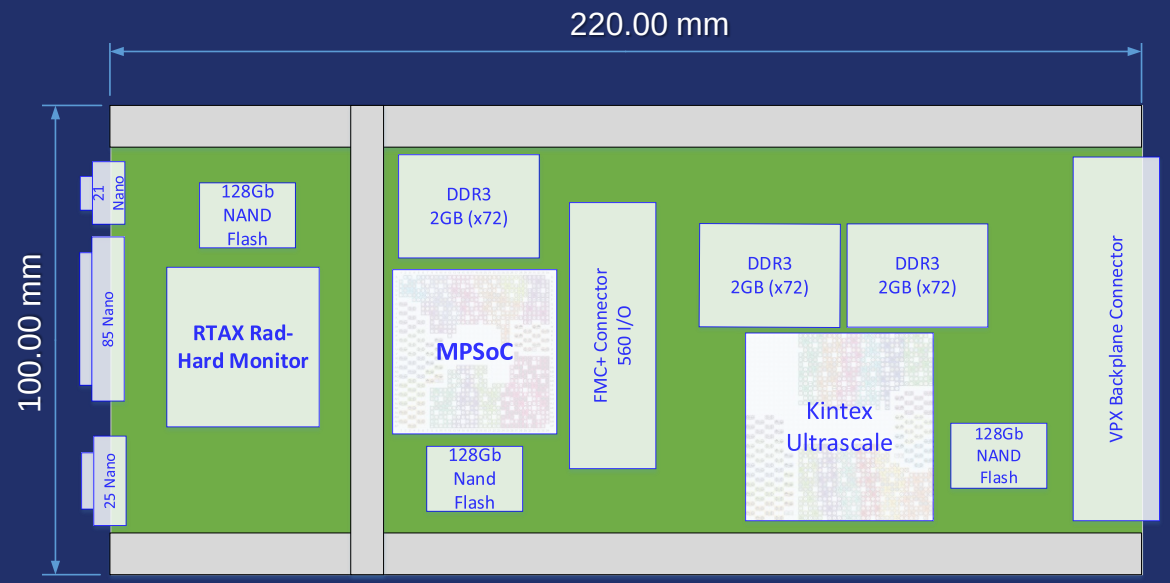
- Quad-core Arm Cortex-A53 processor (1.3GHz)
- Dual Arm R5 processor (533MHz)
- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - I2C/CAN/GigE/SPIO/GPIO/SPW
  - 12x Multi-Gigabit Transceivers
- Debug Interfaces
  - 10/100/1000 Ethernet (non-flight)
  - 2x RS-422 UART / JTAG

Rad-Hard Monitor FPGA

- Internal SpaceWire router between Xilinx FPGAs
- 1x 16GB NAND Flash
- Scrubbing/configuration of Kintex FPGA
- Power sequencing
- External Interfaces
  - SpaceWire
- 2x 8-channel housekeeping A/D with current monitoring

SpaceCube v3.0 Design Approach

SpaceCube v3.0 Processor Card



Reliable Monitor

Reliable supervisors for health monitoring, rollback, reconfiguration, and scrubbing

Quality Parts Selection

Flight-qualified parts where feasible, screening, qualification, and risk mitigation everywhere else

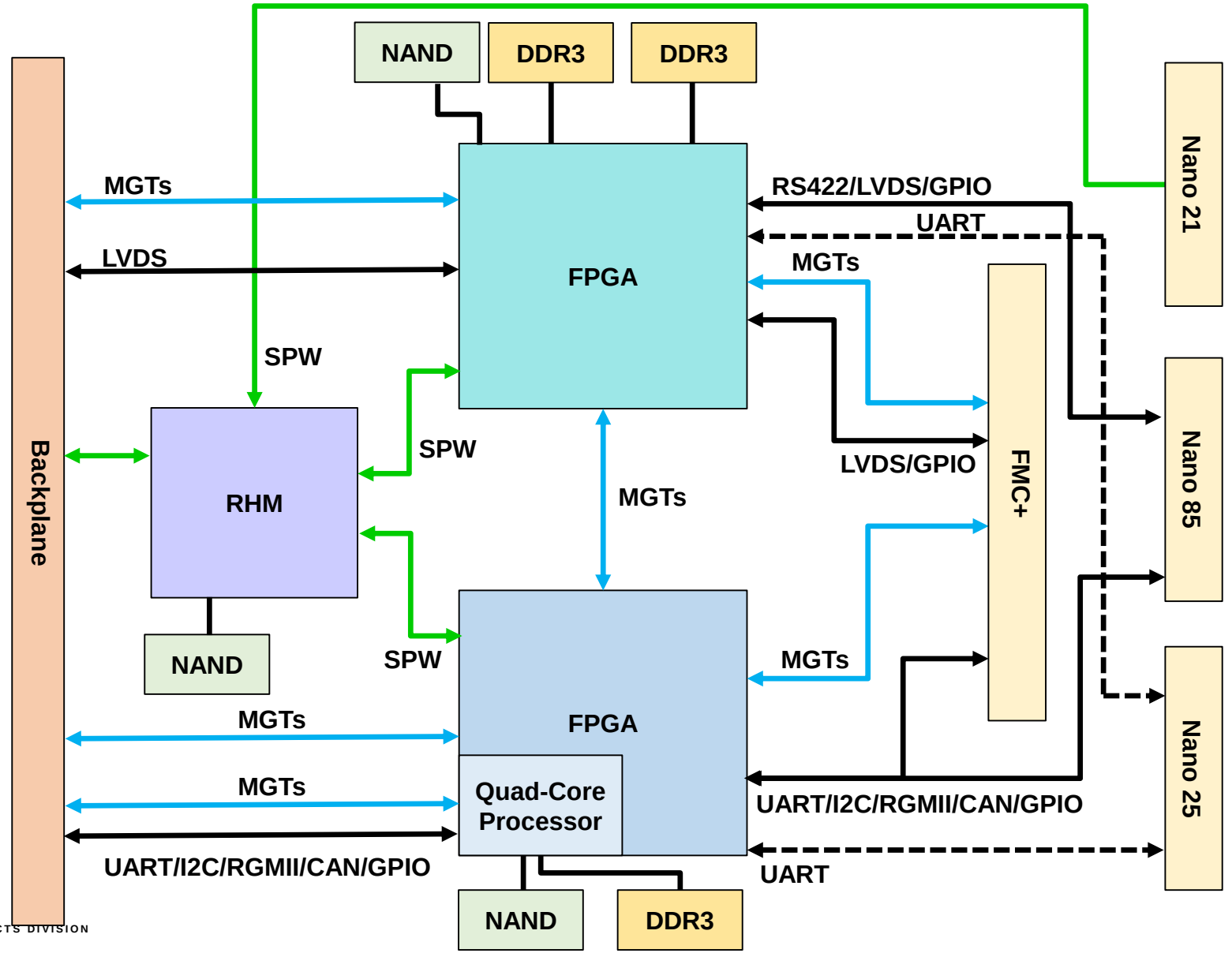
Modularity

Industry standard backplane-style interfaces for compatibility and expandability

Xilinx Devices and System Design

Emphasis on Xilinx designs for reconfigurability and flexibility, and focus on fault tolerance

SpaceCube v3.0 Interconnects



SpaceCube v3.0 HPSC Integration

Overview

- NASA/AFRL Collaboration for radiation hardened multi-core chiplet

Early Prototyping Effort

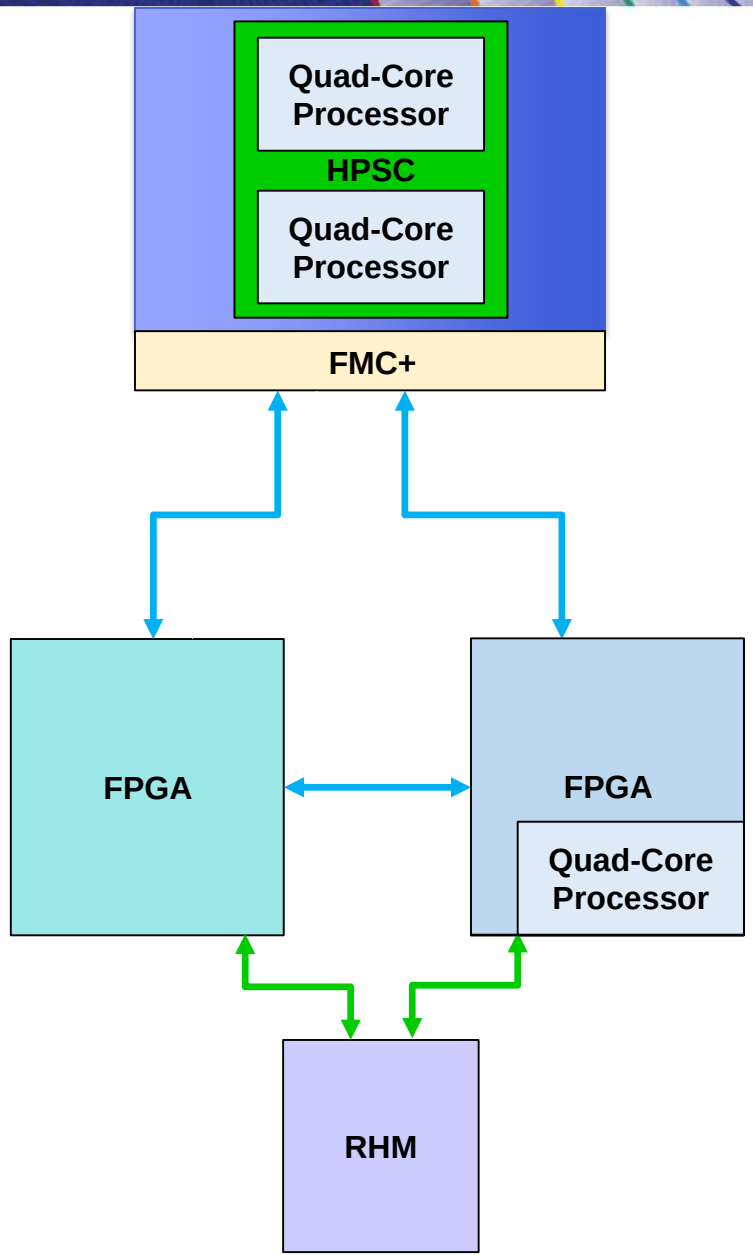
- HPSC chiplets will not be ready until 2021
- HPSC designs and prototypes can be conducted with MPSoC

MPSoC Replacement

- Next version of SpaceCube v3.0 can pair Xilinx Kintex Ultrascale with HPSC replacing MPSoC in design

FMC+ Expansion Add-on

- Separate FMC+ HPSC expansion card can be directly added to SpaceCube v3.0



W. A. Powell, "High-Performance Spaceflight Computing (HPSC) Project Overview," Radiation Hardened Electronics Technology (RHET) Conference, Phoenix, AZ, November 5-8, 2018.

SpaceCube v3.0 Why this capability?

Massive Observatories with Multiple Large Instruments

- Numerous mission concept studies required multiple SpaceCube processor cards to process and compress enormous volumes of data

Unfortunately for FPGA Resources Everywhere… AI and Machine Learning

- Research shows AI/ML constructs have wide applicability for space, however, some complex models incur long execution times or massive resource overheads

Semantic Segmentation / Image Classification

- Computer Vision / Machine Learning Process learns to assign label to all pixels of image
- Parallel computations are scalable and certain accelerator sizes can only be supported on larger devices

S. Sabogal, A. D. George, and G. Crum, "ReCoN: Reconfigurable CNN Acceleration for Space Applications A Framework for Hybrid Semantic Segmentation on Hybrid SoCs," 12th Space Computing Conference, July 30 – August 1, 2019.

Adaptive Compression

- Regenerative compression technique by training neural-network codecs on satellite imagery to improve compression
- Lightweight neural network on spacecraft to encode compressed representation can be hardware accelerated

Accomplishments and Key Highlights: SpaceCube v3.0 Mini

Goals

Develop reliable, high-speed hybrid processor using SpaceCube design approach **enable next-generation instrument and CubeSat capability**

Motivations

Many commercial CubeSat processor offerings primarily target benign LEO orbits and do not strongly address **radiation concerns and parts qualification**

Need exceptional capability to support **complex applications** such as artificial intelligence

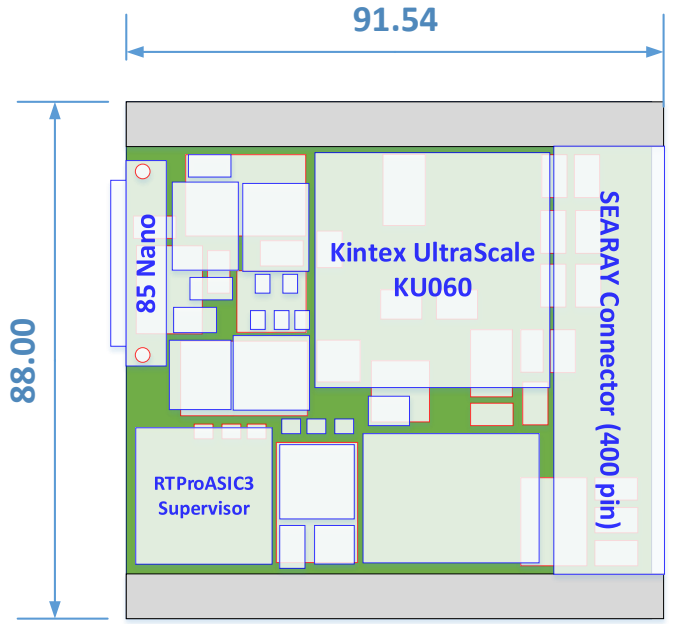
Challenges

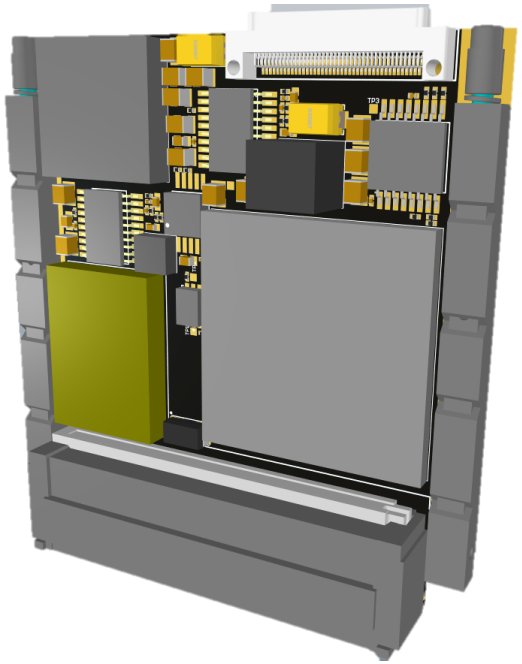
Managing PCB area restrictions for rad-hard components, balancing cost, **educating mission designers** for key reliability differences

SpaceCube v3.0 Mini Specification

Overview

- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus MARES





Key Features

1x Xilinx Kintex UltraScale

- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG

- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 48x 3.3V GPIO
  - SelectMAP Interface
  - (Front Panel) 24x LVDS pairs or 48x 1.8V single-ended I/O
  - (Front Panel) 8x 3.3V GPIO

SmallSat/CubeSat Processor Challenge

Massively Expanding Commercial Market for SBCs

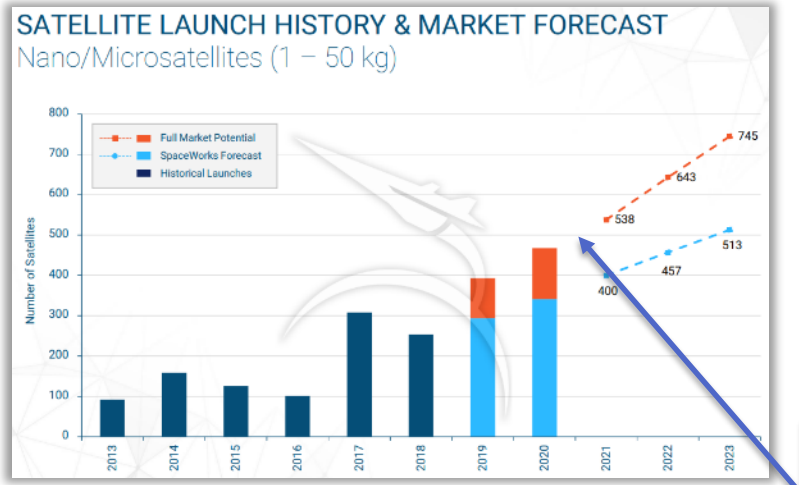
- Tons of commercial vendors in CubeSat Market (e.g. Pumpkin, Tyvak, GomSpace, ISIS, Clyde Space, etc…)

Mission Developers Seeking Commercial Hardware

- Under pressure from cost-cap missions, and reducing costs in general
- Reduced RE for constellation mission concepts
- Attractive all-commercial solutions provided integrating several CubeSat “Kit” types of cards

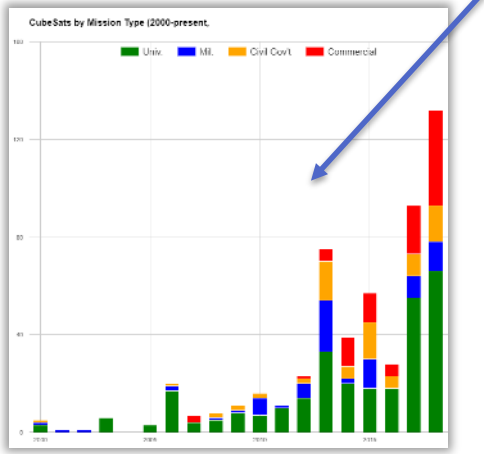
Not Designed With Harsh Orbit Considerations Beyond LEO

- Many vendors largely support missions in more benign LEO orbits
- Little-to-no additional radiation testing or parts qualification
- Mission is radiation test approach
- No recommendations for fault-tolerant configurations of offered SBCs



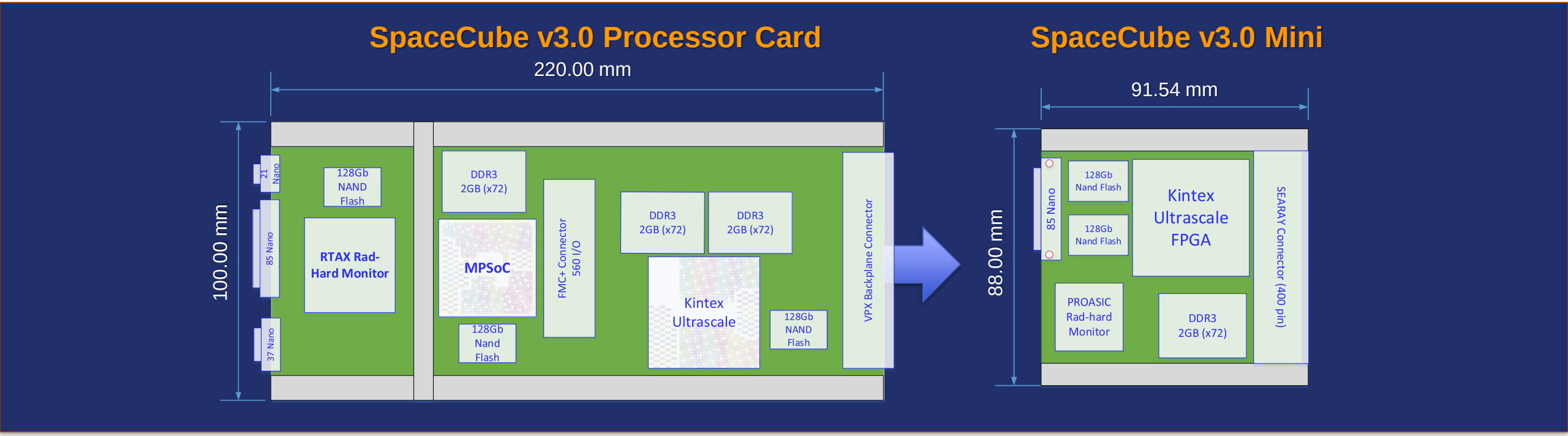
“2019 Nano/Microsatellite Forecast, 9th Edition,” SpaceWorks Enterprises, Inc., Jan 2019.

Dramatic Increasing Trend



M. A. Swartwout @ The CubeSat Database

Mini Design Philosophy



Same Approach, Smaller Size

SpaceCube design approach applied to smaller form-factor

Key Design Reused

Much of UltraScale design and interface remain same between cards including DDR Pinout

Supervision Requested

Radiation-hardened monitor architecture and code reusable

Trade in, Trade Out

EEE parts trades, analysis, and circuits extensively leveraged from main card design

Accomplishments and Key Highlights: SpaceCube Mini-Z

Overview of SpaceCube Mini-Z

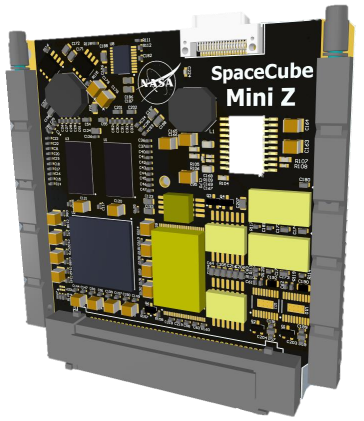
- Collaborative development with **NSF CHREC** at University of Florida for Zynq-based 1U Board
  - Selective population scheme between commercial and rad-hard components
  - Rapid deployment prototyping
  - Convenient pre-built software packages with cFS
- **Re-Envisioned** to support quality-of-life upgrades and enable specific NASA mission needs

Missions and Heritage

- Launched Feb 2017 to ISS on STP-H5/CSP featuring 2 CSPv1 cards performing image processing
- Launched May 2019 to ISS on STP-H6/SSIVP featuring 5 CSPv1 for massive parallel computing
- Featured on many more…

CSPv1 Development Board

Original CSPv1



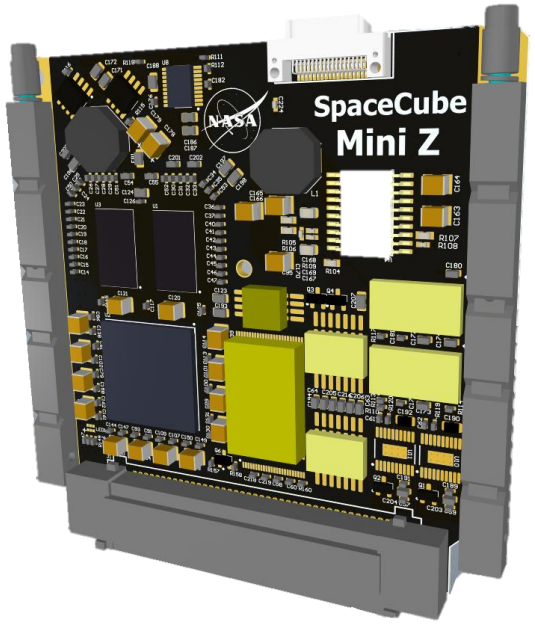
NASA SpaceCube Mini-Z

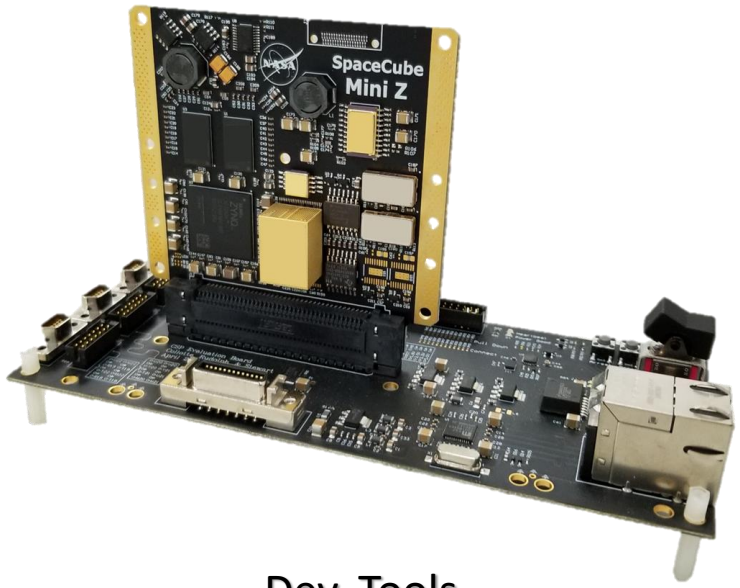
STP-H5/CSP Flight Unit

SpaceCube Mini-Z Specification

Overview

- **Re-envisioned and upgraded** version of popular CSPv1 design collaboratively developed between NASA GSFC and NSF CHREC
- Supports additional IO and form-factor changes to maintain compliance with MARES (GSFC's SmallSat bus) architecture





Key Features

Processing Capability

- Processing System (PS)
  - Xilinx Zynq-7020 SoC with Dual-Core ARM Cortex-A9 up to 667 MHz
  - 32KB I/D L1 Cache per core
  - 512KB L2 Cache
  - 256KB OCM
  - NEON SIMD Single/Double Floating Point Unit per core
- Programmable Logic (PL)
  - 85K Logic Cells
  - 53,200 LUTS /106,400 FF
  - 220 DSPs
  - 4.9Mb BRAM

Storage

- 1GB DDR3 SDRAM
- 4GB NAND Flash

IO

- MIO
  - 26 single-ended configurable IO into common interfaces such as UART, SPI, CAN, and I2C
- EMIO
  - 24 differential pairs and 12 single-ended IO
- Front Panel
  - 12 differential pairs

Dev. Tools

- CSP Evaluation Board
  - JTAG programming support
  - 10/100 Ethernet
  - MIO and EMIO breakout
  - 3 SpaceWire breakouts
  - Camera Link breakout
- USB-UART Board
  - USB to UART Converter

Physical Dimensions

- ~82g, 620 mil thick
- <1U CubeSat form factor
- 1.6-3.6W (FPGA load dependent)

Deployment Configurations

Small form factor makes SpaceCube Mini **versatile** for many use cases and multiple mission classes

Instrument Processing Unit

- Provides high-speed interface to instruments supporting 12 Multi-Gigabit Transceivers and over 70 LVDS pairs
- Convenient small enclosure for tight integration

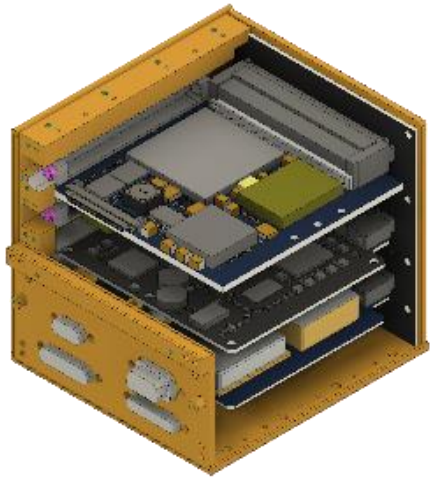
High-Performance Processor

- Featured as the high-performance processor on NASA GSFC's highly reliable CubeSat Bus MARES
- Supports latest Xilinx FPGA development tools including high-level synthesis, reVISION, and Partial Reconfiguration

AI "Edge Node" Co-Processor System

- Can combine SCv3.0 Mini with Mini-Z or Mini-Z45 to provide on-board autonomy and analysis dedicated co-processing node

XILINX



SpaceCube Software Development Kit

SpaceCube provides software packages for mission development

SpaceCube includes support for several popular OS (Linux, RTEMS, FreeRTOS) and allows for end-to-end flatsat testing with ground station software such as Ball Aerospace's COSMOS and NASA's IRC

COSMOS

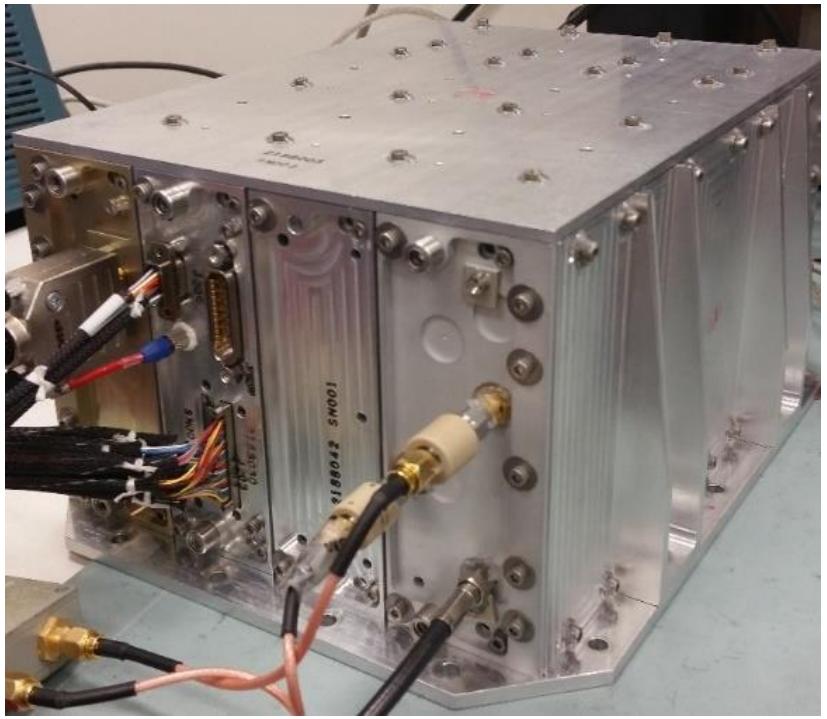
NASA SOFTWARE

freeRTOS

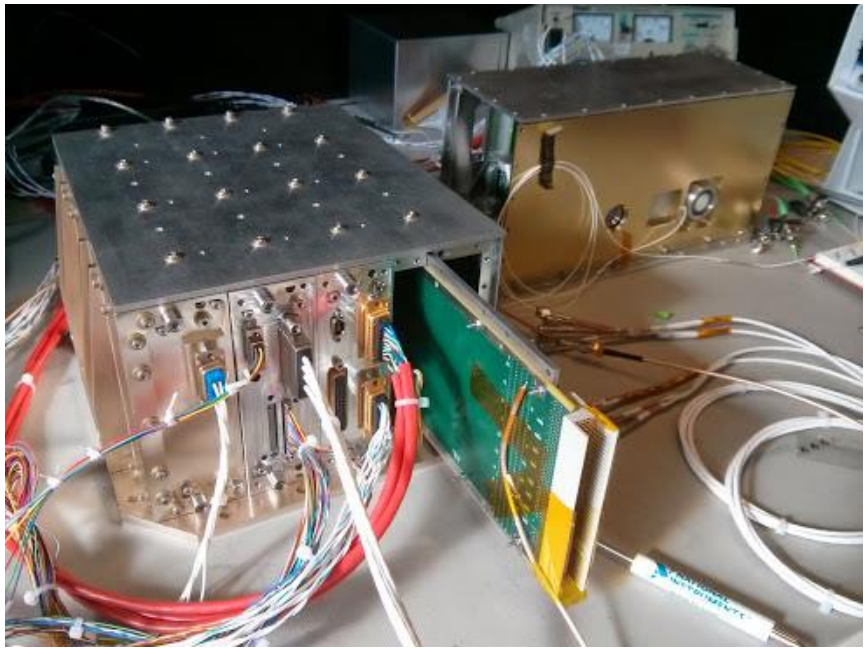
RTEMS™

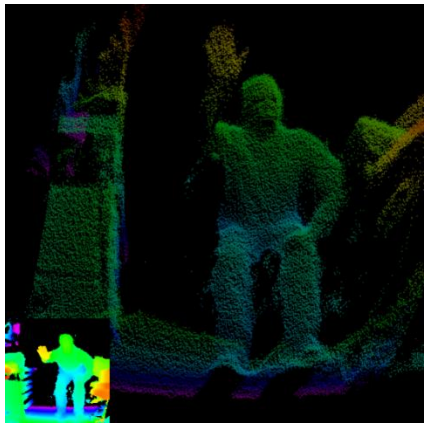
Infusion Overview

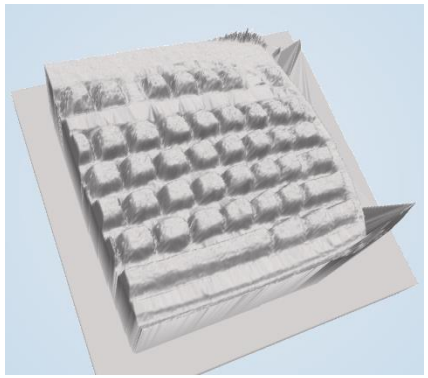
GPS Receiver – L1/L2C Tracking



LIDAR Instrument – Configurable Resolution

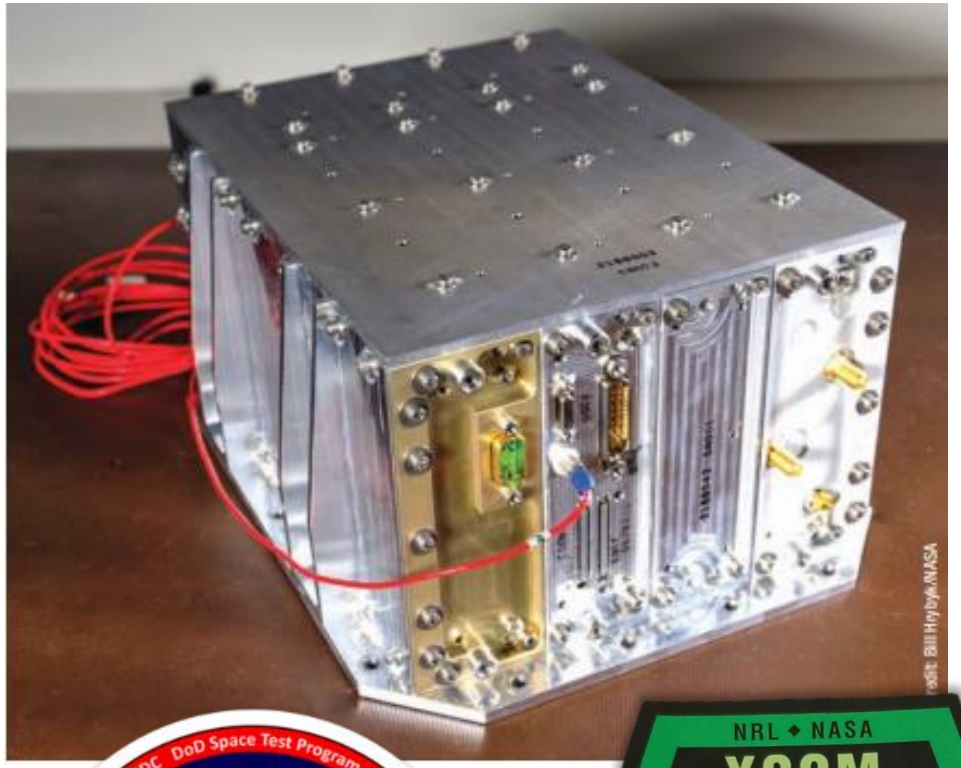






Infusion: NavCube on X-ray Communication Experiment (XCOM)

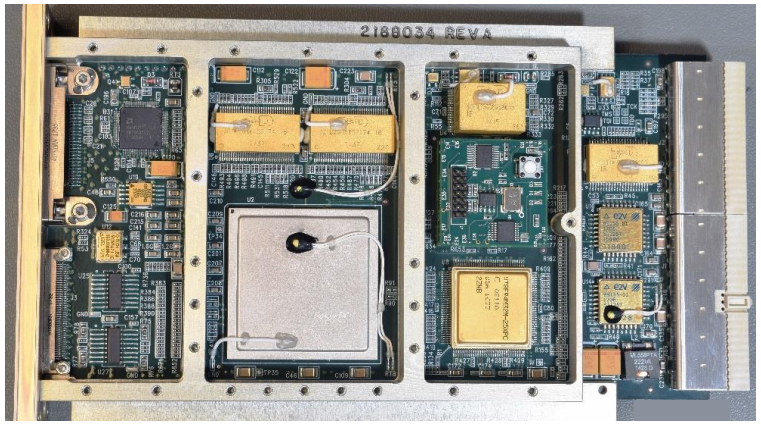
- **NavCube**: Union of Navigator GPS and SpaceCube technology
  - NavCube drives electronics for Modulated X-ray Source on Space Test Program-H6 (**STP-H6**) as part of X-ray Communications Experiment (**XCOM**)
  - 2016 Goddard Innovation of the Year
- Flexible SpaceCube design enabled **low-cost, rapid mission development**
  - Delivered Command and Data Handling FSW
  - Supports inflight updates of FPGA and software
  - Allowed significant software reuse leveraging key components from previous SpaceCube Missions
    - RRM3: Core FSW component
    - CeREs: AOS processing as part of cFS library
    - STP-H: Packet processing for CCSDS and STP protocols



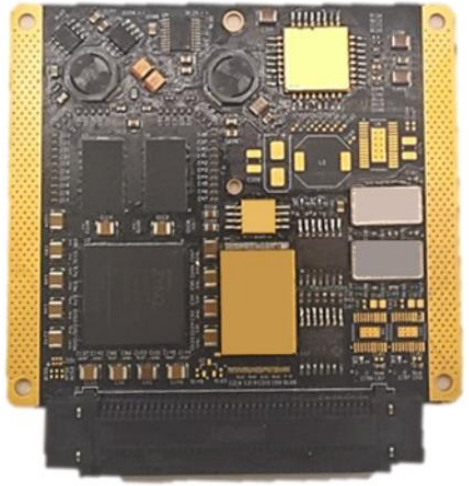
SpaceCube Commercialization

- SpaceCube 2.0 → Genesis Engineering Solutions Inc. “GEN6000”
- NSF CHREC Space Processor → Space Micro “Cubesat Space Processor”

GEN6000 Processor



Cubesat Space Processor



Commercialization for SpaceCube v3.0 and SpaceCube v3.0 Mini **in progress**!

Challenges

Making people aware of what we've been doing for the past 15 years ☺

- Helping others understand radiation effects and acceptable/credible risks
- Conveying benefits and limitations of reconfigurable FPGA systems

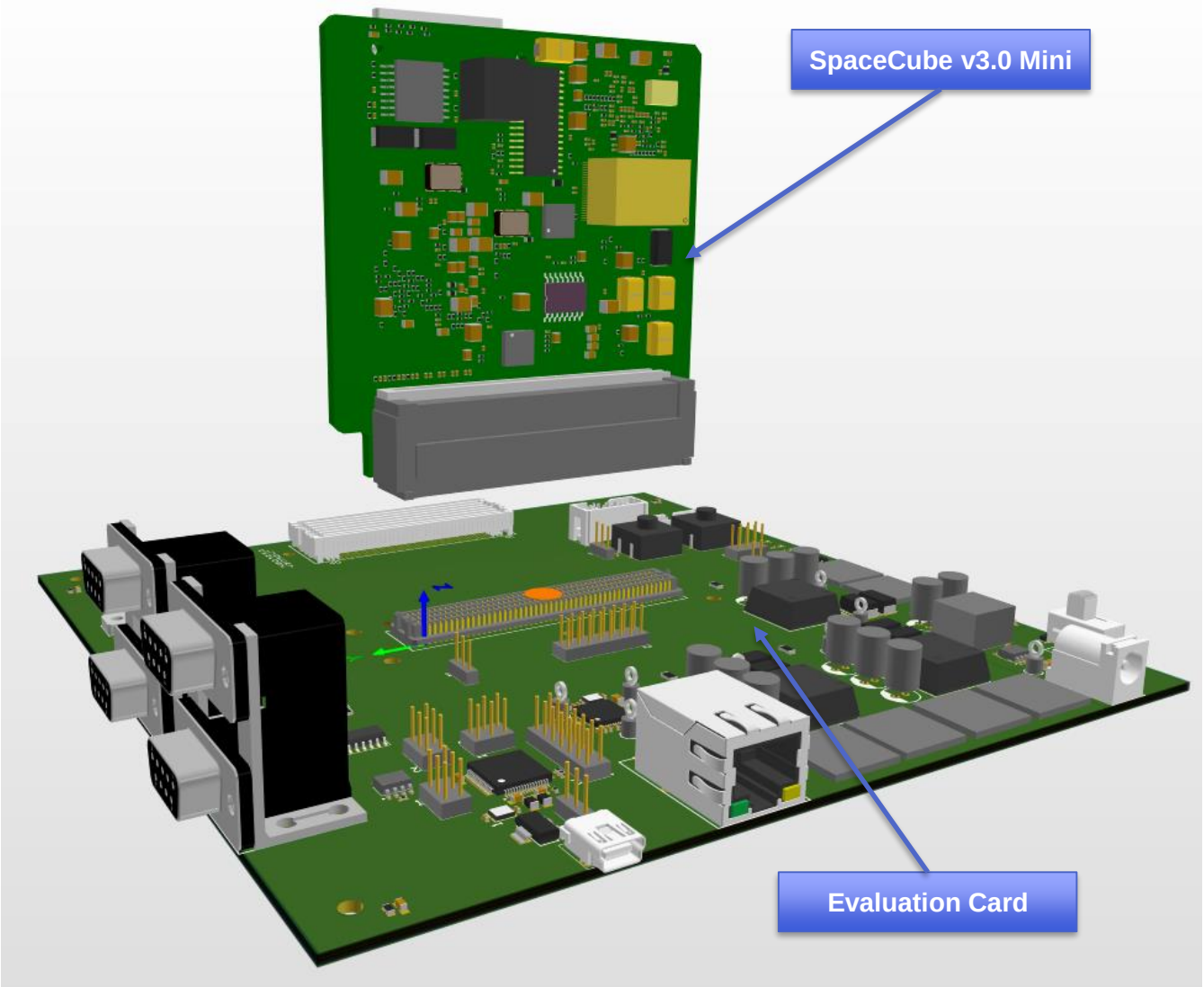
Ongoing and Future Work: SpaceCube Mini Kit

Overview

- Provides **easy development platform** to support SpaceCube v3.0 Mini rapid prototyping and design
- Includes several common interfaces for programming and debug
- Incorporates FMC+ Connector to support future Mezzanine and commercial vendor designs

Key Features

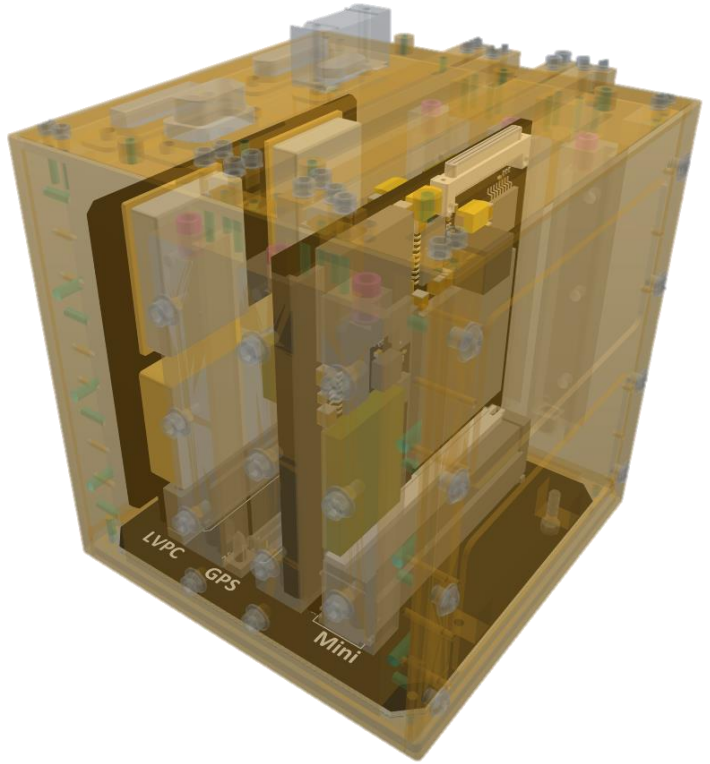
- Gigabit Ethernet (RJ45/SGMII)
- USB Debug / JTAG
- JTAG headers - Xilinx and Microsemi
- SelectMAP programming header
- 2 SpaceWire ports
- 4 RS422 ports
- FMC+ Connector
  - 11 Multi-Gigabit Transceivers
  - 46x LVDS or 92x 1.8V GPIO
  - 22x 3.3V GPIO



Ongoing and Future Work: Mini-NavCube

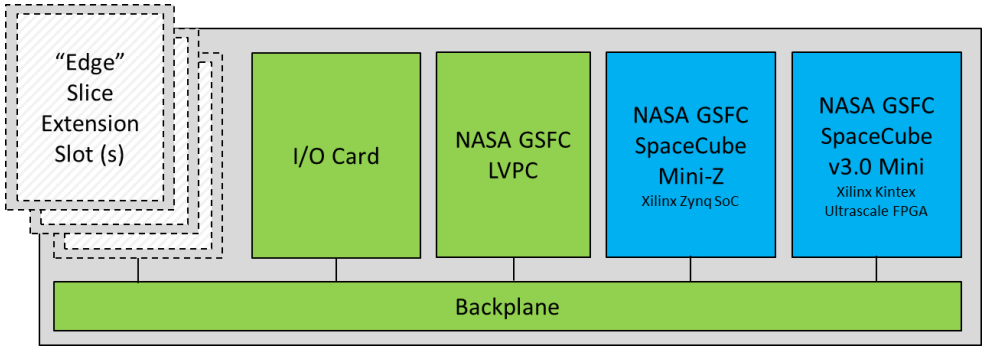
Overview

- Next series development for highly succesful NavCube (2016 Goddard Innovation of the Year)
- NavCube design in CubeSat form-factor solution
- Integration of Navigator GPS RF card and SpaceCube v3.0 Mini

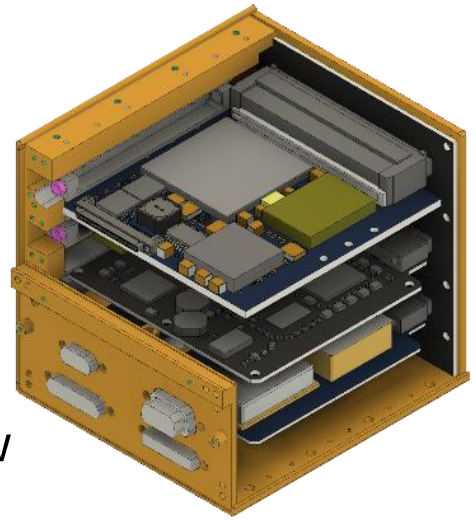


Ongoing and Future Work: SpaceCube AI Co-Processor

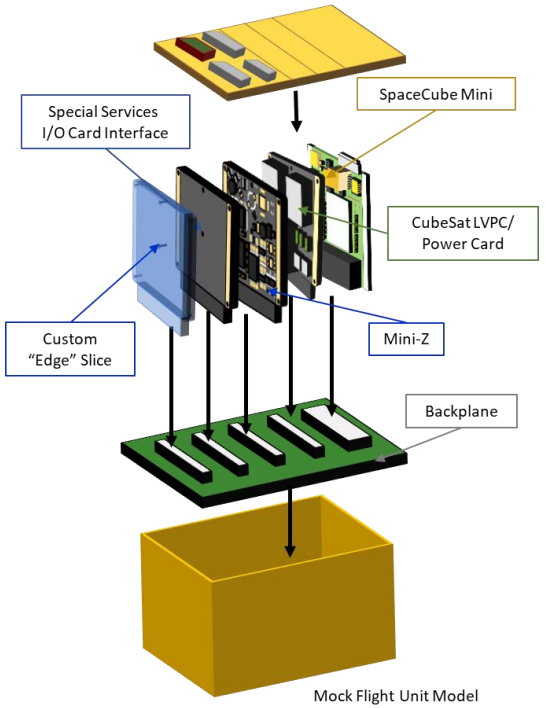
- **Goal:** Deliver **cutting-edge AI applications** on space-based platform for next-generation on-board intelligence and protect system against space radiation effects with fault-tolerant mitigation
  - **Motivations**: AI applications have vast potential for use in space domain, however, many have not been evaluated for flight due to limitations of space computers
  - Baseline system features: NASA Goddard SpaceCube v3.0 Mini (Kintex UltraScale FPGA), NASA Goddard SpaceCube Mini-Z (Zynq SoC), GSFC Low Voltage Power Converter, customizable special services I/O card to support mission and sensor unique interfaces
  - Extendable architecture to include **rapid insertion** of new technology to reliable system
- Vast capability in small package



High-Level System Block Diagram



SpaceCube Co-Processor in 1U Chassis



Extendable Concept Model

Ongoing and Future Work: MARES

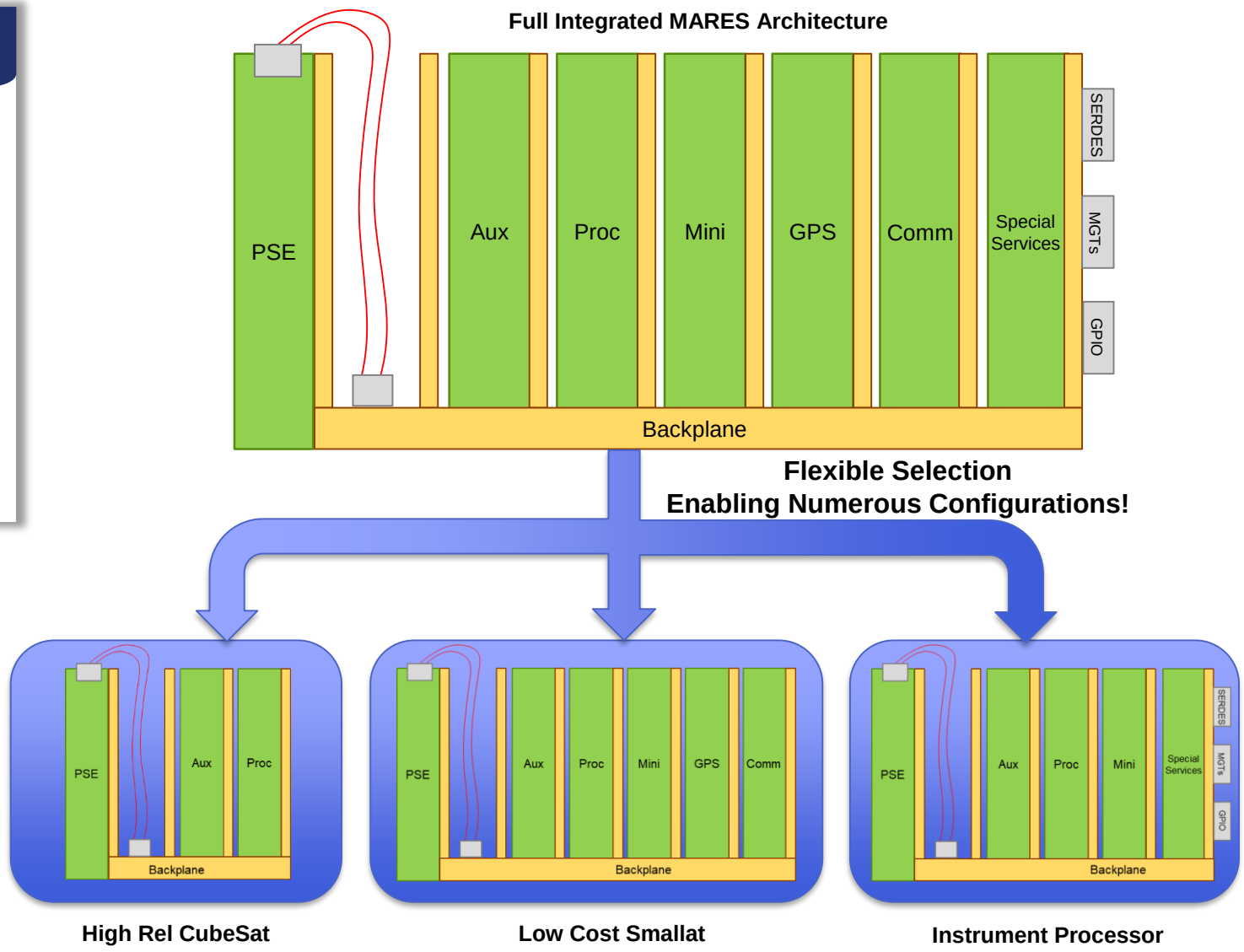
Overview

- Modular Architecture for Resilient Extensible Smallsat (**MARES**)
- Enabling large volume, high-speed NASA science data for challenging environments
- Flexible architecture to support:
  - Small, inexpensive SmallSat bus
  - Reliable, powerful CubeSat bus
  - High-performance instrument processor

Key Features

- Baseline flexible architecture to meet unique Goddard Science Missions (low power, long duration, autonomous, high data rate/volume, high radiation/temperature)

- System design includes:
  - Highly Reliable C&DH
  - SpaceCube Science Data Processing Card
  - Navigator GPS
  - Comm/Software Defined Radio
  - Power and Propulsion system

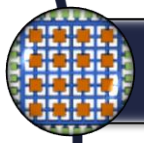


Conclusion

*SpaceCube is a **MISSION ENABLING** technology*

Delivers exceptional computing power in number of form factors

Cross-cutting technology for Comm/Nav, Earth and Space Science, Planetary, and Exploration missions



Being reconfigurable equals BIG SAVINGS

Past research / missions have proven viability

Designs support AI applications for autonomy and analysis onboard

Successful technology transfer to industry through commercialization

Contact Information

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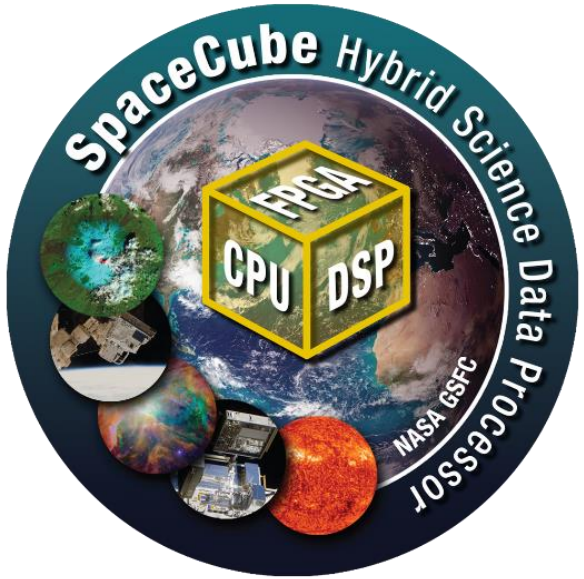


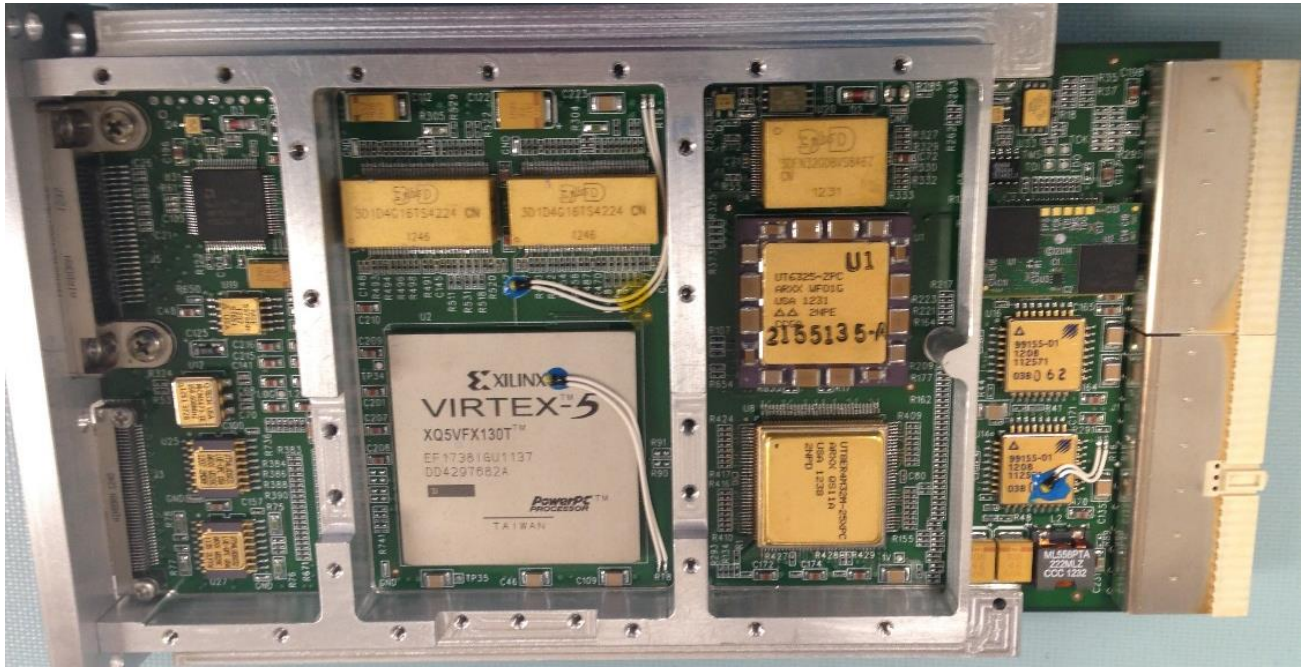
Special thanks to our sponsors: NASA/GSFC IR&D, NASA Satellite Servicing Programs Division (SSPD), NASA Earth Science Technology Office (ESTO), DoD Space Test Program (STP), DoD Operationally Responsive Space (ORS)

Reference Charts

SpaceCube v2.0 Processor Card

Overview

- **TRL9** flight-proven processing system with unique Virtex back-to-back installed design methodology
- **3U cPCI** (190 x 100mm) size
- Typical power draw: 8-10W
- 22-layer, via-in-pad, board design
- IPC 6012B Class 3/A compliant

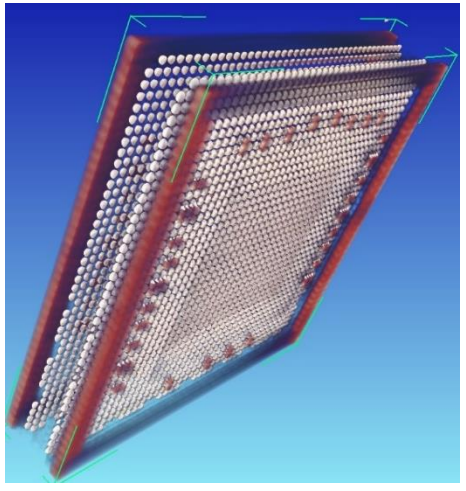


Back-to-Back FPGA Design

Key Features

- 2x Xilinx Virtex-5 (QR) FX130T FPGAs (FX200T Compatible)
- 1x Aeroflex CCGA FPGA
  - Xilinx Configuration, Watchdog, Timers
  - Auxiliary Command/Telemetry port
- 4x 512 MB DDR SDRAM
- 2x 4GB NAND Flash
- 1x 128Mb PROM, contains initial Xilinx configuration files
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 16-channel Analog/Digital circuit for system health
- Mechanical support for heat pipes and stiffener for Xilinx devices

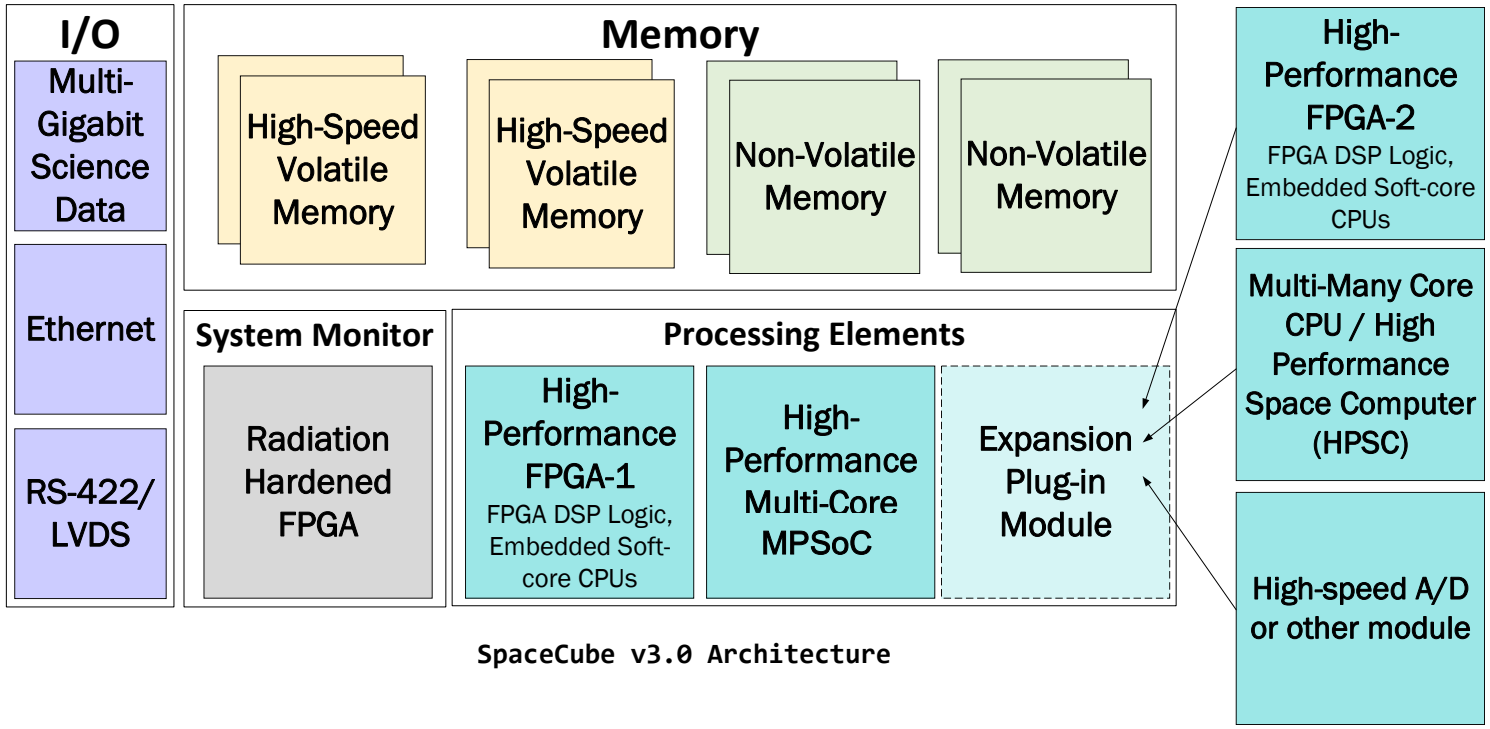
- External Interfaces
  - Gigabit interfaces: 4x external, 2x on backplane
  - 12x Full-Duplex dedicated differential channels
  - 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Debug Interfaces
  - Optional 10/100 Ethernet interface



SpaceCube v3.0 Processor Card

Overview

- **Next-Generation** SpaceCube Design
- Prototype demonstration CY Q1 2020
- **3U SpaceVPX** Form-Factor
- Ultimate goal of using High-Performance Spaceflight Computing (**HPSC**) paired with the high-performance FPGA
  - HPSC will not be ready in time for the prototype design
  - Special FMC+ Expansion Slot



SpaceCube v3.0 Architecture

Key Features

1x Xilinx Kintex UltraScale

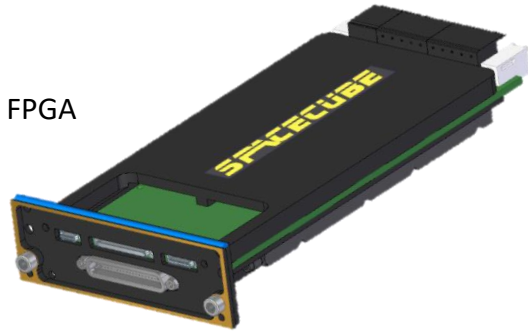
- 2x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - 24x Multi-Gigabit Transceivers
  - 75x LVDS pairs or 150x 1.8V single-ended I/O
  - 38x 3.3V single-ended I/O,
  - 4x RS-422/LVDS/SPW
- Debug Interfaces
  - 2x RS-422 UART / JTAG

1x Xilinx Zynq MPSoC

- Quad-core Arm Cortex-A53 processor (1.3GHz)
- Dual Arm R5 processor (533MHz)
- 1x 2GB DDR3 SDRAM (x72 wide)
- 1x 16GB NAND Flash
- External Interfaces
  - I2C/CAN/GigE/SPIO/GPIO/SPW
  - 12x Multi-Gigabit Transceivers
- Debug Interfaces
  - 10/100/1000 Ethernet (non-flight)
  - 2x RS-422 UART / JTAG

Rad-Hard Monitor FPGA

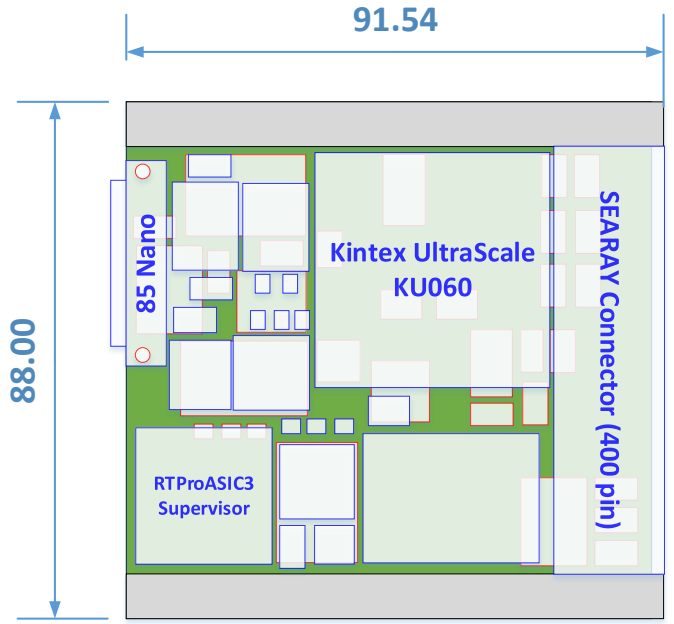
- Internal SpaceWire router between Xilinx FPGAs
- 1x 16GB NAND Flash
- Scrubbing/configuration of Kintex FPGA
- Power sequencing
- External Interfaces
  - SpaceWire
- 2x 8-channel housekeeping A/D with current monitoring

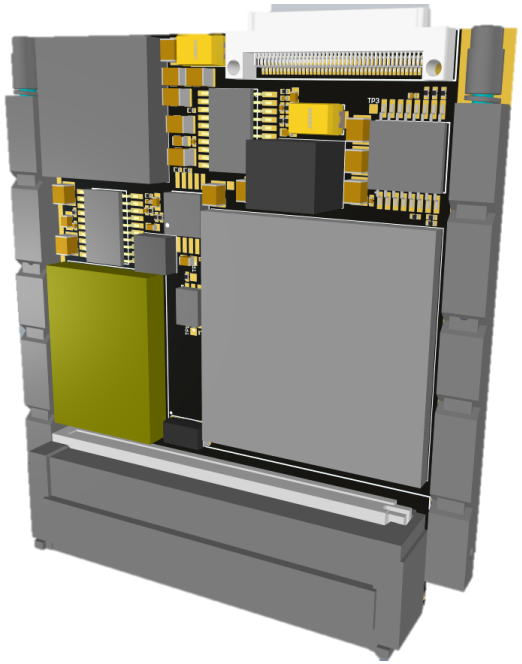


SpaceCube v3.0 Mini Specification

Overview

- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus MARES





Key Features

1x Xilinx Kintex UltraScale

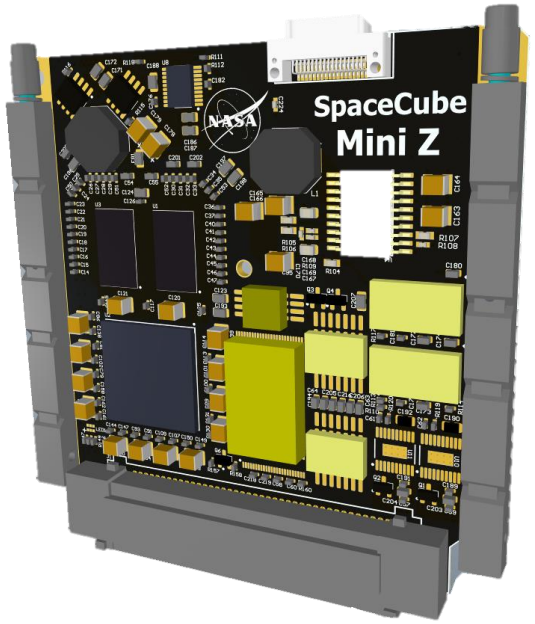
- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG

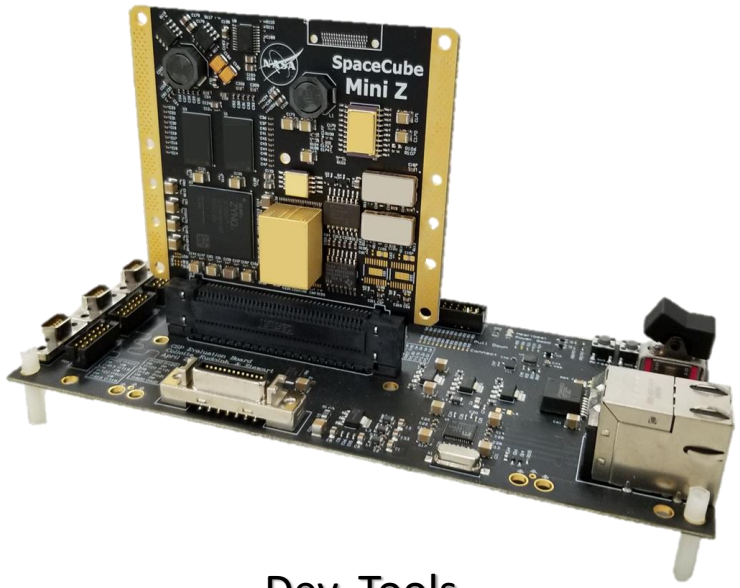
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 48x 3.3V GPIO
  - SelectMAP Interface
  - (Front Panel) 24x LVDS pairs or 48x 1.8V single-ended I/O
  - (Front Panel) 8x 3.3V GPIO

SpaceCube Mini-Z Specification

Overview

- **Re-envisioned and upgraded** version of popular CSPv1 design collaboratively developed between NASA GSFC and NSF CHREC
- Supports additional IO and form-factor changes to maintain compliance with MARES (GSFC's SmallSat bus) architecture





Key Features

Processing Capability

- Processing System (PS)
  - Xilinx Zynq-7020 SoC with Dual-Core ARM Cortex-A9 up to 667 MHz
  - 32KB I/D L1 Cache per core
  - 512KB L2 Cache
  - 256KB OCM
  - NEON SIMD Single/Double Floating Point Unit per core
- Programmable Logic (PL)
  - 85K Logic Cells
  - 53,200 LUTS /106,400 FF
  - 220 DSPs
  - 4.9Mb BRAM

Storage

- 1GB DDR3 SDRAM
- 4GB NAND Flash

IO

- MIO
  - 26 single-ended configurable IO into common interfaces such as UART, SPI, CAN, and I2C
- EMIO
  - 24 differential pairs and 12 single-ended IO
- Front Panel
  - 12 differential pairs

Dev. Tools

- CSP Evaluation Board
  - JTAG programming support
  - 10/100 Ethernet
  - MIO and EMIO breakout
  - 3 SpaceWire breakouts
  - Camera Link breakout
- USB-UART Board
  - USB to UART Converter

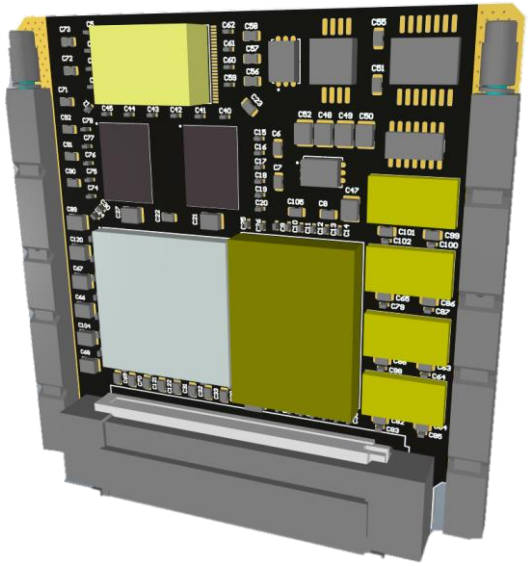
Physical Dimensions

- ~82g, 620 mil thick
- <1U CubeSat form factor
- 1.6-3.6W (FPGA load dependent)

SpaceCube Mini-Z45 Specification

Overview

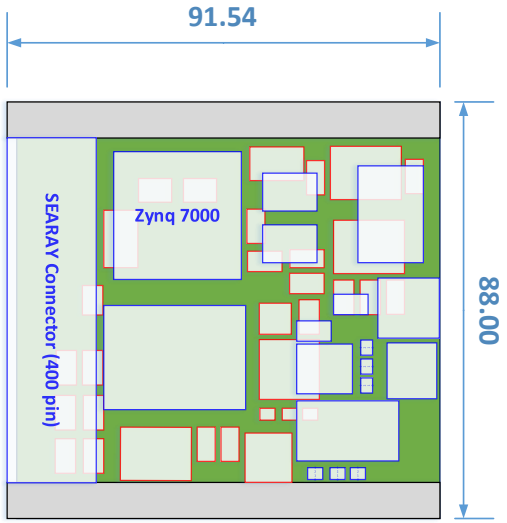
- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0 Mini and Mini-Z designs
- **Upgrade** capabilities of Mini-Z (CSPv1) to provide MGTs, more FPGA resources and more memory



Key Features

1x Xilinx Zynq 7000 System-on-Chip

- 1GB DDR3 SDRAM for ARM Processors
- 2GB DDR3 SDRAM for Programmable Logic
- 16GB NAND Flash
- Radiation-Hardened Watchdog
- External Interfaces
  - 8x Multi-Gigabit Transceivers
  - 31x LVDS pairs or 62x single-ended I/O (voltage selectable)
  - 28x Single-ended PS MIO
- Debug Interfaces
  - 1x RS-422 UART (external transceivers)
  - JTAG



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