SWEL: Hardware Cache Coherence Protocols to Map Shared Data onto Shared Caches

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Background

In chip multiprocessors, replication of cache lines is allowed to reduce the latency each core has to access a cache line. Because of this replication, it is possible for one copy of data to become out of date if another copy of that data is modified.

How a MESI protocol accomplishes this:

➢ Keep a list of sharers for all cache lines

➢ Invalidate all L1s in the list of sharers on modify (write) request

➢ Forward read requests to whichever L1 has most recently modified the data

As can be seen in the diagrams below, the frequency and degree of data sharing is not very high on average, so MESI might be over-provisioning for this uncommon case.

Sharing profile by memory locations

Sharing profile by memory references

Proposal

We propose a new coherence protocol named SWEL (for Shared, Written, Exclusivity Level) that seeks to reduce the frequency and complexity of the operations required to keep the cache coherent in protocols like SWEL.

MESI's drawbacks:

➢ Requires indirection to get up to date data

➢ Requires serialized sequences of messages to perform point to point invalidations

SWEL protocol:

➢ Limits replication of data to reduce coherence operations (only private and read-only replicated)

➢ Speculatively assumes all data is read-only or private

➢ Simple hardware mechanism to detect shared and written state

➢ Broadcast bus to perform invalidates

The RSWEL optimization of this algorithm allows for selective reconstitution of cache blocks so they can be once again cached in L1 after they've been broadcast invalidated, based on some lockout timer N.

Operations needed to maintain coherence

SWEL and RSWEL protocols significantly reduce the number of operations required to keep caches coherent. The use of the broadcast bus simplifies the design process compared to MESI's frequent indirection and waiting for ACK messages, which can make it easier to formally verify. Also, our further experimentation has shown a modest performance improvement over MESI.

MESI State diagram
The states for a single cache line constitute a cyclical graph. It is possible to reach all nodes from all others.

SWEL State Diagram
The states for a single cache line have a source and sink. Once the sink is reached, no more coherence is required.