RADIO FREQUENCY-POWERED MIXED-SIGNAL MICROCONTROLLER WITH WIRELESS ULTRA-WIDEBAND TRANSMITTER FOR ELECTROCHEMISTRY AND BIOSENSING

by

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A dissertation submitted to the faculty of
The University of Utah
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering

The University of Utah

December 2014

The University of Utah Graduate School

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ABSTRACT

Since the late 1950s, scientists have been working toward realizing implantable devices that would directly monitor or even control the human body's internal activities. Sophisticated microsystems are used to improve our understanding of internal biological processes in animals and humans. The diversity of biomedical research dictates that microsystems must be developed and customized specifically for each new application. For advanced long-term experiments, a custom designed system-on-chip (SoC) is usually necessary to meet desired specifications. Custom SoCs, however, are often prohibitively expensive, preventing many new ideas from being explored.

In this work, we have identified a set of sensors that are frequently used in biomedical research and developed a single-chip integrated microsystem that offers the most commonly used sensor interfaces, high computational power, and which requires minimum external components to operate. Included peripherals can also drive chemical reactions by setting the appropriate voltages or currents across electrodes. The SoC is highly modular and well suited for prototyping *in* and *ex vivo* experimental devices.

The system runs from a primary or secondary battery that can be recharged via two inductively coupled coils. The SoC includes a 16-bit microprocessor with 32 kB of on-chip SRAM. The digital core consumes 350 μW at 10 MHz and is capable of running at frequencies up to 200 MHz. The integrated microsystem has been fabricated in a 65 nm CMOS technology and the silicon has been fully tested. Integrated peripherals include two sigma-delta analog-to-digital converters, two 10-bit digital-to-analog converters, and a sleep mode timer.

The system also includes a wireless ultra-wideband (UWB) transmitter. The fully-digital transmitter implementation occupies 68 x 68 μm^2 of silicon area, consumes 0.72 μW static power, and achieves an energy efficiency of 19 pJ/pulse at 200 MHz pulse repetition frequency.

An investigation of the suitability of the UWB technology for neural recording systems is also presented. Experimental data capturing the UWB signal transmission through an animal head are presented and a statistical model for large-scale signal fading is developed.

This research achieved the goal of implementing a single-chip low-power microcontroller for prototyping of biomedical applications with a wide range of electrochemical sensors and actuators.

To my family

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ACKNOWLEDGMENTS

I would like to begin by thanking my advisor, Professor Richard Brown. Professor Brown stepped in and became the chair of my Ph. D. committee when I was at the verge of walking away from the program and discarding three years of my work. His integrity, professionalism, and exceptional leadership skills have made a substantial impact on my life, career, and professional skills. Professor Brown is the main reason I have made it this far and I am very thankful for his giving me the opportunity to work in his research group and for providing an environment conducive to learning and growing beyond my expectations.

I also want to thank Professor Cameron Charles for being my first Ph. D. advisor, for staying on my committee after his departure from the University, and for being such a great source of inspiration at both professional and personal levels. I would also like to thank Professors Neal Patwari, Kent Smith, Thomas Schmid, and Reid Harrison for being on my thesis committee, for their helpful suggestions, and for providing access to some of their equipment. Professor Ken Stevens has helped me on numerous occasions with tasks related to chip design and fabrication and our tapeouts would not be possible without his help. I also want to thank Lori Sather, Janna Nelson, Vicki Jensen, Holly Cox, and Debbie Colgan, who made even the most difficult administrative tasks smooth and easy.

I would also like to thank all fellow students in my current and former research groups for creating a productive study environment. In particular, I thank Bennion Redd and Nathaniel Gaskin, without whom our MOSIS tapeouts would have never happened. Jeff Campbell, Spencer Kellis, Rob Franklin, Manohar Nagaraju, Ahmed Ragab, and Wei Wu have often provided their expertise to solve problems. I really appreciate all the interesting (non-) technical discussions throughout the years.

I would like to thank the entire e-SENS team for the opportunity to work with them and for providing our research group with electrochemical sensors. My frequent interactions with all of the team members have been very inspirational and I have learned a great deal from each of you.

I also owe my sincere gratitude to many close personal friends who have been a great support throughout the years. The list would certainly be long but I want to especially

thank Caroline Keller, Yuko Tatematsu, Bernardo Imbico, Tomas Novak, Tomas Sabolcak, Hynek Novak, Lenka Svarcova, Ondrej Kucera, and Mira Hlasek. Your support is much appreciated.

I want to thank my girlfriend, Yuki Sakuma, for her patience and support. She has been a great listener and provided needed encouragements when times were not so great. Ultimately, I want to deeply thank my parents, Jirina and Jan Novakovi, grandmother, Jirina Kolihova, brother, Lukas, and his wife, Deborah Novakovi, for their constant support. There have been many moments in my life when your encouragement and support have been the only things I could truly rely on. It is only because of your guidance and the values you taught me to worship that I made it this far.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Aggressive scaling of electronic devices, advances in packaging, and new biocompatible materials have contributed to many groundbreaking discoveries in biomedical research in recent years. Scientists use sophisticated microsystems to improve our understanding of internal biological processes in animals and humans. Applications range from simple vital sign monitoring in laboratory animals to very complex instruments recording neocortical electrical activity in primates and even stimulating the human brain. Modern electronic microsystems enable multidisciplinary research and are routinely used to improve quality of life.

The diversity of current biomedical research dictates that microsystems must be developed and customized specifically for each new application. Often, new ideas need to be validated in laboratory animals. It is imperative that these devices be miniature (to enable implantation), biocompatible, highly efficient, and provide sufficient computational power to perform complex data processing. Additionally, for *in vivo* experiments or research on untethered animals, these microsystems need to offer wireless connectivity.

System prototypes are typically used to validate new ideas and to serve as a proof of concept for commercialization. Typically, the first generations of prototypes are designed from commercial components such as microcontrollers, amplifiers, and data converters. These prototypes rarely achieve desired battery life, miniaturization, or accuracy. For advanced long-term experiments, a custom-designed system-on-chip (SoC) is usually necessary to meet desired specifications. Custom SoCs, however, are often prohibitively expensive, preventing many new ideas from being explored.

1.2 Electrochemical Micro-Instrumentation

Miniature wireless electronic devices have become widely used in biomedical and chemical research [1–4]. Complex systems can now be implanted in laboratory animals with

reduced stress levels as animals may move freely in their natural habitats. The uniqueness of each application and a wide spectrum of sensors, however, make these devices expensive to design. Moreover, many sensor technologies, by nature, operate in the analog domain and have to be interfaced with digital microcontrollers, resulting in a very complex chip design.

A closer look at current applications employing wireless microsystems, however, reveals that many sensors used in biomedical and chemical research share commonalities in stimulation and signal processing. Table 1.1 captures several frequently used sensors and actuators. Each column in the table is a group of sensors or actuators that require the same electronic interface to connect to a microcontroller.

Applications such as thermometers, certain types of conductivity meters, pressure gauges, and many others, all use the same principle of sensing. They use sensors that respond by changing their resistivity proportionally to the variable of interest. These sensors are typically stimulated by a constant DC current and the voltage across their terminals is digitized with an analog-to-digital converter (ADC). Consequently, the digital signal is processed in the microcontroller and converted to the appropriate units.

Another group of sensors commonly deployed in chemical research are ion-selective electrodes (ISE). ISEs can be made using a polymeric membrane that has binding sites for specific ions. The potential between the membrane and solution is measured and is proportional to the concentration (or activity) of the selected ions. Many common chemicals such as hydrogen (pH), ammonium, calcium, or CO_2 can be accurately measured by ISEs. From the circuit perspective, however, they all require the same type of interface regardless of the chemical compound they are designed to measure.

Table 1.1: **Review of common chemical sensors and actuators.**

Resistive Sensors	Ion-Selective-Electrodes	Actuators
Temperature	Hydrogen (pH)	Release of nitric oxide
Pressure	Ammonium	pH shifting
Conductivity	Calcium	
	Sodium	
(Many emerging sensors)	Potassium	(Many electrolysis or redox
	Nitrate	reactions)
	Chloride	
	Magnesium	
	Cadmium	
	...	

In addition to sensing and signal processing, microsystems frequently need to directly drive chemical reactions. The rate and type of chemical reactions can be controlled by applying voltages or currents of specific magnitudes and time durations. Also, chemical reactions can generate voltages or currents and commonly need to be measured to gain understanding of biological processes.

In our effort to address the issue of the prohibitive cost of custom SoCs, we have identified a set of interfaces that are frequently used in biomedical and chemical research, and developed an integrated system which offers several common sensor interfaces, high computational power, and requires low power and a small form factor. The system allows each peripheral to be turned *ON/OFF* independently by the firmware, thus making the SoC highly modular. Included are interfaces for sensors measuring pH, temperature, pressure, and conductivity. The included peripherals can also drive chemical reactions by setting the appropriate voltages or currents across electrodes. These interfaces make the system modular and suitable for a wide range of future applications.

1.3 Deep-Submicron SoC Integration

Since the late 1960s, the semiconductor industry has been using Moore's law to set targets for research and development. As a result, transistor density has been increasing exponentially and semiconductor manufacturers are now reliably fabricating chips with billions of transistors on a single silicon die. The capabilities of modern electronic devices such as processing speed and memory capacity are closely linked to Moore's law and have also been improving at exponential rates. This development has given us the ability to design miniature systems-on-chip (SoC) with unprecedented computational power and a wide spectrum of peripherals that can be integrated together on a single chip. Furthermore, decreasing operating voltages result in lower power consumption, allowing batteries to last longer. These benefits of advanced technologies, however, come at the cost of new challenges and risks for designers.

Technology scaling significantly lowers the cost of digital logic and memory, spurring a significant motivation to implement new circuits in the most advanced process technology available. Analog designers, however, are facing new and more severe issues with every successive generation of CMOS technology. Phenomena such as noise, cross-talk, substrate noise, and interconnect parasitics were previously negligible. In submicron technologies, however, these and many other issues represent an immense problem requiring large investments in research and design tools. Although there are many challenges for the analog designer resulting from being forced to design in deep-submicron technologies, only a few

that are related to biomedical applications will be mentioned in the following paragraphs.

With migration to more advanced CMOS processes, the supply voltage is usually decreased, causing the voltage headroom and signal swing of individual transistors to also be decreased. Lower headroom, consequently, decreases the dynamic range of analog circuits and degrades the signal-to-noise ratio (SNR). This problem is often partially eliminated by using thick-oxide transistors and employing advanced circuit design techniques and architectures.

Another (perhaps the most significant) problem related to microsystems for biomedical applications is the increasing leakage current I_{OFF} in deep-submicron technology. Increasing leakage, caused by decreasing gate oxide thicknesses, affects both dynamic and static power. For technologies below 65 nm, leakage might even dominate the total dissipated power, making it problematic for implantable devices that typically operate from miniature batteries with limited power capacity. Techniques such as power gating or adaptive body-biasing [5] have been used to mitigate the leakage issue.

1.3.1 Design Methodology

To realize a miniature and fully operational microsystem, analog and digital circuitry needs to be integrated on a single chip. This represents a challenge as each type of circuit benefits from different semiconductor technologies. Digital circuits benefit from technologies having small minimum dimensions, because they can achieve high device density and high computational power at low power supply voltages. Analog circuits, on the other hand, benefit from technologies having larger dimensions, as fewer parasitic effects need to be considered. Higher power supply voltages give analog designers more headroom and a wider dynamic range. As a compromise between these two contradicting requirements, we decided to use a 65 nm CMOS process for our SoC.

The system is based on a digital core designed at the University of Michigan and later improved at the University of Utah. The digital pipeline has a 16-bit architecture with an optimized instruction set and 32 kB of on-chip SRAM. It has been tested to operate at low power levels and is capable of connecting peripherals through a set of memory-mapped registers.

To serve a wide range of current and future biomedical and chemical applications, the on-chip peripherals include a 4-channel sigma-delta ADC, two digital-to-analog converters (DACs), three voltage regulators, and a voltage bandgap reference. We also include two RF interfaces: an ultra-wideband (UWB) data transmitter and an inductive link. The UWB transmitter is capable of high data rates at low power consumption and the inductive link

provides wireless power for implanted applications. Additionally, two programmable current sources are included for sensor stimulation. All integrated peripherals can be independently turned *ON/OFF* in firmware, giving the system great flexibility and efficiency.

1.4 Thesis Objectives

The ultimate objective of our research is to develop an implantable, biomedical instrument on a chip, which will establish a new benchmark for capability, power, and size of implantable electronics. Our effort aims to push the state of the art in wireless microsystems in two ways: (1) design, implement, and characterize a single-chip microsystem with RF powering capability, wireless data transmitter, and sensor interfaces for potentiometric sensors, conductivity sensor, and temperature sensor; and (2) design a UWB transmitter and evaluate it for suitability in electrocorticography research on untethered animals. This dissertation is organized in the following manner: Chapter 2 describes the role of electronic microsystems in modern biomedicine and introduces three applications that provide the background and motivation for this work. Chapter 3 describes the motivation and implementation details of the proposed Utah microcontroller. Chapter 4 presents a detailed description of the UWB data transmitter and Chapter 5 describes a verification of the transmitter and evaluates its suitability for deployment in experiments on untethered animals. Chapter 6 offers conclusions and a discussion of future work.

CHAPTER 2

MICROSYSTEMS IN MODERN BIOMEDICINE

2.1 Overview

Integrated microsystems refer to miniaturized electronic systems that often include complex digital processors, memories, sensors, actuators, and converters. They must be reliable, light weight, power efficient and, in case of implantable systems, also biocompatible. Microsystem design is an interdisciplinary field with applications reaching across many areas of science, engineering, chemistry, and medicine. Designers in this field engage in research and development of digital and analog integrated circuits, RF circuits, wireless systems, microfabricated sensors and actuators, materials, and microelectronics packaging techniques. Microsystems are becoming increasingly important in a wide range of applications, including medical devices, embedded systems, energy scavenging, environmental monitoring, and sensor networks.

Medical technology is one of the most promising fields in electronics. It has already led to substantial innovations that benefit doctors, patients, and their families. This trend will continue in the coming years and the medical electronics market is expected to reach US$372.4 billion by 2018 [6]. Microsystems will undoubtedly make up a significant portion of this market as many new applications emerge.

The Wireless Microprocessor Group at the University of Utah has traditionally been involved in designing systems for biomedical applications such as cochlear prostheses [7] [8] or decoding spoken words using local field potentials recorded from the cortical surface [9] [10]. Our experience with these diverse, yet closely related from the circuit design perspective, applications led us to identify several areas where we can contribute to the state-of-the-art research in microsystem development. Several applications that our group is currently developing are described in this chapter and will be used to demonstrate the motivation for our work.

2.2 System for Electromodulated Release of Nitric Oxide

Nitric oxide (NO) is a colorless, toxic gas produced by the oxidation of nitrogen. An NO molecule is created when a nitrogen atom combines with an oxygen atom. Despite the fact that it is a simple molecule, NO plays an important regulatory role in the human body, enabling the blood to flow easily through the veins. In fact, NO was named the "Molecule of the Year" in 1992 after the Nobel Prize winning discovery of its role in the blood circulatory system.

The cardiovascular system produces NO naturally to prevent blood platelet activation (thrombosis) and bacterial growth (infections). When a medical procedure such as inserting an intravascular catheter or implantable vessel is performed, the foreign material inserted into the bloodstream lacks the ability to produce NO and the risk of clotting and infection rises rapidly. Clotting on foreign material in the body is currently often controlled by injection of dilute heparin solution, but there is a potential risk of systematic anticoagulation and heparin sensitivity. It is also estimated that 80,000 catheter-related bloodstream infections occur in patients in the United States each year, resulting in as many as 28,000 deaths [11]. The current approach to controlling catheter infections is by cleaning the access site and applying antiseptic catheter coatings. This method, however, frequently results in swelling of the insertion site.

Besides injecting heparin, an alternative approach to protect foreign materials in contact with blood from coagulation and infections has been successfully tested. This method involves coating the surface of objects inserted into the blood stream with NO-releasing polymeric films [12]. This approach has been shown to improve biocompatibility of intravascular chemical sensors. However, the duration of time the polymeric film retains its ability to release NO is limited, making this method futile in chronic and permanent catheters.

Recently, professor Meyerhoff's research group at the University of Michigan has developed a novel method of releasing NO through an electrochemical reaction. This method electrically controls the release of NO through polymeric materials from a stable nitride electrolyte reservoir as depicted in Fig. 2.1 [13].

The reservoir is made of silicone rubber and contains two electrodes; a reference Ag/AgCl electrode and a working electrode made of a copper wire. The reservoir is filled with inorganic nitric salt (NO_2). Application of voltage pulses of specific amplitude and duration creates a chemical reaction on the surface of the working electrode, resulting in formation

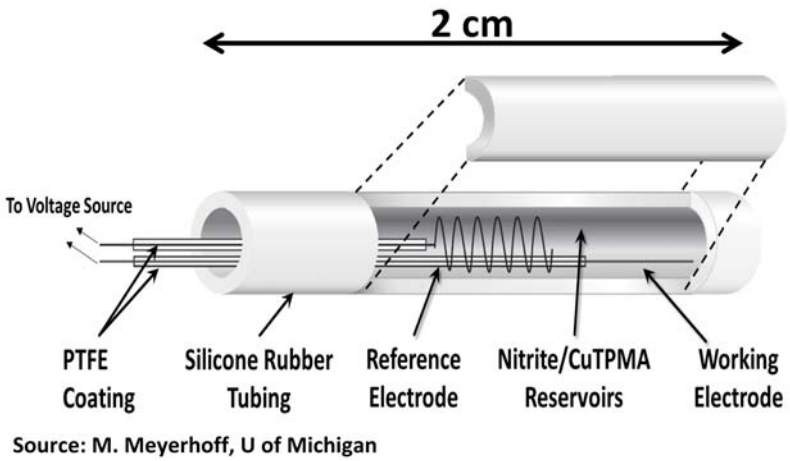


Fig. 2.1. Schematic of an electrochemically modulated NO release catheter.

of NO molecules as described in Equation 2.1. These free NO molecules are released to the bloodstream through the silicone coating.

$$Cu^{+} + NO_{2-} + 2H^{+} \rightarrow Cu^{2+} + NO + H_2O \tag{2.1}$$

The voltage applied to the electrodes must be of alternating polarity to provide a continuous redox reaction producing the NO. The amplitude and duration of the electrical pulses have been determined experimentally. For maximum NO production, the electrical signal alternated between -0.70 V for 30 seconds and +0.20 V for 30 seconds. Experimentally observed NO flux over a period of several hours, during which the reaction was repeatedly turned *ON* and *OFF*, is captured in Fig. 2.2. The amount of NO flux optimized for each application can be adjusted by appropriate combinations of pulse amplitudes and durations. Moreover, some applications require continuous production of NO, while other applications only need to perform NO production on demand.

For the purpose of technology validation, our group had designed a prototype of a microsystem suitable for *ex vivo* testing on small animals. The system prototype, depicted in Fig. 2.3, was built from commercially available components and is fully programmable to generate control signals of desired amplitudes and duty cycles.

Laboratory experiments confirmed that the microsystem performed identically to a commercial laboratory potentiostat used as a reference. Measured NO flux from the experiment, driven first by the potentiostat and then by the microsystem, is captured in Fig. 2.4. Subsequent short-term *ex vivo* experiments on rabbits confirmed a significant difference in catheter clotting when NO was introduced and when it was not. Fig. 2.5 shows three catheters that were implanted in rabbits for six hours. Catheter 1 and 2 were generating

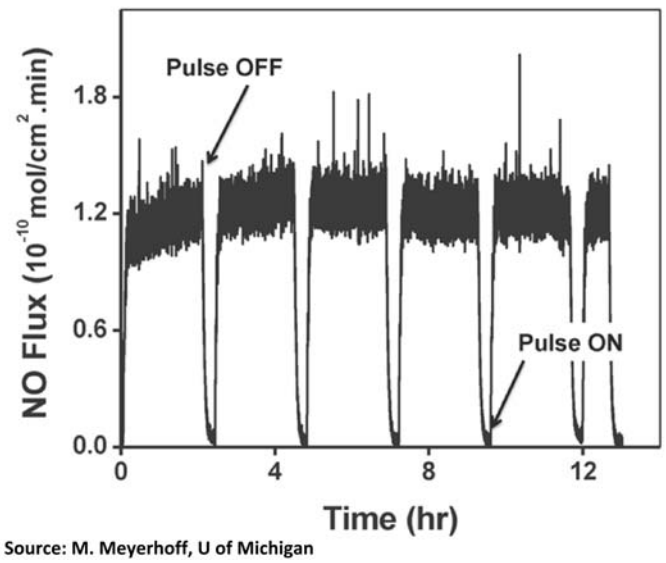


Fig. 2.2. Nitric oxide flux released from a 2 cm catheter.

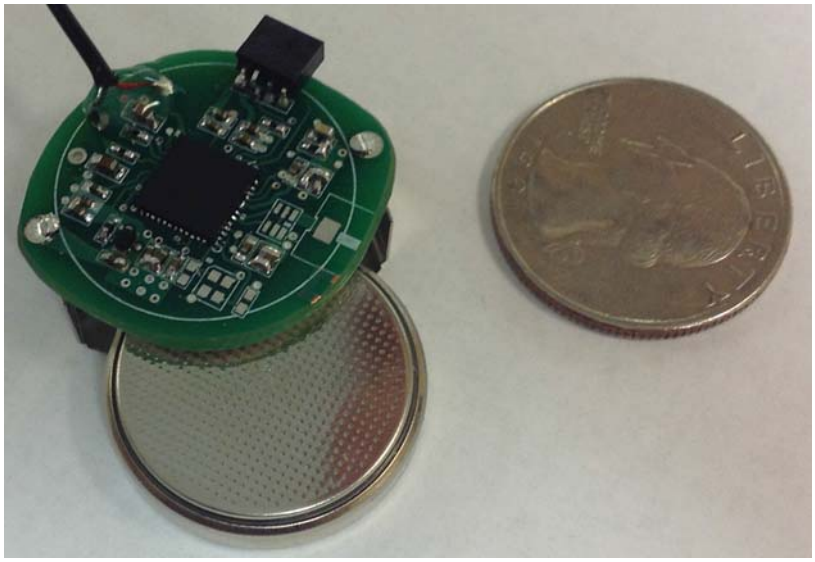


Fig. 2.3. Fully programmable NO system prototype built from commercial components.

1.0x10^{-10} and 0.9x10^{-10} mol min^{-1} cm^{-2} of NO, respectively. Catheter 3 (Control) did not have the ability to produce NO. Catheter 2 clearly shows less coagulation than catheter 3 and catheter 1 with the higher level of NO production showing almost no clotting at all.

Experiments performed on rabbits prove that the technology is viable and the collected data serve well as a proof of concept. However, long-term *in vivo* experiments are now needed to further validate the technology. Opportunities for further improvements in the microsystem's power efficiency and miniaturization are, however, limited if constrained

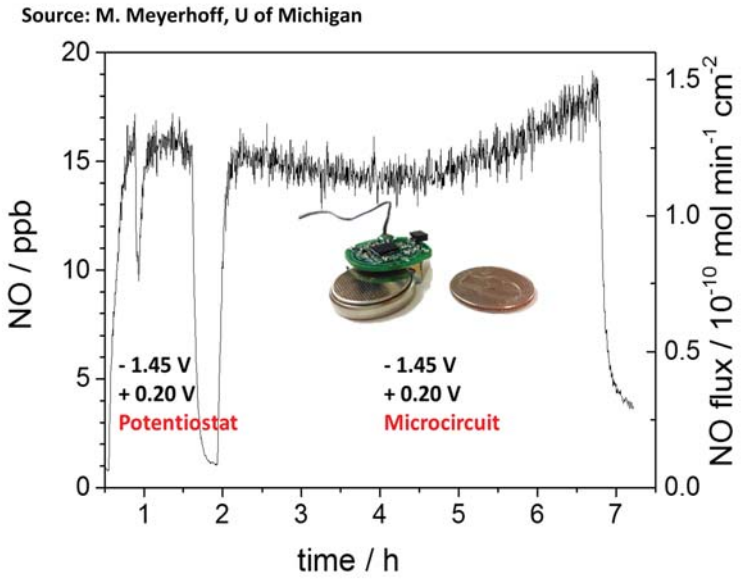


Fig. 2.4. NO flux generated by potentiostat and Utah system prototype.

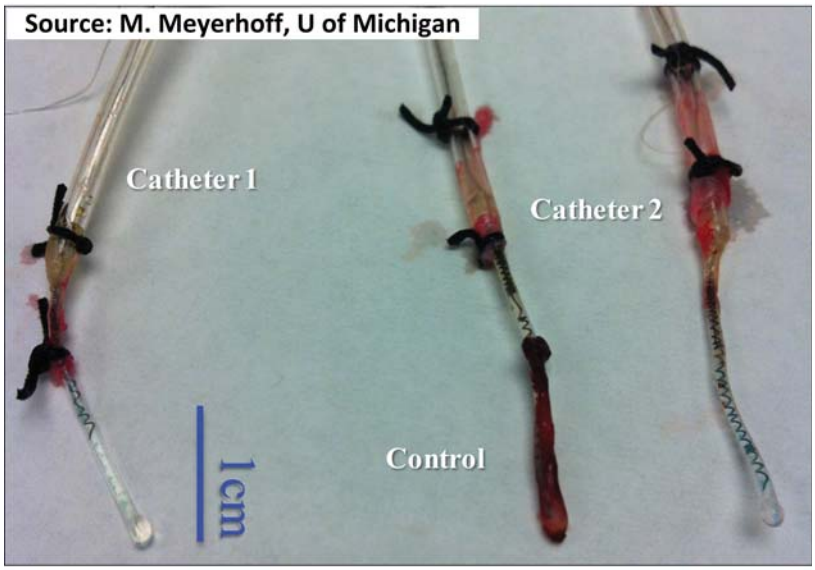


Fig. 2.5. Short-term *in vivo* clotting with electromodulated NO release catheters.

to using standard commercial components. To move this research forward, a significant investment in a custom-designed system-on-a-chip (SoC) is required. Nearly all emerging biotechnologies that require *in vivo* experiments are susceptible to this high cost of development and for some new ideas, the cost may result in the idea not being explored further.

To demonstrate further how wide the microsystem application range is, two more applications are presented in the following subsections. Collectively, these three applications

reveal how a custom-designed SoC with carefully defined specifications could form a new cost-effective prototyping platform for *in* and *ex vivo* biomedical research.

2.3 Smart Intra-Vaginal Ring (S-IVR)

Many research groups around the world, including the Microbicide Delivery Lab at the University of Utah, are working on developing technologies to suppress the global HIV/AIDS epidemic. One area of this effort is focused on developing pre-exposure prophylaxis (PrEP) technologies for men and women to prevent sexual transmission of HIV. Intra-vaginal rings (IVR) have been developed to release antiviral drugs to prevent the spread of HIV in women. Recently, clinical tests have been conducted in communities in Sub-Saharan Africa. Unfortunately, the studies failed to confirm the effectiveness of the microbicides delivered by the IVRs. It is suspected that the failure might have been due to inaccurate usage data, which were self-reported, rather than true inefficiency of the microbicides themselves. It is likely that attention to the social context of IVR use in the geographical region was inadequate, resulting in untruthful data reporting by the study participants [14]. A Smart-IVR (S-IVR) capable of collecting usage data automatically and without user involvement would be very beneficial for the evaluation of microbicide efficacy. Additionally, S-IVRs could be useful in other applications such as fertility assistance.

Our research group, in conjunction with the Microbicide Delivery Lab, is designing the circuits required to implement an S-IVR. Fig. 2.6 shows a computer rendering of the proposed system. The ring is fabricated from an elastic polymer capable of slow release of a microbicide. The ring also encloses a miniature electronic system with a battery and sensors. The microsystem includes sensors for measuring conductivity, pH, and temperature of the surrounding environment, which is sufficient information to interpret user's sexual activity. It periodically records the measurements for a period of one month. Upon the ring's removal, it is wirelessly read and recorded data are retrieved before the system is disposed.

It is clear that the S-IVR can only be implemented with an electronic microsystem that is very small, power efficient, and inexpensive. Similarly to the NO releasing microsystem described in the previous subsection, the S-IVR must be custom-designed to have minimum external components and it must include specialized circuitry to accommodate the chemical sensors and wireless data transmission. There are several important similarities among the two systems, suggesting that the SoC can be designed to fit both applications.

From the design perspective, many internal circuits are identical for both applications. Both systems require a processing unit (CPU) capable of scheduling events, controlling pe-

Fig. 2.6. Smart intra-vaginal ring for HIV research.

ripherals, and processing and storing data. Internally, both SoCs require circuits to generate stable voltage and current references, clock generator, sleep timer, voltage regulators, and a communication interface. The set of peripherals is what differentiates the two applications. The NO releasing application requires a digital-to-analog converter (DAC) and an amplifier with a low output resistance to drive the chemical reaction. The S-IVR, on the other hand, requires a specialized analog-to-digital converter (ADC) and an amplifier with a high input impedance to interface the chemical sensors. With the high level of integration that modern CMOS processes offer, all the required circuits can be integrated on a single die measuring only one or two mm^2. Giving the peripherals the capability of being selectively turned *ON* and *OFF* by the CPU keeps the SoC power efficient and suitable for both applications.

This concept of a single SoC for multiple applications can be extended to many more applications. One additional application in which our group has been involved is presented in the following subsection to demonstrate the application radius of biomedical technologies that can be covered with a single SoC.

2.4 Neural Recording System

Neural recording systems (NRS) have been a subject of research for several decades and have undergone extraordinary advances over the years. These systems are frequently referred to as brain-machine-interfaces (BMIs). Several types of sensors have been developed for NRS research. EEG, ECoG, microECoG, and microwires are perhaps the most commonly used sensor technologies. Although the electronic front-ends used to interface

these sensors vary by technology, there is one commonality that NRSs share with most implantable microsystems: the need for wireless communications. This commonality is therefore addressed in our work. A wireless telemetry system is implemented in our SoC to make it an effective tool for advanced research.

Often, BMI systems physically attach the neural electrodes to an electronic system that provides signal amplification, conversion, and signal processing, effectively tethering the patient to a hospital bed in an intensive care unit. These systems are often physically large, consume a large amount of power, and increase the chance of infections in the patient. A more practically useful system should leave the patient untethered and operate very efficiently to allow long runtime from a single miniature battery. Furthermore, a safe system should minimize the risk of infection, which is usually highest at the physical connection between the electrodes and the hardware, where tissues are exposed.

To address the problem of patients' limited mobility and risk of infections, some recent BMIs employ a high level of integration and use various wireless technologies to avoid physical connection through the scalp. One currently used configuration of a wireless BMI is depicted in Fig. 2.7. In this case, the neural array placed in the brain cortex is connected with microwires through the skull to a wireless microsystem placed in between the scull and the skin [1]. Although this configuration effectively reduces the risk of infections, the system is susceptible to failure due to defects in the microwires.

Improved reliability could be achieved by enclosing the microsystem with battery, ASIC, and a wireless data link into one compact package, which would rest on top of the brain cortex. Fig. 2.8 shows that this configuration effectively eliminates microwires running

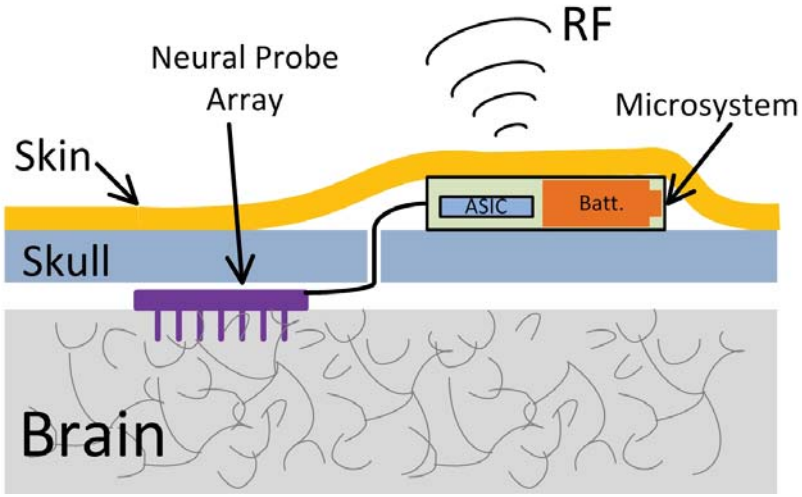


Fig. 2.7. BMI implementation with microwires.

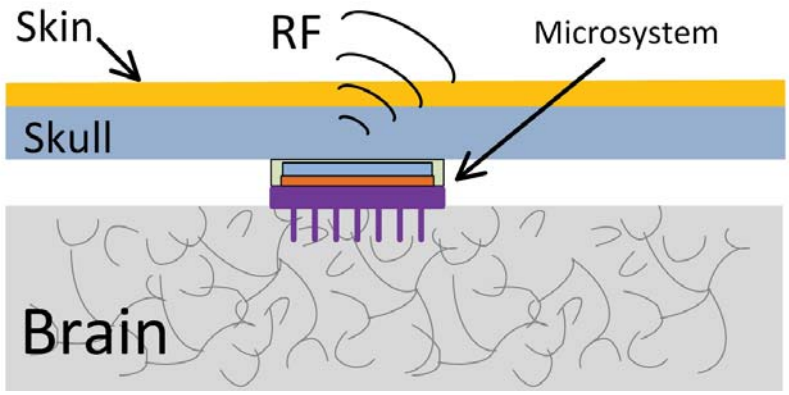


Fig. 2.8. BMI implementation eliminating microwires for improved reliability.

through the skull. Modern technologies allow designers to achieve very high levels of integration and compact packaging. The challenge, however, is to design a wireless data link that is capable of transmitting data through the skull at sufficient data rates while operating at very low power levels. This work investigates in detail one promising wireless technology and also investigates its suitability in both described microsystem configurations.

2.5 Summary

The three microsystem applications presented in this chapter identify several important aspects of modern biomedical research. It is clear that future research will be driven by miniature electronic devices that are capable of interfacing a wide range of electrochemical sensors, sophisticated signal processing, storing a large amount of data, and communicating wirelessly with external digital equipment. All this functionality has to be achieved at a low cost, enabling single or short-term use of the devices. Naturally, biomedical microsystems must be very power efficient to allow the use of miniature batteries, while still providing sufficient experiment time. Furthermore, the presented applications demonstrate that wireless telemetry is essential to both *in* and *ex vivo* applications.

The diversity of current biomedical research dictates that microsystems must be developed and customized for each new application and this is particularly true of the wireless telemetry. There are many different wireless standards and techniques. Each technique offers a distinct set of benefits and drawbacks and must be very carefully selected to meet the exact specifications of each application. Some applications, such as the S-IVR, have low data rates and short transmission distance. The neural recording system, on the other hand, requires very high data rates over an extended transmission range. Because of this diversity, a high level of customization is required for each application.

During the initial evaluation of every new technology, system prototypes are used to validate new hypotheses and serve as proofs of concept for commercialization and fundraising. Typically, the first generations of prototypes are designed from standard commercial components such as microcontrollers, amplifiers, and data converters. These prototypes, however, very rarely achieve desired battery life, miniaturization, and accuracy. For advanced long-term experiments, custom SoCs are usually necessary to meet desired specifications. Custom designs, however, are often prohibitively expensive.

In our effort to address some of these issues, we have developed an SoC that is suitable for rapid and cost-effective prototyping of emerging technologies. It offers very low power consumption and a small form factor. From our previous work, we have identified a set of interfaces that are frequently used in biomedical and chemical research and these interfaces are included on the SoC. All sensors required to implement the S-IVR (pH, temperature, and conductivity) can be directly connected to the microsystem. Moreover, almost any other resistive sensor or ISE can be connected through the integrated interfaces. The on-chip peripherals can also drive chemical reactions by setting the appropriate voltages or currents across electrodes. These interfaces make the system modular and suitable for a wide range of future applications. We have also implemented a wireless telemetry that is well suited for a wide variety of emerging technologies, from applications such as the S-IVR, with low data rates, up to applications with high data rate demand, such as the neural recording system. All integrated peripherals can be turned *ON/OFF* in firmware, giving the system great flexibility and efficiency.

CHAPTER 3

UTAH INTEGRATED MICROSYSTEM

3.1 Background and Motivation

Modern technologies have enabled design of electronic systems with unprecedented functionality. For biomedical devices that are used for *in* and *ex vivo* experiments on untethered animals, miniaturization and low power consumption are perhaps the two most challenging aspects of system design. This is particularly true for systems that are designed for use on small animals such as laboratory mice and rabbits. The form factor of the electronic microsystem is typically defined by the number of components required to build the system. It is also defined by the size of the battery needed to operate the device for the duration of the experiment. Therefore, high-density electronics with optimized power consumption are needed to support many studies conducted using animals.

The main goal of this work is to design an integrated microsystem to be used as a tool for prototyping emerging biomedical applications, reducing the cost of custom designing a new system for each new application. Throughout our long-term involvement in designing such systems, we have compiled a list of frequently used sensor interfaces and peripherals. We have also evaluated the trends in newly emerging sensors and signal processing procedures and included this knowledge in our consideration of which interfaces and peripherals should be integrated on our microchip.

3.1.1 Resistive Sensors

Perhaps the simplest and most commonly used sensors are those in which electrical resistance changes according to the physical or chemical property of interest - resistive sensors. Temperature, blood pressure, or the presence of chemicals can be detected or measured with resistive sensors. These sensors are typically driven by a source of constant electrical current with a known magnitude, as shown in Fig. 3.1. The voltage across the sensor is proportional to the property of interest. The voltage across the sensor needs to be accurately measured. The sensor's resistivity, which according to Ohm's law is simply V/I,

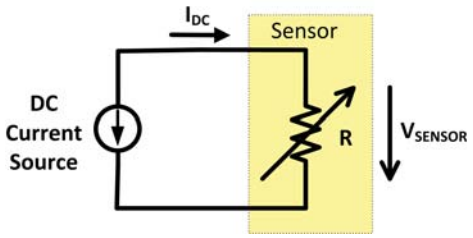


Fig. 3.1. Resistive sensor operation.

is then mathematically converted to the parameter of interest. From the circuit designer's perspective, the peripherals required to interface resistive sensors are a direct current (DC) source and an analog-to-digital converter (ADC).

3.1.2 Ion-Selective-Electrodes

Another group of sensors frequently used in biomedical and chemical research are ion-selective-electrodes (ISE). The basic measuring principle of an ISE is depicted in Fig. 3.2. An external reference electrode measures the potential of the solution independent of ion concentrations. The ISE itself (left side) consists of an Ag/AgCl electrode submerged in a known reference solution, which is separated from the analyte solution (measured) by a polymeric membrane. The membrane is doped with an ionophore designed to bind with the specific ions that are the subject of measurement. Charge separation at the surface of the membrane, which is due to the selective binding of ions, results in a potential difference between the external and internal reference electrodes. There are many types of ionophores commercially sold, and new technologies, focused on ISE miniaturization, are emerging. A leading firm in ISE miniaturization is e-SENS, Inc. in Salt Lake City, UT, which kindly provides our group with miniature pH, conductivity, and temperature sensors for the development of the IVR. Appendix A captures images of the sensors as well as results of sensor structural analysis and performance evaluation.

The voltage developed between the ISE and reference electrode needs to be measured with an electronic circuit that has very high input impedance. Low impedance in the circuit would cause a current to flow through the electrodes, driving the system away from equilibrium, and thus reducing the accuracy of measurement. Therefore, the system must include an analog front-end with very high input impedance.

3.1.3 Chemical Actuators

In addition to interfacing resistive sensors and ISEs, biomedical and chemical research devices frequently need the ability to drive chemical reactions such as the release of nitric

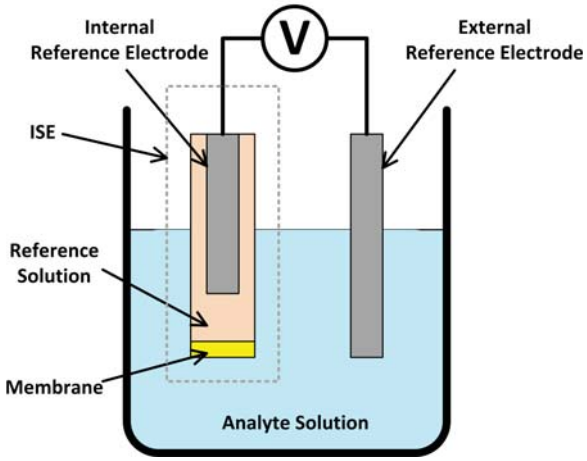


Fig. 3.2. Ion-selective-electrode principle.

oxide. Redox reactions are typically driven either by a controlled current or voltage. In both cases, the current driving capability needs to be considered during the design stage. Typically, redox reactions actuated by battery powered microsystems require currents on the order of several milliamps. A practical system, therefore, should include a programmable current source and a programmable voltage source with low output impedances.

3.1.4 Microsystem Requirements

To design a truly modular microsystem that can serve in a variety of applications, a central processing unit (CPU) that schedules tasks, performs signal processing, and controls data acquisition is needed. The CPU should offer sufficient computational power for applications with complex data processing algorithms such as neural signal recorders, and should also offer power efficient modes of operation for application with light processing demand such as the NO releaser or S-IVR. Furthermore, *in* and *ex vivo* experiments greatly benefit from wireless data transmission and wireless powering for long-term experiments. Therefore, appropriate RF interfaces should be included in the system to accommodate these requirements. Table 3.1 summarizes the requirements for a practical microsystem that would be suitable for many biomedical and chemical research applications. To maximize the benefits of the system, the number of external components should be minimized.

3.1.5 Existing Commercial Microcontrollers

With the microcontroller market reaching $15.7 billion in 2011 and still growing rapidly [15], there are many microcontrollers available for designers to select from. Microcontrollers for biomedical and chemical research, however, usually have a set of requirements that is not

Table 3.1: **Peripherals required for biomedical and chemical research microsystem.**

CPU + memory
Programmable current source (multiple channels)
Analog-to-digital converter (multiple channels)
Digital-to-analog converter (multiple channels)
Internal clock generator (programmable frequency)
Wireless telemetry (low power, high data rates)
Wireless powering
Sleep mode capability (programmable sleep period)

well served by the commercial products. Although there are several semiconductor manufacturers that are developing microcontrollers for the healthcare industry, the specificity of each new application and the low-volume character of the research and development sector make it challenging to find parts that enable experiments on untethered animals. Table 3.2 captures several microcontrollers that offer low-power operation and a set of peripherals close to our needs. It can be seen, however, that no one microcontroller has all of the peripherals that we identified as essential for experiments on untethered animals. To the best of our knowledge, there is currently no microcontroller available that would meet our specifications.

3.1.6 Proposed Utah Microcontroller Architecture

Considering all the described criteria for the SoC, we have designed a system architecture captured in Fig. 3.3. The SoC implementation offers significant computational capability thanks to a powerful 16-bit microprocessor with 32 kB of integrated SRAM.

Table 3.2: **Overview of selected commercial microcontrollers.**

Peripheral	TI CC430	TI RF430FRL	Silicon Labs Si106	Silicon Labs C8051F396
CPU + memory	✓	✓	✓	✓
Programmable current source (PCS)				
Analog-to-digital converter (ADC)	✓	✓	✓	✓
Digital-to-analog converter (DAC)				✓
Internal clock generator	✓	✓	✓	✓
Wireless telemetry	✓	✓	✓	
Wireless powering (rectifier)		✓		
Sleep mode capability	✓	✓	✓	✓

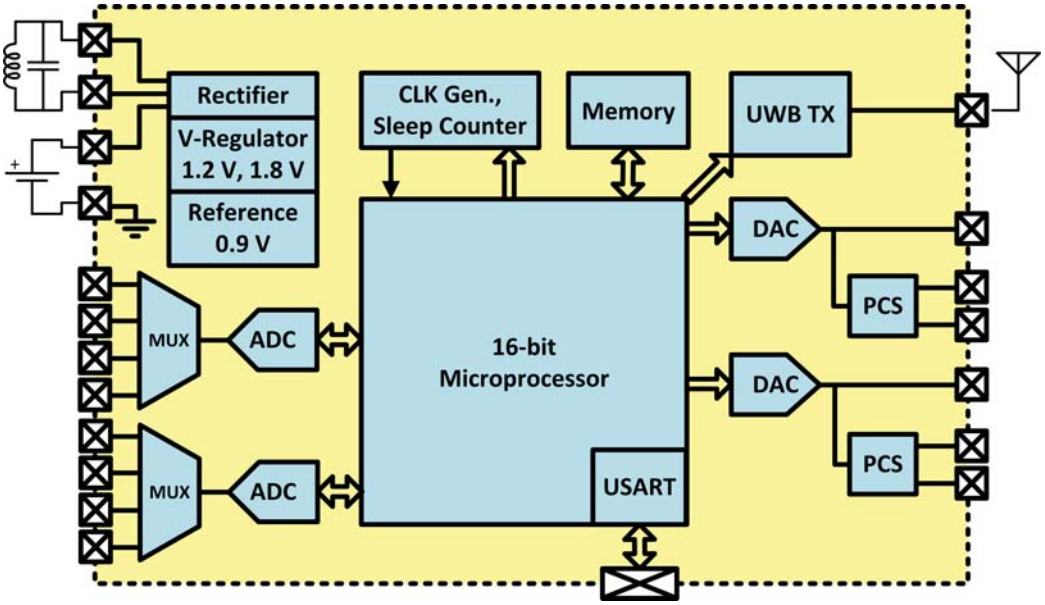


Fig. 3.3. Utah microsystem architecture.

Integrated peripherals include two four-channel 12-bit ADCs, two 10-bit DACs, and two programmable current sources (PCS) for sensor excitation. Additionally, the system has a wireless UWB data transmitter, programmable internal clock source, voltage reference, and voltage regulators.

The aim of this work is to achieve advanced integration of peripherals suitable for biomedical and chemical research. The goal is to enable single-chip prototypes that, due to their high integration, facilitate quick deployment in *in* and *ex vivo* research experiments, eliminating the need for custom-designed microchips, which are often cost-prohibitive. The following sections describe the design choices and procedures for all major system building blocks.

3.2 Digital Core

Nearly all *in* and *ex vivo* experiments require a sophisticated microsystem with the ability to process data, schedule processes, control peripherals, and manage data storage and transmission. The Wireless Integrated Microsystems group (WIMS) has previously developed a custom microprocessor for implantable biosensor systems. Its first generation was designed, fabricated, and fully tested in a 0.18 um CMOS process [8] [16]. Recently, it was redesigned and customized by our group to investigate methods of efficient high-bandwidth data processing in power-restricted environments [17]. For this purpose, the digital core was fabricated and verified in a 65 nm CMOS process. The microcontroller's

features include high customizability, scalability, and high power efficiency, which make it an excellent candidate for the proposed system.

The digital core includes a 3-stage pipeline, 16-bit datapath, 24-bit unified address space, and 32 kB of integrated SRAM. The instruction set contains 89 instructions supporting eight addressing modes and single- and multiword arithmetic, shift, logical, and control-flow operations. The scope of work needed to implement the WIMS microprocessor in a submicron CMOS process dictates that it be a collaborative effort. Previous students and current peers, whose excellent work made the microprocessor possible, are gratefully recognized [1].

The digital core including the pipeline and memory, fabricated in a 65 nm CMOS process, occupied 0.96 mm^2 of silicon area. Power consumption of the fabricated chip was measured for several combinations of V_{DD} and frequency and is plotted in Fig. 3.4 Complete test results and detailed description of the microprocessor have been published in [18] [17].

Fig. 3.4 indicates that the microprocessor can operate very efficiently at low frequencies, which is desirable for low-performance applications such as the S-IVR. It can, however, operate at high frequencies in applications such as a neural interface [19]. The operating frequency can be controlled dynamically in the firmware. Peripherals were connected to the core through a set of memory-mapped registers. Detailed electrical specifications and the user's manual for the WIMS architecture are available in [20].

[1]Matthew Guthaus, Robert Senger, Eric Marsman, Spencer Kellis, Nathaniel Gaskin, Bennion Redd

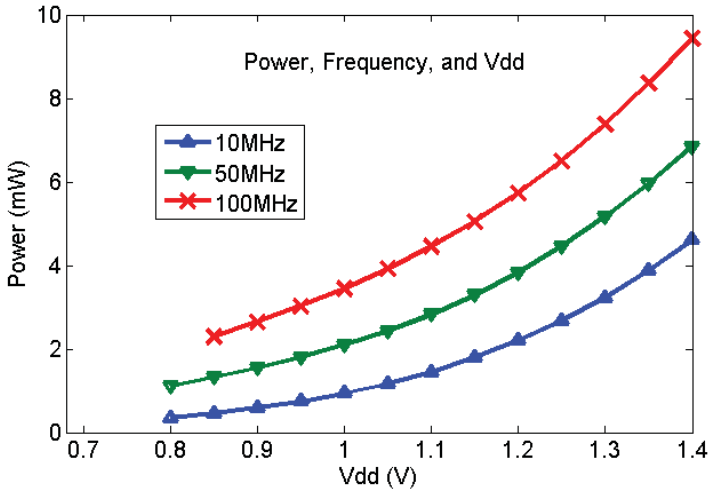


Fig. 3.4. Measured power dissipation profile of WIMS digital core.

3.3 RF Powering

Achieving sufficiently long-lasting power supply is often problematic in implanted microsystems and systems attached to untethered animals. Power efficiency of the electronic device is therefore critical and ultimately limits the maximum duration of an experiment. Commonly, a miniature primary battery is used to supply power for the entire time of testing. Such an approach, however, effectively limits researchers to short-term experiments. Long-term experiments on the order of days, weeks, or months are often needed. Systems for long-term experiments typically employ a secondary battery that can be recharged for prolonged runtime. Conventional plug-in methods for recharging, however, are cumbersome for experiments on untethered animals. Consequently, it is preferable for both *in* and *ex vivo* experiments to employ a wireless technique for recharging.

Near-field inductive coupling has been studied extensively for several decades. Applications ranging from Radio Frequency Identification (RFID) [21] [22], tire pressure monitoring [23], sensor networks [24] [25], to neural recording systems [19] [26], all use a Radio Frequency (RF) signal to transfer energy over a short distance. The transfer is realized through two inductively coupled coils placed in close proximity. The coils need to be axially aligned as shown in Fig. 3.5 to maximize the power transfer efficiency. The physical dimensions of the coils, number of turns, and displacement distance are all variables that need to be carefully optimized to fit each application's needs.

In the quest to design an SoC that fits various applications, and thus coil configurations, a tuning capacitor was left off-chip as shown in Fig. 3.3 to retain system flexibility. For testing and verification, however, a representative configuration for a shallow implant was considered. The design, optimization procedure, and measured results, using the model configuration, are described in the following paragraphs.

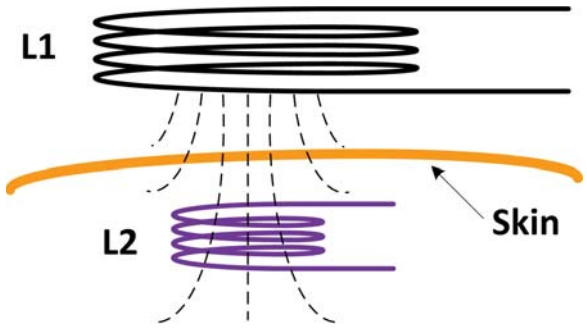


Fig. 3.5. Near-field inductive coupling.

3.3.1 Inductive Link Design

The electrical schematic of a typical inductive link is depicted in Fig. 3.6. The primary circuit consisting of C_1 and L_1 is tuned to resonate at a frequency of the AC voltage V_{IN}. R_1 is a resistor modeling the parasitic series resistance of L_1 and the output resistance of voltage source V_{IN}. Z_{REF} is a model of reflected impedance from the secondary circuit consisting of L_2, C_2, and R_{LOAD}. L_2 and C_2 are tuned to resonate at a frequency of the input voltage V_{IN} and R_{LOAD} is a resistor representing loading of the resonant tank. R_{LOAD} and I_{LOAD} model the power consumption of the entire SoC. R_{P2} is the parallel parasitic resistance of L_2.

For testing and verification, a configuration of coils representing a shallow implant was considered. In the model configuration, we considered the coils L_1 and L_2 to have a diameter D = 8 mm, number of turns N = 5, and separation S = 1 cm. The inductive link was then optimized for maximum power transfer efficiency. To ensure an accurate and realistic optimization procedure, coils were fabricated from a copper wire and characterized. Experimentally obtained parameters were used in the optimization procedure. The measured coil parameters are summarized in Table 3.3.

To optimize the inductive link, the mutual inductance M and coupling coefficient k must be known. In order to obtain these values, an experiment was designed and the coupling

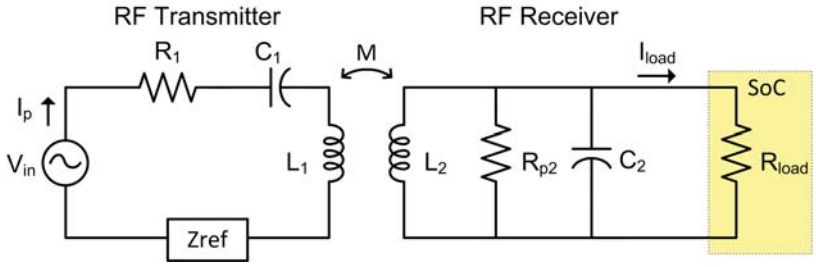


Fig. 3.6. Electrical model of an inductive link.

Table 3.3: Measured coil parameters.

Parameter		$L_1 = L_2$
Diameter	D	8 mm
Number of turns	N	5
Inductance	L	440 nH
Self Resonant Freq.	SRF	110 MHz
Peak Q	Q_{peak}	69@54 MHz
Series resistance (@20 MHz)	R_S	0.9 Ω
Quality factor (@20 MHz)	Q	61

parameters were mathematically derived from measured data. The experiment setup is shown in Fig. 3.7 and represents the circuit in Fig. 3.6. The primary coil L_1, separated from L_2 by 1 cm, was driven with a sinusoidal voltage $V_{IN} = 4$ Vpp at frequency f = 20 MHz. Frequencies between 1 and 50 MHz have been reported for biomedical implants [27]. Signals of higher frequencies, however, are susceptible to higher attenuation in organic tissues such as skin or bone [28]. Furthermore, high frequency signals are absorbed in tissues, potentially resulting in tissue damage due to heating [29] and power conversion inefficiencies. On the other hand, higher frequencies allow the use of smaller inductors and capacitors, which is desirable for miniature microsystems. We selected 20 MHz for our experiment to obtain the mutual inductance of the inductors. For maximum power transfer, inductors L_1 and L_2 have to resonate with capacitors C_1 and C_2, respectively. Resonance is achieved when Equation 3.1 is valid.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

The values of C_1 and C_2 were calculated and resonance experimentally verified. Table 3.4 summarizes the experimentally obtained parameters to calculate M and k. The value of the load resistor R_{LOAD} was selected arbitrarily and has no effect on the coupling coefficient.

The output voltage V_{LOAD} across R_{LOAD} was measured and used to calculate k and M using Equations 3.2 and 3.3.

$$Av = \frac{V_{LOAD}}{V_{IN}} \tag{3.2}$$

Av is the voltage gain, which is used proportional to the mutual inductance M:

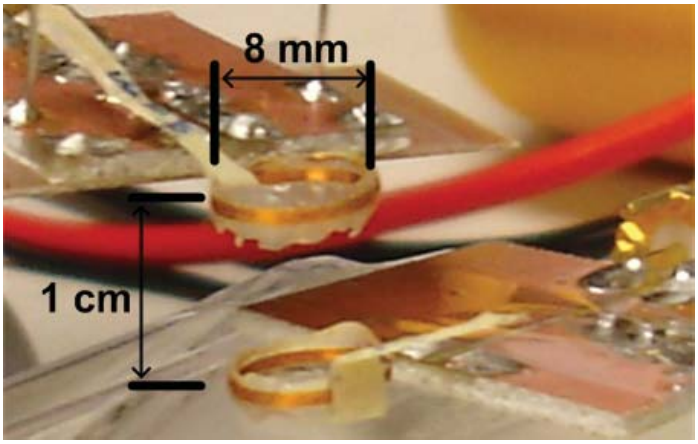


Fig. 3.7. Mutual inductance characterization experiment.

Table 3.4: **Inductive link model parameters.**

Parameter		Measured value
Tank inductance	$L_1 = L_2$	440 nH
Tank capacitance	$C_1 = C_2$	144 pF
Series resistance ($R_{SOURCE} + R_{SL1}$)	R_1	50.9 Ω
Equal parallel resistance ($R_{P2} = R_{S2} \cdot Q_{L2}^2$)	R_{P2}	3.35 kΩ
Load resistance	R_{LOAD}	5 kΩ
AC input voltage	V_{IN}	4 V_{pp}

$$Av = \frac{\omega^2 M L_2}{(\omega M)^2 + R_1 \frac{R_{P2}}{{Q_{L_2}}^2} + R_1 \frac{(\omega L_2)^2}{R_{LOAD}}} \tag{3.3}$$

$$M = k\sqrt{L_1 L_2} \tag{3.4}$$

Solving Equation 3.3 for M gives us M = 9.7 nH. Solving Equation 3.4 for k reveals the mutual coefficient k = 0.022. Consequently, the power transfer efficiency of the inductive link is calculated by Equation 3.5.

$$\eta = k^2 Q_1 Q_{L_2} \frac{\beta}{(\beta+1)^2} \tag{3.5}$$

where Q_1 is the quality factor of the loaded primary resonant tank, Q_{L_2} is the quality factor of the unloaded secondary resonant tank, and β is defined as:

$$\beta = \frac{Q_{L_2}\omega_0 L_2}{R_{LOAD}} = \frac{R_{P2}}{R_{LOAD}} \tag{3.6}$$

where R_{P2} is the equivalent parallel resistance of the secondary LC tank and ω_0 is the resonant frequency.

Equation 3.5 is an approximation that is valid only for weakly coupled coils where $k^2 Q_1 Q_{L_2} \ll 1$. It is a reasonable assumption for all implanted configurations where k is typically very low and Q_1 is lowered by the voltage source output resistance R_S.

For maximum power transfer efficiency, Equation 3.5 needs to be maximized. It can be observed that since k, Q_1, and Q_{L_2} are constants set by the coil configuration, Equation 3.5 is maximum when the term $\beta/(\beta+1)^2$ is maximized. A simple simulation shown in Fig. 3.8 reveals that $\beta/(\beta+1)^2$ is maximum when $\beta = 1$.

Setting $\beta = 1$ in Equation 3.6 yields a condition for maximum power conversion efficiency:

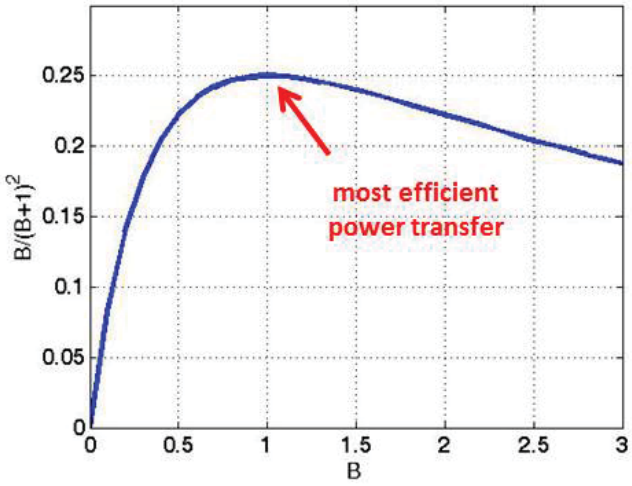


Fig. 3.8. Optimization of β for maximum power transfer efficiency.

$$R_{P2} = Q_{L_2}\omega_0 L_2 = R_{LOAD} \tag{3.7}$$

Equation 3.7 can be used to determine the inductive link's RF frequency, which delivers a desired current I_{LOAD} to a known load R_{LOAD} with maximum efficiency.

The measured and calculated mutual inductance parameters are summarized in Table 3.5.

3.3.2 Full-Wave CMOS Rectifier

With RF power coupled into the internal circuit, the AC voltage must be rectified to provide a DC voltage for charging the battery. There are several techniques for RF signal rectification. Perhaps the most frequently used are the single-wave rectifier, the full-wave rectifier, and the doubler. Half-wave rectifiers, consisting of a single diode and a filtering capacitor, are typically used in low-current applications [30] [31]. Their main benefit is the simplicity of implementation. Low efficiency and high ripple, however, make them problematic for high-current applications. Voltage doublers, which effectively consist of two half-wave rectifiers connected in series with two capacitors, suffer from similar drawbacks. They are usually used when high voltages and low currents are needed or when two voltage levels are needed for the application [32].

Implementation of several high-current rectifier topologies that decrease substrate leakage current and parasitic components, reduce the possibility of latch-up, and improve power transmission efficiency have been presented [33]. The Utah SoC is intended to serve in a

Table 3.5: **Mutual inductance parameters observed for two 8 mm inductors with 1 cm spacing.**

Parameter		Measured value
AC input voltage	V_{IN}	$4\,V_{pp}$
Coil separation	S	1 cm
AC output voltage	V_{LOAD}	$3.44\,V_{pp}$
Voltage gain	A_V	0.860
Mutual inductance	M	9.68 nH
Coupling coefficient	k	0.022

wide range of applications, some of which might require relatively high supply current to recharge their secondary batteries.

Besides recharging and energizing electronic systems, engineers have also been using near-field coupling for uni- or bidirectional data transmission. There have been many implementations published demonstrating data transmission [34–37] through inductive links. A brief analysis of near-field inductive telemetry is offered in Chapter 4. Although the current generation of the Utah SoC does not intend to implement telemetry through the inductive link, a full-wave CMOS rectifier was designed as proposed in [38]. The implementation is adequate for high-current low-loss applications and includes control circuits that allow backscattered communication. The rectifier's ability to modulate and transmit data will be evaluated and a backscattered communication link will be considered for future generations of the Utah SoC. The rectifier's schematic, derived from [38], is depicted in Fig. 3.9 and the component parameters used for the Utah implementation are summarized in Table 3.6. The *OC* (Open Coil) and *SC* (Short Coil) signals are digital inputs used for the backscattering telemetry and will not be used in this generation of the Utah microcontroller.

In subsection 3.3.1, a procedure for power-transfer efficiency optimization was described. Equation 3.7 was used to determine the RF frequency for achieving the highest transfer efficiency. It is clear, however, that not all of the current I_{LOAD} in Fig. 3.6 can be delivered to the final DC load (battery) due to losses in the rectifier. It is important to develop understanding of the relationship between loads seen at various stages of the AC to DC converter. Furthermore, if the inductive link is used to recharge a secondary battery, the DC load will change throughout the recharge cycle and the power transfer efficiency will not be maximized at all times. It is, however, possible to design a charging system, where the RF source (V_{IN}) will adjust the RF signal amplitude during the charging cycle to control the charging current. Understanding how the changing load affects the rest of the system

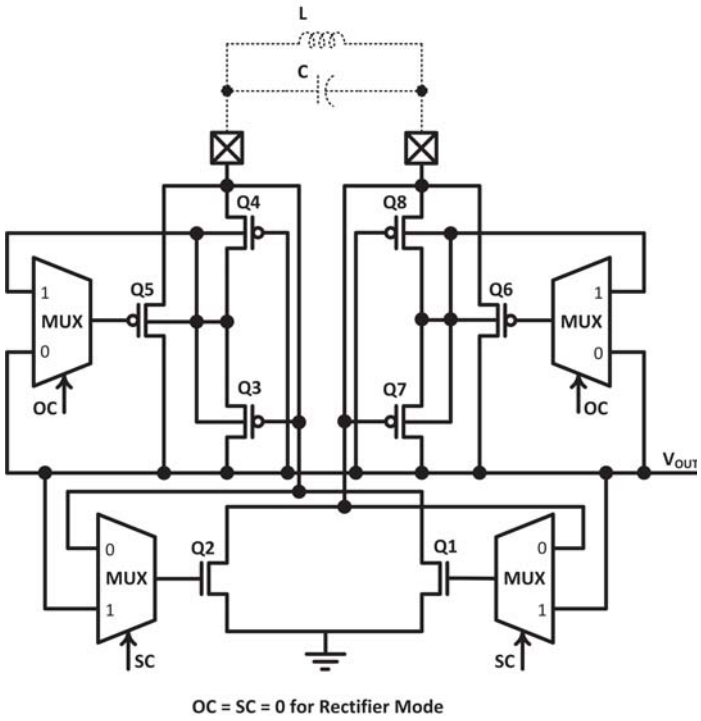


Fig. 3.9. **Electrical schematic of full-wave rectifier implementation [38].**

Table 3.6: **Summary of component values for full-wave rectifier.**

Device	Size
Q_1, Q_2	1960 μm/500 nm
Q_3, Q_7	10 μm/400 nm
Q_4, Q_8	10 μm/400 nm
Q_5, Q_6	4000 μm/400 nm

is crucial.

Fig. 3.10 captures the entire AC to DC conversion chain. An analysis is provided to gain an intuitive understanding of the system. R_{DC} is the load that is seen by the rectifier and it effectively represents the DC resistance of the SoC or SoC + battery. R_{AC} is the load seen by the RF receiver looking into the rectifier. R_{AC} is equivalent to R_{LOAD}, used in section 3.3.1.

The voltage drop across the rectifier and power distribution in the system can be expressed as:

$$V_{DROP} = V_{AC} - V_{DC} \quad \text{and} \tag{3.8}$$

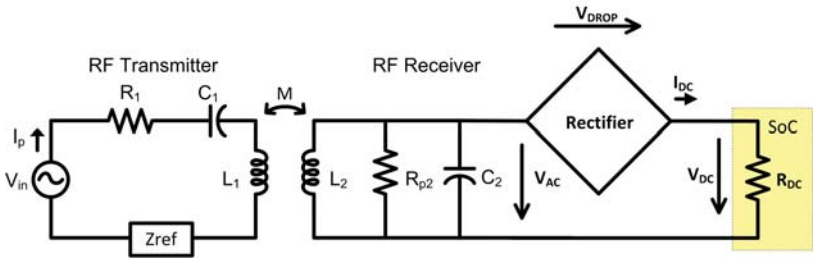


Fig. 3.10. Electrical schematic of the complete AC to DC conversion chain.

$$P_{AC} = P_{DROP} + P_{DC} \tag{3.9}$$

where P_{AC} is the average input power, P_{DC} is the power dissipated in the DC resistive load R_{DC} (chip, battery), and P_{DROP} is the power loss in the rectifier. Assuming that I_{DC} is the average current in the rectifier, Equation 3.9 can be expressed as:

$$\frac{V_{AC,rms}^2}{R_{AC}} = \frac{V_{AC}^2}{2R_{AC}} = V_{DROP}I_{DC} + \frac{V_{DC}^2}{R_{DC}}, \tag{3.10}$$

where R_{AC} is the equivalent AC load resistance seen by the secondary resonant tank, i.e., R_{LOAD}. Substituting Equation 3.8 for V_{AC}, Equation 3.10 yields:

$$\frac{V_{AC}^2}{2R_{AC}} = \frac{(V_{DROP} + V_{DC})^2}{2R_{AC}} = V_{DROP} \cdot \frac{V_{DC}}{R_{DC}} + \frac{V_{DC}^2}{R_{DC}}, \tag{3.11}$$

$$\frac{(V_{DROP} + V_{DC})^2}{2R_{AC}} = \frac{V_{DC}}{R_{DC}} \cdot (V_{DROP} + V_{DC}), \tag{3.12}$$

$$R_{AC} = \frac{R_{DC}}{2} \cdot (1 + \frac{V_{DROP}}{V_{DC}}). \tag{3.13}$$

Considering that V_{DROP} for the full-wave rectifier built in a 65 nm CMOS is approximately 1.4 V, one can calculate R_{AC} and use it as R_{LOAD} for setting optimum parameters of the inductive link as described in section 3.3.1. For example, assume that a microsystem with a secondary battery was characterized and requires a current of 500 μA @ 3.6 V $\rightarrow$ $R_{DC} = 3.6V/500\mu A = 7200\Omega$. Equation 3.13 gives $R_{AC} = 5000\ \Omega$ and from Equation 3.7, we obtain the optimum RF frequency $f_0 = 29.6$ MHz.

The rectifier was tested with an AC voltage source generating 4 Vpp sinusoidal signal at 20 MHz. The loading conditions were set to $R_L = 3$ kΩ and $C_L = 120$ pF. The rectifier's output voltage was measured to be 3 V as shown in Fig. 3.11. The measured ripple amplitude was 280 mVpp, which is 30 % higher than calculated. The ripple peak-to-peak amplitude V_r is a function of the DC loading current I_{DC}, AC input frequency ω, and loading capacitance C_L. It can be calculated as:

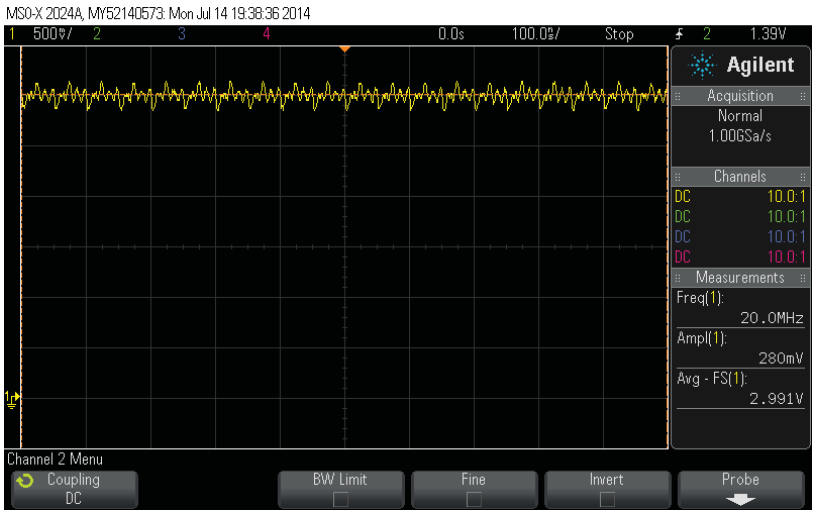


Fig. 3.11. Measured output voltage of the full-wave rectifier.

$$V_r = \frac{\pi \cdot I_{DC}}{C_L \cdot \omega}. \tag{3.14}$$

Alternatively, Equation 3.14 can be reordered and used to determine the loading capacitor C_L that is needed to meet V_r requirements of a specific application.

3.4 Voltage Reference

There are several blocks in the SoC that require a precise reference voltage to perform their function in the system. The DACs, ADCs, and voltage regulators all need a reference voltage that is independent of variations in power supply voltage (V_{DD}), temperature, and variations in the fabrication process. There are several standard methods to achieve a stable voltage reference. Since the 65 nm CMOS process offers bipolar junction transistors (BJT), a bandgap voltage reference circuit using two BJTs was selected. The bandgap's schematic is captured in Fig. 3.12.

This method of generating temperature-independent voltage is based on adding a voltage with a positive temperature coefficient and a voltage with a negative temperature coefficient. The voltage which increases with temperature is called *proportional-to-absolute-temperature* (PTAT) and the voltage which decreases with temperature is called *complementary-to-absolute-temperature* (CTAT). Detailed explanation of PTAT and CTAT voltage generators along with their design procedure is described in [39].

Generally, the bandgap reference circuit achieves the best performance when it is designed to produce V_{REF} around 1.25 V (due to the theoretical 1.22 eV bandgap of silicon at 0 K). The nominal power supply voltage for the 65 nm CMOS process, however, is 1.2

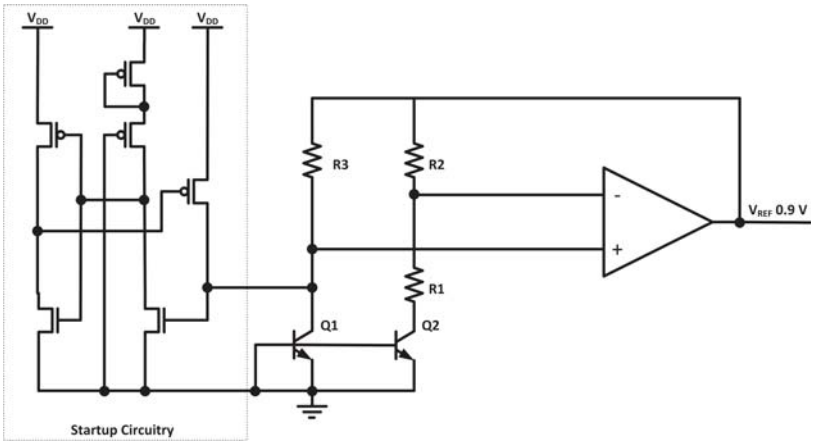


Fig. 3.12. Electrical schematic of bandgap.

V, restricting the maximum achievable V_{REF} to the 1 V neighborhood. Because the Utah SoC peripherals operate at 1.8 V, the bandgap circuit was optimized to produce V_{REF} = 0.9 V, which is the midpoint of the peripherals' power supply. Although reducing V_{REF} to 0.9 V reduces the bandgap's accuracy, it does not represent a significant problem for the intended biomedical application as both *in* and *ex vivo* experiments are typically performed in an environment with only small temperature fluctuations. Table 3.7 summarizes the component parameters used in the bandgap and Fig. 3.13 captures a simulation of the output voltage V_{REF} vs. power supply voltage V_{DD} for temperature range 0 - 50° C. The simulations indicate the bandgap's accuracy of 3.3 % within the temperature range. Fig. 3.14 captures simulated and measured V_{REF} vs. temperature, showing a measured 2.3 % accuracy over a 75° temperature range. Fig. 3.15 shows simulated and measured V_{REF} vs. V_{DD} at 25° C.

3.5 Power Management Circuits

There are three voltage domains on the chip. The pad ring, which drives signals in and out of the chip, operates on a 3.3 V supply. All of the on-chip peripherals, with the exception of the wireless transmitter (ADCs, DACs, and programmable current sources), operate at

Table 3.7: Summary of component values for voltage bandgap reference.

Device	Size
Q_1	1 μm/1 μm
Q_2	10 x Q_1
R1	1.00 kΩ
R2	2.97 kΩ
R3	10.34 kΩ

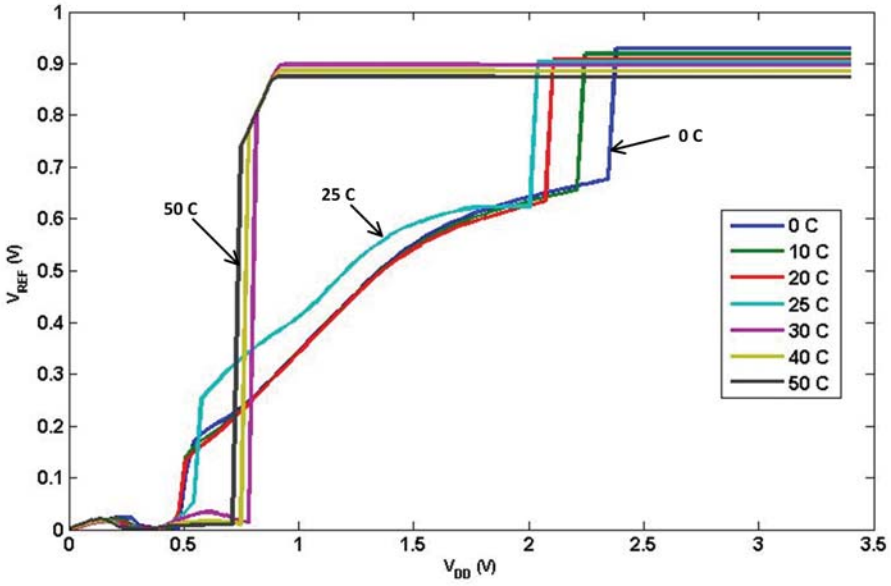


Fig. 3.13. Simulated bandgap accuracy for temperatures 0 - 50° C.

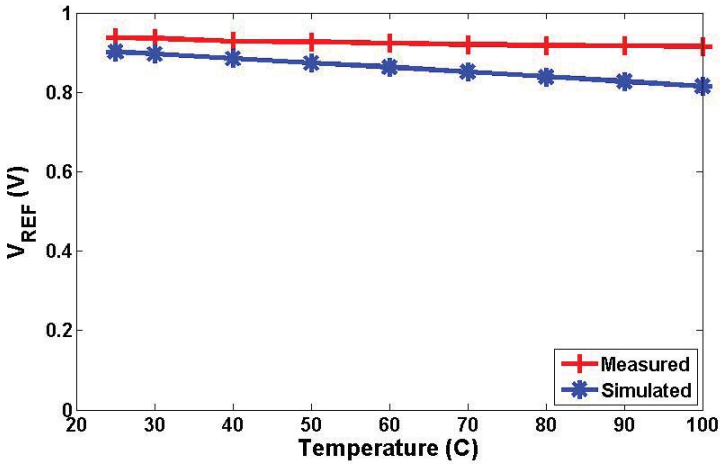


Fig. 3.14. Bandgap output voltage vs. temperature.

1.8 V to maximize their dynamic range. The digital circuitry, clock generator, and the wireless transmitter operate at 1.2 V to take advantage of the low-power properties of the advanced CMOS process. To manage all these domains, there are four voltage regulators on the chip, three of which can be independently turned *ON* and *OFF*. The input to all regulators is 3.3 V from the external battery. The chip is fully functional with power supply voltages from 2 V to 3.4 V. This range is adequate for primary batteries with chemistries such as Li/CFx or Li/MnO_2 or secondary $LiFePO_4$ batteries. When Li-Ion secondary

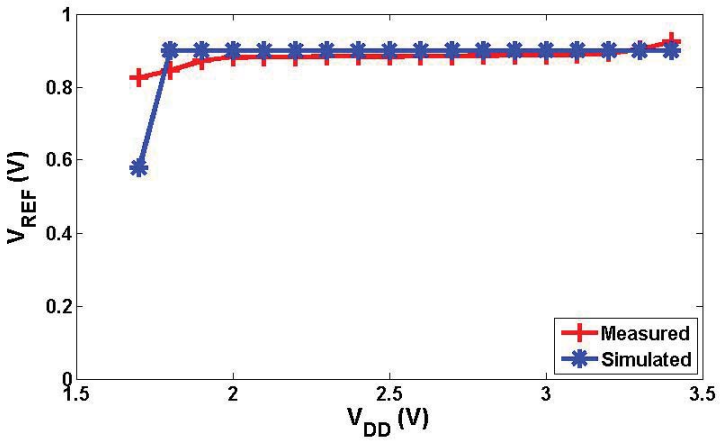


Fig. 3.15. Bandgap output voltage vs. power supply voltage (25° C).

batteries are used, one must ensure that the RF inductive link is designed in such a way that charging beyond 3.4 V does not occur.

Two regulators generate two independent 1.8 V supplies; each one is used for powering one DAC, one ADC, and one PCS. Additionally, there is one 1.2 V regulator on the chip, which supplies the digital microprocessor. It cannot be turned *OFF* but its output voltage can be reduced during sleep mode. The last regulator is operated as a unity buffer and supplies the wireless transmitter. A block diagram of the system indicating the independent power domains is depicted in Fig. 3.16.

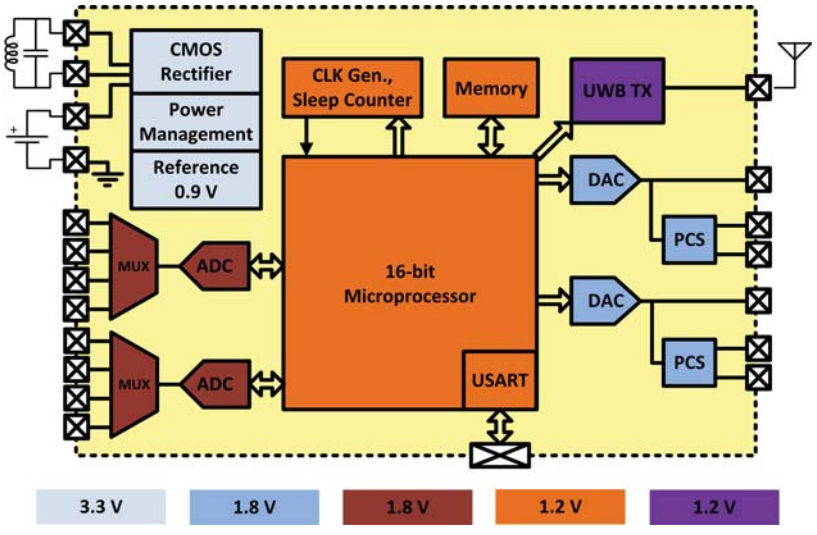


Fig. 3.16. Utah microsystem's power domains.

3.5.1 Regulator 3.3 V → 1.8 V

Low dropout (LDO) voltage regulator architecture was chosen for all on-chip regulators. This architecture has become the de-facto standard for on-chip regulators driving resistive loads with low current demand. A common CMOS implementation is captured in Fig. 3.17.

A rail-to-rail operational amplifier, briefly described in Chapter 3.9, was designed by a fellow member of our group. Stability of the voltage regulator was carefully evaluated for all possible loading conditions to ensure that oscillations do not occur. Loading conditions of 50 μA - 2 mA with load capacitance of up to 5 pF were simulated over temperatures 0 - 50° C to ensure stability. The power supply rejection (PSR) was simulated to be -51.2 dB @ 1 kHz. Fig. 3.18 captures simulated and measured V_{OUT} vs. temperature and Fig. 3.19 shows simulated and measured V_{OUT} vs. V_{DD} at 25° C.

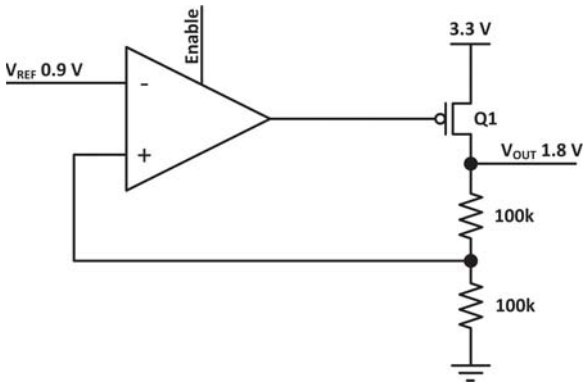


Fig. 3.17. Electrical schematic of 1.8 V LDO regulator.

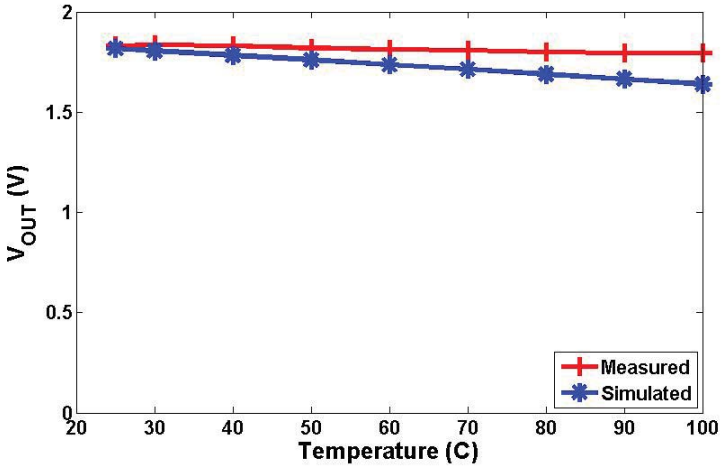


Fig. 3.18. 3.3 V → 1.8 V regulator output voltage vs. temperature.

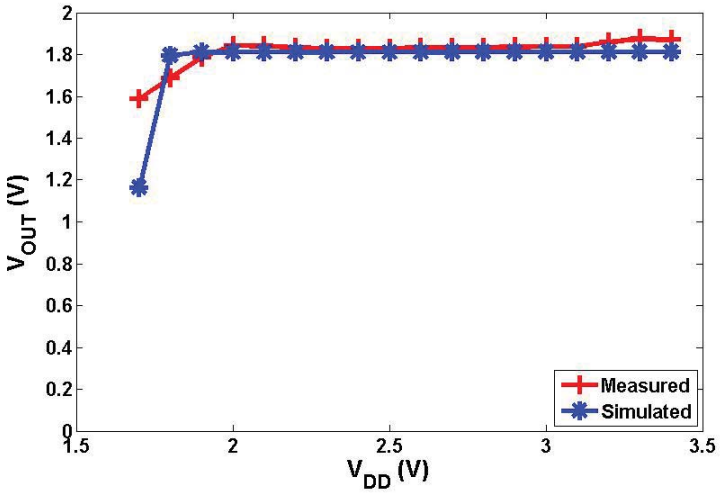


Fig. 3.19. 3.3 V → 1.8 V regulator output voltage vs. power supply voltage (25° C).

3.5.2 Regulator 3.3 V → 1.2 V

There are two 1.2 V regulators included on the chip. One, depicted in Fig. 3.20, supplies the digital core including clock generator, sleep timer, microprocessor, and memory. This regulator is always *ON* but its *Enable* signal reconfigures the regulator to supply 0.9 V instead of 1.2 V. This mode is used for reducing the power consumption during periods when sleep mode is activated. The sleep period can be programmed to last up to 50 days. Lower power supply to the core reduces leakage power, which dominates during the sleep period. Similar to the 1.8 V regulator, loading conditions 50 μA - 2 mA with load capacitance of up to 5 pF were simulated over temperatures 0 - 50° C to ensure stability. The power supply rejection (PSR) was simulated to be -51.1 dB @ 1 kHz. Fig. 3.21 captures simulated and measured V_{OUT} vs. temperature and Fig. 3.22 shows simulated and measured V_{OUT} vs. V_{DD} at 25° C.

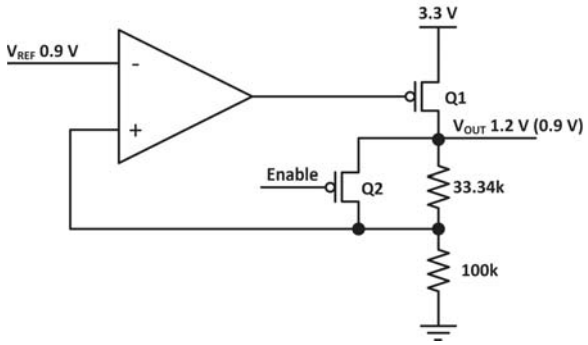


Fig. 3.20. Electrical schematic of 1.2 V LDO regulator.

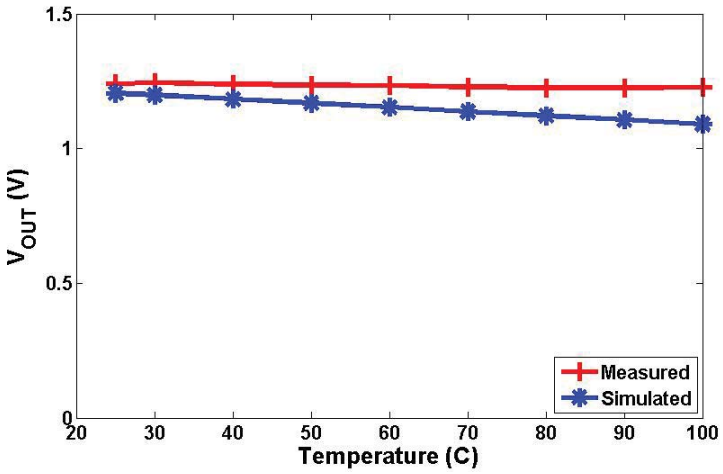


Fig. 3.21. 3.3 V → 1.2 V regulator output voltage vs. temperature.

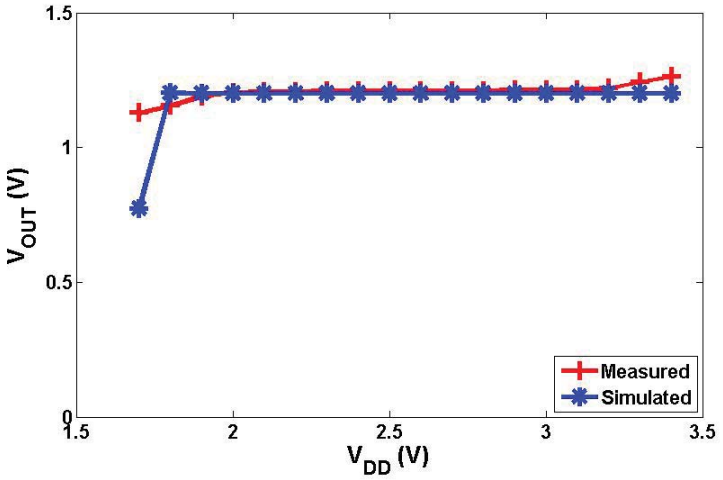


Fig. 3.22. 3.3 V → 1.2 V regulator output voltage vs. power supply voltage (25° C).

The on-chip wireless interface operates at 1.2 V but is typically *OFF* for most of the experiment runtime. When the transmitter is operating, however, it requires currents up to 5 mA and therefore, it has a dedicated regulator. Additionally, the transmitter requires an external filtering capacitor to achieve sufficient stability as described in Chapter 4.5. The regulator is designed as a unity-gain buffer that can be turned *ON* and *OFF* with the *Enable* signal as depicted in Fig. 3.23. Calculations and simulations revealed that the three-stage opamp, used throughout the SoC, was not sufficiently stable in unity-gain configuration when loaded with large capacitance. To ensure the regulator's stability, a two-stage opamp with its nondominant pole at more than 3x the frequency of the dominant pole was designed

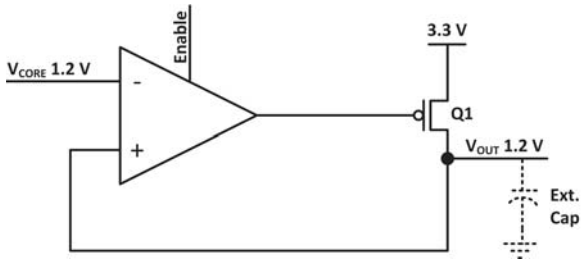


Fig. 3.23. Electrical schematic of 1.2 V V_{DD} buffer.

as depicted in Fig. 3.24. Simulated opamp's performance is summarized in Table 3.8. The regulator's stability and startup without excessive peaking was ensured over temperature corners and loads up to 0.1 μF supplying 15 mA of current, which is several times higher than expected for any possible configuration of the transmitter.

3.6 Clock Generator

Commonly, a clock signal is provided to microcontrollers externally. Quartz crystals are frequently used as clock sources for their stability, low cost, and low phase noise. The Utah microcontroller, however, is designed to require minimum external components to support device miniaturization; therefore, an on-chip clock generator is desired. Because of the wide spectrum of applications considered, two clock sources are included. For applications that do not demand high computational power but require long runtime, such as the S-IVR or NO releaser, a low-frequency power-efficient clock generator is available on-chip. Additionally, for applications that require high sampling rates, complex signal processing, and high-rate RF transmission, a high frequency clock generator is included. The selection of clock signal

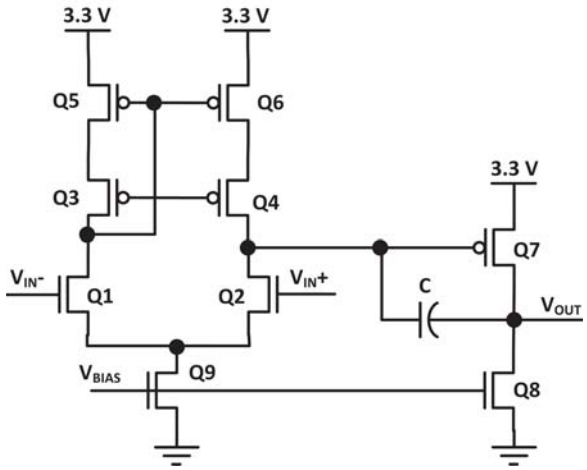


Fig. 3.24. Electrical schematic of the two-stage opamp used in the 1.2V regulator of Fig. 3.23.

Table 3.8: **Summary of simulated two-stage opamp performance.**

Parameter	Simulated value
Input offset	14.5 mV
Open loop gain	52.9 dB
Gain-bandwidth product	6 MHz
Phase margin (R_L = 30 kΩ, C_L = 1 pF)	70 °
Supply current	45 μA

source is controlled by the microcontroller's firmware. The clock generator's block diagram is depicted in Fig. 3.25 and the two oscillators are described in the following paragraphs.

3.6.1 Ring Oscillator

The low-frequency clock generator is based on a ring oscillator (RO) architecture. ROs are known to be very sensitive to temperature changes, process variations, and power supply fluctuations. As a result, they exhibit poor frequency predictability and stability, which leads to inferior phase noise performance. On the other hand, ROs are simple to implement and operate at low power dissipation levels, making them attractive for applications such as the Utah microcontroller, where power performance is critical. The fact that most biomedical applications operate at relatively stable temperatures (animal body) gives designers an opportunity to use ROs as clock sources without the need for frequency trimming or calibration. Additionally, careful design choices allow the troublesome characteristics of ROs to be minimized.

There are several design variables that need to be taken into account when an RO is considered as a clock source. First, the optimal number of stages N needs to be determined. It has been shown that the *impulse sensitivity function* (ISF), which determines the sensitivity of the oscillator to an impulse input, can be approximated as $4/N^{1.5}$ for a single-ended RO [40]. This dependency suggests that the phase noise of an RO can

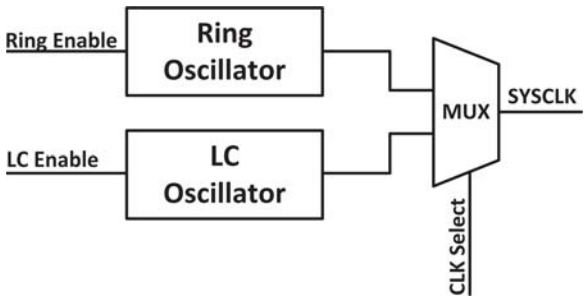


Fig. 3.25. **Internal clock generator configuration.**

be reduced by increasing the number of stages. Conversely, however, a higher number of stages also increases the number of noise sources. An involved analysis, presented in [40], concluded that for a single-ended RO, the phase noise and jitter in $1/f^2$ region are not strong functions of the number of stages if rising and falling edge symmetry is satisfied. Consequently, to minimize the ROs power consumption, which increases with increasing number of stages, a three-stage architecture was selected for the Utah microcontroller.

In order to minimize the phase noise of the RO, equal slope of the rising and falling edges is desired [40]. Custom-designed inverters were therefore used in the RO. The falling and rising edges were equalized in simulations by adjusting the W/L transistor ratios. Furthermore, transistors with increased L (120 nm) were used to improve matching and reliability at the expense of somewhat increased leakage current. It is still expected that the symmetry will be slightly altered due to process variations but the consequent increase in the phase noise will not affect the microcontroller.

A common cause of suboptimal RO operation is an unbalanced loading of the individual stages. To mitigate this effect, dummy inverters were added after stage one and two to make the loads identical for all three stages. A schematic of the clock generator based on an RO is depicted in Fig. 3.26. A NAND gate is used as the first stage in place of an inverter to provide the ability to turn the oscillator *ON/OFF* with an external signal. The output of the three-stage oscillator is buffered with an inverter before it is fed into a predivider consisting of two D flip-flops. The oscillator's frequency is set by three capacitors and was designed to be 4 MHz. This frequency is divided by 4, resulting in the *Ring Out* signal being 1 MHz. Table 3.9 summarized the RO's parameters. The reason for generating a clock signal at a higher-than-desired frequency and dividing it by N = 4 is that the period jitter is reduced by the $\sqrt{N}$ [41]. Fig. 3.27 shows a captured output of the low-frequency clock generator and Fig. 3.28 shows the simulated and measured output frequency vs. temperature. The measured center frequency at 25° C was 17 % higher than simulated, which is within the expected margin of error.

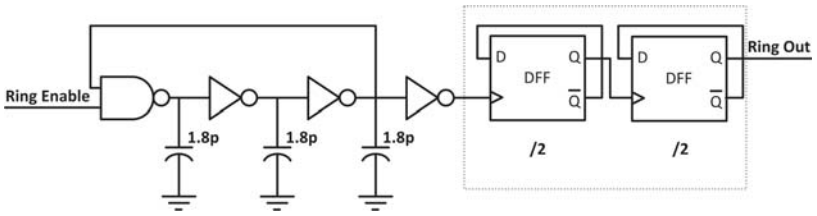


Fig. 3.26. Electrical schematic of ring oscillator.

Table 3.9: **Summary of ring oscillator's parameters.**

Parameter		Value
Number of stages	N	3
Internal oscillation frequency	f_{INT}	4 MHz
Output clock frequency	f_{OUT}	1 MHz
Required current	I_{RO}	16.6 μA

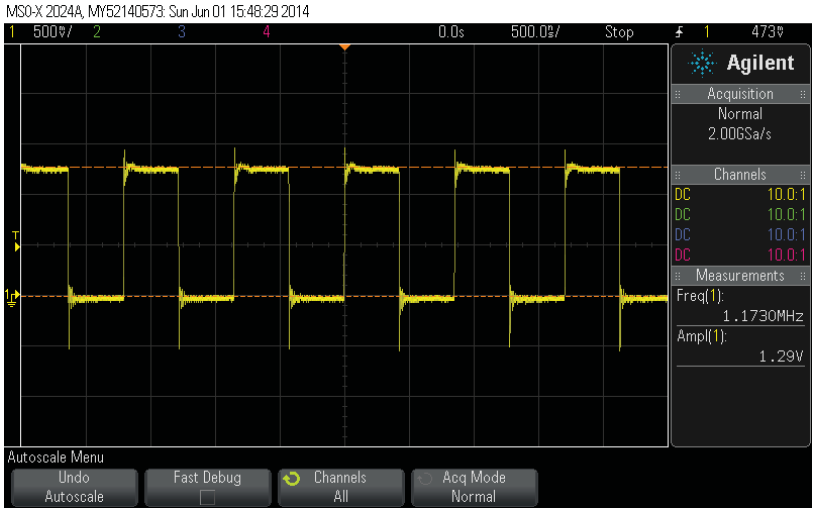


Fig. 3.27. **Measured output of the low-frequency clock generator.**

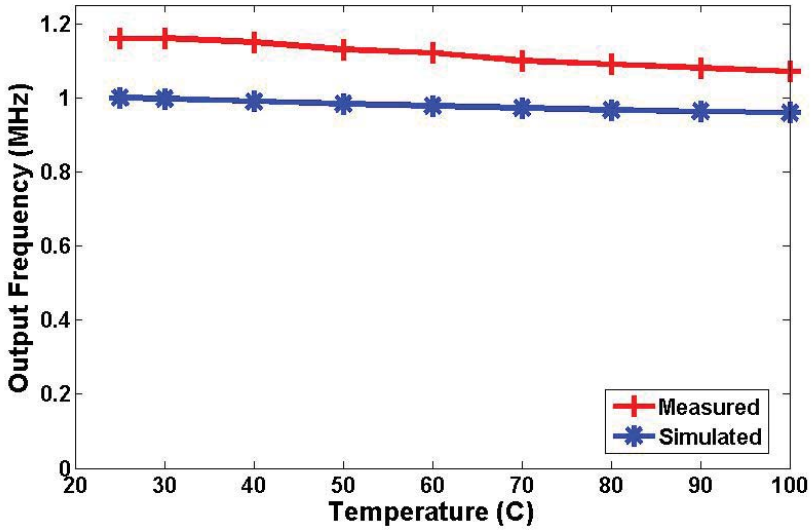


Fig. 3.28. **Low-frequency clock generator output frequency vs. temperature.**

3.6.2 LC Oscillator

For applications that demand high computational power, high sampling rates, or RF data transmission, the microcontroller must be operated at high clock frequencies. Although a ring oscillator could be designed to generate sufficiently high-frequency to drive such applications, its power consumption would increase extensively and its jitter would be unacceptable. A frequently used alternative for a high frequency clock source is an LC oscillator (LCO), which offers improved power and jitter performance over its high-frequency RO counterpart. Furthermore, LCOs are generally less susceptible to instabilities caused by temperature fluctuations, power supply noise, or process variations. They do, however, require a larger silicon area because of the inductor and capacitor that need to be fabricated on-chip.

There are numerous architectures of LCOs. For the Utah SoC, a double-switch (DS) cross-coupled LCO architecture was chosen for its favorable performance over single-switch (SS) architecture when both power consumption and phase noise are considered [42]. The LCO's electrical schematic is shown in Fig. 3.29. The LC tank is tuned to resonate at 1.6 GHz. Its differential output is fed into a comparator which outputs a square clock signal. The output signal is consequently buffered by an inverter and divided by 8 in a predivider, resulting in a 200 MHz clock signal. The clock signal can be further divided in the digital core by a factor of 2^n where n=1, 2, ..., 15.

The LCO design procedure was focused on two main objectives: (1) ensure that the oscillator reliably starts up when power is applied and (2) optimize its power consumption vs. phase noise performance.

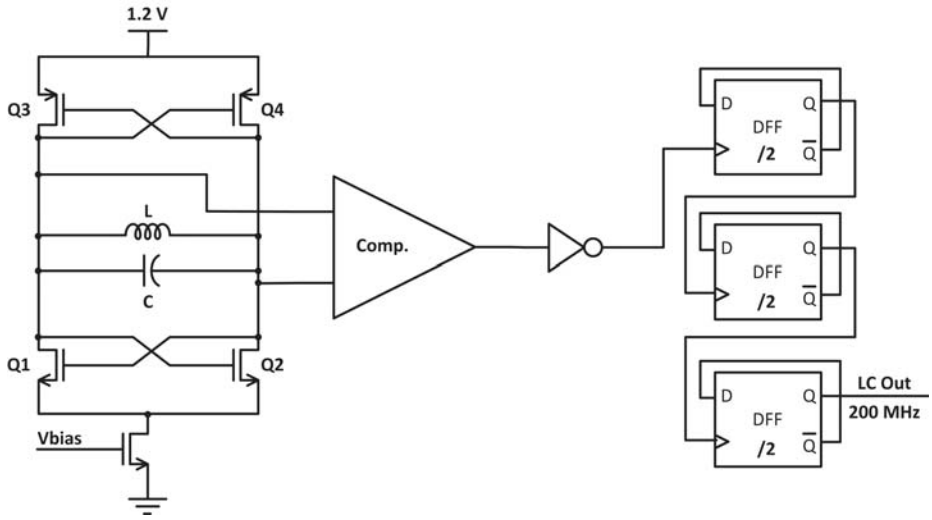


Fig. 3.29. Electrical schematic of LC oscillator.

Generally, the phase noise (PN) of an LCO improves with increasing bias current [40]. Increasing the bias current, however, increases the oscillator's power consumption, which is often undesirable. In most applications, the trade-off must be considered and a balance is reached based on the system's PN requirements. Typically, the most stringent PN requirement comes from the included communication interface. As explained in Chapter 4, the Utah microcontroller employs an ultra-wideband (UWB) signaling technique for data transmission. Since the UWB transmission is based on sending a sequence of short-duration high-frequency pulses, its PN requirements are more relaxed than in conventional narrow-band transmitters. Additionally, the PN in the UWB transmission can be compensated on the receiver's side by employing advanced de-modulating techniques.

It has been shown that the optimal balance between power consumption and PN of the DS architecture is achieved when the oscillator's output amplitude is equal to half of the transistors' threshold voltage V_{TH} [42]. The 65 nm CMOS process, used for this work, has $V_{THp} = 0.4$ V and $V_{THn} = 0.38$ V. For the purpose of the LCO's design optimization, output amplitude of 0.2 V was assumed.

The design equations for the DS LCO architecture in Fig. 3.29 are given by Equations 3.15 and 3.16.

$$V_O = \frac{V_{TH}}{2} = \frac{4}{\pi} \cdot I_{BIAS} \cdot \frac{R_P}{2} \tag{3.15}$$

$$A_l = g_m \cdot \frac{R_P}{2} \tag{3.16}$$

where V_O is the single-ended oscillation amplitude, R_P is the equivalent parallel tank resistance at resonance, I_{BIAS} is the oscillator bias current, A_l is the small signal loop gain, and g_m is the cross coupled transistors' transconductance.

To solve Equation 3.15 for I_{BIAS}, R_P must be determined first. Although R_P, which is the loaded tank equivalent parallel resistance, includes contributions from all components in the tank, it will be dominated by the parasitic resistance of the inductor. For an initial estimation of transistors' W/L ratios, only the inductor's parasitic resistance was considered to simplify the calculations. The final W/L ratios were tuned up by simulations. R_P was determined from the inductor's parameters which were obtained from an automated device synthesizer provided by the CMOS manufacturer's Process Design Kit (PDK). Once R_P was determined, I_{BIAS} was calculated from Equation 3.15. Equation 3.16 was solved for g_m assuming the loop gain $A_l = 3$ to guarantee the oscillator's start up. Equations 3.17 and 3.18 were then used to determine the W/L ratio for NMOS and PMOS devices, respectively.

$$\frac{W}{L_n} = \frac{(\frac{g_m}{2})^2}{I_{BIAS} \cdot \mu_n \cdot C_{OX}} \tag{3.17}$$

$$\frac{W}{L_p} = \frac{(\frac{g_m}{2})^2}{I_{BIAS} \cdot \mu_p \cdot C_{OX}} \tag{3.18}$$

Capacitor C was calculated to resonate the inductor L at 1.6 GHz. The oscillator's design parameters are summarized in Table 3.10. Fig. 3.30 shows the high-frequency clock generator's simulated and measured output frequency vs. temperature. The measured data indicate that the oscillator is stable over temperature and its center frequency at 25° C is within 1.5 % from the designed value.

3.7 Converters

Digital-to-analog (DAC) and analog-to-digital (ADC) converters are critical to any microsystem that employs sensors and actuators. Converters are mixed-signal circuits

Table 3.10: **Summary of LC oscillator's parameters.**

Parameter		Value
$Q_1 = Q_2$	W/L	37 μm / 65 nm
$Q_3 = Q_4$	W/L	82 μm / 65 nm
Inductor	L	4.47 nH
Capacitor	C	1.98 pF
Internal oscillation frequency	f_{INT}	1.6 GHz
Output clock frequency	f_{OUT}	200 MHz
Required current	I_{LC}	1.2 mA

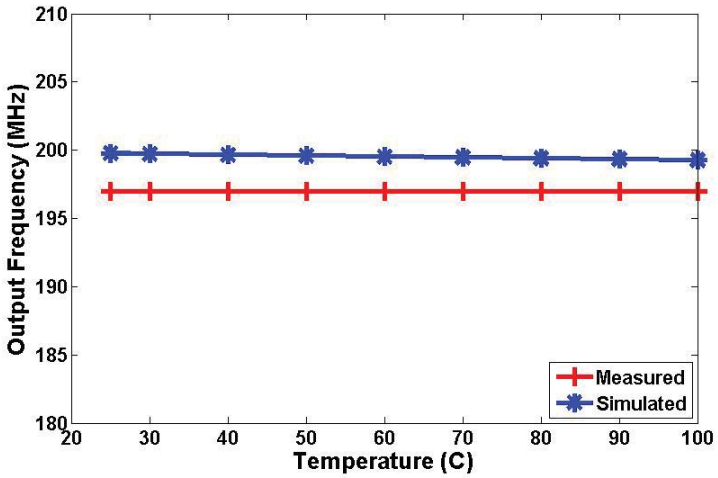


Fig. 3.30. **High-frequency clock generator output frequency vs. temperature.**

that facilitate an interface between the discrete binary world of microcontrollers and the continuous-signal world of nature. A respectable amount of research effort over the last several decades has been focused on improving converters' performance. They can be found in every aspect of our lives, ranging from toothbrushes to complex communications systems carrying data at rates in the Gbps range. There are presently many architectures covering almost any application imaginable.

Both DAC and ADC were designed for the Utah microsystem. The architecture selection, design procedure, simulations, and testing were completed by a fellow member of our group, and therefore will be covered only briefly in this dissertation for completeness [2].

3.7.1 Analog-to-Digital Converter

The area of analog-to-digital signal conversion has been studied for several decades. There are many mature ADC architectures today, each with a distinct set of advantages and drawbacks. The following paragraphs briefly discuss the most common ADC architectures to evaluate their suitability for the Utah microcontroller.

Flash converters consist of a large bank of comparators, each made of low-gain, wide-band pre-amplifiers followed by a latch. The comparators' trip points need to be accurate, while gain linearity is not as critical. Flash converters are usually very fast (with sampling rates as high as several Gsps), but they consume significant power [43–45]. Moreover, their resolution is typically only up to 8 bits because the number of comparators increases by a factor of two for every extra bit of resolution. Flash ADCs are also prone to sporadic and erratic outputs known as "sparkle codes." Sparkle codes are predominantly caused by thermometer-code bubbles and metastability in the 2N-1 comparators.

Successive approximation register (SAR) converters generate bits sequentially by a single high-accuracy high-speed comparator. The sequential nature of the SAR ADC limits the sampling rate to no more than a few Msps and often slower for high-resolution (14- or 16-bit) ADCs [46–48]. Additionally, the comparator in the ADC must be as accurate as the ADC itself, often resulting in the need for calibration. The ADC's clock speed is high and is equivalent to approximately the number of bits multiplied by the sampling rate.

Integrating ADCs, also called dual- or multislope converters, employ a conversion technique that is popular for its relatively easy implementation. The dual-slope converter consists of an analog integrator, comparator, and a counter. A conversion cycle is performed by first integrating the input voltage for a fixed period of time. At the end of this interval, the

[2] Refer to Bennion Redd's dissertation for more details.

internal counter is reset to zero and a reference voltage of an opposite polarity is applied to the integrator's input. The integrator starts "deintegrating" its output, during which period the internal counter increments its state with each clock period. When the integrator's output reaches zero, the counter is stopped, the integrator is reset, and the conversion cycle ends. At the end of the conversion cycle, the counter's state is proportional to the input voltage. Although dual-slope ADCs are simple to implement, they are also one of the slowest architectures, which restricts their applicability. Other factors that limit this architecture's resolution are the dielectric absorption of the integrating capacitor, the accuracy of the comparator used as the null detector, and the voltage rails of the operational amplifier.

Another popular ADC type is the pipelined architecture for sampling rates from a few Msps up to several hundreds of Msps [49–51]. Resolution ranges from 8-bits up to 16-bits at lower sampling rates. The main benefit of the pipelined architecture is that the area and power dissipation grow almost linearly with the number of bits. The drawback of this architecture, on the other hand, is its sensitivity to the internal opamp's gain and offset errors, capacitor matching, switch charge injection mismatch, and sensitivity to offset in the internal comparator. These problems are commonly addressed by digital calibration schemes that increase the complexity of the design.

Sigma-delta ADCs are frequently used in digital audio application for their limited bandwidth of several hundreds of ksps. Some recent high-order sigma-delta ADCs achieve sampling rates of a few Msps [52–54]. Despite their low sampling frequency, sigma-delta ADCs are popular for their accuracy. Even 16 - 18-bit resolution ADCs require no special trimming or calibration. They also require no steep roll-off anti-aliasing filters at the analog inputs because their sampling rates are much higher that the effective bandwidth. Sigma-delta ADCs trade speed for resolution. Since the Utah microcontroller is intended to process biomedical and chemical signals, which typically have low bandwidth, a sigma-delta ADC was selected to suppress the need for complex calibration schemes.

A second order sigma-delta implementation, depicted in Fig. 3.31, was selected to achieve the desired resolution. In order to implement the integrators and quantizer, a low-power rail-to-rail operational amplifier was designed and is briefly described in Section 3.9. The sigma-delta modulator achieves a peak of 81.1 dB SNR in simulations, equivalent to more than 13 bits of resolution, while consuming an average of 222 μW at 1.8 V. The decimation filter for the modulator was synthesized as a part of the digital core. Fig. 3.32 captures the simulation results.

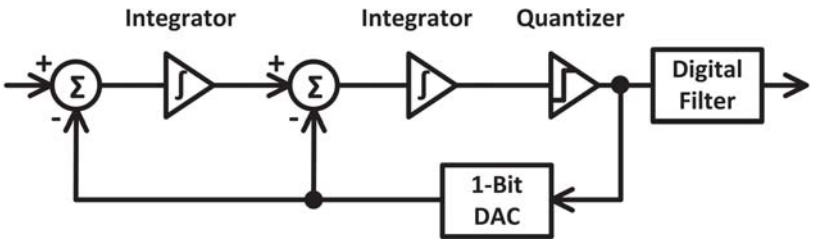


Fig. 3.31. **Block diagram of second order sigma-delta converter.**

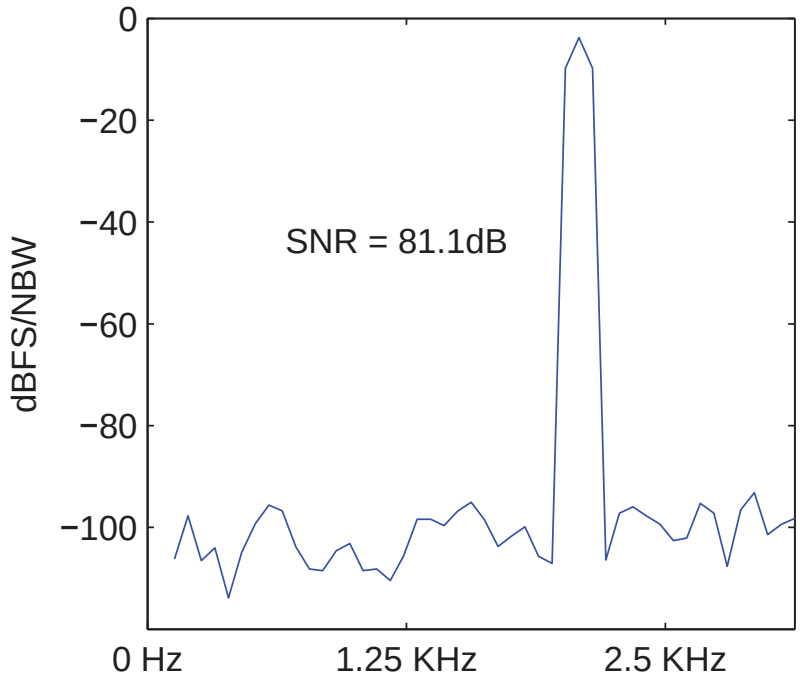


Fig. 3.32. **Sigma-delta ADC - simulated SNR after decimation filter.**

3.7.2 Digital-to-Analog Converter

Three parallel architectures were considered for the Utah microcontroller's DAC. Parallel DACs are characterized by their scaling methods and are classified as current scaling DACs, voltage scaling DACs, and charge scaling DACs. Following is a short discussion of each technique.

Current scaling DACs typically convert a reference voltage to a set of 2N binary-weighted currents. An array of switches, controlled by the digital input, selects the appropriate combination of current sources that contribute to the output current. The output current, which is a sum of the individual weighted currents, is applied to an opamp in the inverting configuration to generate the analog output voltage. This architecture is fast and insensitive to switch parasitics, but its power efficiency is limited due to the high number of current

sources. Furthermore, due to the large device size spread (weighted current sources), this architecture cannot guarantee monotonicity.

Alternatively, voltage scaling DACs convert the reference voltage V_{REF} to a set of scaled voltages that are combined into a single output voltage by the digital input combination. These voltages are commonly generated by at least 2N resistors connected in series and dividing the reference voltage. An advantage of this architecture is that it guarantees monotonicity, but the silicon area required by the resistors is large due to the higher number of bits. Large resistors results in an increased silicon area, causing component matching to become an issue. The conversion speed of this architecture is limited by the parasitic capacitances on the internal nodes.

A charge scaling DAC is a simple architecture based on division of charge applied to a capacitive array. Its advantage is that it is compatible with switched capacitor circuits and can be effectively implemented in a digital manner. Its capacitive nature leads to low power consumption because no DC current other than leakage is dissipated in the capacitor array. Moreover, capacitor matching in CMOS processes is typically significantly better than resistor matching, resulting in improved accuracy over voltage scaling DACs. The drawback of this architecture is, however, an increased silicon area required by the capacitive array, inviting problems with device matching across the area and causing nonmonotonicity. However, the low power consumption, low-complexity of implementation, and good accuracy were attractive for the Utah SoC and as a result, this architecture was selected for the microcontroller.

Fig. 3.33 depicts the implemented DAC's electrical schematic. Requirements of the DAC implementation include 10-bit resolution, low-power consumption, and capability to drive currents at the order of 10s of milliamps to drive chemical reactions such as the NO releasing application. The DAC consumes an average power of 124 μW at 1.8 V. The opamp, which acts as the unity-gain buffer, has a constant-g_m (within 15%) and features rail-to-rail input and output swings. Although it consumes only 120 μW, its class AB output stage enables it to drive current orders of magnitude higher than its own quiescent current.

To ensure that the output remains constant while the input capacitors are discharged in preparation for a new digital input, the DAC output charges a holding capacitor to hold the previous value. Prior to the input capacitors being discharged, the holding capacitor is switched from the output of the unity gain buffer to the input. Transient voltages during the transition do not appear at the output because the bandwidth of the low-power opamp is very low compared to the speed of the switching transistors.

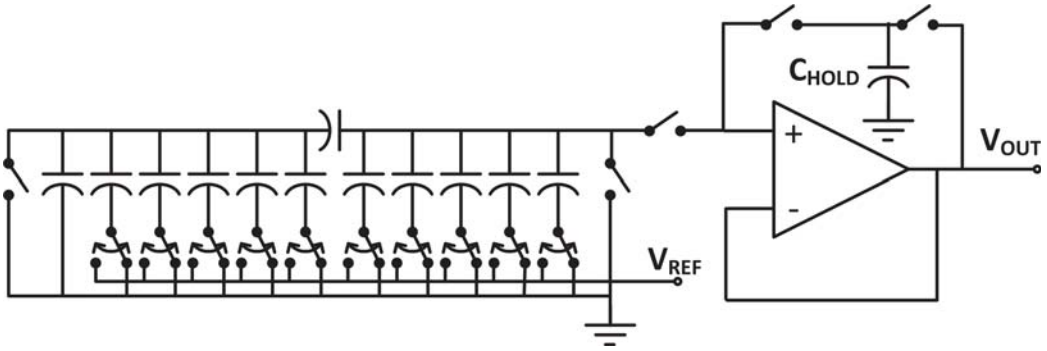


Fig. 3.33. Electrical schematic of charge scaling DAC.

3.8 Programmable Sensor Interface

The implemented ADCs and DACs allow the system to directly read or drive voltages and thus monitor or drive chemical reactions. Many biomedical and chemical applications, however, employ sensors that need to be driven by a current rather than voltage. The required excitation current might be DC or AC, and in most cases, its magnitude needs to be well controlled. Our system includes two programmable current interfaces that offer full control over the output current. Two modes of sensor excitation are recognized.

3.8.1 Direct Current Mode (Resistive Sensors)

One group of sensors our programmable interface can drive are resistive sensors such as pressure and temperature. These sensors are typically driven with a known DC current and the developed voltage is measured with an ADC. The DAC in conjunction with a resistor and opamp form a programmable current source, as shown in Fig. 3.34a. The output voltage from the DAC is connected to a known resistor R. The operational amplifier adjusts its output voltage to achieve 0.9 V at node A. Since there is no current into the opamp's input, all of the current $(V_{DAC} - V_{REF})/R$ is driven through the sensor.

3.8.2 Alternating Current Mode (Conductivity Sensors)

Conductivity of various body fluids is a commonly measured property. It is typically used in conjunction with other measured properties such as temperature and gives researchers information about chemical processes in the body or indicates the presence of a specific fluid in the sensor's surrounding environment. Both 2- and 4-electrode conductivity sensors can be accommodated in our system. A 2-electrode sensor would be driven in the same manner as a resistive sensor, with the exception that an alternating current would be used to prevent electrode polarization. This can be achieved by periodically varying the DAC voltage around 0.9 V. For greater accuracy, a 4-electrode conductivity sensor is usually

preferred over a 2-electrode system because it is more immune to electrode polarization. In a 4-electrode sensor, two electrodes are driven by a known AC current and a voltage drop across the two remaining electrodes is measured as shown in Fig. 3.34b. Two ADC channels are used to measure the voltage V_{OUT}.

3.9 Rail-to-Rail Operational Amplifier

As with the data converters, the operational amplifier was designed by another member of our group and will be described here only briefly. Since the amplifier was used repeatedly in various analog blocks in the microcontroller, it is presented in this work for completeness.

Because advanced CMOS technologies, such as the 65 nm CMOS process used for this project, operate at low nominal voltage levels (1.2 V), it is challenging to design an operational amplifier with high dynamic range. To achieve this goal, rail-to-rail (RR) input and output stages were required. Further increase of the dynamic range was achieved by designing the amplifier using high-voltage I/O devices, available in the CMOS process. The amplifier and all peripheral blocks were designed to operate at 1.8 V power supply so that actuating and observing a wide range of redox chemical reactions could be done without additional external amplifiers. A 3.3 V version of the same amplifier was also designed for 3.3 V operation and was used in the bandgap. Table 3.11 summarizes the opamp's specifications defined for this project and the amplifier's schematic is depicted in Fig. 3.35. Q_1 - Q_4 form a dual RR differential pair. Q_5 - Q_{12} constitute a folded cascode load for the differential pair. Q_{13} - Q_{20} provide class AB output stage and finally Q_{25} - Q_{27} maintain constant G_m across the CMR by controlling the tail currents flowing through each differential pair. The AB output stage is capable of driving currents at the order of milliamps while the opamp's quiescent current stays low.

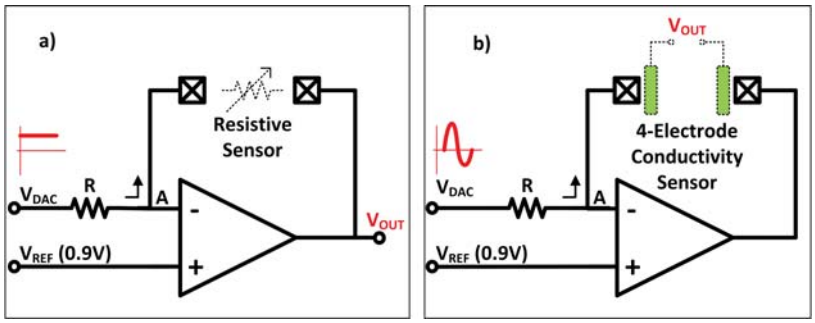


Fig. 3.34. Electrical schematic of programmable sensor interface: a) direct current mode and b) alternating current mode.

Table 3.11: **Summary of rail-to-rail operational amplifier's parameters (1.8 V).**

Parameter	Simulated value
Input offset	107 μV
Open loop gain	81 dB
Gain-bandwidth product	4.9 MHz
Phase margin (R_L = 30 kΩ, C_L = 1 pF)	76 °
Supply current	45 μA

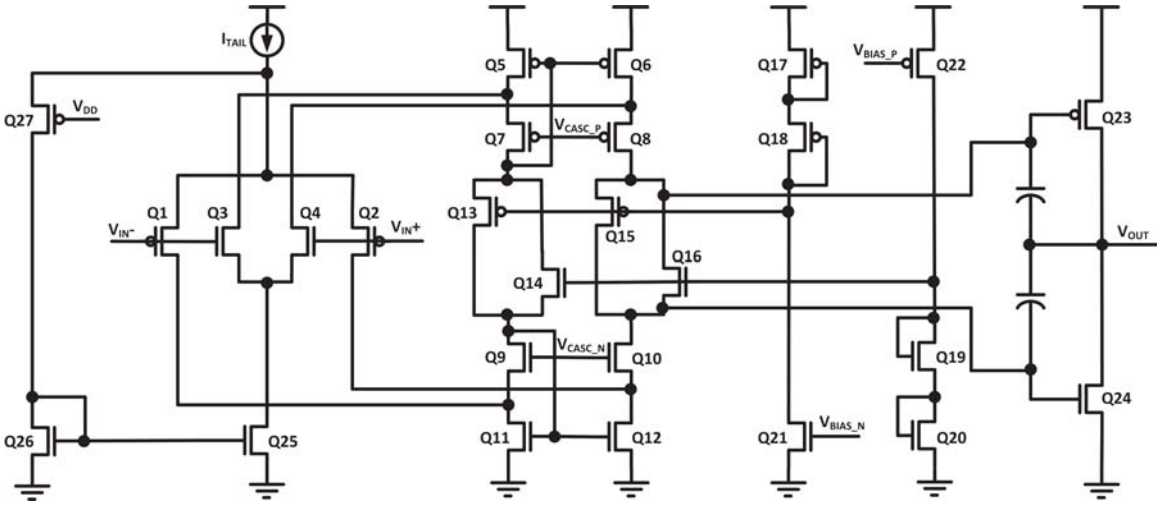


Fig. 3.35. **Electrical schematic of rail-to-rail operational amplifier.**

3.10 Wireless Telemetry

A large portion of this project is to develop a low-power wireless transmitter that can be integrated with the Utah microcontroller and is suitable for a variety of biomedical applications. Wireless data transmission capability is crucial for implanted microsystems and for experiments on untethered animals. There are many tradeoffs and challenges to select and design a wireless technology that meets desired criteria. To fully describe the work that has been done on the communication link, Chapters 4 and 5 are dedicated to this subject.

3.11 Chip Layout

The proposed chip was designed in a 65 nm CMOS process offered by Global Foundries. Its fabrication would not be possible without the Mosis Educational Program. We would like to extend our appreciation to Mosis and all of its employees for support on this project. We would also like to thank Synopsys for providing digital IP.

The digital core of the Utah microcontroller consisting of the three-stage pipeline, memory controller, SRAM, USART, and clock divider were synthesized and automatically placed and routed by EDA tools. The remaining mixed-signal blocks were manually laid out. Advanced layout techniques such as common centroid layout, increased transistor lengths, and dummy transistors were used to improve matching. Guard rings around critical transistors and around critical blocks were used to reduce substrate noise and digital lines were placed away from analog blocks to minimize crosstalk. The fabricated chip occupies a silicon area of 2 x 3 mm^2 and its layout is depicted in Fig. 3.36. It has 104 I/O pads and is packaged in the PGA 145 ceramic package. Please note that a large number of I/O pads were added on this research chip in order to observe critical internal nodes, therefore resulting in a layout that was not as dense as it could be.

To validate the Utah microcontroller's peripherals for sensing applications, a sensor die provided by e-SENS was wire-bonded to a circuit board and encapsulated in a UV-cured silicone as shown in Fig. 3.37. Consequently, a test board with the Utah SoC was mated with the sensor die. Fig. 3.38 shows a test of the pH sensor during which the sensor die was submerged in solutions with known pH levels. Data from the chip's peripherals were observed on an oscilloscope and the functionality of the sensor interfaces was confirmed. The Appendix presents a detailed description of the e-SENS sensor die and performance of the pH, conductivity, and temperature sensors.

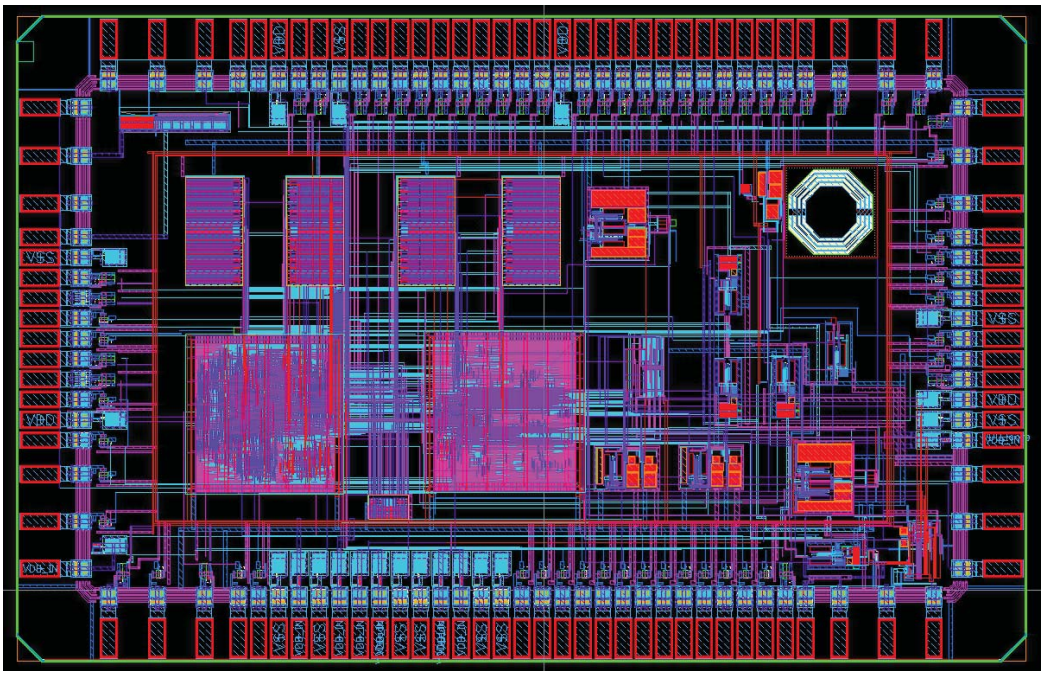


Fig. 3.36. Utah microcontroller's layout (2 x 3 mm^2).

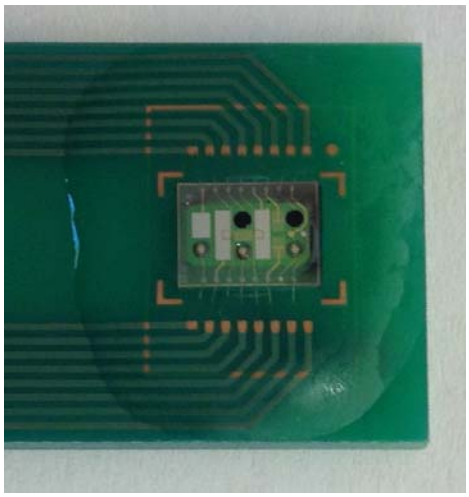


Fig. 3.37. Encapsulated e-SENS sensor die.

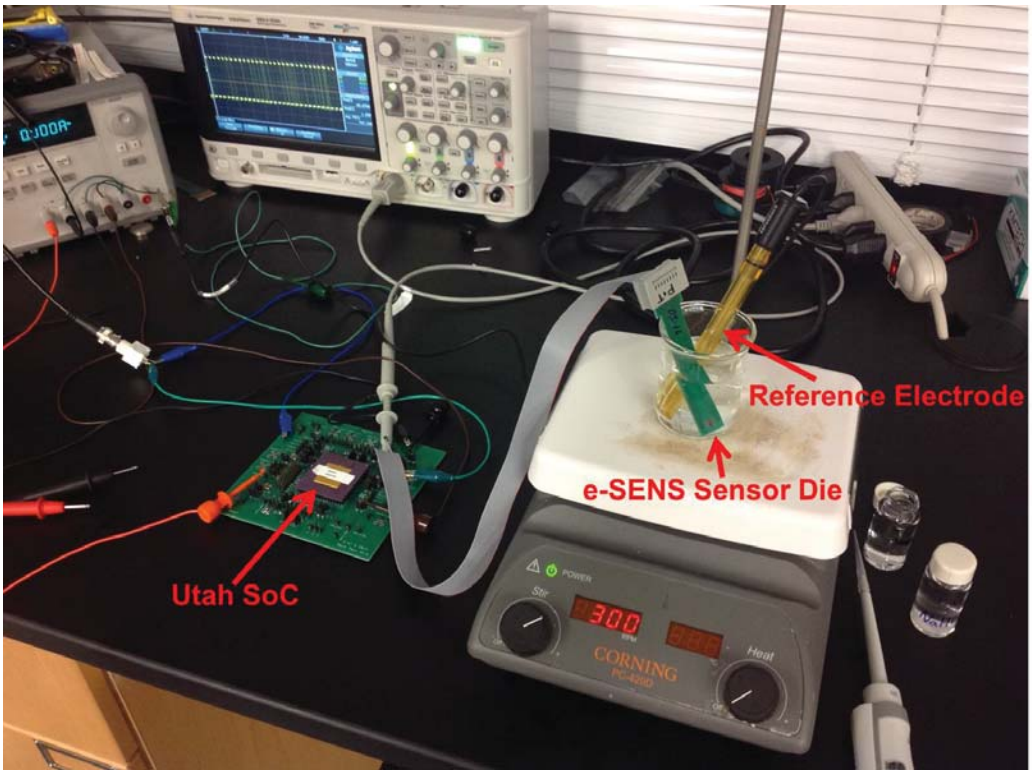


Fig. 3.38. pH sensor test.

3.12 Summary

A fully integrated microsystem was designed to advance the state-of-the-art of electronic microsystems for biomedical and chemical research. The system features a unique set of peripherals that make it particularly suitable for prototyping emerging technologies. It includes two internal clock sources, wireless powering, sleep counter, RF data transmitter, and circuits to process signals from a variety of electrochemical sensors. The SoC was designed to allow advanced miniaturization of devices for *in vivo* and *ex vivo* experiments on untethered animals, where commercially available chips are inadequate. The shortcomings of commercial chips usually occur in the form of lack of sensor interfaces, high power consumption, or the requirement of a high number of external components that increases the system's size and weight, making it unsuitable for implantation in animals.

The system was designed and fabricated in a 65 nm CMOS process which leads to high computational power, low power consumption, and small silicon area. The system includes 32 kB of SRAM memory for data processing and storage.

CHAPTER 4

WIRELESS ULTRA-WIDEBAND DATA TELEMETRY

Nearly all microsystems used in research on laboratory animals can benefit from a wireless communication link. Although experiments are frequently conducted on tethered animals with wired connections, reliability and cost are often problematic. Additionally, wires usually restrict the animal to a small area, and therefore increase the stress level of the animal and alter its natural behavior. Moreover, an increased risk of infections is a common problem of wired implanted microsystems.

Selecting the most appropriate wireless technology is a challenge for each application and requires considerations of many tradeoffs. This and future generations of the Utah microsystem are intended to serve in a wide spectrum of applications ranging from low data rate systems such as the NO releaser up to high bandwidth applications such as the neural recording system with a large number of channels. The system should therefore allow implementation of all these systems while achieving low power consumption. Our approach is to design a high-bandwidth wireless link for the most demanding applications that also allows duty-cycling to effectively scale the power consumption in low-rate applications. This chapter describes the wireless technology selection and circuit design procedures.

There are currently many mature wireless technologies conventionally used in consumer electronics. Most of them, however, are not suitable for biosensing research applications. This is usually because of prohibitive power consumption, large area or volume requirements, or insufficient data rates. Additionally, each biomedical application has a distinct set of requirements in terms of data rates, transmission distance, and power budget. As a result, the telemetry usually has to be custom-designed for each application. Not only does the system have to meet the application's needs, it also must be minimally invasive and comply with regulations established by the Federal Communications Commission (FCC). Several wireless technologies have been reported in biomedical applications that rely on different types of

electromagnetic signals to transmit information. Recently reported low-power transceivers employ narrow-band RF signals [55], infrared signals [56], or wideband RF signals [57]. Our objective is to evaluate these commonly used technologies and identify which one is the most appropriate for the Utah microsystem. Perhaps the most challenging applications from the data rate point of view are implants for neural recording. Understanding their telemetry requirements is critical to develop a microsystem that can cover that end of the application spectrum.

Recording neural activity directly from the human cerebral cortex has become a very active research area in recent years. Understanding better how the brain works holds the promise of developing treatments for several detrimental diseases such as Parkinson's and Alzheimer's [58]. Another application that is being investigated is the inhibition of epilepsy seizures [59]. Recent publications indicate that spoken words can be successfully decoded from neural data recorded from speech-related areas of the brain [60]. Real-time word recognition could eventually lead to real-time speech synthesis and help patients with severely impaired speech motor control.

To develop sufficient understanding of brain activity that will eventually lead to the successful realization of these advanced applications, scientists need to simultaneously observe a larger number of neurons with higher spatial resolution. Sensors offering such capability are being developed along with high-performance digital processors capable of processing large amounts of data [17]. It is realistic to expect that the number of recording channels will increase further in the future and new telemetry technologies will have to be developed to provide sufficient data rates while keeping power consumption low [61].

Meeting the requirements of modern implanted devices calls for large computational power to be fabricated with minimal silicon area. This has become possible as a result of aggressive device scaling of CMOS processes. The introduction of deep-submicron technologies, however, brings several issues that need to be carefully addressed to guarantee the high level of reliability expected from biomedical implants. With shrinking device sizes and decreasing supply voltages, circuits become much more susceptible to the effects of process variations, aging, and intra- and inter-die mismatch. Although a significant effort to mitigate these effects has been reported for digital circuits, considerably less work has been done to address the same issues in analog circuits. Biomedical implants, however, typically contain a large amount of analog circuitry to interface with a large number of sensory channels. Therefore, addressing these issues is critical.

4.1 Background and Motivation

4.1.1 Wireless Telemetry for Neural Recording

Although neural recording systems typically require bidirectional communication, the majority of the data is transferred from the implant to the external equipment (backward telemetry). Forward telemetry is usually required only to send control commands to the implant or to load system variables, and requires very low data rates (in the range of several bits per second); such speeds can be easily realized through an inductive link that supplies power to the implant. Implementing a simple backward transmitter in the implanted electronics offers the advantage of a small, low-power transmitter at the expense of increased power consumption of the external receiver.

A system for decoding spoken words, which is the target application of this project, requires sophisticated and computationally intensive algorithms to process the neural data. These algorithms are currently at an early development stage and are not mature enough to be implemented in the implanted microsystem. Therefore, raw data from a large number of recording channels need to be transmitted from the brain of the test subject.

It is reasonable to assume that new generations of local-field-potential (LFP) sensors such as ECoG or microwires with improved spatial resolution and signal fidelity will be developed and the number of sensing channels will significantly increase. Assuming a sampling rate of 30 kilo-samples per second and an analog-to-digital converter (ADC) with 12-bit resolution, data rates approaching 200 Mbps will be required for 512 channels (30000 x 12 x 512). This project aims to develop an active, power-efficient telemetry system capable of serving such a high demand. The following sections evaluate the most common wireless technologies and propose circuit approaches suitable for applications with an increased number of channels.

4.1.1.1 Narrow-Band Transmitters

Narrow-band transmission, where data are encoded by modulating a single-tone sinusoidal carrier, is commonly deployed in existing wireless communication systems. Two standard technologies of this type, Bluetooth and Zigbee, were designed for low-power operation in portable equipment. Several neural recording systems have been reported using commercial chipsets with these technologies [62] [63] . The maximum data rates of Bluetooth and Zigbee, however, are limited to 24 Mbps and 2 Mbps, respectively, making them insufficient for LFP applications with large numbers of channels.

Other narrow-band systems have been developed specifically for biomedical applications and proven to be effective for transmissions in the kbps or low Mbps range. Fig. 4.1 shows

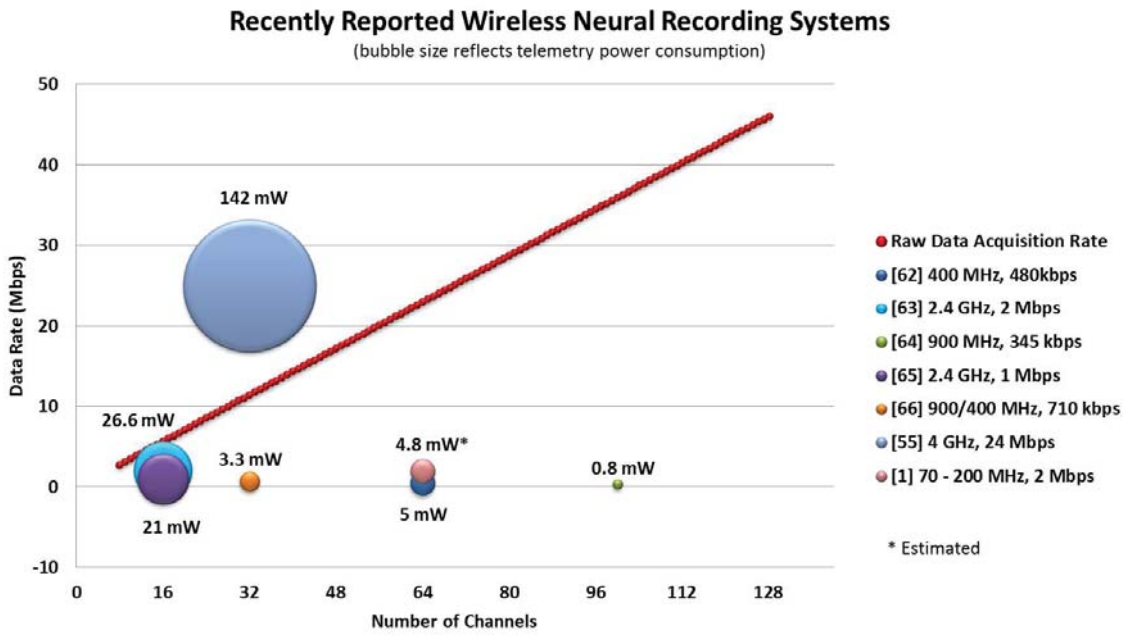


Fig. 4.1. Narrow-band wireless systems.

the required data rates per number of channels compared with the performance of recently reported narrow-band telemetry systems. Although higher data rates are possible, power consumption becomes prohibitive for biomedical applications because of the output power amplifiers required in such systems.

4.1.1.2 Infrared (IR) Transmitters

Perhaps the most significant benefit of using IR transmission instead of other RF methods is its resistance to interference such as from the power carrier or other wireless systems operating in the area. IR signaling for transcutaneous telemetry has been discussed since the 1980s [67], and has recently been considered for high-rate data transmission [68]. Most recent reports indicate that IR transmission is a viable option for biomedical implants reaching data rates in the low Mbps range at power consumption levels below 10 mW. The primary challenge of implementing IR transmission, however, is the need for a precise alignment accuracy of 1 - 2 mm, which is difficult to achieve with neural implants.

4.1.1.3 Human Body Communications

Communication techniques using conduction of the human or animal body itself have been investigated in recent years [69]. Recent publications report data rates of up to 10 Mbps with only 4.8 mW of power consumption [70]. However, there are several obstacles

that need to be resolved before body conduction methods become a viable alternative to traditional RF techniques [71]. One prevalent issue is that the potentials introduced by a body conduction data link will disrupt the neural activity potentials which are typically on the order of several μV. Another difficulty is that the previously reported work has modeled data transmission between two points inside the body, but neural implants require one point to be external to the body.

4.1.1.4 UWB

Communication systems using ultra-wideband signals were approved by the FCC for unlicensed use in 2004 [72]. The standard defines a UWB signal as having an absolute bandwidth of at least 500 MHz and a maximum radiated power density of -41.3 dBm/MHz in the frequency range from 3.1 - 10.6 GHz. These specifications create opportunities for high-rate data transmission at very low levels of power consumption.

There are two main types of UWB transmitters: impulse-based (I-UWB) and multi-carrier UWB (MC-UWB). MC-UWB transmitters simultaneously modulate several narrow-band carriers to generate a UWB signal, offering robust data transmission at the cost of higher power consumption. The I-UWB approach, on the other hand, encodes data into a series of short RF pulses that can be generated with very power-efficient circuitry. I-UWB transmitters have been recently reported as reaching data rates of several 10s of Mbps with power consumption of less than 5 mW [57]. Moreover, since the FCC only defines the spectral mask of the transmitted signal rather than its shape in the time domain, I-UWB transmitters can be implemented with power-efficient and fully digital circuits. This makes I-UWB a particularly attractive candidate for neural recording systems, where most data are only transmitted in a single direction: from the implant.

4.1.2 Related Work

A large amount of work has been reported on investigating various UWB pulse generation and shaping methods: (1) Gaussian pulse generators for very short UWB pulses have been reported, possibly enabling data rates to reach the Gbps range [73]. The drawback of these generators, however, is that they often use components such as step-recovery diodes that are incompatible with standard CMOS processes [74]. (2) On-chip LC oscillators have been reported to produce pulses with precise center frequency and bandwidth control enabling systems with multiple channels at the cost of increased silicon area and power consumption [75]. (3) Several fully digital generators based on ring oscillators or edge combiners have been reported for low-power operation [76]. These digital generators, however, typically

suffer poor center frequency stability and control due to high sensitivity to process and temperature variations. (4) Programmable generators forming precise UWB pulses through combination of triangular waveforms have been demonstrated [77]. Programmability and precise shaping, however, come at the cost of increased complexity, silicon area, and power consumption.

Several modulation schemes have been proposed and used in I-UWB systems. The most straightforward modulation is on-off keying (OOK). This modulation encodes a logical "1" with the presence of a UWB pulse and an "0" with the absence of a UWB pulse. Although this modulation is easy to implement and results in high power efficiency, it suffers high bit-error-rate (BER) and difficult noncoherent synchronization. Improved BER performance can be achieved with pulse-position-modulation (PPM) at the cost of higher power consumption. In PPM, each data bit is represented as a UWB pulse temporary positioned within a time period allocated for each bit [78]. Additionally, frequency modulated UWB (FM-UWB) represents data bits as short pulses with different center frequencies [79]. This method has been reported to yield the most power efficient UWB transceivers [80]. Drawbacks include increased silicon area and limited data rates. FM-UWB receivers, however, can be built with significantly reduced complexity as compared to OOK or PPM receivers, thus making them useful for applications where both transmitter and receiver need to be implemented on a single chip.

Fully functional I-UWB systems have been recently deployed in applications such as flying insect motion control [81] and a 128-channel neural recording system [57]. These successful applications clearly demonstrate the ability of UWB to fulfill the demands of high-performance applications such as BMIs.

The authors of [57] demonstrated that a 90 Mbps I-UWB transmitter can be implemented in a very simple manner. The transmitter consists of a simple digital circuit (only five digital gates), generating a square pulse, which is then passed through an LC filter formed by the parasitic inductance and capacitance of the packaging. Although this is an efficient low-power method, it suffers from several weaknesses. The energy delivered to the antenna and ultimately radiated through the air is low because the majority of the pulse energy is dissipated in the filter. Another problem with this method is its poor performance predictability, as most of the factors defining the center frequency, bandwidth and output power are heavily dependent on process and packaging variations. In the Utah project, a fully-digital I-UWB transmitter that offers better performance than the current state-of-the-art has been developed. The performance matrix includes achievable data rates,

power efficiency, and sensitivity to process variations.

4.1.3 Challenges of Implantable Electronics

In addition to fulfilling the need for increased data rates, wireless data links for implanted systems must be compact, power efficient, and highly reliable.

Reliability and manufacturability have become significant concerns as the implantable electronics industry migrates into deep-submicron technologies. System performance has grown to meet the requirements of new applications, as integration level has followed Moore's Law, but the reliability margin that existed in older technologies has been compromised in the dense, fine-geometry processes. As a result, new design techniques are investigated to mitigate the process variation effects in digital circuits [82–84]. This work implements several digital design techniques to achieve high reliability required for both non-life-supporting and life-supporting implants [85]. The I-UWB circuits are designed with thick-gate-oxide devices which have longer than minimum gate lengths (to reduce DIBL and V_T roll-off effects) and redundant VIAs.

4.2 Transmitter Architecture

In an I-UWB communication system, data are encoded in a sequence of short-duration pulses. The resulting signal has a wide bandwidth in the frequency domain, and thus permits a high data rate. As described above, several modulation schemes, each with a distinct set of trade-offs, are available for I-UWB systems. Phase modulation offers robust data transmission [86] but does not permit receivers based on energy detection. Frequency modulation architectures have been reported for power efficient transceiver design with the penalty of reduced data rates [80]. Pulse Position Modulation (PPM) encodes bits by temporaly positioning pulses within a symbol window. PPM modulation is widely used for I-UWB systems due to its low transmitter power dissipation, the possibility of fully digital implementation, and ability to use energy detectors for demodulation.

The benefits of PPM make it uniquely suited for implanted monitoring and recording systems, where data are transferred unidirectionally to an external receiver. In such applications, complexity and power consumption can be pushed from the implanted transmitter to the external receiver, which can be designed with fewer constraints. Noncoherent demodulation algorithms based on energy detection [87] or high-speed analog-to-digital converters are commonly employed in I-UWB receivers. This work proposes a UWB transmitter that achieves high power efficiency with minimal silicon area by eliminating the need for frequency calibration.

Fig. 4.2 depicts the overall architecture of the proposed transmitter designed to interface with a low-power microcontroller developed by the Center for Wireless Integrated Microsystems (WIMS) and optimized for neural recording systems [17]. Data are provided to the transmitter in a 16-bit parallel format and the data flow is controlled by a handshake protocol implemented with the *DATA Ready* and *TX Empty* signals. Parallel data are serialized and passed to the pulse position modulator. During the shifting period, the *TX Empty* signal is set to logic '0', indicating the transmitter is busy. In addition to serializing data and managing the data flow, the Data Control block also generates the clock signal, *PPM_clk*, for the modulator, which is a gated and delayed version of the master *CLK* signal and is only active during data transmission. Fig. 4.3 shows the timing for the internal signal waveforms when transmitting a 16-bit block of data.

Following the Data Control block is the pulse position modulator shown in Fig. 4.4. The logical value of the *PPM_data_in* signal controls a multiplexer selecting between the *PPM_clk* and its inverted version, *PPM_clk_bar*. The output signal, *PPM_out*, is a pulse that is positioned at either the positive edge or the negative edge of the clock cycle (symbol window).

The *PPM_out* signal is subsequently passed to a voltage-controlled delay cell pictured in Fig. 4.5. The delay cell generates an *Enable* pulse at each positive edge of the input signal. The duration of *Enable* defines the 'on' period of the pulse generator and thus the UWB signal bandwidth. The duration is designed to be 2 ns to meet the minimum required bandwidth. Two modes of operation, selectable by the *Pulse_ctrl* signal, are supported. The first mode generates a single 2 ns UWB pulse per each bit and is used for the fastest data

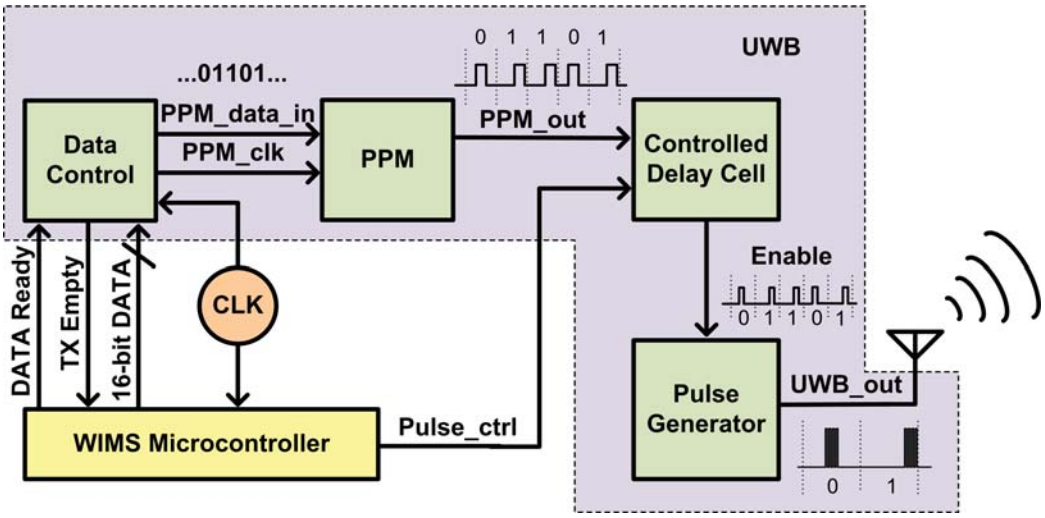


Fig. 4.2. UWB transmitter architecture.

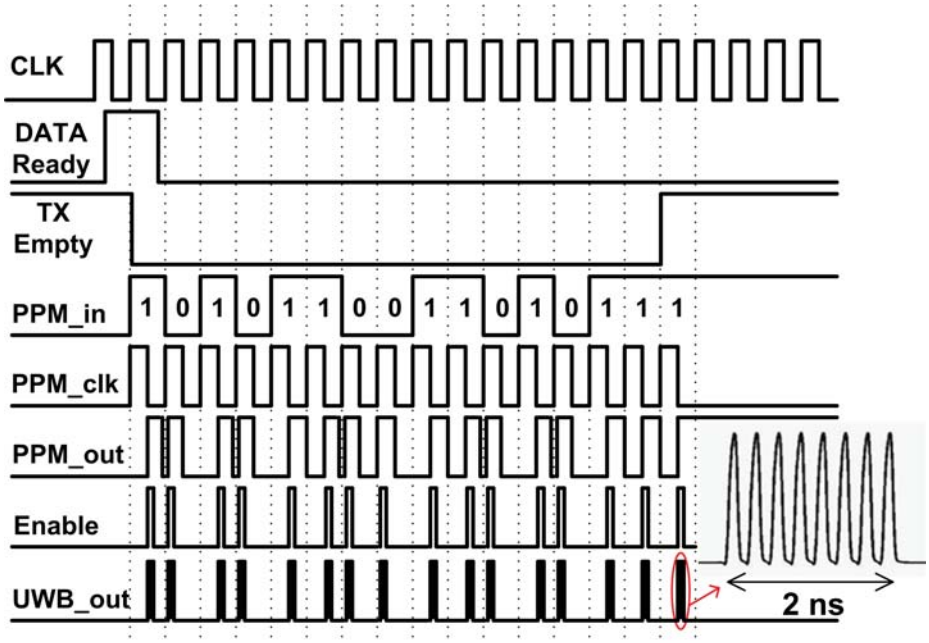


Fig. 4.3. UWB transmitter signals.

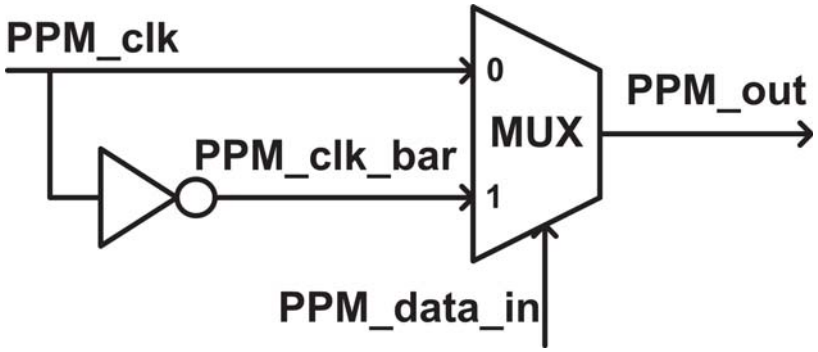


Fig. 4.4. Pulse position modulator schematic.

transmission. The second mode allows multiple UWB pulses to be transmitted per each data bit. This mode causes more electromagnetic energy to be radiated from the antenna, therefore making the signal detection and demodulation easier in the receiver.

The transmitter's overall power consumption is dominated by the pulse generator, which also largely affects the FCC compliance. Therefore, it is critical to design a power-efficient and reliable pulse generator for implantable applications.

4.2.1 Pulse Generator Considerations

The FCC definition of a UWB signal gives high flexibility in terms of the signal shape in the time-domain. Gaussian pulses are convenient for theoretical analysis of UWB systems

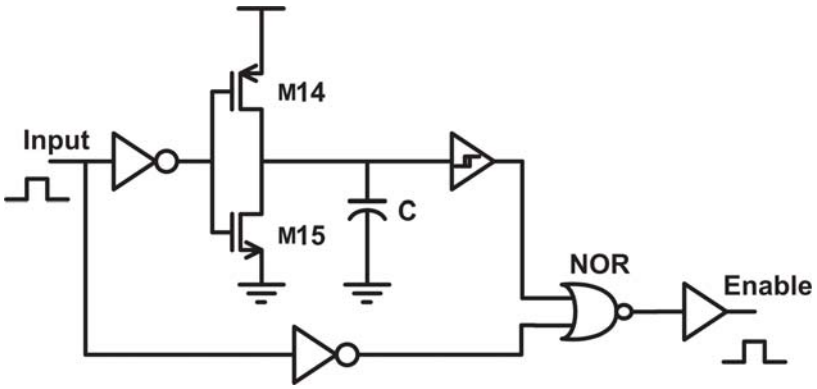


Fig. 4.5. Delay cell schematic.

and are frequently used in literature. Difficulties of generating Gaussian pulses in standard CMOS technology, however, resulted in a need for alternative solutions. A number of fully digital UWB pulse generation techniques have been investigated, including edge combiners, addition of triangular waveforms, and gated ring oscillators. Among these approaches, gated ring oscillators offer the highest power and silicon area efficiency [88], which makes them attractive for the Utah microsystem.

The proposed pulse generator is depicted in Fig. 4.6. The ring oscillator consists of a single-ended three-stage inverter connected in a positive feedback manner. The first stage of the ring oscillator is composed of a NAND gate for pulse width and oscillation frequency control. The transistors are sized to achieve the desired oscillation frequency of 4 GHz. A chain of output inverters with increasing device sizes is employed to drive a 50 Ω load representing antenna impedance. Fig. 4.7 presents the simulated output signal waveform in 2 ns time frame along with the corresponding RF power spectrum.

The oscillator generates 8 cycles of pulses in 2 ns, exhibiting amplitude of approximately 500 mV with a maximum RF power level of -31.8 dBm at 3.989 GHz. The overall transmitter energy per pulse, excluding the clock, is simulated to be 23.6 pJ/pulse for a pulse repetition

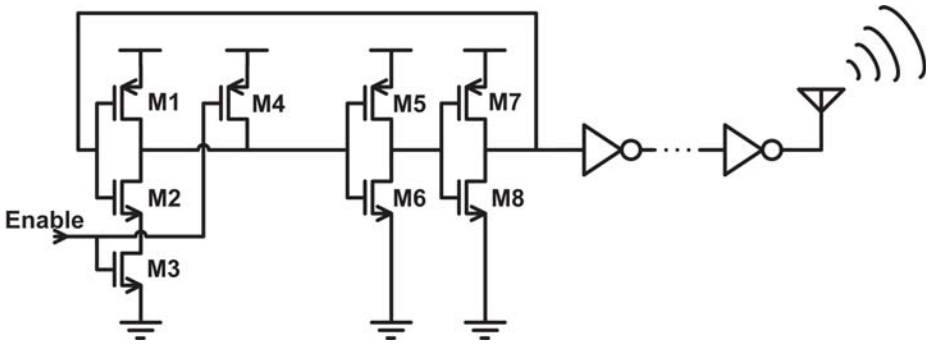


Fig. 4.6. UWB pulse generator schematic.

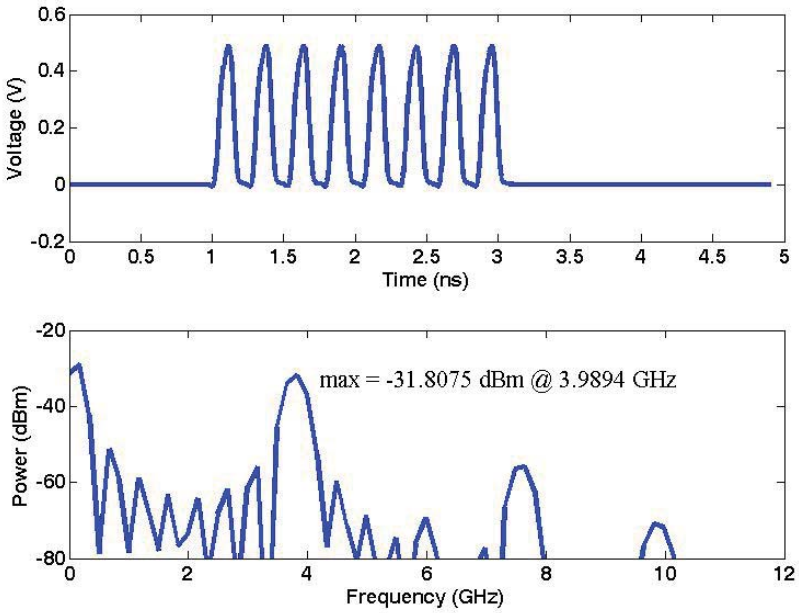


Fig. 4.7. Simulated gated ring oscillator output characteristics.

frequency of 100 MHz, closely matching the published performance prediction in [89].

4.2.2 Initial Pulse Generator Evaluation

The designed gated ring oscillator was fabricated in a 65 nm CMOS process. The gated ring oscillator with a voltage controlled delay cell occupied an area of approximately 30 μm x 30 μm. The fabricated chip was manually wire bonded to a PCB for electrical characterization as shown in Fig. 4.8. The power supply line and gated ring oscillator output are connected to a battery and measurement equipment with 50 Ω input impedance, correspondingly, by high-frequency coaxial cables. The initial test results are shown in Fig. 4.9, which exhibits a significant discrepancy with respect to the simulated characteristics.

In Fig. 4.9(a), the probed V_{DD} signal shows a large variation from 1V over time, and the

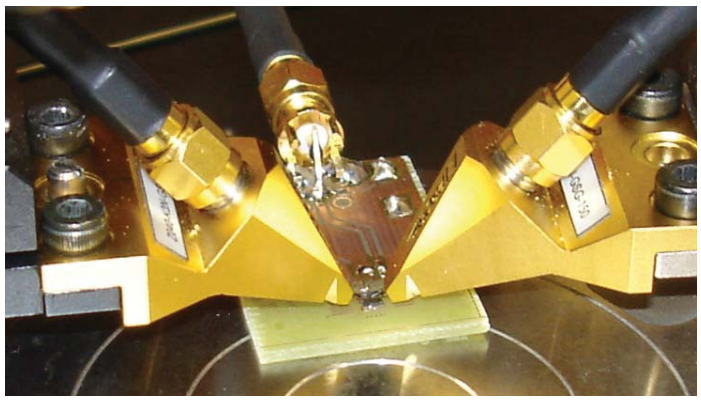
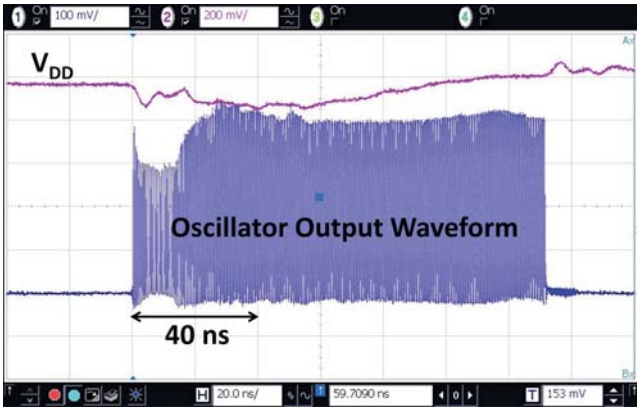
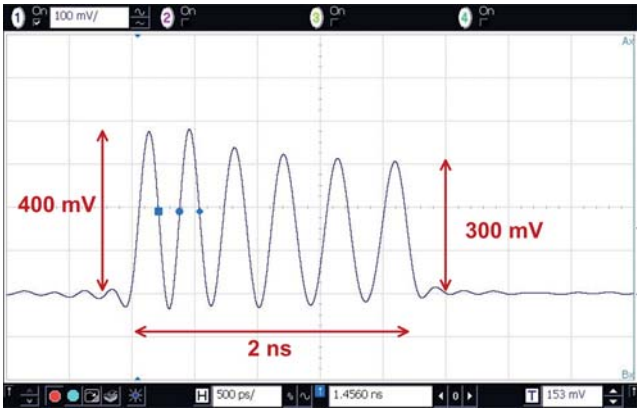


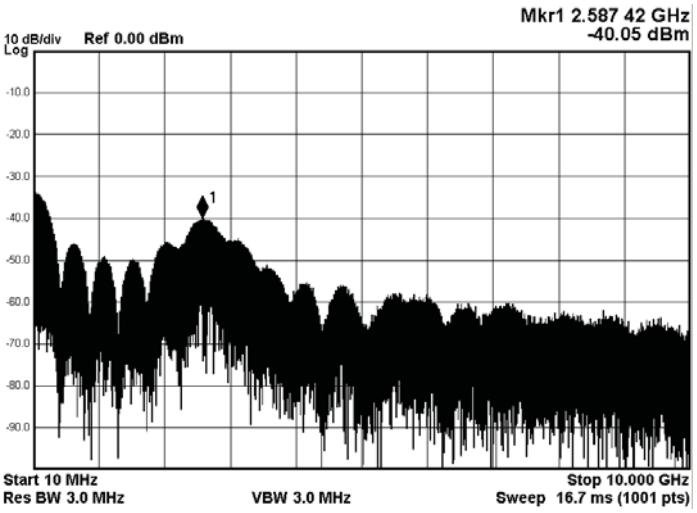
Fig. 4.8. Fabricated pulse generator in 65 nm CMOS.



(a)



(b)



(c)

Fig. 4.9. Gated ring oscillator initial measured results: (a) V_{DD} and oscillator output waveform, (b) oscillator output waveform in 2 ns, and (c) RF output power spectrum.

oscillator output signal amplitude exhibits an initial strong dip followed by a slow settling. An initial 2 ns of oscillator output waveform is presented in Fig. 4.9(b), where the oscillation amplitude degrades from 400 mV to 300 mV, and the individual peak width enlarges over time, thus resulting in an RF power spectrum shown in Fig. 4.9(c) with a center frequency of 2.5 GHz. These phenomena are caused by the initial V_{DD} amplitude degradation. The observed V_{DD} signal and oscillator output amplitude variation suggest a significant parasitic inductive effect associated with the power supply connection coupled with the RF switching current. A careful characterization of the test setup, including inductances of bondwire, PCB trace, and coaxial cable, was conducted. Fig. 4.10 illustrates an electrical model of the test setup including $L_{BONDWIRE}$, L_{PCB}, and L_{COAX} of approximately 10 nH, 20 nH, and 600 nH, respectively, where C_{P1} and C_{P2} are the on-board parasitic capacitances. Incorporating this model in simulation produces closely matched time-domain oscillator waveform compared to the measurement results. Fig. 4.11 shows a measured 2.5 ns pulse. A simulation incorporating the external parasitics is shown in Fig. 4.12, indicating a close match.

Additional experimental characterization along with simulation reveals that on-board

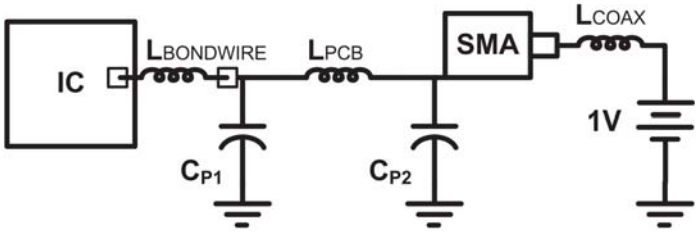


Fig. 4.10. Electrical model of test setup.

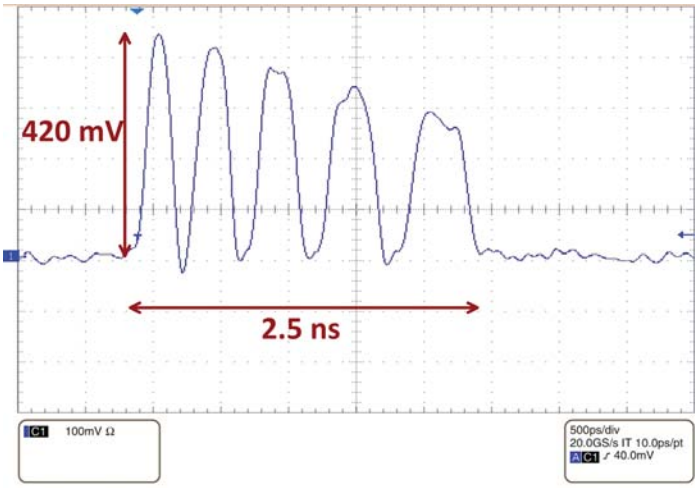


Fig. 4.11. Measured distorted 2.5 ns pulse.

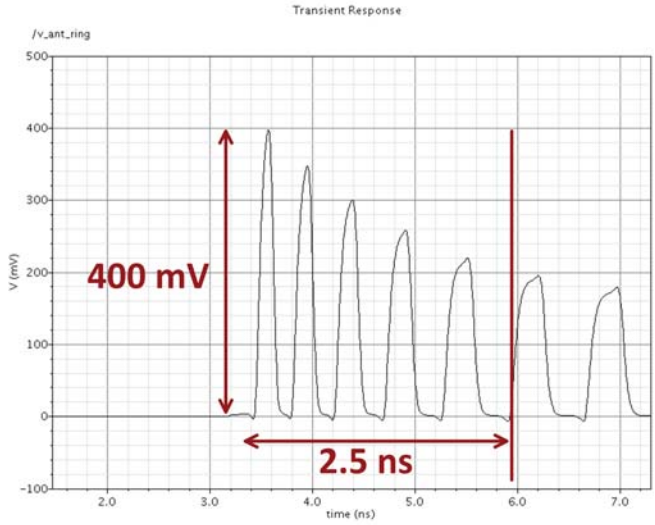


Fig. 4.12. Pulse simulation with incorporated external parasitics.

filtering capacitors, $C_{Filter-1}$ of 100 μF and $C_{Filter-2}$ of 32 μF, are sufficient to substantially eliminate the parasitic inductive effects. Fig. 4.13 presents the updated electrical model of the test setup, incorporating the filtering capacitors.

Fig. 4.14 presents the measured oscillator behavior, in which V_{DD} exhibits a minor variation around 1 V and the oscillator output amplitude settles to a value of approximately 430 mV within 3 ns as shown in Fig. 4.14(a). Note that an additional effort was made to reduce the bondwire and PCB trace inductances to approximately 2 nH and 4 nH, respectively, for this measurement. The reduced amplitude (less than designed 500 mV) is likely caused by the on-chip power supply interconnect resistance and other building blocks connected to the same power supply line in this prototype design. Therefore, a wide on-chip power supply interconnect trace is highly desirable to circumvent this effect. An initial 2 ns of oscillator output waveform is plotted in Fig. 4.14(b), where the oscillation amplitude and individual peak widths are nearly constant. The oscillation amplitude of approximately 370 mV (caused by the on-chip V_{DD} drop) results in a reduced peak power frequency of

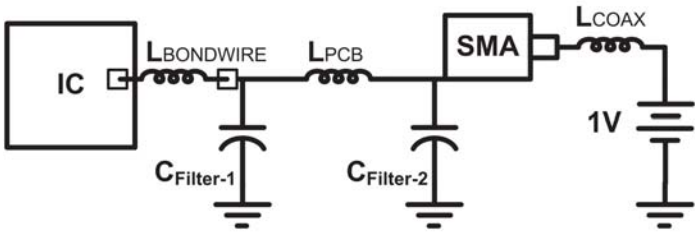


Fig. 4.13. Electrical model of test setup incorporating filtering capacitors.

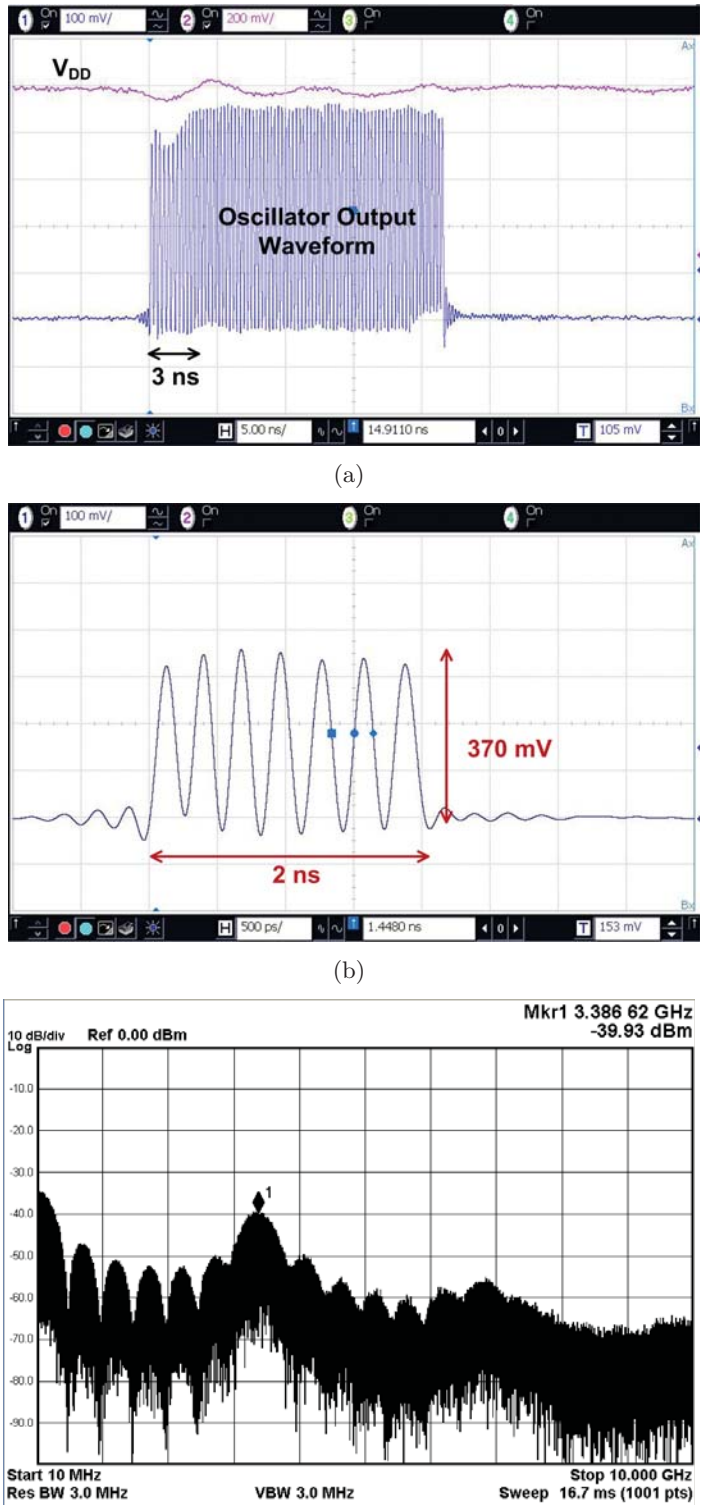


Fig. 4.14. Gated ring oscillator initial measured results with filtering capacitors: (a) V_{DD} and oscillator output waveform, (b) oscillator output waveform in 2 ns, and (c) RF output power spectrum.

3.386 GHz as shown in Fig. 4.14(c). An increased frequency is expected with a reduced on-chip power supply interconnect resistance.

In a practical application, an on-board voltage regulator is employed to provide the power supply voltage, thus eliminating the need for a coaxial cable with its L_{COAX} of 600 nH. Simulations of the corresponding model reveal that a gated oscillator output waveform can settle within 2 ns when the bond wire inductance, $L_{BONDWIRE}$, is reduced below 2 nH. This amount of inductance can be obtained by using short bond wires or flip chip bonding techniques. The oscillator generates 7 cycles of pulses in 2 ns exhibiting amplitude rising from 360 mV to 470 mV with a maximum RF power level of -38.8 dBm at 3.656 GHz. The simulated characteristics represent an improved match to the designed performance.

4.3 Transmitter Design Methodology

The initial evaluation of the UWB pulse generator based on a gated ring oscillator, described in section 4.2.2, confirmed that the architecture was suitable for a calibration-free UWB transmitter desired for the Utah microcontroller. The experiment revealed that external parasitic effects can significantly alter the pulse generator's performance, possibly resulting in FCC noncompliance. On the other hand, the experiment revealed that the external parasitics can be estimated and simulations can be used to achieve highly predictable performance [90]. In addition to the effects from external parasitics, ring oscillators exhibit frequency variations of up to 28% due to other effects such as process variations, neighborhood layout effects, and temperature variations [91].

Biomedical implants usually operate in an environment with predictable and sufficiently stable temperature, so the effect of varying temperature on the frequency of ring oscillators does not represent a significant problem. However, process and local voltage variations caused by the parasitics introduced by packaging and circuit board have substantial effects on the pulse generator's performance as described in section 4.2.2 and need to be considered to ensure FCC compliance. Typically, UWB transmitters calibrate their center frequency during operation using an on-chip feedback loop in order to meet the FCC requirements and allow multiple channel selection. This approach increases the transmitter's complexity, resulting in a larger silicon area and increased power consumption or extensive postfabrication testing and trimming [92]. In most biomedical applications, only a single communication channel is required, so calibration schemes can be effectively avoided through careful design and by taking advantage of the wide frequency band allocated for UWB. The UWB transmitter for the Utah microcontroller is designed employing a worst-case design procedure considering process variations and external parasitics that affect

reliability and performance.

4.3.1 Addressing Process Variations

A ring oscillator's center frequency is heavily dependent on transistor threshold voltages and, consequently, the drain current $I_{D_{SAT}}$. Deep-submicron technologies exhibit large V_T variations, resulting in poor control of output frequency. Analytically calculating gate delays for the highest device V_T specified by the foundry can identify the lowest center frequency for given transistor sizes, facilitating a design procedure that guarantees FCC compliance without postprocess or on-the-fly calibration.

The oscillator center frequency can be estimated by calculating the gate propagation delay for each stage in the ring by evaluating loading capacitance and equivalent resistance as described in [93]:

$$C_L = C_{SELF} + C_{WIRE} + C_{FANOUT} \tag{4.1}$$

$$R_{EQn,p} = \frac{3}{4}\frac{V_{DD}}{I_{D_{SAT}n,p}}\left(1 - \frac{7}{9}\lambda_{n,p}V_{DD}\right) \tag{4.2}$$

$$t_p = 0.69C_L\left(\frac{R_{EQn} + R_{EQp}}{2}\right) \tag{4.3}$$

where C_L, R_{EQ}, and t_p are the load capacitance, equivalent resistance, and a single transition propagation delay for each stage correspondingly. C_{SELF}, C_{WIRE}, and C_{FANOUT} are the output capacitance of the gate itself, wiring capacitance, and input capacitance of the consecutive stage.

The oscillator center frequency can then be calculated as:

$$f_c = \frac{1}{2t_{p1} + 2t_{p2} + 2t_{p3}} \tag{4.4}$$

corresponding to two transitions per clock cycle in each oscillator stage. Subscripts *1 - 3* denote the ring oscillator's stages.

In addition to the analytical calculations, simulations over process corners were performed to ensure the transmitter's FCC compliance without the need for calibration or postfabrication trimming.

4.3.2 Considerations for Packaging and Circuit Board Parasitics

The parasitic inductance introduced by packaging and circuit board traces can significantly impact the transmitter performance. These inductances and the rapidly switching currents cause variations in on-chip V_{DD} during the 2 ns UWB pulses, thereby changing the pulse generator center frequency and output amplitude. These inductive effects can be modeled and simulated with sufficient accuracy, as described in section 4.2.2. In this work, the packaging and circuit board parasitics have been modeled as shown in Fig. 4.15.

The values of $L_{BONDWIRE}$ and L_{PCB} were estimated to be 2 nH and 4 nH, respectively, and C_{filter} was determined through simulation to be at least 0.1 μF.

Transistors in the ring oscillator were sized such that the worst-case center frequency landed above 3.35 GHz.

4.4 UWB Receiver Front-End

Although there are currently several commercial UWB products, to the best of our knowledge, there is none that is capable of demodulating pulse-position-modulated (PPM) UWB signal at bit rates up to 200 Mbps. Most of the commercially available products, such as the PulsON P400 and Bosch D-tect150, are designed for radar applications. Perhaps the closest available commercial product that would be capable to demodulate the PPM signal is the PulsON P220 by Time Domain [94]. This receiver is capable of receiving the UWB signal, digitizing it, and analyzing it in both the time and frequency domains, but the highest pulse repetition frequency the device handles is approximately 10 MHz. Many UWB PPM receivers have been reported in academia [95–98], but none of these is currently available for purchase. In order to test the Utah UWB transmitter and verify that the signal can be received, recovered, and converted to baseband, a simple UWB receiver front-end

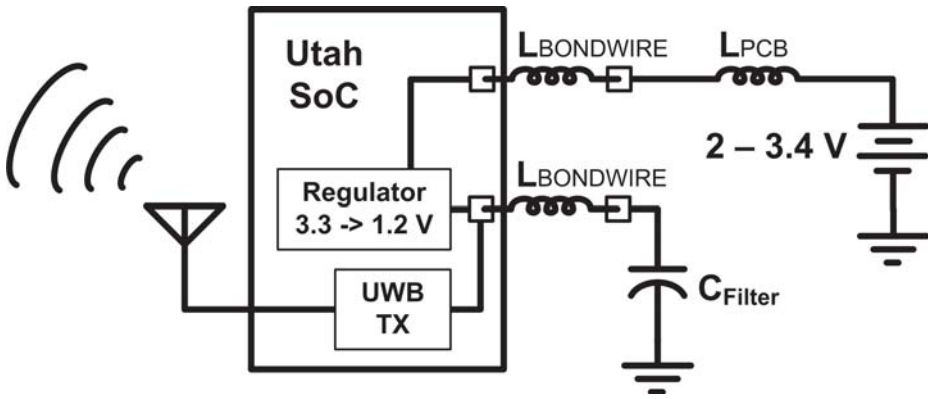


Fig. 4.15. Packaging and circuit board parasitic model.

was built from commercially available components. Baseband signal filtering, amplification, digitization, and demodulation are well-established tasks and can be done using standard techniques and parts. The front-end schematic is captured in Fig. 4.16. It consists of a UWB antenna, band-pass UWB filter, wideband low-noise amplifier (LNA), and an RF diode configured as an RF detector. The front-end prototype circuit board and list of components are shown in Fig. 4.17 and Table 4.1, respectively.

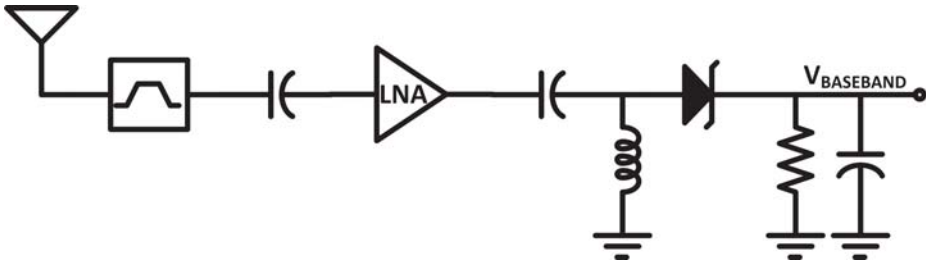


Fig. 4.16. UWB receiver front-end schematic.

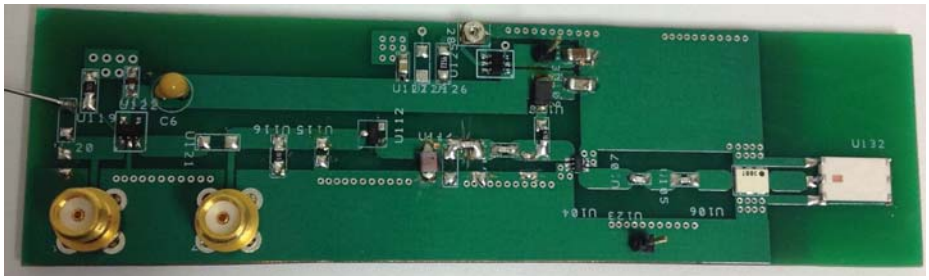


Fig. 4.17. UWB receiver front-end prototype.

Table 4.1: Summary of UWB front-end components

Component	Part Number
Antenna	Johanson Technology 3100AT51A7200
Filter	Johanson Technology 4000BP15U1800
LNA	Avago MGA-86563
Diode	Avago HSMS-2820

4.5 Measured Results

The proposed UWB transmitter was fabricated along with the Utah microcontroller in a 65 nm CMOS process. The transmitter (excluding I/O pads) occupies an area of 68 μm x 68 μm.

A 2 ns UWB pulse measured at 100 MHz pulse repetition frequency (PRF) is presented in Fig. 4.18. The maximum oscillation amplitude reaches approximately 400 mV and results in the RF power spectrum shown in Fig. 4.19 with a center frequency of 3.39 GHz and bandwidth >500 MHz. Among 10 tested die, the measured center frequency variation was 17%. All tested die exhibited a center frequency compliant with the FCC specifications.

Please note that Fig. 4.19 captures the UWB signal before it reaches the transmitting antenna. Its frequency spectrum contains several side-lobes exceeding the FCC mask. These spurs are attenuated by the band-pass property of the UWB transmitting antenna.

Full functionality of the transmitter has been confirmed, including pulse position modulation at PRFs up to 200 MHz [99]. The transmitter's overall power consumption was measured to be 3.1 mW and 4.4 mW at 100 MHz and 200 MHz PRF, respectively, corresponding to energy efficiencies of 26 pJ/pulse and 18.5 pJ/pulse. The standby leakage current measured 0.6 μA. Table 4.2 summarizes the UWB transmitter's performance and compares it to previously reported implementations.

Fig. 4.20 confirms the ability of the transmitter to generate multiple UWB pulses per bit. PRF of 20 MHz was used for this experiment.

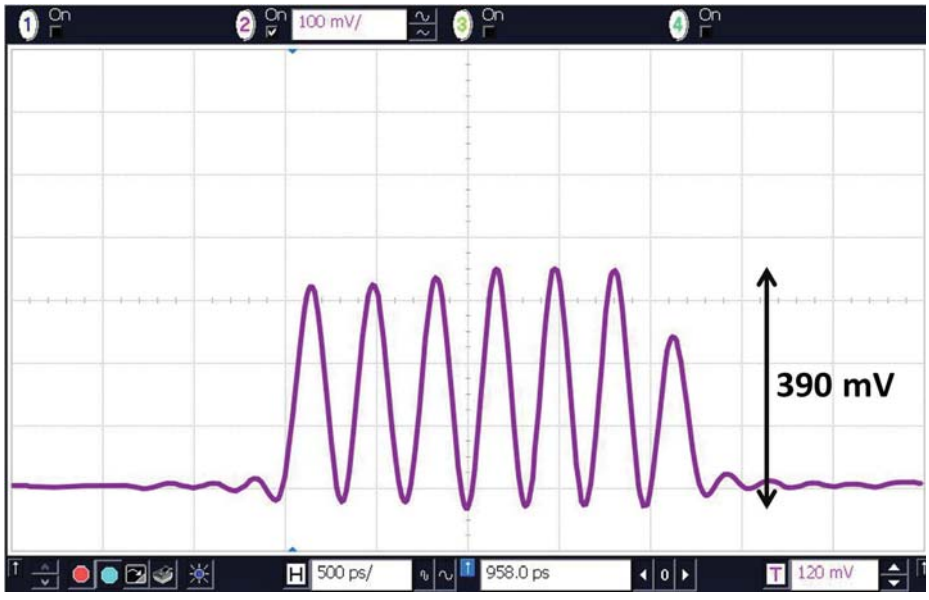


Fig. 4.18. UWB pulse in time domain.

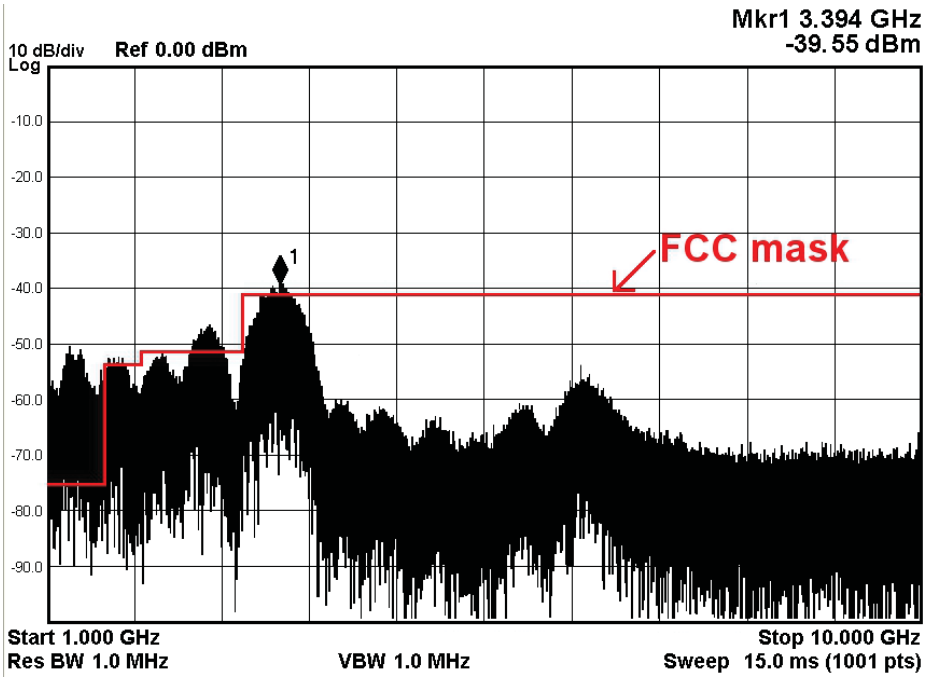


Fig. 4.19. UWB pulse in frequency domain.

Table 4.2: Summary of UWB transmitter's performance

	This work	**[76]**	**[100]**
CMOS Process	65 nm	65 nm	90 nm
Power Supply (V)	1.2	0.9	1
Silicon Area (mm^2)	0.005	0.032	0.07
Modulation	PPM	PPM+DB +BPSK	PPM+BPSK
PRF (MHz)	200	0 - 50	<15.6
Center Frequency (GHz)	3.1 - 5	3.1 - 5	3.1 - 10
Pulse Duration (ns)	2	0.7 - 2	63
Standby Power (μW)	0.72	170	123
Energy/Pulse (pJ/pulse)	19	8 - 16	40

The UWB receiver front-end described in section 4.4 was used to verify that the pulse-position modulated UWB signal can be down-converted back to the baseband. Fig. 4.21 captures the output voltage from the RF detector at 100 Mbps. Bit frames are indicated below the captured waveforms. The receiver front-end performed well up to 200 Mbps, although its sensitivity was estimated to be -55 dBm, resulting in the transmission distance being only a few centimeters.

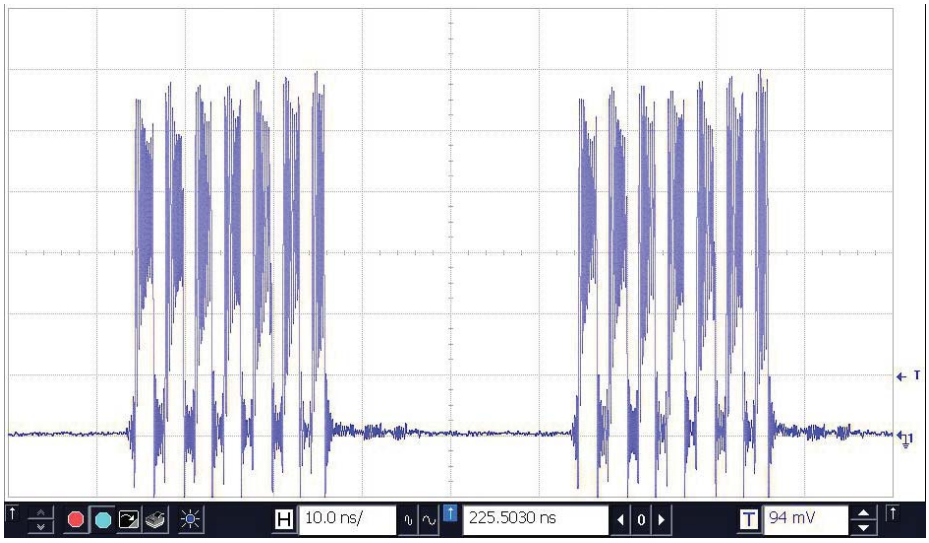


Fig. 4.20. UWB signal with multiple pulses per bit (PRF 20 MHz).

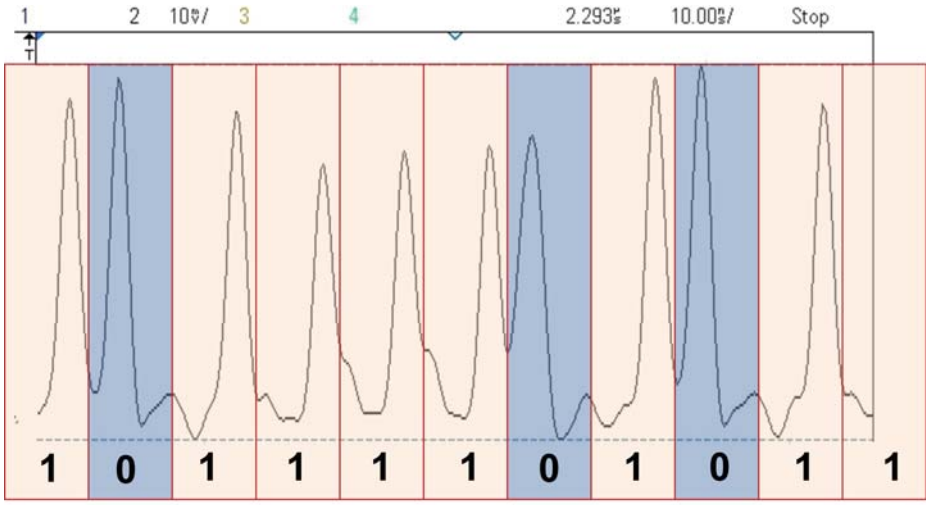


Fig. 4.21. Down-converted pulse-position modulated UWB signal. An impulse in the first half of the bit frame represents a logical "0". Impulse in the second half of the bit frame represents a logical "1".

4.6 Summary

A low-complexity fully digital I-UWB transmitter for biomedical implants requiring high data rates has been fabricated and characterized in a low power 65 nm CMOS process. The transmitter operates in the 3 - 5 GHz UWB frequency band and was designed using worst-case process corner evaluation and accurate modeling of package and board parasitics to ensure FCC compliance without a postprocessing calibration step. The proposed transmitter requires only 0.005 mm^2 of silicon area and consumes 0.6 μA static leakage current

making it suitable for implantable systems. Measured active energy efficiency is 19 pJ/pulse at 200 MHz pulse repetition frequency.

CHAPTER 5

UWB FOR NEOCORTICAL RESEARCH

5.1 Overview

The cerebral cortex, which is responsible for implementing intelligence and conscious behavior in humans, has become a subject of interest and intensive scientific research. Scientists have been trying to understand cortical activity and correlate it with specific tasks and behavioral features. The neocortex, which is the outer-most layer of the cortex with thicknesses ranging from 0.5 mm in the smallest mammals to 2 - 4 mm in humans, is involved in higher functions such as sensory perception, motor control, conscious thoughts, and language.

For several decades, scientists have been developing methods for recording and stimulating neural signals in mammals ranging from rats [101], cats [102], swine [103], monkeys [104], to humans [105]. Understanding the electrical signals in the human brain has the potential to significantly improve the quality of life of amputees, spinal cord injury victims, and those living with neuro-motor diseases.

Some research areas have developed advanced understanding of the electrical activities in the brain so that sophisticated signal processing can be embedded in an implantable device. The amount of data that needs to be transmitted from the implant is therefore significantly reduced, resulting in reduced power consumption by the implant. On the other hand, there are new research applications, such as the recognition of spoken words [9], that do not yet have defined signal processing algorithms and greatly benefit from having as much data from the brain as possible. In these applications, the power consumption of the wireless telemetry is typically the element that limits an experiment's run time. In addition to quickly draining the battery, increased power consumption also results in higher heat dissipation, which can cause irreversible brain damage in a test subject. Achieving wireless high-rate data transmission from the implanted devices at low power dissipation is therefore a challenge that needs to be addressed to support modern cortical research.

Another challenge of advanced neural research is achieving long-term system reliability and safety. Reliability is commonly compromised by the immune system rejecting any foreign material [106] and also by mechanical stress on fragile parts such as wired connections. Safety is typically jeopardized by infections at the tissue exposure sites. To address these issues, implants need to be as compact as possible, to be coated with biocompatible materials, and to have the ability to be chronically implanted without the need for wired connections going through the skin.

In neural recording systems, a partial solution to the reliability and safety issues is depicted in Fig. 5.1. This configuration has been used in experiments on guinea pigs [1]. The sensor array and front-end electronics are placed under the skull on the cortical surface. A bundle of microwires connects the electronics to a source of power and an RF transmitter, which are placed between the skin and skull. This approach effectively eliminates exposure of the raw tissue and reduces the chance of infections. The microwires, however, are a source of reliability issues. The next step to address the reliability issues will be to combine the power source and the RF link together with the sensor and the mixed-signal electronics into a single compact device that rests on the cortical surface, therefore eliminating the unreliable microwires. Such a system is depicted in Fig. 5.2. To design such a system, power efficient, high-data rate telemetry and high power density battery are needed.

Chapter 4 described a high-data rate UWB data transmitter that was designed for neural signal recording in laboratory animals. This chapter investigates the suitability of the UWB technology to be deployed in neural recording systems. Experimental data capturing the UWB signal transmission through an animal skull and skin are presented and evaluated

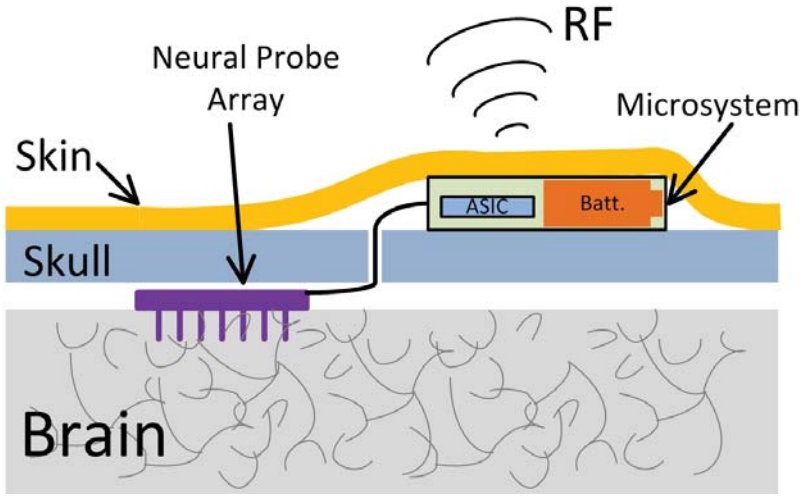


Fig. 5.1. BMI implementation with microwires.

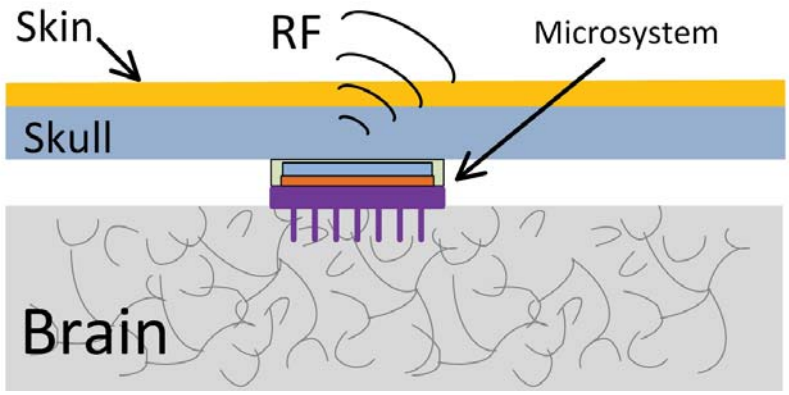


Fig. 5.2. BMI implementation eliminating microwires for improved reliability.

for three different configurations of the signal acquisition system. This experiment differs from all previously published studies in its use of miniature chip antennas as opposed to conventional size antennas typically used for indoor and outdoor UWB applications.

5.2 UWB Propagation Channel Modeling

The key difference between UWB propagation channels and conventional narrow-band channels is the frequency dependence of the transfer function. For the narrow-band channels, transfer functions cover frequency dependency in a very narrow (local) range. UWB channels, however, must cover a wide range of frequencies and show not only the local variations but also the variations of the averaged transfer function. These variations reflect the fact that different frequency components of the UWB signal experience different attenuation.

Furthermore, to accurately model UWB signal propagation, all channel effects such as free-space propagation, antenna gain, reflection, diffraction, and scattering must be modeled as frequency-dependent variables, which make deterministic computations very complex. To make the problem more tractable, a stochastic model can be used because it captures the essential channel properties without attempting to compute the exact behavior for each specific location. Statistical models for the path loss, shadowing, delay dispersion, small-scale fading, angular dispersion, and temporal channel variations have been developed and are summarized in [107].

Most of the published path loss models apply to indoor and outdoor line-of-sight (LOS) or non-line-of-sight (NLOS) environments. Their applicability to biomedical applications is limited, however, because they typically do not capture signal propagation through a stack of biological tissues such as skin, fat, muscles, and bones. Furthermore, the specificity of

each application prevents the definition of a universal model. For the purpose of evaluating the suitability of the Utah UWB transmitter for neocortical research, a simplified path loss model is developed.

5.3 Large-Scale Fading Model

In research experiments, data are typically transmitted via a direct LOS path and only over a short distance. As a result, many signal propagation effects such as multipath modeling often do not need to be considered. In contrast, signal propagation through multiple layers of organic tissues makes the deterministic approach to channel modeling a complex task. In this experiment, a simplified statistical model of large-scale fading effect is derived. Large-scale fading is the dominant cause of signal degradation in the neocortical experiment setup. Due to the statistical nature of the model, based on experimental data, it includes reflection, diffraction, and scattering. On the other hand, the model does not decouple any antenna effects, thus the applicability of the presented model is limited to experiments with miniature chip antennas.

Path loss is defined as the dB reduction in power from the transmitter to the receiver, where the received power is spatially averaged around the location. A general path loss formula has the form

$$PL(d) = PL_0 + 10 \cdot \gamma \cdot \log_{10}(\frac{d}{d_0}) + S \tag{5.1}$$

where PL_0 is the point at a reference distance d_0 (typically 1 m). γ is the slope of the average increase in path loss with distance. The variation S denotes a zero-mean Gaussian random variable with standard deviation σ.

Statistical path loss models for residential and commercial buildings have been presented in literature [108–110]. The authors of [111], for example, derived a model for an indoor residential LOS environment as:

$$PL_{|dB} = 46.6 + 10 \cdot 1.8\log_{10}(d) + 2.9 \tag{5.2}$$

This and most other published statistical models are designed to project the path loss at transmission distances larger than 1 m, which is typically not the case in research experiments on animals. Additionally, the published models cannot be easily modified to estimate the signal propagation through multilayered biological tissue. Extensive research has been done to characterize the dielectric properties of various body tissues [112]. Attenuation constants for those issues have also been previously derived [113]. Attenuation through

a stack of tissues, however, cannot be estimated as a simple addition of the attenuation constants of each tissue because of the signal distortion at each tissue interface caused by reflection and other boundary effects. In addition, conventional models are typically derived by using high-performance antennas. Biomedical applications, however, are usually restricted to miniature antennas coated in biocompatible materials and thus the antenna effects are difficult to predict and incorporate in the models. Because of the difficulties in using existing UWB channel propagation models, we have developed a model specific to neocortical research on swine. This model can be further modified and used for UWB transmission approximation in applications in primates or humans.

5.4 Experimental Setup

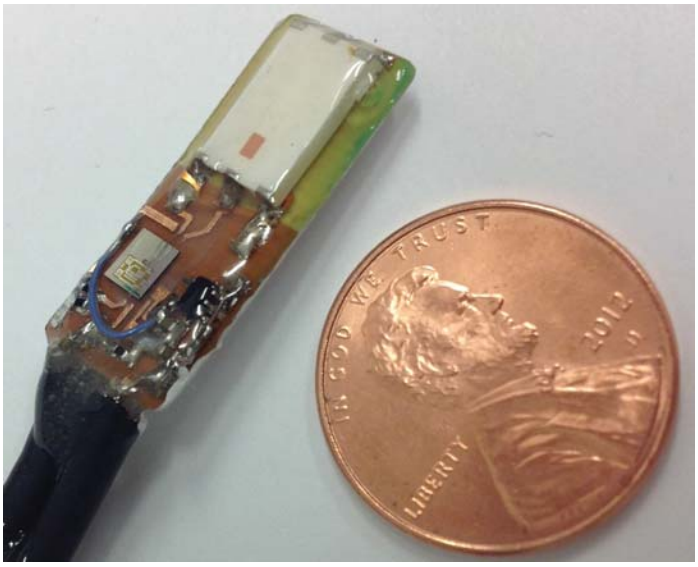
A bare silicon die containing the UWB transmitter described in Chapter 4 is manually wire-bonded to a printed circuit board and is connected to a miniature UWB antenna (Johanson Technology 3100AT51A7200). The transmitter is preprogrammed to continuously transmit UWB pulses at 20 MHz pulse-repetition-frequency (PRF). The transmitter is coated with a UV-cured biomedical silicone. Another UWB antenna is mounted on a PCB and coated with silicone to receive the UWB signal. The signal strength and spectrum are measured by a spectrum analyzer. The transmitter and antenna are depicted in Fig. 5.3.

The head of a domestic pig was purchased from a local butcher for this experiment. Thickness of the skull, periosteum, and skin were estimated at the location of the UWB transmitter. The stack is depicted in Fig. 5.4. Two experimental setups, corresponding to Fig. 5.5 and Fig. 5.6, were considered. The attenuation of the UWB signal received by the antenna at distance 0, 2, 6, 10, 14, and 20 cm from the head surface was recorded. The experiment was repeated for three UWB transmitters.

5.5 Experimental Data

Table 5.1 summarizes the center frequency, bandwidth, and radiated signal power measured for the three UWB transmitters used for this study. Table 5.2 and Table 5.3 capture the signal attenuation at various distances from the head for the transmitter locations under the skin and in the cranial cavity, respectively. Due to the noise floor of the spectrum analyzer used to measure the received signal power and the lack of a pre-amplifier, the maximum resolvable signal attenuation was approximately 32 dB. As a result, transmission distance over 20 cm was not measurable.

Two large-scale fading models were derived from Tables 5.2 and 5.3. The attenuation measured at distance 0 cm (head surface) was used as PL_0 and the attenuation slope γ



(a)

(b)

Fig. 5.3. Setup for large-scale signal fading experiment: (a) UWB transmitter and (b) UWB antenna coated with biocompatible silicone.

was calculated from the remaining data points. Fig. 5.7 shows the measured data with the corresponding models.

For the two configurations when (1) the UWB transmitter is implanted under the skin and (2) the transmitter is under the skull in the cranial cavity, the path loss models are

$$PL_{SKIN|dB} = 6.5 + 10 \cdot 2.5 \log_{10}(\frac{d}{d_0}) \tag{5.3}$$

$$PL_{SKULL|dB} = 19.5 + 10 \cdot 2.6 \log_{10}(\frac{d}{d_0}). \tag{5.4}$$

where the reference distance d_0 is 3 cm (head surface).

5.6 Key Findings

The experiment revealed that the UWB signal path loss in the neocortical research setup is substantial. Conventional models for UWB signal propagation in LOS and NLOS

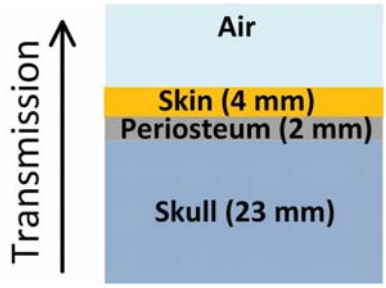


Fig. 5.4. **Multilayer stack of biological tissues in the transmission path.**

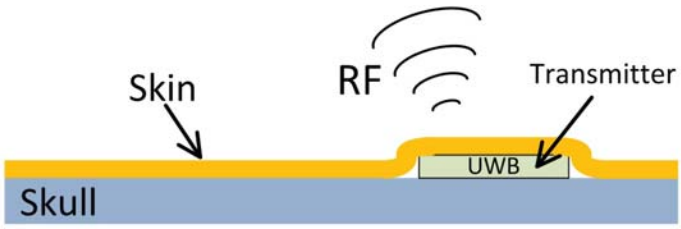


Fig. 5.5. **Neural recording system implanted under the skin.**

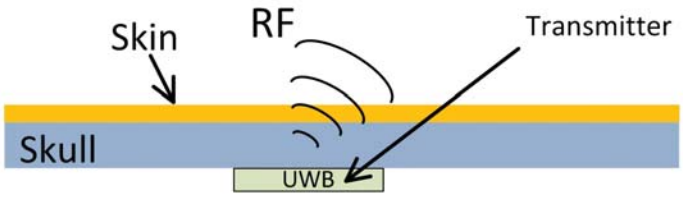


Fig. 5.6. **Neural recording system implanted in the cranial cavity.**

Table 5.1: **UWB transmitters' measured parameters.**

	Center Frequency	Bandwidth	Output Power
TX A	4.258 GHz	550 MHz	-41.05 dBm
TX B	4.132 GHz	600 MHz	-41.32 dBm
TX C	4.312 GHz	580 MHz	-41.58 dBm

environments are problematic to apply when miniature chip antennas are used to transmit signal through a stack of biological tissues. The path loss in LOS propagation in a residential environment has been modeled at approximately 47 dB at 1 m and an additional 18 dB at 10 m separation [111]. In our experiment, an attenuation of nearly 20 dB at 3 cm and 31 dB at 8 cm separation was measured in the configuration with the UWB transmitter implanted in the cranial cavity of a pig's head. Less attenuation was measured in the configuration

Table 5.2: **UWB signal attenuation for implant placed under the skin.**

Distance (cm)	TX A (dB)	TX B (dB)	TX C (dB)
0	7.9	5.5	6.2
2	10.1	8.1	9.5
6	17.9	14.9	15.6
10	22.4	19.2	22.9
14	29.4	25.2	27.9
20	N/A	31.3	32 (18 cm)

Table 5.3: **UWB signal attenuation for implant placed under the skull.**

Distance (cm)	TX A (dB)	TX B (dB)	TX C (dB)
0	21.2	18.7	19.3
2	25.3	22.3	23.3
5	32.2	29.6	30.9

with the transmitter placed just under the skin. Despite the high attenuation of the UWB signal, however, the experiment revealed that the UWB technology may, indeed, be useful in specific configurations of neocortical experiments. The derived models of large-scale fading are valuable for evaluating possible configurations and defining the required performance of UWB receiver.

Although there is currently no commercially available UWB receiver supporting pulse-position-modulation and data rates up to 200 Mbps, several receiver architectures have been described and presented in literature. A 3.1 - 5 GHz UWB receiver with a sensitivity of -99 dBm at 10^{-3} BER was presented in [87]. Another UWB receiver for insect motion control with a sensitivity of -76 dBm was presented in [81]. A UWB receiver based on super-regenerative principle with a sensitivity of -91.3 dBm is proposed in [114]. As Fig. 5.8 indicates, the high-performance receivers would be able to recover the UWB signal approximately 1.6 m away from the pig's head if the transmitter is under the skull, or 3.5 m if it is under the skin only. This would be a sufficient range for most experimental applications on small caged animals. The achievable distance, however, would become shorter with increasing data rates. This is a limitation of the UWB transmitter's applicability. However, enhancements in signal strength can be achieved by using a high-gain receiving antenna, which is easily achievable since the receiver is detached from the animal and typically is not restricted in size and weight. Furthermore, the signal strength could also be enhanced

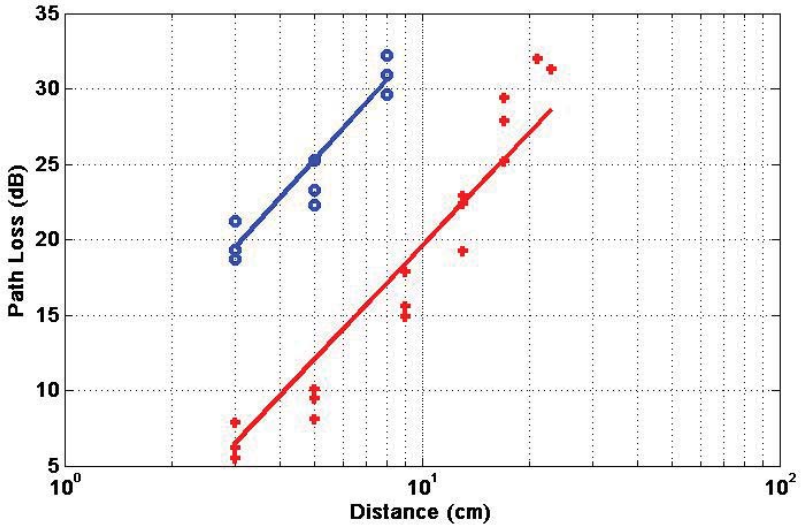


Fig. 5.7. Path loss vs. transmission distance.

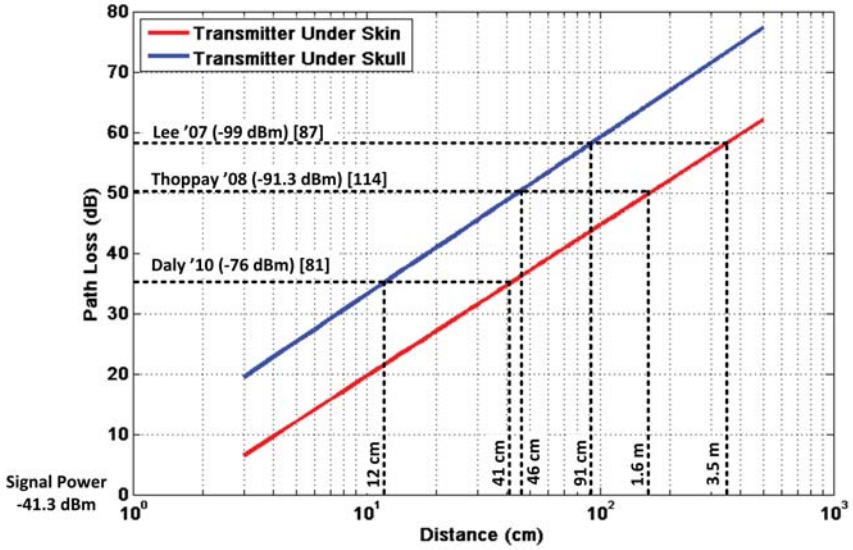


Fig. 5.8. Achievable transmission distance considering recently reported UWB receivers.

by improving impedance matching of the transmitting antenna, which is affected by tissue loading.

Alternatively, a system configuration that would take advantage of the high achievable data rates and low power consumption offered by the UWB technology is proposed in Fig. 5.9. In this scenario, an intermediate transceiver is placed on the animal's head. The low-power high-data rate UWB signal is received in the transceiver and data are forwarded

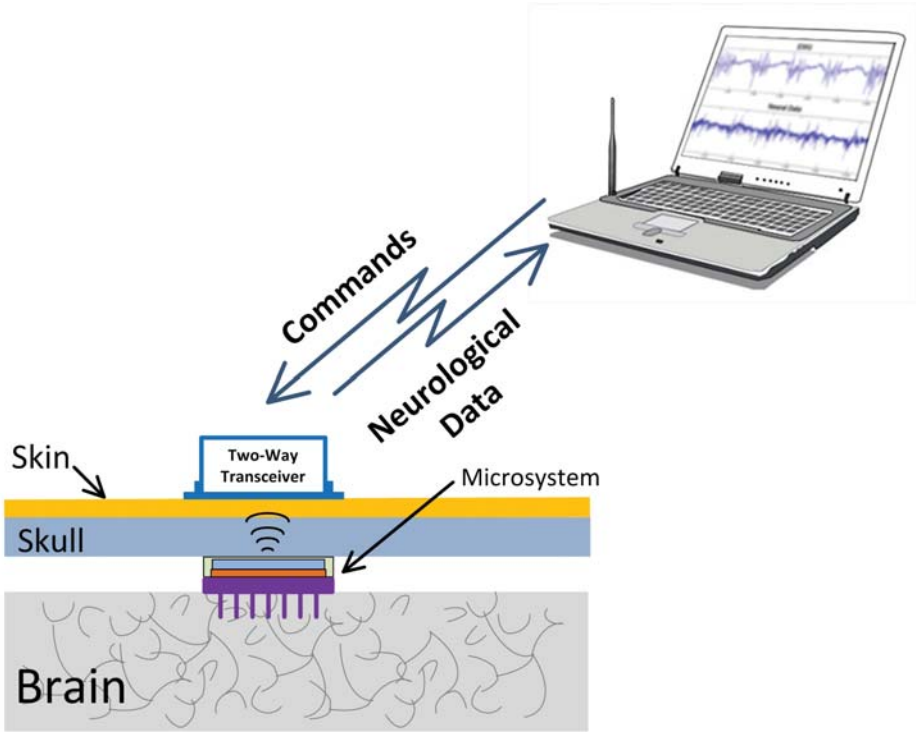


Fig. 5.9. Proposed implantable system configuration with an intermediate transceiver.

over a larger distance via another data link. The benefit of this configuration is that a large transmission area can be covered while the implant can be designed to be smaller and to operate longer. An energy source for the transceiver can be replaced relatively easily since it is not implanted.

Another useful projection that can be made from the derived models is for the use of the UWB transmitter in primates. The skulls of primates are significantly thinner (2.6 mm in Rhesus monkey and 6.9 mm in humans [115]) then the skull of domestic pigs (23 mm). Therefore, the UWB signal would experience considerably less attenuation, resulting in a wider achievable range.

5.7 Summary

In this chapter, we presented a practical evaluation of the Utah UWB transmitter in neocortical research. Two experimental configurations were evaluated mimicking a neural activity monitoring system that is conventionally implanted in swine. The experiment was performed in a laboratory setting using the head of a domestic pig. The main goals of the experiment were (1) to evaluate the strength of the UWB signal after propagating from the cranial cavity through the pig's skull and skin; (2) to develop a statistical model of

large-scale signal fading, which is the dominant source of signal degradation; and (3) to use the developed model to evaluate the system performance with recently published UWB receivers.

The experiment confirmed that high-frequency signals experience high absorption rates in biological tissues. Moreover, using miniature low-gain antennas that are suitable for implantation further deteriorates the system's performance. These effects make the deployment of UWB technology in neocortical research on swine (or other animals with thick skulls) challenging as the separation between the transmitter and receiver must be short. The experimental data along with the derived path loss models, however, indicate that the UWB technology is suitable for research experiments on primates, due to their thinner skulls.

The performance of the UWB link could be improved by employing high-sensitivity receivers with high-gain antennas, therefore enabling experiments on caged animals with thick skull. An effort should also be made to improve impedance matching of the implanted antenna. The antenna impedance is affected by tissue loading, therefore resulting in additional signal losses. Ideally, a custom-designed antenna should be used for the implant. Furthermore, if long transmission distances are required, an intermediate RF transmitter on the surface of the animals' skull can be deployed. This arrangement allows the researchers to take advantage of the high data rate and low power consumption properties of the UWB technology.

CHAPTER 6

CONCLUSION AND FUTURE STUDY

6.1 Summary of Contributions

As research and clinical applications for biomedical implants become pervasive, it is clear that low-power and untethered operation are indispensable features of such electronics. Furthermore, the multidisciplinary nature of advanced biomedical research makes sensor interfaces essential to the implants. Size restrictions call for high levels of integration in the mixed-signal electronics. Sophisticated new algorithms must be developed to perform real-time data processing in the implants; therefore, significant computational power is essential. In addition to advanced sensing and computing, *in vivo* experiments often must facilitate chemical reactions to support specific bodily processes.

In the past, development of microsystems for biomedical research has almost always required custom SoC design to meet the desired specifications and performance. The cost of development and length of time required to design custom SoCs, however, often hinder biomedical research. In this work, a custom-designed SoC with the capability of interfacing with a wide spectrum of common electrochemical sensors, driving redox chemical reactions, and performing complex computations was designed, fabricated, and tested [116]. The microcontroller is also able to store and wirelessly transmit experimental data through an energy efficient ultra-wideband (UWB) link. Additionally, the microsystem's secondary battery can be wirelessly recharged through a near-field inductive link.

Test results indicate that all designed functional blocks performed adequately and the microsystem can be connected to common resistive sensors, conductivity sensors, and ion-selective-electrodes. Integrated output amplifiers were tested to drive sufficient currents to support a range of redox reactions. The microsystem is highly modular and can be configured to implement applications such as the electromodulated release of nitric oxide to prevent blood clotting and biofilm growth on catheters, and the smart intra-vaginal ring for AIDS-prevention research. Future iterations of this benchmark work could be optimized

for higher converter accuracy, conversion speeds, and/or number of channels to serve in a wider range of experiments.

The primary focus of this work was the development of an ultra-wideband signaling technology for energy efficient, high and low data rate wireless transmission. UWB is uniquely appropriate for biomedical implant communications because of the amount of available bandwidth and the ability to design a power-efficient transmitter at the expense of increased resource demand in the receiver. In biomedical applications, devices are mostly needed for transmitting data out of the body and resources on the receiving side are virtually unlimited.

An all-digital UWB transmitter has been presented that exploits the wide available bandwidth of UWB specifications and worst-case design techniques to eliminate the need for center frequency trimming and calibration. As a result, a low-complexity design with reduced leakage current has been achieved [117]. A detailed analysis of external parasitics introduced by circuit board traces and power supply connections has been performed. Close agreement between simulations and silicon testing has been achieved, resulting in reliable FCC compliance. Due to the fully-digital architecture, power in the transmitter is only consumed in the form of leakage currents and CV^2 switching losses. Furthermore, there is no analog bias current and the transmitter has an instantaneous startup, which enables easy duty-cycling. The Utah microcontroller achieves high data rates, supporting demanding applications. Concurrently, low effective data rates and proportionally reduced power consumption can be achieved by storing experimental data in the integrated 32 kB SRAM and duty-cycling transmission.

Test results confirm that data rates of 200 Mbps are achievable at energy per bit of 19 pJ/pulse. Measured performance of the UWB transmitter presented in this thesis is compared to previously published transmitters with similar design goals in Fig. 6.1. The silicon area and standby current, which are critical to implantable electronics, are the lowest among the compared designs.

The suitability of the proposed UWB transmitter for neocortical research was also investigated. The transmitter was inserted in the cranial cavity of a domestic pig and the UWB signal strength was measured at various distances from the head. A statistical model of large-scale fading was developed and its extrapolation was used to evaluate recently published UWB receivers. The performed experiment indicates that the UWB signal attenuation through the pigs head is significant, restricting the distance for reliable transmission to only a few centimeters when miniature chip antennas are used. On the other hand, the test results indicate that a transmission distance of several meters is achievable

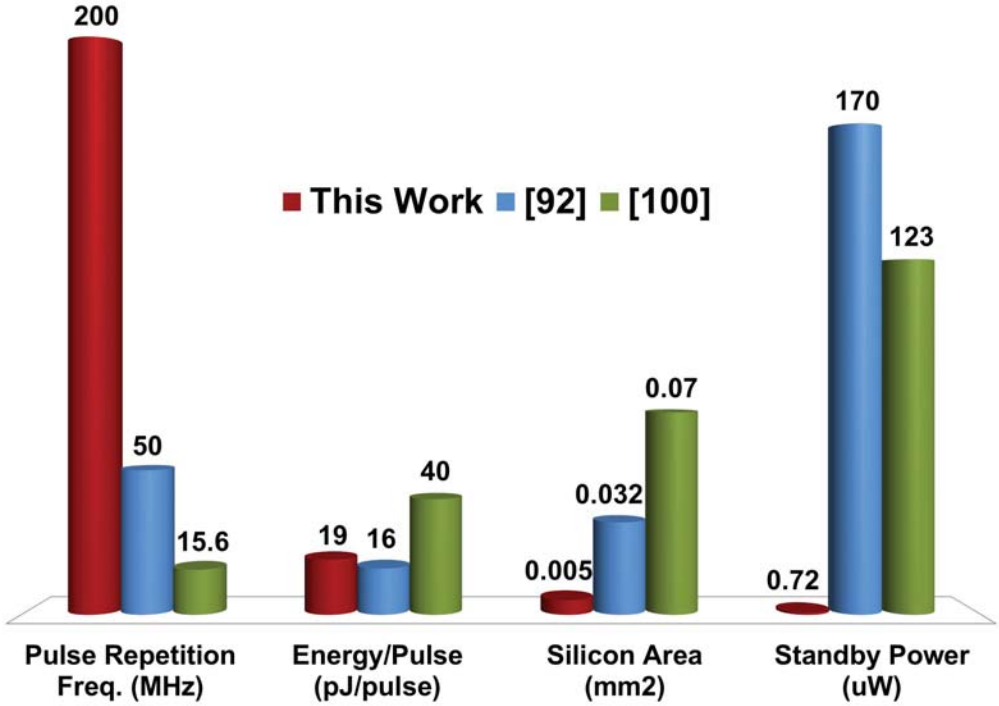


Fig. 6.1. UWB transmitter performance comparison.

in experiments on primates, which have significantly thinner skulls than domestic pigs.

6.2 Future Work

Implantable devices with the ability to interface a wide spectrum of sensors and actuators will continue to be critical for biomedical research. High computational power, data storage capability, wireless connectivity, and RF powering are required to perform experiments on untethered animals. In the past, almost every implant required a custom-designed chip as off-the-shelf components would not meet its specific requirements. This work demonstrates a single-chip microcontroller with enough features that it will cover a significant set of biomedical applications.

The mixed-signal microcontroller presented in this work offers a set of interfaces that are tailored to the most commonly used electrochemical sensors. Resistive, potentiometric, and conductivity sensors can be connected directly to the microcontroller. Frequently used two-electrode voltametric methods such as chronoamperometry, linear sweep voltammetry, and cyclic voltammetry are also possible with the Utah microcontroller. The SoC, however, currently lacks the ability to implement a three-electrode system that would allow addition of a reference electrode to the electrochemical cell [118]. Future generations of the Utah SoC

would benefit from implementation of a potentiostat circuit, which would enable interfacing to more types of sensors and actuators.

In terms of the RF powering of the microsystem, basic functionality has been implemented in this generation of the SoC. However, the existing inductive link only allows recharging of the secondary battery with a constant voltage, which must be regulated by adjusting the external RF source. Most batteries, however, recommend a constant-current recharging method; therefore, future revisions of the SoC design should include such functionality.

Furthermore, many research applications would benefit from forward and backward telemetry through the inductive link. Although the integrated UWB transmitter offers an excellent backward communication capability, utilizing the inductive link would be a great option for low data rate applications. Data transfer via the inductive link is virtually free, in terms of power consumed in the implant. Forward telemetry would also greatly improve the system as it could be wirelessly reconfigured after being implanted. For most applications, forward telemetry with data rates on the order of several kbps is usually sufficient and can be achieved by frequency or amplitude modulation of the RF signal. Future revisions of the microcontroller should include circuits to support both forward and backward telemetry through the inductive link.

6.3 Conclusion

Integrated microsystems will undoubtedly play an increasingly important role in biomedical research. Low-power autonomous implants, capable of long-term operation, will be necessary to explore new concepts in medicine and validate emerging technologies. This work demonstrates a single-chip microcontroller that is suitable for a wide range of applications requiring electrochemical sensing, high computational power, wireless connectivity, and low-power operation. The custom designed System-on-Chip (SoC) includes interfaces for a wide range of commonly used electrochemical sensors and contains peripherals that can drive chemical reactions by setting the appropriate voltages or currents across electrodes.

The system enables battery powered experiments on untethered animals. It runs from a primary or secondary battery that can be recharged via two inductively coupled coils. The SoC includes a 16-bit microprocessor with an optimized instruction set and 32 kB of on-chip SRAM. The integrated microsystem has been fabricated in a 65 nm CMOS technology and the silicon has been fully tested, confirming the functionality of the integrated peripherals. Included are two sigma-delta analog-to-digital converters, two 10-bit digital-to-analog converters, two programmable current sources, and a sleep mode timer.

Wireless data transmission from the implant is realized via a UWB link which is designed to meet the needs of applications requiring high data rates up to 200 Mbps. Due to the fully-digital implementation of the transmitter, its power consumption can be scaled proportionally to the data rates by buffering data in the integrated SRAM memory and duty-cycling the transmission. A design methodology resulting in the UWB transmitter achieving FCC compliance without conventional calibration techniques is also described.

Furthermore, a statistical model of large-scale UWB signal fading in neocortical experiments on swine is experimentally derived. Extrapolation of the model confirms suitability of the UWB technology for neural recording on primates and other caged animals.

APPENDIX

ELECTROCHEMICAL SENSORS - CHARACTERIZATION

As described in Chapter 3, electrochemical sensors are frequently used for advanced biomedical and chemical research. Many electrochemical methods have been well defined and are routinely deployed in laboratory (bench-top) instruments. Implantable electronics, however, bring new challenges such as the need for miniaturization, autonomous long-term operation, and overcoming limited electrical power availability. Additionally, only biocompatible, nontoxic chemicals can be used in experiments on animals or humans.

One of the intended applications of the Utah microcontroller is the Smart Intra-Vaginal Ring (S-IVR), described in Chapter 2.3. In this application, conductivity, pH, and temperature of the surrounding environment need to be measured with high accuracy for a period of one month. Although the measurements of these three parameters have been routinely done in laboratories for several decades, the size of the S-IVR implant requires an unprecedented level of miniaturization. All three sensors must be implemented on an area no larger than a few mm^2. To achieve this level of miniaturization, our group has been working with a sensor miniaturization leader, e-SENS, Inc., located in Salt Lake City, Utah. e-SENS is commercializing miniature solid-state sensors for potable water quality monitoring. The sensors' size, low cost, and maintenance-free operation makes them ideal for implanted devices such as the S-IVR.

Fig. A.1 depicts the layout of the e-SENS' sensor array used for water analysis. The sensor die are fabricated on standard silicon wafers and each die is 4 mm x 5.5 mm in size. Each die contains ten electrochemical sensors: temperature, conductivity, five potentiometric sensors, two amperometric sensors, and an oxidation-reduction potential (ORP) sensor. Ion-selective electrodes (ISEs), for such analytes as pH, CO_2, and calcium are types of potentiometric sensors and are formed by deposition of proprietary chemical solutions in the circular structures visible in the array photograph.

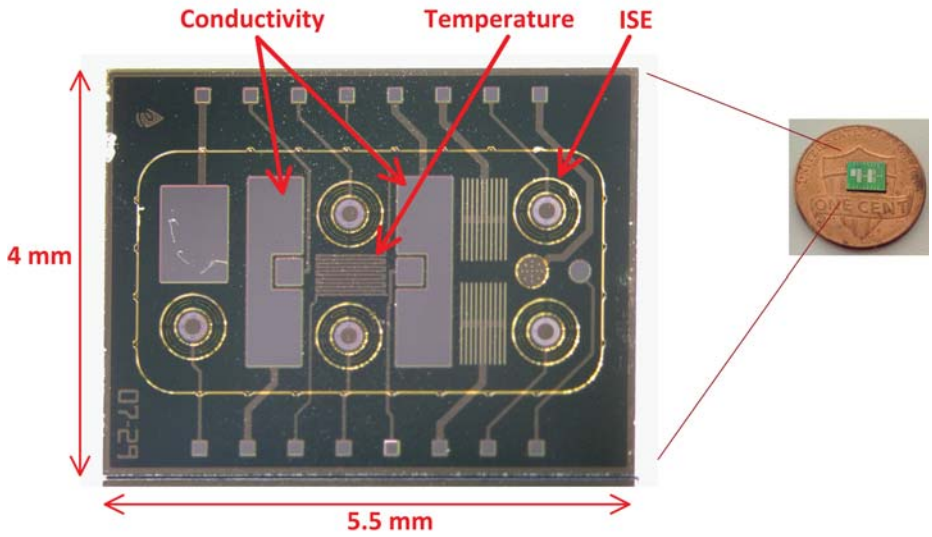


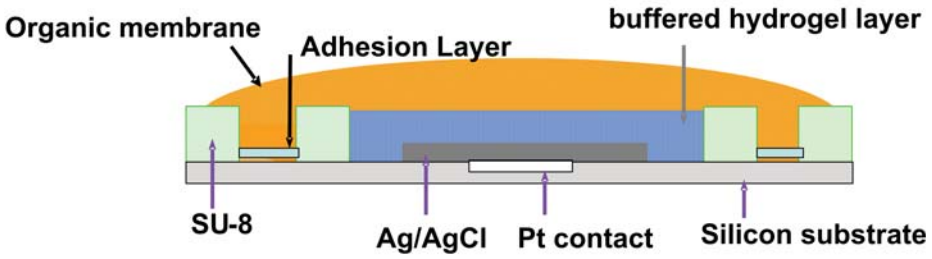
Fig. A.1. Miniature sensor array developed by e-SENS for water quality analysis.

Since the S-IVR application requires only three sensors (pH, temperature, conductivity), the size of the die could be significantly reduced. The projected size for the S-IVR sensor array is approximately 4 x 3 mm^2, thereby making the e-SENS technology suitable for the application. With the generous support of e-SENS, which provided sensors to our group free of charge, the pH, temperature, and conductivity sensors we characterized and results are presented in the following paragraphs.

A.1 pH Sensor

A cross section of the pH sensor is shown in Fig. A.2 It is a miniature implementation of the generic ISE described in section 3.1.2. A buffered hydrogel layer is deposited over an Ag/AgCl layer, forming the sensor's internal electrode. An organic membrane (responding to changes in pH) is dispensed over the hydrogel layer. When the sensor is hydrated, osmotic pressure develops in the hydrogel and could reach levels that detach the membrane from the sensor, resulting in sensor failure. To prevent this, an adhesion layer is formed between two co-axial rings that are lithographically etched from a rigid material such as SU-8 [119]. The layer prevents the membrane from peeling off and thus extends the sensor's lifetime.

Fig. A.3 is a calibration curve taken from the e-SENS sensor. It shows a linear response between a pH of 4 and 10, which exceeds the requirements of the S-IVR application. The slope of the response was measured at -59.6 mV/pH, which is close to the theoretical Nernst slope of -59.16 mV/pH. The membrane's output potential range was measured between ±350 mV for all tested sensors and conditions, which is well within the input range of the



Source: e-SENS, Inc.

Fig. A.2. Miniature solid-state pH sensor developed by e-SENS.

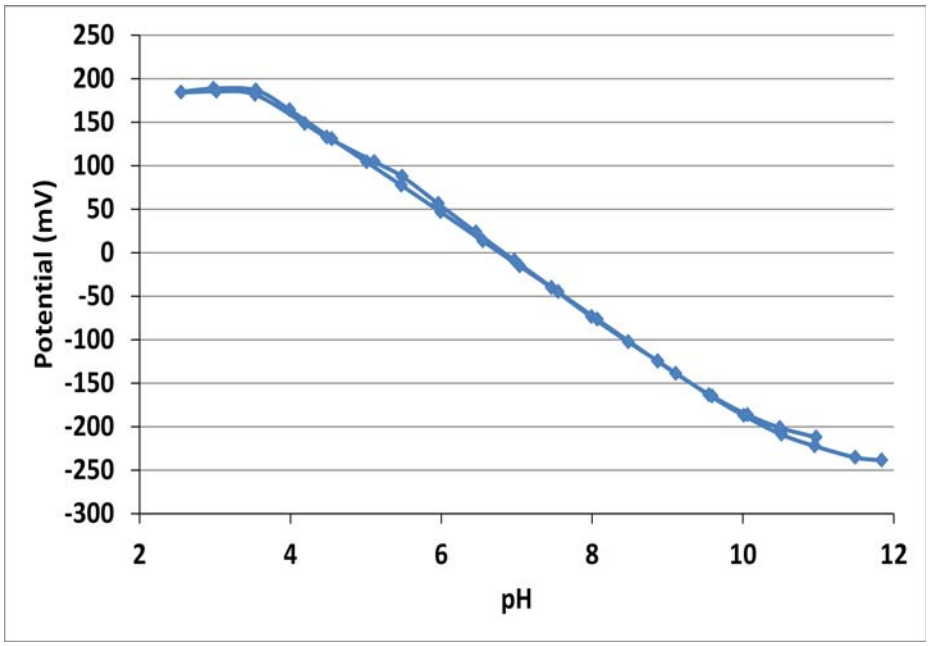


Fig. A.3. Measured calibration curve for e-SENS solid-state sensor.

Utah microcontroller. Experiments also revealed that the sensor is functional for at least 30 days with a maximum error of 5 %.

A.2 Temperature Sensor

The temperature sensor is formed by a thin trace of platinum, which is deposited on an oxidized silicon substrate. The platinum is subsequently covered with a layer of silicon nitride (Si_3N_4) to create a water-resistant separation barrier from the surrounding environment. The sensor is designed with a nominal resistance of 635 Ω. Fig. A.4 shows a measured calibration curve, confirming the sensor's functionality and sufficient linearity. The slope of the sensor's transfer function is approximately 1.5 Ω/C.

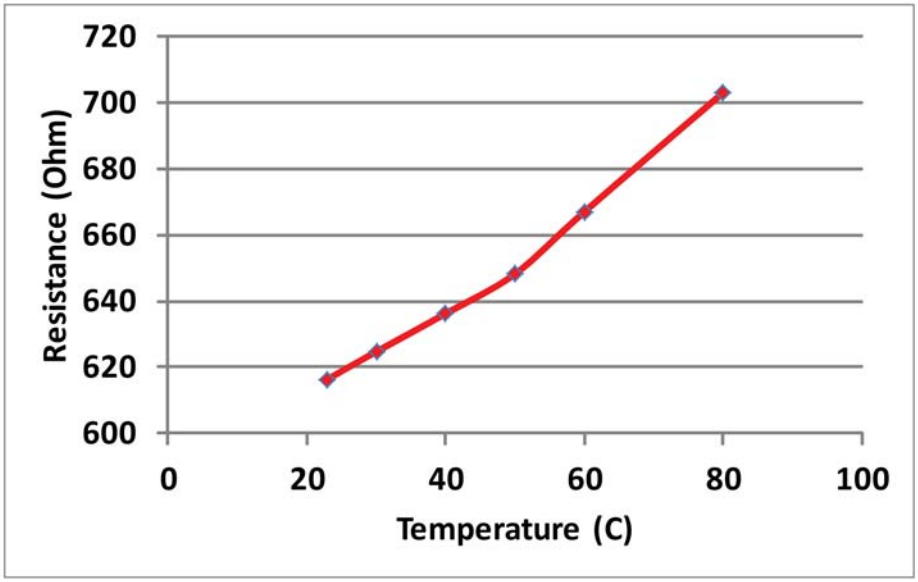


Fig. A.4. Temperature sensor calibration curve.

A.3 Conductivity Sensor

There are two commonly used types of conductivity sensors; two- and four-electrode. Both sensor types are usually driven with an AC signal to minimize electrode polarization. The four-electrode sensors are typically less sensitive to electrode polarization and thus exhibit better accuracy. The e-SENS sensor array has implemented the four-electrode conductivity sensor. In this configuration, one pair of electrodes (outer large electrodes) is driven with a known AC current and an AC voltage is measured over the second pair of electrodes (inner smaller electrodes). The conductivity of the solution is calculated:

$$Conductivity = \frac{I \cdot K_{cell}}{V} \tag{A.1}$$

where I is the applied AC current, V is the measured AC voltage, and K_{cell} is the cell constant in cm^{-1} that can be calculated:

$$K_{cell} = \frac{l}{A} \tag{A.2}$$

where l is the distance in cm between the electrodes and A is the area in cm^2 of the electrodes.

For sensor characterization purposes, a 1 kHz AC current generator with programmable amplitude was built from commercial components. The generator was used to drive the two large electrodes and the voltage across the two small electrodes was captured with an ADC. Sodium chloride was repeatedly added to deionized water to sweep its conductivity

from 47 μS/cm to 2400 μS/cm. A laboratory conductivity meter (Hach HQ 14d) was used as a reference. The observed calibration curve is depicted in Fig. A.5, revealing the sensor's maximum error of less than 5 % vs. the commercial instrument in the measured range.

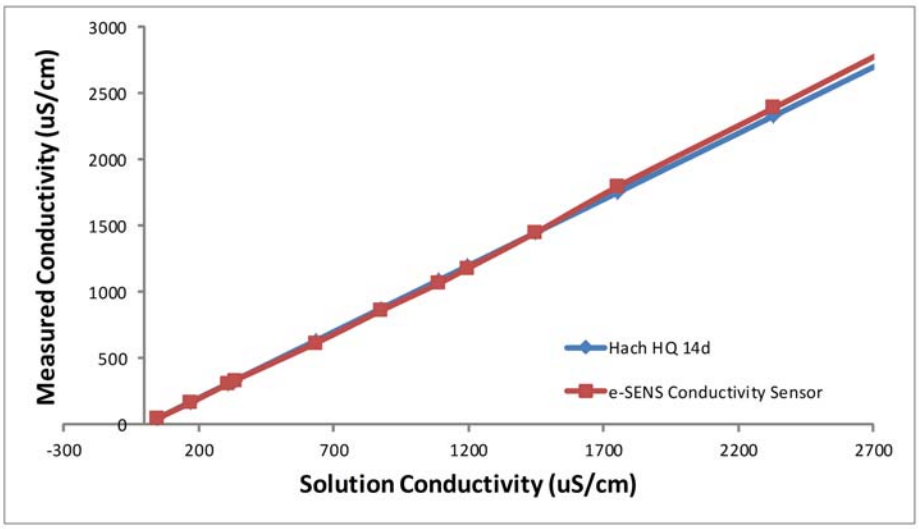


Fig. A.5. Conductivity sensor calibration curve.

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